EM7A8620

Voice over IP

Product Specification

DOC. VERSION 1.0

ELAN MICROELECTRONICS CORP.

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Specification Revision History		
Version	Revision Description	Date
1.0	Preliminary version	2006/03/08

1. Introduction

The EM7A8620 is a high integrated and high-performance ASIC. It integrated with the high performance 32-bit RISC CPU, 16-bit high quality audio Codec and two 802.3 Ethernet PHYs. The ASIC also built in a number of on-chip communications peripherals, like I2S/ I2C/PCM Bus/SPI/UART…etc. This is ideal chip to be integrated into Voice over IP or Adapter phone solution.

1.1 Feature

-32-bit RISC Embedded processor

- 32-bit RISC with 16KB I-Cache/16KB D-Cache
- Memory Management Unit

-System Bus

- AMBA-AHB bus
- AMBA-APB bus

-Components on AHB bus

- SDRAM Controller
- Static Memory Controller
- Two 10/100 Ethernet MAC controllers and PHYs
- Direct Memory Access Controller
- Unified memory bus interface

-Components on APB bus

- I^2C Controller
- 16550-compatible UART
- Three I^2S/SPI Controller
- Embedded audio CODEC
- PCM Controller
- Two 6-ch Internal Timer
- Watch Dog Timer
- 64-ch Interrupt Controller
- LCD (dot matrix) controller interface
- 32-bit General Purpose I/O (GPIO)

-Power & Clock Management

- Embedded PLL for programmable clocks
- Frequency: As high as 196 MHz for CPU at commercial conditions

-Operation Voltage

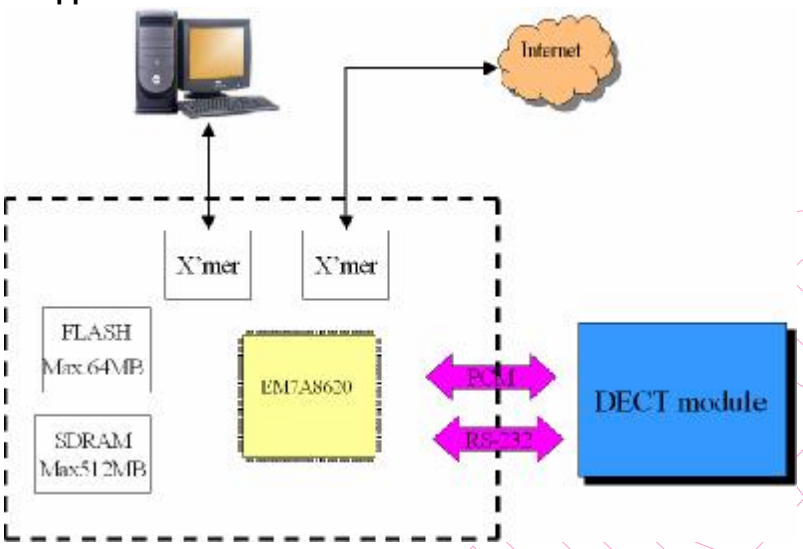
- 1.8V for Core
- 3.3V for Input/Output

-Package Type:

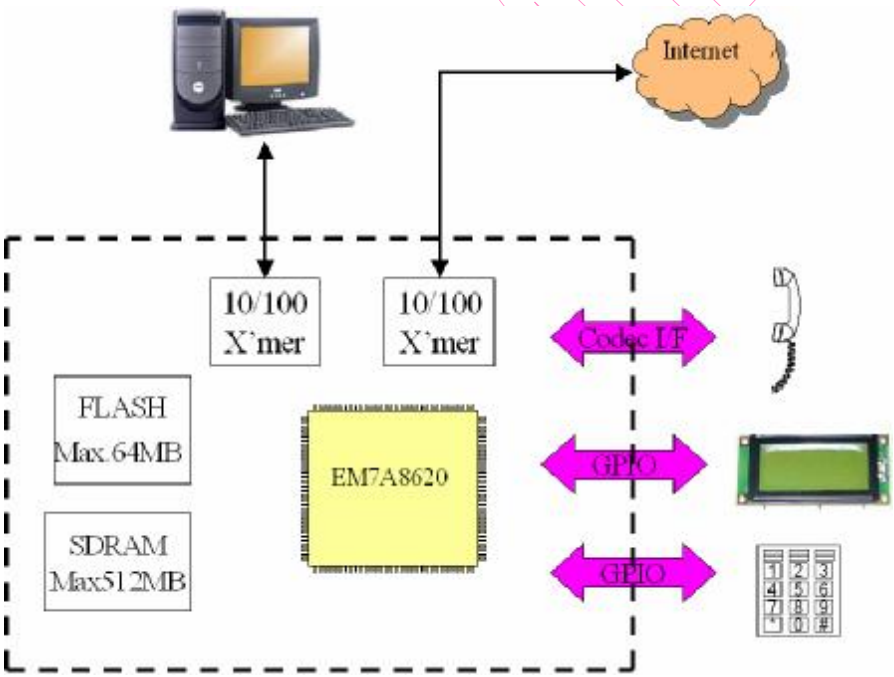
- 208-QFP

1.2 APPLICATION

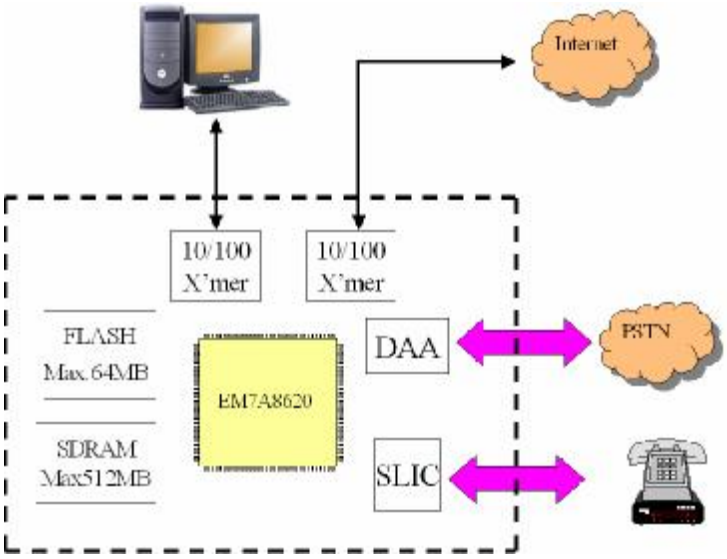
-DECT Application



-VOIP Phone



-VOIP Adapter



1.3 Signal Descriptions

Table 1 Signal Descriptions for the VoIP ASIC Processor

Pin name	Dir	Description
SDRAM/SRAM Address/Data Bus		
MEMADDR[25] / LCD_E	O	SRAM address bit-25 / LCD controller, register select
MEMADDR[24] / LCD_RS	O	LCD controller, read/write start
MEMADDR[23] / LCD_RWn	O	SRAM address bit-24 / LCD controller, read/write command
MEMADDR[22:15] / LCD_DB[7:0]	IO	SRAM address bit-23 to bit-16 / LCD controller, data bus bit-7 to bit-0
MEMADDR[14:0]	O	SDRAM/SRAM Memory address bus.
MEMDATA[31:0]	IO	SDRAM/SRAM Memory data bus.
SDRAM_CKE	O	SDRAM clock enable.
SDRAM_RASn	O	SDRAM row address strobe. Active LOW.
SDRAM_CASn	O	SDRAM column address strobe. Active LOW.
SDRAM_CSn	O	SDRAM chip select. Active LOW.
EBI_WEn	O	SDRAM/SRAM write enable. Active LOW.
EBI_BEn[3:0]	O	SDRAM DQM for data bytes 3 through 0.
SDCLK	O	SDRAM clocks.
SMC_CS0n	O	SRAM chip select
SMC_OEn	O	SRAM output enable
ICE		
ICK / GPIO[29]	IO	ICE clock input / GPIO bit-29
IMS / GPIO[28]	IO	ICE mode select / GPIO bit-28

ID / GPIO [27]	IO	ICE data / GPIO bit-27
EXTGOICE / GPIO[26]	IO	ICE enable / GPIO bit-26
GPIO		
GPIO[25:0]	IO	General purpose I/O
PCM		
PCM_TXD	O	PCM transmit data
PCM_RXD	I	PCM receive data
PCM_FSYN	IO	PCM frame sync.
PCM_BCLK	IO	PCM bit clock
SPI/I^{2}S		
SSP[1:3]_SCLK	IO	SPI bit clock
SSP[1:3]_FS	IO	SPI frame sync
SSP[1:3]_RXD	I	SPI RX
SSP[1:3]_TXD	O	SPI TX
SSP_CLKOUT	O	I^{2}S main clock
I^{2}C		
SCL	IO	I^{2}C clock.
SDA	IO	I^{2}C data.
UART		
SIN / GPIO[31]	I	Full function UART receive.
SOUT / GPIO[30]	O	Full function UART transmit.
Global Reset		
RSTn	I	Hardware reset.
Oscillator Pad		
OSCHIN	I	12 MHz crystal input.
OSCHIO	IO	12 MHz crystal output.
Ethernet PHY 1		
PHY1_RXIP	IO	Differential signal pair RX
PHY1_RXIN	IO	Differential signal pair RX
PHY1_TXOP	IO	Differential signal pair TX
PHY1_TXON	IO	Differential signal pair TX
PHY1_XTLP	I	Crystal input
PHY1_XTLN	I	Crystal input
PHY1_VCCA0	I	VCCA set 0
PHY1_GNDA0	I	GNDA set 0
PHY1_VCCD2	I	VCCD set 2
PHY1_GNDD2	O	GNDD set 2
PHY1_VCCA3	IO	VCCA set 3
PHY1_GNDA3	I	GNDA set 3
PHY1_RSET_BG	O	12.3 KΩ to GND
PHY1_LINKLED	O	LED signal indicates the link status
PHY1_SPDLED	O	LED signal indicates the 10/100 speed

Ethernet PHY 2		
PHY2_RXIP	IO	Differential signal pair RX
PHY2_RXIN	IO	Differential signal pair RX
PHY2_TXOP	IO	Differential signal pair TX
PHY2_TXON	IO	Differential signal pair TX
PHY2_XTLP	I	Crystal input
PHY2_XTLN	I	Crystal input
PHY2_VCCA0	I	VCCA set 0
PHY2_GNDA0	I	GNDA set 0
PHY2_VCCD2	I	VCCD set 2
PHY2_GNDD2	O	GNDD set 2
PHY2_VCCA3	IO	VCCA set 3
PHY2_GNDA3	I	GNDA set 3
PHY2_RSET_BG	O	12.3 KΩ to GND
PHY2_LINKLED	O	LED signal indicates the link status
PHY2_SPDLED	O	LED signal indicates the 10/100 speed
Audio CODEC		
CODEC_GNDA_HP	I	Headphone amplifier analog ground pad
CODEC_RHPOUT	O	Analog head phone, right channel
CODEC_LHPOUT	O	Analog head phone, left channel
CODEC_VCCA_HP	I	Headphone amplifier analog power pad, 3.3V
CODEC_MICIN	I	Analog microphone input
CODEC_LLINEIN	I	Analog line input, left channel
CODEC_RLINEIN	I	Analog line input, right channel
CODEC_VCCA	I	Analog power pad, 3.3V
CODEC_VCM	O	Analog common-mode voltage
CODEC_GNDA	I	Analog ground pad
CODEC_ROUT	O	Analog line out, right channel
CODEC_LOUT	O	Analog line out, left channel
DLL		
HCLK	I	DLL feedback clock
Test		
TEST	I	1: test mode, 0: normal mode
DLL / PLL / OSC Power		
VCC18A_PLL[1:2]	I	PLL analog power (1.8V).
GNDA_PLL[1:2]	I	PLL analog ground
VCC18A_DLL	I	DLL analog power (1.8V).
GNDA_DLL	I	DLL analog ground
VCC18IO_OSC	I	OSCH power (1.8V).
GNDIO_OSC	I	OSCH ground

1.4 System Block Diagram

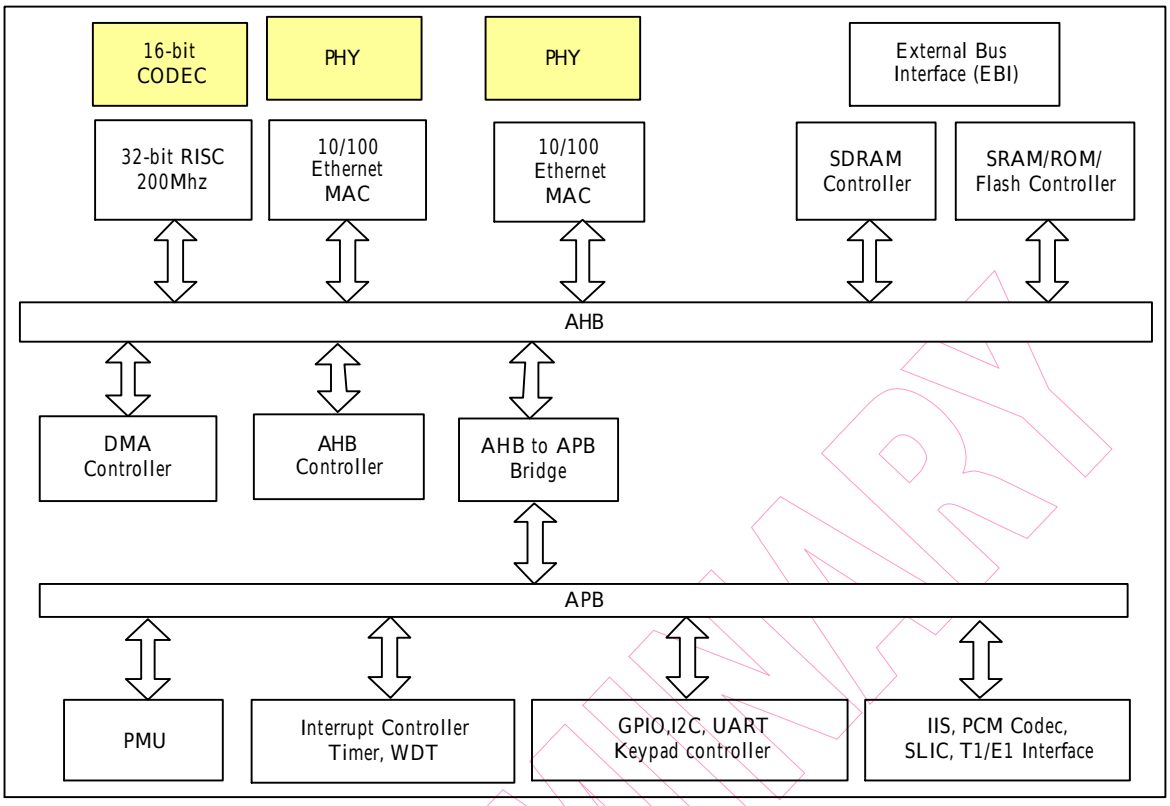


Figure 1 Block Diagram of EM7A8620

1.5 Pin Assignment

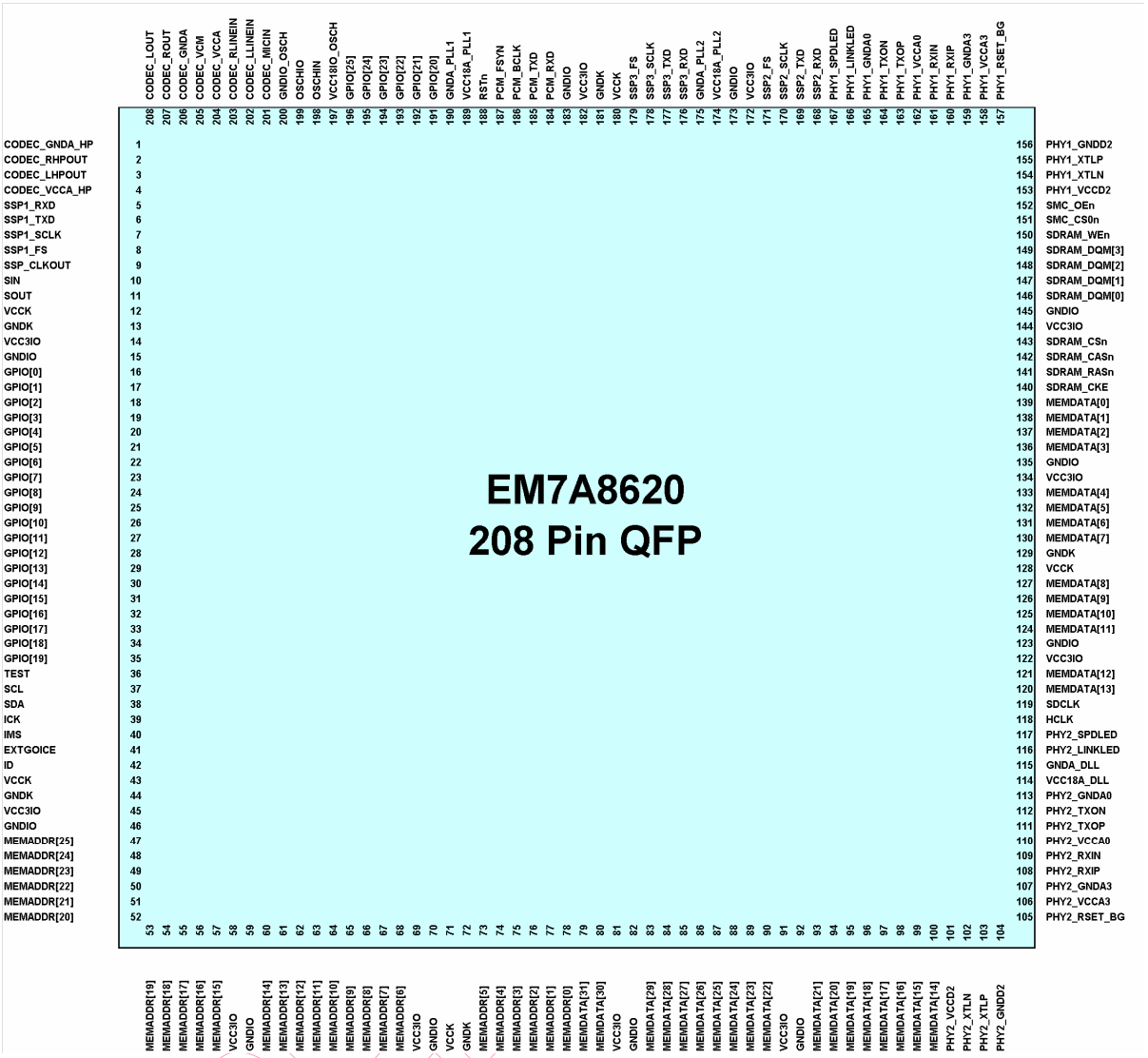


Figure 2 Block Diagram of EM7A8620

2. Function Descriptions

2.1 CPU

The CPU is a general-purpose 32-bit embedded RISC processor. It's a Harvard architecture design with six pipeline stages. It includes separate instruction / data caches, separate instruction / data scratchpads, a write buffer, a branch target buffer, a protection unit, and an ICE interface.

2.2 SDRAM Controller

The SDRAM memory controller supports one 8-, 16- or 32-bit wide bank. The SDRAM controller performs auto-refreshing during normal operation, and supports SDRAM self-refreshing during Sleep. The SDRAMC shares the address / data bus with Static Memory Controller. The SDRAMC features include:

- Wide address range up to 256 M bytes
- Support various SDRAM types
- Support a programmable auto-refresh and self-refresh

2.3 Static Memory Controller

The Static Memory Controller supports Flash memory, SRAM and ROM. Each chip select can be individually programmed to an 8-, 16- or 32-bit wide data bus. The features include:

- Support ROM, FLASH, burst-ROM, asynchronous SRAM
- Wide address range up to 64M bytes

2.4 10/100 Ethernet

The Ethernet MAC 10/100 is a high quality 10/100 Ethernet controller with DMA functions. It includes AHB interface, DMA channel, MAC, and PHY. The Ethernet features include:

- 10Mbps/100Mbps operation
- Half and Full duplex modes
- Support flow control for full duplex and backpressure for half duplex
- Fully compliant with IEEE 802.3u, FDDI-TP-PMD and IEEE 802.3
- Support Auto Negotiation detection and Auto Crossover detection
- Network status LEDs

2.5 Direct Memory Access

The DMA provides up to 4 channels for memory-to-memory, memory-to-peripheral, peripheral-to-peripheral, and peripheral-to-memory transfer with the shared buffer. The features include:

- Up to 4 DMA channels
- Provide memory-to-memory, memory-to-peripheral, peripheral-to-peripheral, and peripheral-to-memory transfer
- Round Robin arbitration scheme with four priority levels
- Support chain transfer
- Support 8/16/32-bit data width transfer

2.6 I^2C

The I^2C is a two-wire bidirectional serial bus. The I^2C bus interface controller allows the host processor to serve as a master or slave residing on the I^2C bus. Data are transmitted to and received from the I^2C bus via a buffered interface. The features include:

- Support Master and Slave modes
- Programable standard and fast modes
- Support 7-bit, 10-bit and general call addressing modes
- Built in Glitch de-bounce circuits
- Programmable address in the slave mode
- Slave mode general call address detection

2.7 UART

The features include:

- Programmable baud rates up to 115.2 Kbps
- Configurable Start, Stop, and Parity bits.
- Support DMA for large data transfer
- Fully programmable serial interface:
  - 5-, 6-, 7-, or 8-bit characters
  - Even, odd, and no parity detection
  - 1-, 1.5-, or 2-stop bit generation

2.8 I2S/SPI Controller

The I²S/SPI controller are friendly to connected external audio codec device. The I²S interface transfers digitized audio between the system memory and an external I²S Codec which is controlled by SPI interface.

- Support I^2S or SPI functions
- Support Master mode or Slave mode
- Programmable frame/sync polarity, serial bit clock polarity and frequency.
- Programmable MSB or LSB first
- Programmable zero bits padding and right or left justification in I^2S Mode
- Support DMA for large data transfer

2.9 PCM Controller

The PCM controller provides PCM BUS for PCM data transferring between SLIC/DAA. The PCM controller features include:

- Support Master and Slave mode.
- Programmable serial bit clock frequency.
- Programmable frame sync length.
- Support DMA for large data transfer

2.10 LCD Dot Matrix Controller

The Dot Matrix controller provides an asynchronous MPU command interface.The features include:

- Uniform LCD Dot Matrix Interface
- Programmable nibble mode or byte mode data/address bus

2.11 Timer

It provides 3 independent sets of timers. The features include:

- Three independent 32-bit timer
- Internal clock source
- Support Interrupts when overflow and time-up
- Support decrementing mode

2.12 Watch Dog Timer (WDT)

The WDT generates one or a combination of the following signals: reset, interrupt or external interrupt. The features include:

- Support System Reset, Interrupt and/or External Interrupt when timeout
- 32-bit down counter
- Variable time-out period of reset
- Access protection
- Watchdog reset is asserted, which resets the system except the PMU and RTC.

2.13 Interrupt Controller

The Interrupt Controller provides both FIQ and IRQ modes to the CPU. The features include:

- Support fast interrupt (FIQ) and standard interrupt (IRQ)
- Interrupts can be routed to either IRQ or FIQ
- Programmable edge or level trigger interrupt source with positive and negative directions
- Support de-bounce circuit for interrupt input sources
- Programmable enable or disable any interrupt source

2.14 General Purpose Input / Output

32 GPIOs are used to input / output data from system and device. The features include:

- Support configurable as interrupt function
- Programmable edge or level trigger in interrupt mode
- Each port can be pulled high or pulled low
- Programmable Input/Output function

2.15 Real Time Clock

The RTC provides a basic alarm function or long time-based counter. The RTC is set to be 1Hz output and employed as a system timekeeper. The features include:

- Support sleep mode
- Support second, minute, hour and day counters Alarm
- Once-per-second, once-per-minute, once-per-hour, and once-per-day interrupts

2.16 Power Management

Most of the device's clock can be enabled or disabled by using the system configuration registers. The clock to any unit that is not being used is turned off to minimize the power consumption. The PMU provides a method to change the PLL frequency and various power modes.

2.17 Audio CODEC

The Audio CODEC has the following features.

- 90-dB SNR sigma-delta DAC
- 92-dB SNR sigma-delta ADC
- 8K ~ 96KHz sampling rate
- Analog volume control with mute
- Stereo line inputs/outputs
- ADC multiplexed input for stereo-line inputs and microphone

3. DC Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CC}	Core power supply	-0.3 to 3.6	V
V_{IN18}	Input voltage of 1.8v I/O	-0.3 to 2.1	V
V_{IN3}	Input voltage of 3.3V I/O	-0.3 to 3.63	V
V_{IN3}	Input voltage of 3.3V I/O with 5V tolerance	-0.3 to 5.5	V
T_{STG}	Storage temperature	-40 to 150	℃

3.2 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC18	Core power supply	1.65	1.8	1.95	V
VCC33	Power supply of 3.3V I/O	3.0	3.3	3.6	V
VCC18A	Power supply of 1.8V I/O	1.65	1.8	1.95	V
VCC18I	Power supply of 1.8V I/O	1.65	1.8	1.95	V
V_{IN3}	Input voltage of 3.3V I/O with 5V tolerance	0	3.3	5.25	V
T_j	Commercial junction operating temperature	0	25	115	℃
T_a	Commercial ambient operating temperature	0		70	℃
ESD	HBM model ESD		1	2000	V
	MM model ESD			200	V
	CDM model ESD				V

3.3 I/O Pad Capacitance

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
C_{IN}	Input capacitance			3.2		pF
C_{OUT}	Output capacitance			3.2		pF
C_{BID}	Bi-directional capacitance			3.2		pF

3.4 DC Characteristics for 3.3V Operation

Recommended operating conditions (V_{CC} = 3.0V to 3.6V)

Symbol	Descriptions	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input low voltage	LVTTL			0.8	V
V_{Ih}	Input high voltage	LVTTL	2.0			V
V_t	Switching threshold	LVTTL		1.5		V

V_{t-}	Schmitt trigger negative going threshold voltage	LVTTL	0.8	1.1		V
V_{t+}	Schmitt trigger positive going threshold voltage	LVTTL		1.6	2.0	V
V_{OL}	Output low voltage	I_{OL} = 2 ~ 16 mA			0.4	V
V_{OH}	Output high voltage	I_{OL} = -2 ~ -16 mA	2.4			V
R_{PU}	Input pull-up resistance	V_{in} = 0	40	75	190	KΩ
R_{PD}	Input pull-down resistance	V_{in} = 3.3V	40	75	190	KΩ
I_{in}	Input leakage current	V_{in} = 3.3V or 0	-10	±1	10	uA
	Input leakage current with pull-up resistance	V_{in} = 0	-15	-45	-85	uA
	Input leakage current with pull-down resistance	V_{in} = 3.3V	15	45	85	uA
I_{OZ}	Tri-state output leakage current		-10	±1	10	uA

3.5 DC Characteristics for 1.8V Operation

Recommended operating conditions (V_{CC} = 1.65V to 1.95V)

Symbol	Descriptions	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input low voltage	CMOS			0.69	V
V_{Ih}	Input high voltage	CMOS	1.05			V
V_t	Switching threshold	CMOS		0.85		V
V_{t-}	Schmitt trigger negative going threshold voltage	CMOS	0.59	0.71		V
V_{t+}	Schmitt trigger positive going threshold voltage	LVTTL		0.98	1.14	V
V_{OL}	Output low voltage	I_{OL} = 2 ~ 16 mA			0.4	V
V_{OH}	Output high voltage	I_{OL} = -2 ~ -16 mA	1.22			V
R_{PU}	Input pull-up resistance	PU = high PD = low	40	75	190	KΩ
R_{PD}	Input pull-down resistance	PU = high PD = low	40	75	190	KΩ
I_{in}	Input leakage current	V_{in} = 1.8V or 0	-10	±1	10	uA
I_{OZ}	Tri-state output leakage current		-10	±1	10	uA