

Vishay Beyschlag

# **Flat Chip Resistor Array**



ACAC 0612 flat chip resistor array combines the proven reliability of precision MFC products with the advantages of a chip array. The possibility of tolerance matching and T.C. tracking makes this product perfectly suited for applications with outstanding requirements towards stable fixed resistor ratios. A small package enables the design of high density circuits in combination with reduction of assembly costs. Different resistance values can be realized on one substrate.

### **FEATURES**



- · Advanced thin film technology
- · Superior overall stability
- · Four resistors on one substrate
- Tight T.C. of ± 25 ppm/K and T.C. tracking of 15 ppm/K, (10 ppm/K on request)
- Tolerance of  $\pm$  0.25 % and matched tolerance of 0.1 %
- Different resistance values are possible
- Pure Sn termination on Ni barrier layer
- Compatible with lead (Pb)-free and lead containing soldering processes
- Lead (Pb)-free and RoHS compliant

#### **APPLICATIONS**

- Precision analogue circuits
- · Voltage divider
- · Feedback circuits
- Signal conditioning

TECHNICAL SPECIFICATIONS	AOAO 0010		
DESCRIPTION	ACAC 0612		
EIA size	0612		
Metric size	RR 1632M		
Configuration, isolated	4 × 0603		
Design:			
all equal	AE		
two pairs	TP		
different values	DF		
Resistance values	100 $\Omega$ to 221 k $\Omega^{1)}$		
Tolerance:			
absolute	± 0.25 %		
matching	0.1 %		
Temperature coefficient:			
absolute	± 25 ppm/K		
tracking	15 ppm/K		
Max. resistance ratio R <sub>min</sub> /R <sub>max</sub>	1:5		
Climatic category (LCT/UCT/days)	55/125/56		
Rated dissipation: P <sub>70</sub> <sup>2)</sup>			
element	0.1 W		
package	0.3 W		
Operating voltage	75 V		
Film temperature	125 °C		
Insulation voltage (U <sub>ins</sub> ) against ambient and between isolated resistors, continuous	75 V		

#### Note

- 1. Resistance values to be selected from E24 and E96.
- The power dissipation on the resistor generates a temperature rise against the local ambient, depending on the heat flow support of the printed-circuit board (thermal resistance). The rated dissipation applies only if the permitted film temperature is not exceeded.

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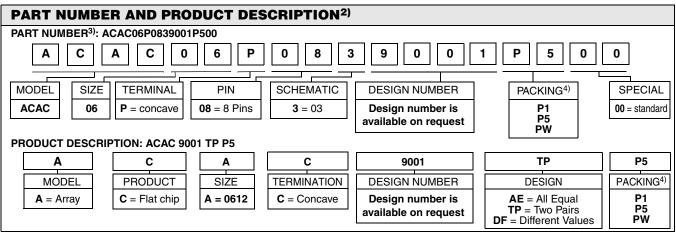
### **12NC INFORMATION**

- The arrays have a 12-digit numeric code starting with 2312. The subsequent 3 digits indicate the array packing and body size; see the 12NC table.
- The last 5 digits indicate the termination and individual array design number (last 4 digits).

12NC - resistor array type and packing								
	DEC	COUDTION	ORDERING CODE 2312					
	DES	SCRIPTION	AE (ALL EQUAL) TP (TWO PAIRS)					
TYPE	T.C.	TOL.	R1; R4	R2; R3	P5 5 000 UNITS	P5 5 000 UNITS		
ACAC 0612		0.1 %	1 kΩ	1 kΩ	441 09001	_		
			10 kΩ	10 kΩ	441 09002	_		
			100 kΩ	100 kΩ	441 09003	_		
	15 ppm/K		1 kΩ	2 kΩ	_	441 19004		
			10 kΩ	20 kΩ	-	441 19005		
			1 kΩ	3 kΩ	-	441 19006		
			10 kΩ	30 kΩ	-	441 19007		

#### Note

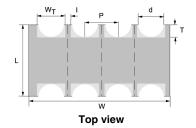
1. 12NC indicating resistor array type and packing table shows standard array types with a resistance divider ratio up to 1:3. Please consult Vishay BEYSCHLAG for specific divider ratio, temperature coefficient, tolerance and ohmic values.

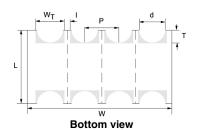


#### Note

- Products can be ordered using either the PRODUCT DESCRIPTION or the 12 NC.
- The PART NUMBER is shown to facilitate the introduction of a unified part numbering system. Currently, this PART NUMBER is applicable in the Americas only.
- Please refer to table PACKING, page 3.

### **DIMENSIONS**





<b>DIMENSIONS -</b> CHIP resistor array top view, mass and relevant physical dimensions									
TYPE	L (mm)	W (mm)	H (mm)	P (mm)	W <sub>T</sub> (mm)	T (mm)	d (mm)	I (mm)	mass (mg)
ACAC 0612	1.6 ± 0.15	$3.2 \pm 0.15$	$0.55 \pm 0.1$	$0.8 \pm 0.1$	$0.6 \pm 0.15$	$0.3 \pm 0.15$	$0.3 \pm 0.1$	min. 0.15	9.41

DIMENSIONS - CHIP resistor array bottom view, mass and relevant physical dimensions									
TYPE	L (mm)	W (mm)	H (mm)	P (mm)	W <sub>T</sub> (mm)	T (mm)	d (mm)	l (mm)	mass (mg)
ACAC 0612	1.6 ± 0.15	3.2 ± 0.15	0.55 ± 0.1	$0.8 \pm 0.1$	0.6 ± 0.15	0.4 ± 0.15	$0.3 \pm 0.1$	min. 0.25	9.41

For technical questions contact: ff3aresistors@vishay.com Document Number: 28741 Revision: 28-Nov-05

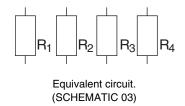


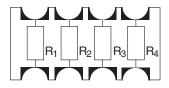
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PACKING								
MODEL	EL TAPE WIDTH DIAMETER PIECES		PITCH	PACKING CODE				
					PAPER TAPE			
	8 mm	180 mm/7"	1000	4 mm	P1			
ACAC	8 mm	180 mm/7"	5000	4 mm	P5			
	8 mm	330 mm/13"	10000	4 mm	PW			

### **APPLICATION INFORMATION**





Array configuration.

#### **DESCRIPTION**

Production is strictly controlled and follows an extensive set of instructions established for reproducibility. A homogeneous film of metal alloy is deposited on a super high grade (96 % Al $_2$  O $_3$ ) ceramic substrate and conditioned to achieve the desired temperature coefficient. Specially designed inner contacts are deposited on both sides. A special laser is used to achieve the target value by smoothly cutting a meander groove in the resistive layer without damaging the ceramics.

The resistor elements are covered by a protective coating designed for electrical, mechanical and climatic protection. The terminations receive a final pure tin on nickel plating.

The result of the determined production is verified by an extensive testing procedure and optical inspection performed on 100 % of the individual chip resistors. Only accepted products are laid directly into the paper tape in accordance with **EN 60 286-3**.

#### **ASSEMBLY**

The resistors are suitable for processing on automatic SMD assembly systems and for automatic soldering using wave, reflow or vapour phase. The encapsulation is resistant to all cleaning solvents commonly used in the electronics industry, including alcohols, esters and aqueous solutions. The resistors are lead (Pb)-free, the pure tin plating provides compatibility with lead (Pb)-free and lead-containing soldering processes. The immunity of the plating against tin whisker growth has been proven under extensive testing. All products comply with the CEFIC-EECA-EICTA list of legal restrictions on hazardous substances:

This includes full compliance with the following directives:

- 2000/53/EC End of Vehicle life Directive (ELV)
- 2000/53/EC Annex II to End of Vehicle Life Directive (ELV II)
- 2002/95/EC Restriction of the use of Hazardous Substances Directive (RoHS)
- 2002/96/EC Waste Electrical and Electronic Equipment Directive (WEEE)

Solderability is specified for 2 years after production or re-qualification. The permitted storage time is 20 years.

### **APPROVALS**

Where applicable, the resistors are tested in accordance with EN 140 401-801 (superseding CECC 40401-801) which refers to EN 140 000 (EN 60 115-1) and EN 140 400 (IEC 60 115-8).

Document Number: 28741 Revision: 28-Nov-05

# Vishay Beyschlag

## Flat Chip Resistor Array



### **TESTS AND REQUIREMENTS**

Essentially all tests are carried out in accordance with the following specifications:

EN 140 000 / EN 60 115-1, Generic specification (includes tests)

EN 140 400 / EN 60 115-1, Sectional specification (includes schedule for qualification approval)

The testing also covers most of the requirements specified by EIA/IS-703 and JIS-C-5202.

The tests are carried out in accordance with IEC 60 068 and under standard atmospheric conditions according to IEC 60 068-1, 5.3. Climatic category LCT/UCT/56 (rated temperature range: Lower Category Temperature, Upper Category Temperature; damp heat, long term, 56 days) is valid.

Unless otherwise specified the following values apply:

Temperature: 15 °C to 35 °C Relative humidity: 45 % to 75 %

Air pressure: 86 kPa to 106 kPa (860 mbar to 1 060 mbar).

The components are mounted for testing on boards in accordance with EN 60 115-1, 4.31 unless otherwise specified.

In the following table only the tests and requirements are listed with reference to the relevant clauses of EN 60 115-1 and IEC 60 068-2; a short description of the test procedure is also given.

TEST PROCEDURES AND REQUIREMENTS						
EN IEC 60115-1 60068-2 CLAUSE TEST METHOD		TEST	PROCEDURE	REQUIREMENTS¹) PERMISSIBLE CHANGE (△R/R)		
			stability for product types:			
			ACAC 0612	100 $\Omega$ to 221 k $\Omega$		
4.5	=	resistance	-	± 0.25 %		
4.8.4.2	-	temperature coefficient	at 20 / LCT / 20 °C and 20 / UCT / 20 °C	± 25 ppm/K		
4.25.1	_	endurance	$U = \sqrt{P_{70} \times R}$ or U = U <sub>max</sub> ; 1.5 h on; 0.5 h off; 70 °C; 1000 h	± (0.25 % R + 0.05 Ω)		
4.25.3	-	endurance at upper category temperature	125 °C; 1000 h	± (0.5 % R + 0.05 Ω)		
4.24	78 (Cab)	damp heat, steady state	(40 ± 2) °C; 56 days; (93 ± 3) % RH	± (0.5 % R + 0.05 Ω)		
4.13	-	short time overload <sup>2)</sup>	$U = 2.5 \times \sqrt{P_{70} \times R} \text{ or}$ $U = 2 \times U_{max}; 5 \text{ s}$	$\pm$ (0.1 % R $\pm$ 0.01 $\Omega$ ) no visible damage		
4.19	14 (Na)	rapid change of temperature	30 min. at LCT and 30 min. at UCT; 5 cycles	$\pm$ (0.1 % R + 0.01 $\Omega$ ) no visible damage		
4.18.2	58 (Tb)	resistance to soldering heat	reflow method 2 (IR / forced gas convention); (260 ± 5) °C; (10 ± 1) s	$\pm$ (0.1 % R + 0.01 $\Omega$ ) no visible damage		
4.17.2	58 (Ta)	solderability	solder bath method; $(215 \pm 3)$ °C; $(3 \pm 0.3)$ s	good tinning (≥ 95 % covered); no visible damage		
4.32	21 (Ue <sub>3</sub> )	shear (adhesion)	RR 1632M; 45 N	no visible damage		
4.7	-	voltage proof	U <sub>rms</sub> = U <sub>ins</sub> ; 60 ± 5 s; against ambient, between adjacent resistors	no flashover or breakdown		

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## Note

- 1. Figures are given for equal values.
- 2. For a single element.

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