

HD74LS76A

Dual J-K Flip-Flops (with Preset and Clear)

REJ03D0417-0300
 Rev.3.00
 Jul.22.2005

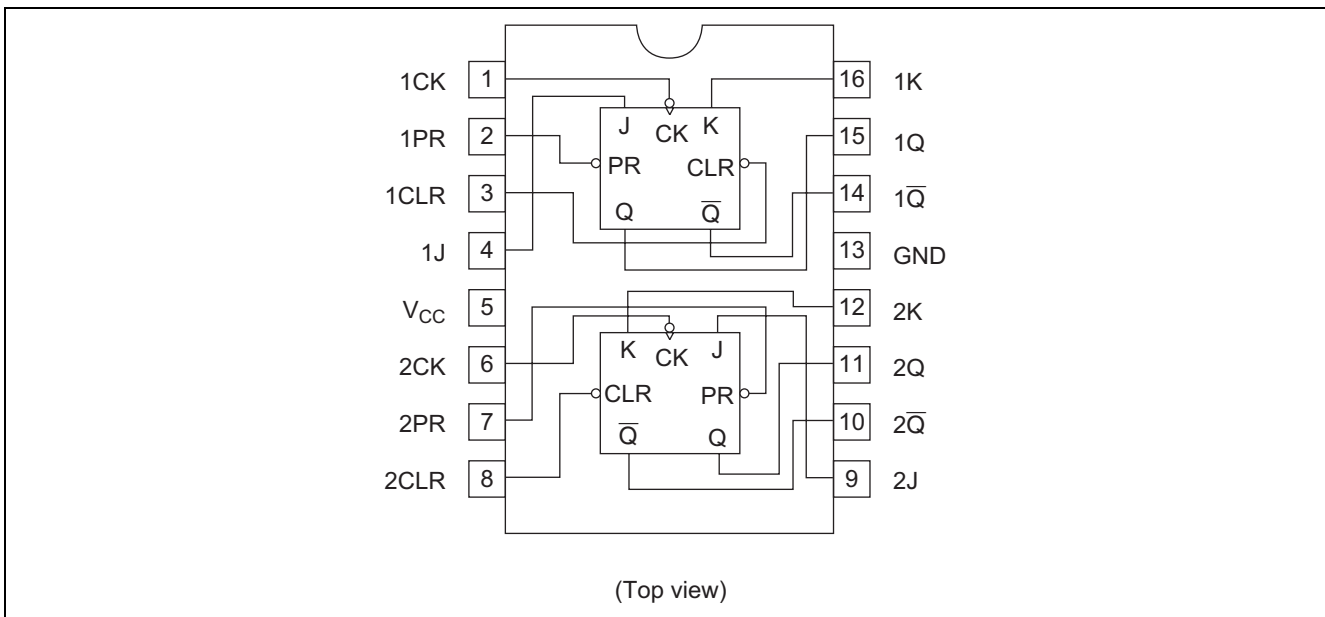
Features

- Ordering Information

| Part Name | Package Type | Package Code (Previous Code) | Package Abbreviation | Taping Abbreviation (Quantity) |
|---------------|-------------------|------------------------------|----------------------|--------------------------------|
| HD74LS76AP | DILP-16 pin | PRDP0016AE-B (DP-16FV) | P | — |
| HD74LS76ARPEL | SOP-16 pin(JEDEC) | PRSP0016DG-A (FP-16DNV) | RP | EL(2,500 pcs/reel) |

Note: Please consult the sales office for the above package availability.

Pin Arrangement



Function Table

| Inputs | | | | | Outputs | |
|--------|-------|-------|---|---|----------------|-------------|
| Preset | Clear | Clock | J | K | Q | \bar{Q} |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H* | H* |
| H | H | ↓ | L | L | Q ₀ | \bar{Q}_0 |
| H | H | ↓ | H | L | H | L |
| H | H | ↓ | L | H | L | H |
| H | H | ↓ | H | H | Toggle | |
| H | H | H | X | X | Q ₀ | \bar{Q}_0 |

H; high level, L; low level, X; irrelevant, ↓; transition from high to low level,

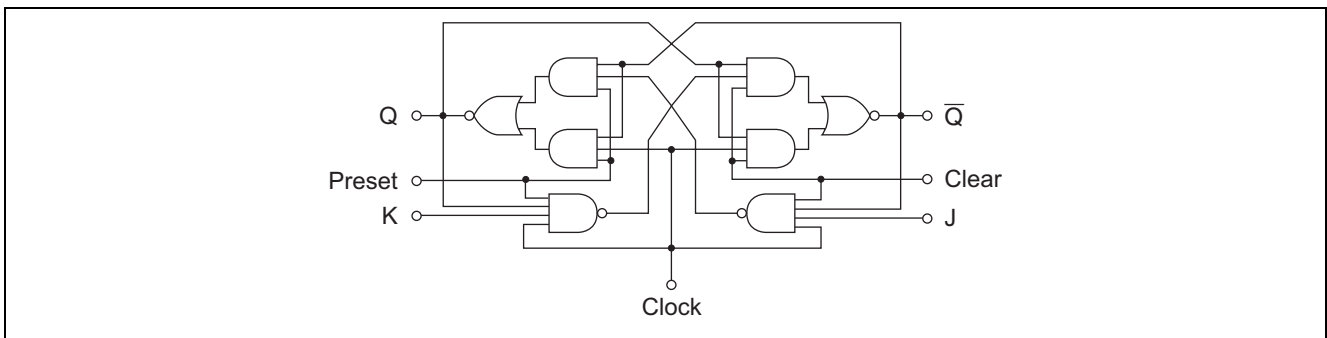
Q₀; level of Q before the indicated steady-state input conditions were established.

\bar{Q}_0 ; complement of \bar{Q}_0 or level of Q before the indicated steady-state input conditions were established.

Toggle; each output changes to the complement of its previous level on each active transition indicated by ↓.

* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Block Diagram (1/2)



Absolute Maximum Ratings

| Item | Symbol | Ratings | Unit |
|---------------------|------------------|-------------|------|
| Supply voltage | V _{CC} | 7 | V |
| Input voltage | V _{IN} | 7 | V |
| Power dissipation | P _T | 400 | mW |
| Storage temperature | T _{stg} | -65 to +150 | °C |

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

| Item | Symbol | Min | Typ | Max | Unit |
|-----------------------|--------------------|-----------------|------|------|------|
| Supply voltage | V _{CC} | 4.75 | 5.00 | 5.25 | V |
| Output current | I _{OH} | — | — | -400 | μA |
| | I _{OL} | — | — | 8 | mA |
| Operating temperature | T _{opr} | -20 | 25 | 75 | °C |
| Clock frequency | f _{clock} | 0 | — | 30 | MHz |
| Pulse width | Clock High | t _w | 20 | — | ns |
| | Clear Preset Low | t _w | 25 | — | |
| Setup time | "H" Data | t _{su} | 20↓ | — | ns |
| | "L" Data | t _{su} | 20↓ | — | |
| Hold time | t _h | 0↓ | — | — | ns |

Electrical Characteristics

(Ta = -20 to +75 °C)

| Item | Symbol | min. | typ.* | max. | Unit | Condition | |
|------------------------------|-----------------|------|-------|------|------|---|--|
| Input voltage | V _{IH} | 2.0 | — | — | V | | |
| | V _{IL} | — | — | 0.8 | V | | |
| Output voltage | V _{OH} | 2.7 | — | — | V | V _{CC} = 4.75 V, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -400 μA | |
| | V _{OL} | — | — | 0.5 | V | V _{CC} = 4.75 V, V _{IH} = 2 V, V _{IL} = 0.8 V | |
| — | | — | 0.4 | | | | |
| Input current | J, K | — | — | 20 | μA | V _{CC} = 5.25 V, V _I = 2.7 V | |
| | Clear | | | 60 | | | |
| | Preset | | | 60 | | | |
| | Clock | | | 80 | | | |
| | J, K | — | — | -0.4 | mA | | V _{CC} = 5.25 V, V _I = 0.4 V |
| | Clear | | | -0.8 | | | |
| | Preset | | | -0.8 | | | |
| | Clock | | | -0.8 | | | |
| | J, K | — | — | 0.1 | mA | V _{CC} = 5.25 V, V _I = 7 V | |
| | Clear | | | 0.3 | | | |
| | Preset | | | 0.3 | | | |
| | Clock | | | 0.4 | | | |
| Short-circuit output current | I _{OS} | -20 | — | -100 | mA | | V _{CC} = 5.25 V |
| Supply current*** | I _{CC} | — | 4 | 6 | mA | | V _{CC} = 5.25 V |
| Input clamp voltage | V _{IK} | — | — | -1.5 | V | | V _{CC} = 4.75 V, I _{IN} = -18 mA |

Notes: * V_{CC} = 5 V, Ta = 25°C

** I_{IL} should not be measured when preset and clear inputs are low at same time.

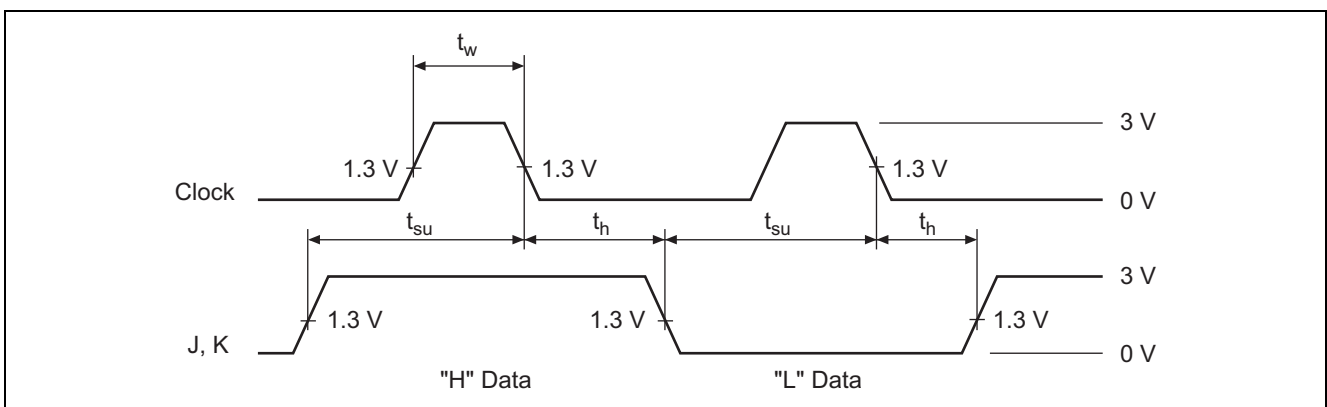
*** With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

Switching Characteristics

(V_{CC} = 5 V, Ta = 25°C)

| Item | Symbol | Inputs | Outputs | min. | typ. | max. | Unit | Condition |
|-------------------------|------------------|-----------------|--------------|------|------|------|------|---|
| Maximum clock frequency | f _{max} | | | 30 | 45 | | MHz | C _L = 15 pF, R _L = 2 kΩ |
| Propagation delay time | t _{PLH} | Clear | Q, \bar{Q} | — | 15 | 20 | ns | |
| | t _{PHL} | Preset Clock | | — | 15 | 20 | ns | |

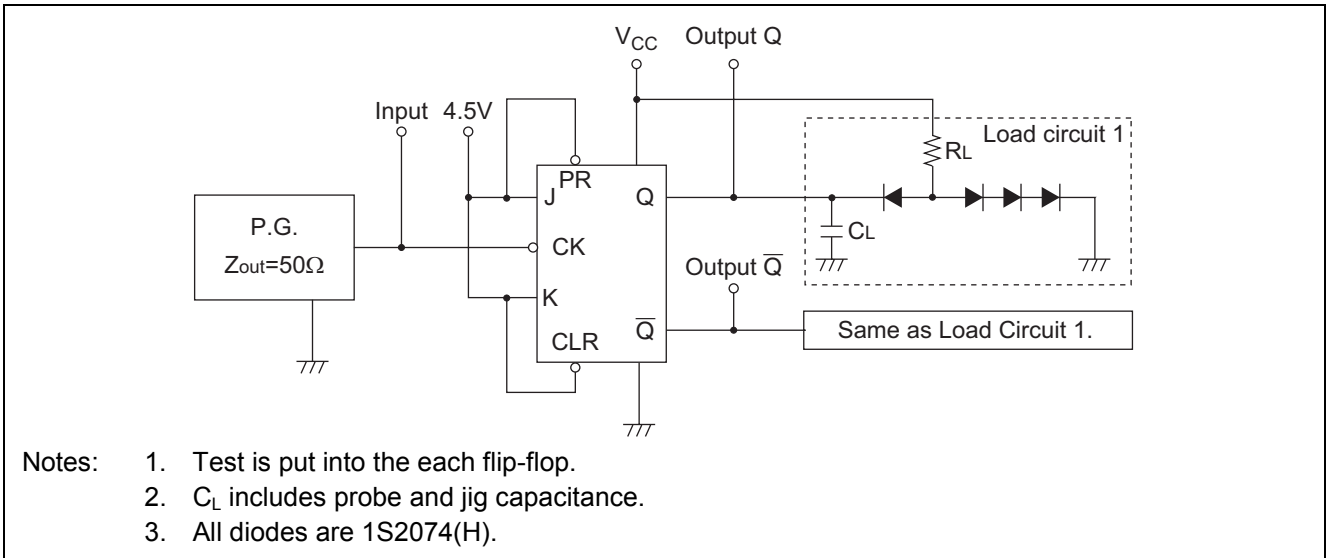
Timing Definition



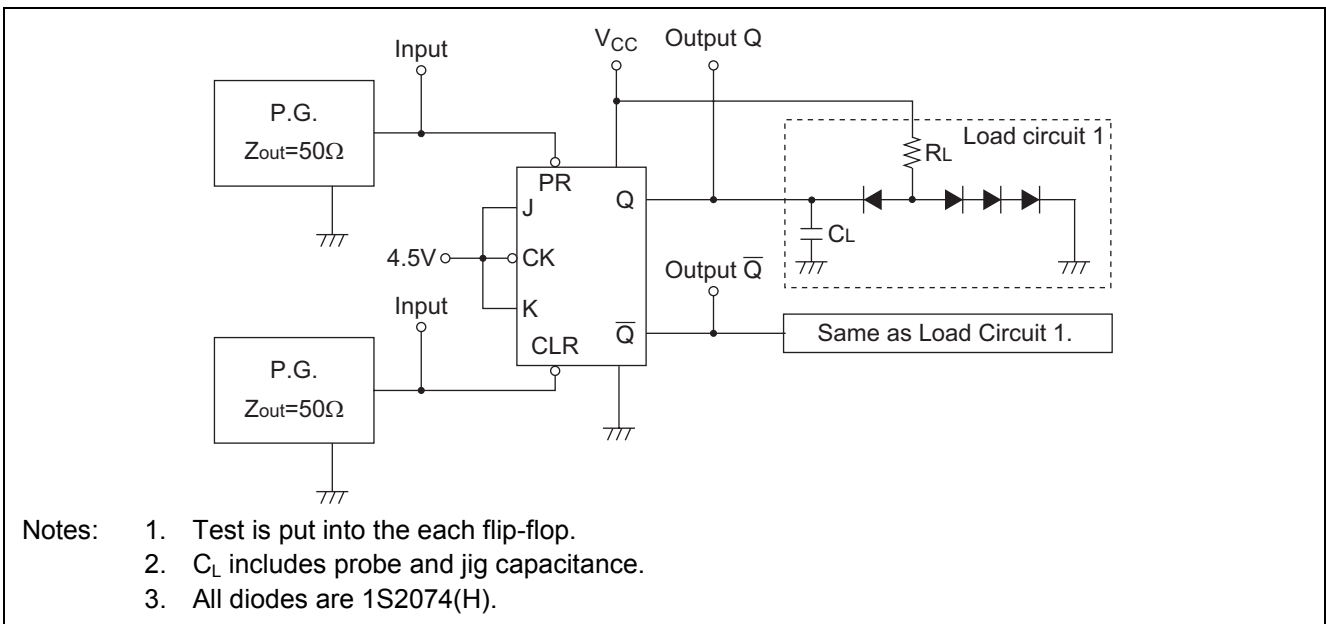
Testing Method

Test Circuit

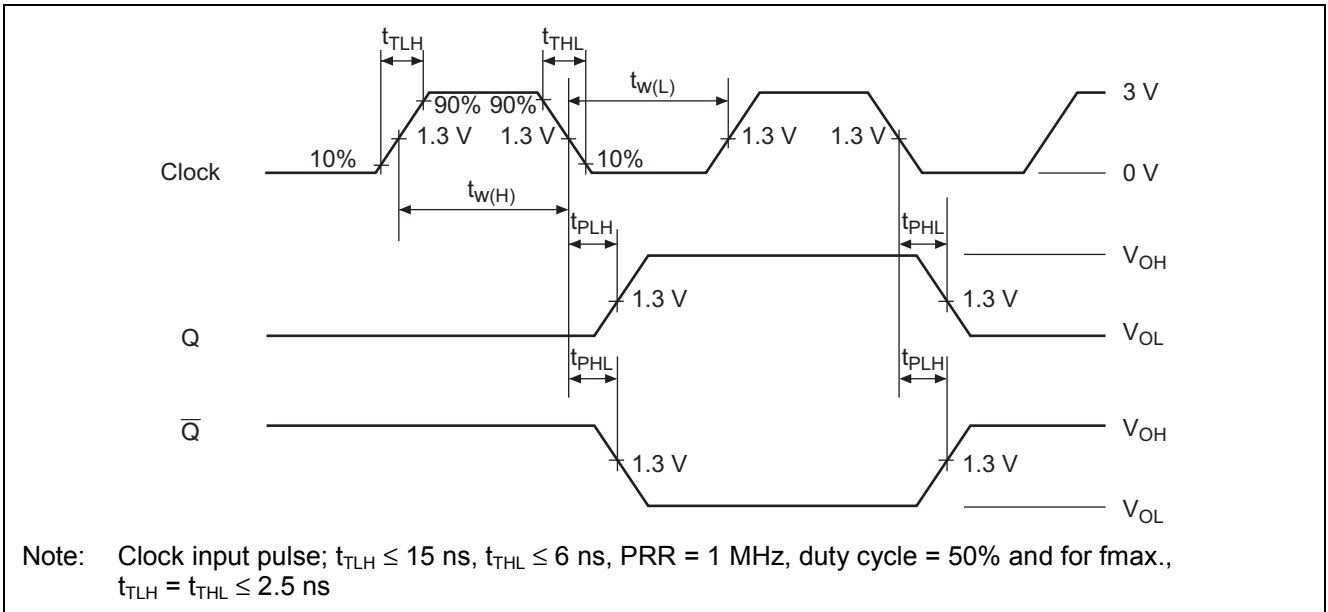
1. f_{max} , t_{PLH} , t_{PHL} , (Clock \rightarrow Q, \bar{Q})



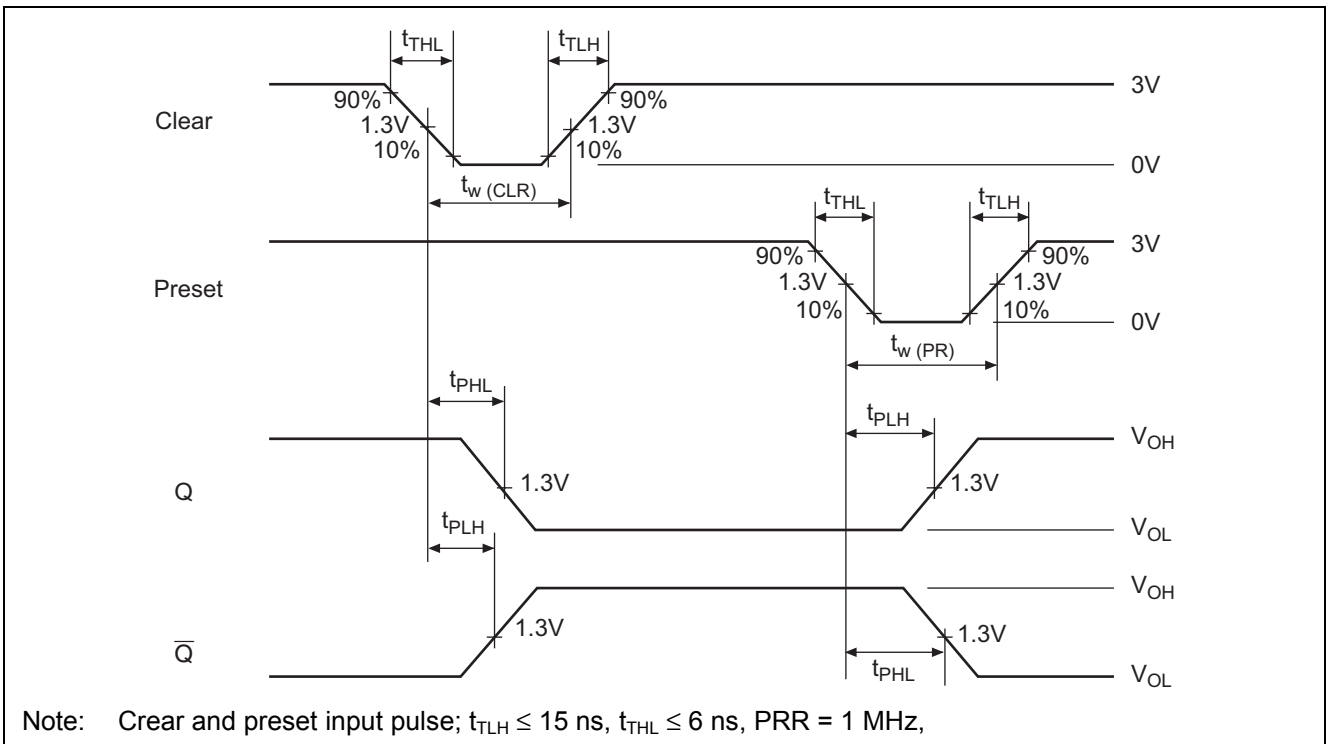
2. t_{PHL} , t_{PLH} (Clear, Preset \rightarrow Q, \bar{Q})



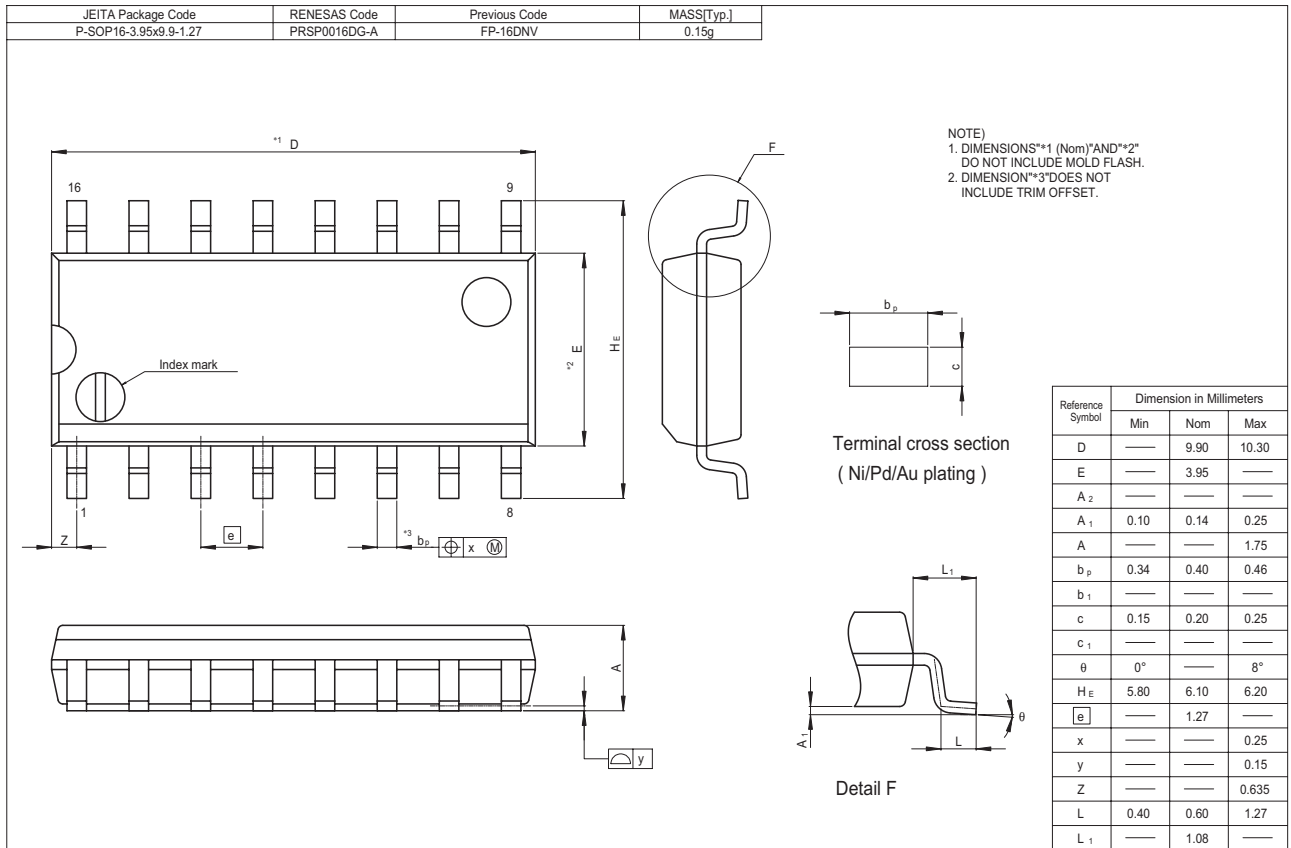
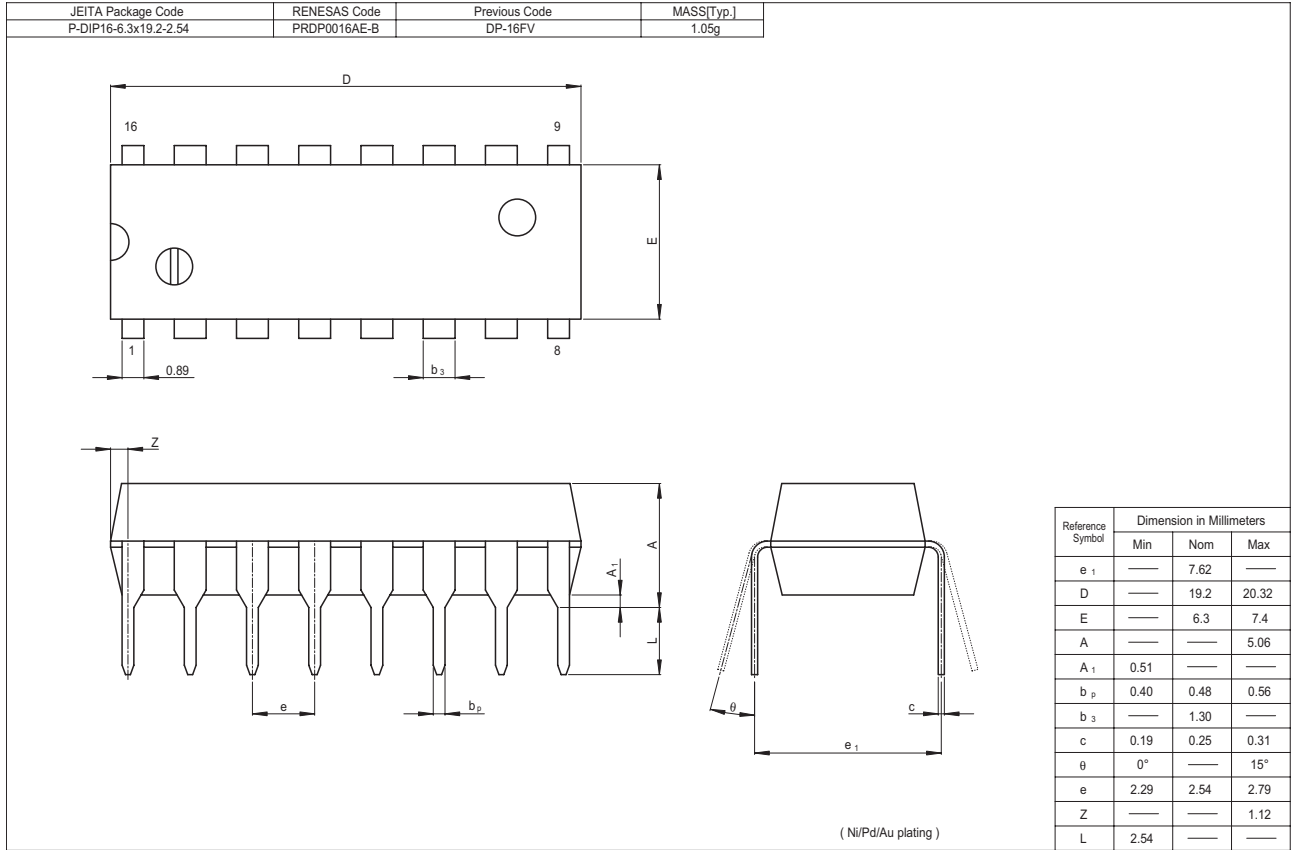
Waveforms 1



Waveforms 2



Package Dimensions



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