REJ09B0441-0010

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R8C/L35A Group, R8C/L36A Group, R8C/L38A Group, R8C/L3AA Group, R8C/L35B Group, R8C/L36B Group, R8C/L38B Group, R8C/L3AB Group Hardware Manual

RENESAS MCU
R8C FAMILY / R8C/Lx SERIES

Preliminary

Hardware Manual

Rev.0.10
Revision Date: Jul 30, 2008

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.
The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the R8C/L35A Group, R8C/L35B Group, R8C/L36A Group, R8C/L36B Group, R8C/L38A Group, R8C/L38B Group, R8C/L3AA Group, R8C/L3AB Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Technology Web site.

Document Type	Description	Document Title	Document No.
Shortsheet	Hardware overview	R8C/L35A Group, R8C/L36A Group, R8C/L38A Group, R8C/L3AA Group, R8C/L35B Group, R8C/L36B Group, R8C/L38B Group, R8C/L3AB Group Shortsheet	REJ03B0243
Hardware manual	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description Note: Refer to the application notes for details on using peripheral functions.	R8C/L35A Group, R8C/L36A Group, R8C/L38A Group, R8C/L3AA Group, R8C/L35B Group, R8C/L36B Group, R8C/L38B Group, R8C/L3AB Group Hardware Manual	This hardware manual
Software manual	Description of CPU instruction set	R8C/Tiny Series Software Manual	REJ09B0001
Application note	Information on using peripheral functions and application examples Sample programs Information on writing programs in assembly language and C	Available from the Renesas Technology Corp. website.	
Renesas technical update	Product specifications, updates on documents, etc.		

2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

(1) Register Names, Bit Names, and Pin Names
Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word “register,” “bit,” or “pin” to distinguish the three categories.
Examples the PM03 bit in the PM0 register
P3_5 pin, VCC pin

(2) Notation of Numbers
The indication “b” is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication “h” is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.
Examples Binary: 11b
Hexadecimal: EFA0h
Decimal: 1234

3. Register Notation

The symbols and terms used in register diagrams are described below.

x.x.x XXX Register (Symbol)

Address XXXXh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	XXX7	XXX6	XXX5	XXX4	—	—	XXX1	XXX0
After Reset	0	0	0	0	0	0	0	0

*1

Bit	Symbol	Bit Name	Function	R/W
b0	XXX0	XXX bit	b1 b0 0 0: XXX 0 1: XXX 1 0: Do not set. 1 1: XXX	R/W
b1	XXX1			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b3	—	Reserved bit	Set to 0.	R/W
b4	XXX4	XXX bit	Function varies according to the operating mode.	R/W
b5	XXX5			W
b6	XXX6			R/W
b7	XXX7	XXX bit	0: XXX 1: XXX	R

*2

*3

*1

R/W: Read and write.
R: Read only.
W: Write only.
–: Nothing is assigned.

*2

- Reserved bit

  Reserved bit. Set to specified value.

*3

- Nothing is assigned.

  Nothing is assigned to the bit. As the bit may be used for future functions, if necessary, set to 0.
- Do not set to a value.

  Operation is not guaranteed when a value is set.
- Function varies according to the operating mode.

  The function of the bit varies with the peripheral function mode. Refer to the register diagram for information on the individual modes.

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connection
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SFR	Special Function Register
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

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0002h			
0003h			
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0007h	System Clock Control Register 1	CM1	130, 147
0008h	Module Standby Control Register	MSTCR	280, 335, 351, 372, 389, 404, 421, 565, 597
0009h	System Clock Control Register 3	CM3	131, 148
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000Fh	Watchdog Timer Control Register	WDTC	213
0010h			
0011h			
0012h			
0013h			
0014h			
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0016h			
0017h			
0018h			
0019h			
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001Eh			
001Fh			
0020h	Power-Off Mode Control Register 0	POMCR0	152
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0022h			
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0028h			
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0048h	Timer RD0 Interrupt Control Register	TRD0IC	175
0049h	Timer RD1 Interrupt Control Register	TRD1IC	175
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Note:
1. Blank spaces are reserved. No access is allowed.

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0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
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Note:
1. Blank spaces are reserved. No access is allowed.

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Note:

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0156h	Timer RD Counter 1	TRD1	343, 362, 380, 412
0157h			
0158h	Timer RD General Register A1	TRDGRA1	344, 363, 381, 397, 412, 430
0159h			
015Ah	Timer RD General Register B1	TRDGRB1	344, 363, 381, 397, 412, 430
015Bh			
015Ch	Timer RD General Register C1	TRDGRC1	344, 363, 381, 397, 412, 430
015Dh			
015Eh	Timer RD General Register D1	TRDGRD1	344, 363, 381, 397, 412, 430
015Fh			

Address	Register	Symbol	Page
0160h	UART1 Transmit/Receive Mode Register	U1MR	496
0161h	UART1 Bit Rate Register	U1BRG	496
0162h	UART1 Transmit Buffer Register	U1TB	497
0163h			
0164h	UART1 Transmit/Receive Control Register 0	U1C0	498
0165h	UART1 Transmit/Receive Control Register 1	U1C1	498
0166h	UART1 Receive Buffer Register	U1RB	499
0167h			
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h	Timer RG Mode Register	TRGMR	463
0171h	Timer RG Count Control Register	TRGCNTC	464
0172h	Timer RG Control Register	TRGCR	465, 489
0173h	Timer RG Interrupt Enable Register	TRGIER	466
0174h	Timer RG Status Register	TRGSR	467
0175h	Timer RG I/O Control Register	TRGIOR	468, 477, 481
0176h	Timer RG Counter	TRG	469
0177h			
0178h	Timer RG General Register A	TRGGRA	470
0179h			
017Ah	Timer RG General Register B	TRGGRB	470
017Bh			
017Ch	Timer RG General Register C	TRGGRC	470
017Dh			
017Eh	Timer RG General Register D	TRGGRD	470
017Fh			
0180h	Timer RA Pin Select Register	TRASR	87, 243
0181h	Timer RB/RC Pin Select Register	TRBRCSR	88, 261, 288
0182h	Timer RC Pin Select Register 0	TRCPSR0	89, 289
0183h	Timer RC Pin Select Register 1	TRCPSR1	90, 290
0184h	Timer RD Pin Select Register 0	TRDPSR0	91, 345, 364, 382, 398, 414, 432
0185h	Timer RD Pin Select Register 1	TRDPSR1	92, 346, 365, 383, 399, 415, 433
0186h			
0187h	Timer RG Pin Select Register	TRGPSR	93
0188h	UART0 Pin Select Register	U0SR	93, 500
0189h	UART1 Pin Select Register	U1SR	94, 501
018Ah	UART2 Pin Select Register 0	U2SR0	95, 525
018Bh	UART2 Pin Select Register 1	U2SR1	96, 526
018Ch	SSU/IIC Pin Select Register	SSUIICSR	97, 566, 597
018Dh	Key Input Pin Select Register	KISR	98, 192
018Eh	INT Interrupt Input Pin Select Register	INTSR	99, 185
018Fh			

Note:
1. Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Page
0190h			
0191h			
0192h			
0193h	SS Bit Counter Register	SSBR	567
0194h	SS Transmit Data Register L / IIC bus Transmit Data Register	SSTDR/ ICDRT	567, 598
0195h	SS Transmit Data Register H	SSTDRH	567
0196h	SS Receive Data Register L / IIC bus Receive Data Register	SSRDR/ ICDRR	568, 598
0197h	SS Receive Data Register H	SSRDRH	568
0198h	SS Control Register H / IIC bus Control Register 1	SSCRH / ICCR1	568, 599
0199h	SS Control Register L / IIC bus Control Register 2	SSCRL / ICCR2	569, 600
019Ah	SS Mode Register / IIC bus Mode Register	SSMR / ICMR	570, 601
019Bh	SS Enable Register / IIC bus Interrupt Enable Register	SSER / ICIER	571, 602
019Ch	SS Status Register / IIC bus Status Register	SSSR / ICSR	572, 603
019Dh	SS Mode Register 2 / Slave Address Register	SSMR2 / SAR	573, 604
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	726
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	728
01B5h	Flash Memory Control Register 1	FMR1	730
01B6h	Flash Memory Control Register 2	FMR2	732
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			
01C0h	Address Match Interrupt Register 0	RMAD0	196
01C1h			
01C2h			
01C3h	Address Match Interrupt Enable Register 0	AIER0	196
01C4h	Address Match Interrupt Register 1	RMAD1	196
01C5h			
01C6h			
01C7h	Address Match Interrupt Enable Register 1	AIER1	196
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			

Address	Register	Symbol	Page
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	Port P0 Pull-Up Control Register	P0PUR	99
01E1h	Port P1 Pull-Up Control Register	P1PUR	99
01E2h	Port P2 Pull-Up Control Register	P2PUR	99
01E3h	Port P3 Pull-Up Control Register	P3PUR	99
01E4h	Port P4 Pull-Up Control Register	P4PUR	99
01E5h	Port P5 Pull-Up Control Register	P5PUR	99
01E6h	Port P6 Pull-Up Control Register	P6PUR	99
01E7h	Port P7 Pull-Up Control Register	P7PUR	99
01E8h			
01E9h			
01EAh	Port P10 Pull-Up Control Register	P10PUR	100
01EBh	Port P11 Pull-Up Control Register	P11PUR	100
01ECh	Port P12 Pull-Up Control Register	P12PUR	100
01EDh	Port P13 Pull-Up Control Register	P13PUR	100
01EEh			
01EFh			
01F0h	Port P10 Drive Capacity Control Register	P10DRR	100
01F1h	Port P11 Drive Capacity Control Register	P11DRR	101
01F2h			
01F3h			
01F4h			
01F5h	Input Threshold Control Register 0	VLT0	101
01F6h	Input Threshold Control Register 1	VLT1	102
01F7h	Input Threshold Control Register 2	VLT2	103
01F8h	Comparator B Control Register 0	INTCMP	686
01F9h			
01FAh	External Input Enable Register 0	INTEN	186, 686
01FBh	External Input Enable Register 1	INTEN1	187
01FCh	INT Input Filter Select Register 0	INTF	188, 687
01FDh	INT Input Filter Select Register 1	INTF1	188
01FEh	Key Input Enable Register 0	KIEN	193
01FFh	Key Input Enable Register 1	KIEN1	194

Note:
1. Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Page
0200h	LCD Control Register	LCR0	694
0201h	LCD Bias Control Register	LCR1	695
0202h	LCD Display Control Register	LCR2	696
0203h	LCD Clock Control Register	LCR3	696
0204h			
0205h			
0206h	LCD Port Select Register 0	LSE0	697
0207h	LCD Port Select Register 1	LSE1	697
0208h	LCD Port Select Register 2	LSE2	698
0209h	LCD Port Select Register 3	LSE3	698
020Ah	LCD Port Select Register 4	LSE4	699
020Bh	LCD Port Select Register 5	LSE5	699
020Ch	LCD Port Select Register 6	LSE6	700
020Dh	LCD Port Select Register 7	LSE7	700
020Eh			
020Fh			
0210h	LCD Display Data Register	LRA0L	701
0211h		LRA1L	701
0212h		LRA2L	701
0213h		LRA3L	701
0214h		LRA4L	701
0215h		LRA5L	701
0216h		LRA6L	701
0217h		LRA7L	701
0218h		LRA8L	701
0219h		LRA9L	701
021Ah		LRA10L	701
021Bh		LRA11L	701
021Ch		LRA12L	701
021Dh		LRA13L	701
021Eh		LRA14L	701
021Fh		LRA15L	701
0220h		LRA16L	701
0221h		LRA17L	701
0222h		LRA18L	701
0223h		LRA19L	701
0224h		LRA20L	701
0225h		LRA21L	701
0226h		LRA22L	701
0227h		LRA23L	701
0228h		LRA24L	701
0229h		LRA25L	701
022Ah		LRA26L	701
022Bh		LRA27L	701
022Ch		LRA28L	701
022Dh		LRA29L	701
022Eh		LRA30L	701
022Fh		LRA31L	701
0230h		LRA32L	701
0231h		LRA33L	701
0232h		LRA34L	701
0233h		LRA35L	701
0234h		LRA36L	701
0235h		LRA37L	701
0236h		LRA38L	701
0237h		LRA39L	701
0238h		LRA40L	701
0239h		LRA41L	701
023Ah		LRA42L	701
023Bh		LRA43L	701
023Ch		LRA44L	701
023Dh		LRA45L	701
023Eh		LRA46L	701
023Fh		LRA47L	701

Address	Register	Symbol	Page
0240h	LCD Display Data Register	LRA48L	701
0241h		LRA49L	701
0242h		LRA50L	701
0243h		LRA51L	701
0244h		LRA52L	701
0245h		LRA53L	701
0246h		LRA54L	701
0247h		LRA55L	701
0248h		LRA56L	701
0249h		LRA57L	701
024Ah		LRA58L	701
024Bh		LRA59L	701
024Ch		LRA60L	701
024Dh		LRA61L	701
024Eh		LRA62L	701
024Fh		LRA63L	701
0250h		LRA64L	701
0251h		LRA65L	701
0252h		LRA66L	701
0253h		LRA67L	701
0254h		LRA68L	701
0255h		LRA69L	701
0256h		LRA70L	701
0257h		LRA71L	701
0258h		LRA72L	701
0259h		LRA73L	701
025Ah		LRA74L	701
025Bh		LRA75L	701
025Ch		LRA76L	701
025Dh		LRA77L	701
025Eh		LRA78L	701
025Fh		LRA79L	701
0260h		LRA80L	701
0261h		LRA81L	701
0262h		LRA82L	701
0263h		LRA83L	701
0264h		LRA84L	701
0265h		LRA85L	701
0266h		LRA86L	701
0267h		LRA87L	701
0268h		LRA88L	701
0269h		LRA89L	701
026Ah		LRA90L	701
026Bh		LRA91L	701
026Ch		LRA92L	701
026Dh		LRA93L	701
026Eh		LRA94L	701
026Fh		LRA95L	701
0270h	LCD Display Control Data Register	LRA0H	702
0271h		LRA1H	702
0272h		LRA2H	702
0273h		LRA3H	702
0274h		LRA4H	702
0275h		LRA5H	702
0276h		LRA6H	702
0277h		LRA7H	702
0278h		LRA8H	702
0279h		LRA9H	702
027Ah		LRA10H	702
027Bh		LRA11H	702
027Ch		LRA12H	702
027Dh		LRA13H	702
027Eh		LRA14H	702
027Fh		LRA15H	702

Address	Register	Symbol	Page
0280h	LCD Display Control Data Register	LRA16H	702
0281h		LRA17H	702
0282h		LRA18H	702
0283h		LRA19H	702
0284h		LRA20H	702
0285h		LRA21H	702
0286h		LRA22H	702
0287h		LRA23H	702
0288h		LRA24H	702
0289h		LRA25H	702
028Ah		LRA26H	702
028Bh		LRA27H	702
028Ch		LRA28H	702
028Dh		LRA29H	702
028Eh		LRA30H	702
028Fh		LRA31H	702
0290h		LRA32H	702
0291h		LRA33H	702
0292h		LRA34H	702
0293h		LRA35H	702
0294h		LRA36H	702
0295h		LRA37H	702
0296h		LRA38H	702
0297h		LRA39H	702
0298h		LRA40H	702
0299h		LRA41H	702
029Ah		LRA42H	702
029Bh		LRA43H	702
029Ch		LRA44H	702
029Dh		LRA45H	702
029Eh		LRA46H	702
029Fh		LRA47H	702
02A0h		LRA48H	702
02A1h		LRA49H	702
02A2h		LRA50H	702
02A3h		LRA51H	702
02A4h		LRA52H	702
02A5h		LRA53H	702
02A6h		LRA54H	702
02A7h		LRA55H	702
02A8h		LRA56H	702
02A9h		LRA57H	702
02AAh		LRA58H	702
02ABh		LRA59H	702
02ACh		LRA60H	702
02ADh		LRA61H	702
02AEh		LRA62H	702
02AFh		LRA63H	702
02B0h		LRA64H	702
02B1h		LRA65H	702
02B2h		LRA66H	702
02B3h		LRA67H	702
02B4h		LRA68H	702
02B5h		LRA69H	702
02B6h		LRA70H	702
02B7h		LRA71H	702
02B8h		LRA72H	702
02B9h		LRA73H	702
02BAh		LRA74H	702
02BBh		LRA75H	702
02BCh		LRA76H	702
02BDh		LRA77H	702
02BEh		LRA78H	702
02BFh		LRA79H	702

Note:
1. Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Page
02C0h	LCD Display Control Data Register	LRA80H	702
02C1h		LRA81H	702
02C2h		LRA82H	702
02C3h		LRA83H	702
02C4h		LRA84H	702
02C5h		LRA85H	702
02C6h		LRA86H	702
02C7h		LRA87H	702
02C8h		LRA88H	702
02C9h		LRA89H	702
02CAh		LRA90H	702
02CBh		LRA91H	702
02CCh		LRA92H	702
02CDh		LRA93H	702
02CEh		LRA94H	702
02CFh		LRA95H	702
02D0h			
02D1h			
02D2h			
02D3h			
02D4h			
02D5h			
02D6h			
02D7h			
02D8h			
02D9h			
02DAh			
02DBh			
02DCh			
02DDh			
02DEh			
02DFh			
02E0h			
02E1h			
02E2h			
02E3h			
02E4h			
02E5h			
02E6h			
02E7h			
02E8h			
02E9h			
02EAh			
02EBh			
02ECh			
02EDh			
02EEh			
02EFh			
02F0h			
02F1h			
02F2h			
02F3h			
02F4h			
02F5h			
02F6h			
02F7h			
02F8h			
02F9h			
02FAh			
02FBh			
02FCh			
02FDh			
02FEh			
02FFh			

Note:
1. Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Page
2C00h	DTC Transfer Vector Area		
2C01h	DTC Transfer Vector Area		
2C02h	DTC Transfer Vector Area		
2C03h	DTC Transfer Vector Area		
2C04h	DTC Transfer Vector Area		
2C05h	DTC Transfer Vector Area		
2C06h	DTC Transfer Vector Area		
2C07h	DTC Transfer Vector Area		
2C08h	DTC Transfer Vector Area		
2C09h	DTC Transfer Vector Area		
2C0Ah	DTC Transfer Vector Area		
:	DTC Transfer Vector Area		
:	DTC Transfer Vector Area		
2C3Ah	DTC Transfer Vector Area		
2C3Bh	DTC Transfer Vector Area		
2C3Ch	DTC Transfer Vector Area		
2C3Dh	DTC Transfer Vector Area		
2C3Eh	DTC Transfer Vector Area		
2C3Fh	DTC Transfer Vector Area		
2C40h	DTC Control Data 0	DTCD0	
2C41h			
2C42h			
2C43h			
2C44h			
2C45h			
2C46h			
2C47h			
2C48h	DTC Control Data 1	DTCD1	
2C49h			
2C4Ah			
2C4Bh			
2C4Ch			
2C4Dh			
2C4Eh			
2C4Fh			
2C50h	DTC Control Data 2	DTCD2	
2C51h			
2C52h			
2C53h			
2C54h			
2C55h			
2C56h			
2C57h			
2C58h	DTC Control Data 3	DTCD3	
2C59h			
2C5Ah			
2C5Bh			
2C5Ch			
2C5Dh			
2C5Eh			
2C5Fh			
2C60h	DTC Control Data 4	DTCD4	
2C61h			
2C62h			
2C63h			
2C64h			
2C65h			
2C66h			
2C67h			
2C68h	DTC Control Data 5	DTCD5	
2C69h			
2C6Ah			
2C6Bh			
2C6Ch			
2C6Dh			
2C6Eh			
2C6Fh			

Address	Register	Symbol	Page
2C70h	DTC Control Data 6	DTCD6	
2C71h			
2C72h			
2C73h			
2C74h			
2C75h			
2C76h			
2C77h			
2C78h	DTC Control Data 7	DTCD7	
2C79h			
2C7Ah			
2C7Bh			
2C7Ch			
2C7Dh			
2C7Eh			
2C7Fh			
2C80h	DTC Control Data 8	DTCD8	
2C81h			
2C82h			
2C83h			
2C84h			
2C85h			
2C86h			
2C87h			
2C88h	DTC Control Data 9	DTCD9	
2C89h			
2C8Ah			
2C8Bh			
2C8Ch			
2C8Dh			
2C8Eh			
2C8Fh			
2C90h	DTC Control Data 10	DTCD10	
2C91h			
2C92h			
2C93h			
2C94h			
2C95h			
2C96h			
2C97h			
2C98h	DTC Control Data 11	DTCD11	
2C99h			
2C9Ah			
2C9Bh			
2C9Ch			
2C9Dh			
2C9Eh			
2C9Fh			
2CA0h	DTC Control Data 12	DTCD12	
2CA1h			
2CA2h			
2CA3h			
2CA4h			
2CA5h			
2CA6h			
2CA7h			
2CA8h	DTC Control Data 13	DTCD13	
2CA9h			
2CAAh			
2CABh			
2CACh			
2CADh			
2CAEh			
2CAFh			

Address	Register	Symbol	Page
2CB0h	DTC Control Data 14	DTCD14	
2CB1h			
2CB2h			
2CB3h			
2CB4h			
2CB5h			
2CB6h			
2CB7h			
2CB8h	DTC Control Data 15	DTCD15	
2CB9h			
2CBAh			
2CBBh			
2CBCh			
2CBDh			
2CBEh			
2CBFh			
2CC0h	DTC Control Data 16	DTCD16	
2CC1h			
2CC2h			
2CC3h			
2CC4h			
2CC5h			
2CC6h			
2CC7h			
2CC8h	DTC Control Data 17	DTCD17	
2CC9h			
2CCAh			
2CCBh			
2CCCh			
2CCDh			
2CCEh			
2CCFh			
2CD0h	DTC Control Data 18	DTCD18	
2CD1h			
2CD2h			
2CD3h			
2CD4h			
2CD5h			
2CD6h			
2CD7h			
2CD8h	DTC Control Data 19	DTCD19	
2CD9h			
2CDAh			
2CDBh			
2CDCh			
2CDDh			
2CDEh			
2CDFh			
2CE0h	DTC Control Data 20	DTCD20	
2CE1h			
2CE2h			
2CE3h			
2CE4h			
2CE5h			
2CE6h			
2CE7h			
2CE8h	DTC Control Data 21	DTCD21	
2CE9h			
2CEAh			
2CEBh			
2CECh			
2CEDh			
2CEEh			
2CEFh			

Note:
1. Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Page
2CF0h	DTC Control Data 22	DTCD22	
2CF1h			
2CF2h			
2CF3h			
2CF4h			
2CF5h			
2CF6h			
2CF7h			
2CF8h	DTC Control Data 23	DTCD23	
2CF9h			
2CFAh			
2CFBh			
2CFCh			
2CFDh			
2CFEh			
2CFFh			
2D00h			
2D01h			
:			
0FFDBh	Option Function Select Register 2	OFS2	53, 208, 215
:			
0FFFFh	Option Function Select Register	OFS	52, 71, 207, 214, 724

Note:
1. Blank spaces are reserved. No access is allowed.

1. Overview

1.1 Features

The R8C/L35A Group, R8C/L36A Group, R8C/L38A Group, R8C/L3AA Group, R8C/L35B Group, R8C/L36B Group, R8C/L38B Group, and R8C/L3AB Group of single-chip MCUs incorporate the R8C CPU core, which implements a powerful instruction set for a high level of efficiency and supports a 1 Mbyte address space, allowing execution of instructions at high speed. In addition, the CPU core integrates a multiplier for high-speed operation processing.

Power consumption is low, and the supported operating modes allow for additional power control. These MCUs use an anti-noise configuration to reduce emissions of electromagnetic noise and are designed to withstand EMI.

Integration of many peripheral functions, including multifunction timer and serial interface, helps reduce the number of system components.

1.1.1 Applications

Household appliances, office equipment, audio equipment, consumer products, etc.

1.1.2 Differences between Groups

Tables 1.1 and 1.2 list the differences between the groups, and Table 1.3 lists the I/O ports provided for each group. Figures 1.13 to 1.17 show the pin assignment for each group, and Tables 1.7 to 1.14 list product information.

The explanations in the chapters which follow apply to the R8C/L3AA Group only. Note the differences shown below.

Table 1.1 Differences between Groups (1)

Item	Function	R8C/L35A Group, R8C/L36A Group R8C/L38A Group, R8C/L3AA Group	R8C/L35B Group, R8C/L36B Group R8C/L38B Group, R8C/L3AB Group
Data flash	1 KB × 4 blocks with BGO (background operation) function	Provided	Not provided

Table 1.2 Differences between Groups (2)

Item	Function	R8C/L35A Group R8C/L35B Group	R8C/L36A Group R8C/L36B Group	R8C/L38A Group R8C/L38B Group	R8C/L3AA Group R8C/L3AB Group
I/O Ports	Programmable I/O ports	41 pins	52 pins	68 pins	88 pins
	High current drive ports	5 pins	8 pins	8 pins	16 pins
Interrupts	$\overline{\text{INT}}$ interrupt pins	5 pins	8 pins	8 pins	8 pins
	Key input interrupt pins	4 pins	4 pins	8 pins	8 pins
Timers	Timer RA pins (I/O: 1, output: 1)	1 pin (I/O pin only)	2 pins	2 pins	2 pins
	Timer RB pin (output: 1)	None	1 pin	1 pin	1 pin
	Timer RD pin (I/O: 8)	None	None	8 pins	8 pins
	Timer RE pin (output: 1)	None	1 pin	1 pin	1 pin
	Timer RG pin (I/O: 2, output: 2)	None	None	None	4 pins
A/D Converter	Analog input pin	12 pins	12 pins	16 pins	20 pins
LCD Drive Control Circuit	LCD power supply	3 pins (VL1, VL2, VL4)	4 pins (VL1 to VL4)	4 pins (VL1 to VL4)	4 pins (VL1 to VL4)
	Common output pins	Max. 4 pins	Max. 8 pins	Max. 8 pins	Max. 8 pins
	Segment output pins	Max. 24 pins	Max. 32 pins	Max. 48 pins	Max. 56 pins
Other Pin Function	$\overline{\text{WKUP1}}$	Not supported	Supported	Supported	Supported
Packages		52-pin LQFP	64-pin LQFP	80-pin LQFP	100-pin LQFP/ 100-pin QFP

Note:
1. I/O ports are shared with I/O functions, such as interrupts or timers.
   Refer to Tables 1.15 to 1.17, Pin Name Information by Pin Number, for details.

Table 1.3 Programmable I/O Ports Provided for Each Group

Programmable I/O Port	R8C/L35A Group R8C/L35B Group Total: 41 I/O pins								R8C/L36A Group R8C/L36B Group Total: 52 I/O pins								R8C/L38A Group R8C/L38B Group Total: 68 I/O pins								R8C/L3AA Group R8C/L3AB Group Total: 88 I/O pins							
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
P0	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√
P1	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	√	√	√	√	√	√	√	√	√	√	√	√
P2	√	√	√	√	–	–	–	–	√	√	√	√	–	–	–	–	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√
P3	–	–	–	–	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√
P4	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√
P5	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	√	√	√	√
P6	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√
P7	√	√	√	√	–	–	–	–	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√
P10	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	√	√	√	√	√	√	√	√
P11	–	–	–	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√
P12	–	–	–	–	√	√	√	√	–	–	–	–	√	√	√	√	–	–	–	–	√	√	√	√	–	–	–	–	√	√	√	√
P13	–	–	–	–	√	√	√	√	–	–	–	–	√	√	√	√	–	–	–	–	√	√	√	√	√	√	√	√	√	√	√	√

Note:
1. The symbol "√" indicates a programmable I/O port.

1.1.3 Specifications

Tables 1.4 to 1.6 list the specifications.

Table 1.4 Specifications (1)

Item	Function		Specification
CPU	Central processing unit		R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V) 200 ns (f(XIN) = 5 MHz, VCC = 1.8 to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operating mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM/RAM Data flash		Refer to Tables 1.7 to 1.14 Product Lists.
Power Supply Voltage Detection	Voltage detection circuit		• Power-on reset • Voltage detection 3 (detection level of voltage detection 0 and voltage detection 1 selectable)
I/O Ports	Programmable I/O ports	R8C/L35A Group R8C/L35B Group	• CMOS I/O ports: 41, selectable pull-up resistor • High current drive ports: 5
		R8C/L36A Group R8C/L36B Group	• CMOS I/O ports: 52, selectable pull-up resistor • High current drive ports: 8
		R8C/L38A Group R8C/L38B Group	• CMOS I/O ports: 68, selectable pull-up resistor • High current drive ports: 8
		R8C/L3AA Group R8C/L3AB Group	• CMOS I/O ports: 88, selectable pull-up resistor • High current drive ports: 16
Clock	Clock generation circuits		4 circuits: XIN clock oscillation circuit XCIN clock oscillation circuit (32 kHz) High-speed on-chip oscillator (with frequency adjustment function) Low-speed on-chip oscillator • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Division ratio selectable from 1, 2, 4, 8, and 16 • Low-power-consumption modes: Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode, power-off mode
			Real-time clock (timer RE)
Interrupts		R8C/L35A Group R8C/L35B Group	• Number of interrupt vectors: 69 • External Interrupt: 9 ($\overline{\text{INT}}$ × 5, key input × 4) • Priority levels: 7 levels
		R8C/L36A Group R8C/L36B Group	• Number of interrupt vectors: 69 • External Interrupt: 12 ($\overline{\text{INT}}$ × 8, key input × 4) • Priority levels: 7 levels
		R8C/L38A Group R8C/L38B Group	• Number of interrupt vectors: 69 • External Interrupt: 16 ($\overline{\text{INT}}$ × 8, key input × 8) • Priority levels: 7 levels
		R8C/L3AA Group R8C/L3AB Group	• Number of interrupt vectors: 69 • External Interrupt: 16 ($\overline{\text{INT}}$ × 8, key input × 8) • Priority levels: 7 levels
Watchdog Timer			• 14 bits × 1 (with prescaler) • Selectable reset start function • Selectable low-speed on-chip oscillator for watchdog timer
DTC (Data Transfer Controller)			• 1 channel • Activation sources: 38 • Transfer modes: 2 (normal mode, repeat mode)

Table 1.5 Specifications (2)

Item	Function	Specification	
Timer	Timer RA	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode	
	Timer RB	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode	
	Timer RC	16 bits × 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output: 3 pins), PWM2 mode (PWM output: 1 pin)	
	Timer RD	16 bits × 2 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output: 6 pins), reset synchronous PWM mode (three-phase waveform output: 6 pins, sawtooth wave modulation), complementary PWM mode (three-phase waveform output: 6 pins, triangular wave modulation), PWM3 mode (PWM output with fixed period: 2 pins)	
	Timer RE	8 bits × 1 Real-time clock mode (counting of seconds, minutes, hours, days of week), output compare mode	
	Timer RG	16 bits × 1 Phase-counting mode, timer mode (output compare function, input capture function), PWM mode (output: 1 pin)	
Serial Interface	UART0, UART1	Clock synchronous serial I/O/UART × 2 channels	
	UART2	Clock synchronous serial I/O/UART, I^2C mode (I^2C-bus), multiprocessor communication function	
Synchronous Serial Communication Unit (SSU)		1 (shared with I^2C-bus)	
I^2C bus		1 (shared with SSU)	
LIN Module		Hardware LIN: 1 channel (timer RA, UART0 used)	
A/D Converter	R8C/L35A Group R8C/L35B Group	10-bit resolution × 12 channels, including sample and hold function, with sweep mode	
	R8C/L36A Group R8C/L36B Group	10-bit resolution × 12 channels, including sample and hold function, with sweep mode	
	R8C/L38A Group R8C/L38B Group	10-bit resolution × 16 channels, including sample and hold function, with sweep mode	
	R8C/L3AA Group R8C/L3AB Group	10-bit resolution × 20 channels, including sample and hold function, with sweep mode	
D/A Converter		8-bit resolution × 2 circuits	
Comparator A		• 2 circuits (shared with voltage monitor 1 and voltage monitor 2) • External reference voltage input available	
Comparator B		2 circuits	
LCD Drive Control Circuit	R8C/L35A Group R8C/L35B Group	Common output: Max. 4 pins Segment output: Max. 24 pins	Bias: 1/2, 1/3 Duty: static, 1/2, 1/3, 1/4
	R8C/L36A Group R8C/L36B Group	Common output: Max. 8 pins Segment output: Max. 32 pins (1)	Bias: 1/2, 1/3, 1/4 Duty: static, 1/2, 1/3, 1/4, 1/8
	R8C/L38A Group R8C/L38B Group	Common output: Max. 8 pins Segment output: Max. 48 pins (1)	
	R8C/L3AA Group R8C/L3AB Group	Common output: Max. 8 pins Segment output: Max. 56 pins (1)	
		Voltage multiplier and dedicated regulator integrated	

Notes:
1. This applies when four pins are selected for common output.

Table 1.6 Specifications (2)

Item	Function	Specification
Flash Memory	R8C/L35A Group R8C/L36A Group R8C/L38A Group R8C/L3AA Group	• Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function • Background operation (BGO) function
	R8C/L35B Group R8C/L36B Group R8C/L38B Group R8C/L3AB Group	• Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 1,000 times • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function
Operating Frequency/ Supply Voltage		f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V) f(XIN) = 5 MHz (VCC = 1.8 to 5.5 V)
Current Consumption		TBD (VCC = 5.0 V, f(XIN) = 20 MHz) TBD (VCC = 3.0 V, f(XIN) = 10 MHz) TBD (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz)) TBD (VCC = 3.0 V, stop mode) TBD (VCC = 3.0 V, power-off mode, timer RE enabled) TBD (VCC = 3.0 V, power-off mode, timer RE disabled)
Operating Ambient Temperature		-20 to 85°C (N version) -40 to 85°C (D version) (1)

Note:
1. Specify the D version if D version functions are to be used.

1.2 Product Lists

Tables 1.7 to 1.14 list product information for each group. Figure 1.1 to 1.8 show the Correspondence of Part No., with Memory Size and Package of R8C/Lx Group.

Table 1.7 Product List for R8C/L35A Group **Current of Jul 2008**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2L357ANFP (D)	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0052JA-A	N Version
R5F2L358ANFP (D)	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0052JA-A	
R5F2L35AANFP (D)	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0052JA-A	
R5F2L35CANFP (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0052JA-A	
R5F2L357ADFP (D)	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0052JA-A	D Version
R5F2L358ADFP (D)	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0052JA-A	
R5F2L35AADFP (D)	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0052JA-A	
R5F2L35CADFP (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0052JA-A	

(D): Under development

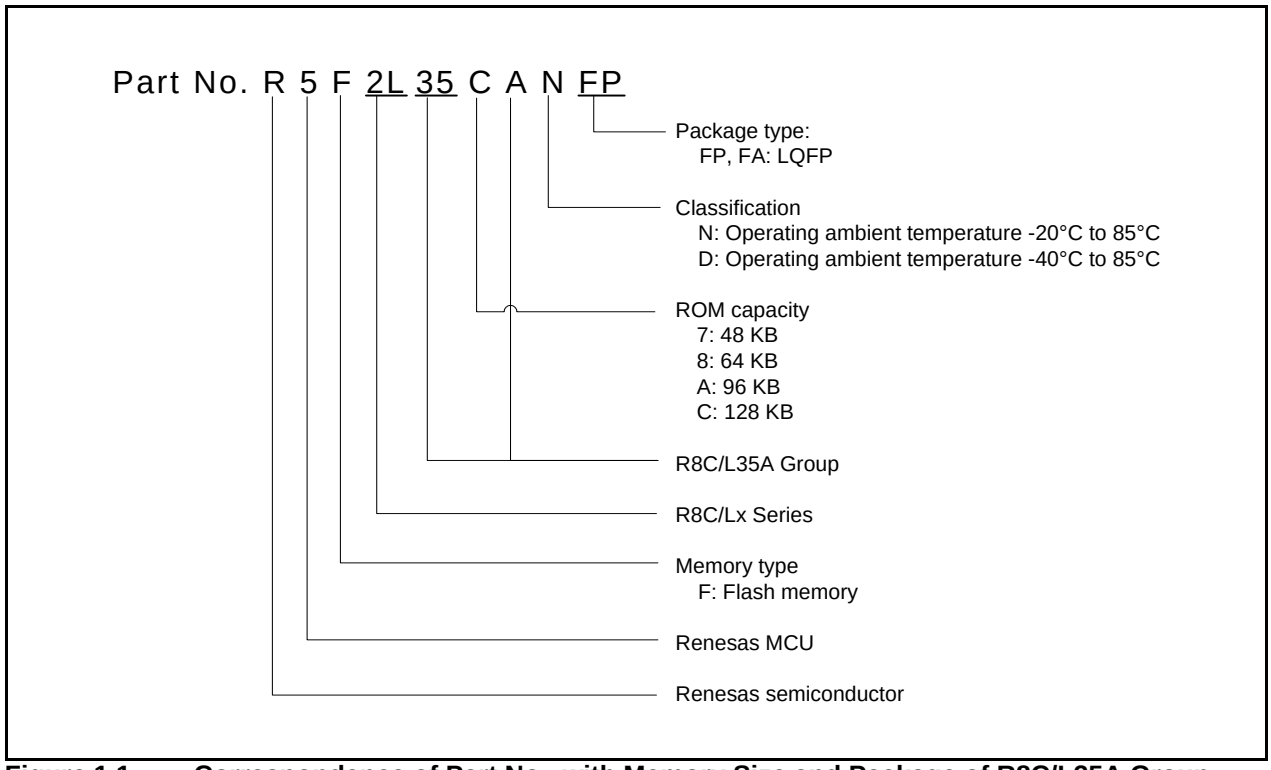


Figure 1.1 Correspondence of Part No., with Memory Size and Package of R8C/L35A Group

Table 1.8 Product List for R8C/L35B Group **Current of Jul 2008**

Part No.	Internal ROM Capacity	Internal RAM Capacity	Package Type	Remarks
R5F2L357BNFP (D)	48 Kbytes	6 Kbytes	PLQP0052JA-A	N Version
R5F2L358BNFP (D)	64 Kbytes	8 Kbytes	PLQP0052JA-A	
R5F2L35ABNFP (D)	96 Kbytes	10 Kbytes	PLQP0052JA-A	
R5F2L35CBNFP (D)	128 Kbytes	10 Kbytes	PLQP0052JA-A	
R5F2L357BDFP (D)	48 Kbytes	6 Kbytes	PLQP0052JA-A	D Version
R5F2L358BDFP (D)	64 Kbytes	8 Kbytes	PLQP0052JA-A	
R5F2L35ABDFP (D)	96 Kbytes	10 Kbytes	PLQP0052JA-A	
R5F2L35CBDFP (D)	128 Kbytes	10 Kbytes	PLQP0052JA-A	

(D): Under development

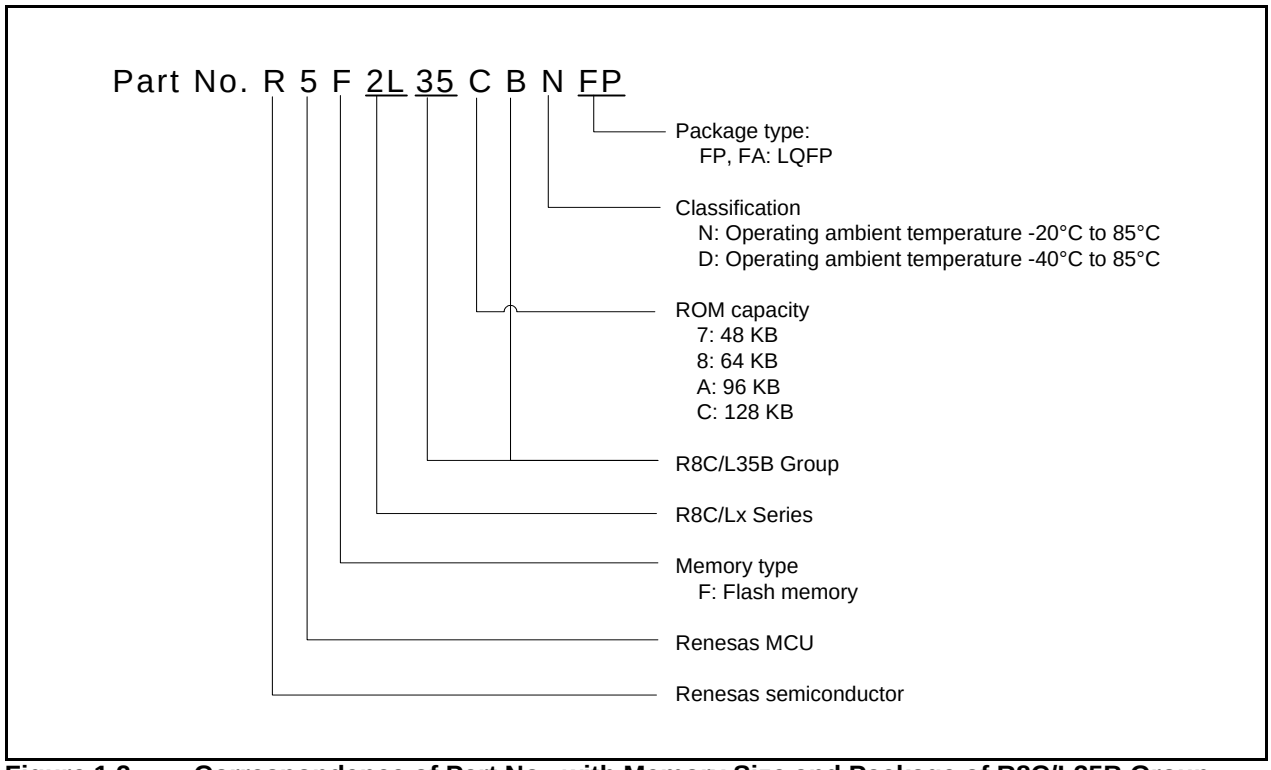


Figure 1.2 Correspondence of Part No., with Memory Size and Package of R8C/L35B Group

Table 1.9 Product List for R8C/L36A Group **Current of Jul 2008**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2L367ANFP (D)	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064KB-A	N Version
R5F2L367ANFA (D)	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064GA-A	
R5F2L368ANFP (D)	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064KB-A	
R5F2L368ANFA (D)	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064GA-A	
R5F2L36AANFP (D)	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A	
R5F2L36AANFA (D)	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A	
R5F2L36CANFP (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A	
R5F2L36CANFA (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A	
R5F2L367ADFP (D)	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064KB-A	D Version
R5F2L367ADFA (D)	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064GA-A	
R5F2L368ADFP (D)	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064KB-A	
R5F2L368ADFA (D)	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064GA-A	
R5F2L36AADFP (D)	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A	
R5F2L36AADFA (D)	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A	
R5F2L36CADFP (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A	
R5F2L36CADFA (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A	

(D): Under development

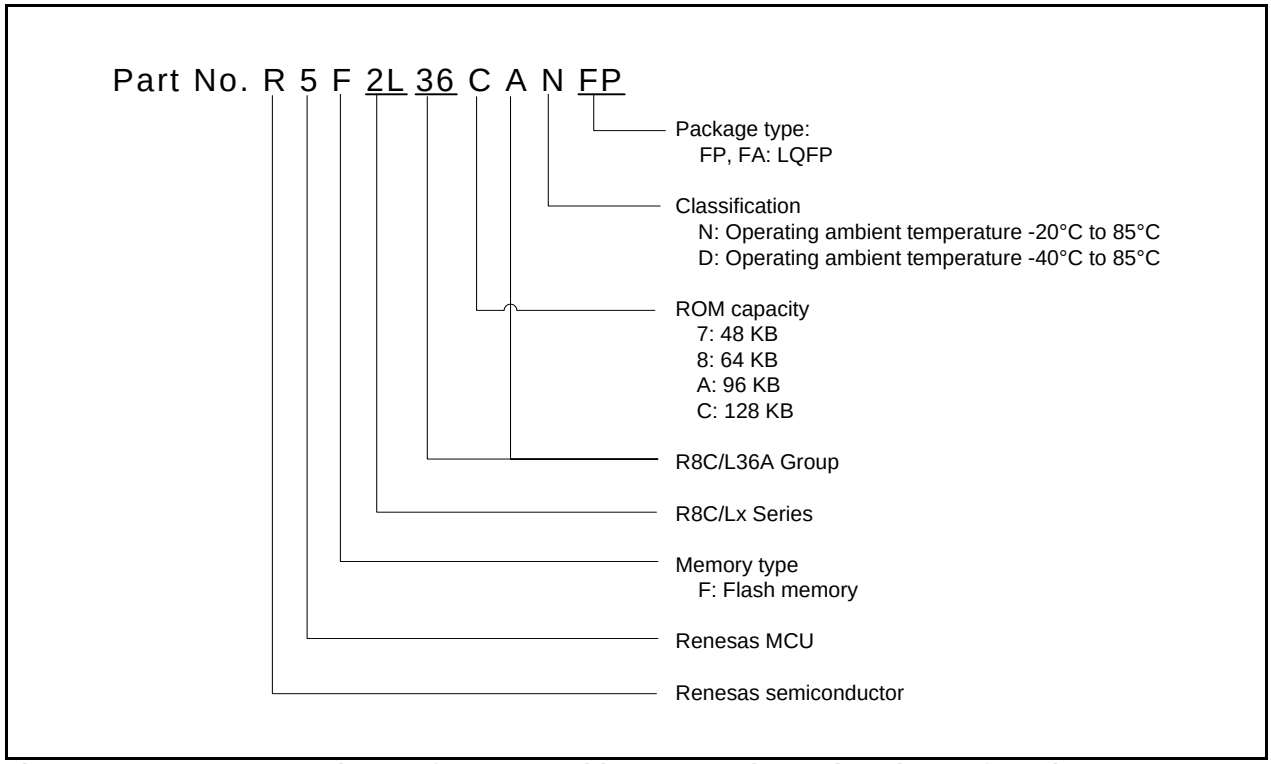


Figure 1.3 Correspondence of Part No., with Memory Size and Package of R8C/L36A Group

Table 1.10 Product List for R8C/L36B Group **Current of Jul 2008**

Part No.	Internal ROM Capacity	Internal RAM Capacity	Package Type	Remarks
R5F2L367BNFP (D)	48 Kbytes	6 Kbytes	PLQP0064KB-A	N Version
R5F2L367BNFA (D)	48 Kbytes	6 Kbytes	PLQP0064GA-A	
R5F2L368BNFP (D)	64 Kbytes	8 Kbytes	PLQP0064KB-A	
R5F2L368BNFA (D)	64 Kbytes	8 Kbytes	PLQP0064GA-A	
R5F2L36ABNFP (D)	96 Kbytes	10 Kbytes	PLQP0064KB-A	
R5F2L36ABNFA (D)	96 Kbytes	10 Kbytes	PLQP0064GA-A	
R5F2L36CBNFP (D)	128 Kbytes	10 Kbytes	PLQP0064KB-A	
R5F2L36CBNFA (D)	128 Kbytes	10 Kbytes	PLQP0064GA-A	
R5F2L367BDFP (D)	48 Kbytes	6 Kbytes	PLQP0064KB-A	D Version
R5F2L367BDFA (D)	48 Kbytes	6 Kbytes	PLQP0064GA-A	
R5F2L368BDFP (D)	64 Kbytes	8 Kbytes	PLQP0064KB-A	
R5F2L368BDFA (D)	64 Kbytes	8 Kbytes	PLQP0064GA-A	
R5F2L36ABDFP (D)	96 Kbytes	10 Kbytes	PLQP0064KB-A	
R5F2L36ABDFA (D)	96 Kbytes	10 Kbytes	PLQP0064GA-A	
R5F2L36CBDFP (D)	128 Kbytes	10 Kbytes	PLQP0064KB-A	
R5F2L36CBDFA (D)	128 Kbytes	10 Kbytes	PLQP0064GA-A	

(D): Under development

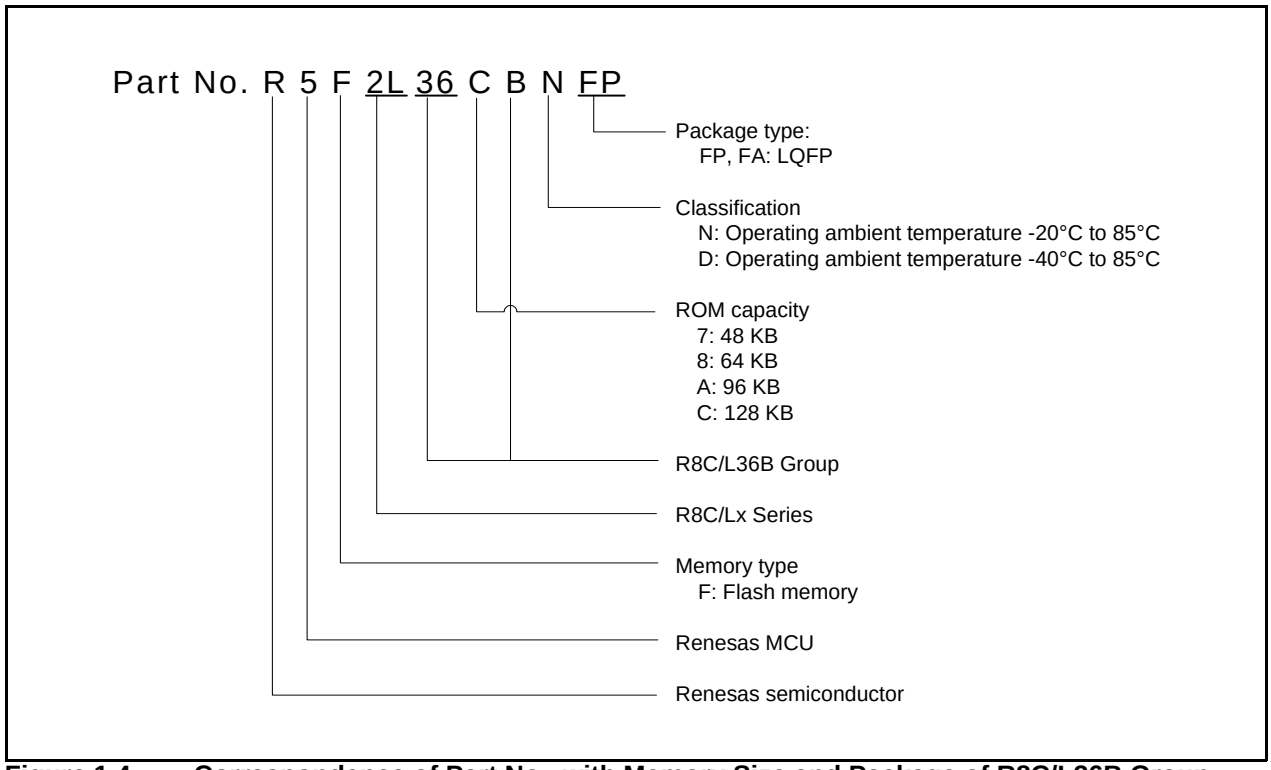


Figure 1.4 Correspondence of Part No., with Memory Size and Package of R8C/L36B Group

Table 1.11 Product List for R8C/L38A Group **Current of Jul 2008**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2L387ANFP (D)	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0080KB-A	N Version
R5F2L387ANFA (D)	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0080JA-A	
R5F2L388ANFP (D)	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0080KB-A	
R5F2L388ANFA (D)	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0080JA-A	
R5F2L38AANFP (D)	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080KB-A	
R5F2L38AANFA (D)	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080JA-A	
R5F2L38CANFP (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080KB-A	
R5F2L38CANFA (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080JA-A	
R5F2L387ADFP (D)	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0080KB-A	D Version
R5F2L387ADFA (D)	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0080JA-A	
R5F2L388ADFP (D)	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0080KB-A	
R5F2L388ADFA (D)	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0080JA-A	
R5F2L38AADFP (D)	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080KB-A	
R5F2L38AADFA (D)	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080JA-A	
R5F2L38CADFP (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080KB-A	
R5F2L38CADFA (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080JA-A	

(D): Under development

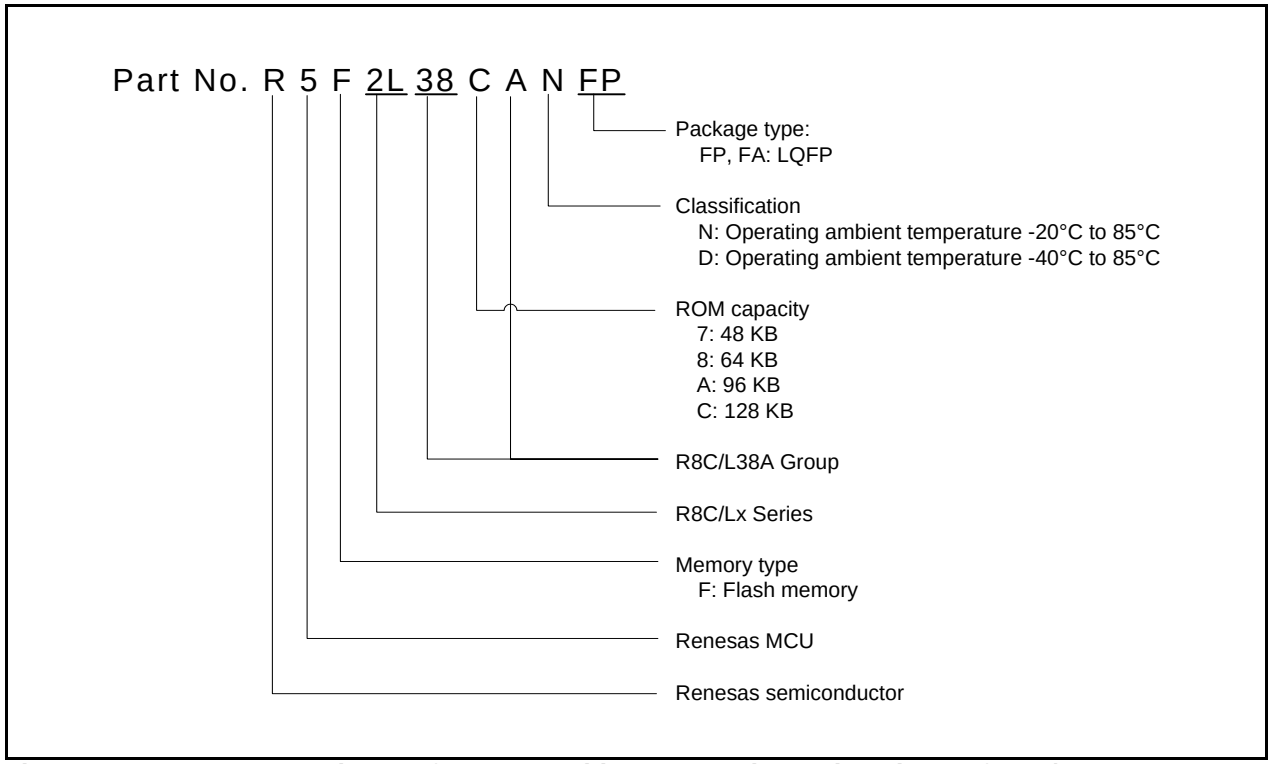


Figure 1.5 Correspondence of Part No., with Memory Size and Package of R8C/L38A Group

Table 1.12 Product List for R8C/L38B Group **Current of Jul 2008**

Part No.	Internal ROM Capacity	Internal RAM Capacity	Package Type	Remarks
R5F2L387BNFP (D)	48 Kbytes	6 Kbytes	PLQP0080KB-A	N Version
R5F2L387BNFA (D)	48 Kbytes	6 Kbytes	PLQP0080JA-A	
R5F2L388BNFP (D)	64 Kbytes	8 Kbytes	PLQP0080KB-A	
R5F2L388BNFA (D)	64 Kbytes	8 Kbytes	PLQP0080JA-A	
R5F2L38ABNFP (D)	96 Kbytes	10 Kbytes	PLQP0080KB-A	
R5F2L38ABNFA (D)	96 Kbytes	10 Kbytes	PLQP0080JA-A	
R5F2L38CBNFP (D)	128 Kbytes	10 Kbytes	PLQP0080KB-A	
R5F2L38CBNFA (D)	128 Kbytes	10 Kbytes	PLQP0080JA-A	
R5F2L387BDFP (D)	48 Kbytes	6 Kbytes	PLQP0080KB-A	D Version
R5F2L387BDFA (D)	48 Kbytes	6 Kbytes	PLQP0080JA-A	
R5F2L388BDFP (D)	64 Kbytes	8 Kbytes	PLQP0080KB-A	
R5F2L388BDFA (D)	64 Kbytes	8 Kbytes	PLQP0080JA-A	
R5F2L38ABDFP (D)	96 Kbytes	10 Kbytes	PLQP0080KB-A	
R5F2L38ABDFA (D)	96 Kbytes	10 Kbytes	PLQP0080JA-A	
R5F2L38CBDFP (D)	128 Kbytes	10 Kbytes	PLQP0080KB-A	
R5F2L38CBDFA (D)	128 Kbytes	10 Kbytes	PLQP0080JA-A	

(D): Under development

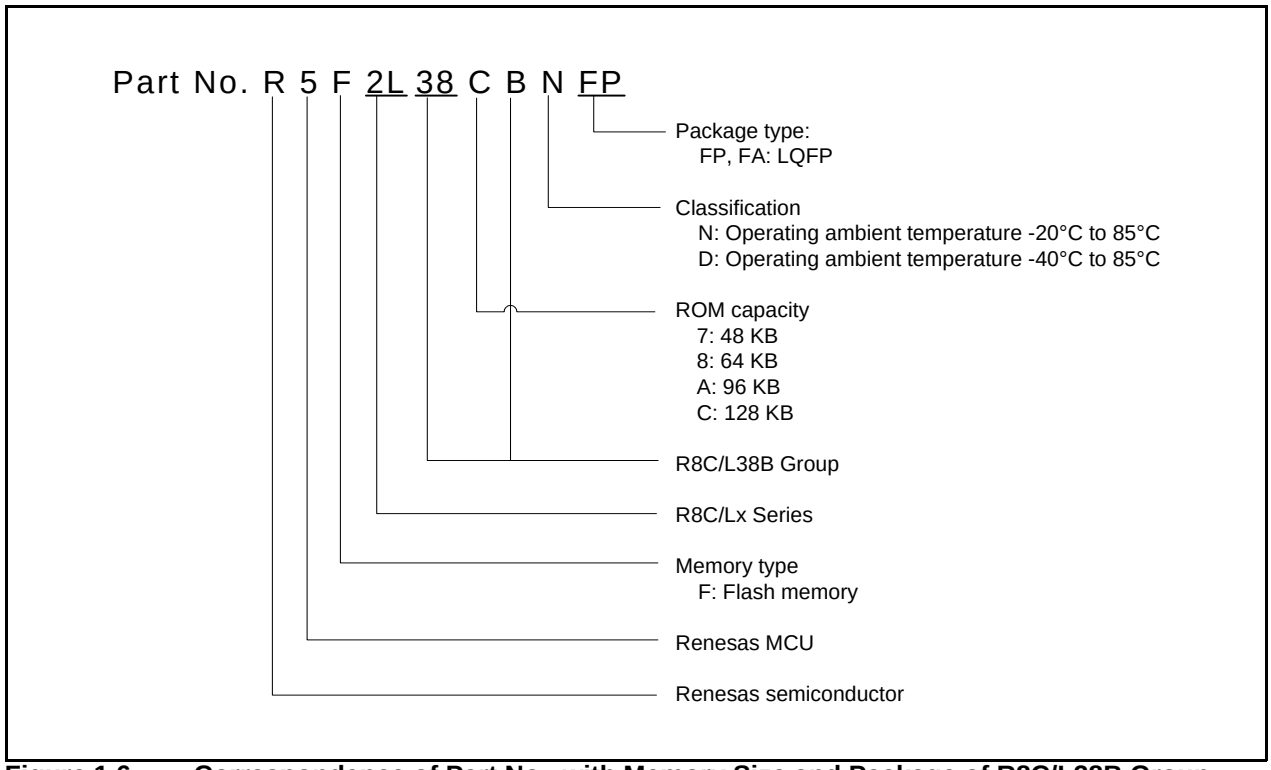


Figure 1.6 Correspondence of Part No., with Memory Size and Package of R8C/L38B Group

Table 1.13 Product List for R8C/L3AA Group **Current of Jul 2008**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2L3A7ANFP (D)	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0100KB-A	N Version
R5F2L3A7ANFA (D)	48 Kbytes	1 Kbyte × 4	6 Kbytes	PRQP0100JD-B	
R5F2L3A8ANFP (D)	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0100KB-A	
R5F2L3A8ANFA (D)	64 Kbytes	1 Kbyte × 4	8 Kbytes	PRQP0100JD-B	
R5F2L3AAANFP (D)	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0100KB-A	
R5F2L3AAANFA (D)	96 Kbytes	1 Kbyte × 4	10 Kbytes	PRQP0100JD-B	
R5F2L3ACANFP (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0100KB-A	
R5F2L3ACANFA (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PRQP0100JD-B	
R5F2L3A7ADFP (D)	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0100KB-A	D Version
R5F2L3A7ADFA (D)	48 Kbytes	1 Kbyte × 4	6 Kbytes	PRQP0100JD-B	
R5F2L3A8ADFP (D)	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0100KB-A	
R5F2L3A8ADFA (D)	64 Kbytes	1 Kbyte × 4	8 Kbytes	PRQP0100JD-B	
R5F2L3AAADFP (D)	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0100KB-A	
R5F2L3AAADFA (D)	96 Kbytes	1 Kbyte × 4	10 Kbytes	PRQP0100JD-B	
R5F2L3ACADFP (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0100KB-A	
R5F2L3ACADFA (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PRQP0100JD-B	

(D): Under development

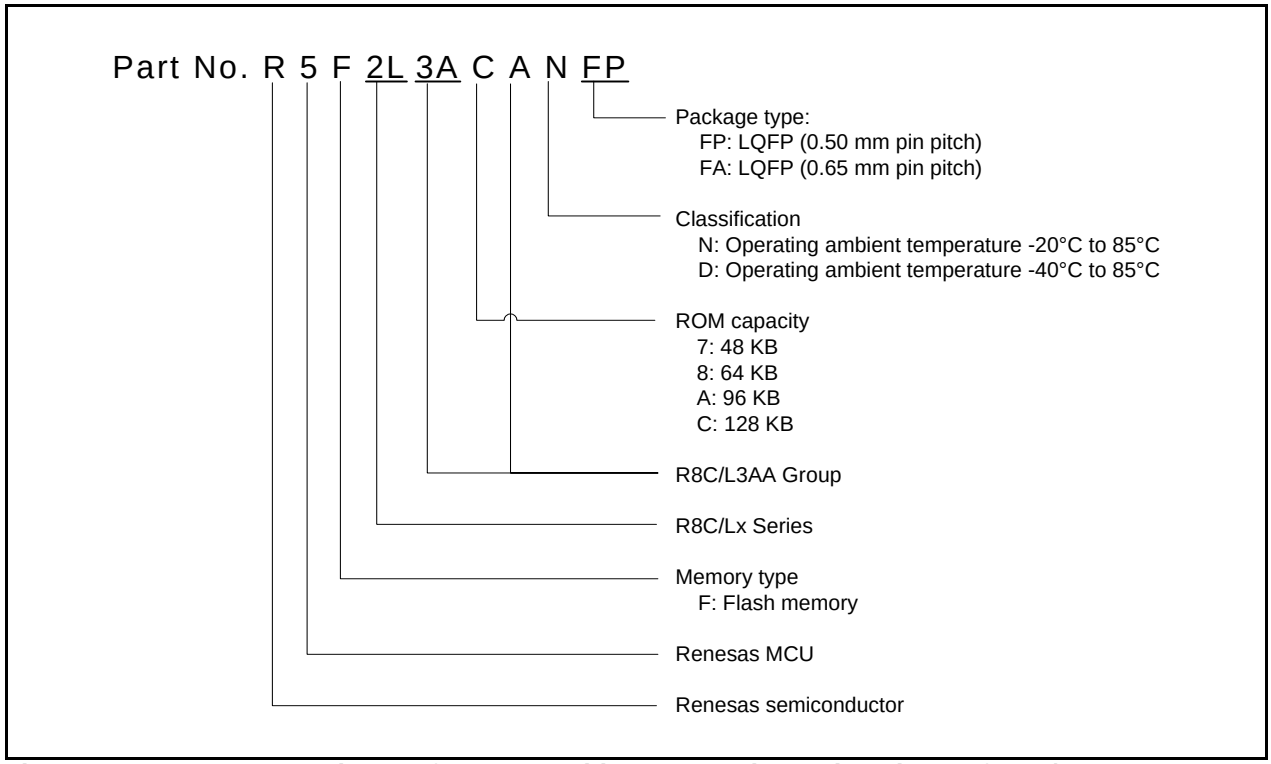


Figure 1.7 Correspondence of Part No., with Memory Size and Package of R8C/L3AA Group

Table 1.14 Product List for R8C/L3AB Group **Current of Jul 2008**

Part No.	Internal ROM Capacity	Internal RAM Capacity	Package Type	Remarks
R5F2L3A7BNFP (D)	48 Kbytes	6 Kbytes	PLQP0100KB-A	N Version
R5F2L3A7BNFA (D)	48 Kbytes	6 Kbytes	PRQP0100JD-B	
R5F2L3A8BNFP (D)	64 Kbytes	8 Kbytes	PLQP0100KB-A	
R5F2L3A8BNFA (D)	64 Kbytes	8 Kbytes	PRQP0100JD-B	
R5F2L3AABNFP (D)	96 Kbytes	10 Kbytes	PLQP0100KB-A	
R5F2L3AABNFA (D)	96 Kbytes	10 Kbytes	PRQP0100JD-B	
R5F2L3ACBNFP (D)	128 Kbytes	10 Kbytes	PLQP0100KB-A	
R5F2L3ACBNFA (D)	128 Kbytes	10 Kbytes	PRQP0100JD-B	
R5F2L3A7BDFP (D)	48 Kbytes	6 Kbytes	PLQP0100KB-A	D Version
R5F2L3A7BDFA (D)	48 Kbytes	6 Kbytes	PRQP0100JD-B	
R5F2L3A8BDFP (D)	64 Kbytes	8 Kbytes	PLQP0100KB-A	
R5F2L3A8BDFA (D)	64 Kbytes	8 Kbytes	PRQP0100JD-B	
R5F2L3AABDFP (D)	96 Kbytes	10 Kbytes	PLQP0100KB-A	
R5F2L3AABDFA (D)	96 Kbytes	10 Kbytes	PRQP0100JD-B	
R5F2L3ACBDFP (D)	128 Kbytes	10 Kbytes	PLQP0100KB-A	
R5F2L3ACBDFA (D)	128 Kbytes	10 Kbytes	PRQP0100JD-B	

(D): Under development

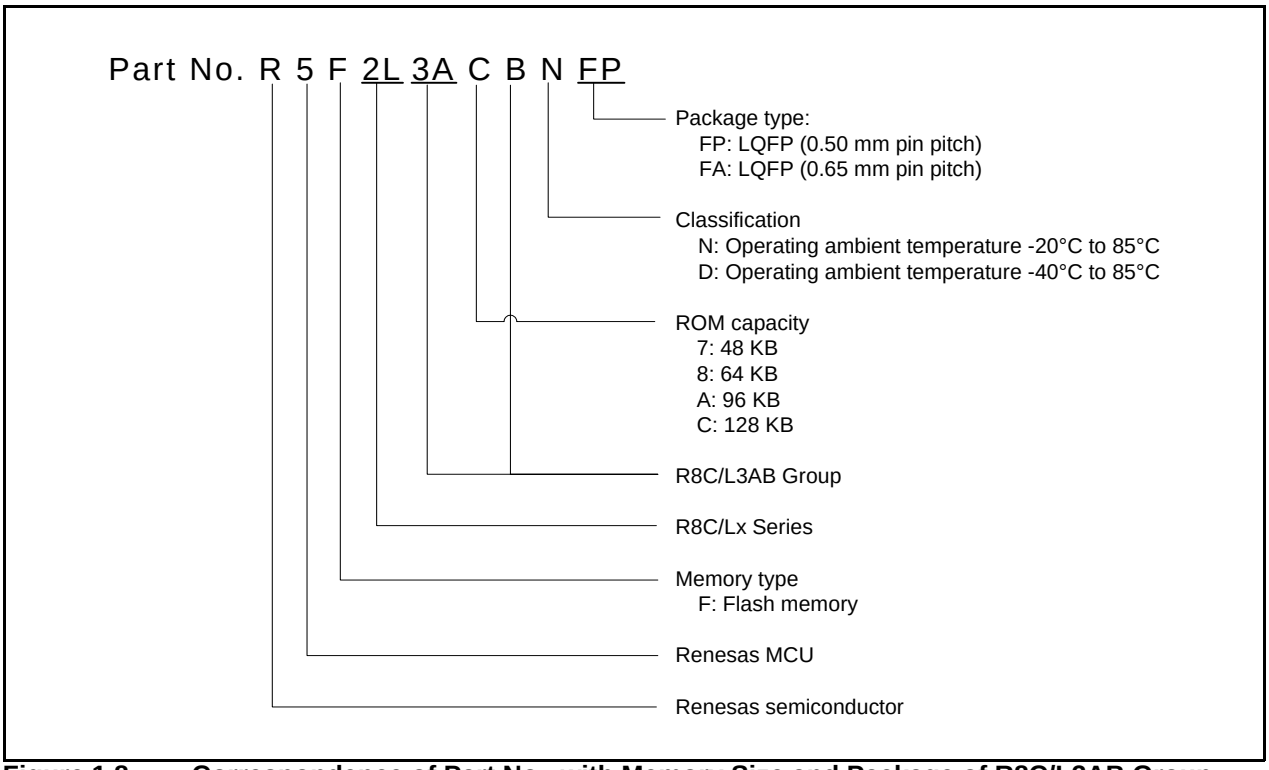
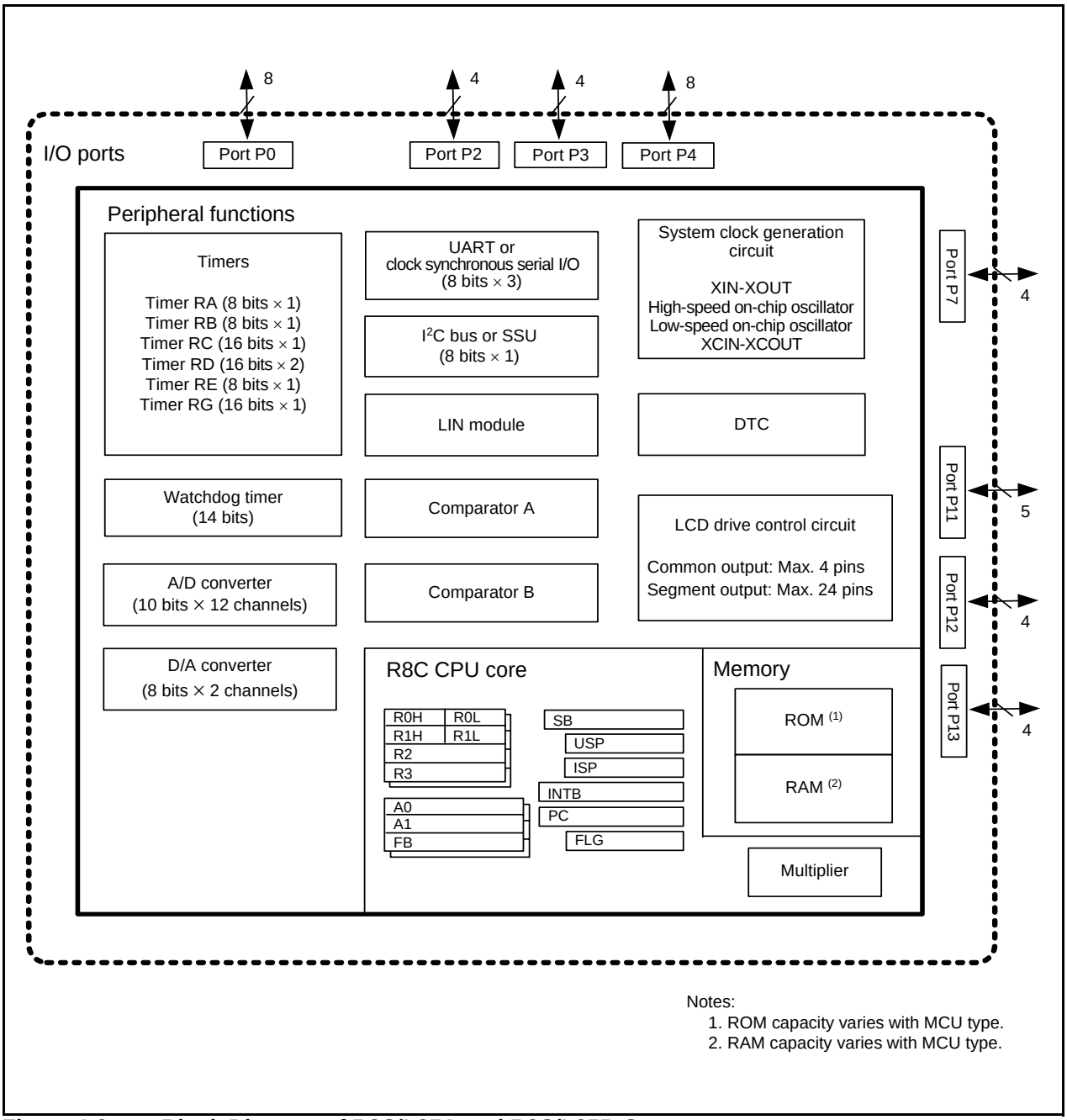


Figure 1.8 Correspondence of Part No., with Memory Size and Package of R8C/L3AB Group

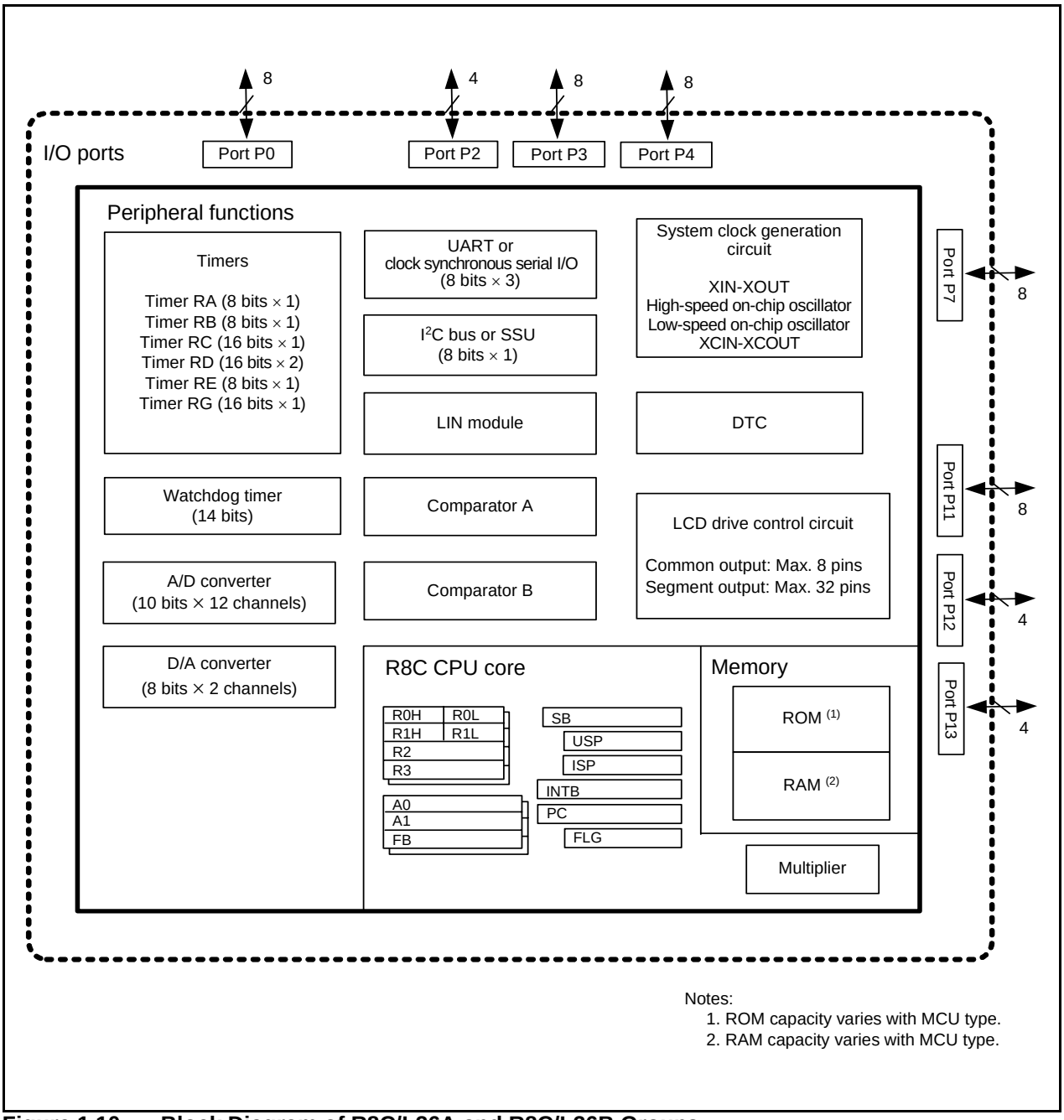
1.3 Block Diagrams

Figure 1.9 shows a Block Diagram of R8C/L35A and R8C/L35B Groups. Figure 1.10 shows a Block Diagram of R8C/L36A and R8C/L36B Groups. Figure 1.11 shows a Block Diagram of R8C/L38A and R8C/L38B Groups. Figure 1.12 shows a Block Diagram of R8C/L3AA and R8C/L3AB Groups.



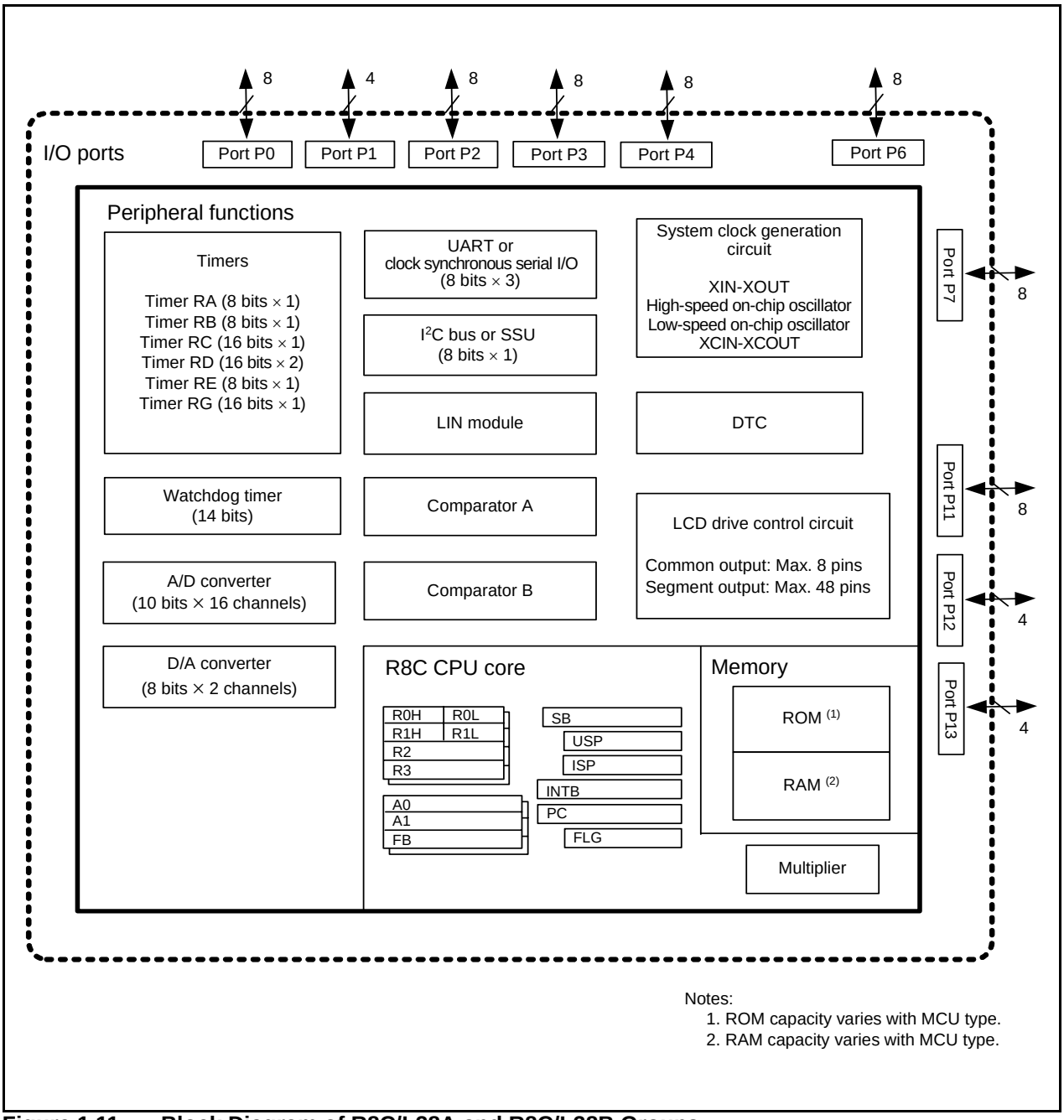
Notes:
1. ROM capacity varies with MCU type.
2. RAM capacity varies with MCU type.

Figure 1.9 Block Diagram of R8C/L35A and R8C/L35B Groups



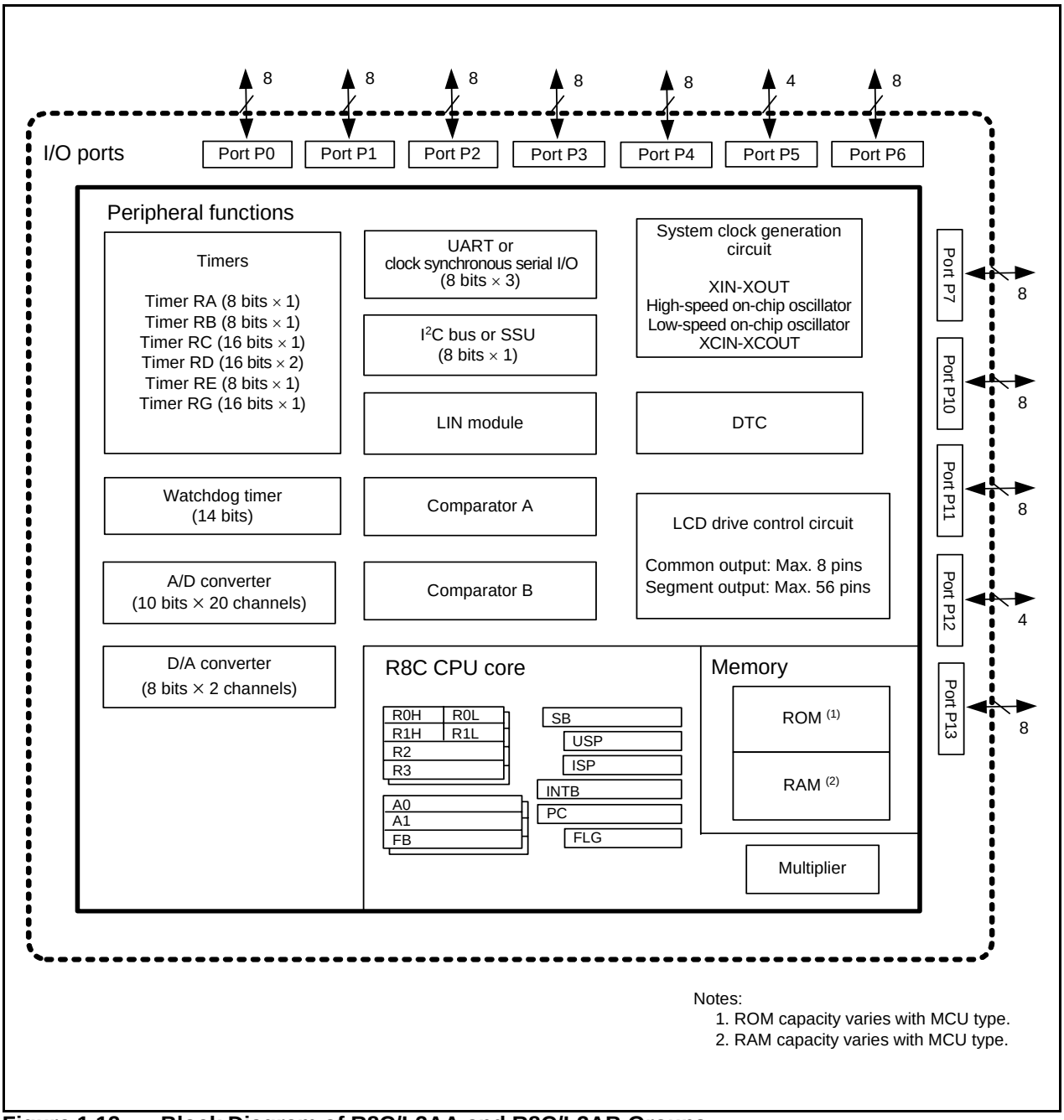
Notes:
1. ROM capacity varies with MCU type.
2. RAM capacity varies with MCU type.

Figure 1.10 Block Diagram of R8C/L36A and R8C/L36B Groups



Notes:
1. ROM capacity varies with MCU type.
2. RAM capacity varies with MCU type.

Figure 1.11 Block Diagram of R8C/L38A and R8C/L38B Groups

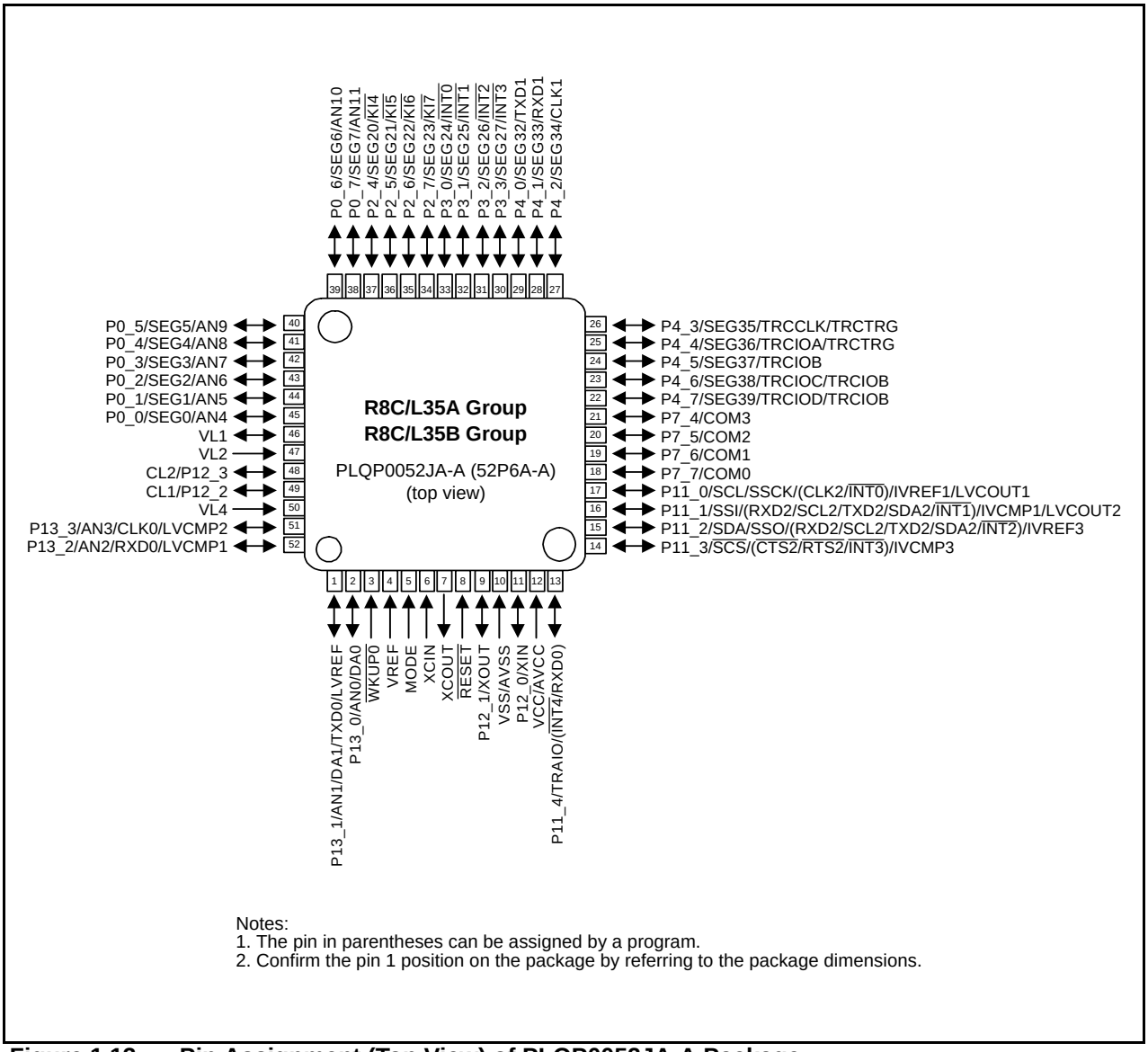


Notes:
1. ROM capacity varies with MCU type.
2. RAM capacity varies with MCU type.

Figure 1.12 Block Diagram of R8C/L3AA and R8C/L3AB Groups

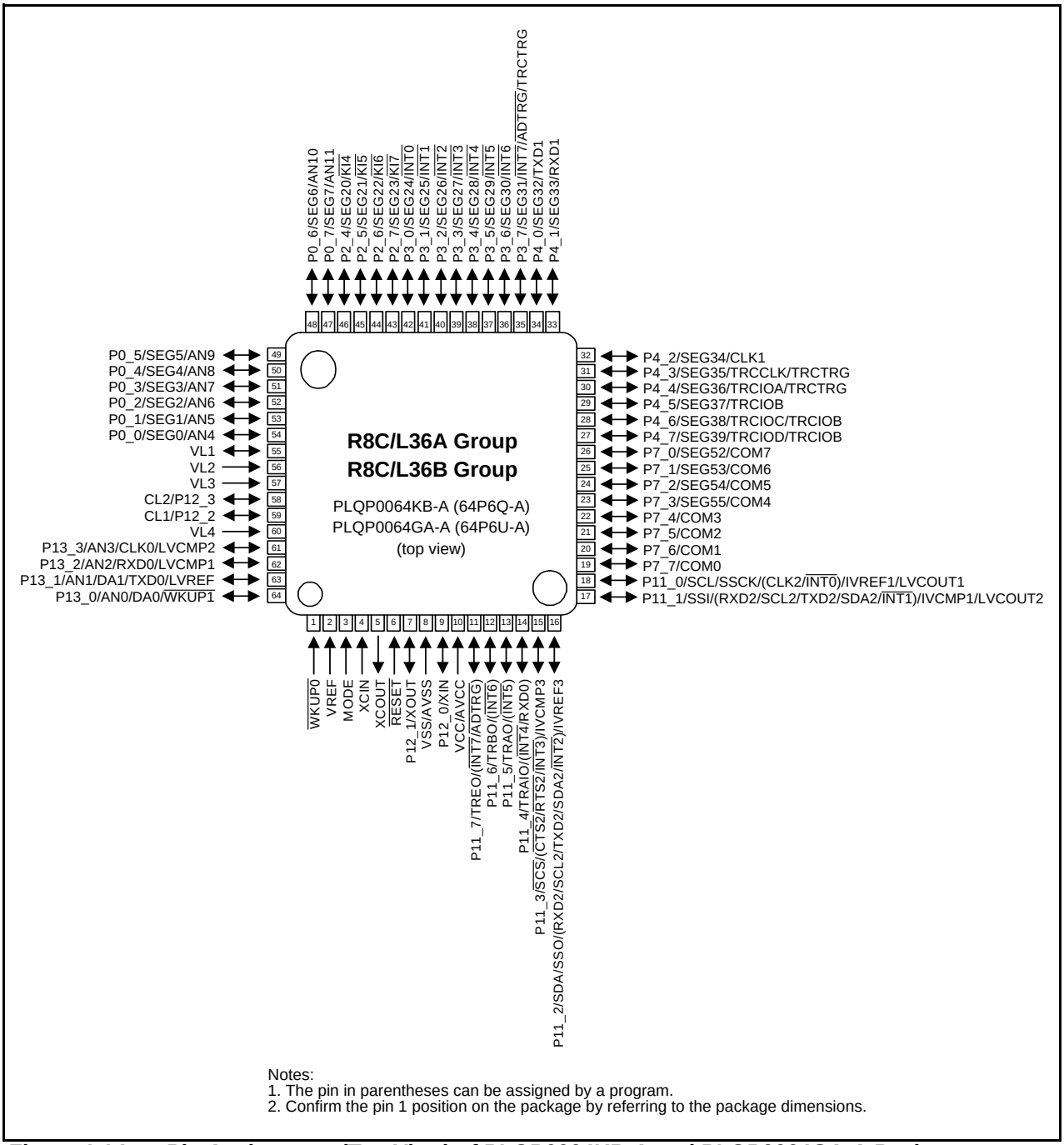
1.4 Pin Assignments

Figures 1.13 to 1.17 show pin assignments (top view). Tables 1.15 to 1.17 list the pin name information by pin number.



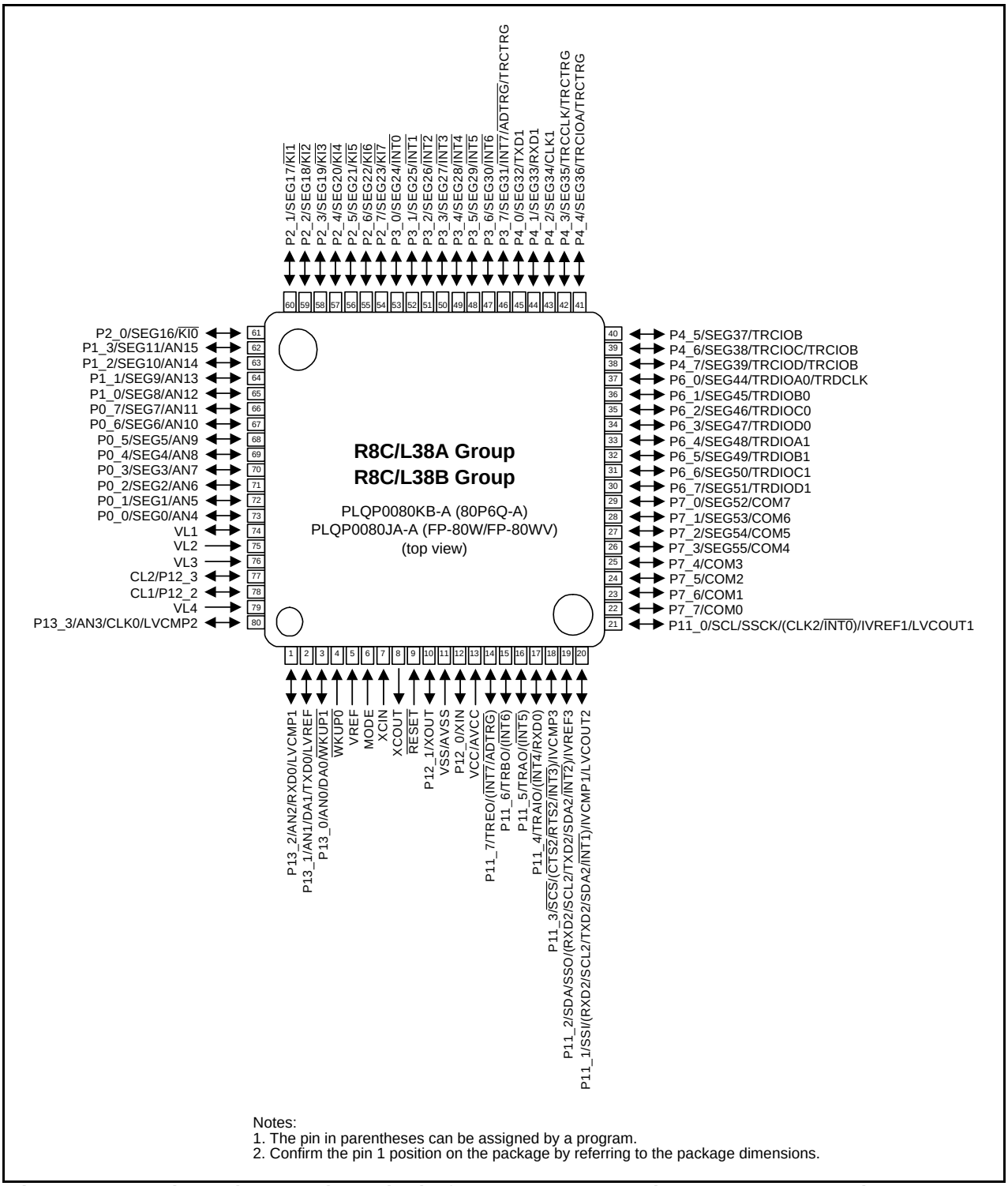
Notes:
1. The pin in parentheses can be assigned by a program.
2. Confirm the pin 1 position on the package by referring to the package dimensions.

Figure 1.13 Pin Assignment (Top View) of PLQP0052JA-A Package



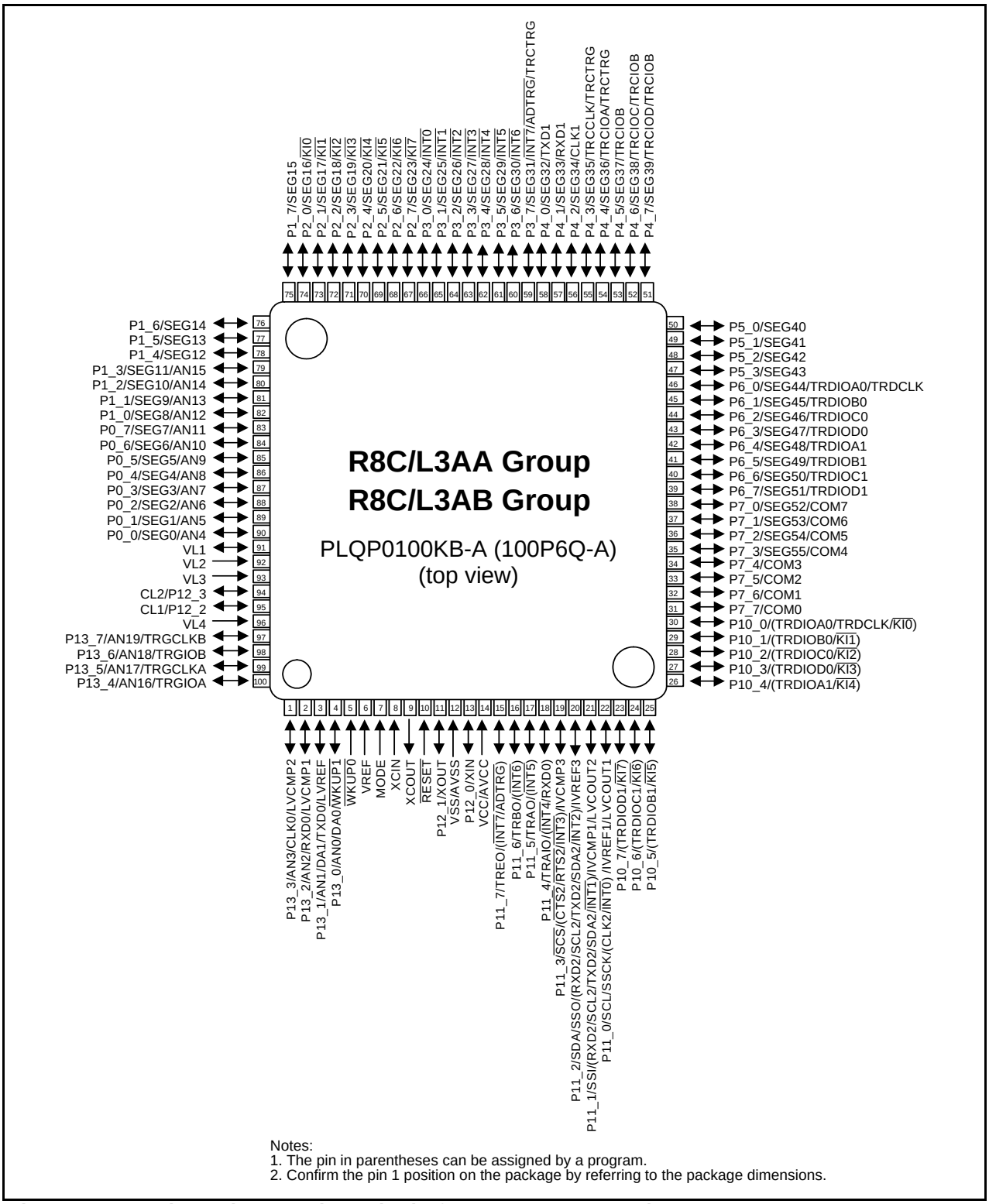
Notes:
1. The pin in parentheses can be assigned by a program.
2. Confirm the pin 1 position on the package by referring to the package dimensions.

Figure 1.14 Pin Assignment (Top View) of PLQP0064KB-A and PLQP0064GA-A Packages



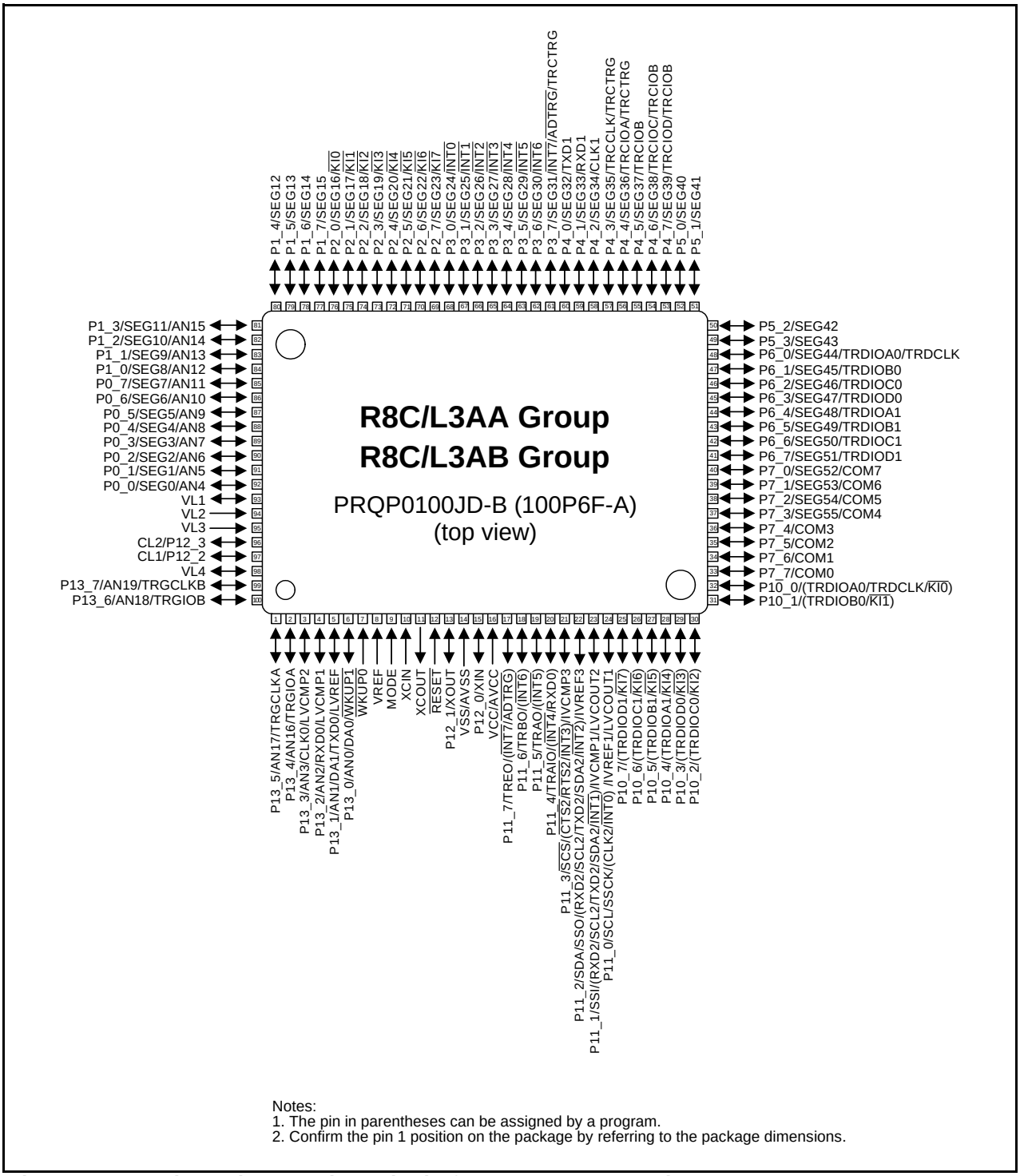
Notes:
1. The pin in parentheses can be assigned by a program.
2. Confirm the pin 1 position on the package by referring to the package dimensions.

Figure 1.15 Pin Assignment (Top View) of PLQP0080KB-A and PLQP0080JA-A Packages



Notes:
1. The pin in parentheses can be assigned by a program.
2. Confirm the pin 1 position on the package by referring to the package dimensions.

Figure 1.16 Pin Assignment (Top View) of PLQP0100KB-A Package



Notes:
1. The pin in parentheses can be assigned by a program.
2. Confirm the pin 1 position on the package by referring to the package dimensions.

Figure 1.17 Pin Assignment (Top View) of PRQP0100JD-B Package

Table 1.15 Pin Name Information by Pin Number (1)

Pin Number				Control Pin	Port	I/O Pin Functions for Peripheral Modules						
L3AA L3AB (Note 2)	L38A L38B	L36A L36B	L35A L35B			Interrupt	Timer	Serial Interface	SSU	I^2C bus	A/D Converter, D/A Converter, Comparators A, B, Voltage Detection Circuit	LCD drive control circuit
1 [3]	80	61	51		P13_3			CLK0			AN3/LVCMP2	
2 [4]	1	62	52		P13_2			RXD0			AN2/LVCMP1	
3 [5]	2	63	1		P13_1			TXD0			AN1/DA1/LVREF	
4 [6]	3	64	2	$\overline{\text{WKUP1}}$(3)	P13_0						AN0/DA0	
5 [7]	4	1	3	$\overline{\text{WKUP0}}$								
6 [8]	5	2	4	VREF								
7 [9]	6	3	5	MODE								
8 [10]	7	4	6	XCIN								
9 [11]	8	5	7	XCOUT								
10 [12]	9	6	8	$\overline{\text{RESET}}$								
11 [13]	10	7	9	XOUT	P12_1							
12 [14]	11	8	10	VSS/ AVSS								
13 [15]	12	9	11	XIN	P12_0							
14 [16]	13	10	12	VCC/ AVCC								
15 [17]	14	11			P11_7	($\overline{\text{INT7}}$)	TREO				($\overline{\text{ADTRG}}$)	
16 [18]	15	12			P11_6	($\overline{\text{INT6}}$)	TRBO					
17 [19]	16	13			P11_5	($\overline{\text{INT5}}$)	TRAO					
18 [20]	17	14	13		P11_4	($\overline{\text{INT4}}$)	TRAIO	(RXD0)				
19 [21]	18	15	14		P11_3	($\overline{\text{INT3}}$)		($\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$)	$\overline{\text{SCS}}$		IVCMP3	
20 [22]	19	16	15		P11_2	($\overline{\text{INT2}}$)		(RXD2/SCL2/ TXD2/SDA2)	SSO	SDA	IVREF3	
21 [23]	20	17	16		P11_1	($\overline{\text{INT1}}$)		(RXD2/SCL2/ TXD2/SDA2)	SSI		IVCMP1/LVCOUT2	
22 [24]	21	18	17		P11_0	($\overline{\text{INT0}}$)		(CLK2)	SSCK	SCL	IVREF1/LVCOUT1	
23 [25]					P10_7	($\overline{\text{KI7}}$)	(TRDIOD1)					
24 [26]					P10_6	($\overline{\text{KI6}}$)	(TRDIOC1)					
25 [27]					P10_5	($\overline{\text{KI5}}$)	(TRDIOB1)					
26 [28]					P10_4	($\overline{\text{KI4}}$)	(TRDIOA1)					
27 [29]					P10_3	($\overline{\text{KI3}}$)	(TRDIOD0)					
28 [30]					P10_2	($\overline{\text{KI2}}$)	(TRDIOC0)					
29 [31]					P10_1	($\overline{\text{KI1}}$)	(TRDIOB0)					
30 [32]					P10_0	($\overline{\text{KI0}}$)	(TRDIOA0/ TRDCLK)					
31 [33]	22	19	18		P7_7							COM0
32 [34]	23	20	19		P7_6							COM1
33 [35]	24	21	20		P7_5							COM2
34 [36]	25	22	21		P7_4							COM3
35 [37]	26	23			P7_3							SEG55/ COM4
36 [38]	27	24			P7_2							SEG54/ COM5
37 [39]	28	25			P7_1							SEG53/ COM6
38 [40]	29	26			P7_0							SEG52/ COM7
39 [41]	30				P6_7		TRDIOD1					SEG51

Notes:
1. The pin in parentheses can be assigned by a program.
2. The number in brackets indicates the pin number for the 100P6F package.
3. 0000The $\overline{\text{WKUP1}}$ pin is not available in the R8C/L35A and R8C/L35B Groups.

Table 1.16 Pin Name Information by Pin Number (2)

Pin Number				Control Pin	Port	I/O Pin Functions for Peripheral Modules						
L3AA L3AB (Note 2)	L38A L38B	L36A L36B	L35A L35B			Interrupt	Timer	Serial Interface	SSU	I^2C bus	A/D Converter, D/A Converter, Comparators A, B, Voltage Detection Circuit	LCD drive control circuit
40 [42]	31				P6_6		TRDIOC1					SEG50
41 [43]	32				P6_5		TRDIOB1					SEG49
42 [44]	33				P6_4		TRDIOA1					SEG48
43 [45]	34				P6_3		TRDIOD0					SEG47
44 [46]	35				P6_2		TRDIOC0					SEG46
45 [47]	36				P6_1		TRDIOB0					SEG45
46 [48]	37				P6_0		TRDIOA0/ TRDCLK					SEG44
47 [49]					P5_3							SEG43
48 [50]					P5_2							SEG42
49 [51]					P5_1							SEG41
50 [52]					P5_0							SEG40
51 [53]	38	27	22		P4_7		TRCIOD/ TRCIOB					SEG39
52 [54]	39	28	23		P4_6		TRCIOC/ TRCIOB					SEG38
53 [55]	40	29	24		P4_5		TRCIOB					SEG37
54 [56]	41	30	25		P4_4		TRCIOA/ TRCTRG					SEG36
55 [57]	42	31	26		P4_3		TRCCLK/ TRCTRG					SEG35
56 [58]	43	32	27		P4_2			CLK1				SEG34
57 [59]	44	33	28		P4_1			RXD1				SEG33
58 [60]	45	34	29		P4_0			TXD1				SEG32
59 [61]	46	35			P3_7	$\overline{INT7}$	TRCTRG				$\overline{ADTRG}$	SEG31
60 [62]	47	36			P3_6	$\overline{INT6}$						SEG30
61 [63]	48	37			P3_5	$\overline{INT5}$						SEG29
62 [64]	49	38			P3_4	$\overline{INT4}$						SEG28
63 [65]	50	39	30		P3_3	$\overline{INT3}$						SEG27
64 [66]	51	40	31		P3_2	$\overline{INT2}$						SEG26
65 [67]	52	41	32		P3_1	$\overline{INT1}$						SEG25
66 [68]	53	42	33		P3_0	$\overline{INT0}$						SEG24
67 [69]	54	43	34		P2_7	$\overline{KI7}$						SEG23
68 [70]	55	44	35		P2_6	$\overline{KI6}$						SEG22
69 [71]	56	45	36		P2_5	$\overline{KI5}$						SEG21
70 [72]	57	46	37		P2_4	$\overline{KI4}$						SEG20
71 [73]	58				P2_3	$\overline{KI3}$						SEG19
72 [74]	59				P2_2	$\overline{KI2}$						SEG18
73 [75]	60				P2_1	$\overline{KI1}$						SEG17
74 [76]	61				P2_0	$\overline{KI0}$						SEG16
75 [77]					P1_7							SEG15
76 [78]					P1_6							SEG14
77 [79]					P1_5							SEG13
78 [80]					P1_4							SEG12
79 [81]	62				P1_3						AN15	SEG11
80 [82]	63				P1_2						AN14	SEG10
81 [83]	64				P1_1						AN13	SEG9
82 [84]	65				P1_0						AN12	SEG8
83 [85]	66	47	38		P0_7						AN11	SEG7
84 [86]	67	48	39		P0_6						AN10	SEG6
85 [87]	68	49	40		P0_5						AN9	SEG5

Notes:
1. The pin in parentheses can be assigned by a program.
2. The number in brackets indicates the pin number for the 100P6F package.

Table 1.17 Pin Name Information by Pin Number (3)

Pin Number				Control Pin	Port	I/O Pin Functions for Peripheral Modules						
L3AA L3AB (Note 2)	L38A L38B	L36A L36B	L35A L35B			Interrupt	Timer	Serial Interface	SSU	I^2C bus	A/D Converter, D/A Converter, Comparators A, B, Voltage Detection Circuit	LCD drive control circuit
86 [88]	69	50	41		P0_4						AN8	SEG4
87 [89]	70	51	42		P0_3						AN7	SEG3
88 [90]	71	52	43		P0_2						AN6	SEG2
89 [91]	72	53	44		P0_1						AN5	SEG1
90 [92]	73	54	45		P0_0						AN4	SEG0
91 [93]	74	55	46									VL1
92 [94]	75	56	47									VL2
93 [95]	76	57										VL3
94 [96]	77	58	48		P12_3							CL2
95 [97]	78	59	49		P12_2							CL1
96 [98]	79	60	50									VL4
97 [99]					P13_7		TRGCLKB				AN19	
98 [100]					P13_6		TRGIOB				AN18	
99 [1]					P13_5		TRGCLKA				AN17	
100 [2]					P13_4		TRGIOA				AN16	

Notes:
1. The pin in parentheses can be assigned by a program.
2. The number in brackets indicates the pin number for the 100P6F package.

1.5 Pin Functions

Tables 1.18 and 1.19 list pin functions.

Table 1.18 Pin Functions (1)

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS	–	Apply 1.8 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	–	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Driving this pin low resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
Power-off mode exit input	$\overline{\text{WKUP0}}$	I	This pin is provided for input to exit the mode used in power-off mode. Connect to VSS when not using power-off mode.
	$\overline{\text{WKUP1}}$	I	This pin is provided for input to exit the mode used in power-off mode.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic oscillator or a crystal oscillator between pins XIN and XOUT. (1) To use an external clock, input it to the XIN pin and leave the XOUT pin open.
XIN clock output	XOUT	O	
XCIN clock input	XCIN	I	These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between pins XCIN and XCOUT. (1) To use an external clock, input it to the XCIN pin and leave the XCOUT pin open.
XCIN clock output	XCOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT7}}$	I	$\overline{\text{INT}}$ interrupt input pins.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI7}}$	I	Key input interrupt input pins
Timer RA	TRAIO	I/O	Timer RA I/O pin
	TRAO	O	Timer RA output pin
Timer RB	TRBO	O	Timer RB output pin
Timer RC	TRCCLK	I	External clock input pin
	TRCTRG	I	External trigger input pin
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins
Timer RD	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1	I/O	Timer RD I/O pins
	TRDCLK	I	External clock input pin
Timer RE	TREO	O	Divided clock output pin
Timer RG	TRGCLKA, TRGCLKB	I	Timer RG input pins
	TRGIOA, TRGIOB	I/O	Timer RG I/O pins
Serial interface	CLK0, CLK1, CLK2	I/O	Transfer clock I/O pins
	RXD0, RXD1, RXD2	I	Serial data input pins
	TXD0, TXD1, TXD2	O	Serial data output pins
	$\overline{\text{CTS2}}$	I	Transmission control input pin
	$\overline{\text{RTS2}}$	O	Reception control output pin
	SCL2	I/O	I^2C mode clock I/O pin
	SDA2	I/O	I^2C mode data I/O pin

I: Input O: Output I/O: Input and output

Note:

1. Contact the oscillator manufacturer for oscillation characteristics.

Table 1.19 Pin Functions (2)

Item	Pin Name	I/O Type	Description
I^2C bus	SCL	I/O	Clock I/O pin
	SDA	I/O	Data I/O pin
SSU	SSI	I/O	Data I/O pin
	$\overline{SCS}$	I/O	Chip-select signal I/O pin
	SSCK	I/O	Clock I/O pin
	SSO	I/O	Data I/O pin
Reference voltage input	VREF	I	Reference voltage input pin for the A/D converter and the D/A converter
A/D converter	AN0 to AN11	I	A/D converter analog input pins
	$\overline{ADTRG}$	I	AD external trigger input pin
D/A converter	DA0, DA1	O	D/A converter output pins
Comparator A	LVCMP1, LVCMP2	I	Comparator A analog voltage input pins
	LVREF	I	Comparator A reference voltage input pin
	LVCOUT1, LVCOUT2	O	Comparator A output pins
Comparator B	IVCMP1, IVCMP3	I	Comparator B analog voltage input pins
	IVREF1, IVREF3	I	Comparator B reference voltage input pins
Voltage detection circuit	LVCMP2	I	Detection target voltage input pin for voltage detection 2
I/O ports	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0, P5_3, P6_0 to P6_7 P7_0 to P7_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_3, P13_0 to P13_7	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. Ports P10_0 to P10_7 and P11_0 to P11_7 can be used as LED drive ports.
Segment output	SEG0 to SEG55	O	LCD segment output pins
Common output	COM0 to COM7	O	LCD common output pins
Voltage multiplier capacity connect pins	CL1, CL2	O	Connect pins for the LCD control voltage multiplier
LCD power supply	VL1	I/O	Apply the voltage: $0 \leq VL1 \leq VL2 \leq VL3 \leq VL4$. VL1 can be used as the reference potential input or output pin when setting the voltage multiplier.
	VL2 to VL4	I	

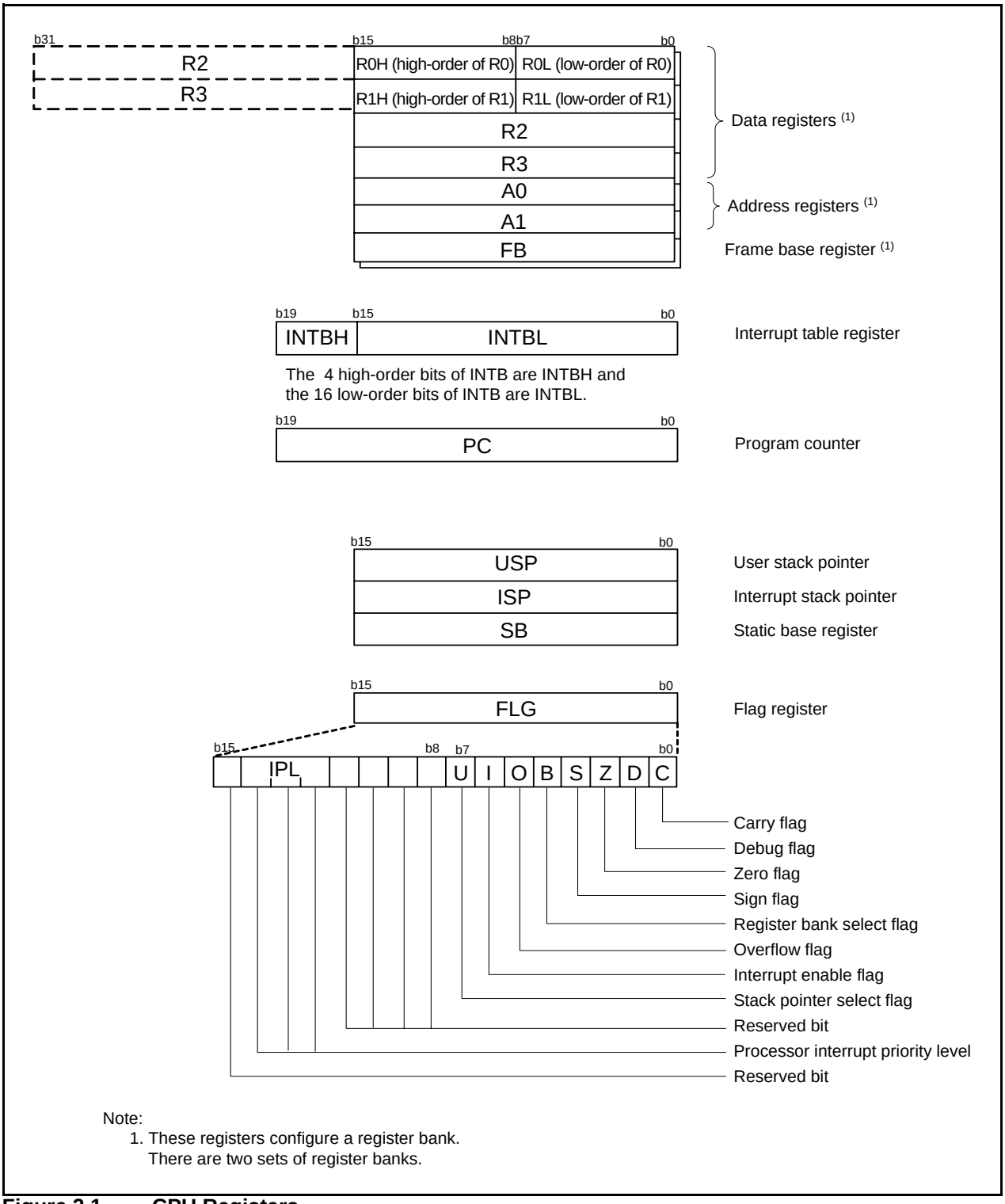
I: Input O: Output I/O: Input and output

Note:

1. Contact the oscillator manufacturer for oscillation characteristics.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register banks.



Note:
1. These registers configure a register bank.
There are two sets of register banks.

Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

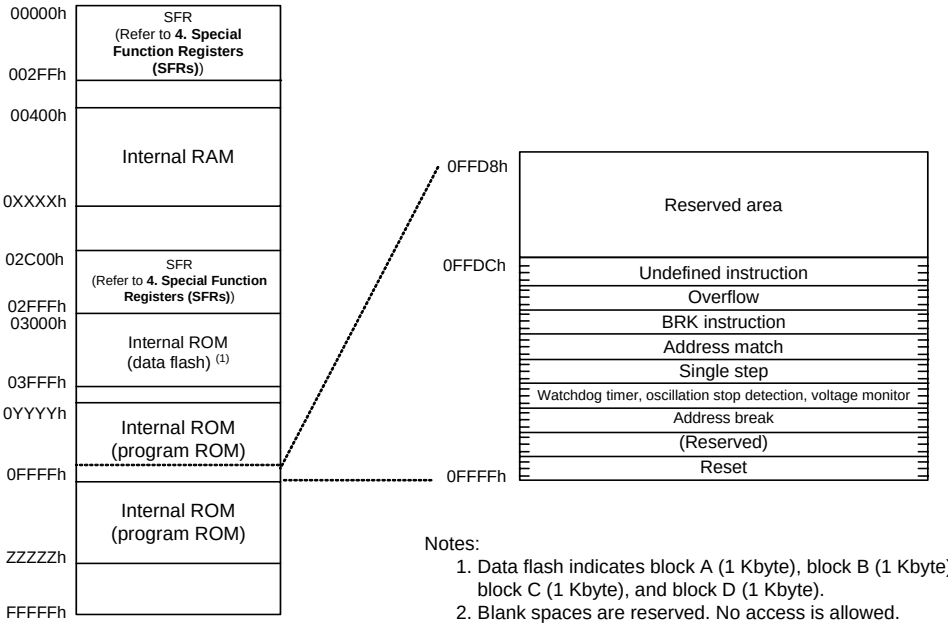
IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3. Memory

Figure 3.1 is a Memory Map of each group. Each group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM area is allocated addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



Notes:
1. Data flash indicates block A (1 Kbyte), block B (1 Kbyte), block C (1 Kbyte), and block D (1 Kbyte).
2. Blank spaces are reserved. No access is allowed.

Part Number	Internal ROM			Internal RAM		Data Flash
	Capacity	Address 0YYYYh	Address ZZZZZh	Capacity	Address 0XXXXh	
R5F2L357A***, R5F2L367A***, R5F2L387A***, R5F2L3A7A***	48 Kbytes	04000h	–	6 Kbytes	01BFFh	Available
R5F2L358A***, R5F2L368A***, R5F2L388A***, R5F2L3A8A***	64 Kbytes	04000h	13FFFh	8 Kbytes	023FFh	
R5F2L35AA***, R5F2L36AA***, R5F2L38AA***, R5F2L3AAA***	96 Kbytes	04000h	1BFFFh	10 Kbytes	02BFFh	
R5F2L35CA***, R5F2L36CA***, R5F2L38CA***, R5F2L3ACA***	128 Kbytes	04000h	23FFFh	10 Kbytes	02BFFh	
R5F2L357B***, R5F2L367B***, R5F2L387B***, R5F2L3A7B***	48 Kbytes	04000h	–	6 Kbytes	01BFFh	Not available
R5F2L358B***, R5F2L368B***, R5F2L388B***, R5F2L3A8B***	64 Kbytes	04000h	13FFFh	8 Kbytes	023FFh	
R5F2L35AB***, R5F2L36AB***, R5F2L38AB***, R5F2L3AAB***	96 Kbytes	04000h	1BFFFh	10 Kbytes	02BFFh	
R5F2L35CB***, R5F2L36CB***, R5F2L38CB***, R5F2L3ACB***	128 Kbytes	04000h	23FFFh	10 Kbytes	02BFFh	

Figure 3.1 Memory Map

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.16 list SFR information.

Table 4.1 SFR Information (1) (1)

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	00100000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h	Module Standby Control Register	MSTCR	00h
0009h	System Clock Control Register 3	CM3	00h
000Ah	Protect Register	PRCR	00h
000Bh	Reset Source Determination Register	RSTFR	XXXX00XXb (2)
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDTC	00111111b
0010h			
0011h			
0012h			
0013h			
0014h			
0015h	High-Speed On-Chip Oscillator Control Register 7	FRA7	When shipping
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b (3)
001Dh			
001Eh			
001Fh			
0020h	Power-Off Mode Control Register 0	POMCR0	X0000000b
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h	On-Chip Reference Voltage Control Register	OCVREFCR	00h
0027h			
0028h			
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	When Shipping
002Ah	High-Speed On-Chip Oscillator Control Register 5	FRA5	When Shipping
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When Shipping
002Ch			
002Dh			
002Eh			
002Fh	High-Speed On-Chip Oscillator Control Register 3	FRA3	When shipping
0030h	Voltage Monitor Circuit/Comparator A Control Register	CMPA	00h
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
0032h			
0033h	Voltage Detect Register 1	VCA1	00001000b
0034h	Voltage Detect Register 2	VCA2	00h (4) 00100000b (5)
0035h			
0036h	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0037h			
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	1100X010b (4) 1100X011b (5)
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	10001010b

X: Undefined
Notes:
1. Blank spaces are reserved. No access is allowed.
2. The CWR bit in the RSTFR register is set to 0 after power-on, voltage monitor 0 reset, or exit from power-off mode. Software reset, watchdog timer reset, or oscillation stop detection reset does not affect this bit.
3. The CSPROINI bit in the OFS register is set to 0.
4. The LVDAS bit in the OFS register is set to 1.
5. The LVDAS bit in the OFS register is set to 0.

Table 4.2 SFR Information (2) (1)

Address	Register	Symbol	After Reset
003Ah	Voltage Monitor 2 Circuit Control Register	VW2C	10000010b
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0042h			
0043h	INT7 Interrupt Control Register	INT7IC	XX00X000b
0044h	INT6 Interrupt Control Register	INT6IC	XX00X000b
0045h	INT5 Interrupt Control Register	INT5IC	XX00X000b
0046h	INT4 Interrupt Control Register	INT4IC	XX00X000b
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h	Timer RD0 Interrupt Control Register	TRD0IC	XXXXX000b
0049h	Timer RD1 Interrupt Control Register	TRD1IC	XXXXX000b
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
004Ch	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU Interrupt Control Register / IIC bus Interrupt Control Register (2)	SSUIC/IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h	INT2 Interrupt Control Register	INT2IC	XX00X000b
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh	UART2 Bus Collision Detection Interrupt Control Register	U2BCNIC	XXXXX000b
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh	Timer RG Interrupt Control Register	TRGIC	XXXXX000b
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h	Voltage monitor 1 / Comparator A1 Interrupt Control Register	VCMP1IC	XXXXX000b
0073h	Voltage monitor 2 / Comparator A2 Interrupt Control Register	VCMP2IC	XXXXX000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

Notes:
1. Blank spaces are reserved. No access is allowed.
2. Selectable by the IICSEL bit in the SSUIICSR register.

Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	After Reset
0080h	DTC Activation Control Register	DTCTL	00h
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DTC Activation Enable Register 0	DTCEN0	00h
0089h	DTC Activation Enable Register 1	DTCEN1	00h
008Ah	DTC Activation Enable Register 2	DTCEN2	00h
008Bh	DTC Activation Enable Register 3	DTCEN3	00h
008Ch	DTC Activation Enable Register 4	DTCEN4	00h
008Dh	DTC Activation Enable Register 5	DTCEN5	00h
008Eh	DTC Activation Enable Register 6	DTCEN6	00h
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART2 Transmit/Receive Mode Register	U2MR	00h
00A9h	UART2 Bit Rate Register	U2BRG	XXh
00AAh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh			XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh	UART2 Special Mode Register 4	U2SMR4	00h
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BEh	UART2 Special Mode Register 2	U2SMR2	X0000000b
00BFh	UART2 Special Mode Register	U2SMR	X0000000b

X: Undefined
Note:
1. Blank spaces are reserved. No access is allowed.

Table 4.4 SFR Information (4) (1)

Address	Register	Symbol	After Reset
00C0h	A/D Register 0	AD0	XXh
00C1h			000000XXb
00C2h	A/D Register 1	AD1	XXh
00C3h			000000XXb
00C4h	A/D Register 2	AD2	XXh
00C5h			000000XXb
00C6h	A/D Register 3	AD3	XXh
00C7h			000000XXb
00C8h	A/D Register 4	AD4	XXh
00C9h			000000XXb
00CAh	A/D Register 5	AD5	XXh
00CBh			000000XXb
00CCh	A/D Register 6	AD6	XXh
00CDh			000000XXb
00CEh	A/D Register 7	AD7	XXh
00CFh			000000XXb
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Mode Register	ADMOD	00h
00D5h	A/D Input Select Register	ADINSEL	11000000b
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h	D/A 0 Register	DA0	00h
00D9h	D/A 1 Register	DA1	00h
00DAh			
00DBh			
00DCh	D/A Control Register	DACON	00h
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h	Port P5 Register	P5	XXh
00EAh	Port P4 Direction Register	PD4	00h
00EBh	Port P5 Direction Register	PD5	00h
00ECh	Port P6 Register	P6	XXh
00EDh	Port P7 Register	P7	XXh
00EEh	Port P6 Direction Register	PD6	00h
00EFh	Port P7 Direction Register	PD7	00h
00F0h			
00F1h			
00F2h			
00F3h			
00F4h	Port P10 Register	P10	XXh
00F5h	Port P11 Register	P11	XXh
00F6h	Port P10 Direction Register	PD10	00h
00F7h	Port P11 Direction Register	PD11	00h
00F8h	Port P12 Register	P12	XXh
00F9h	Port P13 Register	P13	XXh
00FAh	Port P12 Direction Register	PD12	00h
00FBh	Port P13 Direction Register	PD13	00h
00FCh			
00FDh			
00FEh			
00FFh			

X: Undefined
Note:
1. Blank spaces are reserved. No access is allowed.

Table 4.5 SFR Information (5) (1)

Address	Register	Symbol	After Reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h	LIN Control Register 2	LINCR2	00h
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Second Data Register / Timer RE Counter Data Register	TRESEC	XXh
0119h	Timer RE Minute Data Register / Timer RE Compare Data Register	TREMIN	XXh
011Ah	Timer RE Hour Data Register	TREHR	XXh
011Bh	Timer RE Day of Week Data Register	TREWK	XXh
011Ch	Timer RE Control Register 1	TRECR1	XXXXX0XXb
011Dh	Timer RE Control Register 2	TRECR2	XXh
011Eh	Timer RE Count Source Select Register	TRECSR	00001000b
011Fh			
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011000b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h	Timer RC Trigger Control Register	TRCADCR	00h
0134h			
0135h	Timer RD Control Expansion Register	TRDECR	00h
0136h	Timer RD Trigger Control Register	TRDADCR	00h
0137h	Timer RD Start Register	TRDSTR	11111100b
0138h	Timer RD Mode Register	TRDMR	00001110b
0139h	Timer RD PWM Mode Register	TRDPMR	10001000b
013Ah	Timer RD Function Control Register	TRDFCR	10000000b
013Bh	Timer RD Output Master Enable Register 1	TRDOER1	FFh
013Ch	Timer RD Output Master Enable Register 2	TRDOER2	01111111b
013Dh	Timer RD Output Control Register	TRDOCR	00h
013Eh	Timer RD Digital Filter Function Select Register 0	TRDDF0	00h
013Fh	Timer RD Digital Filter Function Select Register 1	TRDDF1	00h

X: Undefined
Note:
1. Blank spaces are reserved. No access is allowed.

Table 4.6 SFR Information (6) (1)

Address	Register	Symbol	After Reset
0140h	Timer RD Control Register 0	TRDCR0	00h
0141h	Timer RD I/O Control Register A0	TRDIORA0	10001000b
0142h	Timer RD I/O Control Register C0	TRDIORC0	10001000b
0143h	Timer RD Status Register 0	TRDSR0	11100000b
0144h	Timer RD Interrupt Enable Register 0	TRDIER0	11100000b
0145h	Timer RD PWM Mode Output Level Control Register 0	TRDPOCR0	11111000b
0146h	Timer RD Counter 0	TRD0	00h
0147h			00h
0148h	Timer RD General Register A0	TRDGRA0	FFh
0149h			FFh
014Ah	Timer RD General Register B0	TRDGRB0	FFh
014Bh			FFh
014Ch	Timer RD General Register C0	TRDGRC0	FFh
014Dh			FFh
014Eh	Timer RD General Register D0	TRDGRD0	FFh
014Fh			FFh
0150h	Timer RD Control Register 1	TRDCR1	00h
0151h	Timer RD I/O Control Register A1	TRDIORA1	10001000b
0152h	Timer RD I/O Control Register C1	TRDIORC1	10001000b
0153h	Timer RD Status Register 1	TRDSR1	11000000b
0154h	Timer RD Interrupt Enable Register 1	TRDIER1	11100000b
0155h	Timer RD PWM Mode Output Level Control Register 1	TRDPOCR1	11111000b
0156h	Timer RD Counter 1	TRD1	00h
0157h			00h
0158h	Timer RD General Register A1	TRDGRA1	FFh
0159h			FFh
015Ah	Timer RD General Register B1	TRDGRB1	FFh
015Bh			FFh
015Ch	Timer RD General Register C1	TRDGRC1	FFh
015Dh			FFh
015Eh	Timer RD General Register D1	TRDGRD1	FFh
015Fh			FFh
0160h	UART1 Transmit/Receive Mode Register	U1MR	00h
0161h	UART1 Bit Rate Register	U1BRG	XXh
0162h	UART1 Transmit Buffer Register	U1TB	XXh
0163h			XXh
0164h	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
0165h	UART1 Transmit/Receive Control Register 1	U1C1	00000010b
0166h	UART1 Receive Buffer Register	U1RB	XXh
0167h			XXh
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h	Timer RG Mode Register	TRGMR	01000000b
0171h	Timer RG Count Control Register	TRGCNTC	00h
0172h	Timer RG Control Register	TRGCR	10000000b
0173h	Timer RG Interrupt Enable Register	TRGIER	11110000b
0174h	Timer RG Status Register	TRGSR	11100000b
0175h	Timer RG I/O Control Register	TRGIOR	00h
0176h	Timer RG Counter	TRG	00h
0177h			00h
0178h	Timer RG General Register A	TRGGRA	FFh
0179h			FFh
017Ah	Timer RG General Register B	TRGGRB	FFh
017Bh			FFh
017Ch	Timer RG General Register C	TRGGRC	FFh
017Dh			FFh
017Eh	Timer RG General Register D	TRGGRD	FFh
017Fh			FFh

X: Undefined
Note:
1. Blank spaces are reserved. No access is allowed.

Table 4.7 SFR Information (7) (1)

Address	Register	Symbol	After Reset
0180h	Timer RA Pin Select Register	TRASR	00h
0181h	Timer RB/RC Pin Select Register	TRBRCSR	00h
0182h	Timer RC Pin Select Register 0	TRCPSR0	00h
0183h	Timer RC Pin Select Register 1	TRCPSR1	00h
0184h	Timer RD Pin Select Register 0	TRDPSR0	00h
0185h	Timer RD Pin Select Register 1	TRDPSR1	00h
0186h			
0187h	Timer RG Pin Select Register	TRGPSR	00h
0188h	UART0 Pin Select Register	U0SR	00h
0189h	UART1 Pin Select Register	U1SR	00h
018Ah	UART2 Pin Select Register 0	U2SR0	00h
018Bh	UART2 Pin Select Register 1	U2SR1	00h
018Ch	SSU/IIC Pin Select Register	SSUIICSR	00h
018Dh	Key Input Pin Select Register	KISR	00h
018Eh	INT Interrupt Input Pin Select Register	INTSR	00h
018Fh			
0190h			
0191h			
0192h			
0193h	SS Bit Counter Register	SSBR	11111000b
0194h	SS Transmit Data Register L / IIC bus Transmit Data Register (2)	SSTDR/ICDRT	FFh
0195h	SS Transmit Data Register H	SSTDRH	FFh
0196h	SS Receive Data Register L / IIC bus Receive Data Register (2)	SSRDR/ICDRR	FFh
0197h	SS Receive Data Register H (2)	SSRDRH	FFh
0198h	SS Control Register H / IIC bus Control Register 1 (2)	SSCRH/ICCR1	00h
0199h	SS Control Register L / IIC bus Control Register 2 (2)	SSCRL/ICCR2	01111101b
019Ah	SS Mode Register / IIC bus Mode Register (2)	SSMR/ICMR	00010000b/00011000b
019Bh	SS Enable Register / IIC bus Interrupt Enable Register (2)	SSER/ICIER	00h
019Ch	SS Status Register / IIC bus Status Register (2)	SSSR/ICSR	00h/0000X000b
019Dh	SS Mode Register 2 / Slave Address Register (2)	SSMR2/SAR	00h
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	00h
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

X: Undefined
Notes:
1. Blank spaces are reserved. No access is allowed.
2. Selectable by the IICSEL bit in the SSUIICSR register.

Table 4.8 SFR Information (8) (1)

Address	Register	Symbol	After Reset
01C0h	Address Match Interrupt Register 0	RMAD0	XXh
01C1h			XXh
01C2h			0000XXXXb
01C3h	Address Match Interrupt Enable Register 0	AIER0	00h
01C4h	Address Match Interrupt Register 1	RMAD1	XXh
01C5h			XXh
01C6h			0000XXXXb
01C7h	Address Match Interrupt Enable Register 1	AIER1	00h
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	Port P0 Pull-Up Control Register	P0PUR	00h
01E1h	Port P1 Pull-Up Control Register	P1PUR	00h
01E2h	Port P2 Pull-Up Control Register	P2PUR	00h
01E3h	Port P3 Pull-Up Control Register	P3PUR	00h
01E4h	Port P4 Pull-Up Control Register	P4PUR	00h
01E5h	Port P5 Pull-Up Control Register	P5PUR	00h
01E6h	Port P6 Pull-Up Control Register	P6PUR	00h
01E7h	Port P7 Pull-Up Control Register	P7PUR	00h
01E8h			
01E9h			
01EAh	Port 10 Pull-Up Control Register	P10PUR	00h
01EBh	Port 11 Pull-Up Control Register	P11PUR	00h
01ECh	Port 12 Pull-Up Control Register	P12PUR	00h
01EDh	Port 13 Pull-Up Control Register	P13PUR	00h
01EEh			
01EFh			
01F0h	Port P10 Drive Capacity Control Register	P10DRR	00h
01F1h	Port P11 Drive Capacity Control Register	P11DRR	00h
01F2h			
01F3h			
01F4h			
01F5h	Input Threshold Control Register 0	VLT0	00h
01F6h	Input Threshold Control Register 1	VLT1	00h
01F7h	Input Threshold Control Register 2	VLT2	00h
01F8h	Comparator B Control Register 0	INTCMP	00h
01F9h			
01FAh	External Input Enable Register 0	INTEN	00h
01FBh	External Input Enable Register 1	INTEN1	00h
01FCh	INT Input Filter Select Register 0	INTF	00h
01FDh	INT Input Filter Select Register 1	INTF1	00h
01FEh	Key Input Enable Register 0	KIEN	00h
01FFh	Key Input Enable Register 1	KIEN1	00h

X: Undefined
Note:
1. Blank spaces are reserved. No access is allowed.

Table 4.9 SFR Information (9) (1)

Address	Register	Symbol	After Reset
0200h	LCD Control Register	LCR0	00h
0201h	LCD Bias Control Register	LCR1	00h
0202h	LCD Display Control Register	LCR2	00h
0203h	LCD Clock Control Register	LCR3	00h
0204h			
0205h			
0206h	LCD Port Select Register 0	LSE0	00h
0207h	LCD Port Select Register 1	LSE1	00h
0208h	LCD Port Select Register 2	LSE2	00h
0209h	LCD Port Select Register 3	LSE3	00h
020Ah	LCD Port Select Register 4	LSE4	00h
020Bh	LCD Port Select Register 5	LSE5	00h
020Ch	LCD Port Select Register 6	LSE6	00h
020Dh	LCD Port Select Register 7	LSE7	00h
020Eh			
020Fh			
0210h	LCD Display Data Register	LRA0L	XXh
0211h		LRA1L	XXh
0212h		LRA2L	XXh
0213h		LRA3L	XXh
0214h		LRA4L	XXh
0215h		LRA5L	XXh
0216h		LRA6L	XXh
0217h		LRA7L	XXh
0218h		LRA8L	XXh
0219h		LRA9L	XXh
021Ah		LRA10L	XXh
021Bh		LRA11L	XXh
021Ch		LRA12L	XXh
021Dh		LRA13L	XXh
021Eh		LRA14L	XXh
021Fh		LRA15L	XXh
0220h		LRA16L	XXh
0221h		LRA17L	XXh
0222h		LRA18L	XXh
0223h		LRA19L	XXh
0224h		LRA20L	XXh
0225h		LRA21L	XXh
0226h		LRA22L	XXh
0227h		LRA23L	XXh
0228h		LRA24L	XXh
0229h		LRA25L	XXh
022Ah		LRA26L	XXh
022Bh		LRA27L	XXh
022Ch		LRA28L	XXh
022Dh		LRA29L	XXh
022Eh		LRA30L	XXh
022Fh		LRA31L	XXh
0230h		LRA32L	XXh
0231h		LRA33L	XXh
0232h		LRA34L	XXh
0233h		LRA35L	XXh
0234h		LRA36L	XXh
0235h		LRA37L	XXh
0236h		LRA38L	XXh
0237h		LRA39L	XXh
0238h		LRA40L	XXh
0239h		LRA41L	XXh
023Ah		LRA42L	XXh
023Bh		LRA43L	XXh
023Ch		LRA44L	XXh
023Dh		LRA45L	XXh
023Eh		LRA46L	XXh
023Fh		LRA47L	XXh

X: Undefined
Note:
1. Blank spaces are reserved. No access is allowed.

Table 4.10 SFR Information (10) (1)

Address	Register	Symbol	After Reset
0240h	LCD Display Data Register	LRA48L	XXh
0241h		LRA49L	XXh
0242h		LRA50L	XXh
0243h		LRA51L	XXh
0244h		LRA52L	XXh
0245h		LRA53L	XXh
0246h		LRA54L	XXh
0247h		LRA55L	XXh
0248h		LRA56L	XXh
0249h		LRA57L	XXh
024Ah		LRA58L	XXh
024Bh		LRA59L	XXh
024Ch		LRA60L	XXh
024Dh		LRA61L	XXh
024Eh		LRA62L	XXh
024Fh		LRA63L	XXh
0250h		LRA64L	XXh
0251h		LRA65L	XXh
0252h		LRA66L	XXh
0253h		LRA67L	XXh
0254h		LRA68L	XXh
0255h		LRA69L	XXh
0256h		LRA70L	XXh
0257h		LRA71L	XXh
0258h		LRA72L	XXh
0259h		LRA73L	XXh
025Ah		LRA74L	XXh
025Bh		LRA75L	XXh
025Ch		LRA76L	XXh
025Dh		LRA77L	XXh
025Eh		LRA78L	XXh
025Fh		LRA79L	XXh
0260h		LRA80L	XXh
0261h		LRA81L	XXh
0262h		LRA82L	XXh
0263h		LRA83L	XXh
0264h		LRA84L	XXh
0265h		LRA85L	XXh
0266h		LRA86L	XXh
0267h		LRA87L	XXh
0268h		LRA88L	XXh
0269h		LRA89L	XXh
026Ah		LRA90L	XXh
026Bh		LRA91L	XXh
026Ch		LRA92L	XXh
026Dh		LRA93L	XXh
026Eh		LRA94L	XXh
026Fh		LRA95L	XXh
0270h	LCD Display Control Data Register	LRA0H	XXh
0271h		LRA1H	XXh
0272h		LRA2H	XXh
0273h		LRA3H	XXh
0274h		LRA4H	XXh
0275h		LRA5H	XXh
0276h		LRA6H	XXh
0277h		LRA7H	XXh
0278h		LRA8H	XXh
0279h		LRA9H	XXh
027Ah		LRA10H	XXh
027Bh		LRA11H	XXh
027Ch		LRA12H	XXh
027Dh		LRA13H	XXh
027Eh		LRA14H	XXh
027Fh		LRA15H	XXh

X: Undefined
Note:
1. Blank spaces are reserved. No access is allowed.

Table 4.11 SFR Information (11) (1)

Address	Register	Symbol	After Reset
0280h	LCD Display Control Data Register	LRA16H	XXh
0281h		LRA17H	XXh
0282h		LRA18H	XXh
0283h		LRA19H	XXh
0284h		LRA20H	XXh
0285h		LRA21H	XXh
0286h		LRA22H	XXh
0287h		LRA23H	XXh
0288h		LRA24H	XXh
0289h		LRA25H	XXh
028Ah		LRA26H	XXh
028Bh		LRA27H	XXh
028Ch		LRA28H	XXh
028Dh		LRA29H	XXh
028Eh		LRA30H	XXh
028Fh		LRA31H	XXh
0290h		LRA32H	XXh
0291h		LRA33H	XXh
0292h		LRA34H	XXh
0293h		LRA35H	XXh
0294h		LRA36H	XXh
0295h		LRA37H	XXh
0296h		LRA38H	XXh
0297h		LRA39H	XXh
0298h		LRA40H	XXh
0299h		LRA41H	XXh
029Ah		LRA42H	XXh
029Bh		LRA43H	XXh
029Ch		LRA44H	XXh
029Dh		LRA45H	XXh
029Eh		LRA46H	XXh
029Fh		LRA47H	XXh
02A0h		LRA48H	XXh
02A1h		LRA49H	XXh
02A2h		LRA50H	XXh
02A3h		LRA51H	XXh
02A4h		LRA52H	XXh
02A5h		LRA53H	XXh
02A6h		LRA54H	XXh
02A7h		LRA55H	XXh
02A8h		LRA56H	XXh
02A9h		LRA57H	XXh
02AAh		LRA58H	XXh
02ABh		LRA59H	XXh
02ACh		LRA60H	XXh
02ADh		LRA61H	XXh
02AEh		LRA62H	XXh
02AFh		LRA63H	XXh
02B0h		LRA64H	XXh
02B1h		LRA65H	XXh
02B2h		LRA66H	XXh
02B3h		LRA67H	XXh
02B4h		LRA68H	XXh
02B5h		LRA69H	XXh
02B6h		LRA70H	XXh
02B7h		LRA71H	XXh
02B8h		LRA72H	XXh
02B9h		LRA73H	XXh
02BAh		LRA74H	XXh
02BBh		LRA75H	XXh
02BCh		LRA76H	XXh
02BDh		LRA77H	XXh
02BEh		LRA78H	XXh
02BFh		LRA79H	XXh

X: Undefined
Note:
1. Blank spaces are reserved. No access is allowed.

Table 4.12 SFR Information (12) (1)

Address	Register	Symbol	After Reset
02C0h	LCD Display Control Data Register	LRA80H	XXh
02C1h		LRA81H	XXh
02C2h		LRA82H	XXh
02C3h		LRA83H	XXh
02C4h		LRA84H	XXh
02C5h		LRA85H	XXh
02C6h		LRA86H	XXh
02C7h		LRA87H	XXh
02C8h		LRA88H	XXh
02C9h		LRA89H	XXh
02CAh		LRA90H	XXh
02CBh		LRA91H	XXh
02CCh		LRA92H	XXh
02CDh		LRA93H	XXh
02CEh		LRA94H	XXh
02CFh		LRA95H	XXh
02D0h			
02D1h			
02D2h			
02D3h			
02D4h			
02D5h			
02D6h			
02D7h			
02D8h			
02D9h			
02DAh			
02DBh			
02DCh			
02DDh			
02DEh			
02DFh			
02E0h			
02E1h			
02E2h			
02E3h			
02E4h			
02E5h			
02E6h			
02E7h			
02E8h			
02E9h			
02EAh			
02EBh			
02ECh			
02EDh			
02EEh			
02EFh			
02F0h			
02F1h			
02F2h			
02F3h			
02F4h			
02F5h			
02F6h			
02F7h			
02F8h			
02F9h			
02FAh			
02FBh			
02FCh			
02FDh			
02FEh			
02FFh			

X: Undefined
Note:
1. Blank spaces are reserved. No access is allowed.

Table 4.13 SFR Information (13) (1)

Address	Register	Symbol	After Reset
2C00h	DTC Transfer Vector Area		XXh
2C01h	DTC Transfer Vector Area		XXh
2C02h	DTC Transfer Vector Area		XXh
2C03h	DTC Transfer Vector Area		XXh
2C04h	DTC Transfer Vector Area		XXh
2C05h	DTC Transfer Vector Area		XXh
2C06h	DTC Transfer Vector Area		XXh
2C07h	DTC Transfer Vector Area		XXh
2C08h	DTC Transfer Vector Area		XXh
2C09h	DTC Transfer Vector Area		XXh
2C0Ah	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
2C3Ah	DTC Transfer Vector Area		XXh
2C3Bh	DTC Transfer Vector Area		XXh
2C3Ch	DTC Transfer Vector Area		XXh
2C3Dh	DTC Transfer Vector Area		XXh
2C3Eh	DTC Transfer Vector Area		XXh
2C3Fh	DTC Transfer Vector Area		XXh
2C40h	DTC Control Data 0	DTCD0	XXh
2C41h			XXh
2C42h			XXh
2C43h			XXh
2C44h			XXh
2C45h			XXh
2C46h			XXh
2C47h			XXh
2C48h	DTC Control Data 1	DTCD1	XXh
2C49h			XXh
2C4Ah			XXh
2C4Bh			XXh
2C4Ch			XXh
2C4Dh			XXh
2C4Eh			XXh
2C4Fh			XXh
2C50h	DTC Control Data 2	DTCD2	XXh
2C51h			XXh
2C52h			XXh
2C53h			XXh
2C54h			XXh
2C55h			XXh
2C56h			XXh
2C57h			XXh
2C58h	DTC Control Data 3	DTCD3	XXh
2C59h			XXh
2C5Ah			XXh
2C5Bh			XXh
2C5Ch			XXh
2C5Dh			XXh
2C5Eh			XXh
2C5Fh			XXh
2C60h	DTC Control Data 4	DTCD4	XXh
2C61h			XXh
2C62h			XXh
2C63h			XXh
2C64h			XXh
2C65h			XXh
2C66h			XXh
2C67h			XXh
2C68h	DTC Control Data 5	DTCD5	XXh
2C69h			XXh
2C6Ah			XXh
2C6Bh			XXh
2C6Ch			XXh
2C6Dh			XXh
2C6Eh			XXh
2C6Fh			XXh

X: Undefined
Note:
1. Blank spaces are reserved. No access is allowed.

Table 4.14 SFR Information (14) (1)

Address	Register	Symbol	After Reset
2C70h	DTC Control Data 6	DTCD6	XXh
2C71h			XXh
2C72h			XXh
2C73h			XXh
2C74h			XXh
2C75h			XXh
2C76h			XXh
2C77h			XXh
2C78h	DTC Control Data 7	DTCD7	XXh
2C79h			XXh
2C7Ah			XXh
2C7Bh			XXh
2C7Ch			XXh
2C7Dh			XXh
2C7Eh			XXh
2C7Fh			XXh
2C80h	DTC Control Data 8	DTCD8	XXh
2C81h			XXh
2C82h			XXh
2C83h			XXh
2C84h			XXh
2C85h			XXh
2C86h			XXh
2C87h			XXh
2C88h	DTC Control Data 9	DTCD9	XXh
2C89h			XXh
2C8Ah			XXh
2C8Bh			XXh
2C8Ch			XXh
2C8Dh			XXh
2C8Eh			XXh
2C8Fh			XXh
2C90h	DTC Control Data 10	DTCD10	XXh
2C91h			XXh
2C92h			XXh
2C93h			XXh
2C94h			XXh
2C95h			XXh
2C96h			XXh
2C97h			XXh
2C98h	DTC Control Data 11	DTCD11	XXh
2C99h			XXh
2C9Ah			XXh
2C9Bh			XXh
2C9Ch			XXh
2C9Dh			XXh
2C9Eh			XXh
2C9Fh			XXh
2CA0h	DTC Control Data 12	DTCD12	XXh
2CA1h			XXh
2CA2h			XXh
2CA3h			XXh
2CA4h			XXh
2CA5h			XXh
2CA6h			XXh
2CA7h			XXh
2CA8h	DTC Control Data 13	DTCD13	XXh
2CA9h			XXh
2CAAh			XXh
2CABh			XXh
2CACh			XXh
2CADh			XXh
2CAEh			XXh
2CAFh			XXh

X: Undefined
Note:
1. Blank spaces are reserved. No access is allowed.

Table 4.15 SFR Information (15) (1)

Address	Register	Symbol	After Reset
2CB0h	DTC Control Data 14	DTCD14	XXh
2CB1h			XXh
2CB2h			XXh
2CB3h			XXh
2CB4h			XXh
2CB5h			XXh
2CB6h			XXh
2CB7h			XXh
2CB8h	DTC Control Data 15	DTCD15	XXh
2CB9h			XXh
2CBAh			XXh
2CBBh			XXh
2CBCh			XXh
2CBDh			XXh
2CBEh			XXh
2CBFh			XXh
2CC0h	DTC Control Data 16	DTCD16	XXh
2CC1h			XXh
2CC2h			XXh
2CC3h			XXh
2CC4h			XXh
2CC5h			XXh
2CC6h			XXh
2CC7h			XXh
2CC8h	DTC Control Data 17	DTCD17	XXh
2CC9h			XXh
2CCAh			XXh
2CCBh			XXh
2CCCh			XXh
2CCDh			XXh
2CCEh			XXh
2CCFh			XXh
2CD0h	DTC Control Data 18	DTCD18	XXh
2CD1h			XXh
2CD2h			XXh
2CD3h			XXh
2CD4h			XXh
2CD5h			XXh
2CD6h			XXh
2CD7h			XXh
2CD8h	DTC Control Data 19	DTCD19	XXh
2CD9h			XXh
2CDAh			XXh
2CDBh			XXh
2CDCh			XXh
2CDDh			XXh
2CDEh			XXh
2CDFh			XXh
2CE0h	DTC Control Data 20	DTCD20	XXh
2CE1h			XXh
2CE2h			XXh
2CE3h			XXh
2CE4h			XXh
2CE5h			XXh
2CE6h			XXh
2CE7h			XXh
2CE8h	DTC Control Data 21	DTCD21	XXh
2CE9h			XXh
2CEAh			XXh
2CEBh			XXh
2CECh			XXh
2CEDh			XXh
2CEEh			XXh
2CEFh			XXh

X: Undefined
Note:
1. Blank spaces are reserved. No access is allowed.

Table 4.16 SFR Information (16) (1)

Address	Register	Symbol	After Reset
2CF0h	DTC Control Data 22	DTCD22	XXh
2CF1h			XXh
2CF2h			XXh
2CF3h			XXh
2CF4h			XXh
2CF5h			XXh
2CF6h			XXh
2CF7h			XXh
2CF8h	DTC Control Data 23	DTCD23	XXh
2CF9h			XXh
2CFAh			XXh
2CFBh			XXh
2CFCh			XXh
2CFDh			XXh
2CFEh			XXh
2CFFh			XXh
2D00h			
2D01h			
0FFDBh	Option Function Select Register 2	OFS2	(Note 2)
:			
0FFFFh	Option Function Select Register	OFS	(Note 2)

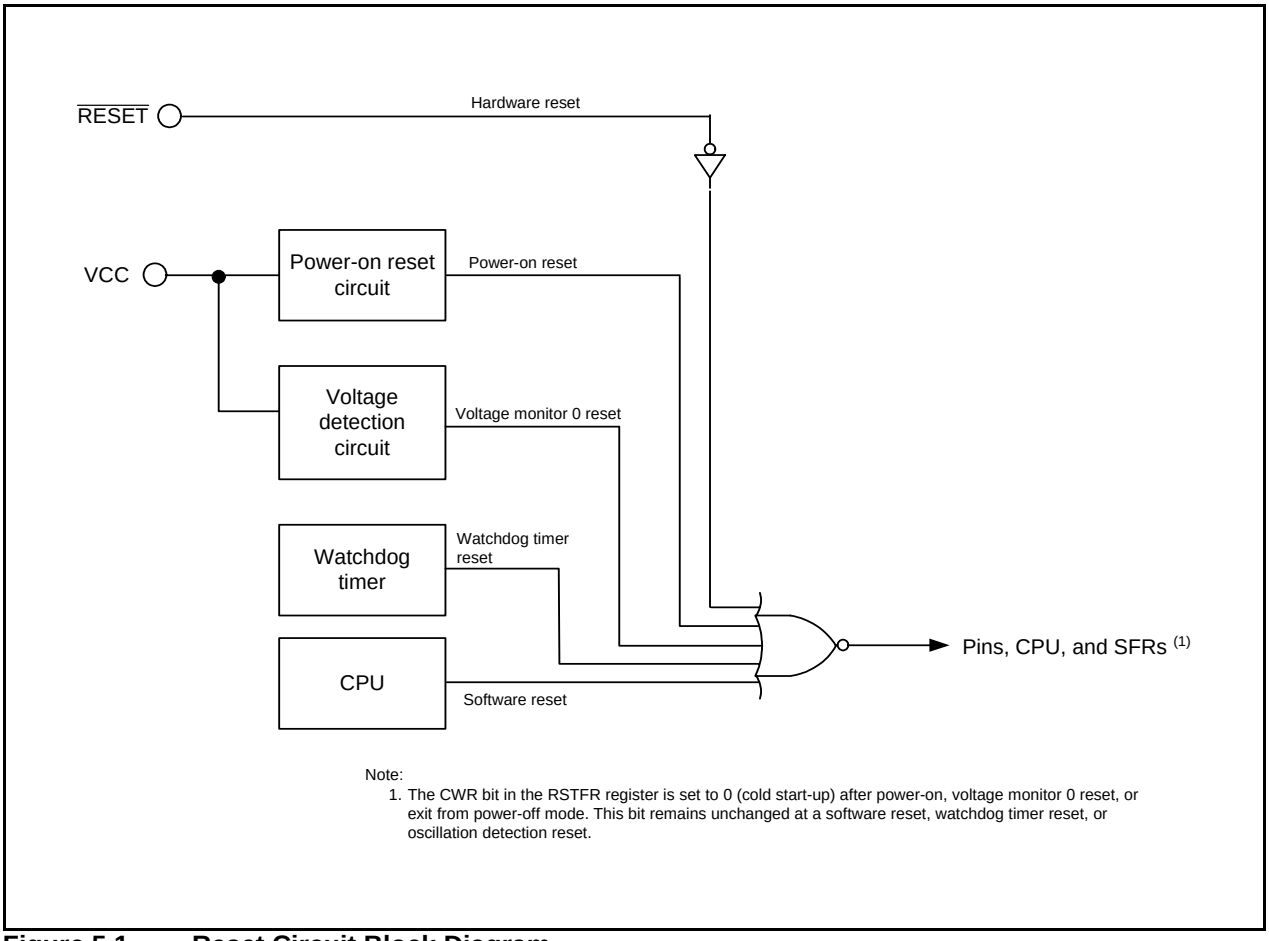
X: Undefined
Notes:
1. Blank spaces are reserved. No access is allowed.
2. This register cannot be changed by a program. Use a flash programmer to write to it.

5. Resets

The following resets are available: hardware reset, power-on reset, voltage monitor 0 reset, watchdog timer reset, and software reset.
Table 5.1 lists the Reset Names and Sources and Figure 5.1 shows the Reset Circuit Block Diagram.

Table 5.1 Reset Names and Sources

Reset Name	Source
Hardware reset	The input voltage to the $\overline{\text{RESET}}$ pin is held low.
Power-on reset	VCC rises.
Voltage monitor 0 reset	VCC falls. (Monitor voltage: Vdet0)
Watchdog timer reset	Underflow of the watchdog timer
Software reset	Write 1 to the PM03 bit in the PM0 register.



Note:
1. The CWR bit in the RSTFR register is set to 0 (cold start-up) after power-on, voltage monitor 0 reset, or exit from power-off mode. This bit remains unchanged at a software reset, watchdog timer reset, or oscillation detection reset.

Figure 5.1 Reset Circuit Block Diagram

Table 5.2 shows the Pin Status while RESET Pin Level is Low. Figure 5.2 shows the CPU Register Status after Reset and Figure 5.3 shows the Reset Sequence.

Table 5.2 Pin Status while $\overline{\text{RESET}}$ Pin Level is Low

Pin Name	Pin Status
P0 to P13	High impedance
$\overline{\text{WKUP0}}$	High impedance
XCIN, XCOUT	Undefined
VL1 to LVL4	High impedance

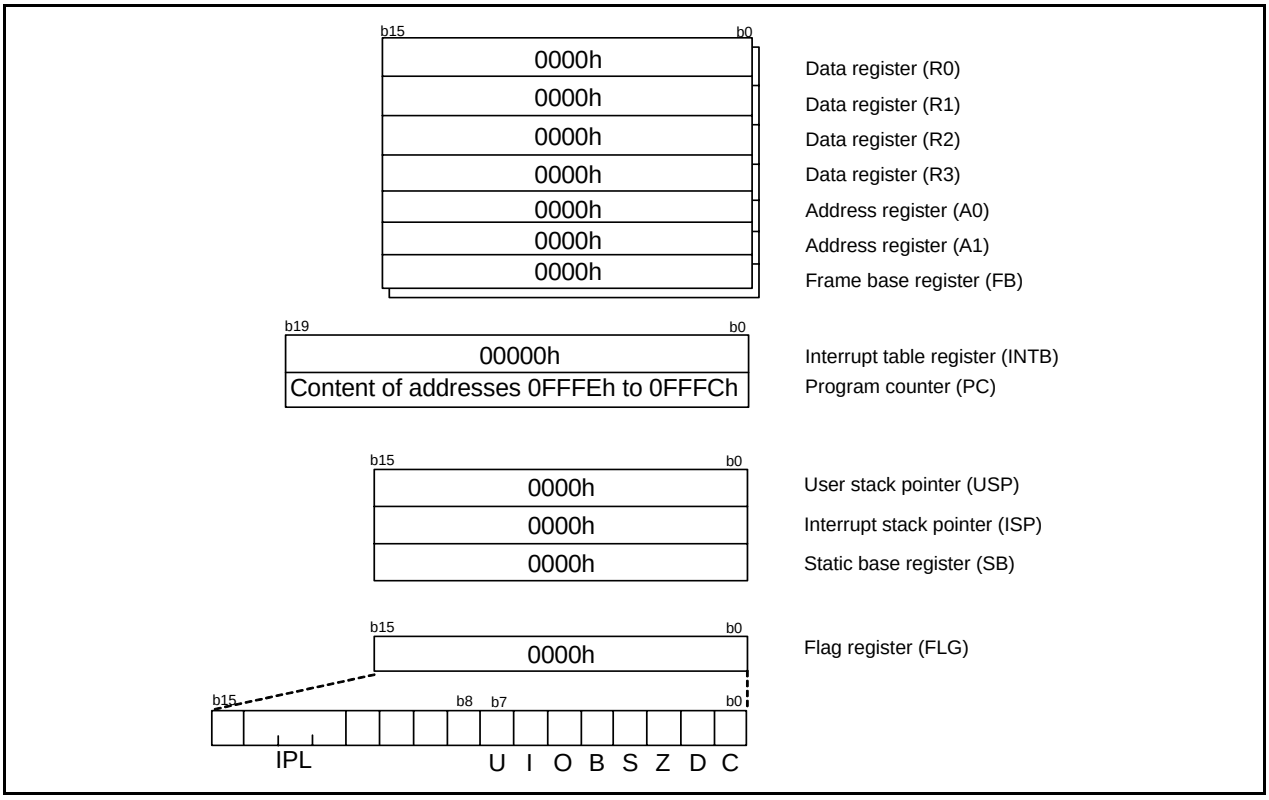
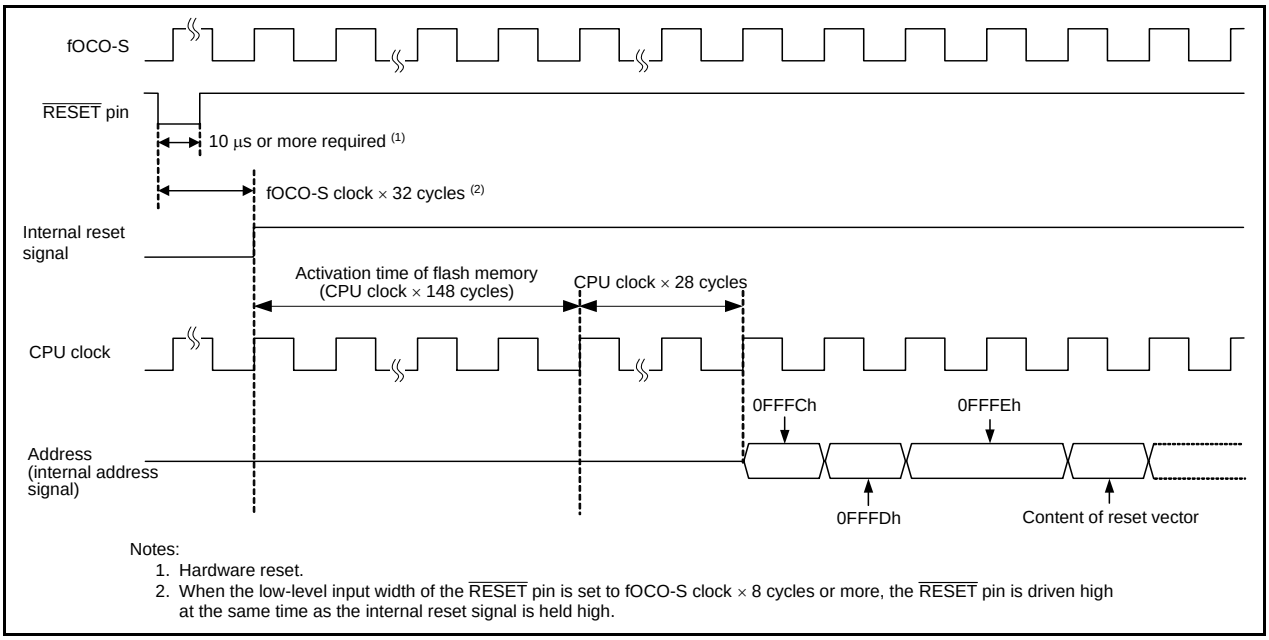


Figure 5.2 CPU Register Status after Reset



Notes:
1. Hardware reset.
2. When the low-level input width of the $\overline{\text{RESET}}$ pin is set to fOCO-S clock × 8 cycles or more, the $\overline{\text{RESET}}$ pin is driven high at the same time as the internal reset signal is held high.

Figure 5.3 Reset Sequence

5.1 Registers

5.1.1 Processor Mode Register 0 (PM0)

Address 0004h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	PM03	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	PM03	Software reset bit	Setting this bit to 1 resets the MCU. When read, the content is 0.	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting the PM0 register.

5.1.2 Reset Source Determination Register (RSTFR)

Address 000Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	—	—	WDR	SWR	HWR	CWR	
After Reset	X	X	X	X	0	0	X	X	(Note 1)

Bit	Symbol	Bit Name	Function	R/W
b0	CWR	Cold start-up/warm start-up determine flag (2, 3)	0: Cold start-up 1: Warm start-up	R/W
b1	HWR	Hardware reset detect flag (4)	0: Not detected 1: Detected	R
b2	SWR	Software reset detect flag	0: Not detected 1: Detected	R
b3	WDR	Watchdog timer reset detect flag	0: Not detected 1: Detected	R
b4	—	Reserved bits	When read, the content is undefined.	R
b5	—			
b6	—			
b7	—			

Notes:
1. The CWR bit is set to 0 (cold start-up) after power-on, voltage monitor 0 reset, or exit from power-off mode. This bit remains unchanged at a hardware reset, software reset, or watchdog timer reset.
2. When 1 is written to the CWR bit by a program, it is set to 1. (Writing 0 does not affect this bit.)
3. When the VW0C0 bit in the VW0C register is set to 0 (voltage monitor 0 reset disabled), the CWR bit value is undefined.
4. A hardware reset or an exit from power-off mode is detected.

5.1.3 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON	
When shipping	1	1	1	1	1	1	1	1	(Note 1)

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bit (2)	b5 b4 0 0: 3.80 V selected (Vdet0_3) 0 1: 2.85 V selected (Vdet0_2) 1 0: 2.35 V selected (Vdet0_1) 1 1: 1.90 V selected (Vdet0_0)	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protection mode enabled after reset 1: Count source protection mode disabled after reset	R/W

Notes:
1. If the block including the OFS register is erased, the OFS register value is set to FFh.
2. The same level of the voltage detection 0 level selected by bits VDSEL0 and VDESL1 is set in both functions of voltage monitor 0 reset and power-on reset.
3. To use power-on reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

The OFS register is allocated in the flash memory. Write to this register with a program.
After writing, do not write additions to this register.

LVDAS Bit (Voltage Detection 0 Circuit Start Bit)

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

5.1.4 Option Function Select Register 2 (OFS2)

Address 0FFDBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	—	—	WDTRCS1	WDTRCS0	WDTUFS1	WDTUFS0	
When shipping	1	1	1	1	1	1	1	1	(Note 1)

Bit	Symbol	Bit Name	Function	R/W
b0	WDTUFS0	Watchdog timer underflow period set bit	b1 b0 0 0: 03FFh 0 1: 0FFFh 1 0: 1FFFh 1 1: 3FFFh	R/W
b1	WDTUFS1			R/W
b2	WDTRCS0	Watchdog timer refresh acknowledgement period set bit	b3 b2 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100%	R/W
b3	WDTRCS1			R/W
b4	—	Reserved bits	Set to 1.	R/W
b5	—			
b6	—			
b7	—			

Note:
1. If the block including the OFS2 register is erased, the OFS2 register value is set to FFh.

The OFS2 register is located on the flash memory. Write to this register with a program.
After writing, do not write additions to this register.

Bits WDTRCS0 and WDTRCS1 (Watchdog Timer Refresh Acknowledgement Period Set Bit)

Assuming that the period from when the watchdog timer starts counting until it underflows is 100%, the refresh acknowledgement period for the watchdog timer can be selected.
For details, refer to **15.3.1.1 Refresh Acknowledgment Period**.

5.2 Hardware Reset

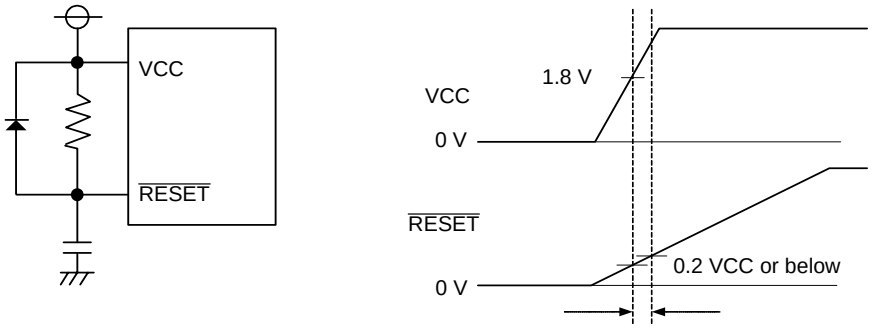
A reset is applied using the $\overline{\text{RESET}}$ pin. When a low-level signal is applied to the $\overline{\text{RESET}}$ pin while the supply voltage meets the recommended operating conditions, the pins, CPU, and SFRs are all reset (refer to **Table 5.2 Pin Status while $\overline{\text{RESET}}$ Pin Level is Low**).
When the input level applied to the $\overline{\text{RESET}}$ pin changes from low to high, a program is executed beginning with the address indicated by the reset vector. After reset, the low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock.
Refer to **4. Special Function Registers (SFRs)** for the status of the SFRs after reset.
The internal RAM is not reset. If the $\overline{\text{RESET}}$ pin is pulled low while writing to the internal RAM is in progress, the contents of internal RAM will be undefined.
Figure 5.4 shows an Example of Hardware Reset Circuit and Operation and Figure 5.5 shows an Example of Hardware Reset Circuit (Usage Example of External Supply Voltage Detection Circuit) and Operation.

5.2.1 When Power Supply is Stable

(1) Apply a low-level signal to the $\overline{\text{RESET}}$ pin.
(2) Wait for 10 µs.
(3) Apply a high-level signal to the $\overline{\text{RESET}}$ pin.

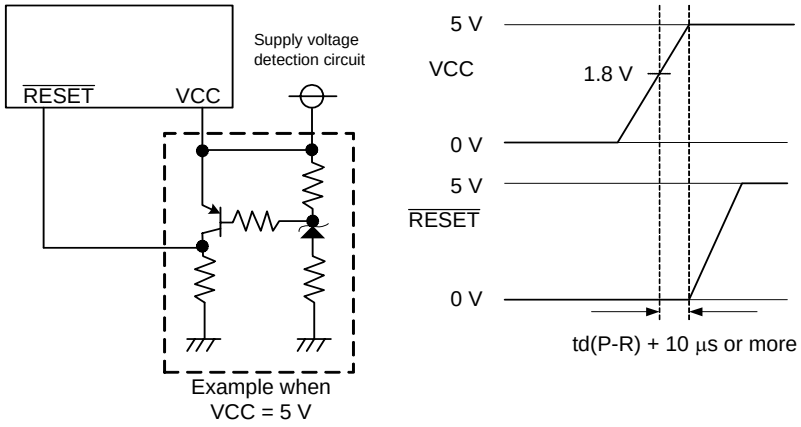
5.2.2 Power On

(1) Apply a low-level signal to the $\overline{\text{RESET}}$ pin.
(2) Let the supply voltage increase until it meets the recommended operating conditions.
(3) Wait for td(P-R) or more to allow the internal power supply to stabilize (refer to **36. Electrical Characteristics**).
(4) Wait for 10 µs.
(5) Apply a high-level signal to the $\overline{\text{RESET}}$ pin.



Note:
1. Refer to **36. Electrical Characteristics.**

Figure 5.4 Example of Hardware Reset Circuit and Operation



Note:
1. Refer to **36. Electrical Characteristics.**

Figure 5.5 Example of Hardware Reset Circuit (Usage Example of External Supply Voltage Detection Circuit) and Operation

5.3 Power-On Reset Function

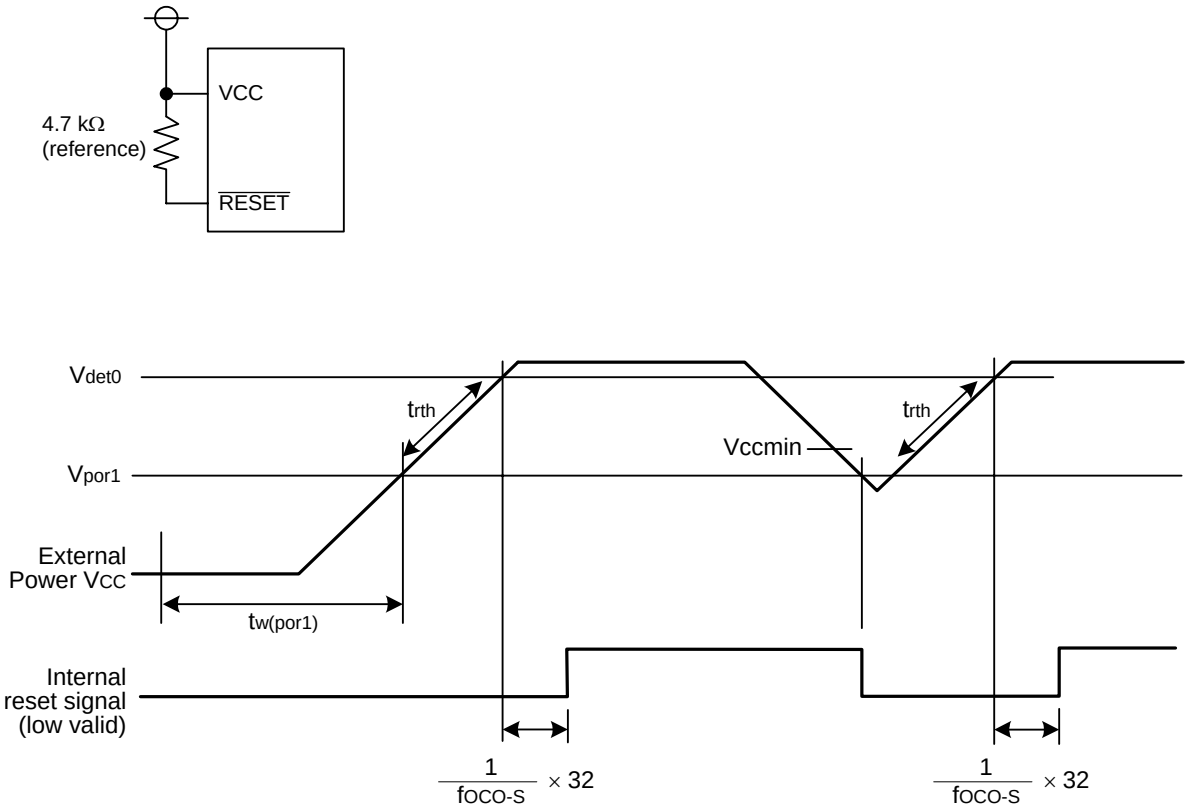
When the $\overline{\text{RESET}}$ pin is connected to the VCC pin via a pull-up resistor, and the VCC pin voltage level rises while the rise gradient is trth or more, the power-on reset function is enabled and the pins, CPU, and SFRs are reset. When a capacitor is connected to the $\overline{\text{RESET}}$ pin, too, always keep the voltage to the $\overline{\text{RESET}}$ pin 0.8 VCC or above.

When the input voltage to the VCC pin reaches the Vdet0 level or above, the low-speed on-chip oscillator clock starts counting. When the low-speed on-chip oscillator clock count reaches 32, the internal reset signal is held high and the MCU enters the reset sequence (refer to Figure 5.3). The low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock after reset.

Refer to **4. Special Function Registers (SFRs)** for the status of the SFRs after power-on reset.

After power-on reset, voltage monitor 0 reset is enabled when the LVDAS bit in the OFS register is set to 0 (voltage monitor 0 reset enabled after reset).

Figure 5.6 shows an Example of Power-On Reset Circuit and Operation.



Notes:
1. Vdet0 indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** for details.
2. Refer to **36. Electrical Characteristics.**
3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0, bits VW0C0 and VW0C6 in the VW0C register to 1 individually, and the VCA25 bit in the VCA2 register to 1.

Figure 5.6 Example of Power-On Reset Circuit and Operation

5.4 Voltage Monitor 0 Reset

A reset is applied using the on-chip voltage detection 0 circuit. The voltage detection 0 circuit monitors the input voltage to the VCC pin. The voltage to monitor is Vdet0. The Vdet0 voltage detection level can be changed by the settings of bits VDSEL0 and VDSEL1 in the OFS register.

When the input voltage to the VCC pin reaches the Vdet0 level or below, the pins, CPU, and SFRs are reset.

When the input voltage to the VCC pin reaches the Vdet0 level or above, the low-speed on-chip oscillator clock starts counting. When the low-speed on-chip oscillator clock count reaches 32, the internal reset signal is held high and the MCU enters the reset sequence (refer to Figure 5.3). The low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock after a reset.

The LVDAS bit in the OFS register can be used to select whether voltage monitor 0 reset is enabled or disabled after a reset. The setting of the LVDAS bit is enabled at all resets.

To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0, bits VW0C0 and VW0C6 bits in the VW0C register to 1 individually, and the VCA25 bit in the VCA2 register to 1.

Bits VDSEL0 to VDSEL1 and LVDAS cannot be changed by a program. To set these bits, write values to b4 to b6 of address 0FFFFh using a flash programmer.

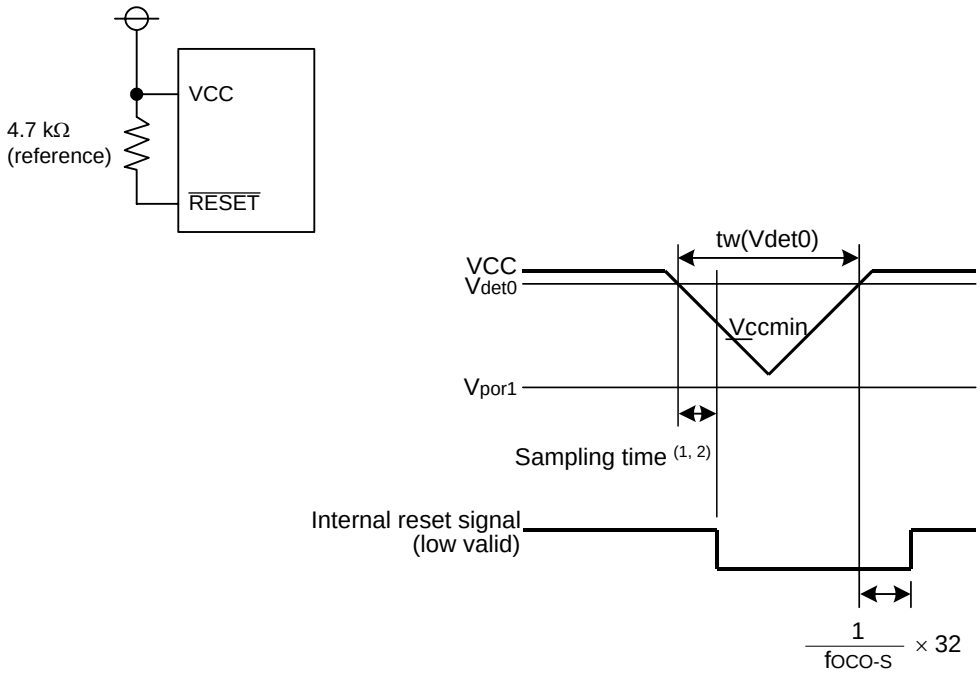
Refer to **5.1.3 Option Function Select Register (OFS)** for details of the OFS register.

Refer to **4. Special Function Registers (SFRs)** for the status of the SFRs after voltage monitor 0 reset.

The internal RAM is not reset. When the input voltage to the VCC pin reaches the Vdet0 level or below while writing to the internal RAM is in progress, the contents of internal RAM are undefined.

Refer to **6. Voltage Detection Circuit** for details of voltage monitor 0 reset.

Figure 5.7 shows an Example of Voltage Monitor 0 Reset Circuit and Operation.



Notes:
1. When using the voltage monitor 0 digital filter, ensure that the voltage is within the MCU operation voltage range (1.8 V or above) during the sampling time.
2. The sampling clock can be selected. Refer to **6. Voltage Detection Circuit** for details.
3. Vdet0 indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** for details.
4. Refer to **36. Electrical Characteristics.**
5. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0, bits VW0C0 and VW0C6 in the VW0C register to 1 individually, and the VCA25 bit in the VCA2 register to 1.

Figure 5.7 Example of Voltage Monitor 0 Reset Circuit and Operation

5.5 Watchdog Timer Reset

When the PM12 bit in the PM1 register is set to 1 (reset when watchdog timer underflows), the MCU resets its pins, CPU, and SFRs when the watchdog timer underflows. Then the program beginning with the address indicated by the reset vector is executed. The low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock after reset.
Refer to **4. Special Function Registers (SFRs)** for the status of the SFRs after watchdog timer reset.
The internal RAM is not reset. When the watchdog timer underflows, the contents of internal RAM are undefined.
The underflow period and refresh acknowledge period for the watchdog timer can be set by bits WDTUFS0 and WDTUFS1 and bits WDTRCS0 and WDTRCS1 in the OFS2 register, respectively.
Refer to **15. Watchdog Timer** for details of the watchdog timer.

5.6 Software Reset

When the PM03 bit in the PM0 register is set to 1 (MCU reset), the MCU resets its pins, CPU, and SFRs. The program beginning with the address indicated by the reset vector is executed. The low-speed on-chip oscillator clock with no division is automatically selected for the CPU clock after reset.
Refer to **4. Special Function Registers (SFRs)** for the status of the SFRs after software reset.
The internal RAM is not reset.

5.7 Cold Start-Up/Warm Start-Up Determination Function

The cold start-up/warm start-up determination function uses the CWR bit in the RSTFR register to determine cold start-up (reset process) at power-on and warm start-up (reset process) when a reset occurred during operation.
The CWR bit is set to 0 (cold start-up) at power-on and also set to 0 at a voltage monitor 0 reset or an exit from power-off mode. When 1 is written to the CWR bit by a program, it is set to 1. This bit remains unchanged at a hardware reset, software reset, or watchdog timer reset.
The cold start-up/warm stat-up determination function uses voltage monitor 0 reset.
To set the bits associated with voltage monitor 0 reset, follow **Table 6.3 Procedure for Setting Bits Associated with Voltage Monitor 0 Reset**.
Figure 5.8 shows an Operating Example of Cold Start-Up/Warm Start-Up Function

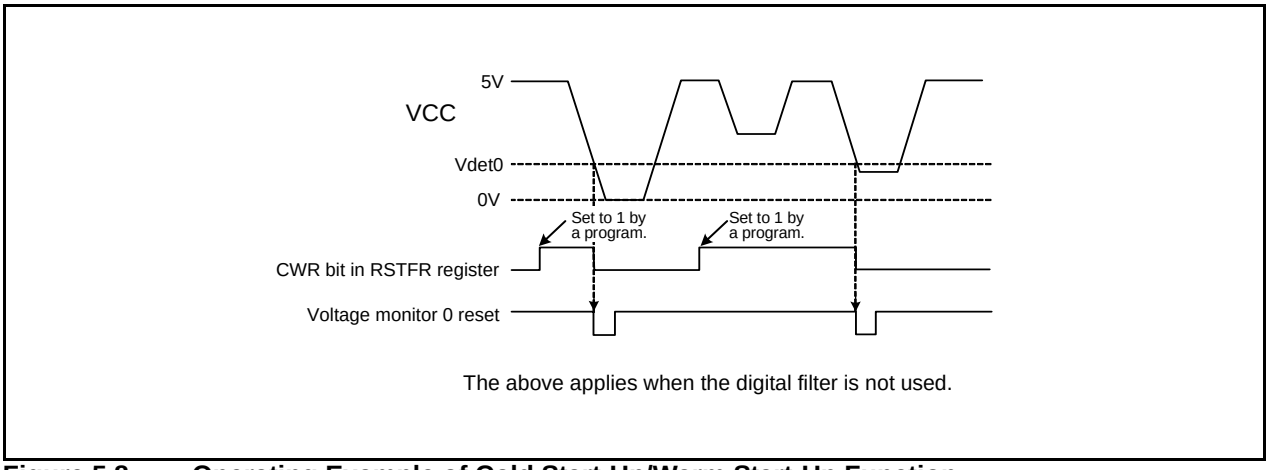


Figure 5.8 Operating Example of Cold Start-Up/Warm Start-Up Function

5.8 Reset Source Determination Function

The RSTFR register can be used to detect whether a hardware reset, software reset, or watchdog timer reset has occurred.
If a hardware reset or an exit from power-off mode occurs, the HWR bit is set to 1 (detected).
If a software reset occurs, the SWR bit is set to 1 (detected).
If a watchdog timer reset occurs, the WDR bit is set to 1 (detected).

6. Voltage Detection Circuit

The voltage detection circuit monitors the voltage input to the VCC pin. This circuit can be used to monitor the VCC input voltage by a program.

6.1 Introduction

The detection voltage of voltage detection 0 can be selected among four levels using the OFS register.
The detection voltage of voltage detection 1 can be selected among 16 levels using the VD1LS register.
As a detection target, the voltage input to VCC and the LVCMP2 pin can be switched for voltage detection 2 only.
The voltage monitor 0 reset, and voltage monitor 1 interrupt and voltage monitor 2 interrupt can also be used.
Note that voltage monitor 1 and voltage monitor 2 share the voltage detection circuit with comparator A1 and comparator A2. Either voltage monitor 1 and voltage monitor 2 or comparator A1 and comparator A2 can be selected.

Table 6.1 Voltage Detection Circuit Specifications

Item		Voltage Monitor 0	Voltage Monitor 1	Voltage Monitor 2
VCC monitor	Voltage to monitor	Vdet0	Vdet1	Vdet2
	Detection target	Whether passing through Vdet0 by falling	Whether passing through Vdet1 by rising or falling	Whether passing through Vdet2 by rising or falling
				The input voltage to VCC and the LVCMP2 pin can be switched by the VCA24 bit in the VCA2 register.
	Detection voltage	Selectable among 4 levels using the OFS register.	Selectable among 16 levels using the VD1LS register.	The detection voltage level varies depending on when VCC is selected or when LVCMP2 is selected. Each value is set as the fixed level.
	Monitor	None	The VW1C3 bit in the VW1C register	The VCA13 bit in the VCA1 register
			Whether VCC is higher or lower than Vdet1	Whether VCC or LVCMP2 input voltage is higher or lower than Vdet2
Process at voltage detection	Reset	Voltage monitor 0 reset	None	None
		Reset at Vdet0 > VCC; CPU operation restarts at VCC > Vdet0		
	Interrupts	None	Voltage monitor 1 interrupt	Voltage monitor 2 interrupt
			Non-maskable or maskable selectable	Non-maskable or maskable selectable
			Interrupt request at: Vdet1 > VCC and/or VCC > Vdet1	Interrupt request at: Vdet2 > VCC (LVCMP2) and/or VCC (LVCMP2) > Vdet2
Digital filter	Switching enable/disable	Supported	Supported	Supported
	Sampling time	(fOCO-S divided by n) × 4 n: 1, 2, 4, and 8	(fOCO-S divided by n) × 2 n: 1, 2, 4, and 8	(fOCO-S divided by n) × 2 n: 1, 2, 4, and 8

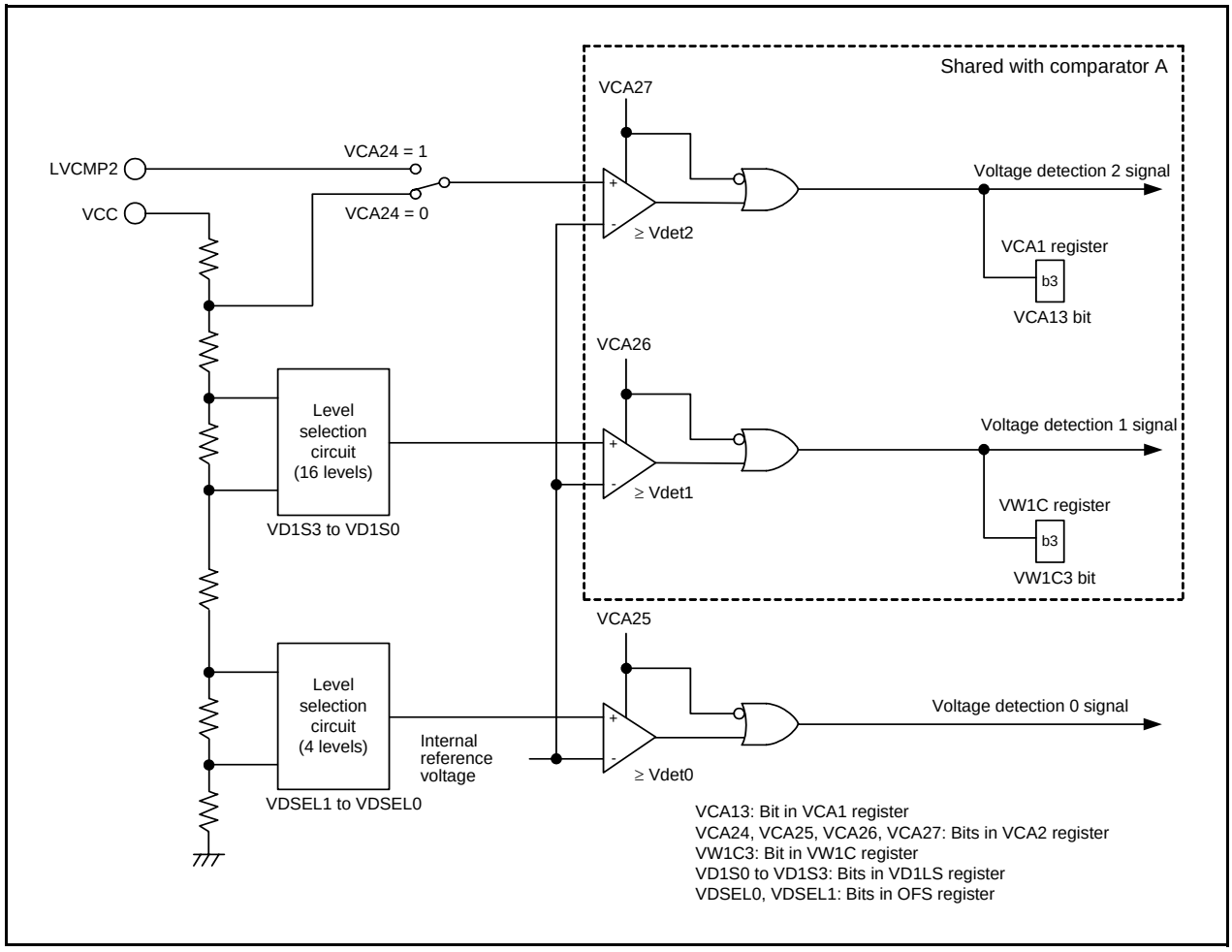


Figure 6.1 Block Diagram of Voltage Detection Circuit

Table 6.2 Pin Configuration of Voltage Detection Circuit

Pin Name	I/O	Function
LVCMP2	Input	Detection target voltage pin for voltage detection 2

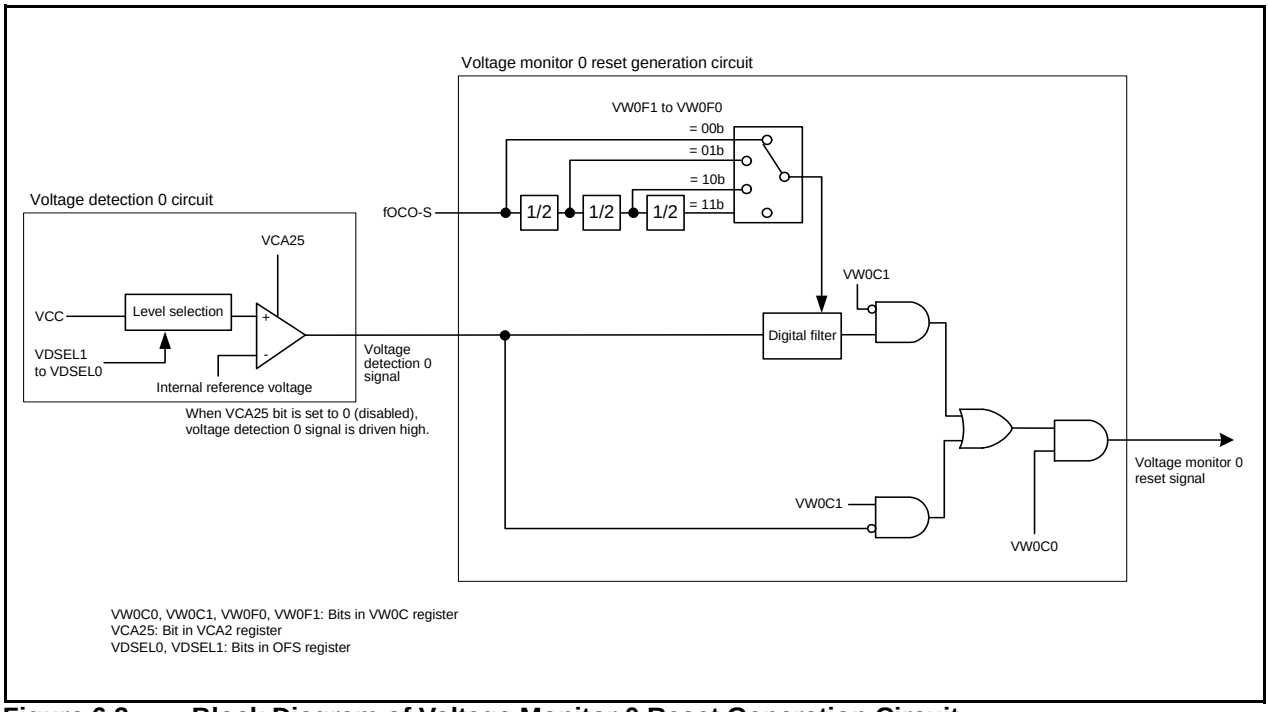


Figure 6.2 Block Diagram of Voltage Monitor 0 Reset Generation Circuit

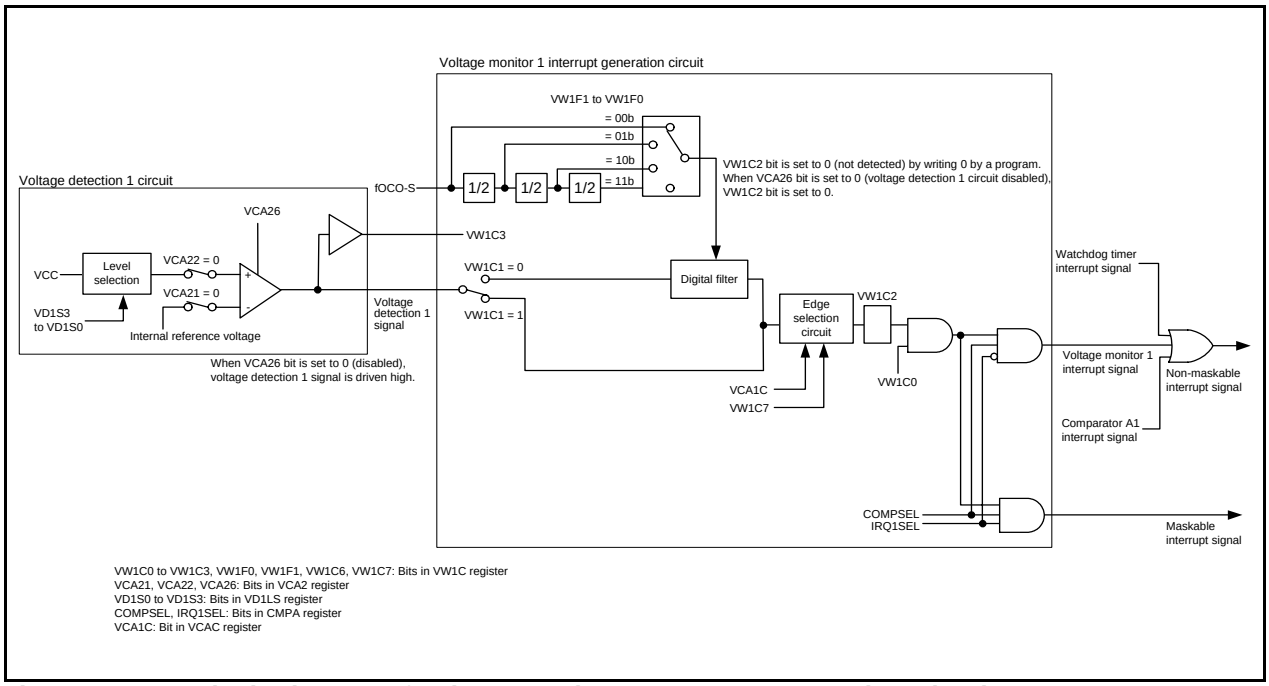


Figure 6.3 Block Diagram of Voltage Monitor 1 Interrupt Generation Circuit

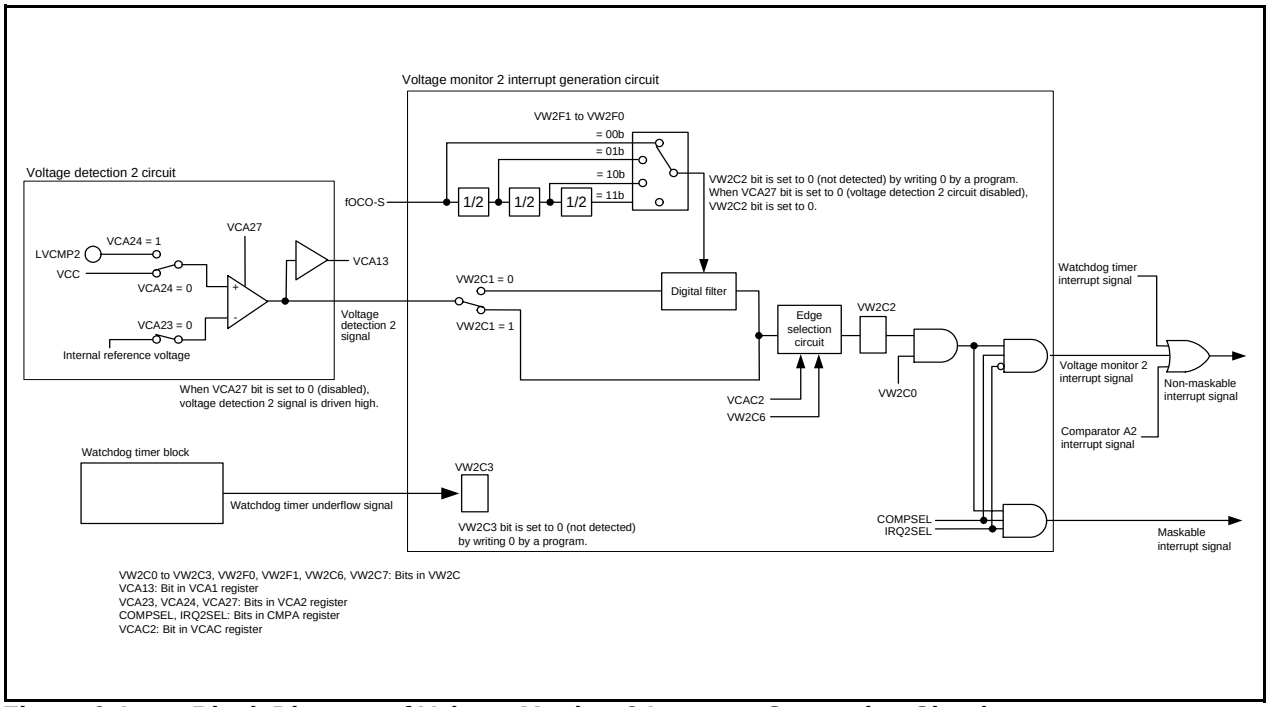


Figure 6.4 Block Diagram of Voltage Monitor 2 Interrupt Generation Circuit

6.2 Registers

6.2.1 Voltage Monitor Circuit/Comparator A Control Register (CMPA)

Address 0030h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	COMPSEL	—	IRQ2SEL	IRQ1SEL	CM2OE	CM1OE	CM2POR	CM1POR
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CM1POR	LVCOUT1 output polarity select bit	0: Non-inverted comparator A1 comparison result is output to LVCOUT1. 1: Inverted comparator A1 comparison result is output to LVCOUT1.	R/W
b1	CM2POR	LVCOUT2 output polarity select bit	0: Non-inverted Comparator A2 comparison result is output to LVCOUT2. 1: Inverted comparator A2 comparison result is output to LVCOUT2.	R/W
b2	CM1OE	LVCOUT1 output enable bit	0: Output disabled 1: Output enabled	R/W
b3	CM2OE	LVCOUT2 output enable bit	0: Output disabled 1: Output enabled	R/W
b4	IRQ1SEL	Voltage monitor 1/comparator A1 interrupt type select bit	0: Non-maskable interrupt 1: Maskable interrupt	R/W
b5	IRQ2SEL	Voltage monitor 2/comparator A2 interrupt type select bit	0: Non-maskable interrupt 1: Maskable interrupt	R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	COMPSEL	Voltage monitor/comparator A interrupt type selection enable bit	0: Bits IRQ1SEL and IRQ2SEL disabled 1: Bits IRQ1SEL and IRQ2SEL enabled	R/W

6.2.2 Voltage Monitor Circuit Edge Select Register (VCAC)

Address 0031h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	VCAC2	VCAC1	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	VCAC1	Voltage monitor 1 circuit edge select bit (1)	0: One edge 1: Both edges	R/W
b2	VCAC2	Voltage monitor 2 circuit edge select bit (2)	0: One edge 1: Both edges	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Notes:
1. When the VCA1 bit is set to 0 (one edge), the VW1C7 bit in the VW1C register is enabled. Set the VW1C7 bit after setting the VCAC1 bit to 0.
2. When the VCA2 bit is set to 0 (one edge), the VW2C7 bit in the VW2C register is enabled. Set the VW2C7 bit after setting the VCAC2 bit to 0.

6.2.3 Voltage Detect Register (VCA1)

Address 0033h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	VCA13	—	—	—
After Reset	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	VCA13	Voltage detection 2 signal monitor flag (1)	0: VCC < Vdet2 1: VCC ≥ Vdet2 or voltage detection 2 circuit disabled	R
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

Note:
1. When the VCA27 bit in the VCA2 register is set to 1 (voltage detection 2 circuit enabled), the VCA13 bit is enabled.
   When the VCA27 bit in the VCA2 register is set to 0 (voltage detection 2 circuit disabled), the VCA13 bit is set to 1 (VCC ≥ Vdet2).

6.2.4 Voltage Detect Register 2 (VCA2)

Address 0034h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VCA27	VCA26	VCA25	VCA24	VCA23	VCA22	VCA21	VCA20
After Reset	The LVDAS bit in the OFS register is set to 1.							
	0	0	0	0	0	0	0	0
After Reset	The LVDAS bit in the OFS register is set to 0.							
	0	0	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	VCA20	Internal power low consumption enable bit (1)	0: Low consumption disabled 1: Low consumption enabled (2)	R/W
b1	VCA21	Comparator A1 reference voltage input select bit	0: Internal reference voltage 1: LVREF pin input voltage	R/W
b2	VCA22	LVCMP1 comparison voltage external input select bit	0: Supply voltage (VCC) 1: LVCMP1 pin input voltage	R/W
b3	VCA23	Comparator A2 reference voltage input select bit	0: Internal reference voltage 1: LVREF pin input voltage	R/W
b4	VCA24	LVCMP2 comparison voltage external input select bit	0: Supply voltage (VCC) (Vdet2_0) 1: LVCMP2 pin input voltage (Vdet2_EXT)	R/W
b5	VCA25	Voltage detection 0 enable bit (3)	0: Voltage detection 0 circuit disabled 1: Voltage detection 0 circuit enabled	R/W
b6	VCA26	Voltage detection 1/comparator A1 enable bit (4)	0: Voltage detection 1/comparator A1 circuit disabled 1: Voltage detection 1/comparator A1 circuit enabled	R/W
b7	VCA27	Voltage detection 2/comparator A2 enable bit (5)	0: Voltage detection 2/comparator A2 circuit disabled 1: Voltage detection 2/comparator A2 circuit enabled	R/W

Notes:
1. Use the VCA20 bit only when the MCU enters wait mode. To set the VCA20 bit, follow the procedure shown in **Figure 10.7 Handling Procedure for Reducing Internal Power Consumption Using VCA20 Bit**.
2. When the VCA20 bit is set to 1 (low consumption enabled), do not set the CM10 bit in the CM1 register to 1 (stop mode).
3. To use voltage monitor 0 reset, set the VCA25 bit to 1.
   After the VCA25 bit is set to 1 from 0, allow td(E-A) to elapse before the voltage detection circuit starts operation.
4. To use the voltage detection 1/comparator A1 interrupt or the VW1C3 bit in the VW1C register, set the VCA26 bit to 1.
   After the VCA26 bit is set to 1 from 0, allow td(E-A) to elapse before the voltage detection 1/comparator A1 circuit starts operation.
5. To use the voltage detection 2/comparator A2 interrupt or the VCAC13 bit in the VCA1 register, set the VCA27 bit to 1.
   After the VCA27 bit is set to 1 from 0, allow td(E-A) to elapse before the voltage detection 2/comparator A2 circuit starts operation.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VCA2 register.

6.2.5 Voltage Detection 1 Level Select Register (VD1LS)

Address 0036h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	VD1S3	VD1S2	VD1S1	VD1S0
After Reset	0	0	0	0	0	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	VD1S0	Voltage detection 1 level select bit (Reference voltage when the voltage falls)	b3 b2 b1 b0 0 0 0 0: 2.20 V (Vdet1_0) 0 0 0 1: 2.35 V (Vdet1_1) 0 0 1 0: 2.50 V (Vdet1_2) 0 0 1 1: 2.65 V (Vdet1_3) 0 1 0 0: 2.80 V (Vdet1_4) 0 1 0 1: 2.95 V (Vdet1_5) 0 1 1 0: 3.10 V (Vdet1_6) 0 1 1 1: 3.25 V (Vdet1_7) 1 0 0 0: 3.40 V (Vdet1_8) 1 0 0 1: 3.55 V (Vdet1_9) 1 0 1 0: 3.70 V (Vdet1_A) 1 0 1 1: 3.85 V (Vdet1_B) 1 1 0 0: 4.00 V (Vdet1_C) 1 1 0 1: 4.15 V (Vdet1_D) 1 1 1 0: 4.30 V (Vdet1_E) 1 1 1 1: 4.45 V (Vdet1_F)	R/W
b1	VD1S1			R/W
b2	VD1S2			R/W
b3	VD1S3			R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			R/W
b6	—			R/W
b7	—			R/W

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VD1LS register.

6.2.6 Voltage Monitor 0 Circuit Control Register (VW0C)

Address 0038h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	VW0F1	VW0F0	—	—	VW0C1	VW0C0
After Reset	The LVDAS bit in the OFS register is set to 1.							
	1	1	0	0	X	0	1	0
After Reset	The LVDAS bit in the OFS register is set to 0.							
	1	1	0	0	X	0	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	VW0C0	Voltage monitor 0 reset enable bit (1)	0: Disabled 1: Enabled	R/W
b1	VW0C1	Voltage monitor 0 digital filter disabled mode select bit	0: Digital filter enabled mode (digital filter circuit enabled) 1: Digital filter disabled mode (digital filter circuit disabled)	R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	—	Reserved bit	When read, the content is undefined.	R
b4	VW0F0	Sampling clock select bit	b5 b4 0 0: fOCO-S divided by 1 0 1: fOCO-S divided by 2 1 0: fOCO-S divided by 4 1 1: fOCO-S divided by 8	R/W
b5	VW0F1			R/W
b6	—	Reserved bits	Set to 1.	R/W
b7	—			R/W

Note:
1. The VW0C0 bit is enabled when the VCA25 bit in the VCA2 register is set to 1 (voltage detection 0 circuit enabled). Set the VW0C0 bit to 0 (disabled) when the VCA25 bit in the VCA2 register is set to 0 (voltage detection 0 circuit disabled). To set the VW0C0 bit to 1 (enabled), follow the procedure in **Table 6.3 Procedure for Setting Bits Associated with Voltage Monitor 0 Reset**.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before writing to the VW0C register.

6.2.7 Voltage Monitor 1 Circuit Control Register (VW1C)

Address 0039h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VW1C7	—	VW1F1	VW1F0	VW1C3	VW1C2	VW1C1	VW1C0
After Reset	1	0	0	0	1	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	VW1C0	Voltage monitor 1 reset enable bit (1)	0: Disabled 1: Enabled	R/W
b1	VW1C1	Voltage monitor 0 digital filter disable mode select bit (2)	0: Digital filter enabled mode (digital filter circuit enabled) 1: Digital filter disable mode (digital filter circuit disabled)	R/W
b2	VW1C2	Voltage change detection flag (3, 4)	0: Not detected 1: Vdet1 passing detected	R/W
b3	VW1C3	Voltage detection 1 signal monitor flag (3)	0: VCC < Vdet1 1: VCC ≥ Vdet1 or voltage detection 1 circuit disabled	R
b4	VW1F0	Sampling clock select bit	b5 b4 0 0: fOCO-S divided by 1 0 1: fOCO-S divided by 2 1 0: fOCO-S divided by 4 1 1: fOCO-S divided by 8	R/W
b5	VW1F1			R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	VW1C7	Voltage monitor 1 reset generation condition select bit (5)	0: When VCC reaches Vdet1 or above. 1: When VCC reaches Vdet1 or below.	R/W

Notes:
1. The VW1C0 is enabled when the VCA26 bit in the VCA2 register is set to 1 (voltage detection 1 circuit enabled). Set the VW1C0 bit to 0 (disabled) when the VCA26 bit is set to 0 (voltage detection 1 circuit disabled). To set the VW0C0 bit to 1 (enabled), follow the procedure shown in **Table 6.4 Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt**.
2. To use the voltage monitor 1 interrupt to exit stop mode and to return again, write 0 and then 1 to the VW1C1 bit.
3. Bits VW1C2 and VW1C3 are enabled when the VCA26 bit in the VCA2 register is set to 1 (voltage detection 1 circuit enabled).
4. Set the VW1C2 bit to 0 by a program. When 0 is written by a program, this bit is set to 0 (and remains unchanged even if 1 is written to it).
5. The VW1C7 bit is enabled when the VCAC1 bit in the VCAC register is set to 0 (one edge). After setting the VCAC1 bit to 0, set the VW1C7 bit.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before writing the VW1C register.
Rewriting the VW1C register may set the VW1C2 bit to 1. Set the VW1C2 bit to 0 after rewriting the VW1C register.

6.2.8 Voltage Monitor 2 Circuit Control Register (VW2C)

Address 003Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VW2C7	—	VW2F1	VW2F0	VW2C3	VW2C2	VW2C1	VW2C0
After Reset	1	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	VW2C0	Voltage monitor 2 interrupt enable bit (1)	0: Disabled 1: Enabled	R/W
b1	VW2C1	Voltage monitor 2 digital filter disable mode select bit (2)	0: Digital filter enable mode (digital filter circuit enabled) 1: Digital filter disable mode (digital filter circuit disabled)	R/W
b2	VW2C2	Voltage change detection flag (3, 4)	0: Not detected 1: Vdet2 passing detected	R/W
b3	VW2C3	WDT detection monitor flag (4)	0: Not detected 1: Detected	R/W
b4	VW2F0	Sampling clock select bit	b5 b4 0 0: fOCO-S divided by 1 0 1: fOCO-S divided by 2 1 0: fOCO-S divided by 4 1 1: fOCO-S divided by 8	R/W
b5	VW2F1			R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	VW2C7	Voltage monitor 2 interrupt generation condition select bit (5)	0: When VCC or LVCMP2 reaches Vdet2 or above. 1: When VCC or LVCMP2 reaches Vdet2 or below.	R/W

Notes:

1. The VW2C0 is enabled when the VCA27 bit in the VCA2 register is set to 1 (voltage detection 2 circuit enabled). Set the VW2C0 bit to 0 (disabled) when the VCA27 bit is set to 0 (voltage detection 2 circuit disabled). To set the VW2C0 bit to 1 (enabled), follow the procedure shown in **Table 6.5 Procedure for Setting Bits Associated with Voltage Monitor 2 Interrupt**.
2. To use the voltage monitor 2 interrupt to exit stop mode and to return again, write 0 and then 1 to the VW2C1 bit.
3. The VW2C2 bit is enabled when the VCA27 bit in the VCA2 register is set to 1 (voltage detection 2 circuit enabled).
4. Set this bit to 0 by a program. When 0 is written by a program, this bit is set to 0 (and remains unchanged even if 1 is written to it).
5. The VW2C7 bit is enabled when the VCAC2 bit in the VCAC register is set to 0 (one edge). After setting the VCAC2 bit to 0, set the VW2C7 bit.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VW2C register.
Rewriting the VW2C register may set the VW2C2 bit to 1. After rewriting this register, set the VW2C2 bit to 0.

6.2.9 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON	
When shipping	1	1	1	1	1	1	1	1	(Note 1)

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bit (2)	b5 b4 0 0: 3.80 V selected (Vdet0_3) 0 1: 2.85 V selected (Vdet0_2) 1 0: 2.35 V selected (Vdet0_1) 1 1: 1.90 V selected (Vdet0_0)	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protection mode enabled after reset 1: Count source protection mode disabled after reset	R/W

Notes:
1. If the block including the OFS register is erased, the OFS register value is set to FFh.
2. The same level of the voltage detection 0 level selected by bits VDSEL0 and VDESL1 is set in both functions of voltage monitor 0 reset and power-on reset.
3. To use power-on reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

The OFS register is allocated in the flash memory. Write to this register with a program.
After writing, do not write additions to this register.

LVDAS Bit (Voltage Detection 0 Circuit Start Bit)

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

6.3 VCC Input Voltage

6.3.1 Monitoring Vdet0

Vdet0 cannot be monitored.

6.3.2 Monitoring Vdet1

Once the following settings are made, the comparison result of voltage monitor 1 can be monitored by the VW1C3 bit in the VW1C register after td(E-A) has elapsed (refer to **36. Electrical Characteristics**).

(1) Set bits VD1S3 to VD1S0 in the VD1LS register (voltage detection 1 detection voltage).
(2) Set the VCA21 bit in the VCA2 register to 0 (internal reference voltage).
(3) Set the VCA22 bit in the VCA2 register to 0 (VCC voltage).
(4) Set the VCA26 bit in the VCA2 register to 1 (voltage detection 1 circuit enabled).

6.3.3 Monitoring Vdet2

Once the following settings are made, the comparison result of voltage monitor 2 can be monitored by the VCA13 bit in the VCA1 register after td(E-A) has elapsed (refer to **36. Electrical Characteristics**).

(1) Set the VCA23 bit in the VCA2 register to 0 (internal reference voltage).
(2) Set the VCA24 bit in the VCA2 register to 0 (VCC voltage), or 1 (LVCMP2 pin input voltage).
(3) Set the VCA27 bit in the VCA2 register to 1 (voltage detection 2 circuit enabled).

6.4 Voltage Monitor 0 Reset

Table 6.3 lists the Procedure for Setting Bits Associated with Voltage Monitor 0 Reset and Figure 6.5 shows an Operating Example of Voltage Monitor 0 Reset.

To use the voltage monitor 0 reset to exit stop mode, set the VW0C1 bit in the VW0C register to 1 (digital filter disabled).

Table 6.3 Procedure for Setting Bits Associated with Voltage Monitor 0 Reset

Step	When Using Digital Filter	When Using No Digital Filter
1	Set the VCA25 bit in the VCA2 register to 1 (voltage detection 0 circuit enabled).	
2	Wait for td(E-A).	
3	Select the sampling clock of the digital filter by bits VW0F1 to VW0F0 in the VW0C register.	Set the VW0C7 bit in the VW0C register to 1.
4 (1)	Set the VW0C1 bit in the VW0C register to 0 (digital filter enabled).	Set the VW0C1 bit in the VW0C register to 1 (digital filter disabled).
5	Set the VW0C2 bit in the VW0C register to 0.	
6	Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on).	–
7	Wait for 4 cycles of the sampling clock of the digital filter.	– (No wait time required)
8	Set the VW0C0 bit in the VW0C register to 1 (voltage monitor 0 reset enabled).	

Note:
1. When the VW0C0 bit is set to 0, steps 3 and 4 can be executed simultaneously (with one instruction).

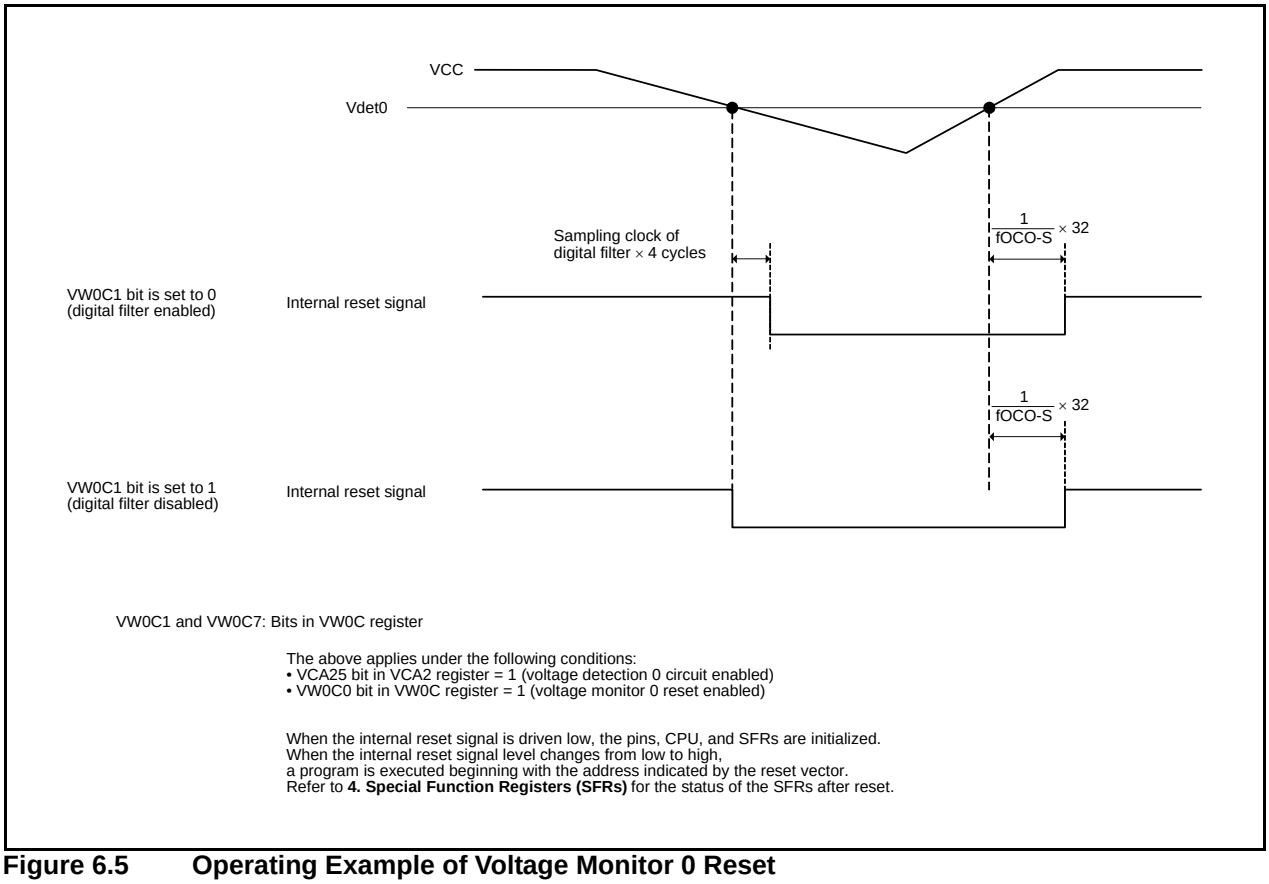


Figure 6.5 Operating Example of Voltage Monitor 0 Reset

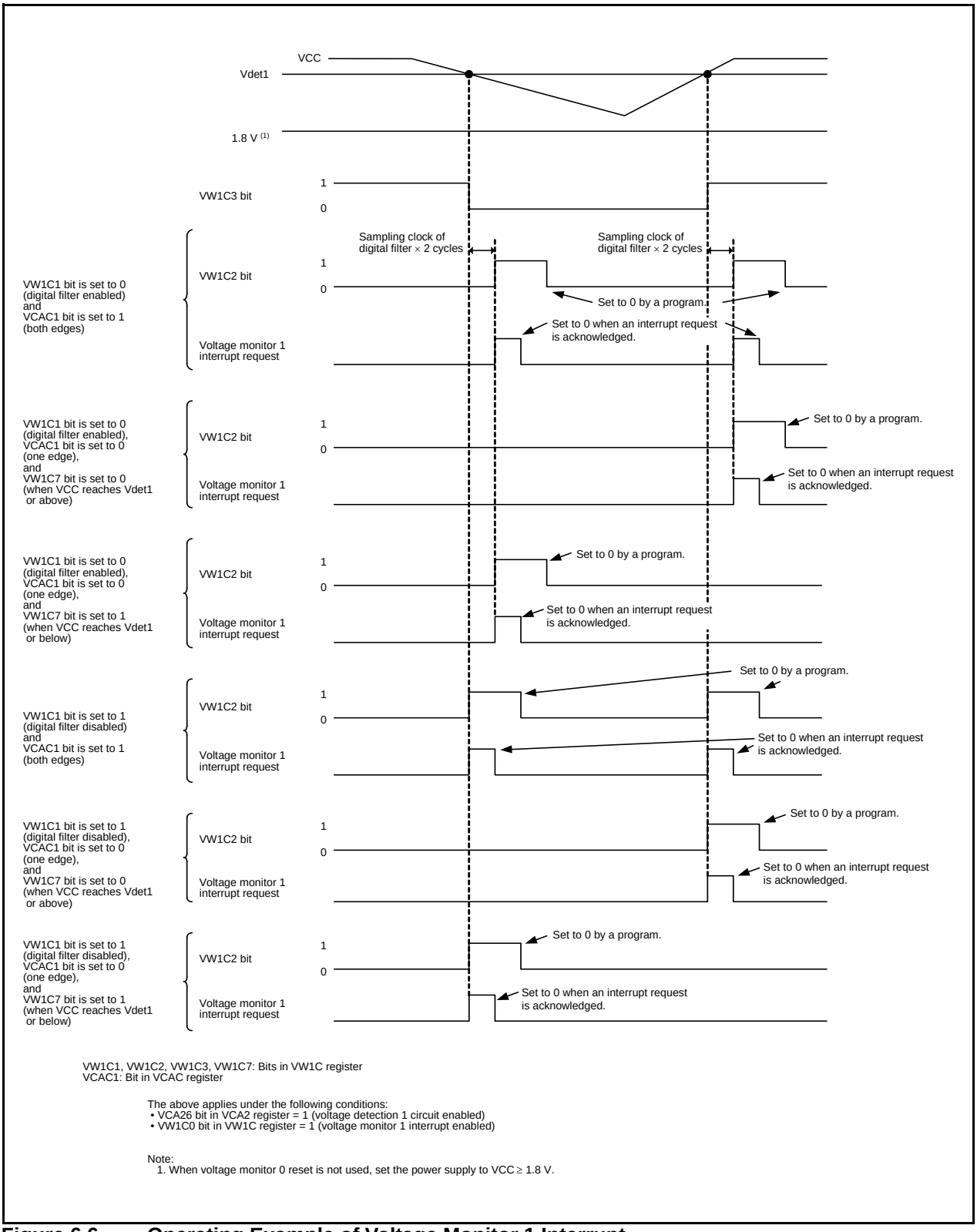
6.5 Voltage Monitor 1 Interrupt

Table 6.4 lists the Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt. Figure 6.6 shows an Operating Example of Voltage Monitor 1 Interrupt.
To use the voltage monitor 1 interrupt to exit stop mode, set the VW1C1 bit in the VW1C register to 1 (digital filter disabled).

Table 6.4 Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt

Step	When Using Digital Filter	When Using No Digital Filter
1	Select the voltage detection 1 detection voltage by bits VD1S3 to VD1S0 in the VD1LS register.	
2	Set the VCA21 bit in the VCA2 register to 0 (internal reference voltage).	
3 (1)	Set the VCA22 bit in the VCA2 register to 0 (VCC voltage).	
4 (1)	Set the VCA26 bit in the VCA2 register to 1 (voltage detection 1 circuit enabled).	
5	Wait for td(E-A).	
6	Set the COMPSEL bit in the CMPA register to 1.	
7 (2)	Select the interrupt type by the IRQ1SEL in the CMPA register.	
8	Select the sampling clock of the digital filter by bits VW1F1 to VW1F0 in the VW1C register.	Set the VW1C1 bit in the VW1C register to 1 (digital filter disabled).
9 (3)	Set the VW1C1 bit in the VW1C register to 0 (digital filter enabled).	–
10	Select the interrupt request timing by the VCAC1 bit in the VCAC register and the VW1C7 bit in the VW1C register.	
11	Set the VW1C2 bit in the VW1C register to 0.	
12	Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on)	–
13	Wait for 2 cycles of the sampling clock of the digital filter	– (No wait time required)
14	Set the VW1C0 bit in the VW1C register to 1 (voltage monitor 1 interrupt enabled)	

Notes:
1. When the VW1C0 bit is set to 0, steps 2, 3, and 4 can be executed simultaneously (with one instruction).
2. When the VW1C0 bit is set to 0, steps 6 and 7 can be executed simultaneously (with one instruction).
3. When the VW1C0 bit is set to 0, steps 8 and 9 can be executed simultaneously (with one instruction).



VW1C1, VW1C2, VW1C3, VW1C7: Bits in VW1C register
VCAC1: Bit in VCAC register

The above applies under the following conditions:
- VCA26 bit in VCA2 register = 1 (voltage detection 1 circuit enabled)
- VW1C0 bit in VW1C register = 1 (voltage monitor 1 interrupt enabled)

Note:
1. When voltage monitor 0 reset is not used, set the power supply to VCC ≥ 1.8 V.

Figure 6.6 Operating Example of Voltage Monitor 1 Interrupt

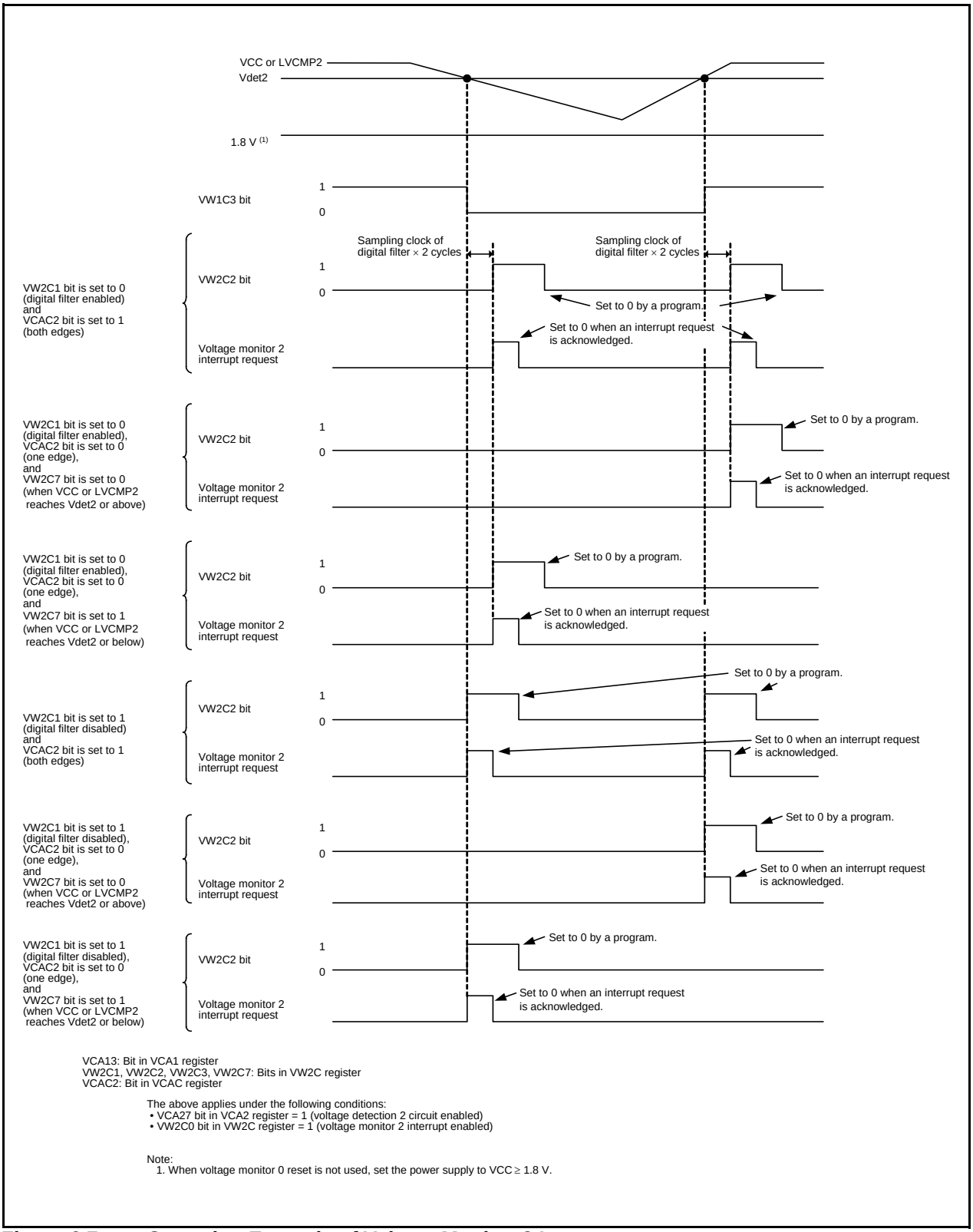
6.6 Voltage Monitor 2 Interrupt

Table 6.5 lists the Procedure for Setting Bits Associated with Voltage Monitor 2 Interrupt. Figure 6.7 shows an Operating Example of Voltage Monitor 2 Interrupt.
To use the voltage monitor 2 interrupt to exit stop mode, set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).

Table 6.5 Procedure for Setting Bits Associated with Voltage Monitor 2 Interrupt

Step	When Using Digital Filter	When Using No Digital Filter
1	Set the VCA23 bit in the VCA2 register to 0 (internal reference voltage).	
2 (1)	Set the VCA24 bit in the VCA2 register to 0 (VCC voltage) or 1 (LCVCMP2 pin input voltage).	
3 (1)	Set the VCA27 bit in the VCA2 register to 1 (voltage detection 2 circuit enabled).	
4	Wait for td(E-A).	
5	Set the COMPSEL bit in the CMPA register to 1.	
6 (2)	Select the interrupt type by the IRQ2SEL in the CMPA register.	
7	Select the sampling clock of the digital filter by bits VW2F1 to VW2F0 in the VW2C register.	Set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).
8 (3)	Set the VW2C1 bit in the VW2C register to 0 (digital filter enabled).	–
9	Select the interrupt request timing by the VCAC2 bit in the VCAC register and the VW2C7 bit in the VW2C register.	
10	Set the VW2C2 bit in the VW2C register to 0.	
11	Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on).	–
12	Wait for 2 cycles of the sampling clock of the digital filter.	– (No wait time required)
13	Set the VW2C0 bit in the VW2C register to 1 (voltage monitor 2 interrupt enabled).	

Notes:
1. When the VW2C0 bit is set to 0, steps 1, 2, and 3 can be executed simultaneously (with one instruction).
2. When the VW2C0 bit is set to 0, steps 5 and 6 can be executed simultaneously (with one instruction).
3. When the VW2C0 bit is set to 0, steps 7 and 8 can be executed simultaneously (with one instruction).



VCA13: Bit in VCA1 register
VW2C1, VW2C2, VW2C3, VW2C7: Bits in VW2C register
VCAC2: Bit in VCAC register

The above applies under the following conditions:
- VCA27 bit in VCA2 register = 1 (voltage detection 2 circuit enabled)
- VW2C0 bit in VW2C register = 1 (voltage monitor 2 interrupt enabled)

Note:
1. When voltage monitor 0 reset is not used, set the power supply to VCC ≥ 1.8 V.

Figure 6.7 Operating Example of Voltage Monitor 2 Interrupt

7. I/O Ports

I/O ports are shared with the LCD ports for the LCD dive control waveform output and the I/O functions for the oscillation circuits, timers, and A/D converter. When these functions are not used, pins can be used as I/O ports.
Table 7.1 lists the Overview of I/O Ports.
The following explanation applies to the R8C/L33A Group and R8C/L3AB Group, which have the maximum number of I/O ports. For other groups, note that only the pins listed in Table 7.2 are provided.

Table 7.1 Overview of I/O Ports

Port	I/O Format	I/O Setting	Internal Pull-Up Resister (1)	Drive Capacity Switch (2)	Input Level Switch (3)
P0 to P4	I/O CMOS3 state	Set in 1-bit units.	Set in 1-bit units.	None	Set in 8-bit units.
P5_0 to P5_3	I/O CMOS3 state	Set in 1-bit units.	Set in 1-bit units.	None	Set in 4-bit units.
P6, P7	I/O CMOS3 state	Set in 1-bit units.	Set in 1-bit units.	None	Set in 8-bit units.
P10, P11	I/O CMOS3 state	Set in 1-bit units.	Set in 1-bit units.	Set in 1-bit units.	Set in 8-bit units.
P12_0 to P12_3	I/O CMOS3 state	Set in 1-bit units.	Set in 1-bit units.	None	Set in 4-bit units.
P13	I/O CMOS3 state	Set in 1-bit units.	Set in 1-bit units.	None	Set in 8-bit units.

Notes:
1. In input mode, whether an internal pull-up resistor is connected or not can be selected by registers P0PUR to and P13PUR.
2. Whether the drive capacity of the output transistor is set to low or high can be selected by registers P10DRR and P11DRR.
3. The input threshold value can be selected among three voltage levels (0.35 VCC, 0.50 VCC, and 0.70 VCC) using registers VLT0 and VLT1.

Table 7.2 Programmable I/O Ports Provided for Each Group

Programmable I/O Port	R8C/L35A Group R8C/L35B Group Total: 41 I/O pins								R8C/L36A Group R8C/L36B Group Total: 52 I/O pins								R8C/L38A Group R8C/L38B Group Total: 68 I/O pins								R8C/L3AA Group R8C/L3AB Group Total: 88 I/O pins							
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
P0	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√
P1	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	√	√	√	√	√	√	√	√	√	√	√	√
P2	√	√	√	√	–	–	–	–	√	√	√	√	–	–	–	–	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√
P3	–	–	–	–	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√
P4	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√
P5	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	√	√	√	√
P6	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√
P7	√	√	√	√	–	–	–	–	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√
P10	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	√	√	√	√	√	√	√	√
P11	–	–	–	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√
P12	–	–	–	–	√	√	√	√	–	–	–	–	√	√	√	√	–	–	–	–	√	√	√	√	–	–	–	–	√	√	√	√
P13	–	–	–	–	√	√	√	√	–	–	–	–	√	√	√	√	–	–	–	–	√	√	√	√	√	√	√	√	√	√	√	√

Note:
1. The symbol "√" indicates a programmable I/O port.

7.1 I/O Port Functions

The PDi_j (j = 0 to 7) bit in the PDi (i = 0 to 7, 10 to 13) register controls the input/output of ports P0 to P7 and P10 to P13. The Pi register consists of a port latch to retain output data and a circuit to read the pin status.
Figures 7.1 to 7.4 show the I/O Port Configurations, and Table 7.3 lists the I/O Port Functions.

Table 7.3 I/O Port Functions

Operation When Accessing Pi Register	Value of PDi_j Bit in PDi Register (1)	
	When PDi_j Bit is Set to 0 (Input Mode)	When PDi_j Bit is Set to 1 (Output Mode)
Read	Read the pin input level.	Read the port latch.
Write	Write to the port latch.	Write to the port latch. The value written to the port latch is output from the pin.

Note:
1. i = 0 to 7, 10 to 13; j = 0 to 7

7.2 Effect on Peripheral Functions

I/O ports function as I/O ports for peripheral functions (refer to **Tables 1.15 to 1.17 Pin Name Information by Pin Number**).
Table 7.4 lists the Setting of PDi_j Bit when Functioning as I/O Ports for Peripheral Functions (i = 0 to 7, 10 to 13; j = 0 to 7). Refer to the description of each function for information on how to set peripheral functions.

Table 7.4 Setting of PDi_j Bit when Functioning as I/O Ports for Peripheral Functions (i = 0 to 7, 10 to 13; j = 0 to 7)

I/O of Peripheral Function	PDi_j Bit Settings for Shared Pin Function
Input	Set this bit to 0 (input mode).
Output	This bit can be set to either 0 or 1 (output regardless of the port setting).

7.3 Pins Other than I/O Ports

Figure 7.5 shows the Pin Configuration.

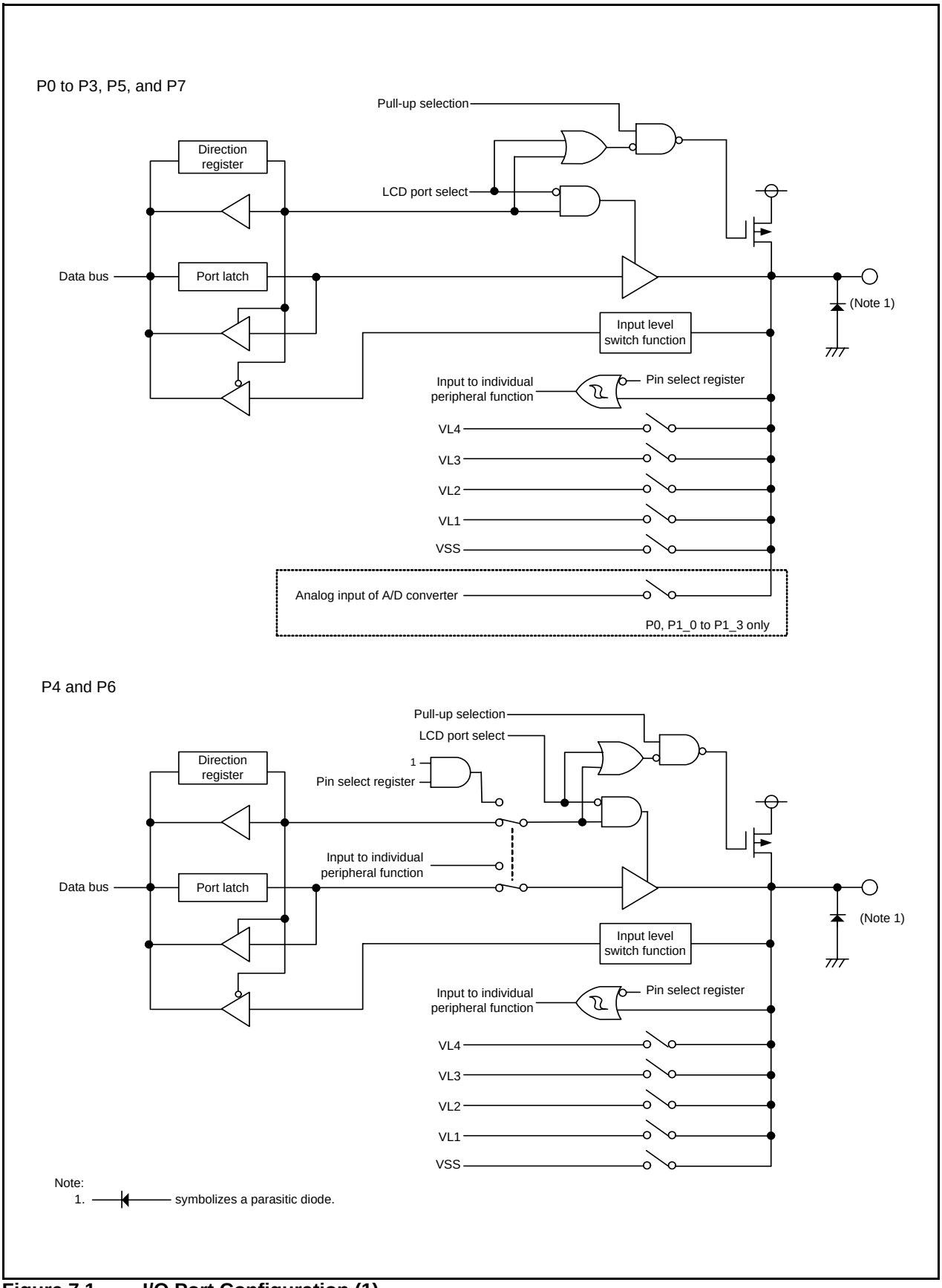
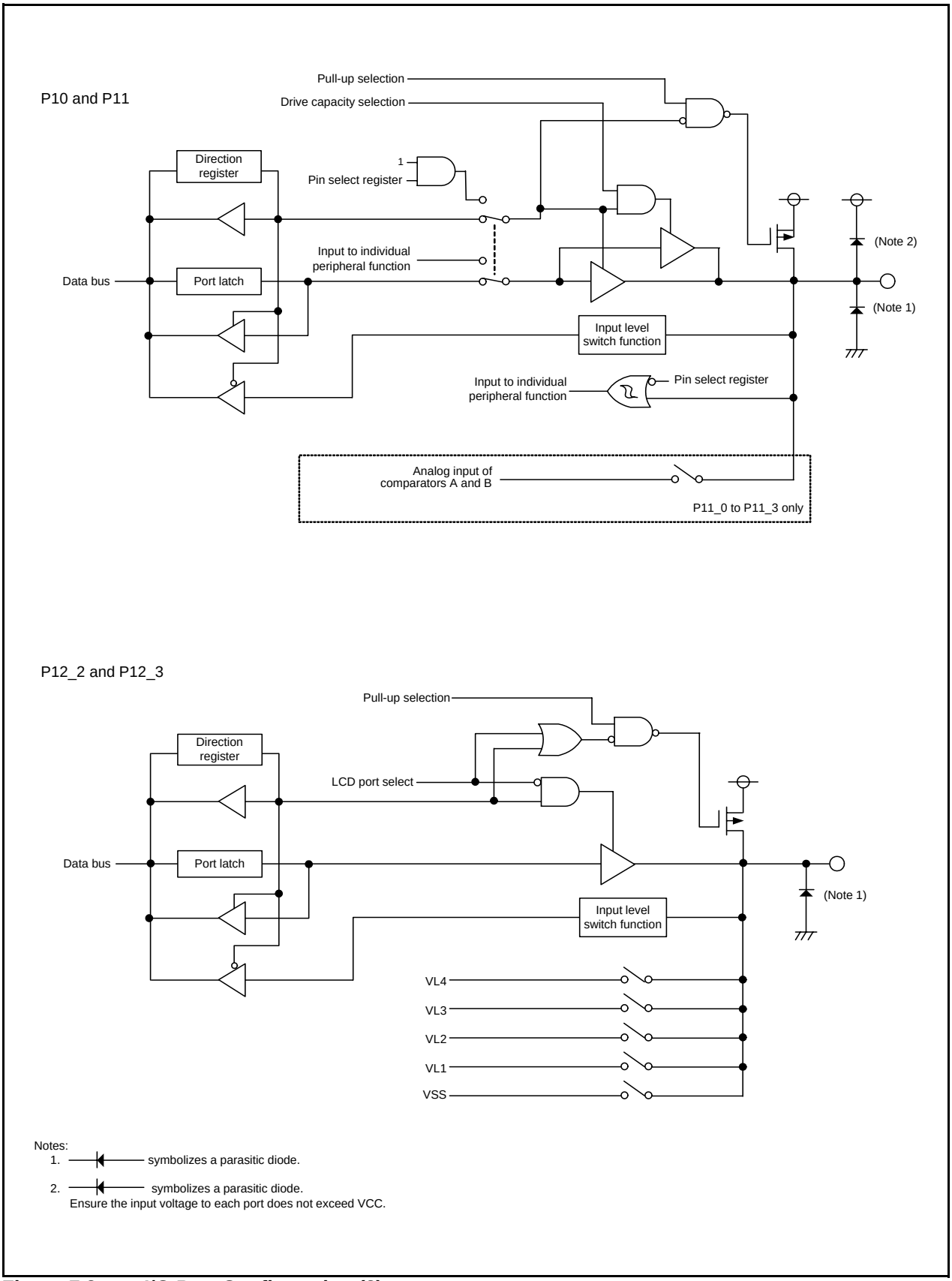


Figure 7.1 I/O Port Configuration (1)



Notes:
1. ⊣◄ symbolizes a parasitic diode.
2. ⊣◄ symbolizes a parasitic diode.
Ensure the input voltage to each port does not exceed VCC.

Figure 7.2 I/O Port Configuration (2)

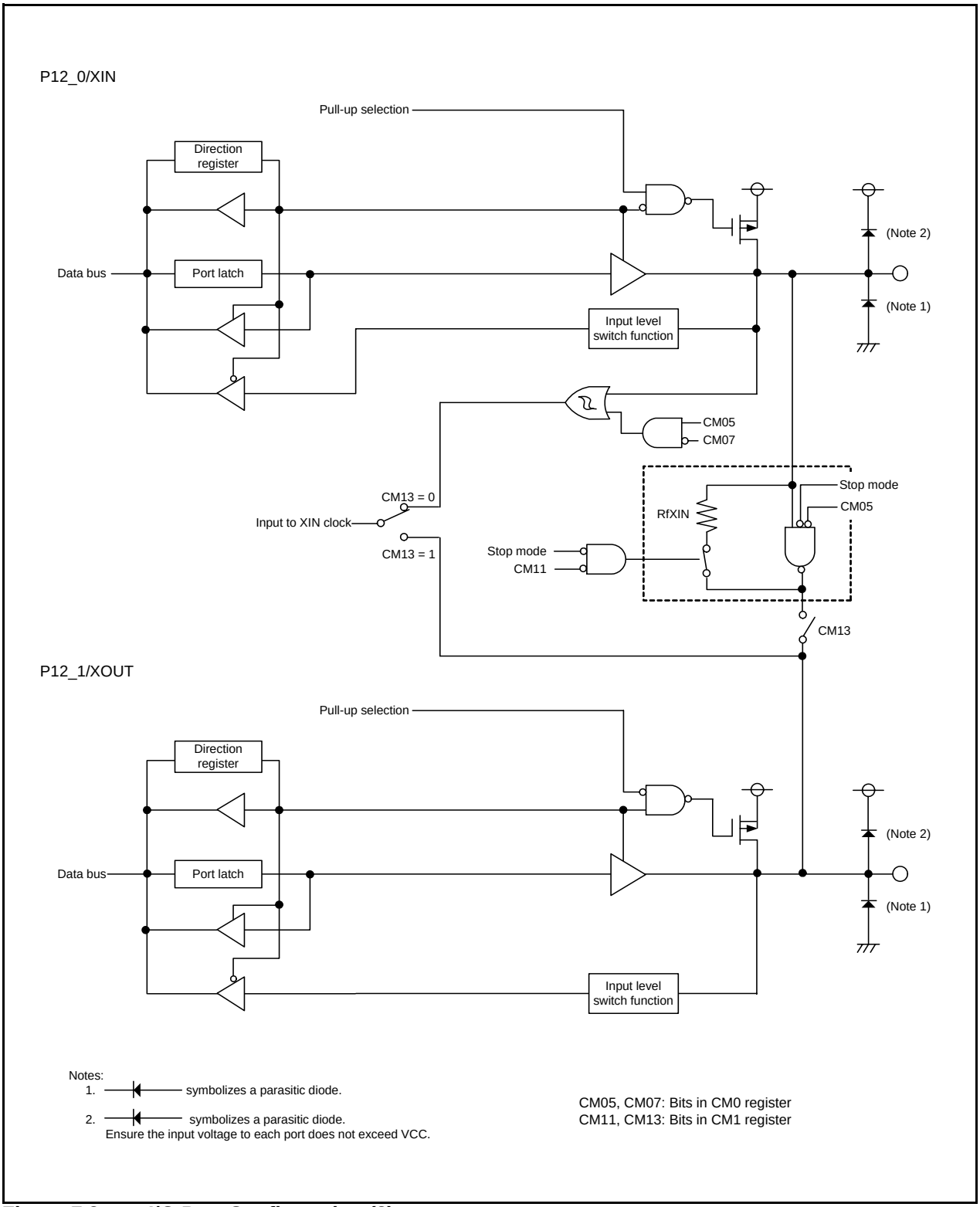
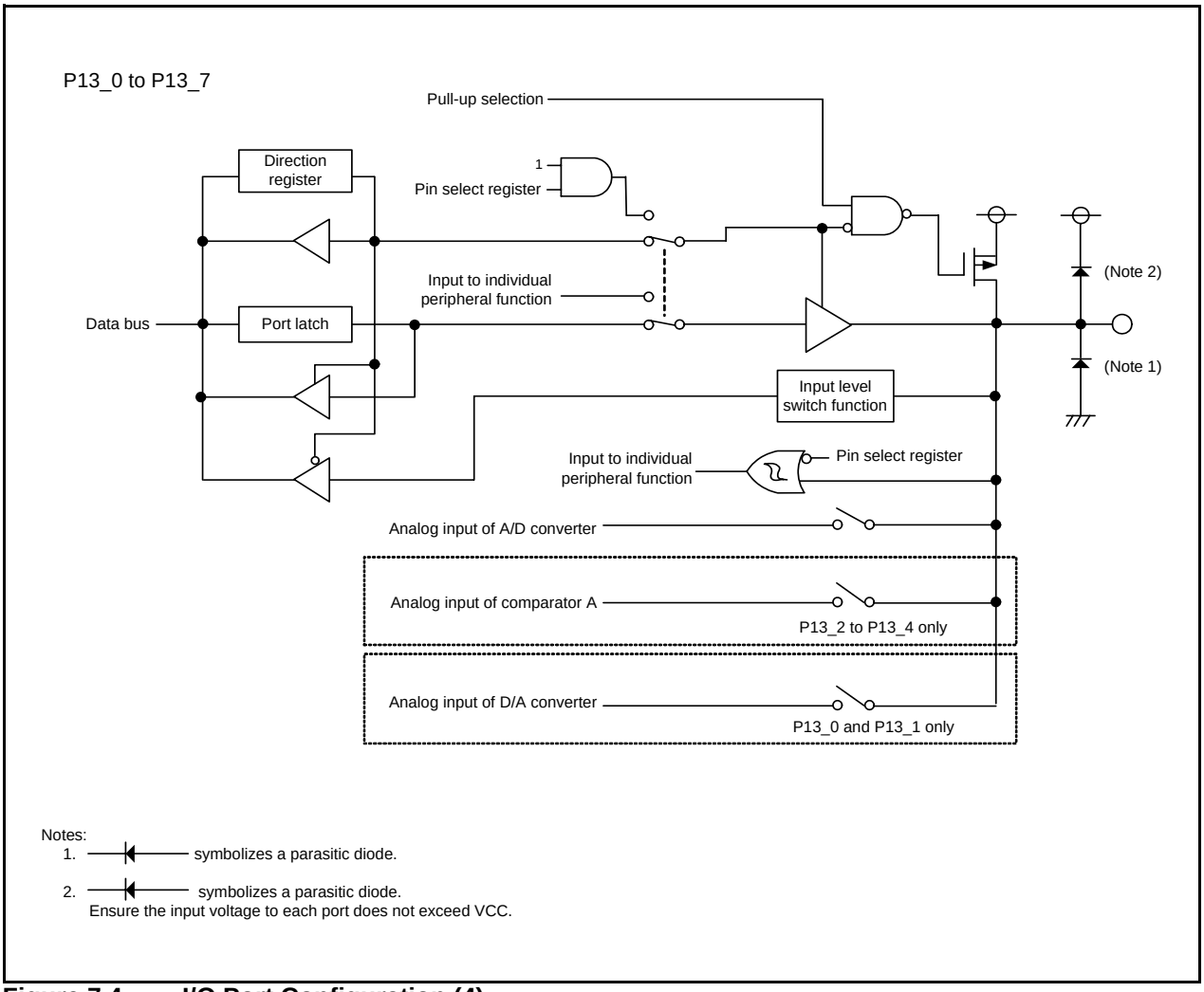


Figure 7.3 I/O Port Configuration (3)



Notes:
1. ⟵| symbolizes a parasitic diode.
2. ⟵| symbolizes a parasitic diode.
Ensure the input voltage to each port does not exceed VCC.

Figure 7.4 I/O Port Configuration (4)

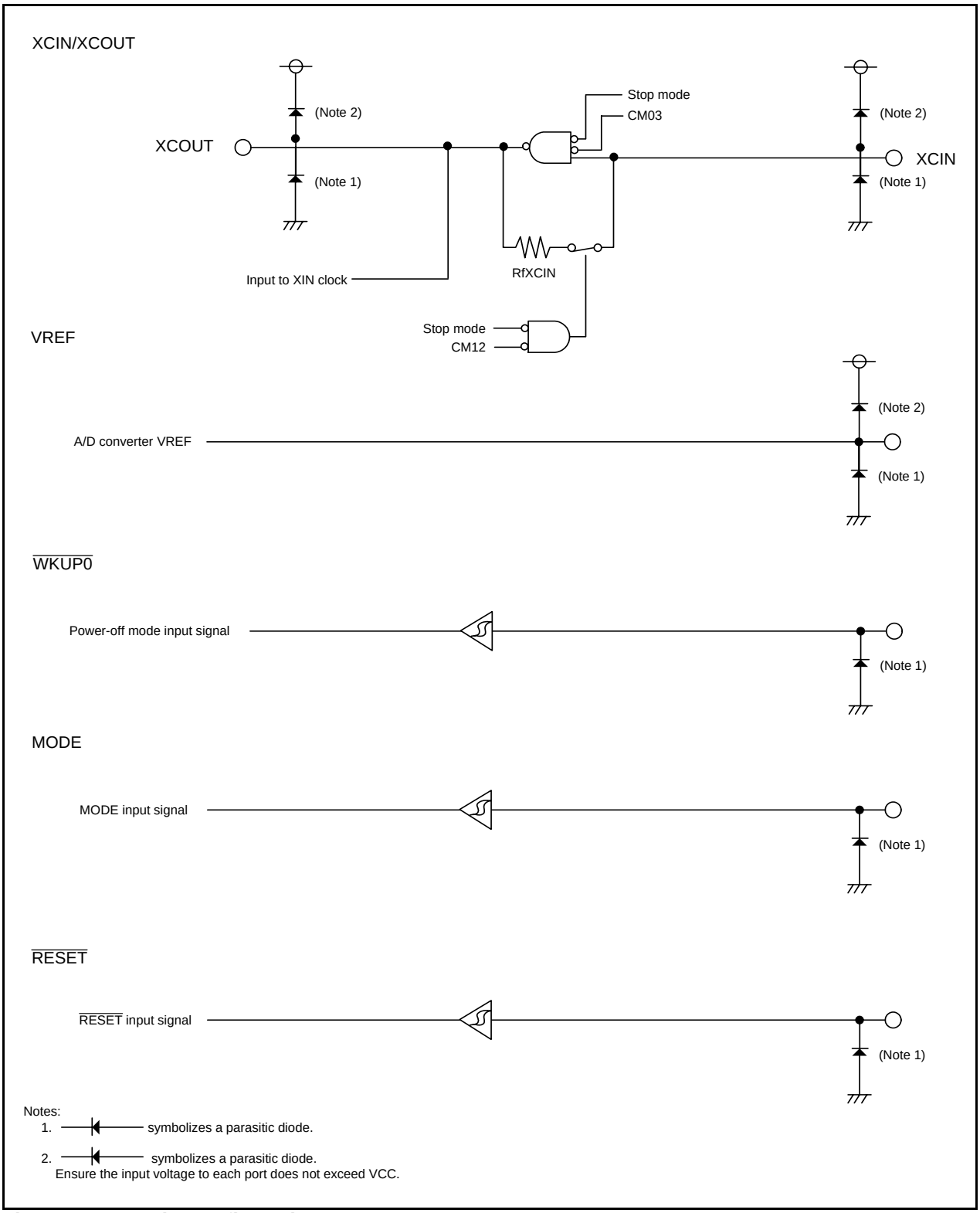


Figure 7.5 Pin Configuration

7.4 Registers

7.4.1 Port Pi Direction Register (PDi) (i = 0 to 7, 10 to 13)

Address 00E2h (PD0), 00E3h (PD1), 00E6h (PD2), 00E7h (PD3),
00EAh (PD4 (1)), 00EBh (PD5 (2)), 00EEh (PD6), 00EFh (PD7),
00F6h (PD10), 00F7h (PD11), 00FAh (PD12), 00FBh (PD13),

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PDi_7	PDi_6	PDi_5	PDi_4	PDi_3	PDi_2	PDi_1	PDi_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PDi_0	Port Pi_0 direction bit	0: Input mode (function as an input port) 1: Output mode (function as an output port)	R/W
b1	PDi_1	Port Pi_1 direction bit		R/W
b2	PDi_2	Port Pi_2 direction bit		R/W
b3	PDi_3	Port Pi_3 direction bit		R/W
b4	PDi_4	Port Pi_4 direction bit		R/W
b5	PDi_5	Port Pi_5 direction bit		R/W
b6	PDi_6	Port Pi_6 direction bit		R/W
b7	PDi_7	Port Pi_7 direction bit		R/W

Notes:
1. Bits PD5_4 to PD5_7 in the PD5 register are unavailable on this MCU.
   If it is necessary to set bits PD5_4 to PD5_7, set to 0. When read, the content is 0.
2. Bits PD12_4 to PD12_7 in the PD12 register are unavailable on this MCU.
   If it is necessary to set bits PD12_4 to PD12_7, set to 0. When read, the content is 0.

The PDi register selects whether I/O ports are used for input or output. Each bit in the PDi register corresponds to one port.

7.4.2 Port Pi Register (Pi) (i = 0 to 7, 10 to 13)

Address 00E0h (P0), 00E1h (P1), 00E4h (P2), 00E5h (P3),
00E8h (P4 (1)), 00E9h (P5 (2)), 00ECh(P6), 00EDh (P7),
00F4h (P10), 00F5h (P11), 00F8h (P12), 00F9h (P13),

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	Pi_7	Pi_6	Pi_5	Pi_4	Pi_3	Pi_2	Pi_1	Pi_0
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	Pi_0	Port Pi_0 bit	0: Low level 1: High level	R/W
b1	Pi_1	Port Pi_1 bit		R/W
b2	Pi_2	Port Pi_2 bit		R/W
b3	Pi_3	Port Pi_3 bit		R/W
b4	Pi_4	Port Pi_4 bit		R/W
b5	Pi_5	Port Pi_5 bit		R/W
b6	Pi_6	Port Pi_6 bit		R/W
b7	Pi_7	Port Pi_7 bit		R/W

Notes:
1. Bits PD5_4 to PD5_7 in the PD5 register are unavailable on this MCU.
   If it is necessary to set bits PD5_4 to PD5_7, set to 0. When read, the content is 0.
2. Bits PD12_4 to PD12_7 in the PD12 register are unavailable on this MCU.
   If it is necessary to set bits PD12_4 to PD12_7, set to 0. When read, the content is 0.

Data input and output to and from external devices are accomplished by reading and writing to the Pi register. The Pi register consists of a port latch to retain output data and a circuit to read the pin status. The value written in the port latch is output from the pin. Each bit in the Pi register corresponds to one port.

Pi_j Bit (i = 0 to 7, 10 to 13, j = 0 to 7) (Port Pi_0 Bit)

The pin level of any I/O port which is set to input mode can be read by reading the corresponding bit in this register. The pin level of any I/O port which is set to output mode can be controlled by writing to the corresponding bit in this register.

7.4.3 Timer RA Pin Select Register (TRASR)

Address 0180h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	TRAIOSEL1	TRAIOSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRAIOSEL0	TRAIO pin select bit	b1 b0 0 0: TRAIO pin not used 0 1: P11_4 assigned 1 0: $\overline{\text{INT4}}$ assigned 1 1: Do not set.	R/W
b1	TRAIOSEL1			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. To use hardware LIN, set 01b to bits TRAIOSEL1 to TRAIOSEL0.

To use the I/O pin for timer RA, set the TRASR register.
Set this register before setting the timer RA associated registers. Also, do not change the setting value of this register during timer RA operation.

7.4.4 Timer RB/RC Pin Select Register (TRBRCSR)

Address 0181h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRCTRGSEL1	TRCTRGSEL0	—	TRCCLKSEL0	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	—			
b4	TRCCLKSEL0	TRCCLK pin select bit	0: TRCCLK pin not used 1: TRCCLK pin used	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	TRCTRGSEL0	TRCTRG pin select bit	b7 b6 0 0: TRCTRG pin not used 0 1: P3_7 assigned 1 0: P4_3 assigned 1 1: P4_4 assigned	R/W
b7	TRCTRGSEL1			R/W

The register function for timer RB is not implemented.
To use the I/O pins for timer RC, set the TRBRCSR register.
Set this register before setting the timer RC associated registers. Also, do not change the setting value of the TRCCLKSEL0 bit during timer RC operation.

7.4.5 Timer RC Pin Select Register 0 (TRCPSR0)

Address 0182h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	TRCIOBSEL1	TRCIOBSEL0	—	—	—	TRCIOASEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCIOASEL0	TRCIOA pin select bit	0: TRCIOA pin not used 1: TRCIOA pin used	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—			
b4	TRCIOBSEL0	TRCIOB pin select bit	b5 b4 0 0: TRCIOB pin not used 0 1: P4_5 assigned 1 0: P4_6 assigned 1 1: P4_7 assigned	R/W
b5	TRCIOBSEL1			R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

The TRCPSR0 register selects whether to use the timer RC input. To use the I/O pins for timer RC, set this register.
Set the TRCPSR0 register before setting the timer RC associated registers. Also, do not change the setting value of this register during timer RC operation.

7.4.6 Timer RC Pin Select Register 1 (TRCPSR1)

Address 0183h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	TRCIODSEL0	—	—	—	TRCIOCSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCIOCSEL0	TRCIOC pin select bit (1)	0: TRCIOC pin not used 1: P4_6 assigned	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—			
b4	TRCIODSEL0	TRCIOD pin select bit (2)	0: TRCIOD pin not used 1: P4_7 assigned	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	—			
b7	—			

Notes:
1. When bits TRCIOBSEL1 to TRCIOBSEL0 in the TRCPSR0 register are set to 10b (P4_6 assigned as TRCIOB pin), P4_6 functions as the TRCIOB pin regardless of the content of the TRCIOCSEL0 bit.
2. When bits TRCIOBSEL1 to TRCIOBSEL0 in the TRCPSR0 register are set to 11b (P4_7 assigned as TRCIOB pin), P4_7 functions as the TRCIOB pin regardless of the content of the TRCIODSEL0 bit.

The TRCPSR1 register selects whether to use the timer RC input. To use the I/O pins for timer RC, set this register.
Set the TRCPSR1 register before setting the timer RC associated registers. Also, do not change the setting value of this register during timer RC operation.

7.4.7 Timer RD Pin Select Register 0 (TRDPSR0)

Address 0184h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRDIOD0SEL1	TRDIOD0SEL0	TRDIOC0SEL1	TRDIOC0SEL0	TRDIOB0SEL1	TRDIOB0SEL0	TRDIOA0SEL1	TRDIOA0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRDIOA0SEL0	TRDIOA0/TRDCLK pin select bit	b1 b0 0 0: TRDIOA0/TRDCLK pin not used 0 1: P6_0 assigned 1 0: P10_0 assigned 1 1: Do not set.	R/W
b1	TRDIOA0SEL1			R/W
b2	TRDIOB0SEL0	TRDIOB0 pin select bit	b3 b2 0 0: TRDIOB0 pin not used 0 1: P6_1 assigned 1 0: P10_1 assigned 1 1: Do not set.	R/W
b3	TRDIOB0SEL1			R/W
b4	TRDIOC0SEL0	TRDIOC0 pin select bit	b5 b4 0 0: TRDIOC0 pin not used 0 1: P6_2 assigned 1 0: P10_2 assigned 1 1: Do not set.	R/W
b5	TRDIOC0SEL1			R/W
b6	TRDIOD0SEL0	TRDIOD0 pin select bit	b7 b6 0 0: TRDIOC0 pin not used 0 1: P6_3 assigned 1 0: P10_3 assigned 1 1: Do not set.	R/W
b7	TRDIOD0SEL1			R/W

The TRDPSR0 register selects which pin is assigned as the timer RD input/output. To use the I/O pins for timer RD, set this register.
Set the TRDPSR0 register before setting the timer RD associated registers. Also, do not change the setting value of this register during timer RD operation.

7.4.8 Timer RD Pin Select Register 1 (TRDPSR1)

Address 0185h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRDIOD1SEL1	TRDIOD1SEL0	TRDIOC1SEL1	TRDIOC1SEL0	TRDIOB1SEL1	TRDIOB1SEL0	TRDIOA1SEL1	TRDIOA1SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRDIOA1SEL0	TRDIOA1 pin select bit	b1 b0 0 0: TRDIOA1 pin not used 0 1: P6_4 assigned 1 0: P10_4 assigned 1 1: Do not set.	R/W
b1	TRDIOA1SEL1			R/W
b2	TRDIOB1SEL0	TRDIOB1 pin select bit	b3 b2 0 0: TRDIOB1 pin not used 0 1: P6_5 assigned 1 0: P10_5 assigned 1 1: Do not set.	R/W
b3	TRDIOB1SEL1			R/W
b4	TRDIOC1SEL0	TRDIOC1 pin select bit	b5 b4 0 0: TRDIOC1 pin not used 0 1: P6_6 assigned 1 0: P10_6 assigned 1 1: Do not set.	R/W
b5	TRDIOC1SEL1			R/W
b6	TRDIOD1SEL0	TRDIOD1 pin select bit	b7 b6 0 0: TRDIOC1 pin not used 0 1: P6_7 assigned 1 0: P10_7 assigned 1 1: Do not set.	R/W
b7	TRDIOD1SEL1			R/W

The TRDPSR1 register selects which pin is assigned as the timer RD input/output. To use the I/O pins for timer RD, set this register.
Set the TRDPSR1 register before setting the timer RD associated registers. Also, do not change the setting value of this register during timer RD operation.

7.4.9 Timer RG Pin Select Register (TRGPSR)

Address 0187h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRGCLKBSEL0	TRGCLKASEL0	TRGIOBSEL0	TRGIOASEL0	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	—			
b4	TRGIOASEL0	TRGIOA pin select bit	0: TRGIOA pin not used 1: TRGIOA pin used	R/W
b5	TRGIOBSEL0	TRGIOB pin select bit	0: TRGIOB pin not used 1: TRGIOB pin used	R/W
b6	TRGCLKASEL0	TRGCLKA pin select bit	0: TRGCLKA pin not used 1: TRGCLKA pin used	R/W
b7	TRGCLKBSEL0	TRGCLKB pin select bit	0: TRGCLKB pin not used 1: TRGCLKB pin used	R/W

The TRGPSR register selects which pin is assigned as the timer RG input/output. To use the I/O pins for timer RG, set this register.
Set the TRGPSR register before setting the timer RG associated registers. Also, do not change the setting value of this register during timer RG operation.

7.4.10 UART0 Pin Select Register (U0SR)

Address 0188h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	CLK0SEL0	—	RXD0SEL0	RXD0SEL1	TXD0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TXD0SEL0	TXD0 pin select bit	0: TXD0 pin not used 1: TXD0 pin used	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	RXD0SEL0	RXD0 pin select bit	b3 b2 0 0: RXD0 pin not used 0 1: P13_2 assigned 1 0: P11_4 assigned 1 1: Do not set.	R/W
b3	RXD0SEL1			R/W
b4	CLK0SEL0	CLK0 pin select bit	0: CLK0 pin not used 1: CLK0 pin used	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	—			
b7	—			

The U0SR register selects which pin is assigned as the UART0 input/output. To use the I/O pins for UART0, set this register.
Set the U0SR register before setting the UART0 associated registers. Also, do not change the setting value of this register during UART0 operation.

7.4.11 UART1 Pin Select Register (U1SR)

Address 0189h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	CLK1SEL0	—	RXD1SEL0	—	TXD1SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TXD1SEL0	TXD1 pin select bit	0: TXD1 pin not used 1: TXD1 pin used	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	RXD1SEL0	RXD1 pin select bit	0: RXD1 pin not used 1: RXD1 pin used	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	CLK1SEL0	CLK1 pin select bit	0: CLK1 pin not used 1: CLK1 pin used	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	—			
b7	—			

The U1SR register selects which pin is assigned as the UART1 input/output. To use the I/O pins for UART1, set this register.
Set the U1SR register before setting the UART1 associated registers. Also, do not change the setting value of this register during UART1 operation.

7.4.12 UART2 Pin Select Register 0 (U2SR0)

Address 018Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	RXD2SEL1	RXD2SEL0	—	—	TXD2SEL1	TXD2SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TXD2SEL0	TXD2/SDA2 pin select bit	b1 b0 0 0: TXD2/SDA2 pin not used 0 1: P11_2 assigned 1 0: P11_1 assigned 1 1: Do not set.	R/W
b1	TXD2SEL1			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	RXD2SEL0	RXD2/SCL2 pin select bit	b5 b4 0 0: RXD2/SCL2 pin not used 0 1: P11_1 assigned 1 0: P11_2 assigned 1 1: Do not set.	R/W
b5	RXD2SEL1			R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

The U2SR0 register selects which pin is assigned as the UART2 input/output. To use the I/O pins for UART2, set this register.
Set the U2SR0 register before setting the UART2 associated registers. Also, do not change the setting value of this register during UART2 operation.

7.4.13 UART2 Pin Select Register 1 (U2SR1)

Address 018Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	CTS2SEL0	—	—	—	CLK2SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CLK2SEL0	CLK2 pin select bit	0: CLK2 pin not used 1: CLK2 pin used	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—			
b4	CTS2SEL0	$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$ pin select bit	0: $\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$ pin not used 0: $\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$ pin used	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	—			
b7	—			

The U2SR1 register selects which pin is assigned as the UART2 input/output. To use the I/O pins for UART2, set this register.
Set the U2SR1 register before setting the UART2 associated registers. Also, do not change the setting value of this register during UART2 operation.

7.4.14 SSU/IIC Pin Select Register (SSUIICSR)

Address 018Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	IICSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IICSEL	SSU/I^{2}C bus switch bit	0: SSU function selected 1: I^{2}C bus function selected	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

7.4.15 Key Input Pin Select Register (KISR)

Address 018Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	KI7SEL0	KI6SEL0	KISEL0	KI4SEL0	KI3SEL0	KI2SEL0	KI1SEL0	KI0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	KI0SEL0	$\overline{KI0}$ pin select bit	0: P2_0 assigned 1: P10_0 assigned	R/W
b1	KI1SEL0	$\overline{KI1}$ pin select bit	0: P2_1 assigned 1: P10_1 assigned	R/W
b2	KI2SEL0	$\overline{KI2}$ pin select bit	0: P2_2 assigned 1: P10_2 assigned	R/W
b3	KI3SEL0	$\overline{KI3}$ pin select bit	0: P2_3 assigned 1: P10_3 assigned	R/W
b4	KI4SEL0	$\overline{KI4}$ pin select bit	0: P2_4 assigned 1: P10_4 assigned	R/W
b5	KI5SEL0	$\overline{KI5}$ pin select bit	0: P2_5 assigned 1: P10_5 assigned	R/W
b6	KI6SEL0	$\overline{KI6}$ pin select bit	0: P2_6 assigned 1: P10_6 assigned	R/W
b7	KI7SEL0	$\overline{KI7}$ pin select bit	0: P2_7 assigned 1: P10_7 assigned	R/W

The KISR register selects which pin is assigned as the $\overline{KIi}$ (i = 1 to 7) input. To use the $\overline{KIi}$, set this register. Set the KISR register before setting the $\overline{KIi}$ associated registers. Also, do not change the setting values in this register during $\overline{KIi}$ operation.

7.4.16 INT Interrupt Input Pin Select Register (INTSR)

Address 018Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT7SEL0	INT6SEL0	INT5SEL0	INT4SEL0	INT3SEL0	INT2SEL0	INT1SEL0	INT0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0SEL0	$\overline{\text{INT0}}$ pin select bit	0: P3_0 assigned 1: P11_0 assigned	R/W
b1	INT1SEL0	$\overline{\text{INT1}}$ pin select bit	0: P3_1 assigned 1: P11_1 assigned	R/W
b2	INT2SEL0	$\overline{\text{INT2}}$ pin select bit	0: P3_2 assigned 1: P11_2 assigned	R/W
b3	INT3SEL0	$\overline{\text{INT3}}$ pin select bit	0: P3_3 assigned 1: P11_3 assigned	R/W
b4	INT4SEL0	$\overline{\text{INT4}}$ pin select bit	0: P3_4 assigned 1: P11_4 assigned	R/W
b5	INT5SEL0	$\overline{\text{INT5}}$ pin select bit	0: P3_5 assigned 1: P11_5 assigned	R/W
b6	INT6SEL0	$\overline{\text{INT6}}$ pin select bit	0: P3_6 assigned 1: P11_6 assigned	R/W
b7	INT7SEL0	$\overline{\text{INT7}}$ pin select bit	0: P3_7 assigned 1: P11_7 assigned	R/W

The INTSR register selects which pin is assigned as the $\overline{\text{INTi}}$ (i = 1 to 7) input. To use the $\overline{\text{INTi}}$, set this register. Set the INTSR register before setting the $\overline{\text{INTi}}$ associated registers. Also, do not change the setting values in this register during $\overline{\text{INTi}}$ operation.

7.4.17 Port Pi Pull-Up Control Register (PiPUR) (i = 0 to 7)

Address 01E0h (P0PUR), 01E1h (P1PUR), 01E2h (P2PUR), 01E3h (P3PUR),
01E4h (P4PUR), 01E5h (P5PUR), 01E6h (P6PUR), 01E7h (P7PUR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PUi7	PUi6	PUi5	PUi4	PUi3	PUi2	PUi1	PUi0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PUi0	Port Pi_0 pull-up	0: Not pulled up 1: Pulled up (1)	R/W
b1	PUi1	Port Pi_1 pull-up		R/W
b2	PUi2	Port Pi_2 pull-up		R/W
b3	PUi3	Port Pi_3 pull-up		R/W
b4	PUi4	Port Pi_4 pull-up		R/W
b5	PUi5	Port Pi_5 pull-up		R/W
b6	PUi6	Port Pi_6 pull-up		R/W
b7	PUi7	Port Pi_7 pull-up		R/W

Note:
1. When this bit is set to 1 (pulled up), the pin whose port direction bit is set to 0 (input mode) is pulled up.

For ports set to output as I/O pins for peripheral functions, the setting values of the PiPUR register are invalid and no pull-up resistor is connected.

7.4.18 Port Pj Pull-Up Control Register (PjPUR) (j = 10 to 13)

Address 01EAh (P10PUR), 01EBh (P11PUR), 01ECh (P12PUR), 01EDh (P13PUR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PUj7	PUj6	PUj5	PUj4	PUj3	PUi2	PUj1	PUj0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PUj0	Port Pj_0 pull-up	0: Not pulled up	R/W
b1	PUj1	Port Pj_1 pull-up	1: Pulled up (1)	R/W
b2	PUj2	Port Pj_2 pull-up		R/W
b3	PUj3	Port Pj_3 pull-up		R/W
b4	PUj4	Port Pj_4 pull-up		R/W
b5	PUj5	Port Pj_5 pull-up		R/W
b6	PUj6	Port Pj_6 pull-up		R/W
b7	PUj7	Port Pj_7 pull-up		R/W

Note:
1. When this bit is set to 1 (pulled up), the pin whose port direction bit is set to 0 (input mode) is pulled up.

For ports set to output as I/O pins for peripheral functions, the setting values of the PjPUR register are invalid and no pull-up resistor is connected.

7.4.19 Port P10 Drive Capacity Control Register (P10DRR)

Address 01F0h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	P10DRR7	P10DRR6	P10DRR5	P10DRR4	P10DRR3	P10DRR2	P10DRR1	P10DRR0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	P10DRR0	P10_0 drive capacity	0: Low	R/W
b1	P10DRR1	P10_1 drive capacity	1: High (1)	R/W
b2	P10DRR2	P10_2 drive capacity		R/W
b3	P10DRR3	P10_3 drive capacity		R/W
b4	P10DRR4	P10_4 drive capacity		R/W
b5	P10DRR5	P10_5 drive capacity		R/W
b6	P10DRR6	P10_6 drive capacity		R/W
b7	P10DRR7	P10_7 drive capacity		R/W

Note:
1. Both high-level output and low-level output are set to high drive capacity.

The P10DRR register selects whether the drive capacity of the P10 output transistor is set to low or high.
The P10DRRi bit (i = 0 to 7) is used to select whether the drive capacity of the output transistor is set to low or high for each pin.

7.4.20 Port P11 Drive Capacity Control Register (P11DRR)

Address 01F1h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	P11DRR7	P11DRR6	P11DRR5	P11DRR4	P11DRR3	P11DRR2	P11DRR1	P11DRR0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	P11DRR0	P11_0 drive capacity	0: Low 1: High (1)	R/W
b1	P11DRR1	P11_1 drive capacity		R/W
b2	P11DRR2	P11_2 drive capacity		R/W
b3	P11DRR3	P11_3 drive capacity		R/W
b4	P11DRR4	P11_4 drive capacity		R/W
b5	P11DRR5	P11_5 drive capacity		R/W
b6	P11DRR6	P11_6 drive capacity		R/W
b7	P11DRR7	P11_7 drive capacity		R/W

Note:
1. Both high-level output and low-level output are set to high drive capacity.

The P11DRR register selects whether the drive capacity of the P11 output transistor is set to low or high. The P11DRRi bit (i = 0 to 7) is used to select whether the drive capacity of the output transistor is set to low or high for each pin.

7.4.21 Input Threshold Control Register 0 (VLT0)

Address 01F5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VLT07	VLT06	VLT05	VLT04	VLT03	VLT02	VLT01	VLT00
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	VLT00	P0 input level select bit	b1 b0 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b1	VLT01			R/W
b2	VLT02	P1 input level select bit	b3 b2 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b3	VLT03			R/W
b4	VLT04	P2 input level select bit	b5 b4 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b5	VLT05			R/W
b6	VLT06	P3 input level select bit	b7 b6 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b7	VLT07			R/W

The VLT0 register selects the voltage level of the input threshold values for ports P0 to P3. Bits VLT00 to VLT07 are used to select the input threshold values among three voltage levels (0.35 VCC, 0.50 VCC, and 0.70 VCC).

7.4.22 Input Threshold Control Register 1 (VLT1)

Address 01F6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VLT17	VLT16	VLT15	VLT14	VLT13	VLT12	VLT11	VLT10
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	VLT10	P4 input level select bit	b1 b0 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b1	VLT11			R/W
b2	VLT12	P5_0 and P5_3 input level select bit	b3 b2 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b3	VLT13			R/W
b4	VLT14	P6 input level select bit	b5 b4 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b5	VLT15			R/W
b6	VLT16	P7 input level select bit	b7 b6 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b7	VLT17			R/W

The VLT1 register selects the voltage level of the input threshold values for ports P4 to P7. Bits VLT10 to VLT17 are used to select the input threshold values among three voltage levels (0.35 VCC, 0.50 VCC, and 0.70 VCC).

7.4.23 Input Threshold Control Register 2 (VLT2)

Address 01F7h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VLT17	VLT16	VLT15	VLT14	VLT13	VLT12	VLT11	VLT10
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	VLT20	P10 input level select bit	b1 b0 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b1	VLT21			R/W
b2	VLT22	P11 input level select bit	b3 b2 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b3	VLT23			R/W
b4	VLT24	P12_0 to P12_3 input level select bit	b5 b4 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b5	VLT25			R/W
b6	VLT26	P13 input level select bit	b7 b6 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b7	VLT27			R/W

The VLT2 register selects the voltage level of the input threshold values for ports P10 to P13. Bits VLT20 to VLT27 are used to select the input threshold values among three voltage levels (0.35 VCC, 0.50 VCC, and 0.70 VCC).

7.5 Port Settings

Tables 7.5 to 7.23 list the port settings.

Table 7.5 Port P0

Pin	Register	PD0	LSE0	ADINSEL					—	Function
	Bit	PD0_i	LSEi	CH			ADGSEL			
				2	1	0	1	0		
Port P0_0 SEG0 AN4	i = 0	0	0	X	X	X	X	X		Input port (1)
		1	0	X	X	X	X	X		Output port
		X	1	X	X	X	X	X		LCD drive control output (SEG0)
		0	0	1	0	0	0	0		A/D converter input (AN4) (1)
Port P0_1 SEG1 AN5	i = 1	0	0	X	X	X	X	X		Input port (1)
		1	0	X	X	X	X	X		Output port
		X	1	X	X	X	X	X		LCD drive control output (SEG1)
		0	0	1	0	1	0	0		A/D converter input (AN5) (1)
Port P0_2 SEG2 AN6	i = 2	0	0	X	X	X	X	X		Input port (1)
		1	0	X	X	X	X	X		Output port
		X	1	X	X	X	X	X		LCD drive control output (SEG2)
		0	0	1	1	0	0	0		A/D converter input (AN6) (1)
Port P0_3 SEG3 AN7	i = 3	0	0	X	X	X	X	X		Input port (1)
		1	0	X	X	X	X	X		Output port
		X	1	X	X	X	X	X		LCD drive control output (SEG3)
		0	0	1	1	1	0	0		A/D converter input (AN7) (1)
Port P0_4 SEG4 AN8	i = 4	0	0	X	X	X	X	X		Input port (1)
		1	0	X	X	X	X	X		Output port
		X	1	X	X	X	X	X		LCD drive control output (SEG4)
		0	0	0	0	0	0	1		A/D converter input (AN8) (1)
Port P0_5 SEG5 AN9	i = 5	0	0	X	X	X	X	X		Input port (1)
		1	0	X	X	X	X	X		Output port
		X	1	X	X	X	X	X		LCD drive control output (SEG5)
		0	0	0	0	1	0	1		A/D converter input (AN9) (1)
Port P0_6 SEG6 AN10	i = 6	0	0	X	X	X	X	X		Input port (1)
		1	0	X	X	X	X	X		Output port
		X	1	X	X	X	X	X		LCD drive control output (SEG6)
		0	0	0	1	0	0	1		A/D converter input (AN10) (1)
Port P0_7 SEG7 AN11	i = 7	0	0	X	X	X	X	X		Input port (1)
		1	0	X	X	X	X	X		Output port
		X	1	X	X	X	X	X		LCD drive control output (SEG7)
		0	0	0	1	1	0	1		A/D converter input (AN11) (1)

X: 0 or 1

Note:

1. Pulled up by setting the corresponding bit in the P0PUR register to 1.

Table 7.6 Port P1

Pin	Register	PD1	LSE1	ADINSEL					—	Function
	Bit	PD1_i	LSEi+8	CH			ADGSEL			
				2	1	0	1	0		
Port P1_0 SEG8 AN12	i = 0	0	0	X	X	X	X	X		Input port (1)
		1	0	X	X	X	X	X		Output port
		X	1	X	X	X	X	X		LCD drive control output (SEG8)
		0	0	1	0	0	0	1		A/D converter input (AN12) (1)
Port P1_1 SEG9 AN13	i = 1	0	0	X	X	X	X	X		Input port (1)
		1	0	X	X	X	X	X		Output port
		X	1	X	X	X	X	X		LCD drive control output (SEG9)
		0	0	1	0	1	0	1		A/D converter input (AN13) (1)
Port P1_2 SEG10 AN14	i = 2	0	0	X	X	X	X	X		Input port (1)
		1	0	X	X	X	X	X		Output port
		X	1	X	X	X	X	X		LCD drive control output (SEG10)
		0	0	1	1	0	0	1		A/D converter input (AN14) (1)
Port P1_3 SEG11 AN15	i = 3	0	0	X	X	X	X	X		Input port (1)
		1	0	X	X	X	X	X		Output port
		X	1	X	X	X	X	X		LCD drive control output (SEG11)
		0	0	1	1	1	0	1		A/D converter input (AN15) (1)
Port P1_4 SEG12	i = 4	0	0							Input port (1)
		1	0							Output port
		X	1							LCD drive control output (SEG12)
Port P1_5 SEG13	i = 5	0	0							Input port (1)
		1	0							Output port
		X	1							LCD drive control output (SEG13)
Port P1_6 SEG14	i = 6	0	0							Input port (1)
		1	0							Output port
		X	1							LCD drive control output (SEG14)
Port P1_7 SEG15	i = 7	0	0							Input port (1)
		1	0							Output port
		X	1							LCD drive control output (SEG15)

X: 0 or 1

Note:

1. Pulled up by setting the corresponding bit in the P1PUR register to 1.

Table 7.7 Port P2

Pin	Register	PD2	LSE2	KISR	KIEN	KIEN1	—	Function
	Bit	PD2_i	LSEi+16	KIiSEL0	KIiEN	KIiEN		
Port P2_0 SEG16 $\overline{KI0}$	i = 0	0	0	X	X	—		Input port (1)
		1	0	X	X	—		Output port
		X	1	X	X	—		LCD drive control output (SEG16)
		0	0	0	1	—		$\overline{KI0}$ input (1)
Port P2_1 SEG17 $\overline{KI1}$	i = 1	0	0	X	X	—		Input port (1)
		1	0	X	X	—		Output port
		X	1	X	X	—		LCD drive control output (SEG17)
		0	0	0	1	—		$\overline{KI1}$ input (1)
Port P2_2 SEG18 $\overline{KI2}$	i = 2	0	0	X	X	—		Input port (1)
		1	0	X	X	—		Output port
		X	1	X	X	—		LCD drive control output (SEG18)
		0	0	0	1	—		$\overline{KI2}$ input (1)
Port P2_3 SEG19 $\overline{KI3}$	i = 3	0	0	X	X	—		Input port (1)
		1	0	X	X	—		Output port
		X	1	X	X	—		LCD drive control output (SEG19)
		0	0	0	1	—		$\overline{KI3}$ input (1)
Port P2_4 SEG20 $\overline{KI4}$	i = 4	0	0	X	—	X		Input port (1)
		1	0	X	—	X		Output port
		X	1	X	—	X		LCD drive control output (SEG20)
		0	0	0	—	1		$\overline{KI4}$ input (1)
Port P2_5 SEG21 $\overline{KI5}$	i = 5	0	0	X	—	X		Input port (1)
		1	0	X	—	X		Output port
		X	1	X	—	X		LCD drive control output (SEG21)
		0	0	0	—	1		$\overline{KI5}$ input (1)
Port P2_6 SEG22 $\overline{KI6}$	i = 6	0	0	X	—	X		Input port (1)
		1	0	X	—	X		Output port
		X	1	X	—	X		LCD drive control output (SEG22)
		0	0	0	—	1		$\overline{KI6}$ input (1)
Port P2_7 SEG23 $\overline{KI7}$	i = 7	0	0	X	—	X		Input port (1)
		1	0	X	—	X		Output port
		X	1	X	—	X		LCD drive control output (SEG23)
		0	0	0	—	1		$\overline{KI7}$ input (1)

X: 0 or 1; —: No change in outcome

Note:

1. Pulled up by setting the corresponding bit in the P2PUR register to 1.

Table 7.8 Port P3

Pin	Register	PD3	LSE3	INTSR	INTEN	INTEN1	ADMOD		TRBRCSR		TRCMR	TRCCR2		Function
	Bit	PD3_i	LSEi+24	INTiSEL0	INTiEN	INTiEN	ADCAP1	ADCAP0	TRCTRGSEL1	TRCTRGSEL0	PWM2	TCEG1	TCEG0	
Port P3_0 SEG24 $\overline{\text{INT0}}$	i = 0	0	0	X	X	—	—	—	—	—	—	—	—	Input port (1)
		1	0	X	X	—	—	—	—	—	—	—	—	Output port
		X	1	X	X	—		—		—	—		—	LCD drive control output (SEG24)
		0	0	0	1	—	—	—	—	—	—	—	—	$\overline{\text{INT0}}$ input (1)
Port P3_1 SEG25 $\overline{\text{INT1}}$	i = 1	0	0	X	X	—	—	—	—	—	—	—	—	Input port (1)
		1	0	X	X	—	—	—	—	—	—	—	—	Output port
		X	1	X	X	—	—	—	—	—	—	—	—	LCD drive control output (SEG25)
		0	0	0	1	—	—	—	—	—	—	—	—	$\overline{\text{INT1}}$ input (1)
Port P3_2 SEG26 $\overline{\text{INT2}}$	i = 2	0	0	X	X	—	—	—	—	—	—	—	—	Input port (1)
		1	0	X	X	—	—	—	—	—	—	—	—	Output port
		X	1	X	X	—		—		—	—		—	LCD drive control output (SEG26)
		0	0	0	1	—	—	—	—	—	—	—	—	$\overline{\text{INT2}}$ input (1)
Port P3_3 SEG27 $\overline{\text{INT3}}$	i = 3	0	0	X	X	—	—	—	—	—	—	—	—	Input port (1)
		1	0	X	X	—	—	—	—	—	—	—	—	Output port
		X	1	X	X	—	—	—	—	—	—	—	—	LCD drive control output (SEG27)
		0	0	0	1	—	—	—	—	—	—	—	—	$\overline{\text{INT3}}$ input (1)
Port P3_4 SEG28 $\overline{\text{INT4}}$	i = 4	0	0	X	—	X	—	—	—	—	—	—	—	Input port (1)
		1	0	X	—	X	—	—	—	—	—	—	—	Output port
		X	1	X	—	X		—		—	—		—	LCD drive control output (SEG28)
		0	0	0	—	1	—	—	—	—	—	—	—	$\overline{\text{INT4}}$ input (1)
Port P3_5 SEG29 $\overline{\text{INT5}}$	i = 5	0	0	X	—	X	—	—	—	—	—	—	—	Input port (1)
		1	0	X	—	X	—	—	—	—	—	—	—	Output port
		X	1	X	—	X	—	—	—	—	—	—	—	LCD drive control output (SEG29)
		0	0	0	—	1	—	—	—	—	—	—	—	$\overline{\text{INT5}}$ input (1)
Port P3_6 SEG30 $\overline{\text{INT6}}$	i = 6	0	0	X	—	X	—	—	—	—	—	—	—	Input port (1)
		1	0	X	—	X	—	—	—	—	—	—	—	Output port
		X	1	X	—	X		—		—	—		—	LCD drive control output (SEG30)
		0	0	0	—	1	—	—	—	—	—	—	—	$\overline{\text{INT6}}$ input (1)
Port P3_7 SEG31 $\overline{\text{INT7}}$ $\overline{\text{ADTRG}}$ TRCTRG	i = 7	0	0	X	—	X	X	X	X	X	X	X	X	Input port (1)
		1	0	X	—	X	X	X	X	X	X	X	X	Output port
		X	1	X	—	1	X	X	X	X	X	X	X	LCD drive control output (SEG31)
		0	0	0	—	1	X	X	X	X	X	X	X	$\overline{\text{INT7}}$ input (1)
		0	0	0	—	1	1	1	X	X	X	X	X	$\overline{\text{ADTRG}}$ input (1)
		0	0	X	— —	X	X	X	0	1	0	0 1	1 X	PWM2 mode TRCTRG input (1)

X: 0 or 1; —: No change in outcome

Note:

1. Pulled up by setting the corresponding bit in the P3PUR register to 1.

Table 7.9 Ports P4_0 to 4_2

Pin	Register	PD4	LSE4	U1SR			U1MR				—	Function
	Bit	PD4_i	LSEi+32	CLK1SEL0	RXD1SEL0	TXD1SEL0	SMD2	SMD1	SMD0	CKDIR		
Port P4_0 SEG32 TXD1	i = 0	0	0	—	—	0	X	X	X	X		Input port (1)
		0	0	—	—	0	X	X	X	X		Output port
		X	1	—	—	0	X	X	X	X		LCD drive control output (SEG32)
		0	0	—	—	1	0	0	1	X		TXD1 output (2)
							1	0	X			
							1	1	0			
Port P4_1 SEG33 RXD1	i = 1	0	0	—	X	—	X	X	X	X		Input port (1)
		0	0	—	X	—	X	X	X	X		Output port
		X	1	—	X	—	X	X	X	X		LCD drive control output (SEG33)
		0	0	—	1	—	X	X	X	X		RXD1 input (1)
Port P4_2 SEG34 CLK1	i = 2	0	0	0	—	—	X	X	X	X		Input port (1)
		0	0	0	—	—	X	X	X	X		Output port
		X	1	0	—	—	X	X	X	X		LCD drive control output (SEG34)
		0	0	1	—	—	X	X	X	1		CLK1 (external clock) input (1)
		X	0	1	—	—	0	0	1	0		CLK1 (internal clock) output (2)

X: 0 or 1; —: No change in outcome

Notes:
1. Pulled up by setting the corresponding bit in the P4PUR register to 1.
2. N-channel open-drain output by setting the MCH bit in the U1C0 register to 1.

Table 7.10 Ports P4_3 and 4_4

Pin	Register	PD4	LSE4	TRBRCSR			TRCCR1			TRCMR	TRCCR2		—	Function
	Bit	PD4_i	LSE35	TRCTRG SEL1	TRCTRG SEL0	TRCCLK SEL0	TCK2	TCK1	TCK0	PWM2	TCEG1	TCEG0		
Port P4_3 SEG35 TRCCLK TRCTRG	i = 3	0	0	X	X	X	X	X	X	X	X	X		Input port (1)
		1	0	X	X	X	X	X	X	X	X	X		Output port
		X	1	X	X	X	X	X	X	X	X	X		LCD drive control output (SEG35)
		0	X	X	X	1	1	0	1	X	X	X		TRCCLK input (1)
		0	0	1	0	X	X	X	X	0	0	1		PWM2 mode TRCTRG input (1)
											1	X		

Pin	Register	PD4	LSE4	TRBRCSR		TRCPSR0	TRCOER	TRCMR	TRCIOR0			TRCCR2		Function
	Bit	PD4_i	LSE36	TRCTRG SEL1	TRCTRG SEL0	TRCIOA SEL0	EA	PWM2	IOA2	IOA1	IOA0	TCEG1	TCEG 0	
Port P4_4 SEG36 TRCIOA TRCTRG	i = 4	0	0	X	X	0	X	X	X	X	X	X	X	Input port (1)
		1	0	X	X	0	X	X	X	X	X	X	X	Output port
		X	1	X	X	0	X	X	X	X	X	X	X	LCD drive control output (SEG36)
		X	0	X	X	1	0	1	0	0	1	X	X	Timer waveform (output compare function)
									0	1	X	X	X	
		0	0	X	X	1	X	1	1	X	X	X	X	Timer mode (input capture function) (1)
		0	0	1	1	X	X	0	X	X	X	0	1	PWM2 mode TRCTRG input (1)
												1	X	

X: 0 or 1; —: No change in outcome
Note:
1. Pulled up by setting the corresponding bit in the P4PUR register to 1.

Table 7.11 Ports P4_5 to 4_7

Pin	Register	PD4	LSE4	TRCPSR0		—	TRCOER	TRCMR		TRCIOR0			—	Function
	Bit	PD4_i	LSE37	TRCIOBSEL			EB	PWM2	PWMB	IOB				
				1	0					2	1	0		
Port P4_5 SEG37 TRCIOB	i = 5	0	0	Other than 01b			X	X	X	X	X	X		Input port (1)
		1	0	Other than 01b			X	X	X	X	X	X		Output port
		X	1	Other than 01b			X	X	X	X	X	X		LCD drive control output (SEG37)
		X	0	0	1		0	0	X	X	X	X		PWM2 mode waveform output
		X	0	0	1		0	1	1	X	X	X		PWM mode waveform output
		X	0	0	1		0	1	0	0	0	1		Timer waveform output (output compare function)
										0	1	X		
		0	0	0	1		X	1	0	1	X	X		Timer mode (input capture function) (1)

Pin	Register	PD4	LSE4	TRCPSR0		TRCPSR1	TRCOER		TRCMR			TRCIOR0			TRCIOR1			Function
	Bit	PD4_i	LSE38	TRCIOBSEL		TRCIOC	EB	EC	PWM2	PWMB	PWMC	IOB			IOC			
				1	0	SEL0						2	1	0	2	1	0	
Port P4_6 SEG38 TRCIOB TRCIOC	i = 6	0	0	Other than 10b		0	X	X	X	X	X	X	X	X	X	X	X	Input port (1)
		1	0	Other than 10b		0	X	X	X	X	X	X	X	X	X	X	X	Output port
		X	1	Other than 10b		0	X	X	X	X	X	X	X	X	X	X	X	LCD drive control output (SEG38)
		X	0	1	0	X	0	X	0	X	X	X	X	X	X	X	X	PWM2 mode waveform output
		X	0	1	0	X	0	X	1	1	X	X	X	X	X	X	X	PWM mode waveform output
		X	0	1	0	X	0	X	1	0	X	0	0	1	X	X	X	Timer waveform output (output compare function)
												0	1	X	X	X	X	
		0	0	1	0	0	X	X	1	0	X	1	X	X	X	X	X	Timer mode (input capture function) (1)
		X	0	Other than 10b		1	X	0	1	X	1	X	X	X	X	X	X	PWM mode waveform output
		X	0	Other than 10b		1	X	0	1	X	0	X	X	X	0	0	1	Timer waveform (output compare function)
												X	X	X	0	1	X	
		0	0	Other than 10b		1	X	X	1	X	0	X	X	X	1	X	X	Timer mode (input capture function) (1)

Pin	Register	PD4	LSE4	TRCPSR0		TRCPSR1	TRCOER		TRCMR			TRCIOR0			TRCIOR1			Function
	Bit	PD4_i	LSE39	TRCIOBSEL		TRCIOD	EB	ED	PWM2	PWMB	PWMD	IOB			IOD			
				1	0	SEL0						2	1	0	2	1	0	
Port P4_7 SEG39 TRCIOB TRCIOD	i = 7	0	0	Other than 11b		0	X	X	X	X	X	X	X	X	X	X	X	Input port (1)
		1	0	Other than 11b		0	X	X	X	X	X	X	X	X	X	X	X	Output port
		X	1	Other than 11b		0	X	X	X	X	X	X	X	X	X	X	X	LCD drive control output (SEG39)
		X	0	1	1	X	0	X	0	X	X	X	X	X	X	X	X	PWM2 mode waveform output
		X	0	1	1	X	0	X	1	1	X	X	X	X	X	X	X	PWM mode waveform output
		X	0	1	1	X	0	X	1	0	X	0	0	1	X	X	X	Timer waveform output (output compare function)
												0	1	X	X	X	X	
		0	0	1	1	0	X	X	1	0	X	1	X	X	X	X	X	Timer mode (input capture function) (1)
		X	0	Other than 11b		1	X	0	1	X	1	X	X	X	X	X	X	PWM mode waveform output
		X	0	Other than 11b		1	X	0	1	X	0	X	X	X	0	0	1	Timer waveform output (output compare function)
												X	X	X	0	1	X	
		0	0	Other than 11b		1	X	X	1	X	0	X	X	X	1	X	X	Timer mode (input capture function) (1)

X: 0 or 1; —: No change in outcome

Note:

1. Pulled up by setting the corresponding bit in the P4PUR register to 1.

Table 7.12 Port P5

Pin	Register	PD5	LSE5	—	Function
	Bit	PD5_i	LSEi+40		
Port P5_0 SEG40	i = 0	0	0		Input port (1)
		1	0		Output port
		X	1		LCD drive control output (SEG40)
Port P5_1 SEG41	i = 1	0	0		Input port (1)
		1	0		Output port
		X	1		LCD drive control output (SEG41)
Port P5_2 SEG42	i = 2	0	0		Input port (1)
		1	0		Output port
		X	1		LCD drive control output (SEG42)
Port P5_3 SEG43	i = 3	0	0		Input port (1)
		1	0		Output port
		X	1		LCD drive control output (SEG43)

X: 0 or 1; —: No change in outcome

Note:

1. Pulled up by setting the corresponding bit in the P5PUR register to 1.

Table 7.13 Ports P6_0 to P6_3

Pin	Register	PD6	LSE5	TRDPSR0		TRDOER1	TRDFCR				TRDIORA0			Function
	Bit	PD6_i	LSE44	TRDIOA0SEL		EA0	CMD1	CMD0	STCLK	PWM3	IOA2	IOA1	IOA0	
				1	0									
Port P6_0 SEG44 TRDIOA0 TRDCLK	i = 0	0	0	Other than 01b		X	X	X	X	X	X	X	X	Input port (1)
		1	0			X	X	X	X	X	X	X	X	Output port
		X	1	Other than 01b		X	X	X	X	X	X	X	X	LCD drive control output (SEG44)
		0	0	0	1	X	0	0	0	1	1	X	X	Timer mode (input capture function) (1)
		0	0	0	1	X	X	X	1	1	0	0	0	External clock input (TRDCLK) (1)
		X	0	0	1	0	0	0	0	0	X	X	X	PWM3 mode waveform output
		X	0	0	1	0	0	0	0	1	0	0	1	Timer mode waveform output (output compare function)
											0	1	X	

Pin	Register	PD6	LSE5	TRDPSR0		TRDOER1	TRDFCR			TRDPMR	TRDIORB0			Function
	Bit	PD6_i	LSE45	TRDIOB0SEL		EB0	CMD1	CMD0	PWM3	PWMB0	IOB2	IOB1	IOB0	
				1	0									
Port P6_1 SEG45 TRDIOB0	i = 1	0	0	Other than 01b		X	X	X	X	X	X	X	X	Input port (1)
		1	0			X	X	X	X	X	X	X	X	Output port
		X	1	Other than 01b		X	X	X	X	X	X	X	X	LCD drive control output (SEG45)
		0	0	0	1	X	0	0	1	0	1	X	X	Timer mode (input capture function) (1)
		X	0	0	1	0	1	X	X	X	X	X	X	Complementary PWM mode waveform output
		X	0	0	1	0	0	1	X	X	X	X	X	Reset synchronous PWM mode waveform output
		X	0	0	1	0	0	0	0	X	X	X	X	PWM3 mode waveform output
		X	0	0	1	0	0	0	1	1	X	X	X	PWM mode waveform output
		X	0	0	1	0	0	0	1	0	0	0	1	Timer mode waveform output (output compare function)
											0	1	X	

Pin	Register	PD6	LSE5	TRDPSR0		TRDOER1	TRDFCR			TRDPMR	TRDIORC0			Function
	Bit	PD6_i	LSE46	TRDIOC0SEL		EC0	CMD1	CMD0	PWM3	PWMC0	IOC2	IOC1	IOC0	
				1	0									
Port P6_2 SEG46 TRDIOC0	i = 2	0	0	Other than 01b		X	X	X	X	X	X	X	X	Input port (1)
		1	0			X	X	X	X	X	X	X	X	Output port
		X	1	Other than 01b		X	X	X	X	X	X	X	X	LCD drive control output (SEG46)
		0	0	0	1	X	0	0	1	0	1	X	X	Timer mode (input capture function) (1)
		X	0	0	1	0	1	X	X	X	X	X	X	Complementary PWM mode waveform output
		X	0	0	1	0	0	1	X	X	X	X	X	Reset synchronous PWM mode waveform output
		X	0	0	1	0	0	0	1	1	X	X	X	PWM mode waveform output
		X	0	0	1	0	0	0	1	0	0	0	1	Timer mode waveform output (output compare function)
											0	1	X	

Pin	Register	PD6	LSE5	TRDPSR0		TRDOER1	TRDFCR			TRDPMR	TRDIORC0			Function
	Bit	PD6_i	LSE47	TRDIOD0SEL		ED0	CMD1	CMD0	PWM3	PWMD0	IOD2	IOD1	IOD0	
				1	0									
Port P6_3 SEG47 TRDIOD0	i = 3	0	0	Other than 01b		X	X	X	X	X	X	X	X	Input port (1)
		1	0			X	X	X	X	X	X	X	X	Output port
		X	1	Other than 01b		X	X	X	X	X	X	X	X	LCD drive control output (SEG47)
		0	0	0	1	X	0	0	1	0	1	X	X	Timer mode (input capture function) (1)
		X	0	0	1	0	1	X	X	X	X	X	X	Complementary PWM mode waveform output
		X	0	0	1	0	0	1	X	X	X	X	X	Reset synchronous PWM mode waveform output
		X	0	0	1	0	0	0	1	1	X	X	X	PWM mode waveform output
		X	0	0	1	0	0	0	1	0	0	0	1	Timer mode waveform output (output compare function)
											0	1	X	

X: 0 or 1; —: No change in outcome

Note:

1. Pulled up by setting the corresponding bit in the P6PUR register to 1.

Table 7.14 Ports P6_4 to P6_7

Pin	Register	PD6	LSE6	TRDPSR1		TRDOER1	TRDFCR				TRDIORA1			Function
	Bit	PD6_i	LSE48	TRDIOA1SEL 1	TRDIOA1SEL 0	EA1	CMD1	CMD0	PWM3	—	IOA2	IOA1	IOA0	
Port P6_4 SEG48 TRDIOA1	i = 4	0	0	Other than 01b		X	X	X	X		X	X	X	Input port (1)
		1	0			X	X	X	X		X	X	X	Output port
		X	1	Other than 01b		X	X	X	X		X	X	X	LCD drive control output (SEG48)
		0	0	0	1	X	0	0	1		1	X	X	Timer mode (input capture function) (1)
		X	0	0	1	0	1	X	X		X	X	X	Complementary PWM mode waveform output
		X	0	0	1	0	0	1	X		X	X	X	Reset synchronous PWM mode waveform output
		X	0	0	1	0	0	0	1		0	0	1	Timer mode waveform output (output compare function)
											0	1	X	

Pin	Register	PD6	LSE6	TRDPSR1		TRDOER1	TRDFCR			TRDPMR	TRDIORB1			Function
	Bit	PD6_i	LSE49	TRDIOB1SEL 1	TRDIOB1SEL 0	EB1	CMD1	CMD0	PWM3	PWMB1	IOB2	IOB1	IOB0	
Port P6_5 SEG49 TRDIOB1	i = 5	0	0	Other than 01b		X	X	X	X	X	X	X	X	Input port (1)
		1	0			X	X	X	X	X	X	X	X	Output port
		X	1	Other than 01b		X	X	X	X	X	X	X	X	LCD drive control output (SEG49)
		0	0	0	1	X	0	0	1	0	1	X	X	Timer mode (input capture function) (1)
		X	0	0	1	0	1	X	X	X	X	X	X	Complementary PWM mode waveform output
		X	0	0	1	0	0	1	X	X	X	X	X	Reset synchronous PWM mode waveform output
		X	0	0	1	0	0	0	1	1	X	X	X	PWM mode waveform output
		X	0	0	1	0	0	0	1	0	0	0	1	Timer mode waveform output (output compare function)
											0	1	X	

Pin	Register	PD6	LSE6	TRDPSR1		TRDOER1	TRDFCR			TRDPMR	TRDIORC1			Function
	Bit	PD6_i	LSE50	TRDIOC1SEL 1	TRDIOC1SEL 0	EC1	CMD1	CMD0	PWM3	PWMC1	IOC2	IOC1	IOC0	
Port P6_6 SEG50 TRDIOC1	i = 6	0	0	Other than 01b		X	X	X	X	X	X	X	X	Input port (1)
		0	0			X	X	X	X	X	X	X	X	Output port
		X	1	Other than 01b		X	X	X	X	X	X	X	X	LCD drive control output (SEG50)
		0	0	0	1	X	0	0	1	0	1	X	X	Timer mode (input capture function) (1)
		X	0	0	1	0	1	X	X	X	X	X	X	Complementary PWM mode waveform output
		X	0	0	1	0	0	1	X	X	X	X	X	Reset synchronous PWM mode waveform output
		X	0	0	1	0	0	0	1	1	X	X	X	PWM mode waveform output
		X	0	0	1	0	0	0	1	0	0	0	1	Timer mode waveform output (output compare function)
											0	1	X	

Pin	Register	PD6	LSE6	TRDPSR1		TRDOER1	TRDFCR			TRDPMR	TRDIORD1			Function
	Bit	PD6_i	LSE51	TRDIOC1SEL 1	TRDIOC1SEL 0	ED1	CMD1	CMD0	PWM3	PWMD1	IOD2	IOD1	IOD0	
Port P6_7 SEG51 TRDIOD1	i = 7	0	0	Other than 01b		X	X	X	X	X	X	X	X	Input port (1)
		0	0			X	X	X	X	X	X	X	X	Output port
		X	1	Other than 01b		X	X	X	X	X	X	X	X	LCD drive control output (SEG51)
		0	0	0	1	X	0	0	1	0	1	X	X	Timer mode (input capture function) (1)
		X	0	0	1	0	1	X	X	X	X	X	X	Complementary PWM mode waveform output
		X	0	0	1	0	0	1	X	X	X	X	X	Reset synchronous PWM mode waveform output
		X	0	0	1	0	0	0	1	1	X	X	X	PWM mode waveform output
		X	0	0	1	0	0	0	1	0	0	0	1	Timer mode waveform output (output compare function)
											0	1	X	

X: 0 or 1; —: No change in outcome

Note:

1. Pulled up by setting the corresponding bit in the P6PUR register to 1.

Table 7.15 Port P7

Pin	Register	PD7	LSE6/ LSE7	LCR0			—	Function
	Bit	PD7_i	LSEi+52	LDTY				
				2	1	0		
Port P7_0 SEG52 COM7	i = 0	0	0	X	X	X		Input port (1)
		1	0	X	X	X		Output port
		X	1	0	X	X		LCD drive control output (SEG52)
				1	0	0		LCD drive control output (COM7)
Port P7_1 SEG53 COM6	i = 1	0	0	X	X	X		Input port (1)
		1	0	X	X	X		Output port
		X	1	0	X	X		LCD drive control output (SEG53)
				1	0	0		LCD drive control output (COM6)
Port P7_2 SEG54 COM5	i = 2	0	0	X	X	X		Input port (1)
		1	0	X	X	X		Output port
		X	1	0	X	X		LCD drive control output (SEG54)
				1	0	0		LCD drive control output (COM5)
Port P7_3 SEG55 COM4	i = 3	0	0	X	X	X		Input port (1)
		1	0	X	X	X		Output port
		X	1	0	X	X		LCD drive control output (SEG55)
				1	0	0		LCD drive control output (COM4)
Port P7_4 COM3	i = 4	0	0					Input port (1)
		1	0					Output port
		X	1					LCD drive control output (COM3)
Port P7_5 COM2	i = 5	0	0					Input port (1)
		1	0					Output port
		X	1					LCD drive control output (COM2)
Port P7_6 COM1	i = 6	0	0					Input port (1)
		1	0					Output port
		X	1					LCD drive control output (COM1)
Port P7_7 COM0	i = 7	0	0					Input port (1)
		1	0					Output port
		X	1					LCD drive control output (COM0)

X: 0 or 1; —: No change in outcome
Note:
1. Pulled up by setting the corresponding bit in the P6PUR or P7PUR register to 1.

Table 7.16 Ports P10_0 to P10_3

Pin	Register	PD10	KISR	KIEN	TRDPSR0		TRDOER1	TRDFCR				TRDIORA0			Function
	Bit	PD10_i	KISEL0	KIEN	TRDIOA0SEL 1	TRDIOA0SEL 0	EA0	CMD1	CMD0	STCLK	PWM3	IOA2	IOA1	IOA0	
Port P10_0 (TRDIOA0 TRDCLK $\overline{KI0}$)	i = 0	0	X	X	Other than 10b		X	X	X	X	X	X	X	X	Input port (1)
		1	X	X			X	X	X	X	X	X	X	X	Output port
		0	1	1	Other than 10b		X	X	X	X	X	X	X	X	$\overline{KI0}$ input (1)
		0	X	X	1	0	X	0	0	0	1	1	X	X	Timer mode (input capture function) (1)
		0	X	X	1	0	X	X	X	1	1	0	0	0	External clock input (TRDCLK) (1)
		X	X	X	1	0	0	0	0	0	0	X	X	X	PWM3 mode waveform output
		X	X	X	1	0	0	0	0	0	1	0	0	1	Timer mode waveform output (output compare function)
												0	1	X	
Pin	Register	PD10	KISR	KIEN	TRDPSR0		TRDOER1	TRDFCR			TRDPMR	TRDIORB0			Function
	Bit	PD10_i	KISEL0	KIEN	TRDIOB0SEL 1	TRDIOB0SEL 0	EB0	CMD1	CMD0	PWM3	PWMB0	IOB2	IOB1	IOB0	
Port P10_1 (TRDIOB0 $\overline{KI1}$)	i = 1	0	X	X	Other than 10b		X	X	X	X	X	X	X	X	Input port (1)
		1	X	X			X	X	X	X	X	X	X	X	Output port
		0	1	1	Other than 10b		X	X	X	X	X	X	X	X	$\overline{KI1}$ input (1)
		0	X	X	1	0	X	0	0	1	0	1	X	X	Timer mode (input capture function) (1)
		X	X	X	1	0	0	1	X	X	X	X	X	X	Complementary PWM mode waveform output
		X	X	X	1	0	0	0	1	X	X	X	X	X	Reset synchronous PWM mode waveform output
		X	X	X	1	0	0	0	0	0	X	X	X	X	PWM3 mode waveform output
		X	X	X	1	0	0	0	0	1	1	X	X	X	PWM mode waveform output
		X	X	X	1	0	0	0	0	1	0	0	0	1	Timer mode waveform output (output compare function)
												0	1	X	
Pin	Register	PD10	KISR	KIEN	TRDPSR0		TRDOER1	TRDFCR			TRDPMR	TRDIORC0			Function
	Bit	PD10_i	KISEL0	KIEN	TRDIOC0SEL 1	TRDIOC0SEL 0	EB0	CMD1	CMD0	PWM3	PWMC0	IOC2	IOC1	IOC0	
Port P10_2 (TRDIOC0 $\overline{KI2}$)	i = 2	0	X	X	Other than 10b		X	X	X	X	X	X	X	X	Input port (1)
		1	X	X			X	X	X	X	X	X	X	X	Output port
		0	1	1	Other than 10b		X	X	X	X	X	X	X	X	$\overline{KI2}$ input (1)
		0	X	X	1	0	X	0	0	1	0	1	X	X	Timer mode (input capture function) (1)
		X	X	X	1	0	0	1	X	X	X	X	X	X	Complementary PWM mode waveform output
		X	X	X	1	0	0	0	1	X	X	X	X	X	Reset synchronous PWM mode waveform output
		X	X	X	1	0	0	0	0	1	1	X	X	X	PWM mode waveform output
		X	X	X	1	0	0	0	0	1	0	0	0	1	Timer mode waveform output (output compare function)
												0	1	X	
Pin	Register	PD10	KISR	KIEN	TRDPSR0		TRDOER1	TRDFCR			TRDPMR	TRDIORD0			Function
	Bit	PD10_i	KISEL0	KIEN	TRDIOD0SEL 1	TRDIOD0SEL 0	ED0	CMD1	CMD0	PWM3	PWMD0	IOD2	IOD1	IOD0	
Port P10_3 (TRDIOD0 $\overline{KI3}$)	i = 3	0	X	X	Other than 10b		X	X	X	X	X	X	X	X	Input port (1)
		1	X	X			X	X	X	X	X	X	X	X	Output port
		0	1	1	Other than 10b		X	X	X	X	X	X	X	X	$\overline{KI3}$ input (1)
		0	X	X	1	0	X	0	0	1	0	1	X	X	Timer mode (input capture function) (1)
		X	X	X	1	0	0	1	X	X	X	X	X	X	Complementary PWM mode waveform output
		X	X	X	1	0	0	0	1	X	X	X	X	X	Reset synchronous PWM mode waveform output
		X	X	X	1	0	0	0	0	1	1	X	X	X	PWM mode waveform output
		X	X	X	1	0	0	0	0	1	0	0	0	1	Timer mode waveform output (output compare function)
												0	1	X	

X: 0 or 1; —: No change in outcome

Note:

1. Pulled up by setting the corresponding bit in the P10PUR register to 1.

Table 7.17 Ports P10_4 to P10_7

Pin	Register	PD10	KISR	KIEN1	TRDPSR1		TRDOER1	TRDFCR				TRDIORA1			Function
	Bit	PD10_i	KiSEL0	KiEN	TRDIOA1SEL 1	TRDIOA1SEL 0	EA1	CMD1	CMD0	PWM3	—	IOA2	IOA1	IOA0	
Port P10_4 (TRDIOA1 $\overline{KI4}$)	i = 4	0	X	X	Other than 10b		X	X	X	X		X	X	X	Input port (1)
		1	X	X			X	X	X	X		X	X	X	Output port
		0	1	1	Other than 10b		X	X	X	X		X	X	X	$\overline{KI4}$ input (1)
		0	X	X	1	0	X	0	0	1		1	X	X	Timer mode (input capture function) (1)
		X	X	X	1	0	0	1	X	X		X	X	X	Complementary PWM mode waveform output
		X	X	X	1	0	0	0	1	X		X	X	X	Reset synchronous PWM mode waveform output
		X	X	X	1	0	0	0	0	1		0	0	1	Timer mode waveform output (output compare function)
												0	1	X	

Pin	Register	PD10	KISR	KIEN	TRDPSR1		TRDOER1	TRDFCR			TRDPMR	TRDIORA1			Function
	Bit	PD10_i	KiSEL0	KiEN	TRDIOB1SEL 1	TRDIOB1SEL 0	EB1	CMD1	CMD0	PWM3	PWMB1	IOB2	IOB1	IOB0	
Port P10_5 (TRDIOB1 $\overline{KI5}$)	i = 5	0	X	X	Other than 10b		X	X	X	X	X	X	X	X	Input port (1)
		1	X	X			X	X	X	X	X	X	X	X	Output port
		0	1	1	Other than 10b		X	X	X	X	X	X	X	X	$\overline{KI5}$ input (1)
		0	X	X	1	0	X	0	0	1	0	1	X	X	Timer mode (input capture function) (1)
		X	X	X	1	0	0	1	X	X	X	X	X	X	Complementary PWM mode waveform output
		X	X	X	1	0	0	0	1	X	X	X	X	X	Reset synchronous PWM mode waveform output
		X	X	X	1	0	0	0	0	1	1	X	X	X	PWM mode waveform output
		X	X	X	1	0	0	0	0	1	0	0	0	1	Timer mode waveform output (output compare function)
												0	1	X	

Pin	Register	PD10	KISR	KIEN	TRDPSR1		TRDOER1	TRDFCR			TRDPMR	TRDIORC1			Function
	Bit	PD10_i	KiSEL0	KiEN	TRDIOC1SEL 1	TRDIOC1SEL 0	EC1	CMD1	CMD0	PWM3	PWMC1	IOC2	IOC1	IOC0	
Port P10_6 (TRDIOC1 $\overline{KI6}$)	i = 6	0	X	X	Other than 10b		X	X	X	X	X	X	X	X	Input port (1)
		1	X	X			X	X	X	X	X	X	X	X	Output port
		0	1	1	Other than 10b		X	X	X	X	X	X	X	X	$\overline{KI6}$ input (1)
		0	X	X	1	0	X	0	0	1	0	1	X	X	Timer mode (input capture function) (1)
		X	X	X	1	0	0	1	X	X	X	X	X	X	Complementary PWM mode waveform output
		X	X	X	1	0	0	0	1	X	X	X	X	X	Reset synchronous PWM mode waveform output
		X	X	X	1	0	0	0	0	1	1	X	X	X	PWM mode waveform output
		X	X	X	1	0	0	0	0	1	0	0	0	1	Timer mode waveform output (output compare function)
												0	1	X	

Pin	Register	PD10	KISR	KIEN	TRDPSR1		TRDOER1	TRDFCR			TRDPMR	TRDIORC1			Function
	Bit	PD10_i	KiSEL0	KiEN	TRDIOD1SEL 1	TRDIOD1SEL 0	ED1	CMD1	CMD0	PWM3	PWMD1	IOD2	IOD1	IOD0	
Port P10_7 (TRDIOD1 $\overline{KI7}$)	i = 7	0	X	X	Other than 10b		X	X	X	X	X	X	X	X	Input port (1)
		1	X	X			X	X	X	X	X	X	X	X	Output port
		0	1	1	Other than 10b		X	X	X	X	X	X	X	X	$\overline{KI7}$ input (1)
		0	X	X	1	0	X	0	0	1	0	1	X	X	Timer mode (input capture function) (1)
		X	X	X	1	0	0	1	X	X	X	X	X	X	Complementary PWM mode waveform output
		X	X	X	1	0	0	0	1	X	X	X	X	X	Reset synchronous PWM mode waveform output
		X	X	X	1	0	0	0	0	1	1	X	X	X	PWM mode waveform output
		X	X	X	1	0	0	0	0	1	0	0	0	1	Timer mode waveform output (output compare function)
												0	1	X	

X: 0 or 1; —: No change in outcome

Note:

1. Pulled up by setting the corresponding bit in the P10PUR register to 1.

Table 7.18 Ports P11_0 and P11_1

Pin	Register	PD11	INTSR	INTEN	INTCMP	ACMR	SSUIICSR	ICCR1	SSU Associated Register (7)		U2SR1	U2MR				Function
	Bit	PD11_i	INTi SEL0	INTiEN	INT1 CP0	CM10E	IICSEL	ICE	SSCK output control	SSCK input control	CLK2SEL0	SMD 2	SMD 1	SMD 0	CKDIR	
Port P11_0 SCL SSCK (CLK2 INT0) IVREF1 LVCOUT1	i = 0	0	X	X	X	0	0	X	0	0	0	X	X	X	X	Input port (1)
							1	0	X	X						
		1	X	X	X	0	0	X	0	0	0	X	X	X	X	Output port (2)
							1	0	X	X						
		0	X	X	X	0	1	1	X	X	0	X	X	X	X	SCL input/output (2)
		0	X	X	X	0	0	X	0	1	0	X	X	X	X	SSCK input (1)
		0	X	X	X	0	0	X	1	0	0	X	X	X	X	SSCK output (2, 5)
		0	X	X	X	0	0	X	0	0	1	X	X	X	1	CLK2 input (1)
							1	0	X	X						
		0	X	X	X	0	0	X	0	0	1	0	0	1	0	CLK2 output (2, 6)
							1	0	X	X						
		0	1	1	X	0	0	X	0	0	0	X	X	X	X	$\overline{\text{INT0}}$ input (1)
							1	0	X	X						
		0	X	X	1	0	0	X	0	0	0	X	X	X	X	Comparator B1 reference voltage input (IVREF1)
							1	0	X	X						
		X	X	X	X	1	0	X	0	0	0	X	X	X	X	Comparator A1 output (LVCOUT1) (2)
							1	0	X	X						

Pin	Register	PD11	INTSR	INTEN	INTCMP	ACMR	SSUIICSR	SSU Associated Register (7)		U2SR0				U2MR			U2SMR	Function
	Bit	PD11_i	INTi SEL0	INTiEN	INT1 CP0	CM20E	IICSEL	SSI output control	SSI input control	RXD2 SEL 1	RXD2 SEL 0	TXD2 SEL 1	TXD2 SEL 0	SMD 2	SMD 1	SMD 0	IICM	
Port P11_1 SSI (RXD2 SCL2 TXD2 SDA2 $\overline{\text{INT1}}$) IVCMP1 LVCOUT2	i = 1	0	X	X	X	0	X	0	0	X	X	Other than 10b		X	X	X	X	Input port (1)
		1	X	X	X	0	X	0	0	X	X			X	X	X	X	Output port (2)
		0	X	X	X	0	0	0	1	X	X			X	X	X	X	SSI input (1)
		X	X	X	X	0	0	1	0	X	X			X	X	X	X	SSI output (2, 5)
		0	X	X	X	0	X	0	0	0	1			X	X	X	0	RXD2 input (1)
		0	X	X	X	0	X	0	0	0	1			0	1	0	1	SCL2 input/output (2, 6)
		X	X	X	X	0	X	0	0	X	X	1	0	0	0	1	0	TXD2 output (2, 6)
														1	0	X	0	
														1	1	0	0	
		0	X	X	X	0	X	0	0	X	X	1	0	0	1	0	1	SDA2 input/output (2, 6)
		0	1	1	0	0	X	0	0	X	X	Other than 10b		X	X	X	X	$\overline{\text{INT1}}$ input (1)
		0	0	1	1	0	X	0	0	X	X			X	X	X	X	Comparator B1 input (IVCMP1)
		0	X	X	X	1	X	0	0	X	X			X	X	X	X	Comparator A2 output (LVCOUT2) (2)

X: 0 or 1; —: No change in outcome

Notes:
1. Pulled up by setting the corresponding bit in the P11PUR register to 1.
2. Output drive capacity high by setting the corresponding bit in the P10DRR register to 1.
3. N-channel open-drain output by setting the SCKOS bit in the SSMR2 register to 1.
4. N-channel open-drain output by setting the NODC bit in the U2SMR3 register to 1.
5. N-channel open-drain output by setting the SOOS bit in the SSMR2 register to 1 (N-channel open-drain output) and setting the BIDE bit to 0 (standard mode).
6. N-channel open-drain output by setting the NCH bit in the U2C0 register to 1.
7. Synchronous serial communication unit (refer to **Table 27.4 Association between Communication Modes and I/O Pins**).

Table 7.19 Ports P11_2 and P11_3

Pin	Register	PD11	INTSR	INTEN	INTCMP	—	SSUIICSR	ICCR1	SSU Associated Register (6)		U2SR0				U2MR			U2SMR	Function
	Bit	PD11_i	INTi SEL0	INTiEN	INT3 CP0	—	IICSEL	ICE	SSI output control	SSI input control	RXD2 SEL		TXD2 SEL		SMD			IICM	
											1	0	1	0	2	1	0		
Port P11_2 SDA SSO (RXD2 SCL2 TXD2 SDA2 $\overline{INT2}$) IVREF3	i = 2	0	X	X	X	—	1	0	X	X	X	X	Other than 01b		X	X	X	0	Input port (1)
		0	X	X	X	—	0	X	0	0	X	X			X	X	X	0	
		1	X	X	X	—	1	0	X	X	X	X	Other than 01b		X	X	X	0	Output port (2)
		1	X	X	X	—	0	X	0	0	X	X			X	X	X	0	
		0	X	X	X	—	1	1	X	X	X	X	Other than 01b		X	X	X	0	SDA input/output (2)
		0	X	X	X	—	0	X	0	1	X	X			X	X	X	0	SSO input (1)
		0	X	X	X	—	0	X	1	0	X	X			X	X	X	0	SSO output (2, 3)
		0	X	X	X	—	1	0	X	X	1	0	Other than 01b		X	X	X	0	RXD2 input (1)
							0	X	0	0									
		0	X	X	X	—	1	0	X	X	1	0	Other than 01b		0	1	0	1	SCL2 input/output (2, 4)
							0	X	0	0									
		0	X	X	X	—	1	0	X	X	X	X	0	1	0	0	1	0	TXD2 output (2, 4)
			X	X	X	—	0	X	0	0					1	0	X		
															1	1	0		
		0	X	X	X	—	1	0	X	X	X	X	0	1	0	1	0	1	SDA2 input/outpu (2, 4)
							0	X	0	0									
		0	1	1	X	—	X	X	0	0	X	X	0	1	X	X	X	X	$\overline{INT2}$ input (1)
		0	X	X	1	—	X	X	0	0	X	X	Other than 01b		X	X	X	X	Comparator B3 reference voltage input (IVREF3)

Pin	Register	PD11	INTSR	INTEN	INTCMP	—	—	SSMR2		U2CO		U2SR1	U2MR			—	Function
	Bit	PD11_i	INTi SEL0	INTiEN	INT3 CP0	—	—	CSS		CRS	CRD	CTSSEL0	SMD				
								1	0				2	1	0		
Port P11_3 $\overline{SCS}$ ($\overline{CTS2}$ $\overline{RTS2}$ $\overline{INT3}$) IVCMP3	i = 3	0	X	X	X	—	—	0	0	X	X	0	X	X	X		Input port (1)
		1	X	X	X	—	—	0	0	X	X	0	X	X	X		Output port (2)
		X	X	X	X	—	—	0	1	X	X	X	X	X	X		$\overline{SCS}$ input (1)
		X	X	X	X	—	—	1	X	X	X	X	X	X	X		$\overline{SCS}$ output (2, 5)
		0	X	X	X	—	—	0	0	0	0	1	Other than 000b				$\overline{CTS2}$ input (1)
		0	X	X	X	—	—	0	0	1	0	1					$\overline{RTS2}$ output (2)
		0	1	1	0	—	—	0	0	X	X	0	X	X	X		$\overline{INT3}$ input (1)
		0	0	1	1	—	—	0	0	X	X	0	X	X	X		Comparator B3 input (IVCMP3)

X: 0 or 1; —: No change in outcome

Notes:

1. Pulled up by setting the corresponding bit in the P11PUR register to 1.
2. Output drive capacity high by setting the corresponding bit in the P11DRR register to 1.
3. N-channel open-drain output by setting the SOOS bit in the SSMR2 register to 1 (N-channel open-drain output).
4. N-channel open-drain output by setting the NCH bit in the U2C0 register to 1.
5. N-channel open-drain output by setting the CSOS bit in the SSMR2 register to 1.
6. Synchronous serial communication unit (refer to **Table 27.4 Association between Communication Modes and I/O Pins**).

Table 7.20 Ports P11_4 to P11_7

Pin	Register	PD11	INTSR	INTEN1	TRASR		TRAIOC	TRAMR			U0SR			Function
	Bit	PD11_i	INTiSEL0	INTiEN	TRAIOSEL		TOPCR	TMOD0			RXD0SEL			
					1	0		2	1	0	1	0		
Port P11_4 TRAIO ($\overline{\text{INT4}}$ RXD0)	i = 4	0	X	X	0	0	X	X	X	X	X	X		Input port (1)
		1	X	X	0	0	X	X	X	X	X	X		Output port (2)
		0	X	X	1	1	0	Other than 000b, 001b			X	X		TRAIO input (1)
		0	1	1	0	0	X	X	X	X	X	X		$\overline{\text{INT4}}$ input (1)
		0	1	1	1	0	0	Other than 000b, 001b			X	X		TRAIO/$\overline{\text{INT4}}$ input (1)
		X	X	X	1	1	0	0	0	1	X	X		TRAIO pulse output (2)
		0	X	X	0	0	X	X	X	X	1	0		RXD0 input (1)
Pin	Register	PD11	INTSR	INTEN1	—		TRAIOC	—	—	—				Function
	Bit	PD11_i	INTiSEL0	INTiEN	—		TOENA	—	—	—				
Port P11_5 TRAO ($\overline{\text{INT5}}$)	i = 5	0	X	X	—		0							Input port (1)
		1	X	X	—		0							Output port (2)
		X	X	X	—		1							TRAO input (1)
		0	1	1	—		0							$\overline{\text{INT5}}$ input (1)
Pin	Register	PD11	INTSR	INTEN1	—		TRBIOC	TRBMR						Function
	Bit	PD11_i	INTiSEL0	INTiEN	—		TOCNT	TMOD						
								1	0					
Port P11_6 TRBO ($\overline{\text{INT6}}$)	i = 6	0	X	X	—		X	0	0					Input port (1)
		1	X	X	—		X	0	0					Output port (2)
		X	X	X	—		1	X	X					
		X	X	X	—		0	0	1					Programmable waveform generation mode (2)
		X	X	X	—		0	1	0					Programmable one-shot generation mode (2)
		X	X	X	—		0	1	1					Programmable wait one-shot generation mode (2)
		0	1	1	—		X	0	0					$\overline{\text{INT6}}$ input (1)
Pin	Register	PD11	INTSR	INTEN1	—		TRECR1	ADMOD						Function
	Bit	PD11_i	INTiSEL0	INTiEN	—		TOENA	ADCAP						
					—			1	0					
Port P11_7 TREO ($\overline{\text{INT7}}$ $\overline{\text{ADTRG}}$)	i = 7	0	X	X	—		0	X	X					Input port (1)
		1	X	X	—		0	X	X					Output port (2)
		X	X	X	—		1	X	X					TREO output (2)
		0	1	1	—		0	X	X					$\overline{\text{INT7}}$ input (1)
		0	1	1	—		0	1	1					$\overline{\text{ADTRG}}$ input (1)

X: 0 or 1; —: No change in outcome

Notes:
1. Pulled up by setting the corresponding bit in the P11PUR register to 1.
2. Output drive capacity high by setting the corresponding bit in the P11DRR register to 1.

Table 7.21 Ports P12_0 to P12_3

Pin	Register	PD12	CM0		CM1				Circuit Specifications		Function
	Bit	PD12_i	CM05	CM07	CM10	CM11	CM13		Oscillation buffer	Feedback resistor	
Port P12_0 XIN	i = 4	0	1	1	0	1	0		OFF	OFF	Input port (1)
		1	1	1	0	1	0		OFF	OFF	Output port
		0	1	0	0	1	0		ON	ON	XIN clock input (1)
		0	1	0	1	1	0		ON	ON	XIN clock input stop (STOP mode) (1)
		0	0	0	0	0	1		ON	ON	XIN-XOUT oscillation (on-chip feedback resistor enabled)
		0	0	0	0	1	1		ON	OFF	XIN-XOUT oscillation (on-chip feedback resistor disabled)
		0	1	0	0	0	1		OFF	ON	XIN-XOUT oscillation stop (on-chip feedback resistor enabled)
		0	1	0	0	1	1		OFF	OFF	XIN-XOUT oscillation stop (on-chip feedback resistor disabled)
		0	0	0	1	X	1		OFF	OFF	oscillation stop (STOP mode)
Pin	Register	PD12	CM0		CM1				Circuit Specifications		Function
	Bit	PD12_i	CM05	CM07	CM10	CM11	CM13		Oscillation buffer	Feedback resistor	
Port P12_1 XOUT	i = 1	0	1	X	0	1	0		OFF	OFF	Input port (1)
		1	1	X	0	1	0		OFF	OFF	Output port
		0	0	0	0	0	1		ON	ON	XIN-XOUT oscillation (on-chip feedback resistor enabled)
		0	0	0	0	1	1		ON	OFF	XIN-XOUT oscillation (on-chip feedback resistor disabled)
		0	1	0	0	0	1		OFF	ON	XIN-XOUT oscillation stop (on-chip feedback resistor enabled)
		0	1	0	0	1	1		OFF	OFF	XIN-XOUT oscillation stop (on-chip feedback resistor disabled)
		0	0	0	1	X	1		OFF	OFF	oscillation stop (STOP mode)
Pin	Register	PD12	LSE7	—							Function
	Bit	PD12_i	LSE60								
Port P12_2 CL1	i = 2	0	0								Input port (1)
		1	0								Output port
		X	1								CL1
Port P12_3 CL2	i = 3	0	0								Input port (1)
		1	0								Output port
		X	1								CL2

X: 0 or 1; —: No change in outcome

Note:

1. Pulled up by setting the corresponding bit in the P12PUR register to 1.

Table 7.22 Ports P13_0 to P13_3

Pin	Register	PD13	ADINSEL					DACON	—	Function
	Bit	PD13_i	CH			ADGSEL		DA0E		
			2	1	0	1	0			
Port P13_0 AN0 DA0 $\overline{\text{WKUP1}}$	i = 0	0	X	X	X	X	X	0		Input port (1)
		1	X	X	X	X	X	0		Output port
		0	X	X	X	X	X	0		$\overline{\text{WKUP1}}$ input (1)
		0	0	0	0	0	0	0		A/D converter input (AN0) (1)
		0	X	X	X	X	X	1		D/A converter output (DA0)

Pin	Register	PD13	ADINSEL					DACON	VCA2		U0SR	U0MR			—	Function
	Bit	PD13_i	CH			ADGSEL		DA1E	VCA21	VCA23	TXD0 SEL0	SMD				
			2	1	0	1	0					2	1	0		
Port P13_1 AN1 DA1 TXD0 LVREF	i = 1	0	X	X	X	X	X	0	X	X	0	X	X	X		Input port (1)
		1	X	X	X	X	X	0	X	X	0	X	X	X		Output port
		0	0	0	1	0	0	0	X	X	0	X	X	X		A/D converter input (AN1) (1)
		0	X	X	X	X	X	1	X	X	0	X	X	X		D/A converter output (DA1)
		0	X	X	X	X	X	0	X	X	1	0	0	1		TXD0 output (2)
												1	0	X		
												1	1	0		
		0	X	X	X	X	X	0	1	X	0	X	X	X		Comparator A1 reference input (LVREF)
		0	X	X	X	X	X	0	X	1	0	X	X	X		Comparator A2 reference input (LVREF)

Pin	Register	PD13	ADINSEL					—	VCA2	U0SR		—	Function
	Bit	PD13_i	CH			ADGSEL		—	VCA22	RXD0 SEL			
			2	1	0	1	0			1	0		
Port P13_2 AN2 RXD0 LVCMP1	i = 2	0	X	X	X	X	X	—	X	X	X		Input port (1)
		1	X	X	X	X	X	—	X	X	X		Output port
		0	0	1	0	0	0	—	X	X	X		A/D converter input (AN2) (1)
		0	X	X	X	X	X	—	X	0	1		RXD0 input (1)
		0	X	X	X	X	X	—	1	X	X		Comparator A1 input (LVCMP1)

Pin	Register	PD13	ADINSEL					—	VCA2	U0SR	U0MR				—	Function
	Bit	PD13_i	CH			ADGSEL		—	VCA24	CLK0 SEL0	SMD			CKDIR		
			2	1	0	1	0				2	1	0			
Port P13_3 AN3 CLK0 LVCMP2	i = 3	0	X	X	X	X	X	—	X	0	X	X	X	X		Input port (1)
		1	X	X	X	X	X	—	X	0	X	X	X	X		Output port
		0	0	1	1	0	0	—	X	0	X	X	X	X		A/D converter input (AN3) (1)
		0	X	X	X	X	X	—	X	1	X	X	X	1		CLK0 (external clock input) (1)
		X	X	X	X	X	X	—	X	1	0	0	1	0		CLK0 (internal clock) output
		0	X	X	X	X	X	—	1	0	X	X	X	X		Comparator A2 input (LVCMP2)

X: 0 or 1; —: No change in outcome

Notes:
1. Pulled up by setting the corresponding bit in the P13PUR register to 1.
2. N-channel open-drain output by setting the NCH bit in the U0C0 register to 1.

Table 7.23 Ports P13_4 to P13_7

Pin	Register	PD13	ADINSEL					TRGPSR	TRGIOR			TRGMR		Function
			CH			ADGSEL		TRG IOASEL	IOA			PWM		
	Bit	PD13_i	2	1	0	1	0		2	1	0			
Port P13_4 AN16 TRGIOA	i = 4	0	X	X	X	X	X	0	X	X	X	X		Input port (1)
		1	X	X	X	X	X	0	X	X	X	X		Output port
		0	0	0	0	1	0	0	X	X	X	X		A/D converter input (AN16) (1)
		0	X	X	X	X	X	1	1	X	X	0		Timer mode (input capture function) (1)
		X	X	X	X	X	X	1	X	X	X	1		PWM mode waveform output
		X	X	X	X	X	X	1	0	0	1	0		Timer mode waveform output (output compare function)
										1	X			
Pin	Register	PD13	ADINSEL					TRGPSR	TRGCR			TRGMR		Function
			CH			ADGSEL		TRG CLKA SEL	TCK			MDF		
	Bit	PD13_i	2	1	0	1	0		2	1	0			
Port P13_5 AN17 TRGCLKA	i = 5	0	X	X	X	X	X	0	X	X	X	X		Input port (1)
		1	X	X	X	X	X	0	X	X	X	X		Output port
		0	0	0	1	1	0	0	X	X	X	X		A/D converter input (AN17) (1)
		X	X	X	X	X	X	1	1	0	1	0		TRGCLKA input (other than phase-counting mode) (1)
		X	X	X	X	X	X	1	X	X	X	1		TRGCLKA input (phase-counting mode) (1)
Pin	Register	PD13	ADINSEL					TRGPSR	TRGIOR					Function
			CH			ADGSEL		TRG IOBSEL	IOB					
	Bit	PD13_i	2	1	0	1	0		2	1	0			
Port P13_6 AN18 TRGIOB	i = 6	0	X	X	X	X	X	0	X	X	X			Input port (1)
		1	X	X	X	X	X	0	X	X	X			Output port
		0	0	1	0	1	0	0	X	X	X			A/D converter input (AN18) (1)
		0	X	X	X	X	X	1	1	X	X			Timer mode (input capture function) (1)
		X	X	X	X	X	X	1	0	0	1			Timer mode waveform output (output compare function)
										1	X			
Pin	Register	PD13	ADINSEL					TRGPSR	TRGCR			TRGMR		Function
			CH			ADGSEL		TRG CLKB SEL	TCK			MDF		
	Bit	PD13_i	2	1	0	1	0		2	1	0			
Port P13_7 AN19 TRGCLKB	i = 7	0	X	X	X	X	X	0	X	X	X	X		Input port (1)
		1	X	X	X	X	X	0	X	X	X	X		Output port
		0	0	1	1	1	0	0	X	X	X	X		A/D converter input (AN19) (1)
		0	X	X	X	X	X	1	1	1	1	0		TRGCLKB input (other than phase-counting mode) (1)
		0	X	X	X	X	X	1	X	X	X	1		TRGCLKB input (phase-counting mode) (1)

X: 0 or 1; —: No change in outcome

Note:

1. Pulled up by setting the corresponding bit in the P13PUR register to 1.

7.6 Unassigned Pin Handling

Table 7.24 lists Unassigned Pin Handling.

Table 7.24 Unassigned Pin Handling

Pin Name	Connection
Ports P0 to P7, Ports P10, P11, 12_2, P12_3	• After setting to input mode, connect each pin to VSS via a resistor (pull-down) or connect each pin to VCC via a resistor (pull-up). (2) • After setting to output mode, leave these pins open. (1, 2)
Ports P12_0, P12_1	Connect to VCC via a pull-up resistor. (2)
VREF	Connect to VCC.
$\overline{\text{WKUP0}}$ (3)	Connect to VSS. (3)
$\overline{\text{RESET}}$ (4)	Connect to VCC via a pull-up resistor. (4)

Notes:
1. If these ports are set to output mode and left open, they remain in input mode until they are switched to output mode by a program. The voltage level of these pins may be undefined and the power current may increase while the ports remain in input mode.
   The content of the direction registers may change due to noise or program runaway caused by noise. In order to enhance program reliability, the program should periodically repeat the setting of the direction registers.
2. Connect these unassigned pins to the MCU using the shortest wire length (2 cm or less) possible.
3. When power-off mode is not used.
4. When the power-on reset function is used.

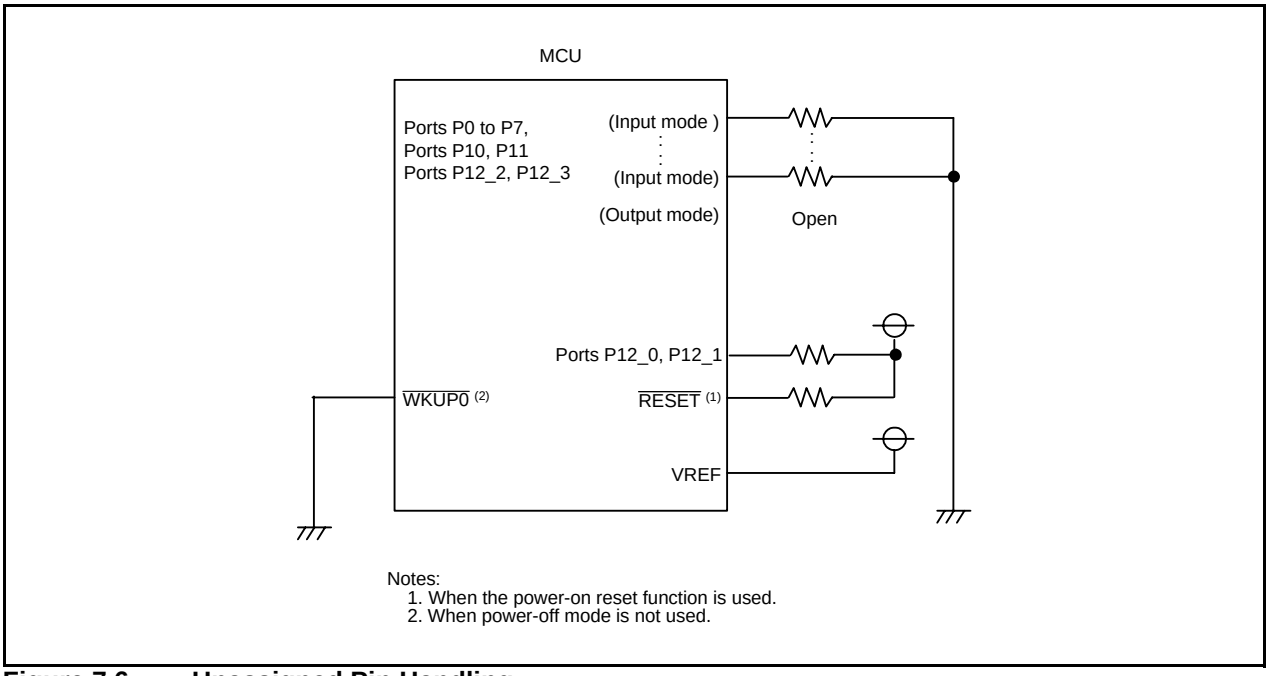


Figure 7.6 Unassigned Pin Handling

8. Bus

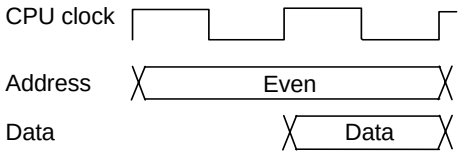
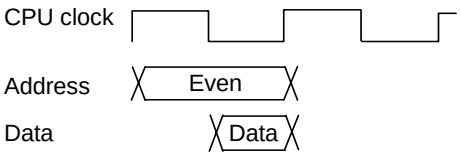
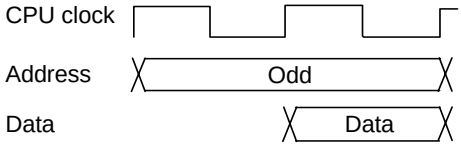
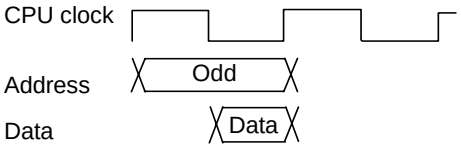
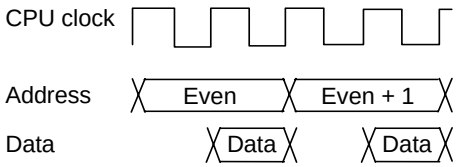
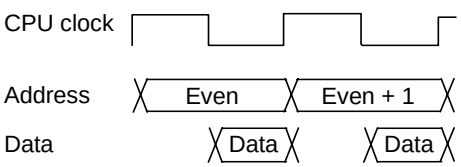
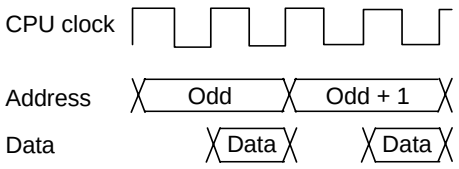
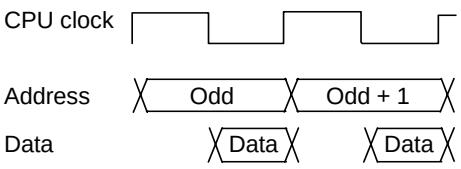
The bus cycles differ when accessing ROM/RAM and when accessing SFR.
Table 8.1 lists the Bus Cycles by Access Area.
ROM/RAM and SFR are connected to the CPU by an 8-bit bus. When accessing in word (16-bit) units, these areas are accessed twice in 8-bit units.
Table 8.2 shows Access Units and Bus Operations.

Table 8.1 Bus Cycles by Access Area

Access Area	Bus Cycle
SFR/Data flash	2 cycles of CPU clock
Program ROM/RAM	1 cycle of CPU clock

Note:
1. Data flash is provided only in the following four: the R8C/L35A Group, L36A Group, L38A Group, and L3AA Group.

Table 8.2 Access Units and Bus Operations

Area	SFR, Data flash	ROM (program ROM), RAM
Even address Byte access		
Odd address Byte access		
Even address Word access		
Odd address Word access		

However, only the following SFRs are connected with the 16-bit bus:

Interrupts: Each interrupt control register
Timer RC: Registers TRC, TRCGRA, TRCGRB, TRCGRC, and TRCGRD
Timer RD: Registers TRDi (i = 0 or 1), TRDGRAi, TRDGRBi, TRDGRCi, and TRDGRDi
Timer RG: Registers TRG, TRGGRA, and TRGGRB
SSU: Registers SSTDR, SSTDRH, SSRDR, and SSRDRH
UART2: Registers U2MR, U2BRG, U2TB, U2C0, U2C1, U2RB, U2SMR5, U2SMR4, U2SMR3, U2SMR2, and U2SMR
A/D converter: Registers AD0, AD1, AD2, AD3, AD4, AD5, AD6, AD7, ADMOD, ADINSEL, ADCON0, and ADCON1
D/A converter: Registers DA0 and DA1
Address match interrupt: Registers RMAD0, AIER0, RMAD1, and AIER1
Therefore, they are accessed once in 16-bit units. The bus operation is the same as “Area: SFR, Data flash, Even address Byte Access” in Table 8.2 Access Units and Bus Operations, and 16-bit data is accessed at a time.

9. Clock Generation Circuit

The following five circuits are incorporated in the clock generation circuit:

- XIN clock oscillation circuit
- XCIN clock oscillation circuit
- Low-speed on-chip oscillator
- High-speed on-chip oscillator
- Low-speed on-chip oscillator for the watchdog timer

9.1 Introduction

Table 9.1 lists the Specification Overview of Clock Generation Circuit. Figure 9.1 shows the Clock Generation Circuit and Figure 9.2 shows the Peripheral Function Clock.

Table 9.1 Specification Overview of Clock Generation Circuit

Item	XIN Clock Oscillation Circuit	XCIN Clock Oscillation Circuit	On-Chip Oscillator		Low-Speed On-Chip Oscillator for Watchdog Timer
			High-Speed On-Chip Oscillator	Low-Speed On-Chip Oscillator	
Applications	• CPU clock source • Peripheral function clock source	• CPU clock source • Peripheral function clock source	• CPU clock source • Peripheral function clock source • CPU and peripheral function clock source when XIN clock stops oscillating	• CPU clock source • Peripheral function clock source • CPU and peripheral function clock source when XIN clock stops oscillating	• Watchdog timer clock source
Clock frequency	0 to 20 MHz	32.768 kHz	Approx. 40 MHz (3)	Approx. 125 kHz	Approx. 125 kHz
Connectable oscillator	• Ceramic resonator • Crystal oscillator	• Crystal oscillator	–	–	–
Oscillator connect pins	XIN, XOUT (1)	XCIN, XCOUT	– (1)	– (1)	–
Oscillation stop, restart function	Usable	Usable	Usable	Usable	Usable
Oscillator status after reset	Stop	Oscillate	Stop	Oscillate	Stop (4) Oscillate (5)
Others	Externally generated clock can be input (2)	• Externally generated clock can be input • On-chip feedback resistor Rf (connected/ not connected selectable)	–	–	–

Notes:

1. These pins can be used as P12_0 and P12_1 when using the on-chip oscillator clock as the CPU clock while the XIN clock oscillation circuit and the XCIN clock oscillation circuit are not used.
2. To input an external clock, set the CM05 bit in the CM0 register to 1 (XIN clock stops), the CM11 bit in the CM1 register to 1 (on-chip feedback resistor enabled), and the CM13 bit to 1 (XIN-XOUT pin).
3. The clock frequency is set to up to 20 MHz by a divider when using the high-speed on-chip oscillator as the CPU clock source.
4. This applies when the CSPROINI bit in the OFS register is set to 1 (count source protection mode disabled after reset).
5. This applies when the CSPROINI bit in the OFS register is set to 0 (count source protection mode enabled after reset).

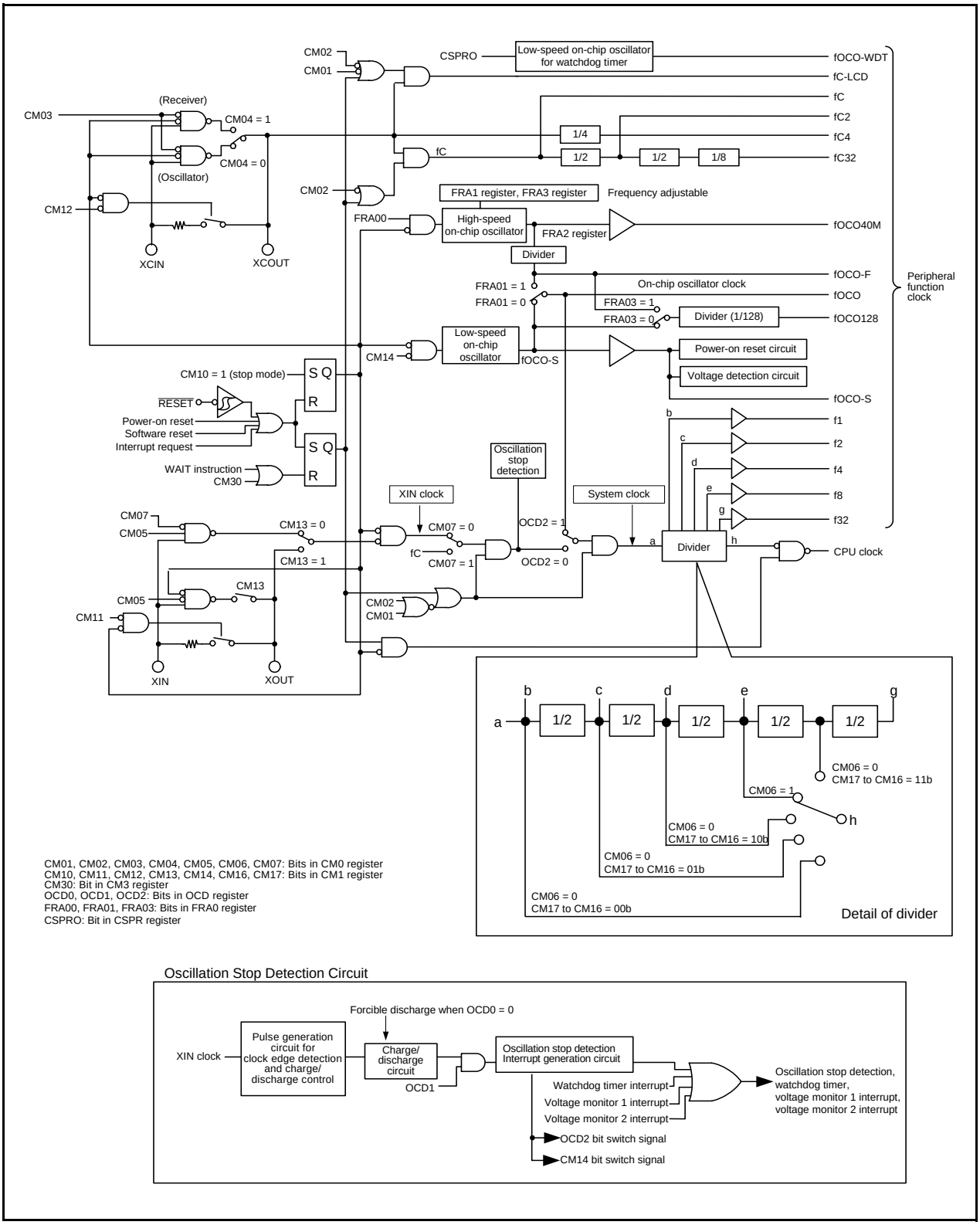


Figure 9.1 Clock Generation Circuit

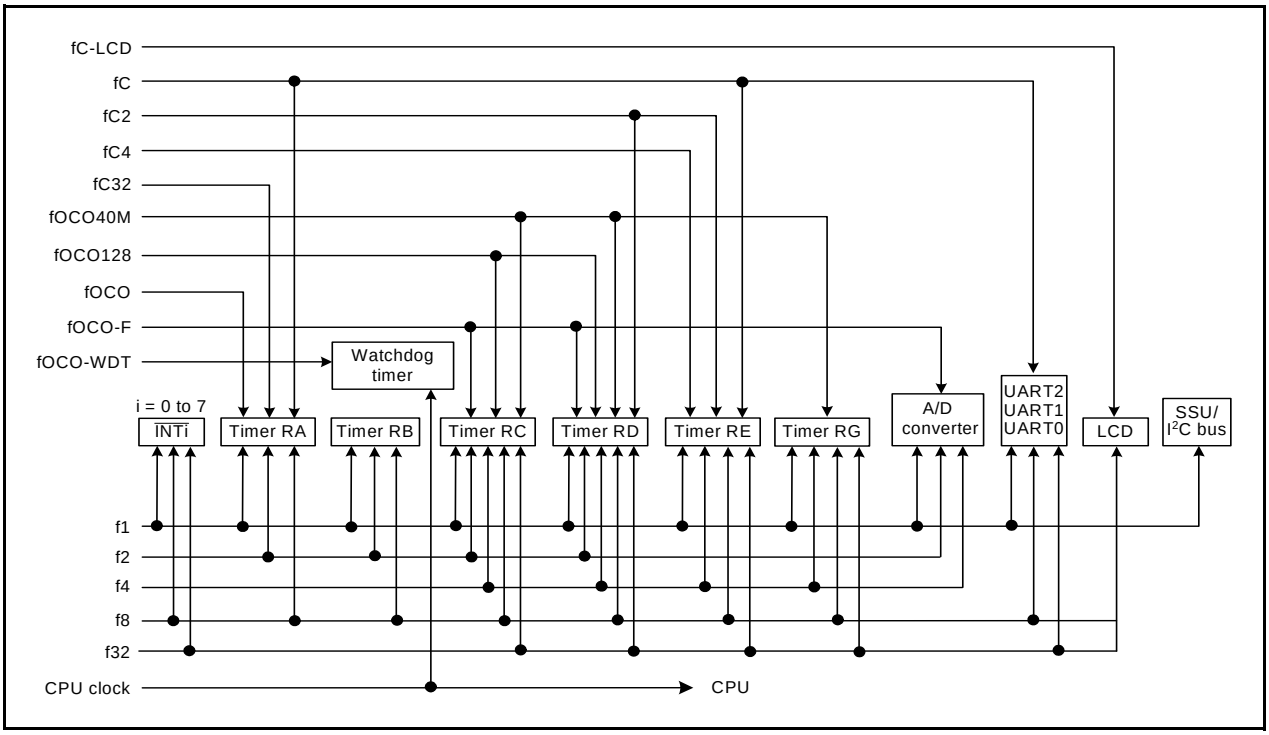


Figure 9.2 Peripheral Function Clock

9.2 Registers

9.2.1 System Clock Control Register 0 (CM0)

Address 0006h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM07	CM06	CM05	CM04	CM03	CM02	CM01	—
After Reset	0	0	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bit	Set to 0.	R/W
b1	CM01	Peripheral function clock stop bit in wait mode	b1 b0 0 0: Peripheral function clock does not stop in wait mode 0 1: Clocks f1 to f32 stop in wait mode 1 0: Clocks f1 to f32 and fC stop in wait mode 1 1: Clocks f1 to f32, fC, and fC-LCD stop in wait mode	R/W
b2	CM02			R/W
b3	CM03	XCIN clock stop bit	0: XCIN clock oscillates 1: XCIN clock stops	R/W
b4	CM04	XCIN external clock input enable bit	0: External clock input disabled 1: External clock input enabled	R/W
b5	CM05	XIN clock (XIN-XOUT) stop bit (1, 3)	0: XIN clock oscillates 1: XIN clock stops (2)	R/W
b6	CM06	System clock division select bit 0 (4)	0: Bits CM16 and CM17 in CM1 register enabled 1: Divide-by-8 mode	R/W
b7	CM07	XIN and XCIN clock select bit (5)	0: XIN clock 1: XCIN clock	R/W

Notes:
1. The CM05 bit stops the XIN clock when high-speed on-chip oscillator mode or low-speed on-chip oscillator mode is selected. This bit cannot be used to detect whether the XIN clock has stopped. To stop the XIN clock, set the bits in the following order:
   (a) Set bits OCD1 to OCD0 in the OCD register to 00b.
   (b) Set the OCD2 bit to 1 (on-chip oscillator clock selected).
2. During external clock input, only the clock oscillation buffer stops and clock input is acknowledged.
3. Only when the CM05 bit to 1 (XIN clock stops) and the CM07 bit is set to 1 (XCIN clock), P12_0 and P12_1 can be used as I/O ports.
4. When the MCU enters stop mode, the CM06 bit is set to 1 (divide-by-8 mode).
5. Change the CM07 bit from 0 to 1 (XCIN clock) after the XCIN clock oscillation has become stable.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM0 register.

9.2.2 System Clock Control Register 1 (CM1)

Address 0007h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM17	CM16	—	CM14	CM13	CM12	CM11	CM10
After Reset	0	0	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CM10	All clock stop control bit (2, 5)	0: Clock oscillates 1: All clocks stop (stop mode)	R/W
b1	CM11	XIN-XOUT on-chip feedback resistor select bit	0: On-chip feedback resistor enabled 1: On-chip feedback resistor disabled	R/W
b2	CM12	XCIN-XCOUT on-chip feedback resistor select bit	0: On-chip feedback resistor enabled 1: On-chip feedback resistor disabled	R/W
b3	CM13	Port/XIN-XOUT switch bit (5, 6, 7)	0: I/O ports P12_0 and P12_1 1: XIN-XOUT pin	R/W
b4	CM14	Low-speed on-chip oscillator oscillation stop bit (3, 4)	0: Low-speed on-chip oscillator on 1: Low-speed on-chip oscillator off	R/W
b5	—	Reserved bit	Set to 1.	R/W
b6	CM16	System clock division select bit 1 (1)	b7 b6 0 0: No division mode 0 1: Divide-by-2 mode 1 0: Divide-by-4 mode 1 1: Divide-by-16 mode	R/W
b7	CM17			R/W

Notes:
1. When the CM06 bit is set to 0, bits CM16 and CM17 are enabled.
2. When the CM10 bit is set to 1 (stop mode), the on-chip feedback resistor is disabled.
3. When the OCD2 bit is set to 0 (XIN clock selected), the CM14 bit can be set to 1 (low-speed on-chip oscillator off). When the OCD2 bit is set to 1 (on-chip oscillator clock selected), the CM14 bit is set to 0 (low-speed on-chip oscillator on). It remains unchanged even if 1 is written to it.
4. To use the voltage monitor 1 interrupt or voltage monitor 2 interrupt (when the digital filter is used), set the CM14 bit to 0 (low-speed on-chip oscillator on).
5. To use P12_0 and P12_1 as input ports, set the CM13 bit to 0 (I/O ports), the CM05 bit in the CM0 register to 1 (XIN clock stops), and the CM07 bit to 1 (XCIN clock).
   To use as external clock input, set the CM13 bit to 0 (I/O ports), the CM05 bit to 1 (XIN clock oscillates), the CM07 bit to 0 (XIN clock). When the PD12_0 bit in the PD12 register is further set to 0 (input mode), an external clock can be input. XOUT can be used as the input port P12_1 at this time.
6. When the CM10 bit is set to 1 (stop mode), the XOUT pin is held high while the CM13 bit is set to 1 (XIN-XOUT pin).
7. Once the CM13 bit is set to 1 by a program, it cannot be set to 0.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM1 register.

9.2.3 System Clock Control Register 3 (CM3)

Address 0009h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM37	CM36	CM35	—	—	—	—	CM30
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CM30	Wait control bit (1)	0: Other than wait mode 1: MCU enters wait mode	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—			
b4	—			
b5	CM35	CPU clock division ratio select bit when exiting wait mode	0: Following settings are enabled: CM06 bit in CM0 register Bits CM16 and CM17 in CM1 register 1: No division (2)	R/W
b6	CM36	CPU clock select bit when exiting wait or stop mode	b7 b6 0 0: MCU exits with the CPU clock used immediately before entering wait or stop mode 0 1: Do not set. 1 0: High-speed on-chip oscillator clock selected (3) 1 1: XIN clock selected (4)	R/W
b7	CM37			R/W

Notes:
1. When the MCU exits wait mode by a peripheral function interrupt, the CM30 bit is set to 0 (other than wait mode).
2. Set the CM35 bit to 0 in stop mode. When the MCU enters wait mode, if the CM35 bit is set to 1 (no division), the CM06 bit in the CM0 register is set to 0 (bits CM16 and CM17 enabled) and bits CM17 and CM16 in the CM1 register is set to 00b (no division mode).
3. When bits CM37 to CM36 are set to 10b (high-speed on-chip oscillator clock selected), the following will be set when the MCU exits wait mode or stop mode:
   • OCD2 bit in OCD register = 1 (on-chip oscillator selected)
   • FRA00 bit in FRA0 register = 1 (high-speed on-chip oscillator on)
   • FRA01 bit in FRA0 register = 1 (high-speed on-chip oscillator selected)
4. When bits CM37 to CM36 are set to 11b (XIN clock selected), the following will be set when the MCU exits wait mode or stop mode.
   • OM05 bit in OM0 register = 1 (XIN clock oscillates)
   • OM13 bit in OM1 register = 1 (XIN-XOUT pin)
   • OCD2 bit in OCD register = 0 (XIN clock selected)

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM3 register.

CM30 bit (Wait Control Bit)

When the CM30 bit is set to 1 (MCU enters wait mode), the CPU clock stops (wait mode). However, the XIN clock, XCIN clock, and on-chip oscillator clock do not stop, so peripheral functions using these clocks continue operating.

The MCU exits wait mode by a reset or peripheral function interrupt. If the MCU enters wait mode while the I flag is set to 0 (maskable interrupt disabled), it resumes executing the instruction immediately after the instruction to set the CM30 bit to 1 when exiting wait mode. If the MCU enters wait mode with the WAIT instruction, interrupt handling is performed by the CPU when exiting wait mode.

9.2.4 Oscillation Stop Detection Register (OCD)

Address 000Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	OCD3	OCD2	OCD1	OCD0
After Reset	0	0	0	0	0	1	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	OCD0	Oscillation stop detection enable bit (6)	0: Oscillation stop detection function disabled (1) 1: Oscillation stop detection function enabled	R/W
b1	OCD1	Oscillation stop detection interrupt enable bit	0: Disabled (1) 1: Enabled	R/W
b2	OCD2	System clock select bit (3)	0: XIN clock selected (6) 1: On-chip oscillator clock selected (2)	R/W
b3	OCD3	Clock monitor bit (4, 5)	0: XIN clock oscillates 1: XIN clock stops	R
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

Notes:
1. Set bits OCD1 to OCD0 to 00b before the MCU enters stop mode, high-speed on-chip oscillator mode, or low-speed on-chip oscillator mode (XIN clock stops).
2. When the OCD2 bit is set to 1 (on-chip oscillator clock selected), the CM14 bit is set to 0 (low-speed on-chip oscillator on).
3. The OCD2 bit is automatically set to 1 (on-chip oscillator clock selected) when the XIN clock oscillation stop is detected while bits OCD1 to OCD0 are set to 11b. When the OCD3 bit is set to 1 (XIN clock stops), the OCD2 bit remains unchanged even if 0 (XIN clock selected) is written to it.
4. The OCD3 bit is enabled when the OCD0 bit is set to 1 (oscillation stop detection function enabled).
5. The OCD3 bit remains 0 (XIN clock oscillates) when bits OCD1 to OCD0 are set to 00b.
6. Refer to **9.7.1 How to Use Oscillation Stop Detection Function** for the switching procedure when the XIN clock re-oscillates after detecting an oscillation stop.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the OCD register.

9.2.5 High-Speed On-Chip Oscillator Control Register 7 (FRA7)

Address 0015h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	When shipping							

Bit	Function	R/W
b7-b0	32 MHz frequency correction data is stored. The frequency can be adjusted by transferring this value to the FRA3 register and by transferring the correction value of the FRA6 register to the FRA1 register.	R

9.2.6 High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Address 0023h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	FRA03	—	FRA01	FRA00
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FRA00	High-speed on-chip oscillator enable bit	0: High-speed on-chip oscillator off 1: High-speed on-chip oscillator on	R/W
b1	FRA01	High-speed on-chip oscillator select bit (1)	0: Low-speed on-chip oscillator selected (2) 1: High-speed on-chip oscillator selected	R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	FRA03	fOCO128 clock select bit	0: fOCO-S divided by 128 selected 1: fOCO-F divided by 128 selected	R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

Notes:
1. Change the FRA01 bit under the following conditions.
   - FRA00 = 1 (high-speed on-chip oscillator on)
   - CM14 bit in CM1 register = 0 (low-speed on-chip oscillator on)
   - Bits FRA22 to FRA20 in the FRA2 register:
     All division mode can be set when VCC = 3.0 V to 5.5 V 000b to 111b
     Division ratio of 4 or more when VCC = 2.7 V to 5.5 V 010b to 111b (divide-by-4 or more)
     Division ratio of 8 or more when VCC = 2.2 V to 5.5 V 110b to 111b (divide-by-8 or more)
2. When setting the FRA01 bit to 0 (low-speed on-chip oscillator selected), do not set the FRA00 bit to 0 (high-speed on-chip oscillator off) at the same time. Set the FRA01 bit to 0 before setting the FRA00 bit to 0.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRA0 register.

9.2.7 High-Speed On-Chip Oscillator Control Register 1 (FRA1)

Address 0024h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	When shipping							

Bit	Function	R/W
b7-b0	The frequency of the high-speed on-chip oscillator can be changed by the following settings. 40 MHz: FRA1=FRA3=Value after a reset 36.864 MHz: Transfer the data of the FRA4 register to the FRA1 register, and transfer the data of the FRA5 register to the FRA3 register. 32 MHz: Transfer the data of the FRA6 register to the FRA1 register, and transfer the data of the FRA7 register to the FRA3 register.	R/W

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRA1 register.

9.2.8 High-Speed On-Chip Oscillator Control Register 2 (FRA2)

Address 0025h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	FRA22	FRA21	FRA20
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FRA20	High-speed on-chip oscillator frequency switch bit	Division ratio selection These bits select the division ratio for the high-speed on-chip oscillator clock. b2 b1 b0 0 0 0: Divide-by-2 mode 0 0 1: Divide-by-3 mode 0 1 0: Divide-by-4 mode 0 1 1: Divide-by-5 mode 1 0 0: Divide-by-6 mode 1 0 1: Divide-by-7 mode 1 1 0: Divide-by-8 mode 1 1 1: Divide-by-9 mode	R/W
b1	FRA21			R/W
b2	FRA22			R/W
b3	—	Reserved bits	Set to 0.	R/W
b4	—			
b5	—			
b6	—			
b7	—			

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRA2 register.

9.2.9 High-Speed On-Chip Oscillator Control Register 4 (FRA4)

Address 0029h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	When shipping							

Bit	Function	R/W
b7-b0	36.864 MHz frequency correction data is stored. The frequency can be adjusted by transferring this value to the FRA1 register and by transferring the correction value of the FRA5 register to the FRA3 register.	R

9.2.10 High-Speed On-Chip Oscillator Control Register 5 (FRA5)

Address 002Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	When shipping							

Bit	Function	R/W
b7-b0	36.864 MHz frequency correction data is stored. The frequency can be adjusted by transferring this value to the FRA3 register and by transferring the correction value of the FRA4 register to the FRA1 register.	R

9.2.11 High-Speed On-Chip Oscillator Control Register 6 (FRA6)

Address 002Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	When shipping							

Bit	Function	R/W
b7-b0	32 MHz frequency correction data is stored. The frequency can be adjusted by transferring this value to the FRA1 register and by transferring the correction value of the FRA7 register to the FRA3 register.	R

9.2.12 High-Speed On-Chip Oscillator Control Register 3 (FRA3)

Address 002Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	When shipping							

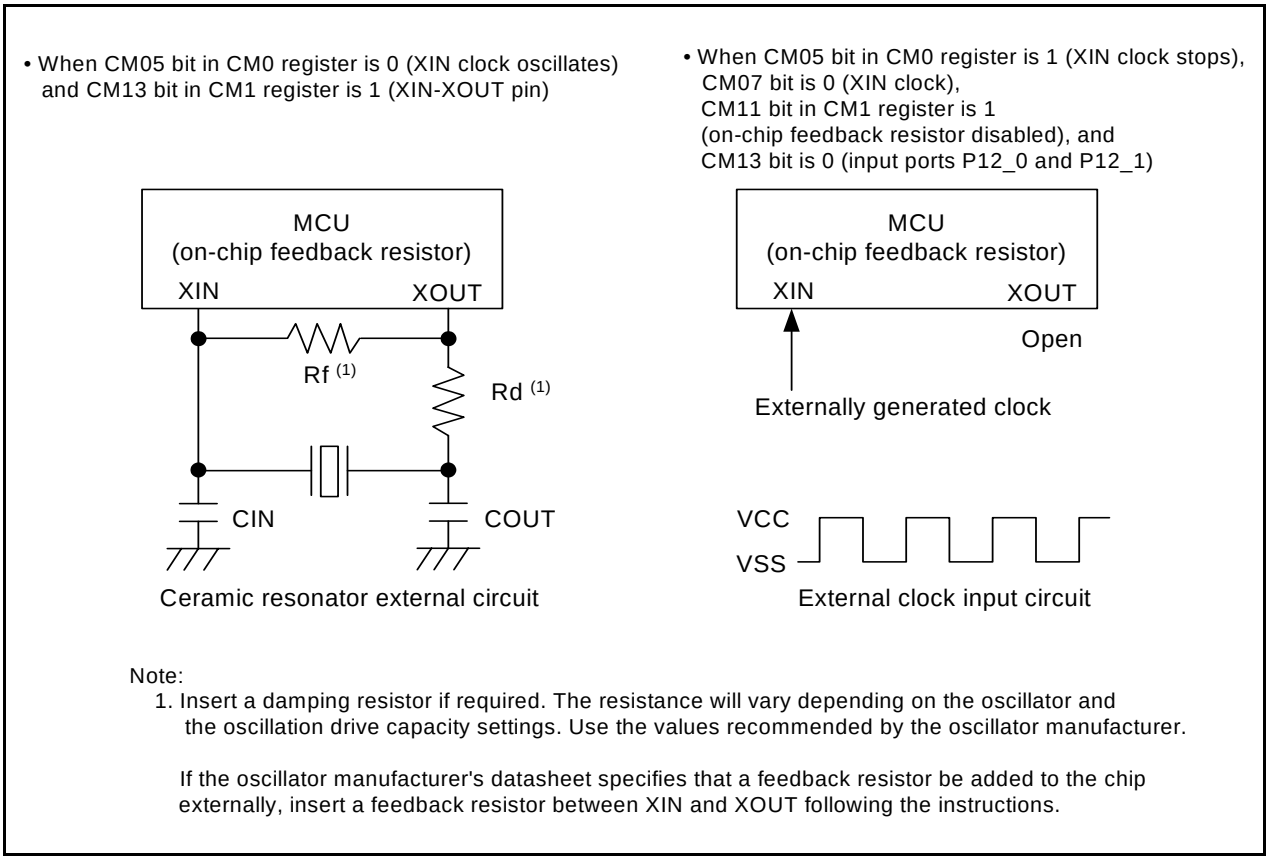
Bit	Function	R/W
b7-b0	The frequency of the high-speed on-chip oscillator can be changed by the following settings. 40 MHz: FRA1=FRA3=Value after a reset 36.864 MHz: Transfer the data of the FRA4 register to the FRA1 register, and transfer the data of the FRA5 register to the FRA3 register. 32 MHz: Transfer the data of the FRA6 register to the FRA1 register, and transfer the data of the FRA7 register to the FRA3 register.	R/W

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRA3 register.

The clocks generated by the clock generation circuits are described below.

9.3 XIN Clock

The XIN clock is supplied by the XIN clock oscillation circuit. This clock is used as the clock source for the CPU and peripheral function clocks. The XIN clock oscillation circuit is configured by connecting a resonator between pins XIN and XOUT. The XIN clock oscillation circuit includes an on-chip feedback resistor, which is disconnected from the oscillation circuit in stop mode in order to reduce the amount of power consumed by the chip. The XIN clock oscillation circuit may also be configured by feeding an externally generated clock to the XOUT pin.
Figure 9.3 shows Examples of XIN Clock Connection Circuit.
During and after reset, the XIN clock stops.
After setting the CM13 bit in the CM1 register to 1 (XIN-XOUT pin), the XIN clock starts oscillating when the CM05 bit in the CM0 register is set to 0 (XIN clock oscillates).
After the XIN clock oscillation stabilizes, the XIN clock is used as the CPU clock source by setting the OCD2 bit in the OCD register to 0 (XIN clock selected).
The power consumption can be reduced by setting the CM05 bit in the CM0 register to 1 (XIN clock stops) by setting the OCD2 bit is to 1 (on-chip oscillator clock selected).
In stop mode, all clocks including the XIN clock stop. Refer to **10. Power Control** for details.



Note:
1. Insert a damping resistor if required. The resistance will vary depending on the oscillator and the oscillation drive capacity settings. Use the values recommended by the oscillator manufacturer.

If the oscillator manufacturer's datasheet specifies that a feedback resistor be added to the chip externally, insert a feedback resistor between XIN and XOUT following the instructions.

Figure 9.3 Examples of XIN Clock Connection Circuit

9.4 On-Chip Oscillator Clock

The on-chip oscillator clock is supplied by the on-chip oscillator (high-speed on-chip oscillator or low-speed on-chip oscillator). This clock is selected by the FRA01 bit in the FRA0 register.

9.4.1 Low-Speed On-Chip Oscillator Clock

The clock generated by the low-speed on-chip oscillator is used as the clock source for the CPU clock, and peripheral function clock (fOCO, fOCO-S, and fOCO128).
After a reset, the on-chip oscillator clock generated by the low-speed on-chip oscillator divided by 1 (no division) is selected as the CPU clock.
If the XIN clock stops oscillating when bits OCD1 to OCD0 in the OCD register are set to 11b, the low-speed on-chip oscillator automatically starts operating and supplies the necessary clock for the MCU.
The frequency of the low-speed on-chip oscillator varies depending on the supply voltage and the operating ambient temperature. Application products must be designed with sufficient margin to allow for frequency changes.

9.4.2 High-Speed On-Chip Oscillator Clock

The clock generated by the high-speed on-chip oscillator is used as the clock source for the CPU clock, and peripheral function clock (fOCO, fOCO-F, fOCO40M, and fOCO128).
To use the high-speed on-chip oscillator clock as the clock source for the CPU clock, peripheral clock, fOCO, and fOCO-F, set bits FRA20 to FRA22 in the FRA2 register as follows:

- All division mode can be set when VCC = 3.0 V to 5.5 V — 000b to 111b
- Division ratio of 4 or more when VCC = 2.7 V to 5.5 V — 010b to 111b (divide-by-4 or more)
- Division ratio of 8 or more when VCC = 2.2 V to 5.5 V — 110b to 111b (divide-by-8 or more)

After a reset, the on-chip oscillator clock generated by the high-speed on-chip oscillator stops. Oscillation is started by setting the FRA00 bit in the FRA0 register to 1 (high-speed on-chip oscillator on).

Frequency correction data is stored in registers FRA4 to FRA7.
To adjust the frequency of the high-speed on-chip oscillator clock to 36.864 MHz, first transfer the correction value of the FRA4 register to the FRA1 register and the correction value of the FRA5 register to the FRA3 register before using the values. This enables the setting errors of bit rates such as 9,600 bps and 38,400 bps to be 0% when the serial interface is used in UART mode (refer to **Table 24.8** and **Table 25.8 Bit Rate Setting Example in UART Mode (Internal Clock Selected)**).
To adjust the frequency of the high-speed on-chip oscillator clock to 32 MHz, first transfer the correction value of the FRA6 register to the FRA1 register and the correction value of the FRA7 register to the FRA3 register before using the values.

9.5 XCIN Clock

The XCIN clock is supplied by the XCIN clock oscillation circuit. This clock is used as the clock source for the CPU and peripheral function clocks. The XCIN clock oscillation circuit is configured by connecting a resonator between pins XCIN and XCOUT. The XCIN clock oscillation circuit includes an on-chip a feedback resistor, which is disconnected from the oscillation circuit in stop mode in order to reduce the amount of power consumed by the chip. The XCIN clock oscillation circuit may also be configured by feeding an externally generated clock to the XCIN pin.

Figure 9.4 shows Examples of XCIN Clock Connection Circuits.

Bits CM04 to CM03 in the CM0 register are set to 00b (external clock input disabled, XCIN clock oscillates) by reset and the XCIN clock starts oscillating (with the on-chip feedback resistor enabled). After the XCIN clock oscillation stabilizes following reset, the XCIN clock is used as the CPU clock source by setting the CM07 bit in the CM07 register to 1 (XCIN clock).

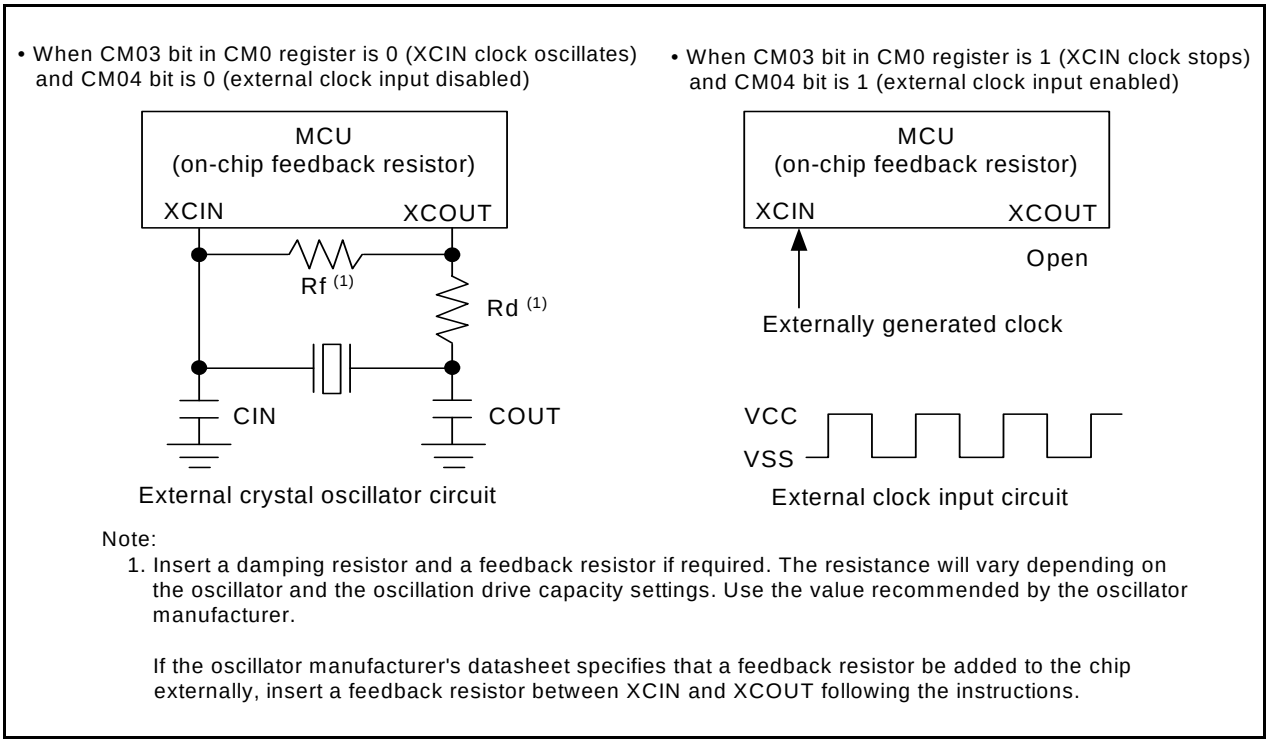
When the CM03 bit is set to 1 (XCIN clock stops), the XCIN clock stops.

When bits CM04 to CM03 are set to 10b (external clock input enabled, XCIN clock oscillates), an externally generated clock can also be input to the XCIN pin. Leave the XCOUT pin open at this time.

This MCU has an on-chip feedback resistor, which can be disabled/enabled by the CM12 bit in the CM1 register.

When the XCIN clock is not used, set bits CM04 to CM03 to 01b (external clock input disabled, XCIN clock stops) and the CM12 bit to 1 (on-chip feedback resistor disabled).

In stop mode, all clocks including the XCIN clock stop. Refer to **10. Power Control** for details.



Note:
1. Insert a damping resistor and a feedback resistor if required. The resistance will vary depending on the oscillator and the oscillation drive capacity settings. Use the value recommended by the oscillator manufacturer.

   If the oscillator manufacturer's datasheet specifies that a feedback resistor be added to the chip externally, insert a feedback resistor between XCIN and XCOUT following the instructions.

Figure 9.4 Examples of XCIN Clock Connection Circuits

9.6 CPU Clock and Peripheral Function Clock

There are a CPU clock to operate the CPU and a peripheral function clock to operate the peripheral functions. (Refer to **Figure 9.1 Clock Generation Circuit**.)

9.6.1 System Clock

The system clock is the clock source for the CPU and peripheral function clocks. The XIN clock, XCIN clock, or on-chip oscillator clock can be selected.

9.6.2 CPU Clock

The CPU clock is an operating clock for the CPU and the watchdog timer.
The system clock divided by 1 (no division), 2, 4, 8, or 16 is used as the CPU clock. The division ratio can be selected by the CM06 bit in the CM0 register and bits CM16 and CM17 in the CM1 register.
Use the XCIN clock while the XCIN clock oscillation stabilizes.
After a reset, the low-speed on-chip oscillator clock divided by 1 (no division) is used as the CPU clock.
When the MCU enters stop mode, the CM06 bit is set to 1 (divide-by-8 mode). To enter stop mode, set the CM35 bit in the CM3 register to 0 (settings of CM06 in CM0 register and bits CM16 and CM17 in CM1 register enabled).

9.6.3 Peripheral Function Clock (f1, f2, f4, f8, and f32)

The peripheral function clock is an operating clock for the peripheral functions.
The fi (i = 1, 2, 4, 8, and 32) clock is generated by the system clock divided by i. It is used for timers RA, RB, RC, RD, RE, RG, the serial interface, the A/D converter, and the LCD waveform control circuit.
When the MCU enters wait mode after bits CM02 to CM01 in the CM0 register are set to 01, 10, or 11, the fi clock stops.

9.6.4 fOCO

fOCO is an operating clock for the peripheral functions.
This clock runs at the same frequency as the on-chip oscillator clock and can be used as the source for timer RA.
In wait mode, the fOCO clock does not stop.

9.6.5 fOCO40M

fOCO40M is used as the count source for timers RC, RD, and RG.
This clock is generated by the high-speed on-chip oscillator and supplied by setting the FRA00 bit to 1.
In wait mode, the fOCO40M clock does not stop.
This clock can be used with supply voltage VCC = 3.0 to 5.5 V.

9.6.6 fOCO-F

fOCO-F is used as the count source for timers RC and RD, and the A/D converter.
This clock is generated by the high-speed on-chip oscillator, divided by i (i = 2, 3, 4, 5, 6, 7, 8, or 9; division ratio selected by the FRA2 register). It is supplied by setting the FRA00 bit to 1.
In wait mode, the fOCO-F clock does not stop.

9.6.7 fOCO-S

fOCO-S is an operating clock for the voltage detection circuit.
This clock is generated by the low-speed on-chip oscillator and supplied by setting the CM14 bit to 0 (low-speed on-chip oscillator on).
In wait mode, the fOCO-S clock does not stop.

9.6.8 fOCO128

fOCO128 clock is generated by fOCO-S or fOCO-E divided by 128. fOCO-S divided by 128 is selected by setting the FRA03 bit to 0 and fOCO-F divided by 128 is selected by setting the FRA03 bit to 1.
fOCO128 is configured as the capture signal used in the TRCGRA register for timer RC and timer RD0 for timer RD.

9.6.9 fC-LCD

fC-LCD is used in the LCD waveform control circuit.
Use this clock only while the XCIN clock oscillation stabilizes.

9.6.10 fC, fC2, fC4, and fC32

fC, fC2, fC4, and fC32 are used for timers RA, RD, RE and the serial interface.
Use theses clocks while the XCIN clock oscillation stabilizes.

9.6.11 fOCO-WDT

fOCO-WDT is an operating clock for the watchdog timer.
This clock is generated by the low-speed on-chip oscillator for the watchdog timer and supplied by setting the CSPRO bit in the CSPR register to 1 (count source protection mode enabled).
In count source protection mode for the watchdog timer, the fOCO-WDT clock does not stop.

9.7 Oscillation Stop Detection Function

The oscillation stop detection function detects the stop of the XIN clock oscillating circuit.
The oscillation stop detection function can be enabled and disabled by the OCD0 bit in the OCD register.
Table 9.2 lists the Specifications of Oscillation Stop Detection Function.

When the XIN clock is the CPU clock source and bits OCD1 to OCD0 are set to 11b, the MCU is placed in the following states if the XIN clock stops.

- OCD2 bit in OCD register = 1 (on-chip oscillator clock selected)
- OCD3 bit in OCD register = 1 (XIN clock stops)
- CM14 bit in CM1 register = 0 (low-speed on-chip oscillator on)
- Oscillation stop detection interrupt request is generated

Table 9.2 Specifications of Oscillation Stop Detection Function

Item	Specification
Oscillation stop detection clock and frequency bandwidth	f(XIN) ≥ 2 MHz
Condition for enabling the oscillation stop detection function	Bits OCD1 to OCD0 are set to 11b.
Operation at oscillation stop detection	Oscillation stop detection interrupt generation

9.7.1 How to Use Oscillation Stop Detection Function

- The oscillation stop detection interrupt shares a vector with the voltage monitor 1 interrupt, the voltage monitor 2 interrupt, and the watchdog timer interrupt. To use the oscillation stop detection interrupt and watchdog timer interrupt, the interrupt source needs to be determined.
  Table 9.3 lists the Determination of Interrupt Sources for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, or Voltage Monitor 2 Interrupt. Figure 9.6 shows an Example of Determining Interrupt Sources for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, or Voltage Monitor 2 Interrupt.
- When the XIN clock restarts after oscillation stop, switch the XIN clock to the clock source for the CPU clock and the peripheral functions by a program.
  Figure 9.5 shows the Procedure for Switching Low-Speed On-Chip Oscillator to XIN Clock.
- To enter wait mode while the oscillation stop detection function is used, set bits CM02 to CM1 to 00 (peripheral function clock does not stop in wait mode).
- Since the oscillation stop detection function is a function for cases where the XIN clock is stopped by an external cause, set bits OCD1 to OCD0 to 00b to stop or start the XIN clock by a program (select stop mode or change the CM05 bit).
- This function cannot be used when the XIN clock frequency is below 2 MHz. In this case, set bits OCD1 to OCD0 to 00b.
- To use the low-speed on-chip oscillator clock as the clock source for the CPU clock and the peripheral functions after detecting the oscillation stop, set the FRA01 bit in the FRA0 register to 0 (low-speed on-chip oscillator selected) and then bits OCD1 to OCD0 to 11b.
  To use the high-speed on-chip oscillator clock as the clock source for the CPU clock and the peripheral functions after detecting the oscillation stop, first set the FRA00 bit to 1 (high-speed on-chip oscillator on) and the FRA01 bit to 1 (high-speed on-chip oscillator selected). Then set bits OCD1 to OCD0 to 11b.

Table 9.3 Determination of Interrupt Sources for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, or Voltage Monitor 2 Interrupt

Generated Interrupt Source	Bit Indicating Interrupt Source
Oscillation stop detection (when (a) or (b))	(a) OCD3 bit in OCD register = 1
	(b) Bits OCD1 to OCD0 in OCD register = 11b and OCD2 bit = 1
Watchdog timer	VW2C3 bit in VW2C register = 1
Voltage monitor 1	VW1C2 bit in VW1C register = 1
Voltage monitor 2	VW2C2 bit in VW2C register = 1

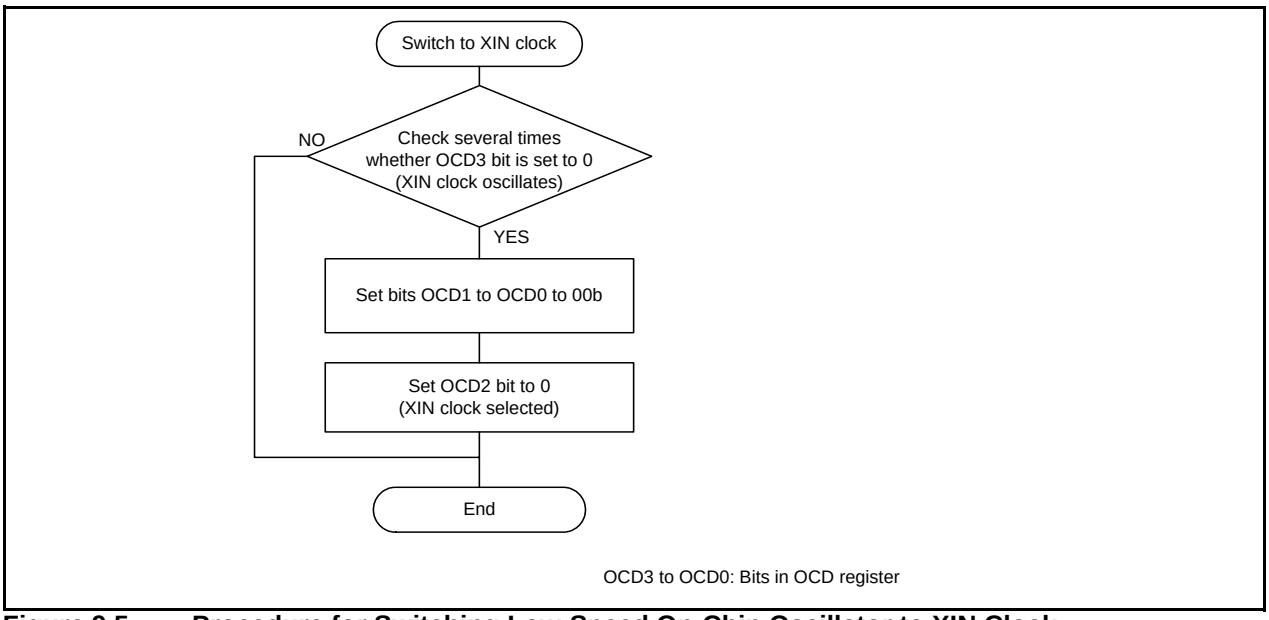


Figure 9.5 Procedure for Switching Low-Speed On-Chip Oscillator to XIN Clock

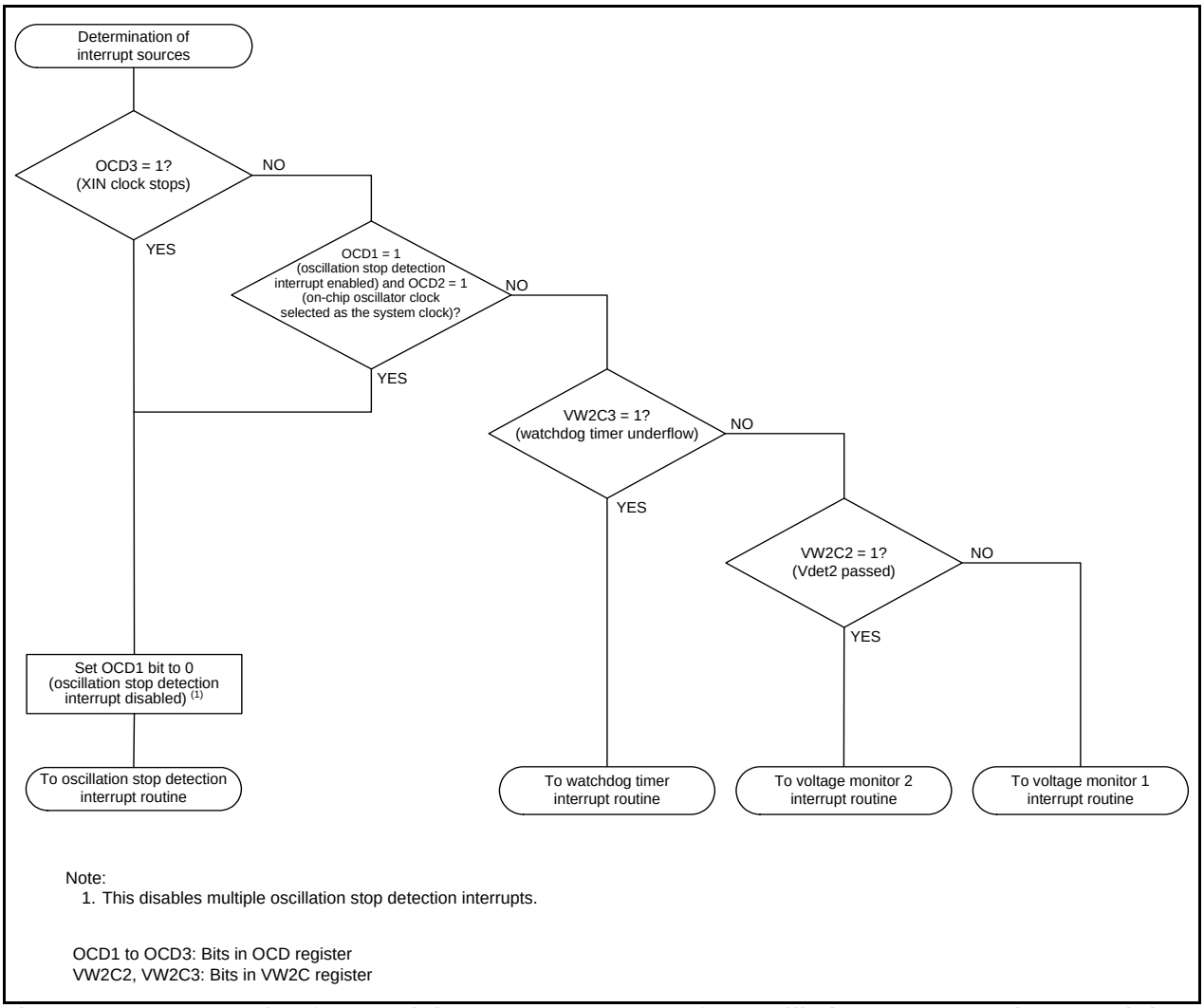


Figure 9.6 Example of Determining Interrupt Sources for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, or Voltage Monitor 2 Interrupt

9.8 Notes on Clock Generation Circuit

9.8.1 Oscillation Stop Detection Function

Since the oscillation stop detection function cannot be used when the XIN clock frequency is below 2 MHz, set bits OCD1 to OCD0 to 00b.

9.8.2 Oscillation Circuit Constants

Consult the oscillator manufacturer to determine the optimal oscillation circuit constants for the user system. To use the MCU with supply voltage below VCC = 2.7 V, it is recommended to set the CM11 bit in the CM1 register to 1 (on-chip feedback resistor disabled) and connect the feedback resistor to the chip externally.

10. Power Control

There are four power control modes. All modes other than wait mode, stop mode, and power-off mode are referred to as standard operating mode.

10.1 Introduction

Table 10.1 lists each mode. Figure 10.1 shows the State Transitions in Power Control Mode.

Table 10.1 Power Control

Mode		Operation
Standard operating mode	High-speed clock	The CPU and peripheral functions operate.
	High-speed on-chip oscillator	
	Low-speed clock	The CPU and peripheral functions operate.
	Low-speed on-chip oscillator	
Wait mode		The CPU stops and peripheral functions operate.
Stop mode		The CPU and peripheral functions stop (oscillation stops).
Power-off mode		Functions other than the low-speed clock and timer RE stop or all functions stop.

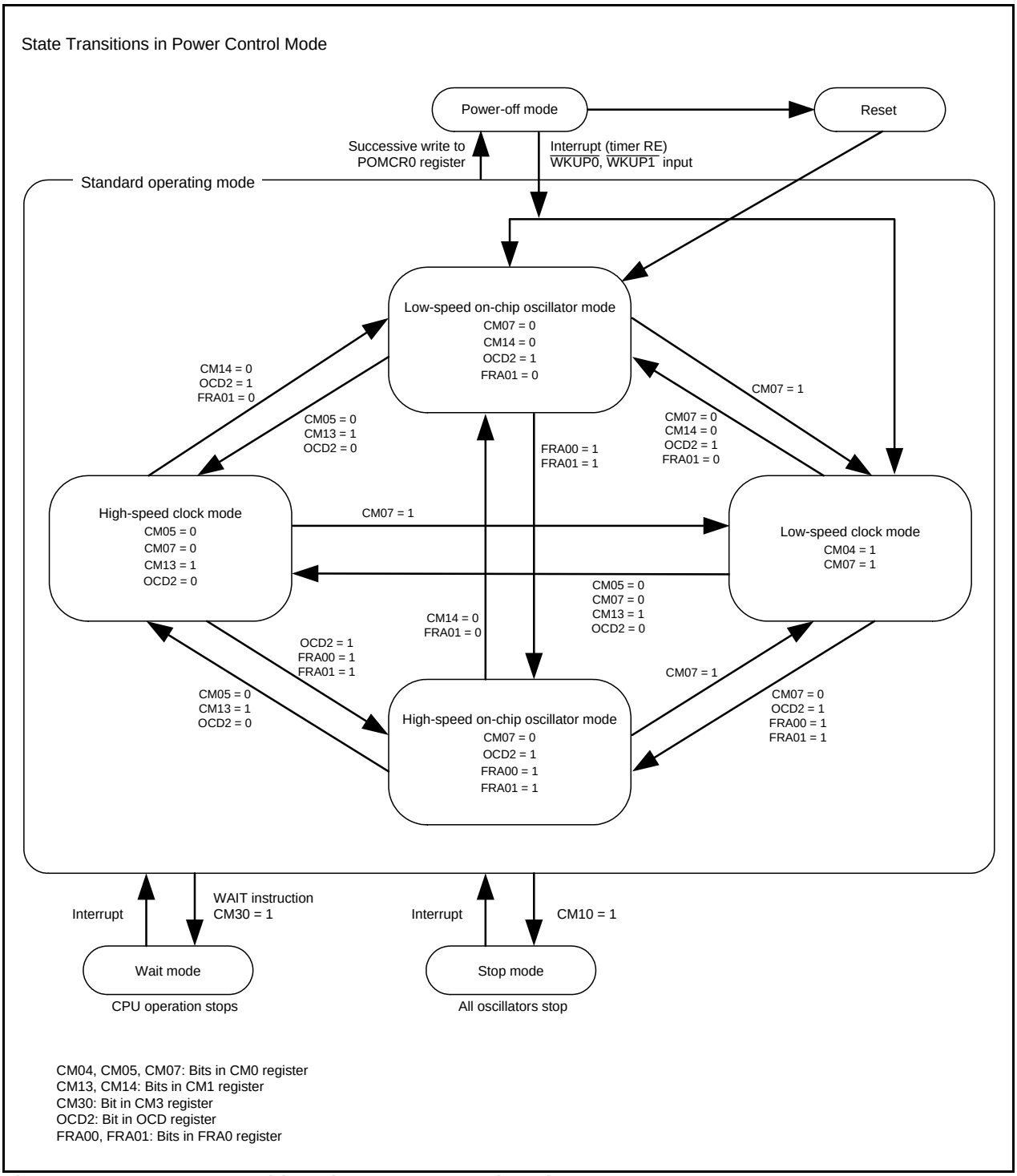


Figure 10.1 State Transitions in Power Control Mode

10.2 Registers

10.2.1 System Clock Control Register 0 (CM0)

Address 0006h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM07	CM06	CM05	CM04	CM03	CM02	CM01	—
After Reset	0	0	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bit	Set to 0.	R/W
b1	CM01	Peripheral function clock stop bit in wait mode	b1 b0 0 0: Peripheral function clock does not stop in wait mode 0 1: Clocks f1 to f32 stop in wait mode 1 0: Clocks f1 to f32 and fC stop in wait mode 1 1: Clocks f1 to f32, fC, and fC-LCD stop in wait mode	R/W
b2	CM02			R/W
b3	CM03	XCIN clock stop bit	0: XCIN clock oscillates 1: XCIN clock stops	R/W
b4	CM04	XCIN external clock input enable bit	0: External clock input disabled 1: External clock input enabled	R/W
b5	CM05	XIN clock (XIN-XOUT) stop bit (1, 3)	0: XIN clock oscillates 1: XIN clock stops (2)	R/W
b6	CM06	System clock division select bit 0 (4)	0: Bits CM16 and CM17 in CM1 register enabled 1: Divide-by-8 mode	R/W
b7	CM07	XIN and XCIN clock select bit (5)	0: XIN clock 1: XCIN clock	R/W

Notes:
1. The CM05 bit stops the XIN clock when high-speed on-chip oscillator mode or low-speed on-chip oscillator mode is selected. This bit cannot be used to detect whether the XIN clock has stopped. To stop the XIN clock, set the bits in the following order:
   (a) Set bits OCD1 to OCD0 in the OCD register to 00b.
   (b) Set the OCD2 bit to 1 (on-chip oscillator clock selected).
2. During external clock input, only the clock oscillation buffer stops and clock input is acknowledged.
3. Only when the CM05 bit to 1 (XIN clock stops) and the CM07 bit is set to 1 (XCIN clock), P12_0 and P12_1 can be used as I/O ports.
4. When the MCU enters stop mode, the CM06 bit is set to 1 (divide-by-8 mode).
5. Change the CM07 bit from 0 to 1 (XCIN clock) after the XCIN clock oscillation has become stable.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM0 register.

10.2.2 System Clock Control Register 1 (CM1)

Address 0007h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM17	CM16	—	CM14	CM13	CM12	CM11	CM10
After Reset	0	0	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CM10	All clock stop control bit (2, 5)	0: Clock oscillates 1: All clocks stop (stop mode)	R/W
b1	CM11	XIN-XOUT on-chip feedback resistor select bit	0: On-chip feedback resistor enabled 1: On-chip feedback resistor disabled	R/W
b2	CM12	XCIN-XCOUT on-chip feedback resistor select bit	0: On-chip feedback resistor enabled 1: On-chip feedback resistor disabled	R/W
b3	CM13	Port/XIN-XOUT switch bit (5, 6, 7)	0: I/O ports P12_0 and P12_1 1: XIN-XOUT pin	R/W
b4	CM14	Low-speed on-chip oscillator oscillation stop bit (3, 4)	0: Low-speed on-chip oscillator on 1: Low-speed on-chip oscillator off	R/W
b5	—	Reserved bit	Set to 1.	R/W
b6	CM16	System clock division select bit 1 (1)	b7 b6 0 0: No division mode 0 1: Divide-by-2 mode 1 0: Divide-by-4 mode 1 1: Divide-by-16 mode	R/W
b7	CM17			R/W

Notes:
1. When the CM06 bit is set to 0, bits CM16 and CM17 are enabled.
2. When the CM10 bit is set to 1 (stop mode), the on-chip feedback resistor is disabled.
3. When the OCD2 bit is set to 0 (XIN clock selected), the CM14 bit can be set to 1 (low-speed on-chip oscillator off). When the OCD2 bit is set to 1 (on-chip oscillator clock selected), the CM14 bit is set to 0 (low-speed on-chip oscillator on). It remains unchanged even if 1 is written to it.
4. To use the voltage monitor 1 interrupt or voltage monitor 2 interrupt (when the digital filter is used), set the CM14 bit to 0 (low-speed on-chip oscillator on).
5. To use P12_0 and P12_1 as input ports, set the CM13 bit to 0 (I/O ports), the CM05 bit in the CM0 register to 1 (XIN clock stops), and the CM07 bit to 1 (XCIN clock).
   To use as external clock input, set the CM13 bit to 0 (I/O ports), the CM05 bit to 1 (XIN clock oscillates), the CM07 bit to 0 (XIN clock). When the PD12_0 bit in the PD12 register is further set to 0 (input mode), an external clock can be input. XOUT can be used as the input port P12_1 at this time.
6. When the CM10 bit is set to 1 (stop mode), the XOUT pin is held high while the CM13 bit is set to 1 (XIN-XOUT pin).
7. Once the CM13 bit is set to 1 by a program, it cannot be set to 0.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM1 register.

10.2.3 System Clock Control Register 3 (CM3)

Address 0009h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM37	CM36	CM35	—	—	—	—	CM30
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CM30	Wait control bit (1)	0: Other than wait mode 1: MCU enters wait mode	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—			
b4	—			
b5	CM35	CPU clock division ratio select bit when exiting wait mode	0: Following settings are enabled: CM06 bit in CM0 register Bits CM16 and CM17 in CM1 register 1: No division (2)	R/W
b6	CM36	CPU clock select bit when exiting wait or stop mode	b7 b6 0 0: MCU exits with the CPU clock used immediately before entering wait or stop mode 0 1: Do not set. 1 0: High-speed on-chip oscillator clock selected (3) 1 1: XIN clock selected (4)	R/W
b7	CM37			R/W

Notes:
1. When the MCU exits wait mode by a peripheral function interrupt, the CM30 bit is set to 0 (other than wait mode).
2. Set the CM35 bit to 0 in stop mode. When the MCU enters wait mode, if the CM35 bit is set to 1 (no division), the CM06 bit in the CM0 register is set to 0 (bits CM16 and CM17 enabled) and bits CM17 and CM16 in the CM1 register is set to 00b (no division mode).
3. When bits CM37 to CM36 are set to 10b (high-speed on-chip oscillator clock selected), the following will be set when the MCU exits wait mode or stop mode:
   • OCD2 bit in OCD register = 1 (on-chip oscillator selected)
   • FRA00 bit in FRA0 register = 1 (high-speed on-chip oscillator on)
   • FRA01 bit in FRA0 register = 1 (high-speed on-chip oscillator selected)
4. When bits CM37 to CM36 are set to 11b (XIN clock selected), the following will be set when the MCU exits wait mode or stop mode.
   • OM05 bit in OM0 register = 1 (XIN clock oscillates)
   • OM13 bit in OM1 register = 1 (XIN-XOUT pin)
   • OCD2 bit in OCD register = 0 (XIN clock selected)

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM3 register.

CM30 bit (Wait Control Bit)

When the CM30 bit is set to 1 (MCU enters wait mode), the CPU clock stops (wait mode). However, the XIN clock, XCIN clock, and on-chip oscillator clock do not stop, so peripheral functions using these clocks continue operating.

The MCU exits wait mode by a reset or peripheral function interrupt. If the MCU enters wait mode while the I flag is set to 0 (maskable interrupt disabled), it resumes executing the instruction immediately after the instruction to set the CM30 bit to 1 when exiting wait mode. If the MCU enters wait mode with the WAIT instruction, interrupt handling is performed by the CPU when exiting wait mode.

10.2.4 Oscillation Stop Detection Register (OCD)

Address 000Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	OCD3	OCD2	OCD1	OCD0
After Reset	0	0	0	0	0	1	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	OCD0	Oscillation stop detection enable bit (6)	0: Oscillation stop detection function disabled (1) 1: Oscillation stop detection function enabled	R/W
b1	OCD1	Oscillation stop detection interrupt enable bit	0: Disabled (1) 1: Enabled	R/W
b2	OCD2	System clock select bit (3)	0: XIN clock selected (6) 1: On-chip oscillator clock selected (2)	R/W
b3	OCD3	Clock monitor bit (4, 5)	0: XIN clock oscillates 1: XIN clock stops	R
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

Notes:
1. Set bits OCD1 to OCD0 to 00b before the MCU enters stop mode, high-speed on-chip oscillator mode, or low-speed on-chip oscillator mode (XIN clock stops).
2. When the OCD2 bit is set to 1 (on-chip oscillator clock selected), the CM14 bit is set to 0 (low-speed on-chip oscillator on).
3. The OCD2 bit is automatically set to 1 (on-chip oscillator clock selected) when the XIN clock oscillation stop is detected while bits OCD1 to OCD0 are set to 11b. When the OCD3 bit is set to 1 (XIN clock stops), the OCD2 bit remains unchanged even if 0 (XIN clock selected) is written to it.
4. The OCD3 bit is enabled when the OCD0 bit is set to 1 (oscillation stop detection function enabled).
5. The OCD3 bit remains 0 (XIN clock oscillates) when bits OCD1 to OCD0 are set to 00b.
6. Refer to **9.7.1 How to Use Oscillation Stop Detection Function** for the switching procedure when the XIN clock re-oscillates after detecting an oscillation stop.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the OCD register.

10.2.5 High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Address 0023h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	FRA03	—	FRA01	FRA00
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FRA00	High-speed on-chip oscillator enable bit	0: High-speed on-chip oscillator off 1: High-speed on-chip oscillator on	R/W
b1	FRA01	High-speed on-chip oscillator select bit (1)	0: Low-speed on-chip oscillator selected (2) 1: High-speed on-chip oscillator selected	R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	FRA03	fOCO128 clock select bit	0: fOCO-S divided by 128 selected 1: fOCO-F divided by 128 selected	R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

Notes:

1. Change the FRA01 bit under the following conditions.
   - FRA00 = 1 (high-speed on-chip oscillator on)
   - CM14 bit in CM1 register = 0 (low-speed on-chip oscillator on)
   - Bits FRA22 to FRA20 in the FRA2 register:
     All division mode can be set when VCC = 3.0 V to 5.5 V 000b to 111b
     Division ratio of 4 or more when VCC = 2.7 V to 5.5 V 010b to 111b (divide-by-4 or more)
     Division ratio of 8 or more when VCC = 2.2 V to 5.5 V 110b to 111b (divide-by-8 or more)
2. When setting the FRA01 bit to 0 (low-speed on-chip oscillator selected), do not set the FRA00 bit to 0 (high-speed on-chip oscillator off) at the same time. Set the FRA01 bit to 0 before setting the FRA00 bit to 0.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRA0 register.

10.2.6 Voltage Detect Register 2 (VCA2)

Address 0034h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VCA27	VCA26	VCA25	VCA24	VCA23	VCA22	VCA21	VCA20
After Reset	The LVDAS bit in the OFS register is set to 1.							
	0	0	0	0	0	0	0	0
After Reset	The LVDAS bit in the OFS register is set to 0.							
	0	0	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	VCA20	Internal power low consumption enable bit (1)	0: Low consumption disabled 1: Low consumption enabled (2)	R/W
b1	VCA21	Comparator A1 reference voltage input select bit	0: Internal reference voltage 1: LVREF pin input voltage	R/W
b2	VCA22	LVCMP1 comparison voltage external input select bit	0: Supply voltage (VCC) 1: LVCMP1 pin input voltage	R/W
b3	VCA23	Comparator A2 reference voltage input select bit	0: Internal reference voltage 1: LVREF pin input voltage	R/W
b4	VCA24	LVCMP2 comparison voltage external input select bit	0: Supply voltage (VCC) (Vdet2_0) 1: LVCMP2 pin input voltage (Vdet2_EXT)	R/W
b5	VCA25	Voltage detection 0 enable bit (3)	0: Voltage detection 0 circuit disabled 1: Voltage detection 0 circuit enabled	R/W
b6	VCA26	Voltage detection 1/comparator A1 enable bit (4)	0: Voltage detection 1/comparator A1 circuit disabled 1: Voltage detection 1/comparator A1 circuit enabled	R/W
b7	VCA27	Voltage detection 2/comparator A2 enable bit (5)	0: Voltage detection 2/comparator A2 circuit disabled 1: Voltage detection 2/comparator A2 circuit enabled	R/W

Notes:
1. Use the VCA20 bit only when the MCU enters wait mode. To set the VCA20 bit, follow the procedure shown in **Figure 10.7 Handling Procedure for Reducing Internal Power Consumption Using VCA20 Bit**.
2. When the VCA20 bit is set to 1 (low consumption enabled), do not set the CM10 bit in the CM1 register to 1 (stop mode).
3. To use voltage monitor 0 reset, set the VCA25 bit to 1.
   After the VCA25 bit is set to 1 from 0, allow td(E-A) to elapse before the voltage detection circuit starts operation.
4. To use the voltage detection 1/comparator A1 interrupt or the VW1C3 bit in the VW1C register, set the VCA26 bit to 1.
   After the VCA26 bit is set to 1 from 0, allow td(E-A) to elapse before the voltage detection 1/comparator A1 circuit starts operation.
5. To use the voltage detection 2/comparator A2 interrupt or the VCAC13 bit in the VCA1 register, set the VCA27 bit to 1.
   After the VCA27 bit is set to 1 from 0, allow td(E-A) to elapse before the voltage detection 2/comparator A2 circuit starts operation.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VCA2 register.

10.2.7 Power-Off Mode Control Register 0 (POMCR0)

Address 0020h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	POM07	POM06	POM05	POM04	POM03	POM02	POM01	POM00
After Reset	X	0	0	0	0	0	0	0

Initial write: Selection of the pin status in power-off mode and the exit methods

Bit	Symbol	Bit Name	Function	R/W
b0	POM00	Power-off mode select bit	0: Power-off 0 (all functions stop) 1: Power-off 1 (timer RE enabled)	W
b1	POM01	Reserved bits	Set to 0.	W
b2	POM02			W
b3	POM03	$\overline{\text{WKUP1}}$ input enable bit	0: Input disabled 1: Input enabled	W
b4	POM04	Reserved bits	Set to 0.	W
b5	POM05			W
b6	POM06			W
b7	POM07			W

Second to fifth write: Entering power-off mode

Bit	Function	R/W
b7 to b0	Write 88h, 15h, 92h, and 25h successively.	W

Read

Bit	Symbol	Bit Name	Function	R/W
b0	POM00	$\overline{\text{WKUP0}}$ source power-off exit flag	0: Undetected 1: Detected	R
b1	POM01	$\overline{\text{WKUP1}}$ source power-off exit flag	0: Undetected 1: Detected	R
b2	—	Nothing is assigned. When read, the content is undefined.		R
b3	—			
b4	—			
b5	—			
b6	POM06	Timer RE source power-off exit flag	0: Undetected 1: Detected	R
b7	—	Nothing is assigned. When read, the content is undefined.		R

Note:
1. Write to the POMCR0 register five times successively to enter power-off mode.

10.3 Standard Operating Mode

Table 10.2 lists the Clock Selection in Standard Operating Mode.

In standard operating mode, the CPU and peripheral function clocks are supplied to operate the CPU and the peripheral functions. Power control is enabled by controlling the CPU clock frequency. The higher the CPU clock frequency, the more processing power increases. The lower the CPU clock frequency, the more power consumption decreases. If unnecessary oscillator circuits stop, power consumption is further reduced.

Before the clock sources for the CPU clock can be switched over, the new clock source needs to be oscillating and stable. If the new clock source is the XIN clock or XCIN clock, allow sufficient wait time in a program until oscillation stabilizes before the MCU exits.

Table 10.2 Clock Selection in Standard Operating Mode

Modes		OCD Register	CM1 Register				CM0 Register					FRA0 Register	
		OCD2	CM17	CM16	CM14	CM13	CM07	CM06	CM05	CM04	CM03	FRA01	FRA00
High-speed clock mode	No division	0	0	0	–	1	0	0	0	–	–	–	–
	Divide-by-2	0	0	1	–	1	0	0	0	–	–	–	–
	Divide-by-4	0	1	0	–	1	0	0	0	–	–	–	–
	Divide-by-8	0	–	–	–	1	0	1	0	–	–	–	–
	Divide-by-16	0	1	1	–	1	0	0	0	–	–	–	–
Low-speed clock mode	No division	–	0	0	–	–	1	0	–	0	0	–	–
	Divide-by-2	–	0	1	–	–	1	0	–	0	0	–	–
	Divide-by-4	–	1	0	–	–	1	0	–	0	0	–	–
	Divide-by-8	–	–	–	–	–	1	1	–	0	0	–	–
	Divide-by-16	–	1	1	–	–	1	0	–	0	0	–	–
High-speed on-chip oscillator mode	No division	1	0	0	–	–	0	0	–	–	–	1	1
	Divide-by-2	1	0	1	–	–	0	0	–	–	–	1	1
	Divide-by-4	1	1	0	–	–	0	0	–	–	–	1	1
	Divide-by-8	1	–	–	–	–	0	1	–	–	–	1	1
	Divide-by-16	1	1	1	–	–	0	0	–	–	–	1	1
Low-speed on-chip oscillator mode	No division	1	0	0	0	–	0	0	–	–	–	0	–
	Divide-by-2	1	0	1	0	–	0	0	–	–	–	0	–
	Divide-by-4	1	1	0	0	–	0	0	–	–	–	0	–
	Divide-by-8	1	–	–	0	–	0	1	–	–	–	0	–
	Divide-by-16	–	1	1	0	–	0	0	–	–	–	0	–

–: Indicates that either 0 or 1 can be set.

10.3.1 High-Speed Clock Mode

The XIN clock divided by 1 (no division), 2, 4, 8, or 16 is used as the CPU clock. When the CM14 bit is set to 0 (low-speed on-chip oscillator on) or the FRA00 bit in the FRA0 register is set to 1 (high-speed on-chip oscillator on), fOCO can be used for timer RA.
Also, when the FRA00 bit is set to 1, fOCO40M can be used for timers RC, RD, and RG.
When the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used for the voltage detection circuit.

10.3.2 Low-Speed Clock Mode

The XCIN clock divided by 1 (no division), 2, 4, 8, or 16 is used as the CPU clock.
In this mode, low consumption operation is enabled by stopping the XIN clock and the high-speed on-chip oscillator, and by setting the FMR27 bit in the FMR2 register to 1 (flash memory low-consumption-current read mode enabled).
Also, when the FRA00 bit is set to 1, fOCO40M can be used for timers RC, RD, and RG.
When the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used for the voltage detection circuit.
To enter wait mode from low-speed clock mode, lower consumption current in wait mode is enabled by setting the VCA20 bit in the VCA2 register to 1 (internal power low consumption enabled).
To reduce the power consumption, refer to **10.7 Reducing Power Consumption**.

10.3.3 High-Speed On-Chip Oscillator Mode

The high-speed on-chip oscillator is used as the on-chip oscillator clock when the FRA00 bit in the FRA0 register is set to 1 (high-speed on-chip oscillator on) and the FRA01 bit in the FRA0 register is set to 1. The on-chip oscillator divided by 1 (no division), 2, 4, 8, or 16 is used as the CPU clock. When the FRA00 bit is set to 1, fOCO40M can be used for timers RC, RD, and RG.
Also, when the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used for the voltage detection circuit.

10.3.4 Low-Speed On-Chip Oscillator Mode

When the CM14 bit in the CM1 register is set to 0 (low-speed on-chip oscillator on) and the FRA01 bit in the FRA0 register is set to 0, the low-speed on-chip oscillator is used as the on-chip oscillator clock. At this time, the on-chip oscillator clock divided by 1 (no division), 2, 4, 8 or 16 is used as the CPU clock. The on-chip oscillator clock is also the clock source for the peripheral function clocks. When the FRA00 bit is set to 1, fOCO40M can be used for timers RC, RD, and RG.
Also, When the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used for the voltage detection circuit.
In this mode, low consumption operation is enabled by stopping the XIN clock and the high-speed on-chip oscillator, and by setting the FMR27 bit in the FMR2 register to 1 (flash memory low-consumption-current read mode enabled).
To enter wait mode from low-speed clock mode, current consumption in wait mode can be further reduced by setting the VCA20 bit in the VCA2 register to 1 (internal power low consumption enabled).
To reduce the power consumption, refer to **10.7 Reducing Power Consumption**.

10.4 Wait Mode

Since the CPU clock stops in wait mode, CPU operation using the CPU clock and watchdog timer operation with count source protection mode disabled are halted. However, the XIN clock, XCIN clock, and on-chip oscillator clock do not stop, so peripheral functions using these clocks continue operating.

10.4.1 Peripheral Function Clock Stop Function

The peripheral function clock to stop in wait mode can be selected by setting bits CM01 and CM02 in the CM0 register (peripheral function clock stop bits in wait mode). This controls power consumption according to applications.

10.4.2 Entering Wait Mode

The MCU enters wait mode by executing the WAIT instruction or setting the CM30 bit in the CM3 register to 1 (MCU enters wait mode).
When the OCD2 bit in the OCD register is set to 1 (on-chip oscillator selected as system clock), set the OCD1 bit in the OCD register to 0 (oscillation stop detection interrupt disabled) before executing the WAIT instruction or setting the CM30 bit in the CM3 register to 1 (MCU enters wait mode).
If the MCU enters wait mode while the OCD1 bit is set to 1 (oscillation stop detection interrupt enabled), current consumption is not reduced because the CPU clock does not stop.

10.4.3 Pin Status in Wait Mode

Each I/O port retains its states immediately before the MCU enters wait mode.

10.4.4 Exiting Wait Mode

The MCU exits wait mode by a reset or peripheral function interrupt. The peripheral function interrupts are affected by bits CM01 and CM02.

Table 10.3 Interrupts to Exit Wait Mode and Usage Conditions

Interrupt	CM02 to CM01 = 00b	CM02 to CM01 = 01b	CM02 to CM01 = 10b	CM02 to CM01 = 11b
Serial interface interrupt	Usable when operating with an internal or external clock.	Usable when operating with fC or an external clock.	Usable when operating with an external clock.	Usable when operating with an external clock.
Clock synchronous serial I/O with chip select interrupt / I^2C bus interface interrupt	Usable in all modes.	(Do not use.)	(Do not use.)	(Do not use.)
Key input interrupt	Usable	Usable	Usable	Usable
A/D conversion interrupt	(Do not use.)	(Do not use.)	(Do not use.)	(Do not use.)
Timer RA interrupt	Usable in all modes.	Usable if there is no filter in event counter mode. Usable by selecting fOCO, fC, or fC32 as the count source.	Usable if there is no filter in event counter mode. Usable by selecting fOCO as the count source.	Usable if there is no filter in event counter mode. Usable by selecting fOCO as the count source.
Timer RB interrupt	Usable in all modes.	(Do not use.)	(Do not use.)	(Do not use.)
Timer RC interrupt	Usable in all modes.	(Do not use.)	(Do not use.)	(Do not use.)
Timer RD interrupt	Usable in all modes.	Usable by selecting fOCO40M as the count source.	Usable by selecting fOCO40M as the count source.	Usable by selecting fOCO40M as the count source.
Timer RE interrupt	Usable in all modes.	Usable when operating in real time clock mode.	Usable when operating in real time clock mode.	Usable when operating in real time clock mode.
Timer RG interrupt	Usable in all modes.	(Do not use.)	(Do not use.)	(Do not use.)
$\overline{\text{INT}}$ interrupt	Usable	Usable if there is no filter.	Usable if there is no filter.	Usable if there is no filter.
Voltage monitor 1 interrupt	Usable	Usable	Usable	Usable
Voltage monitor 2 interrupt	Usable	Usable	Usable	Usable
Oscillation stop detection interrupt	Usable	(Do not use.)	(Do not use.)	(Do not use.)
Watchdog timer interrupt	Usable in count source protection mode.	Usable in count source protection mode.	Usable in count source protection mode.	Usable in count source protection mode.
Comparator A1 interrupt	Usable	Usable	Usable	Usable
Comparator A2 interrupt	Usable	Usable	Usable	Usable
LCD counter interrupt	Usable	Usable by selecting fC-LCD as the count source.	Usable by selecting fC-LCD as the count source.	(Do not use.)

The following interrupts can be used to exit wait mode:

- When bits CM02 to CM01 are set to 00b (peripheral function clock does not stop in wait mode), peripheral function interrupts other than A/D conversion interrupts.
- When bits CM02 to CM01 are set to 01b (clocks f1 to f32 stop in wait mode), the interrupts of the peripheral functions operating with external signals, the on-chip oscillator clock, or clocks fC1 to f32.
- When bits CM02 to CM01 are set to 10b (clocks f1 to f32 and fC stop in wait mode), the interrupts of the peripheral functions operating with external signals or the on-chip oscillator clock.
- When bits CM02 to CM01 are set to 11b (clocks f1 to f32, fC, and fC-LCD stop in wait mode), the same applies when bits CM02 to CM01 are set to 10b.

Table 10.3 lists Interrupts to Exit Wait Mode and Usage Conditions.

Figure 10.2 shows the Time from Wait Mode to Interrupt Routine Execution after CM30 Bit in CM3 Register is Set to 1 (MCU Enters Wait Mode).
To use a peripheral function interrupt to exit wait mode, set up the following before setting the CM30 bit to 1.

(1) Set the interrupt priority level in bits ILVL2 to ILVL0 in the interrupt control registers of the peripheral function interrupts to be used for exiting wait mode. Set bits ILVL2 to ILVL0 of the peripheral function interrupts that are not to be used for exiting wait mode to 000b (interrupt disabled).
(2) Operate the peripheral function to be used for exiting wait mode.

When the MCU exits by a peripheral function interrupt, the time (number of cycles) between interrupt request generation and interrupt routine execution is determined by the settings of the FMSTP bit in the FMR0 register and the VCA20 bit in the VCA2 register, as shown in Figure 10.2.
The clock set by bits CM35, CM36, and CM37 in the CM3 register is used as the CPU clock when the MCU exits wait mode by a peripheral function interrupt. At this time, the CM06 bit in the CM0 register and bits CM16 and CM17 in the CM1 register automatically change.

FMR0 Register	VCA2 Register	Internal Power Stabilization Time (T0)	Time until Flash Memory Activation (T1)	Time until CPU Clock Supply (T2)	Time for Interrupt Sequence (T3)	Remarks
FMSTP Bit	VCA20 Bit					
0 (flash memory operates)	0 (internal power low consumption disabled)	0 µs	Period of system clock × 1 cycle + 60 µs (max.)	Period of CPU clock × 2 cycles	Period of CPU clock × 20 cycles	The total of T0 to T3 is the time from wait mode until an interrupt routine is executed.
	1 (internal power low consumption enabled)	100 µs (max.)				
1 (flash memory stops)	0 (internal power low consumption disabled	0 µs	Period of system clock × 1 cycle	Same as above	Same as above	
	1 (internal power low consumption enabled)	100 µs (max.)				

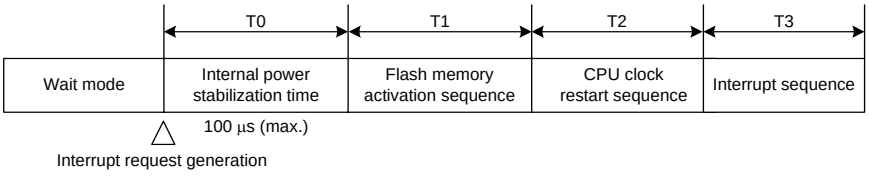


Figure 10.2 Time from Wait Mode to Interrupt Routine Execution after CM30 Bit in CM3 Register is Set to 1 (MCU Enters Wait Mode)

Figure 10.3 shows the Time from Wait Mode to Interrupt Routine Execution after WAIT instruction is Executed.
To use a peripheral function interrupt to exit wait mode, set up the following before executing the WAIT instruction.

(1) Set the interrupt priority level in bits ILVL2 to ILVL0 of the peripheral function interrupts to be used for exiting stop mode. Set bits ILVL2 to ILVL0 of the peripheral function interrupts that are not to be used for exiting stop mode to 000b (interrupt disabled).
(2) Set the I flag to 1.
(3) Operate the peripheral function to be used for exiting stop mode.

When the MCU exits by a peripheral function interrupt, the time (number of cycles) between interrupt request generation and interrupt routine execution is determined by the settings of the FMSTP bit in the FMR0 register and the VCA20 bit in the VCA2 register, as shown in Figure 10.3.
The clock set by bits CM35, CM36, and CM37 in the CM3 register is used as the CPU clock when the MCU exits wait mode by a peripheral function interrupt. At this time, the CM06 bit in the CM0 register and bits CM16 and CM17 in the CM1 register automatically change.

FMR0 Register / FMSTP Bit	VCA2 Register / VCA20 Bit	Internal Power Stabilization Time (T0)	Time until Flash Memory Activation (T1)	Time until CPU Clock Supply (T2)	Time for Interrupt Sequence (T3)	Remarks
0 (flash memory operates)	0 (internal power low consumption disabled)	0 µs	Period of system clock × 1 cycle + 60 µs (max.)	Period of CPU clock × 2 cycles	Period of CPU clock × 20 cycles	The total of T0 to T3 is the time from wait mode until an interrupt routine is executed.
	1 (internal power low consumption enabled)	100 µs (max.)				
1 (flash memory stops)	0 (internal power low consumption disabled	0 µs	Period of system clock × 1 cycle	Same as above	Same as above	
	1 (internal power low consumption enabled)	100 µs (max.)				

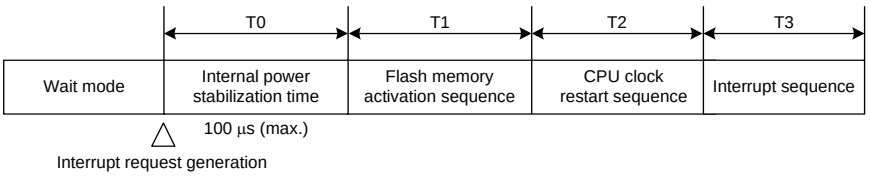


Figure 10.3 Time from Wait Mode to Interrupt Routine Execution after WAIT instruction is Executed

10.5 Stop Mode

All oscillator circuits except fOCO-WDT stop in stop mode. Since the CPU clock and the peripheral function clock stop, CPU operation and peripheral function operation using these clocks are halted. If the voltage applied to the VCC pin is VRAM or more, the content of internal RAM is retained.
The peripheral functions clocked by external signals continue operating.
Table 10.4 lists Interrupts to Exit Stop Mode and Usage Conditions.

Table 10.4 Interrupts to Exit Stop Mode and Usage Conditions

Interrupt	Usage Conditions
Key input interrupt	–
$\overline{\text{INT}}$ interrupt	Usable if there is no filter.
Timer RA interrupt	Usable if there is no filter when an external pulse is counted in event counter mode.
Serial interface interrupt	When an external clock is selected.
Voltage monitor 1 interrupt	Usable in digital filter disabled mode (the VW1C1 bit in the VW1C register is set to 1).
Voltage monitor 2 interrupt	Usable in digital filter disabled mode (the VW2C1 bit in the VW2C register is set to 1).
Comparator A1 interrupt	Usable in digital filter disabled mode (the VW1C1 bit in the VW1C register is set to 1).
Comparator A2 interrupt	Usable in digital filter disabled mode (the VW2C1 bit in the VW2C register is set to 1).

10.5.1 Entering Stop Mode

The MCU enters stop mode when the CM10 bit in the CM1 register is set to 1 (all clocks stop). At the same time, the CM06 bit in the CM0 register is set to 1 (divide-by-8 mode).
To use stop mode, set the following before the MCU enters stop mode:

- Bits OCD1 to OCD0 in the OCD register = 00b
- CM35 bit in CM3 register = 0 (settings of CM06 bit in CM0 register and bits CM16 and CM17 in CM1 register enabled)

10.5.2 Pin Status in Stop Mode

Each I/O port retains its state before the MCU enters stop mode.
However, when the CM13 bit in the CM1 register is set to 1 (XIN-XOUT pin), the XOUT (P12_0) pin is held high.

10.5.3 Exiting Stop Mode

The MCU exits stop mode by a reset or peripheral function interrupt.
Figure 10.4 shows the Time from Stop Mode to Interrupt Routine Execution.
To use a peripheral function interrupt to exit stop mode, set up the following before setting the CM10 bit to 1.

(1) Set the interrupt priority level in bits ILVL2 to ILVL0 of the peripheral function interrupts to be used for exiting stop mode. Set bits ILVL2 to ILVL0 of the peripheral function interrupts that are not to be used for exiting stop mode to 000b (interrupt disabled).
(2) Set the I flag to 1.
(3) Operate the peripheral function to be used for exiting stop mode.
When the MCU exits stop mode by a peripheral function interrupt, the interrupt sequence is executed when an interrupt request is generated and the CPU clock supply starts.

The clock used immediately before stop mode divided by 8 is used as the CPU clock when the MCU exits stop mode by a peripheral function interrupt. To enter stop mode, set the CM35 bit in the CM3 register to 0 (settings of CM06 bit in CM0 register and bits CM16 and CM17 in CM1 register enabled).

FMR0 Register / FMSTP Bit	Internal Power Stabilization Time (T0)	Time until Flash Memory Activation (T2)	Time until CPU Clock Supply (T3)	Time for Interrupt Sequence (T4)	Remarks
0 (flash memory operates)	100 µs (max.)	Period of system clock × 1 cycle + 60 µs (max.)	Period of CPU clock × 2 cycles	Period of CPU clock × 20 cycles	The total of T0 to T4 is the time from wait mode until an interrupt routine is executed.
1 (flash memory stops)	100 µs (max.)	Period of system clock × 1 cycle	Same as above	Same as above	

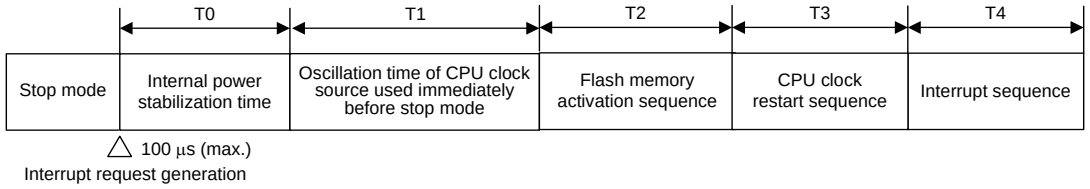


Figure 10.4 Time from Stop Mode to Interrupt Routine Execution

10.6 Power-Off Mode

All functions stop in power-off mode. However, the low-speed clock and timer RE functions can be set to operate or stop by means of register settings. The least power is consumed in this mode.

10.6.1 Pin Handling in Power-Off Mode

Figure 10.5 shows Pin Handling in Power-Off Mode. To use this mode, hardware reset input is required. For details of hardware resets, refer to **5.2 Hardware Reset**.

10.6.2 Entering Power-Off Mode

Table 10.5 lists the register settings in power-off mode.
The pin status in power-off mode and the method of exiting are selected by the initial write to the POMCR0 register. When 88h, 15h, 92h, and 25h are then written successively, the MCU enters power-off mode.

- Power-off 0
  When the POM00 bit is set to 0 (power-off 0) by the initial write, all functions stop once the MCU enters power-off mode.
- Power-off 1
  When the POM00 bit is set to 1 (power-off 1) by the initial write, all functions except the low-speed clock and timer RE stop once the MCU enters power-off mode. The timer RE interrupt can be used to exit the mode when power-off 1 is selected.

An access to another register during the write to the POMCR0 register does not affect entering the mode.

10.6.3 Pin Status in Power-Off Mode

Table 10.6 lists the Pin Status in Power-Off Mode. When the MCU enters power-off mode, the contents of RAM and registers are not retained. Save the data needs to be retained to the data flash before entering power-off mode.

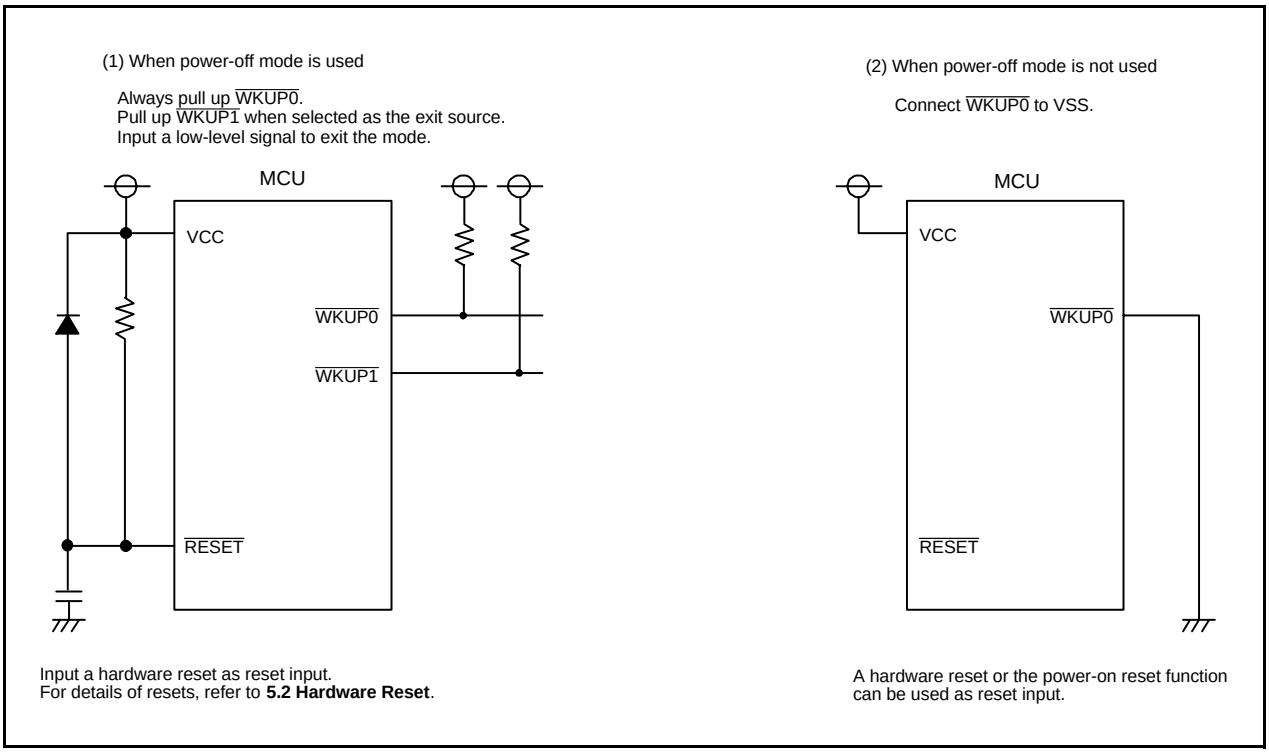


Figure 10.5 Pin Handling in Power-Off Mode

10.6.4 Exiting Power-Off Mode

To exit power-off mode, input a low signal pulse to the $\overline{\text{RESET}}$, $\overline{\text{WKUP0}}$, or $\overline{\text{WKUP1}}$ pin or use the timer RE interrupt (power-off 1 is selected). The timer RE interrupt enabled in the TREC2 register can be used to exit the mode.
After exiting power-off mode, the operation is the same as a normal reset sequence.
When power-off mode is exited, the exit source can be identified by reading the flags in the SDCR0 register. The values of these flags are undefined after power-on and set to 0 by writing to the SDCR0 register. If multiple exit sources coincide, multiple flags are set.
Figure 10.6 show the Time from Power-Off Mode to Reset Vector Address Read Execution.

Table 10.5 Entering Power-Off Mode and Exit Methods

Entering Power-Off Mode	Status	Exit Method
Write the pin state and the exit method to the POMCR0 register (1, 2) in power-off mode. Then, write 88h,15h, 92h, and 25h successively.	All functions stop when the SDC00 bit is set to 0 (power-off 0) by the initial write.	$\overline{\text{RESET}}$ input, $\overline{\text{WKUP0}}$ input, or $\overline{\text{WKUP1}}$ input
	Functions other the low-speed clock and timer RE stop when the SDC00 bit is set to 1 (power-off 1) by the initial write.	$\overline{\text{RESET}}$ input, timer RE interrupt, $\overline{\text{WKUP0}}$ input, or $\overline{\text{WKUP1}}$ input

Notes:
1. To use $\overline{\text{WKUP1}}$ to exit power-off mode, set the POM03 bit to 1 (input enabled) by the initial write to the POMCR0 register.
2. To use timer RE to exit power-off mode, enable the timer RE interrupt in registers TREIC and TRECR2, then set the POM00 bit in the POMCR0 register to 1 (timer RE enabled). When all interrupts are disabled by the TRECR2 register, the low-speed clock and timer RE functions operate, but timer RE cannot be used to exit power-off mode.

Table 10.6 Pin Status in Power-Off Mode

Pin Name	Status
Ports P0 to P7	The states of registers LSE0 to LSE7 before entering power-off mode are retained. When LCD ports are selected by these registers, low-level output. When ports are selected, the pins are placed in the high-impedance state.
Ports 10 to P13	High impedance
$\overline{\text{WKUP0}}$	$\overline{\text{WKUP0}}$ input
XCIN, XCOUT	Oscillation is off (high impedance) at power-off 0, and oscillation is on at power-off 1.
VL1 to VL4	High impedance

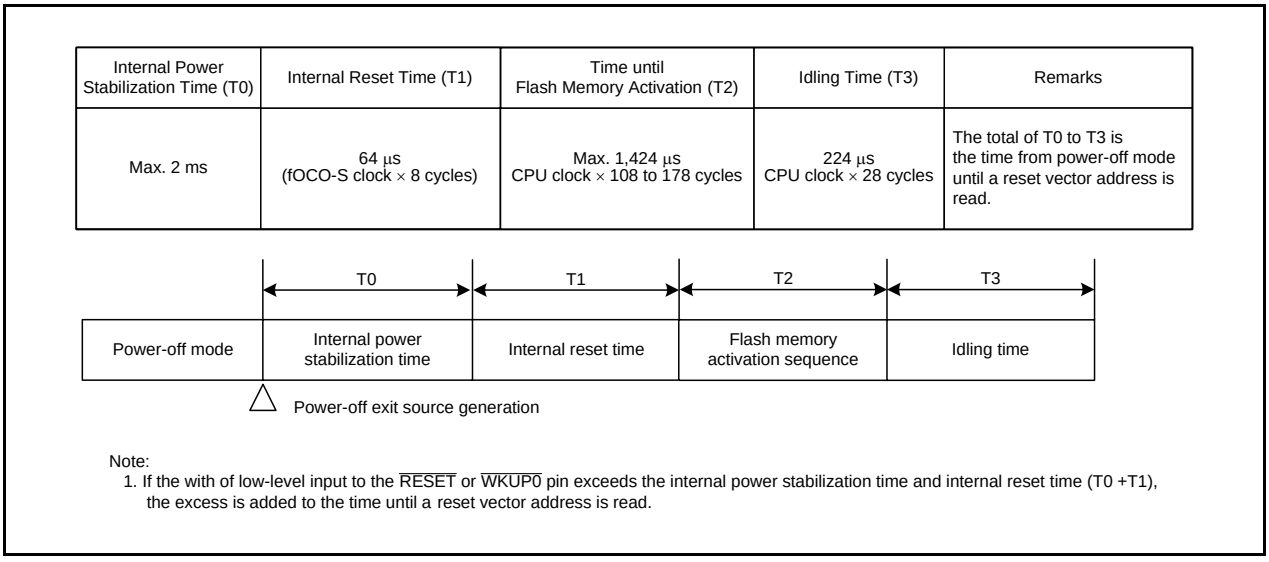


Figure 10.6 Time from Power-Off Mode to Reset Vector Address Read Execution

10.7 Reducing Power Consumption

This section describes key points and processing methods for reducing power consumption. They should be referred to when designing a system or creating a program.

10.7.1 Voltage Detection Circuit

When voltage monitor 1 and comparator A1 are not used, set the VCA26 bit in the VCA2 register to 0 (voltage detection 1 circuit disabled). When voltage monitor 2 and comparator A2 are not used, set the VCA27 bit in the VCA2 register to 0 (voltage detection 2 circuit disabled).
When power-on reset and voltage monitor 0 reset are not used, set the VCA25 bit in the VCA2 register to 0 (voltage detection 0 circuit disabled).

10.7.2 Ports

Even after the MCU enters wait mode or stop mode, the states of the I/O ports are retained. Current flows into the output ports in the active state, and shoot-through current flows into the input ports in the high-impedance state. Unnecessary ports should be set to input and fixed to a stable electric potential before the MCU enters wait mode or stop mode.

10.7.3 Clocks

Power consumption generally depends on the number of the operating clocks and their frequencies. The fewer the number of operating clocks or the lower their frequencies, the more power consumption decreases.
Unnecessary clocks should be stopped accordingly.

Stopping the low-speed on-chip oscillator oscillation: CM14 bit in CM1 register
Stopping the high-speed on-chip oscillator oscillation: FRA00 bit in FRA0 register

10.7.4 Wait Mode, Stop Mode, and Power-Off Mode

Power consumption can be reduced in wait mode, stop mode, and power-off mode.

10.7.5 Stopping Peripheral Function Clocks

When peripheral function clocks are not necessary in wait mode, set bits CM01 and CM02 bit in the CM0 register to stop the clock.

10.7.6 Timers

When timer RA is not used, set the TCKCUT bit in the TRAMR register to 1 (count source cutoff).
When timer RB is not used, set the TCKCUT bit in the TRBMR register to 1 (count source cutoff).
When timer RC is not used, set the MSTTRC bit in the MSTCR register to 1 (standby).
When timer RD is not used, set the MSTTRD bit in the MSTCR register to 1 (standby).
When timer RG is not used, set the MSTTRG bit in the MSTCR register to 1 (standby).

10.7.7 A/D Converter

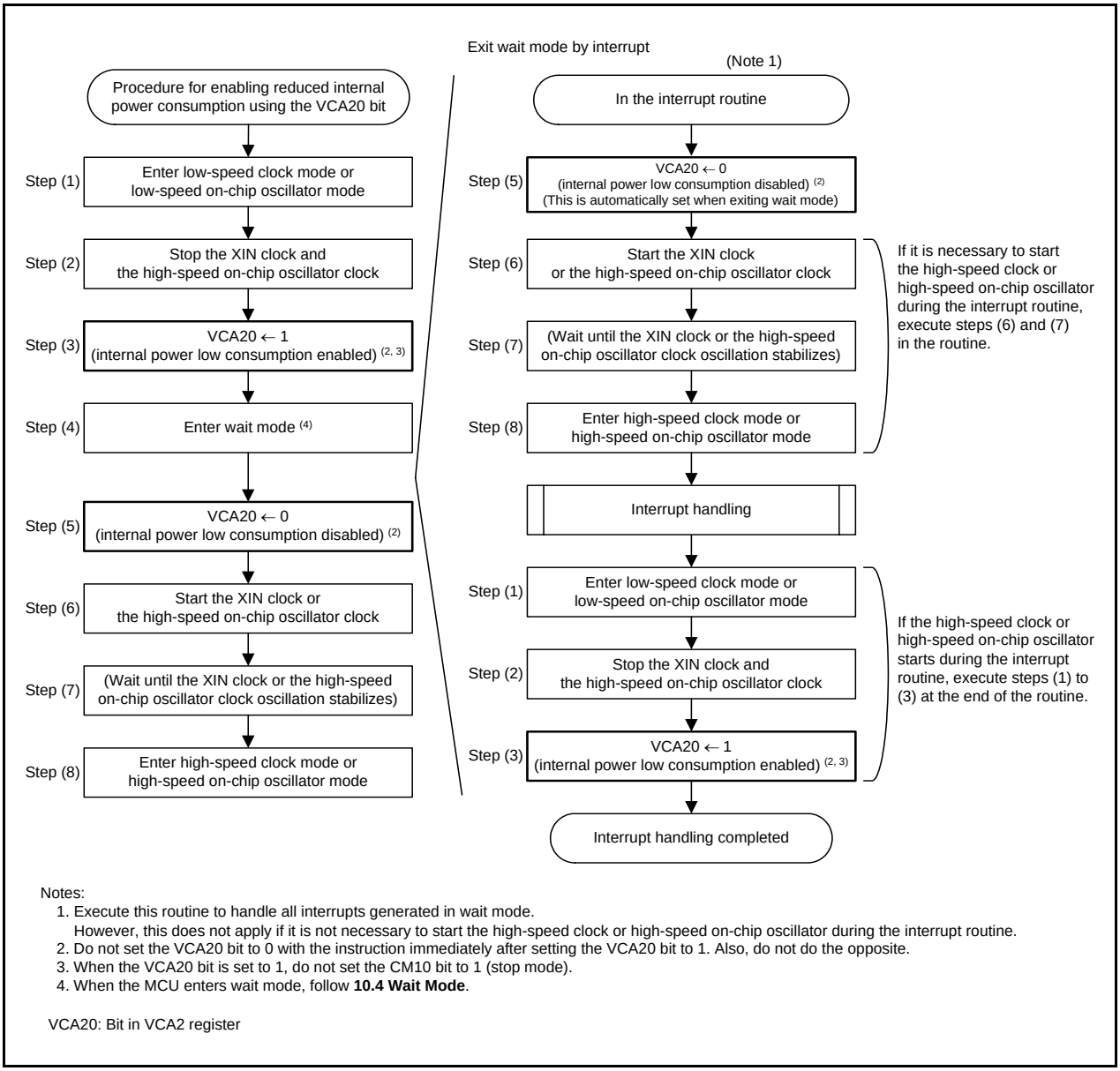
When the A/D converter is not used, power consumption can be reduced by setting the ADSTBY bit in the ADCON1 register to 0 (A/D operation stops (standby)) to shut off any analog circuit current flow.

10.7.8 Clock Synchronous Serial Interface

When the SSU or I^2C bus is not used, set the MSTIIC bit in the MSTCR register to 1 (standby).

10.7.9 Reducing Internal Power Consumption

When the MCU enters wait mode using low-speed clock mode or low-speed on-chip oscillator mode, internal power consumption can be reduced by using the VCA20 bit in the VCA2 register. Figure 10.7 shows the Handling Procedure for Reducing Internal Power Consumption Using VCA20 Bit. To enable reduced internal power consumption by the VCA20 bit, follow this procedure.



Notes:
1. Execute this routine to handle all interrupts generated in wait mode.
   However, this does not apply if it is not necessary to start the high-speed clock or high-speed on-chip oscillator during the interrupt routine.
2. Do not set the VCA20 bit to 0 with the instruction immediately after setting the VCA20 bit to 1. Also, do not do the opposite.
3. When the VCA20 bit is set to 1, do not set the CM10 bit to 1 (stop mode).
4. When the MCU enters wait mode, follow **10.4 Wait Mode**.

VCA20: Bit in VCA2 register

Figure 10.7 Handling Procedure for Reducing Internal Power Consumption Using VCA20 Bit

10.7.10 Stopping Flash Memory

In low-speed on-chip oscillator mode and low-speed clock mode, power consumption can be further reduced by stopping the flash memory using the FMSTP bit in the FMR0 register.
Access to the flash memory is disabled by setting the FMSTP bit to 1 (flash memory stops). The FMSTP bit must be written to by a program transferred to RAM.
When the MUC enters stop mode or wait mode while CPU rewrite mode is disabled, the power for the flash memory is automatically turned off. It is turned back on again after the MCU exit stop mode or wait mode. This eliminates the need to set the FMR0 register.
Figure 10.8 shows the Handling Procedure Example for Reducing Power Consumption Using FMSTP Bit.

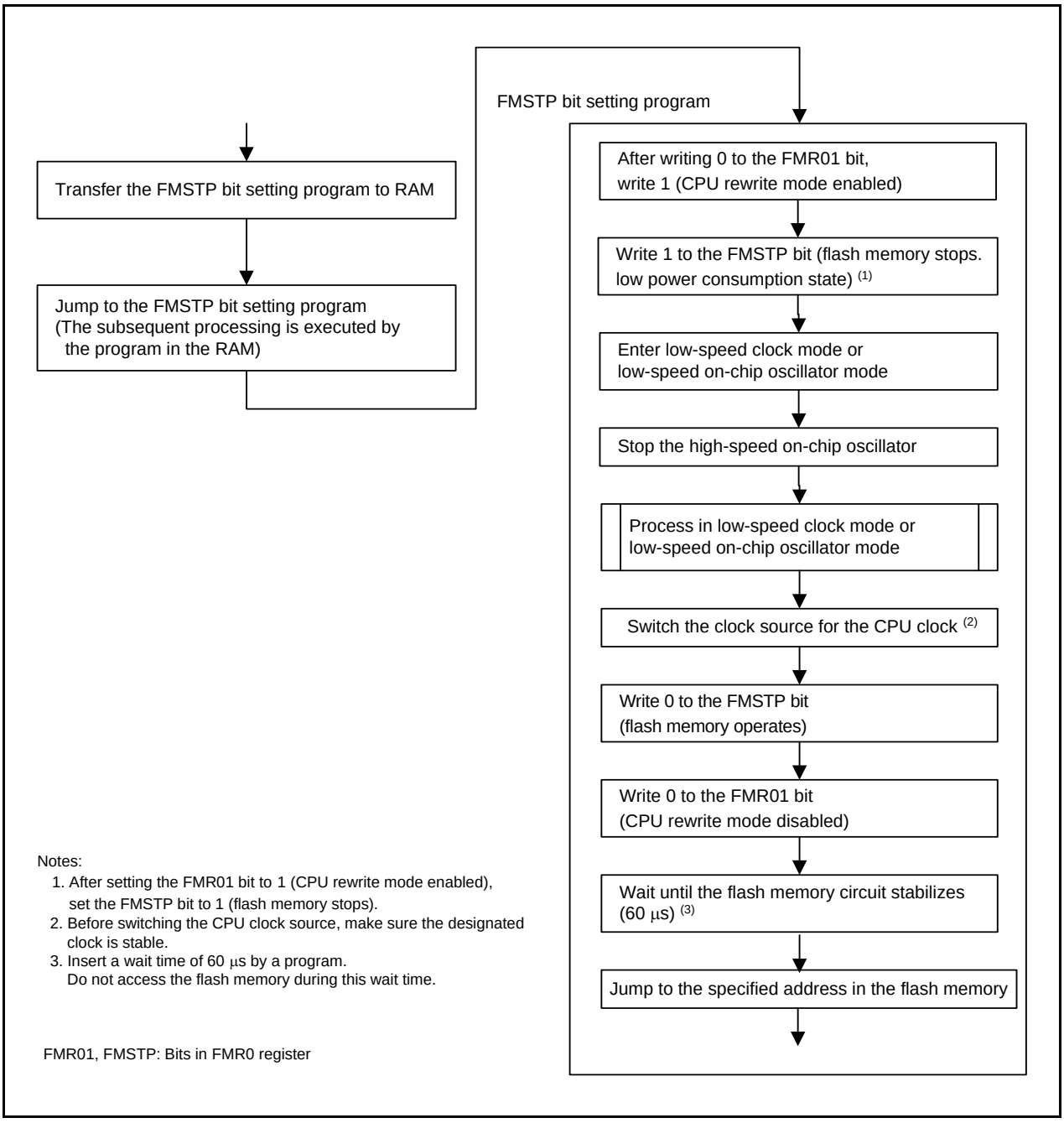
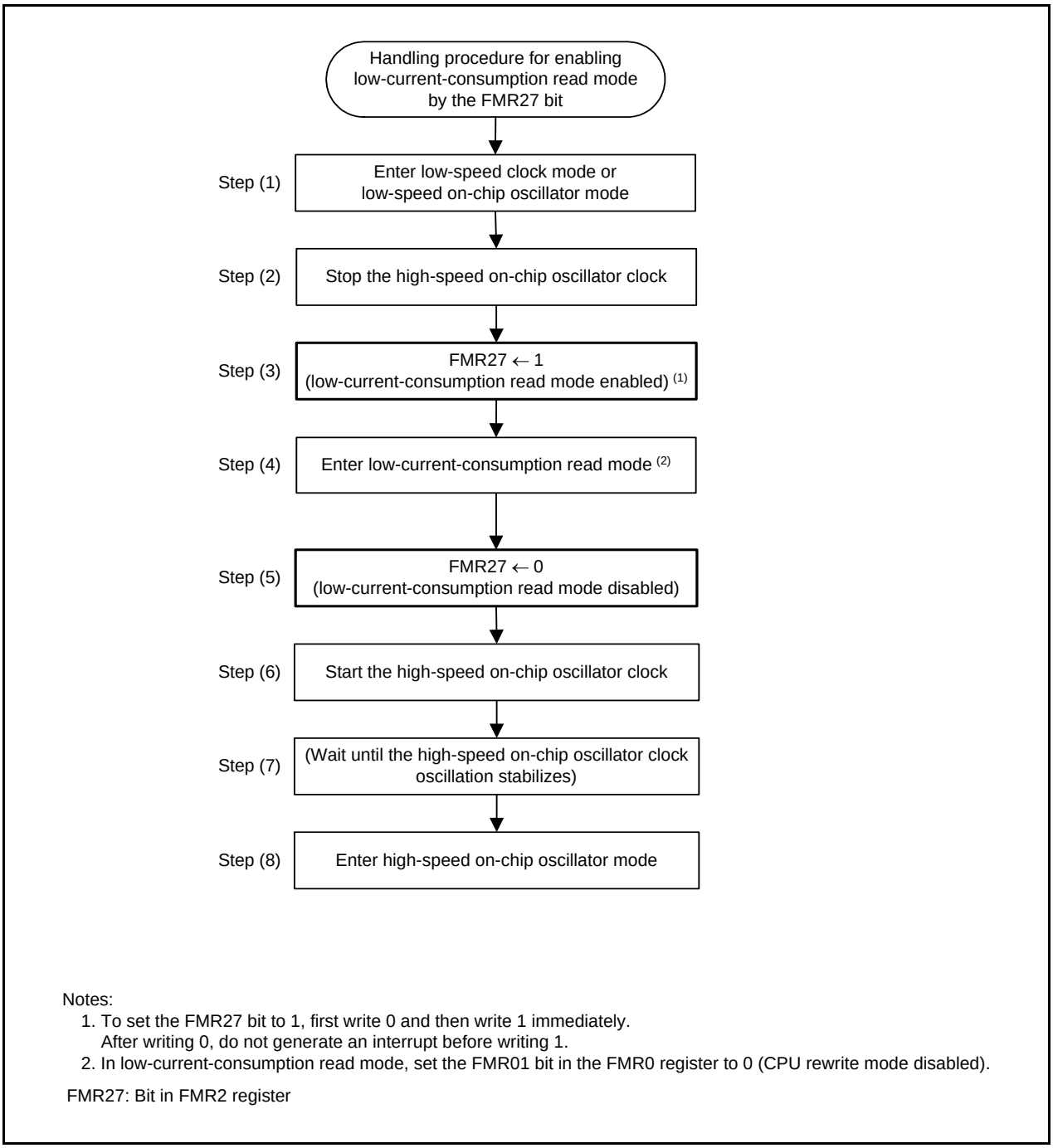


Figure 10.8 Handling Procedure Example for Reducing Power Consumption Using FMSTP Bit

10.7.11 Low-Current-Consumption Read Mode

In low-speed clock mode and low-speed on-chip oscillator mode, the current consumption when reading the flash memory can be reduced by setting the FMR27 bit in the FMR2 register to 1 (enabled).
Figure 10.9 shows the Handling Procedure Example of Low-Current-Consumption Read Mode.



Notes:
1. To set the FMR27 bit to 1, first write 0 and then write 1 immediately.
   After writing 0, do not generate an interrupt before writing 1.
2. In low-current-consumption read mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled).

FMR27: Bit in FMR2 register

Figure 10.9 Handling Procedure Example of Low-Current-Consumption Read Mode

10.8 Notes on Power Control

10.8.1 Stop Mode

To enter stop mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and then the CM10 bit in the CM1 register to 1 (stop mode). An instruction queue pre-reads 4 bytes from the instruction which sets the CM10 bit to 1 (stop mode) and the program stops.
Insert at least four NOP instructions following the JMP.B instruction after the instruction which sets the CM10 bit to 1.

- Program example to enter stop mode
  BCLR 1, FMR0; CPU rewrite mode disabled
  BSET 0, PRCR; Protect disabled
  FSET I; Enable interrupt
  BSET 0, CM1; Stop mode
  JMP.B LABEL_001
  LABEL_001:
  NOP
  NOP
  NOP
  NOP

10.8.2 Wait Mode

To enter wait mode with the WAIT instruction, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and then execute the WAIT instruction. An instruction queue pre-reads 4 bytes from the WAIT instruction and the program stops. Insert at least four NOP instructions after the WAIT instruction.

- Program example to execute the WAIT instruction
  BCLR 1, FMR0; CPU rewrite mode disabled
  FSET I; Enable interrupt
  WAIT; Wait mode
  NOP
  NOP
  NOP
  NOP

10.8.3 Power-Off Mode

To enter power-off mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and then access the POMCR0 register. A period of a few microseconds is required between accessing the POMCR0 register and entering power-off mode. As the CPU continues to operate during this period, insert the NOP and the WAIT instructions to stop the program.

- Program example to enter power-off mode (when timer RE and the low-speed clock is enabled)
  BCLR 1, FMR0; CPU rewrite mode disabled
  MOV. B #08H, POMCR0; Select power-off 0 and $\overline{\text{WKUP1}}$ input enabled
  MOV. B #88H, POMCR0; Fixed value
  MOV. B #15H, POMCR0; Fixed value
  MOV. B #92H, POMCR0; Fixed value
  MOV. B #25H, POMCR0; Fixed value
  NOP;
  NOP;
  NOP;
  NOP; Enter power-off mode
  WAIT; Wait mode

11. Protection

The protection function protects important registers from being easily overwritten if a program runs out of control. The registers protected by the PRCR register are as follows:

- Registers protected by PRC0 bit: Registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3
- Registers protected by PRC1 bit: Registers PM0 and PM1
- Registers protected by PRC2 bit: PD0 register
- Registers protected by PRC3 bit: Registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C

11.1 Register

11.1.1 Protect Register (PRCR)

Address 000Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	PRC3	PRC2	PRC1	PRC0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 0: Write disabled 1: Write enabled	R/W
b1	PRC1	Protect bit 1	Enables writing to registers PM0 and PM1. 0: Write disabled 1: Write enabled	R/W
b2	PRC2	Protect bit 2	Enables writing to the PD0 register. 0: Write disabled 1: Write enabled (1)	R/W
b3	PRC3	Protect bit 3	Enables writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C. 0: Write disabled 1: Write enabled	R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—	Reserved bits	When read, the content is 0.	R
b7	—			

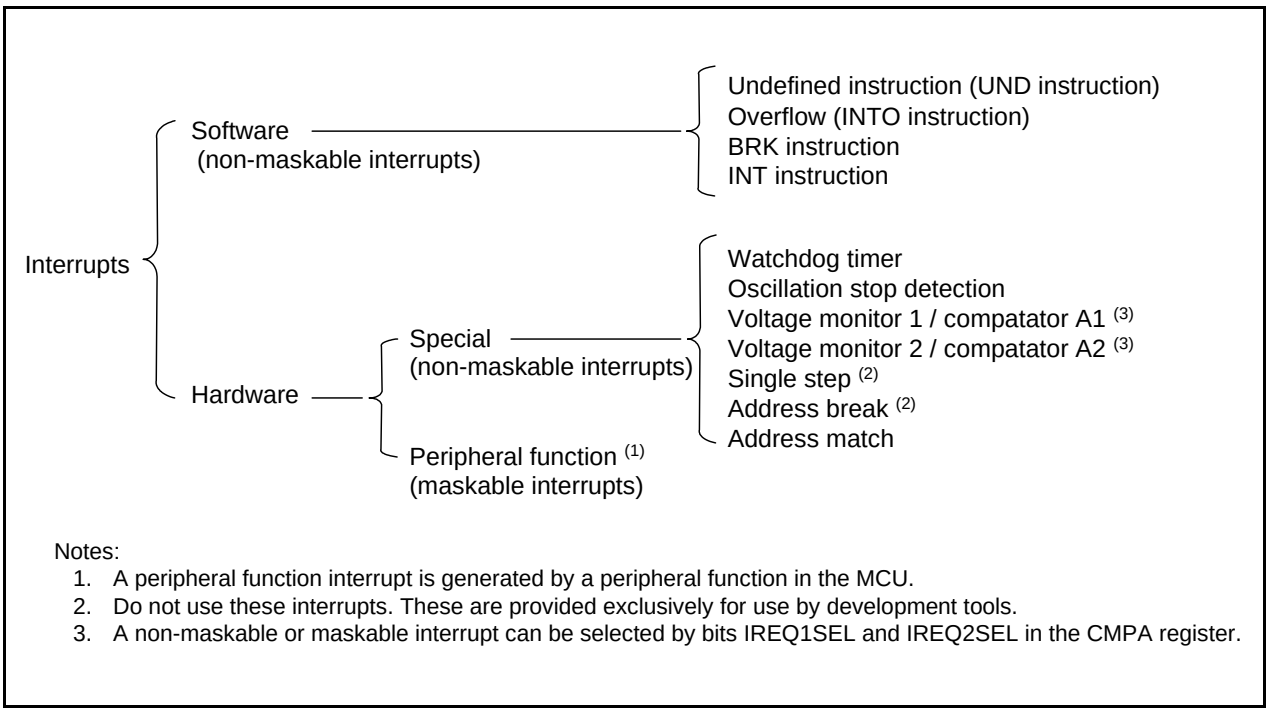
Note:
1. The PRC2 bit is set to 0 after writing 1 to it and executing a write to any address. Since the other bits are not set to 0, set them to 0 by a program.

12. Interrupts

12.1 Introduction

12.1.1 Types of Interrupts

Figure 12.1 shows the Types of Interrupts.



Notes:
1. A peripheral function interrupt is generated by a peripheral function in the MCU.
2. Do not use these interrupts. These are provided exclusively for use by development tools.
3. A non-maskable or maskable interrupt can be selected by bits IREQ1SEL and IREQ2SEL in the CMPA register.

Figure 12.1 Types of Interrupts

- Maskable interrupts: These interrupts are enabled or disabled by the interrupt enable flag (I flag). The interrupt priority **can be changed** based on the interrupt priority level.
- Non-maskable interrupts: These interrupts are not enabled or disabled by the interrupt enable flag (I flag). The interrupt priority **cannot be changed** based on the interrupt priority level.

12.1.2 Software Interrupts

A software interrupt is generated when an instruction is executed. Software interrupts are non-maskable.

12.1.2.1 Undefined Instruction Interrupt

An undefined instruction interrupt is generated when the UND instruction is executed.

12.1.2.2 Overflow Interrupt

An overflow interrupt is generated when the O flag is set to 1 (arithmetic operation overflow) and the INTO instruction is executed. Instructions that set the O flag are as follows:
ABS, ADC, ADCF, ADD, CMP, DIV, DIVU, DIVX, NEG, RMPA, SBB, SHA, and SUB.

12.1.2.3 BRK Interrupt

A BRK interrupt is generated when the BRK instruction is executed.

12.1.2.4 INT Instruction Interrupt

An INT instruction interrupt is generated when the INT instruction is executed. Software interrupt numbers 0 to 63 can be specified with the INT instruction. Because software interrupt numbers are assigned to peripheral function interrupts, the same interrupt routine as for peripheral function interrupts can be executed by executing the INT instruction.
For software interrupt numbers 0 to 31, the U flag is saved on the stack during instruction execution and the U flag is set to 0 (ISP selected) before the interrupt sequence is executed. The U flag is restored from the stack when returning from the interrupt routine. For software interrupt numbers 32 to 63, the U flag does not change state during instruction execution, and the selected SP is used.

12.1.3 Special Interrupts

Special interrupts are non-maskable.

12.1.3.1 Watchdog Timer Interrupt

A watchdog timer interrupt is generated by the watchdog timer. For details, refer to **15. Watchdog Timer**.

12.1.3.2 Oscillation Stop Detection Interrupt

An oscillation stop detection interrupt is generated by the oscillation stop detection function. For details of the oscillation stop detection function, refer to **9. Clock Generation Circuit**.

12.1.3.3 Voltage Monitor 1/Comparator A1 Interrupt

A voltage monitor 1/Comparator A1 interrupt is generated by the voltage detection circuit or the comparator A. A non-maskable or maskable interrupt can be selected by IRQ1SEL bit in the CMPA register. For details of the voltage detection circuit, refer to **6. Voltage Detection Circuit** and for details of the comparator A, refer to **32. Comparator A**.

12.1.3.4 Voltage Monitor 2/Comparator A2 Interrupt

A voltage monitor 2/Comparator A2 interrupt is generated by the voltage detection circuit or the comparator A. A non-maskable or maskable interrupt can be selected by IRQ2SEL bit in the CMPA register. For details of the voltage detection circuit, refer to **6. Voltage Detection Circuit** and for details of the comparator A, refer to **32. Comparator A**.

12.1.3.5 Single-Step Interrupt, Address Break Interrupt

Do not use these interrupts. They are provided exclusively for use by development tools.

12.1.3.6 Address Match Interrupt

An address match interrupt is generated immediately before executing an instruction that is stored at an address indicated by registers RMAD0 to RMAD1 if the AIER0 bit in the AIER0 register or AIER1 bit in the AIER1 register is set to 1 (address match interrupt enabled).
For details of the address match interrupt, refer to **12.6 Address Match Interrupt**.

12.1.4 Peripheral Function Interrupts

A peripheral function interrupt is generated by a peripheral function in the MCU. Peripheral function interrupts are maskable. Refer to **Table 12.2 Relocatable Vector Tables** for sources of the corresponding peripheral function interrupt. For details of peripheral functions, refer to the descriptions of individual peripheral functions.

12.1.5 Interrupts and Interrupt Vectors

There are 4 bytes in each vector. Set the starting address of an interrupt routine in each interrupt vector. When an interrupt request is acknowledged, the CPU branches to the address set in the corresponding interrupt vector. Figure 12.2 shows an Interrupt Vector.

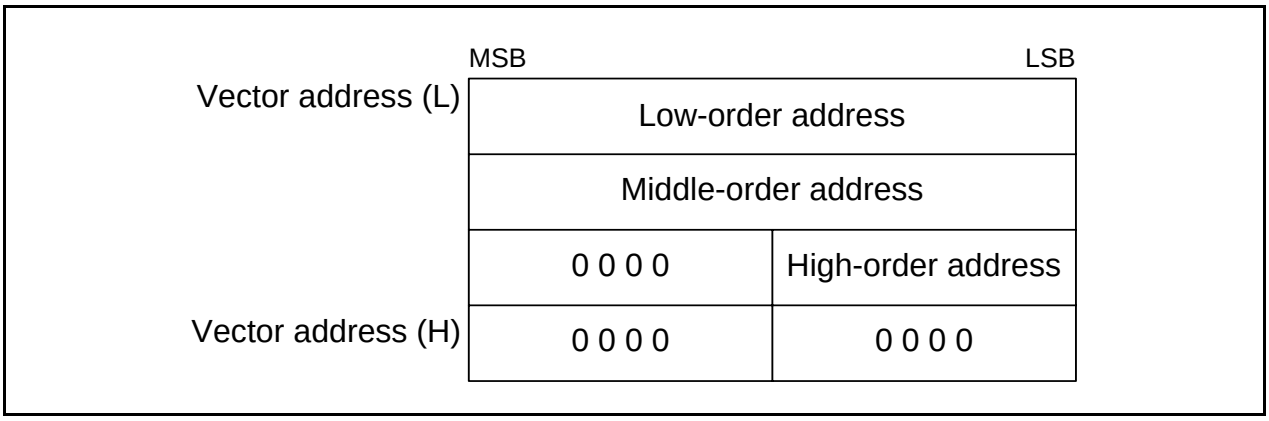


Figure 12.2 Interrupt Vector

12.1.5.1 Fixed Vector Tables

The fixed vector tables are allocated addresses 0FFDCh to 0FFFFh.
Table 12.1 lists the Fixed Vector Tables. The vector addresses (H) of fixed vectors are used by the ID code check function. For details, refer to **35.3 Functions to Prevent Flash Memory from being Rewritten**.

Table 12.1 Fixed Vector Tables

Interrupt Source	Vector Addresses Address (L) to (H)	Remarks	Reference
Undefined instruction	0FFDCh to 0FFDFh	Interrupt with UND instruction	R8C/Tiny Series Software Manual
Overflow	0FFE0h to 0FFE3h	Interrupt with INTO instruction	
BRK instruction	0FFE4h to 0FFE7h	If the content of address 0FFE7h is FFh, program execution starts from the address shown by the vector in the relocatable vector table.	
Address match	0FFE8h to 0FFEBh		12.6 Address Match Interrupt
Single step (1)	0FFECh to 0FFEFh		
Watchdog timer, Oscillation stop detection, Voltage monitor 1/ comparator A1, Voltage monitor 2/ comparator A2	0FFF0h to 0FFF3h		15. Watchdog Timer, 9. Clock Generation Circuit, 6. Voltage Detection Circuit, 32. Comparator A
Address break (1)	0FFF4h to 0FFF7h		
(Reserved)	0FFF8h to 0FFFBh		
Reset	0FFFCh to 0FFFFh		5. Resets

Note:
1. Do not use these interrupts. They are provided exclusively for use by development tools.

12.1.5.2 Relocatable Vector Tables

The relocatable vector tables occupy 256 bytes beginning from the starting address set in the INTB register. Table 12.2 lists the Relocatable Vector Tables.

Table 12.2 Relocatable Vector Tables

Interrupt Source	Vector Addresses (1) Address (L) to Address (H)	Software Interrupt Number	Interrupt Control Register	Reference
BRK instruction (3)	+0 to +3 (0000h to 0003h)	0	–	R8C/Tiny Series Software Manual
Flash memory ready	+4 to +7 (0004h to 0007h)	1	FMRDYIC	35. Flash Memory
(Reserved)		2	–	–
$\overline{\text{INT7}}$	+12 to +15 (000Ch to 000Fh)	3	INT7IC	12.4 $\overline{\text{INT}}$ Interrupt
$\overline{\text{INT6}}$	+16 to +19 (0010h to 0013h)	4	INT6IC	12.4 $\overline{\text{INT}}$ Interrupt
$\overline{\text{INT5}}$	+20 to +23 (0014h to 0017h)	5	INT5IC	12.4 $\overline{\text{INT}}$ Interrupt
$\overline{\text{INT4}}$	+24 to +27 (0018h to 001Bh)	6	INT4IC	12.4 $\overline{\text{INT}}$ Interrupt
Timer RC	+28 to +31 (001Ch to 001Fh)	7	TRCIC	20. Timer RC
Timer RD0	+32 to +35 (0020h to 0023h)	8	TRD0IC	21. Timer RD
Timer RD1	+36 to +39 (0024h to 0027h)	9	TRD1IC	
Timer RE	+40 to +43 (0028h to 002Bh)	10	TREIC	22. Timer RE
UART2 transmission/NACK2	+44 to +47 (002Ch to 002Fh)	11	S2TIC	25. Serial Interface (UART2)
UART2 reception/ACK2	+48 to +51 (0030h to 0033h)	12	S2RIC	
Key input	+52 to +55 (0034h to 0037h)	13	KUPIC	12.5 Key Input Interrupt
A/D conversion	+56 to +59 (0038h to 003Bh)	14	ADIC	30. A/D Converter
Synchronous serial communication unit/ I^2C bus interface (2)	+60 to +63 (003Ch to 003Fh)	15	SSUIC/IICIC	27. Synchronous Serial Communication Unit (SSU), 28. I^2C bus Interface
(Reserved)		16	–	–
UART0 transmission	+68 to +71 (0044h to 0047h)	17	S0TIC	24. Serial Interface (UARTi (i = 0 or 1))
UART0 reception	+72 to +75 (0048h to 004Bh)	18	S0RIC	
UART1 transmission	+76 to +79 (004Ch to 004Fh)	19	S1TIC	
UART1 reception	+80 to +83 (0050h to 0053h)	20	S1RIC	
$\overline{\text{INT2}}$	+84 to +87 (0054h to 0057h)	21	INT2IC	12.4 $\overline{\text{INT}}$ Interrupt
Timer RA	+88 to +91 (0058h to 005Bh)	22	TRAIC	18. Timer RA
(Reserved)		23	–	–
Timer RB	+96 to +99 (0060h to 0063h)	24	TRBIC	19. Timer RB
$\overline{\text{INT1}}$	+100 to +103 (0064h to 0067h)	25	INT1IC	12.4 $\overline{\text{INT}}$ Interrupt
$\overline{\text{INT3}}$	+104 to +107 (0068h to 006Bh)	26	INT3IC	
(Reserved)		27	–	–
(Reserved)		28	–	–
$\overline{\text{INT0}}$	+116 to +119 (0074h to 0077h)	29	INT0IC	12.4 $\overline{\text{INT}}$ Interrupt
UART2 bus collision detection	+120 to +123 (0078h to 007Bh)	30	U2BCNIC	25. Serial Interface (UART2)
(Reserved)		31	–	–
Software (3)	+128 to +131 (0080h to 0083h) to +164 to +167 (00A4h to 00A7h)	32 to 41	–	R8C/Tiny Series Software Manual
(Reserved)		42	–	–
Timer RG	+172 to +175 (00ACh to 00AFh)	43	TRGIC	23. Timer RG
(Reserved)		44 to 49	–	–
Voltage monitor 1/comparator A1	+200 to +203 (00C8h to 00CBh)	50	VCMP1IC	6. Voltage Detection Circuit 32. Comparator A
Voltage monitor 2/comparator A2	+204 to +207 (00CCh to 00CFh)	51	VCMP2IC	
(Reserved)		52 to 55	–	–
Software (3)	+224 to +227 (00E0h to 00E3h) to +252 to +255 (00FCh to 00FFh)	56 to 63	–	R8C/Tiny Series Software Manual

Notes:
1. These addresses are relative to those in the INTB register.
2. Selectable by the IICSEL bit in the SSUIICSR register.
3. These interrupts are not disabled by the I flag.

12.2 Registers

12.2.1 Interrupt Control Register (TREIC, S2TIC, S2RIC, KUPIC, ADIC, S0TIC, S0RIC, S1TIC, S1RIC, TRAIC, TRBIC, U2BCNIC, VCMP1IC, VCMP2IC)

Address 004Ah (TREIC), 004Bh (S2TIC), 004Ch (S2RIC), 004Dh (KUPIC), 004Eh (ADIC), 0051h (S0TIC), 0052h (S0RIC), 0053h (S1TIC), 0054h (S1RIC), 0056h (TRAIC), 0058h (TRBIC), 005Eh (U2BCNIC), 0072h (VCMP1IC), 0073h (VCMP2IC),

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	IR	ILVL2	ILVL1	ILVL0
After Reset	X	X	X	X	X	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled) 0 0 1: Level 1 0 1 0: Level 2 0 1 1: Level 3 1 0 0: Level 4 1 0 1: Level 5 1 1 0: Level 6 1 1 1: Level 7	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R/W (1)
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b5	—			
b6	—			
b7	—			

Note:
1. Only 0 can be written to the IR bit. Do not write 1 to this bit.

Rewrite the interrupt control register when an interrupt request corresponding to the register is not generated. Refer to **12.8.5 Rewriting Interrupt Control Register**.

12.2.2 Interrupt Control Register (FMRDYIC, TRCIC, TRD0IC, TRD1IC, SSUIC/IICIC, TRGIC)

Address 0041h (FMRDYIC), 0047h (TRCIC), 0048h (TRD0IC), 0049h (TRD1IC), 004Fh (SSUIC/IICIC (Note 1)), 006Bh (TRGIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	IR	ILVL2	ILVL1	ILVL0
After Reset	X	X	X	X	X	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled) 0 0 1: Level 1 0 1 0: Level 2 0 1 1: Level 3 1 0 0: Level 4 1 0 1: Level 5 1 1 0: Level 6 1 1 1: Level 7	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R/W (1)
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b5	—			
b6	—			
b7	—			

Note:
1. Selectable by the IICSEL bit in the SSUIICSR register.

Rewrite the interrupt control register when an interrupt request corresponding to the register is not generated. Refer to **12.8.5 Rewriting Interrupt Control Register**.

12.2.3 INTi Interrupt Control Register (INTiIC) (i = 0 to 7)

Address 0043h (INT7IC), 0044h (INT6IC), 0045h (INT5IC), 0046h (INT4IC),
0055h (INT2IC), 0059h (INT1IC), 005Ah (INT3IC), 005Dh (INT0IC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	POL	IR	ILVL2	ILVL1	ILVL0
After Reset	X	X	0	0	X	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled) 0 0 1: Level 1 0 1 0: Level 2 0 1 1: Level 3 1 0 0: Level 4 1 0 1: Level 5 1 1 0: Level 6 1 1 1: Level 7	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R/W (1)
b4	POL	Polarity switch bit (3)	0: Falling edge selected 1: Rising edge selected (2)	R/W
b5	—	Reserved bit	Set to 0.	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b7	—			

Notes:
1. Only 0 can be written to the IR bit. Do not write 1 to this bit.
2. When the INTiPL bit in the INTEN register is set to 1 (both edges), set the POL bit to 0 (falling edge selected).
3. The IR bit may be set to 1 (interrupt requested) when the POL bit is rewritten. Refer to **12.8.4 Changing Interrupt Sources**.

Rewrite the interrupt control register when an interrupt request corresponding to the register is not generated. Refer to **12.8.5 Rewriting Interrupt Control Register**.

12.3 Interrupt Control

The following describes enabling and disabling maskable interrupts and setting the acknowledgement priority. This description does not apply to non-maskable interrupts.
Use the I flag in the FLG register, IPL, and bits ILVL2 to ILVL0 in the corresponding interrupt control register to enable or disable a maskable interrupt. Whether an interrupt is requested or not is indicated by the IR bit in the corresponding interrupt control register.

12.3.1 I Flag

The I flag enables or disables maskable interrupts. Setting the I flag to 1 (enabled) enables maskable interrupts. Setting the I flag to 0 (disabled) disables all maskable interrupts.

12.3.2 IR Bit

The IR bit is set to 1 (interrupt requested) when an interrupt request is generated. After the interrupt request is acknowledged and the CPU branches to the corresponding interrupt vector, the IR bit is set to 0 (no interrupt requested).
The IR bit can be set to 0 by a program. Do not write 1 to this bit.
However, the IR bit operations of the timer RC interrupt, the timer RD interrupt, the synchronous serial communication unit interrupt the I^2C bus interface interrupt, and the flash memory interrupt are different. Refer to **12.7 Interrupts of Timer RC, Timer RD, Timer RG, Synchronous Serial Communication Unit, I^2C bus Interface, and Flash Memory (Interrupts with Multiple Interrupt Request Sources)**.

12.3.3 Bits ILVL2 to ILVL0, IPL

Interrupt priority levels can be set using bits ILVL2 to ILVL0.
Table 12.3 lists the Settings of Interrupt Priority Levels and Table 12.4 lists the Interrupt Priority Levels Enabled by IPL.

The following are the conditions when an interrupt is acknowledged:

- I flag = 1
- IR bit = 1
- Interrupt priority level > IPL

The I flag, IR bit, bits ILVL2 to ILVL0, and IPL are independent of each other. They do not affect one another.

Table 12.3 Settings of Interrupt Priority Levels

Bits ILVL2 to ILVL0	Interrupt Priority Level	Priority
000b	Level 0 (interrupt disabled)	–
001b	Level 1	Low
010b	Level 2	↓
011b	Level 3	↓
100b	Level 4	↓
101b	Level 5	↓
110b	Level 6	↓
111b	Level 7	High

Table 12.4 Interrupt Priority Levels Enabled by IPL

IPL	Enabled Interrupt Priority Level
000b	Interrupt level 1 and above
001b	Interrupt level 2 and above
010b	Interrupt level 3 and above
011b	Interrupt level 4 and above
100b	Interrupt level 5 and above
101b	Interrupt level 6 and above
110b	Interrupt level 7 and above
111b	All maskable interrupts disabled

12.3.4 Interrupt Sequence

The following describes an interrupt sequence which is performed from when an interrupt request is acknowledged until the interrupt routine is executed.
When an interrupt request is generated while an instruction is being executed, the CPU determines its interrupt priority level after the instruction is completed. The CPU starts the interrupt sequence from the following cycle. However, for the SMOVB, SMOVF, SSTR, or RMPA instruction, if an interrupt request is generated while the instruction is being executed, the MCU suspends the instruction to start the interrupt sequence. The interrupt sequence is performed as indicated below.
Figure 12.3 shows the Time Required for Executing Interrupt Sequence.

(1) The CPU obtains interrupt information (interrupt number and interrupt request level) by reading address 00000h. The IR bit for the corresponding interrupt is set to 0 (no interrupt requested). (2)
(2) The FLG register is saved to a temporary register (1) in the CPU immediately before entering the interrupt sequence.
(3) The I, D and U flags in the FLG register are set as follows:
The I flag is set to 0 (interrupts disabled).
The D flag is set to 0 (single-step interrupt disabled).
The U flag is set to 0 (ISP selected).
However, the U flag does not change state if an INT instruction for software interrupt number 32 to 63 is executed.
(4) The CPU internal temporary register (1) is saved on the stack.
(5) The PC is saved on the stack.
(6) The interrupt priority level of the acknowledged interrupt is set in the IPL.
(7) The starting address of the interrupt routine set in the interrupt vector is stored in the PC.

After the interrupt sequence is completed, instructions are executed from the starting address of the interrupt routine.

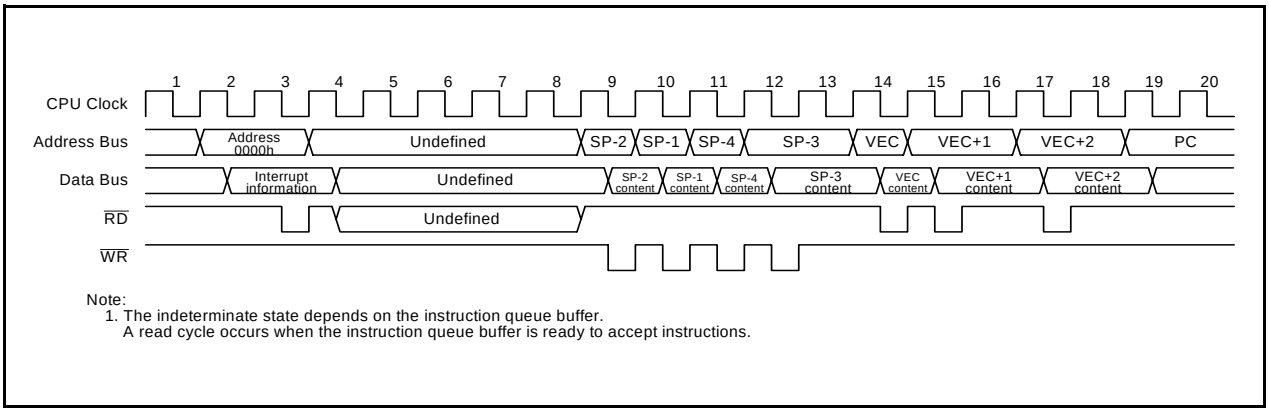
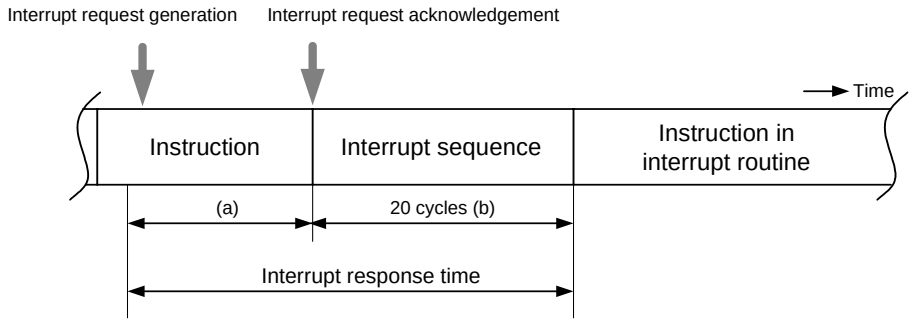


Figure 12.3 Time Required for Executing Interrupt Sequence

Notes:
1. These registers cannot be accessed by the user.
2. Refer to **12.7 Interrupts of Timer RC, Timer RD, Timer RG, Synchronous Serial Communication Unit, I²C bus Interface, and Flash Memory (Interrupts with Multiple Interrupt Request Sources)** for the IR bit operations of the above interrupts.

12.3.5 Interrupt Response Time

Figure 12.4 shows the Interrupt Response Time. The interrupt response time is the period from when an interrupt request is generated until the first instruction in the interrupt routine is executed. The interrupt response time includes the period from when an interrupt request is generated until the currently executing instruction is completed (refer to (a) in Figure 12.4) and the period required for executing the interrupt sequence (20 cycles, refer to (b) in Figure 12.4).



(a) The period from when an interrupt request is generated until the currently executing instruction is completed. The length of time varies depending on the instruction being executed. The DIVX instruction requires the longest time, 30 cycles (no wait states if the divisor is a register).
(b) 21 cycles for address match and single-step interrupts.

Figure 12.4 Interrupt Response Time

12.3.6 IPL Change when Interrupt Request is Acknowledged

When a maskable interrupt request is acknowledged, the interrupt priority level of the acknowledged interrupt is set in the IPL.
When a software interrupt or special interrupt request is acknowledged, the level listed in Table 12.5 is set in the IPL.
Table 12.5 lists the IPL Value When Software or Special Interrupt is Acknowledged.

Table 12.5 IPL Value When Software or Special Interrupt is Acknowledged

Interrupt Source without Interrupt Priority Level	Value Set in IPL
Watchdog timer, oscillation stop detection, voltage monitor 1/comparator A1, voltage monitor 2/comparator A2, address break	7
Software, address match, single-step	No change

12.3.7 Saving Registers

In the interrupt sequence, the FLG register and PC are saved on the stack.
After an extended 16 bits, 4 high-order bits in the PC and 4 high-order (IPL) and 8 low-order bits in the FLG register, are saved on the stack, the 16 low-order bits in the PC are saved.
Figure 12.5 shows the Stack State Before and After Acknowledgement of Interrupt Request.
The other necessary registers should be saved by a program at the beginning of the interrupt routine. The PUSHM instruction can save several registers in the register bank being currently used (1) with a single instruction.

Note:
1. Selectable from registers R0, R1, R2, R3, A0, A1, SB, and FB.

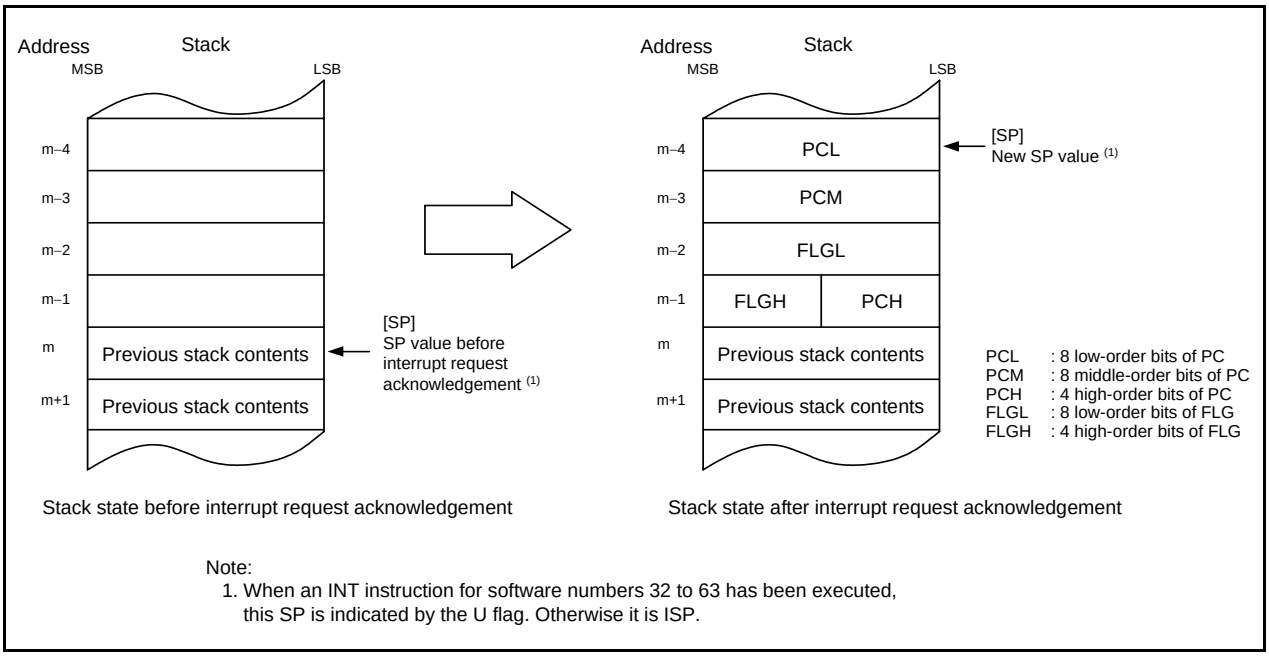
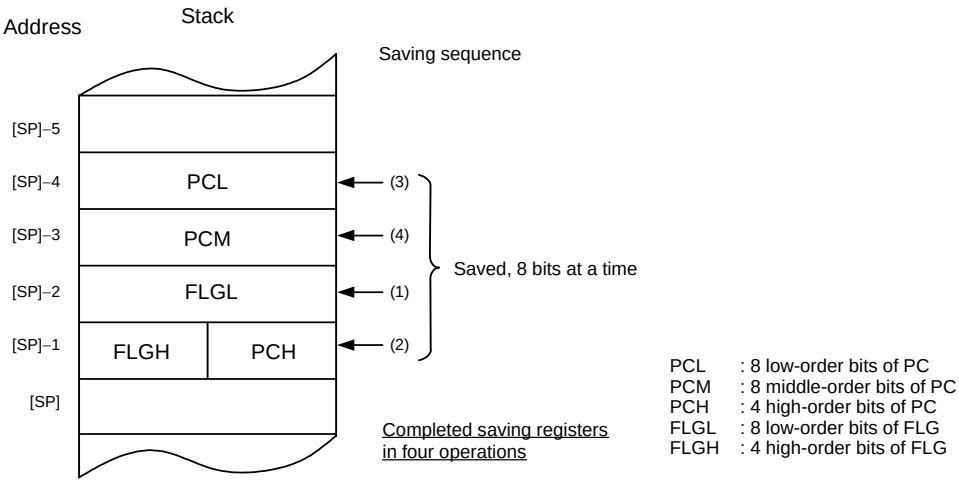


Figure 12.5 Stack State Before and After Acknowledgement of Interrupt Request

The register saving operation, which is performed as part of the interrupt sequence, saved in 8 bits at a time in four steps.
Figure 12.6 shows the Register Saving Operation.



Note:
1. [SP] indicates the SP initial value when an interrupt request is acknowledged.
After registers are saved, the SP content is [SP] minus 4.
When an INT instruction for software numbers 32 to 63 has been executed,
this SP is indicated by the U flag. Otherwise it is ISP.

Figure 12.6 Register Saving Operation

12.3.8 Returning from Interrupt Routine

When the REIT instruction is executed at the end of an interrupt routine, the FLG register and PC, which have been saved on the stack, are automatically restored. The program, that was running before the interrupt request was acknowledged, starts running again.

Registers saved by a program in an interrupt routine should be saved using the POPM instruction or a similar instruction before executing the REIT instruction.

12.3.9 Interrupt Priority

If two or more interrupt requests are generated while a single instruction is being executed, the interrupt with the higher priority is acknowledged.

Set bits ILVL2 to ILVL0 to select any priority level for maskable interrupts (peripheral function). However, if two or more maskable interrupts have the same priority level, their interrupt priority is resolved by hardware, with the higher priority interrupts acknowledged.

The priority of the watchdog timer and other special interrupts is set by hardware.

Figure 12.7 shows the Hardware Interrupt Priority.

Software interrupts are not affected by the interrupt priority. When an instruction is executed, the MCU executes the interrupt routine.

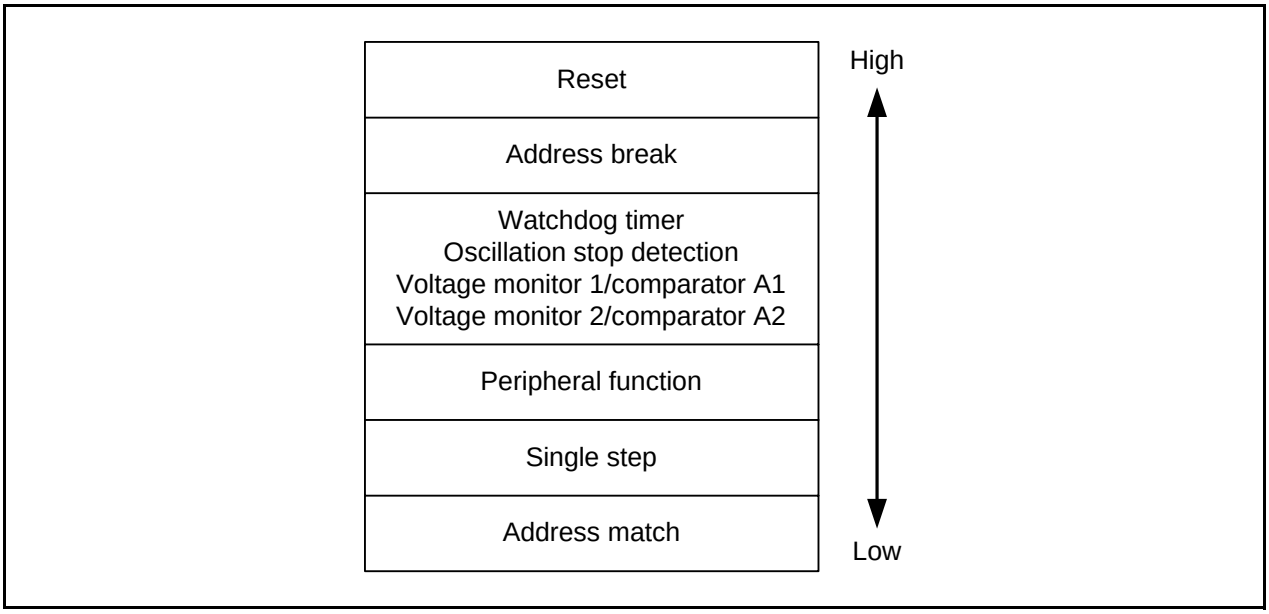


Figure 12.7 Hardware Interrupt Priority

12.3.10 Interrupt Priority Level Selection Circuit

The interrupt priority level selection circuit is used to select the highest priority interrupt. Figure 12.8 shows the Interrupt Priority Level Selection Circuit.

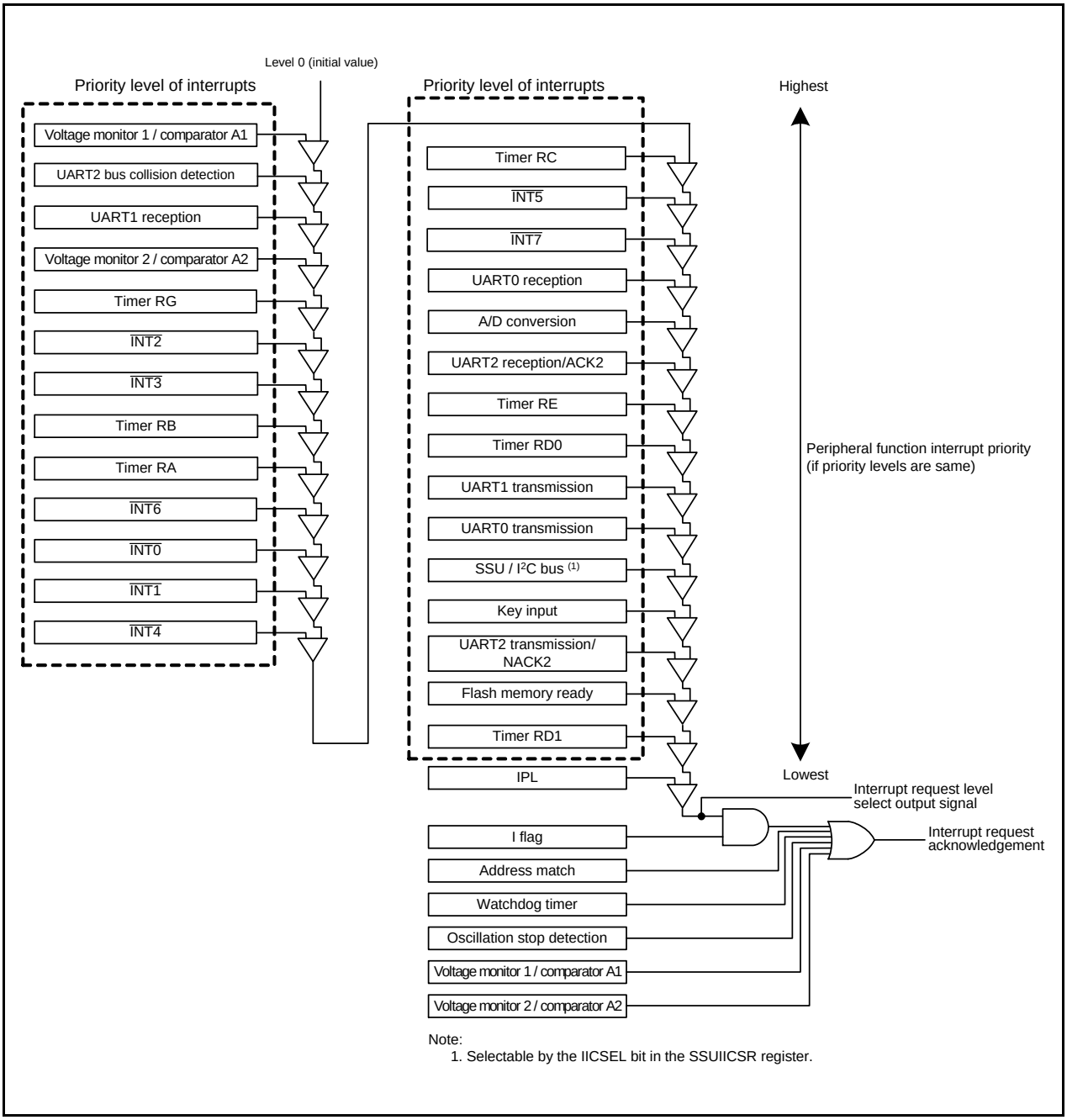


Figure 12.8 Interrupt Priority Level Selection Circuit

12.4 $\overline{\text{INT}}$ Interrupt

12.4.1 $\overline{\text{INTi}}$ Interrupt (i = 0 to 7)

The $\overline{\text{INTi}}$ interrupt is generated by an $\overline{\text{INTi}}$ input. To use the $\overline{\text{INTi}}$ interrupt, set the INTiEN bit in the INTEN register is to 1 (enabled). The edge polarity is selected using the INTiPL bit in the INTEN register and the POL bit in the INTiIC register. The input pin used as the $\overline{\text{INTi}}$ input can be selected.
Also, inputs can be passed through a digital filter with three different sampling clocks.
The $\overline{\text{INT0}}$ pin is shared with the pulse output forced cutoff input of timer RC and timer RD, and the external trigger input of timer RB.
Table 12.6 lists the Pin Configuration of $\overline{\text{INT}}$ Interrupt.

Table 12.6 Pin Configuration of $\overline{\text{INT}}$ Interrupt

Pin Name	Assigned Pin	I/O	Function
$\overline{\text{INT0}}$	P3_0 or P11_0	Input	$\overline{\text{INT0}}$ interrupt input, timer RB external trigger input, timer RC and timer RD pulse output forced cutoff input
$\overline{\text{INT1}}$	P3_1 or P11_1	Input	$\overline{\text{INT1}}$ interrupt input
$\overline{\text{INT2}}$	P3_2 or P11_2	Input	$\overline{\text{INT2}}$ interrupt input
$\overline{\text{INT3}}$	P3_3 or P11_3	Input	$\overline{\text{INT3}}$ interrupt input
$\overline{\text{INT4}}$	P3_4 or P11_4	Input	$\overline{\text{INT4}}$ interrupt input
$\overline{\text{INT5}}$	P3_5 or P11_5	Input	$\overline{\text{INT5}}$ interrupt input
$\overline{\text{INT6}}$	P3_6 or P11_6	Input	$\overline{\text{INT6}}$ interrupt input
$\overline{\text{INT7}}$	P3_7 or P11_7	Input	$\overline{\text{INT7}}$ interrupt input

12.4.2 INT Interrupt Input Pin Select Register (INTSR)

Address 018Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT7SEL0	INT6SEL0	INT5SEL0	INT4SEL0	INT3SEL0	INT2SEL0	INT1SEL0	INT0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0SEL0	$\overline{\text{INT0}}$ pin select bit	0: P3_0 assigned 1: P11_0 assigned	R/W
b1	INT1SEL0	$\overline{\text{INT1}}$ pin select bit	0: P3_1 assigned 1: P11_1 assigned	R/W
b2	INT2SEL0	$\overline{\text{INT2}}$ pin select bit	0: P3_2 assigned 1: P11_2 assigned	R/W
b3	INT3SEL0	$\overline{\text{INT3}}$ pin select bit	0: P3_3 assigned 1: P11_3 assigned	R/W
b4	INT4SEL0	$\overline{\text{INT4}}$ pin select bit	0: P3_4 assigned 1: P11_4 assigned	R/W
b5	INT5SEL0	$\overline{\text{INT5}}$ pin select bit	0: P3_5 assigned 1: P11_5 assigned	R/W
b6	INT6SEL0	$\overline{\text{INT6}}$ pin select bit	0: P3_6 assigned 1: P11_6 assigned	R/W
b7	INT7SEL0	$\overline{\text{INT7}}$ pin select bit	0: P3_7 assigned 1: P11_7 assigned	R/W

The INTSR register selects which pin is assigned as the $\overline{\text{INTi}}$ (i = 1 to 7) input. To use the $\overline{\text{INTi}}$, set this register. Set the INTSR register before setting the $\overline{\text{INTi}}$ associated registers. Also, do not change the setting values in this register during $\overline{\text{INTi}}$ operation.

12.4.3 External Input Enable Register 0 (INTEN)

Address 01FAh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3PL	INT3EN	INT2PL	INT2EN	INT1PL	INT1EN	INT0PL	INT0EN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0EN	$\overline{\text{INT0}}$ input enable bit	0: Disabled 1: Enabled	R/W
b1	INT0PL	$\overline{\text{INT0}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b2	INT1EN	$\overline{\text{INT1}}$ input enable bit	0: Disabled 1: Enabled	R/W
b3	INT1PL	$\overline{\text{INT1}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b4	INT2EN	$\overline{\text{INT2}}$ input enable bit	0: Disabled 1: Enabled	R/W
b5	INT2PL	$\overline{\text{INT2}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b6	INT3EN	$\overline{\text{INT3}}$ input enable bit	0: Disabled 1: Enabled	R/W
b7	INT3PL	$\overline{\text{INT3}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W

Notes:
1. To set the INTiPL bit (i = 0 to 3) to 1 (both edges), set the POL bit in the INTiIC register to 0 (falling edge selected).
2. The IR bit in the INTiIC register may be set to 1 (interrupt requested) if the INTiPL bit is rewritten. Refer to **12.8.4 Changing Interrupt Sources**.

12.4.4 External Input Enable Register 1 (INTEN1)

Address 01FBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT7PL	IN7EN	INT6PL	INT6EN	INT5PL	INT5EN	INT4PL	INT4EN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT4EN	$\overline{\text{INT4}}$ input enable bit	0: Disabled 1: Enabled	R/W
b1	INT4PL	$\overline{\text{INT4}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b2	INT5EN	$\overline{\text{INT5}}$ input enable bit	0: Disabled 1: Enabled	R/W
b3	INT5PL	$\overline{\text{INT5}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b4	INT6EN	$\overline{\text{INT6}}$ input enable bit	0: Disabled 1: Enabled	R/W
b5	INT6PL	$\overline{\text{INT6}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b6	IN7EN	$\overline{\text{INT7}}$ input enable bit	0: Disabled 1: Enabled	R/W
b7	INT7PL	$\overline{\text{INT7}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W

Notes:
1. To set the INTiPL bit (i = 4 to 7) to 1 (both edges), set the POL bit in the INTiIC register to 0 (falling edge selected).
2. The IR bit in the INTiIC register may be set to 1 (interrupt requested) if the INTiPL bit is rewritten. Refer to **12.8.4 Changing Interrupt Sources**.

12.4.5 INT Input Filter Select Register 0 (INTF)

Address 01FCh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3F1	INT3F0	INT2F1	INT2F0	INT1F1	INT1F0	INT0F1	INT0F0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0F0	$\overline{\text{INT0}}$ input filter select bit	b1 b0 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b1	INT0F1			R/W
b2	INT1F0	$\overline{\text{INT1}}$ input filter select bit	b3 b2 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b3	INT1F1			R/W
b4	INT2F0	$\overline{\text{INT2}}$ input filter select bit	b5 b4 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b5	INT2F1			R/W
b6	INT3F0	$\overline{\text{INT3}}$ input filter select bit	b7 b6 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b7	INT3F1			R/W

12.4.6 INT Input Filter Select Register 1 (INTF1)

Address 01FDh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT7F1	INT7F0	INT6F1	INT6F0	INT5F1	INT5F0	INT4F1	INT4F0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT4F0	$\overline{\text{INT4}}$ input filter select bit	b1 b0 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b1	INT4F1			R/W
b2	INT5F0	$\overline{\text{INT5}}$ input filter select bit	b3 b2 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b3	INT5F1			R/W
b4	INT6F0	$\overline{\text{INT6}}$ input filter select bit	b5 b4 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b5	INT6F1			R/W
b6	INT7F0	$\overline{\text{INT7}}$ input filter select bit	b7 b6 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b7	INT7F1			R/W

12.4.7 $\overline{\text{INTi}}$ Input Filter (i = 0 to 7)

The $\overline{\text{INTi}}$ input contains a digital filter. The sampling clock is selected using bits INTiF0 and INTiF1 in the INTF register. The $\overline{\text{INTi}}$ level is sampled every sampling clock cycle and if the sampled input level matches three times, the IR bit in the INTiIC register is set to 1 (interrupt requested).

Figure 12.9 shows the $\overline{\text{INTi}}$ Input Filter Configuration. Figure 12.10 shows an Operating Example of $\overline{\text{INTi}}$ Input Filter.

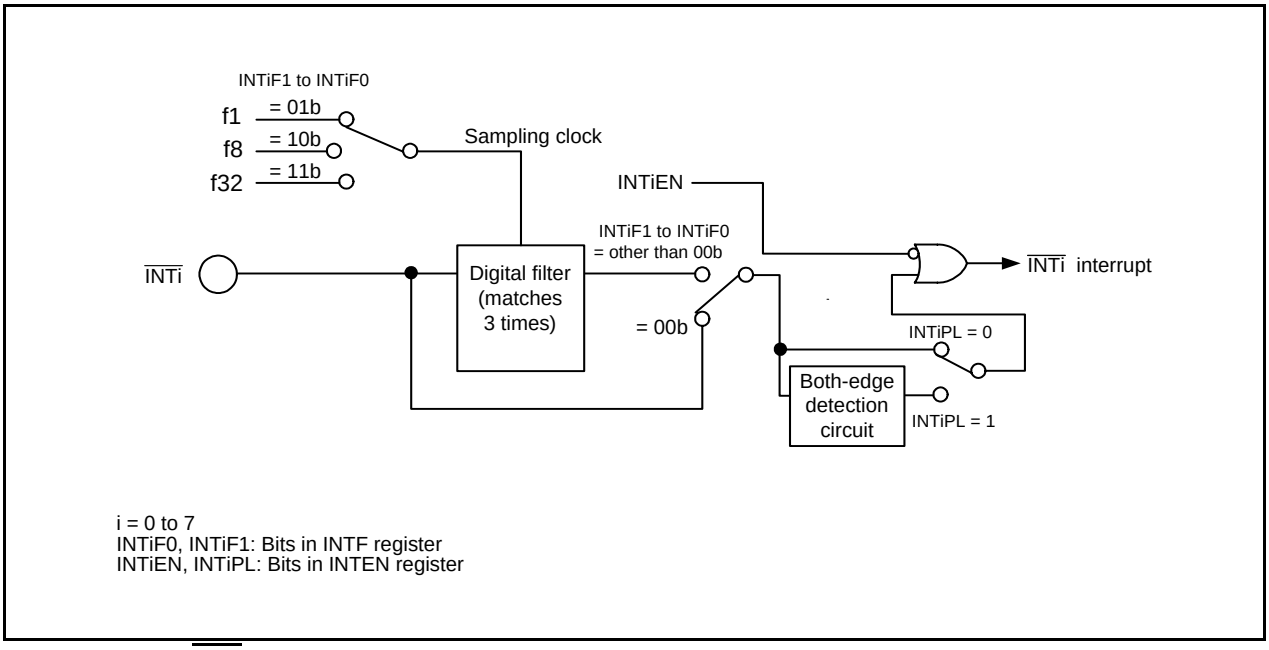


Figure 12.9 $\overline{\text{INTi}}$ Input Filter Configuration

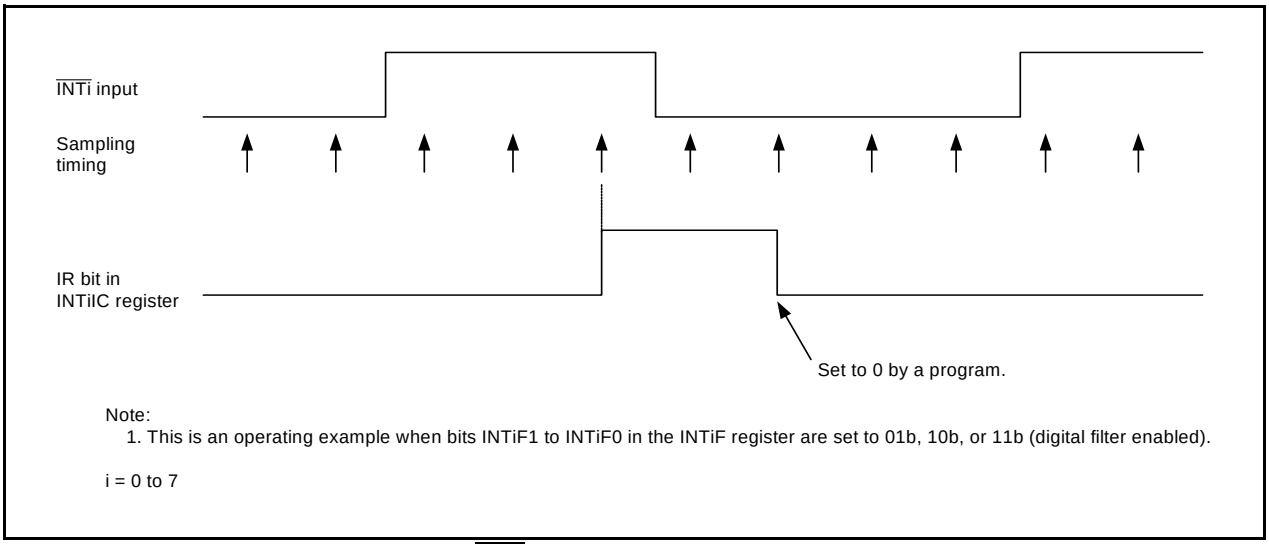


Figure 12.10 Operating Example of $\overline{\text{INTi}}$ Input Filter

12.5 Key Input Interrupt

A key input interrupt request is generated by one of the input edges of pins $\overline{K10}$ to $\overline{K17}$. The key input interrupt can be used as a key-on wake-up function to exit wait or stop mode.

The KIiEN bit (i = 0 to 7) in the KIEN register is be used to select whether or not the pins are used as the $\overline{KIi}$ input. The KIiPL bit in the KIEN register is also be used to select the input polarity.

When inputting a low signal to the $\overline{KIi}$ pin, which sets the KIiPL bit to 0 (falling edge), the input to the other pins $\overline{K10}$ to $\overline{K17}$ is not detected as interrupts. When inputting a high signal to the $\overline{KIi}$ pin, which sets the KIiPL bit to 1 (rising edge), the input to the other pins $\overline{K10}$ to $\overline{K17}$ is also not detected as interrupts.

Figure 12.11 shows a Block Diagram of Key Input Interrupt. Table 12.7 lists the Key Input Interrupt Pin Configuration.

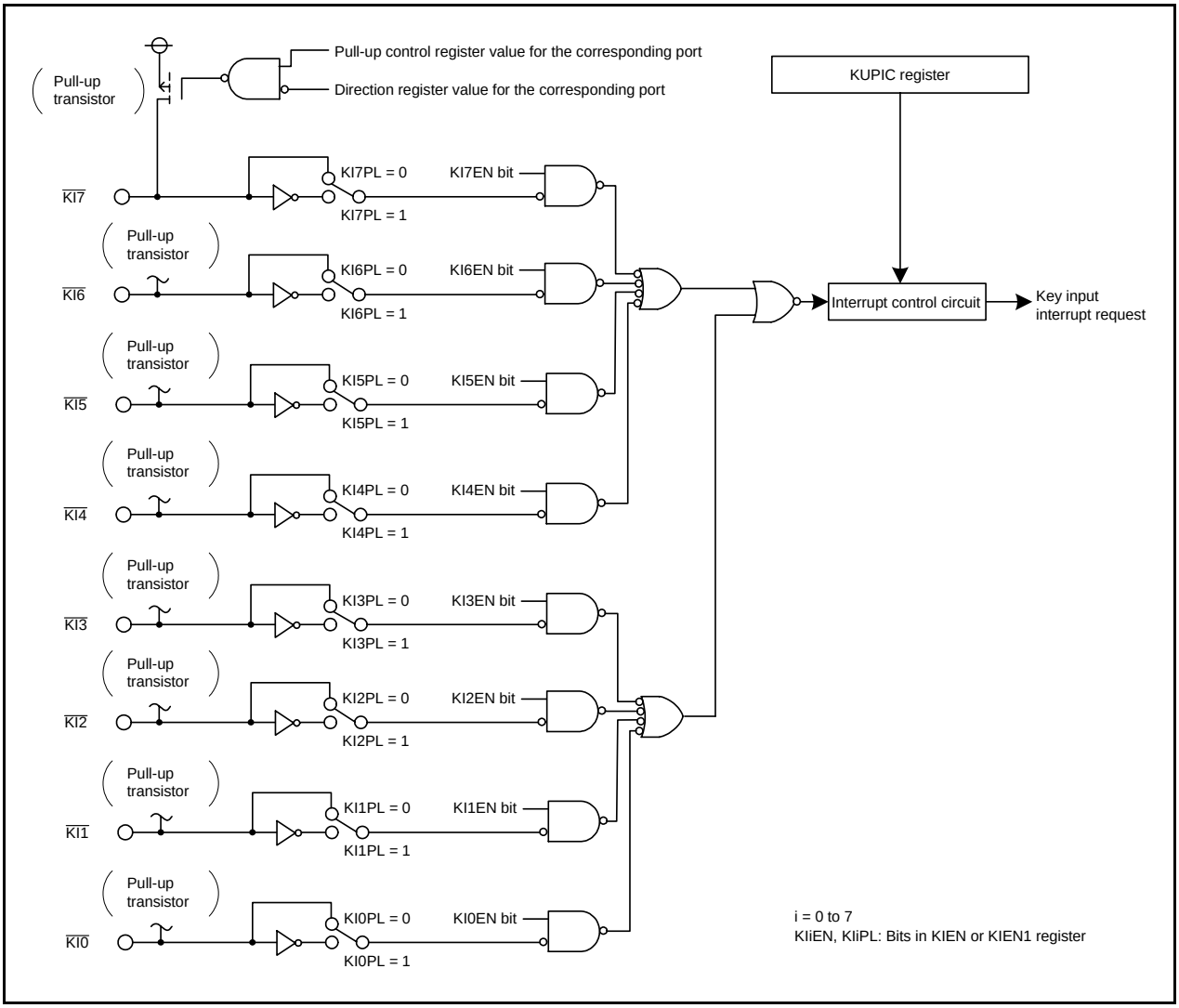


Figure 12.11 Block Diagram of Key Input Interrupt

Table 12.7 Key Input Interrupt Pin Configuration

Pin Name	I/O	Function
$\overline{KI0}$	Input	$\overline{KI0}$ interrupt input
$\overline{KI1}$	Input	$\overline{KI1}$ interrupt input
$\overline{KI2}$	Input	$\overline{KI2}$ interrupt input
$\overline{KI3}$	Input	$\overline{KI3}$ interrupt input
$\overline{KI4}$	Input	$\overline{KI4}$ interrupt input
$\overline{KI5}$	Input	$\overline{KI5}$ interrupt input
$\overline{KI6}$	Input	$\overline{KI6}$ interrupt input
$\overline{KI7}$	Input	$\overline{KI7}$ interrupt input

12.5.1 Key Input Pin Select Register (KISR)

Address 018Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	KI7SEL0	KI6SEL0	KISEL0	KI4SEL0	KI3SEL0	KI2SEL0	KI1SEL0	KI0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	KI0SEL0	$\overline{KI0}$ pin select bit	0: P2_0 assigned 1: P10_0 assigned	R/W
b1	KI1SEL0	$\overline{KI1}$ pin select bit	0: P2_1 assigned 1: P10_1 assigned	R/W
b2	KI2SEL0	$\overline{KI2}$ pin select bit	0: P2_2 assigned 1: P10_2 assigned	R/W
b3	KI3SEL0	$\overline{KI3}$ pin select bit	0: P2_3 assigned 1: P10_3 assigned	R/W
b4	KI4SEL0	$\overline{KI4}$ pin select bit	0: P2_4 assigned 1: P10_4 assigned	R/W
b5	KI5SEL0	$\overline{KI5}$ pin select bit	0: P2_5 assigned 1: P10_5 assigned	R/W
b6	KI6SEL0	$\overline{KI6}$ pin select bit	0: P2_6 assigned 1: P10_6 assigned	R/W
b7	KI7SEL0	$\overline{KI7}$ pin select bit	0: P2_7 assigned 1: P10_7 assigned	R/W

The KISR register selects which pin is assigned as the $\overline{KIi}$ (i = 1 to 7) input. To use the $\overline{KIi}$, set this register. Set the KISR register before setting the $\overline{KIi}$ associated registers. Also, do not change the setting values in this register during $\overline{KIi}$ operation.

12.5.2 Key Input Enable Register 0 (KIEN)

Address 01FEh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	KI3PL	KI3EN	KI2PL	KI2EN	KI1PL	KI1EN	KI0PL	KI0EN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	KI0EN	KI0 input enable bit	0: Disabled 1: Enabled	R/W
b1	KI0PL	KI0 input polarity select bit	0: Falling edge 1: Rising edge	R/W
b2	KI1EN	KI1 input enable bit	0: Disabled 1: Enabled	R/W
b3	KI1PL	KI1 input polarity select bit	0: Falling edge 1: Rising edge	R/W
b4	KI2EN	KI2 input enable bit	0: Disabled 1: Enabled	R/W
b5	KI2PL	KI2 input polarity select bit	0: Falling edge 1: Rising edge	R/W
b6	KI3EN	KI3 input enable bit	0: Disabled 1: Enabled	R/W
b7	KI3PL	KI3 input polarity select bit	0: Falling edge 1: Rising edge	R/W

The IR bit in the KUPIC register may be set to 1 (interrupt requested) when the KIEN register is rewritten. Refer to **12.8.4 Changing Interrupt Sources**.

12.5.3 Key Input Enable Register 1 (KIEN1)

Address 01FFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	KI7PL	KI7EN	KI6PL	KI6EN	KI5PL	KI5EN	KI4PL	KI4EN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	KI4EN	KI4 input enable bit	0: Disabled 1: Enabled	R/W
b1	KI4PL	KI4 input polarity select bit	0: Falling edge 1: Rising edge	R/W
b2	KI5EN	KI5 input enable bit	0: Disabled 1: Enabled	R/W
b3	KI5PL	KI5 input polarity select bit	0: Falling edge 1: Rising edge	R/W
b4	KI6EN	KI6 input enable bit	0: Disabled 1: Enabled	R/W
b5	KI6PL	KI6 input polarity select bit	0: Falling edge 1: Rising edge	R/W
b6	KI7EN	KI7 input enable bit	0: Disabled 1: Enabled	R/W
b7	KI7PL	KI7 input polarity select bit	0: Falling edge 1: Rising edge	R/W

The IR bit in the KUPIC register may be set to 1 (interrupt requested) when the KIEN1 register is rewritten. Refer to **12.8.4 Changing Interrupt Sources**.

12.6 Address Match Interrupt

An address match interrupt request is generated immediately before execution of the instruction at the address indicated by the RMADi (i = 0 or 1) register. This interrupt is used as a break function by the debugger. When the on-chip debugger is used, do not set an address match interrupt (registers AIER0, AIER1, RMAD0, and RMAD1, and fixed vector tables) in the user system.

Set the starting address of any instruction in the RMADi (i = 0 or 1) register. The AIERi bit in the AIERi register can be used to select the interrupt enabled or disabled. The address match interrupt is not affected by the I flag and IPL.

The PC value (refer to **12.3.7 Saving Registers**) which is saved on the stack when an address match interrupt request is acknowledged varies depending on the instruction at the address indicated by the RMADi register. (The appropriate return address is not saved on the stack.) When returning from the address match interrupt, follow one of the following means:

- Rewrite the contents of the stack and use the REIT instruction to return.
- Use an instruction such as POP to restore the stack to its previous state before the interrupt request was acknowledged. Then use a jump instruction to return.

Table 12.8 lists the PC Value Saved on Stack When Address Match Interrupt Request is Acknowledged.

Table 12.8 PC Value Saved on Stack When Address Match Interrupt Request is Acknowledged

Address Indicated by RMADi Register (i = 0 or 1)	PC Value Saved (1)
• Instruction with 2-byte operation code (2) • Instruction with 1-byte operation code (2) ADD.B:S #IMM8,dest SUB.B:S #IMM8,dest AND.B:S #IMM8,dest OR.B:S #IMM8,dest MOV.B:S #IMM8,dest STZ #IMM8,dest STNZ #IMM8,dest STZX #IMM81,#IMM82,dest CMP.B:S #IMM8,dest PUSHM src POPM dest JMPS #IMM8 JSRS #IMM8 MOV.B:S #IMM,dest (however, dest = A0 or A1)	Address indicated by RMADi register + 2
• Instructions other than listed above	Address indicated by RMADi register + 1

Notes:
1. Refer to the **12.3.7 Saving Registers**.
2. Operation code: Refer to the **R8C/Tiny Series Software Manual** (REJ09B0001).
   Chapter 4. Instruction Code/Number of Cycles contains diagrams showing operation code below each syntax. Operation code is shown in the bold frame in the diagrams.

Table 12.9 Correspondence Between Address Match Interrupt Sources and Associated Registers

Address Match Interrupt Source	Address Match Interrupt Enable Bit	Address Match Interrupt Register
Address match interrupt 0	AIER0	RMAD0
Address match interrupt 1	AIER1	RMAD1

12.6.1 Address Match Interrupt Enable Register i (AIERi) (i = 0 or 1)

Address 01C3h (AIER0), 01C7h (AIER1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	—	—	—	—	—	AIER0	AIER0 register
After Reset	0	0	0	0	0	0	0	0	

Symbol	—	—	—	—	—	—	—	AIER1	AIER1 register
After Reset	0	0	0	0	0	0	0	0	

Bit	Symbol	Bit Name	Function	R/W
b0	AIERi	Address match interrupt i enable bit	0: Disabled 1: Enabled	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

12.6.2 Address Match Interrupt Register i (RMADi) (i = 0 or 1)

Address 01C2h to 01C0h (RMAD0), 01C6h to 01C4h (RMAD1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b23	b22	b21	b20	b19	b18	b17	b16
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	X	X	X	X

Bit	Symbol	Function	Setting Range	R/W
b19 to b0	—	Address setting register for address match interrupt	00000h to FFFFFh	R/W
b20	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b21	—			
b22	—			
b23	—			

12.7 Interrupts of Timer RC, Timer RD, Timer RG, Synchronous Serial Communication Unit, I²C bus Interface, and Flash Memory (Interrupts with Multiple Interrupt Request Sources)

The interrupts of timer RC, timer RD (timer RD0) interrupt, timer RD (timer RD1), timer RG, the synchronous serial communication unit, the I²C bus interface, and the flash memory each have multiple interrupt request sources. An interrupt request is generated by the logical OR of several interrupt request sources and is reflected in the IR bit in the corresponding interrupt control register. Therefore, each of these peripheral functions has its own interrupt request source status register (status register) and interrupt request source enable register (enable register) to control the generation of interrupt requests (change of the IR bit in the interrupt control register). Table 12.10 lists the Registers Associated with Interrupts of Timer RC, Timer RD, Timer RG, Synchronous Serial Communication Unit, I²C bus Interface, and Flash Memory and Figure 12.12 shows a Block Diagram of Timer RD Interrupt.

Table 12.10 Registers Associated with Interrupts of Timer RC, Timer RD, Timer RG, Synchronous Serial Communication Unit, I²C bus Interface, and Flash Memory

Peripheral Function Name		Status Register of Interrupt Request Source	Enable Register of Interrupt Request Source	Interrupt Control Register
Timer RC		TRCSR	TRCIER	TRCIC
Timer RD	Timer RD0	TRDSR0	TRDIER0	TRD0IC
	Timer RD1	TRDSR1	TRDIER1	TRD1IC
Timer RG		TRGSR	TRGIER	TRGIC
Synchronous serial communication unit		SSSR	SSER	SSUIC
I²C bus interface		ICSR	ICIER	IICIC
Flash memory		RDYSTI	RDYSTIE	FMRDYIC
		BSYAEI	BSYAEIE	
			CMDERIE	

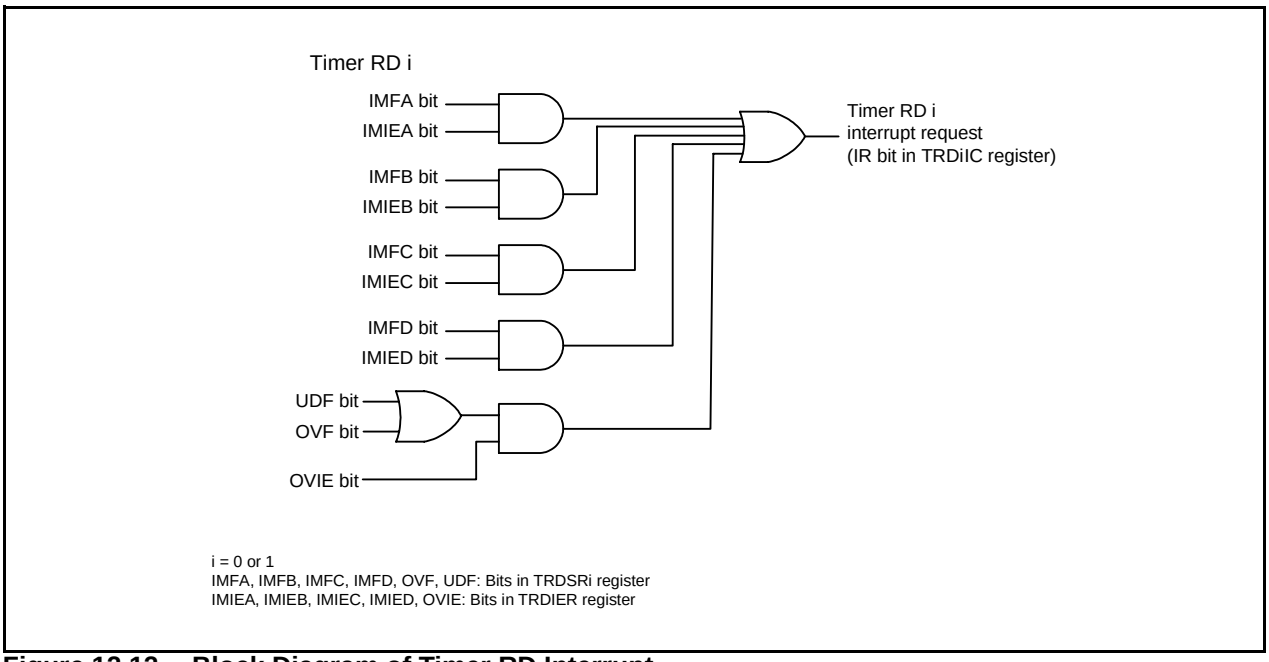


Figure 12.12 Block Diagram of Timer RD Interrupt

As with other maskable interrupts, the interrupts of timer RC, timer RD (timer RD0), timer RD (timer RD1), timer RG, the synchronous serial communication unit, the I^2C bus interface, and the flash memory are controlled by the combination of the I flag, IR bit, bits ILVL0 to ILVL2, and IPL. However, since each interrupt source is generated by a combination of multiple interrupt request sources, the following differences from other maskable interrupts apply:

- When bits in the enable register are set to 1 and the corresponding bits in the status register are set to 1 (interrupt enabled), the IR bit in the interrupt control register is set to 1 (interrupt requested).
- When either bits in the status register or the corresponding bits in the enable register, or both are set to 0, the IR bit is set to 0 (no interrupt requested).
  That is, even if the interrupt is not acknowledged after the IR bit is set to 1, the interrupt request will not be retained.
  Also, the IR bit is not set to 0 even if 0 is written to this bit.
- Individual bits in the status register are not automatically set to 0 even if the interrupt is acknowledged.
  The IR bit is also not automatically set to 0 when the interrupt is acknowledged.
  Set individual bits in the status register to 0 in the interrupt routine. Refer to the status register figure for how to set individual bits in the status register to 0.
- When multiple bits in the enable register are set to 1 and other request sources are generated after the IR bit is set to 1, the IR bit remains 1.
- When multiple bits in the enable register are set to 1, use the status register to determine which request source causes an interrupt.

Refer to chapters of the individual peripheral functions (**20. Timer RC**, **21. Timer RD**, **23. Timer RG**, **27. Synchronous Serial Communication Unit (SSU), 28. I^2C bus Interface,** and **35. Flash Memory**) for the status register and enable register.
For the interrupt control register, refer to **12.3 Interrupt Control**.

12.8 Notes on Interrupts

12.8.1 Reading Address 00000h

Do not read address 00000h by a program. When a maskable interrupt request is acknowledged, the CPU reads interrupt information (interrupt number and interrupt request level) from 00000h in the interrupt sequence. At this time, the IR bit for the acknowledged interrupt is set to 0.
If address 00000h is read by a program, the IR bit for the interrupt which has the highest priority among the enabled interrupts is set to 0. This may cause the interrupt to be canceled, or an unexpected interrupt to be generated.

12.8.2 SP Setting

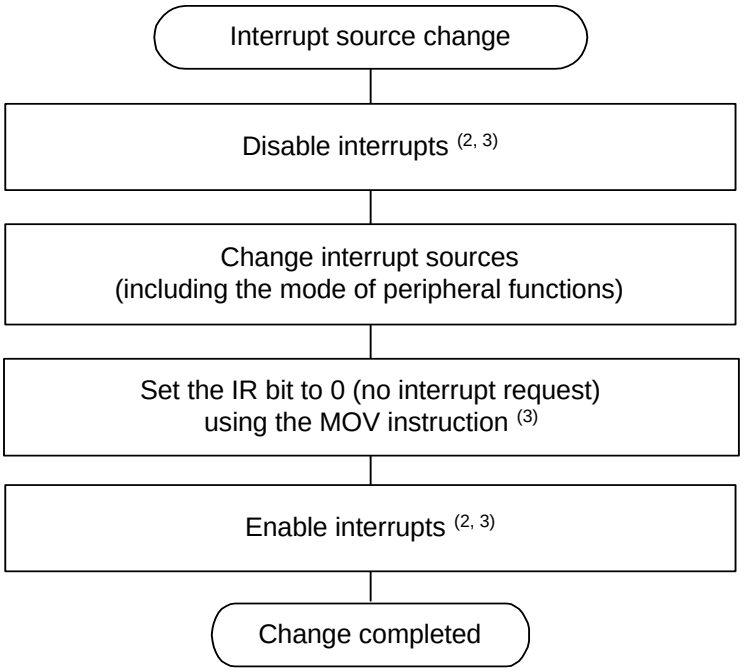
Set a value in the SP before an interrupt is acknowledged. The SP is set to 0000h after a reset. If an interrupt is acknowledged before setting a value in the SP, the program may run out of control.

12.8.3 External Interrupt, Key Input Interrupt

Either the low-level width or high-level width shown in the Electrical Characteristics is required for the signal input to pins $\overline{\text{INT0}}$ to $\overline{\text{INT7}}$ and pins $\overline{\text{KI0}}$ to $\overline{\text{KI7}}$, regardless of the CPU clock.
For details, refer to **Table 36.XX** (VCC = 5 V), **Table 36.XX** (VCC = 3 V), **Table 36.XX** (VCC = 1.8 V) **External Interrupt INTi (i = 0 to 7) Input**, **Key Input Interrupt KIi (i = 0 to 7)**.

12.8.4 Changing Interrupt Sources

The IR bit in the interrupt control register may be set to 1 (interrupt requested) when the interrupt source changes. To use an interrupt, set the IR bit to 0 (no interrupt requested) after changing interrupt sources.
Changing interrupt sources as referred to here includes all factors that change the source, polarity, or timing of the interrupt assigned to a software interrupt number. Therefore, if a mode change of a peripheral function involves the source, polarity, or timing of an interrupt, set the IR bit to 0 (no interrupt requested) after making these changes. Refer to the descriptions of the individual peripheral functions for related interrupts.
Figure 12.13 shows a Procedure Example for Changing Interrupt Sources.



IR bit: Bit in the interrupt control register bit for the interrupt whose source is to be changed

Notes:
1. The above settings must be executed individually. Do not execute two or more settings simultaneously (using one instruction).
2. To prevent interrupt requests from being generated, disable the peripheral function before changing the interrupt source. In this case, use the I flag if all maskable interrupts can be disabled.
   If all maskable interrupts cannot be disabled, use bits ILVL0 to ILVL2 for the interrupt whose source is to be changed.
3. Refer to **12.8.5 Rewriting Interrupt Control Register** for the instructions to use and related notes.

Figure 12.13 Procedure Example for Changing Interrupt Sources

12.8.5 Rewriting Interrupt Control Register

(a) The contents of the interrupt control register can be rewritten only while no interrupt requests corresponding to that register are generated. If an interrupt request may be generated, disable the interrupt before rewriting the contents of the interrupt control register.

(b) When rewriting the contents of the interrupt control register after disabling the interrupt, be careful to choose appropriate instructions.
Changing any bit other than the IR bit
If an interrupt request corresponding to the register is generated while executing the instruction, the IR bit may not be set to 1 (interrupt requested), and the interrupt may be ignored. If this causes a problem, use one of the following instructions to rewrite the contents of the register:
AND, OR, BCLR, and BSET.

Changing the IR bit
Depending on the instruction used, the IR bit may not be set to 0 (no interrupt requested).
Use the MOV instruction to set the IR bit to 0.

(c) When using the I flag to disable an interrupt, set the I flag as shown in the sample programs below.
Refer to (b) regarding rewriting the contents of interrupt control registers using the sample programs.

Examples 1 to 3 shows how to prevent the I flag from being set to 1 (interrupts enabled) before the contents of the interrupt control register are rewritten for the effects of the internal bus and the instruction queue buffer.

Example 1: Use the NOP instructions to pause program until the interrupt control register is rewritten

```
INT_SWITCH1:
    FCLR    I               ; Disable interrupts
    AND.B   #00H,0056H      ; Set the TRAIC register to 00h
    NOP                     ;
    NOP
    FSET    I               ; Enable interrupts
```

Example 2: Use a dummy read to delay the FSET instruction

```
INT_SWITCH2:
    FCLR    I               ; Disable interrupts
    AND.B   #00H,0056H      ; Set the TRAIC register to 00h
    MOV.W   MEM,R0          ; Dummy read
    FSET    I               ; Enable interrupts
```

Example 3: Use the POPC instruction to change the I flag

```
INT_SWITCH3:
    PUSHC   FLG
    FCLR    I               ; Disable interrupts
    AND.B   #00H,0056H      ; Set the TRAIC register to 00h
    POPC    FLG             ; Enable interrupts
```

13. ID Code Areas

The ID code areas are used to implement a function that prevents the flash memory from being rewritten in standard serial I/O mode. This function prevents the flash memory from being read, rewritten, or erased.

13.1 Introduction

The ID code areas are assigned to 0FFDFh, 0FFE3h, 0FFEBh, 0FFEFh, 0FFF3h, 0FFF7h, and 0FFFBh of the respective vector highest-order addresses of the fixed vector table. Figure 13.1 shows the ID Code Areas.

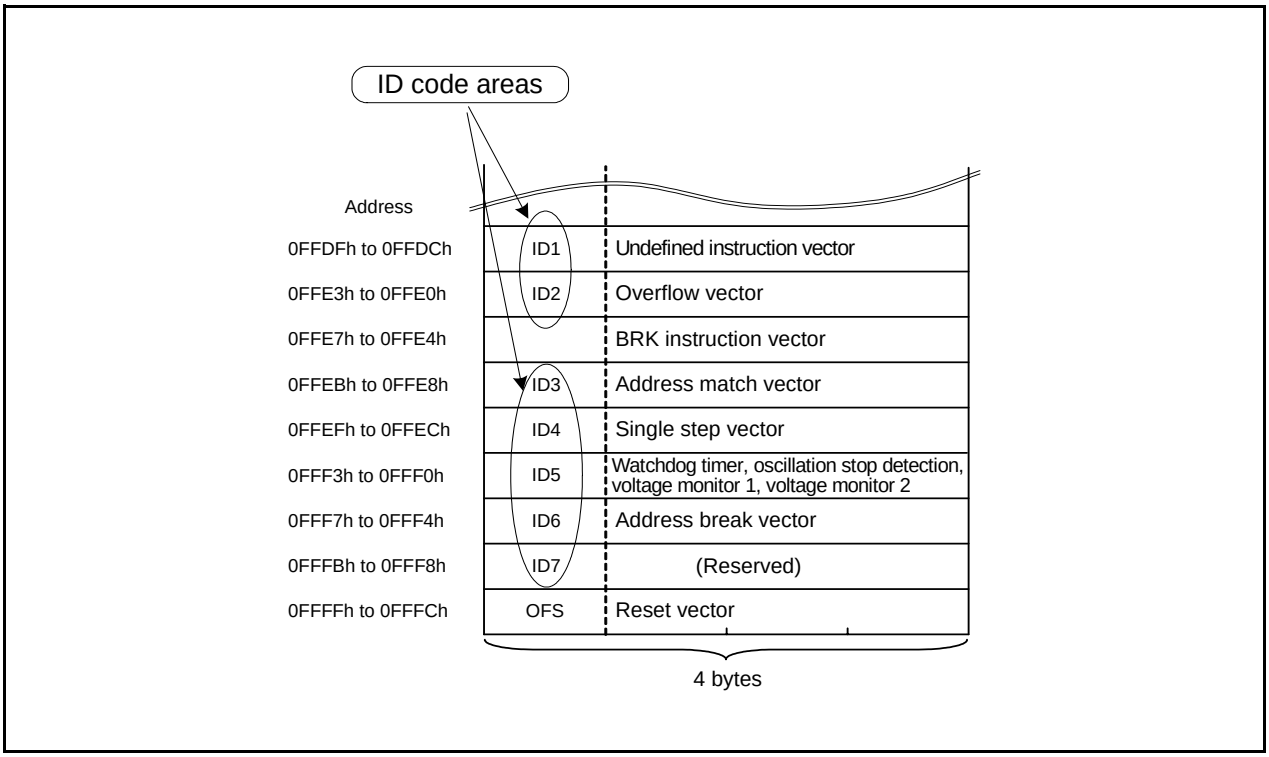


Figure 13.1 ID Code Areas

13.2 Functions

The ID code areas are used in standard serial I/O mode. Unless 3 bytes (addresses 0FFFCh to 0FFFEh) of the reset vector are set to FFFFFFh, the ID codes stored in the ID code areas and the ID codes sent from the serial programmer or the on-chip debugging emulator are checked to see if they match. If the ID codes match, the commands sent from the serial programmer or the on-chip debugging emulator are acknowledged. If the ID codes do not match, the commands are not acknowledged. To use the serial programmer or the on-chip debugging emulator, first write predetermined ID codes to the ID code areas.
If 3 bytes (addresses 0FFFCh to 0FFFEh) of the reset vector are set to FFFFFFh, the ID codes are not checked and all commands are accepted.

As the ID code areas are allocated in the flash memory (not in the SFRs), they cannot be rewritten by executing an instruction. Write appropriate values when creating a program.

The character sequence of the ASCII codes “ALeRASE” is the reserved word used for the forced erase function. The character sequence of the ASCII codes “Protect” is the reserved word used for the standard serial I/O mode disabled function. Table 13.1 shows the ID Code Reserved Word. The reserved word is a set of reserved characters when all the addresses and data in the ID code storage addresses sequentially match Table 13.1. When the forced erase function or standard serial I/O mode disabled function is not used, use another character sequence of the ASCII codes.

Table 13.1 ID Code Reserved Word

ID Code Storage Address		ID Code Reserved Word (ASCII) (1)	
		ALeRASE	Protect
0FFDFh	ID1	41h (upper-case “A”)	50h (upper-case “P”)
0FFE3h	ID2	4Ch (upper-case “L”)	72h (lower-case “r”)
0FFEBh	ID3	65h (lower-case “e”)	6Fh (lower-case “o”)
0FFEFh	ID4	52h (upper-case “R”)	74h (lower-case “t”)
0FFF3h	ID5	41h (upper-case “A”)	65h (lower-case “e”)
0FFF7h	ID6	53h (upper-case “S”)	63h (lower-case “c”)
0FFFBh	ID7	45h (upper-case “E”)	74h (lower-case “t”)

Note:
1. Reserve word:
   A set of characters when all the addresses and data in the ID code storage addresses sequentially match Table 13.1.

13.3 Forced Erase Function

This function is used in standard serial I/O mode. When the ID codes sent from the serial programmer or the on-chip debugging emulator are "ALeRASE" in ASCII code, the content of the user ROM area will be erased at once. However, if the contents of the ID code addresses are set to other than "ALeRASE" (other than **Table 13.1 ID Code Reserved Word**) when the ROMCR bit in the OFS register is set to 1 and the ROMCP1 bit is set to 0 (ROM code protect enabled), forced erasure is not executed and the ID codes are checked with the ID code check function. Table 13.2 lists the Conditions and Operations of Forced Erase Function.
When the contents of the ID code addresses are set to "ALeRASE" in ASCII code, if the ID codes sent from the serial programmer or the on-chip debugging emulator are "ALeRASE", the content of the user ROM area will be erased. If the ID codes sent from the serial programmer are other than "ALeRASE", the ID codes do not match and no command is acknowledged, thus the user ROM area remains protected.

Table 13.2 Conditions and Operations of Forced Erase Function

Condition			Operation
ID code from serial programmer or on-chip debugging emulator	ID code in ID code storage address	Bits ROMCP1 and ROMCR in OFS register	
ALeRASE	ALeRASE	–	All erasure of user ROM area (forced erase function)
	Other than ALeRASE (1)	Other than 01b (ROM code protect disabled)	
		01b (ROM code protect enabled)	ID code check (ID code check function)
Other than ALeRASE	ALeRASE	–	ID code check (ID code check function. No ID code match)
	Other than ALeRASE (1)	–	ID code check (ID code check function)

Note:
1. For "Protect", refer to **13.4 Standard Serial I/O Mode Disabled Function**.

13.4 Standard Serial I/O Mode Disabled Function

This function is used in standard serial I/O mode. When the I/D codes in the ID code storage addresses are set to the reserved character sequence of the ASCII codes "Protect" (refer to **Table 13.1 ID Code Reserved Word**), communication with the serial programmer or the on-chip debugging emulator is not performed. This does not allow the flash memory to be read, rewritten, or erased using the serial programmer or the on-chip debugging emulator.
Also, if the ID codes are also set to the reserved character sequence of the ASCII codes "Protect" when the ROMCR bit in the OFS register is set to 1 and the ROMCP1 bit is set to 0 (ROM code protect enabled), ROM code protection cannot be disabled using the serial programmer or the on-chip debugging emulator. This prevents the flash memory from being read, rewritten, or erased using the serial programmer, the on-chip debugging emulator, or the parallel programmer.

13.5 Notes on ID Code Areas

13.5.1 Setting Example of ID Code Areas

As the ID code areas are allocated in the flash memory (not in the SFRs), they cannot be rewritten by executing an instruction. Write appropriate values when creating a program. The following shows a setting example.

- To set 55h in all of the ID code areas

```
.org 00FFDCH
.lword dummy | (55000000h)    ; UND
.lword dummy | (55000000h)    ; INTO
.lword dummy ; BREAK
.lword dummy | (55000000h)    ; ADDRESS MATCH
.lword dummy | (55000000h)    ; SET SINGLE STEP
.lword dummy | (55000000h)    ; WDT
.lword dummy | (55000000h)    ; ADDRESS BREAK
.lword dummy | (55000000h)    ; RESERVE
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

14. Option Function Select Area

14.1 Introduction

The option function select area is used to select the MCU state after a reset, the function to prevent rewriting in parallel I/O mode, or the watchdog timer operation. The reset vector highest-order-addresses, 0FFFFh and 0FFDBh, are assigned as the option function select area. Figure 14.1 shows the Option Function Select Area.

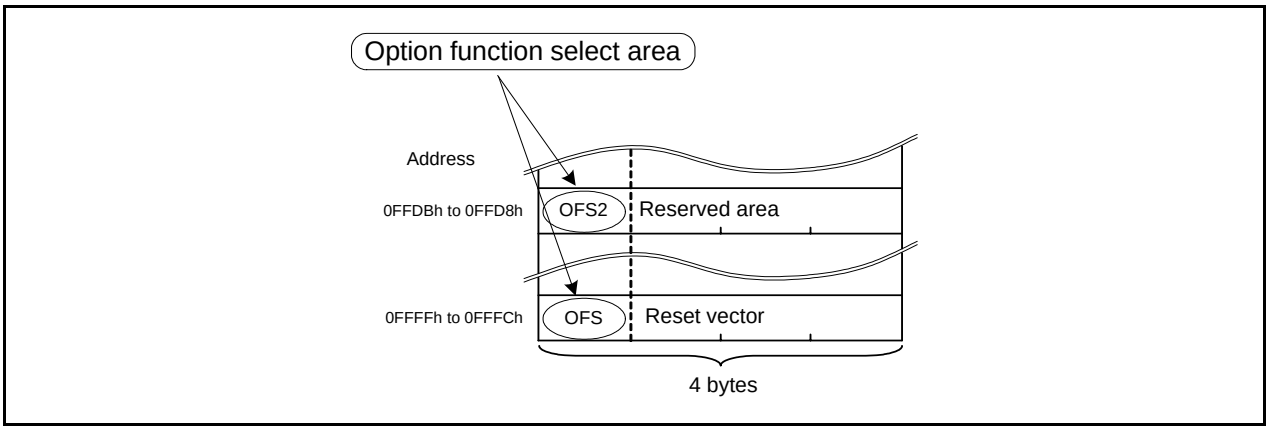


Figure 14.1 Option Function Select Area

14.2 Registers

Registers OFS and OFS2 are used to select the MCU state after a reset, the function to prevent rewriting in parallel I/O mode, or the watchdog timer operation.

14.2.1 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON	
When shipping	1	1	1	1	1	1	1	1	(Note 1)

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bit (2)	b5 b4 0 0: 3.80 V selected (Vdet0_3) 0 1: 2.85 V selected (Vdet0_2) 1 0: 2.35 V selected (Vdet0_1) 1 1: 1.90 V selected (Vdet0_0)	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protection mode enabled after reset 1: Count source protection mode disabled after reset	R/W

Notes:
1. If the block including the OFS register is erased, the OFS register value is set to FFh.
2. The same level of the voltage detection 0 level selected by bits VDSEL0 and VDESL1 is set in both functions of voltage monitor 0 reset and power-on reset.
3. To use power-on reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

The OFS register is allocated in the flash memory. Write to this register with a program.
After writing, do not write additions to this register.

LVDAS Bit (Voltage Detection 0 Circuit Start Bit)

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

14.2.2 Option Function Select Register 2 (OFS2)

Address 0FFDBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	—	—	WDTRCS1	WDTRCS0	WDTUFS1	WDTUFS0	
When shipping	1	1	1	1	1	1	1	1	(Note 1)

Bit	Symbol	Bit Name	Function	R/W
b0	WDTUFS0	Watchdog timer underflow period set bit	b1 b0 0 0: 03FFh 0 1: 0FFFh 1 0: 1FFFh 1 1: 3FFFh	R/W
b1	WDTUFS1			R/W
b2	WDTRCS0	Watchdog timer refresh acknowledgement period set bit	b3 b2 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100%	R/W
b3	WDTRCS1			R/W
b4	—	Reserved bits	Set to 1.	R/W
b5	—			
b6	—			
b7	—			

Note:
1. If the block including the OFS2 register is erased, the OFS2 register value is set to FFh.

The OFS2 register is located on the flash memory. Write to this register with a program.
After writing, do not write additions to this register.

Bits WDTRCS0 and WDTRCS1 (Watchdog Timer Refresh Acknowledgement Period Set Bit)

Assuming that the period from when the watchdog timer starts counting until it underflows is 100%, the refresh acknowledgement period for the watchdog timer can be selected.
For details, refer to **15.3.1.1 Refresh Acknowledgment Period**.

14.3 Notes on Option Function Select Area

14.3.1 Setting Example of Option Function Select Area

As the option function select area is allocated in the flash memory (not in the SFRs), they cannot be rewritten by executing an instruction. Write appropriate values when creating a program. The following shows a setting example.

- To set FFh in the OFS register

```
.org 00FFFCH
.lword reset | (0FF000000h)      ; RESET
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

15. Watchdog Timer

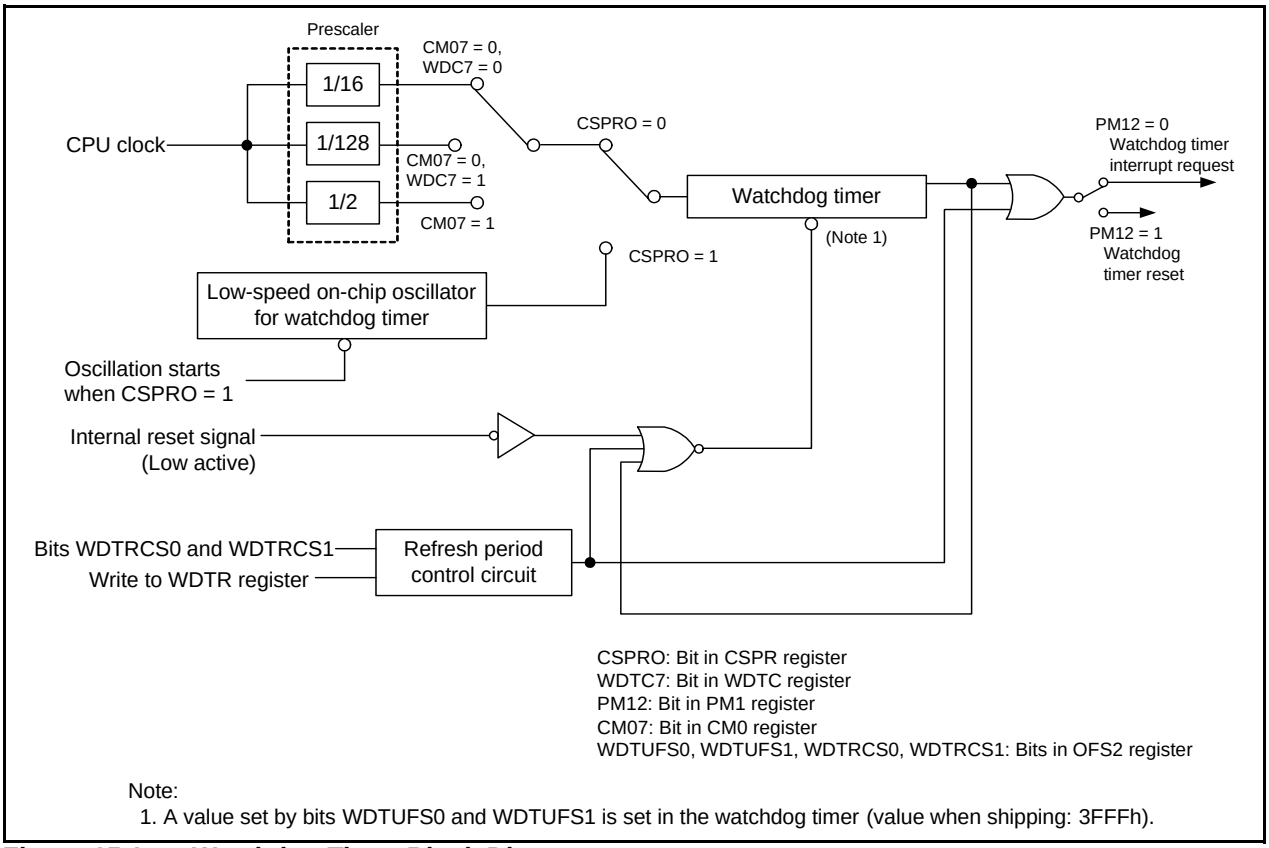
The watchdog timer is a function that detects when a program is out of control. Use of the watchdog timer is recommended to improve the reliability of the system.

15.1 Introduction

The watchdog timer contains a 14-bit counter and allows selection of count source protection mode enable or disable.
Table 15.1 lists the Watchdog Timer Specifications.
Refer to **5.5 Watchdog Timer Reset** for details of the watchdog timer reset.
Figure 15.1 shows the Watchdog Timer Block Diagram.

Table 15.1 Watchdog Timer Specifications

Item	Count Source Protection Mode Disabled	Count Source Protection Mode Enabled
Count source	CPU clock	Low-speed on-chip oscillator clock for the watchdog timer
Count operation	Decrement	
Count start condition	Either of the following can be selected: • After a reset, count starts automatically. • Count starts by writing to the WDTS register.	
Count stop condition	Stop mode, wait mode	None
Watchdog timer initialization conditions	• Reset • Write 00h and then FFh to the WDTR register (with acknowledgement period setting). • Underflow	
Operations at underflow	Watchdog timer interrupt or watchdog timer reset	Watchdog timer reset
Selectable functions	• Division ratio of the prescaler Selectable by the WDTC7 bit in the WDTC register or the CM07 bit in the CM0 register. • Count source protection mode Whether count source protection mode is enabled or disabled after a reset can be selected by the CSPROINI bit in the OFS register (flash memory). If count source protection mode is disabled after a reset, it can be enabled or disabled by the CSPRO bit in the CSPR register (program). • Start or stop of the watchdog timer after a reset Selectable by the WDTON bit in the OFS register (flash memory). • Initial value of the watchdog timer Selectable by bits WDTUFS0 and WDTUFS1 in the OFS2 register. • Refresh acknowledgement period for the watchdog timer Selectable by bits WDTRCS0 and WDTRCS1 in the OFS2 register.	



Note:
1. A value set by bits WDTUFS0 and WDTUFS1 is set in the watchdog timer (value when shipping: 3FFFh).

Figure 15.1 Watchdog Timer Block Diagram

15.2 Registers

15.2.1 Processor Mode Register 1 (PM1)

Address 0005h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	PM12	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	PM12	WDT interrupt/reset switch bit	0: Watchdog timer interrupt 1: Watchdog timer reset (1)	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—	Reserved bit	Set to 0.	R/W

Note:
1. The PM12 bit is set to 1 when 1 is written by a program (and remains unchanged even if 0 is written to it). This bit is automatically set to 1 when the CSPRO bit in the CSPR register is set to 1 (count source protection mode enabled).

Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting the PM1 register.

15.2.2 Watchdog Timer Reset Register (WDTR)

Address 000Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	R/W
b7 to b0	Writing 00h and then FFh into this register initializes the watchdog timer. The initial value of the watchdog timer is specified by bits WDTUFS0 and WDTUF1 in the OFS2 register. (1)	W

Note:
1. Write the WDTR register during the count operation of the watchdog timer.

15.2.3 Watchdog Timer Start Register (WDTS)

Address 000Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	R/W
b7 to b0	A write instruction to this register starts the watchdog timer.	W

15.2.4 Watchdog Timer Control Register (WDTC)

Address 000Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	WDTC7	—	—	—	—	—	—	—
After Reset	0	0	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	The following bits of the watchdog timer can be read. When bits WDTUFS1 to WDTUFS0 in the OFS2 register are 00b (03FFh): b5 to b0 01b (0FFFh): b8 to b3 10b (1FFFh): b9 to b4 11b (3FFFh): b10 to b5		R
b1	—			R
b2	—			R
b3	—			R
b4	—			R
b5	—			R
b6	—	Reserved bit	When read, the content is 0.	R
b7	WDTC7	Prescaler select bit	0: Divide-by-16 1: Divide-by-128	R/W

15.2.5 Count Source Protection Mode Register (CSPR)

Address 001Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	CSPRO	—	—	—	—	—	—	—	
After Reset	0	0	0	0	0	0	0	0	(Note 1)

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	CSPRO	Count source protection mode select bit (2)	0: Count source protection mode disabled 1: Count source protection mode enabled	R/W

Notes:
1. When 0 is written to the CSPROINI bit in the OFS register, the value after reset is 10000000b.
2. To set the CSPRO bit to 1, write 0 and then 1 to it. This bit cannot be set to 0 by a program.

15.2.6 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON	
When shipping	1	1	1	1	1	1	1	1	(Note 1)

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bit (2)	b5 b4 0 0: 3.80 V selected (Vdet0_3) 0 1: 2.85 V selected (Vdet0_2) 1 0: 2.35 V selected (Vdet0_1) 1 1: 1.90 V selected (Vdet0_0)	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protection mode enabled after reset 1: Count source protection mode disabled after reset	R/W

Notes:
1. If the block including the OFS register is erased, the OFS register value is set to FFh.
2. The same level of the voltage detection 0 level selected by bits VDSEL0 and VDESL1 is set in both functions of voltage monitor 0 reset and power-on reset.
3. To use power-on reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

The OFS register is allocated in the flash memory. Write to this register with a program.
After writing, do not write additions to this register.

LVDAS Bit (Voltage Detection 0 Circuit Start Bit)

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

15.2.7 Option Function Select Register 2 (OFS2)

Address 0FFDBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	—	—	WDTRCS1	WDTRCS0	WDTUFS1	WDTUFS0	
When shipping	1	1	1	1	1	1	1	1	(Note 1)

Bit	Symbol	Bit Name	Function	R/W
b0	WDTUFS0	Watchdog timer underflow period set bit	b1 b0 0 0: 03FFh 0 1: 0FFFh 1 0: 1FFFh 1 1: 3FFFh	R/W
b1	WDTUFS1			R/W
b2	WDTRCS0	Watchdog timer refresh acknowledgement period set bit	b3 b2 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100%	R/W
b3	WDTRCS1			R/W
b4	—	Reserved bits	Set to 1.	R/W
b5	—			
b6	—			
b7	—			

Note:
1. If the block including the OFS2 register is erased, the OFS2 register value is set to FFh.

The OFS2 register is located on the flash memory. Write to this register with a program.
After writing, do not write additions to this register.

Bits WDTRCS0 and WDTRCS1 (Watchdog Timer Refresh Acknowledgement Period Set Bit)

Assuming that the period from when the watchdog timer starts counting until it underflows is 100%, the refresh acknowledgement period for the watchdog timer can be selected.
For details, refer to **15.3.1.1 Refresh Acknowledgment Period**.

15.3 Functional Description

15.3.1 Common Items for Multiple Modes

15.3.1.1 Refresh Acknowledgment Period

The period for acknowledging refreshment operation to the watchdog timer (write to the WDTR register) can be selected by bits WDTRCS0 and WDTRCS1 in the OFS2 register. Figure 15.2 shows the Refresh Acknowledgement Period for Watchdog Timer.

Assuming that the period from when the watchdog timer starts counting until it underflows is 100%, a refresh operation executed during the refresh acknowledgement period is acknowledged. Any refresh operation executed during the period other than the above is processed as an incorrect write, and a watchdog timer interrupt or watchdog timer reset (selectable by the PM12 bit in the PM1 register) is generated.

Do not execute any refresh operation while the count operation of the watchdog timer is stopped.

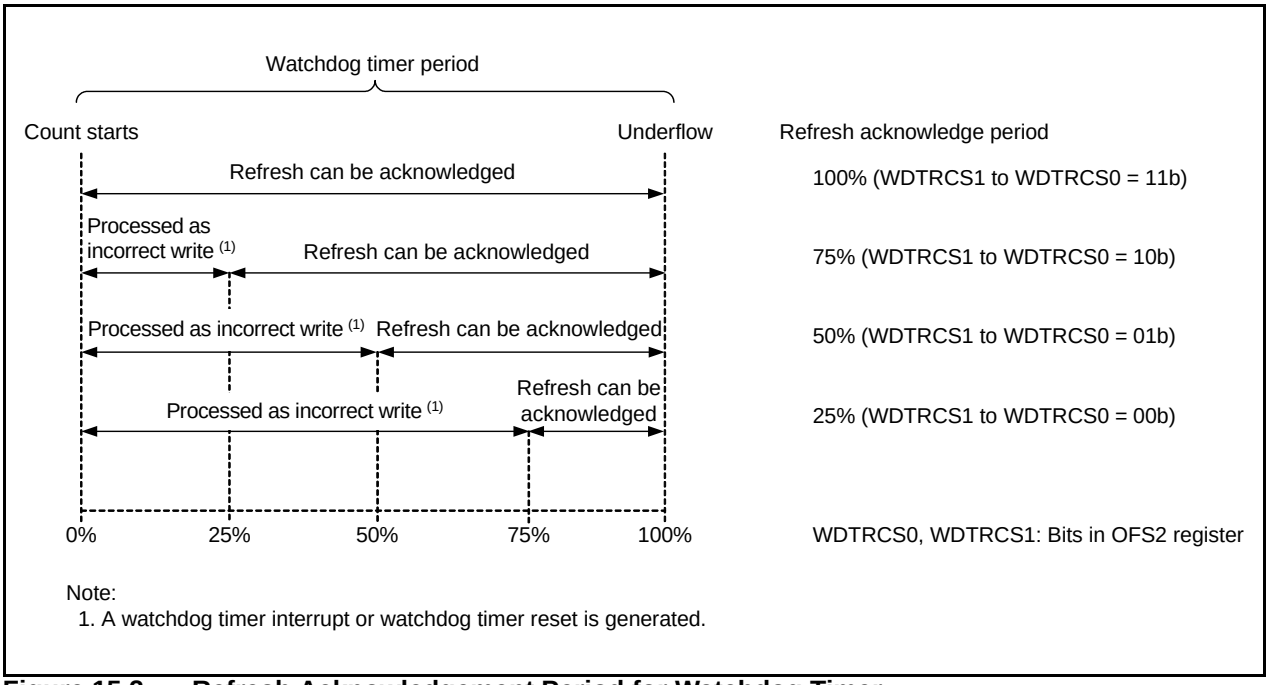


Figure 15.2 Refresh Acknowledgement Period for Watchdog Timer

15.3.2 Count Source Protection Mode Disabled

The count source for the watchdog timer is the CPU clock when count source protection mode is disabled. Table 15.2 lists the Watchdog Timer Specifications (Count Source Protection Mode Disabled).

Table 15.2 Watchdog Timer Specifications (Count Source Protection Mode Disabled)

Item	Specification
Count source	CPU clock
Count operation	Decrement
Period	$\frac{\text{Division ratio of prescaler (n)} \times \text{count value of watchdog timer (m)}}{\text{CPU clock}}$ (1) n: 16 or 128 (selected by the WDTC7 bit in the WDTC register), or 2 when the low-speed clock is selected (CM07 bit in CM0 register = 1) m: Value set by bits WDTUFS0 and WDTUFS1 in the OFS2 register Example: The period is approximately 13.1 ms when: - The CPU clock frequency is set to 20 MHz. - The prescaler is divided by 16. - Bits WDTUFS1 to WDTUFS0 are set to 11b (3FFFh).
Watchdog timer initialization conditions	• Reset • Write 00h and then FFh to the WDTR register. (3) • Underflow
Count start conditions	The operation of the watchdog timer after a reset is selected by the WDTON bit (2) in the OFS register (address 0FFFFh). • When the WDTON bit is set to 1 (watchdog timer is stopped after reset). The watchdog timer and prescaler are stopped after a reset and start counting when the WDTS register is written to. • When the WDTON bit is set to 0 (watchdog timer starts automatically after reset). The watchdog timer and prescaler start counting automatically after a reset.
Count stop condition	Stop mode, wait mode (Count resumes from the retained value after exiting.)
Operations at underflow	• When the PM12 bit in the PM1 register is set to 0. Watchdog timer interrupt • When the PM12 bit in the PM1 register is set to 1. Watchdog timer reset (refer to **5.5 Watchdog Timer Reset**)

Notes:
1. The watchdog timer is initialized when 00h and then FFh is written to the WDTR register. The prescaler is initialized after a reset. This may cause some errors due to the prescaler during the watchdog timer period.
2. The WDTON bit cannot be changed by a program. To set this bit, write 0 to bit 0 of address 0FFFFh with a flash programmer.
3. Write the WDTR register during the count operation of the watchdog timer.

15.3.3 Count Source Protection Mode Enabled

The count source for the watchdog timer is the low-speed on-chip oscillator clock for the watchdog timer when count source protection mode is enabled. If the CPU clock stops when a program is out of control, the clock can still be supplied to the watchdog timer.
Table 15.3 lists the Watchdog Timer Specifications (Count Source Protection Mode Enabled).

Table 15.3 Watchdog Timer Specifications (Count Source Protection Mode Enabled)

Item	Specification
Count source	Low-speed on-chip oscillator clock
Count operation	Decrement
Period	$\frac{\text{Count value of watchdog timer (m)}}{\text{Low-speed on-chip oscillator clock for the watchdog timer}}$ m: Value set by bits WDTUFS0 and WDTUFS1 in the OFS2 register Example: The period is approximately 8.2 ms when: - The on-chip oscillator clock for the watchdog timer is set to 125 kHz. - Bits WDTUFS1 to WDTUFS0 are set to 00b (03FFh).
Watchdog timer initialization conditions	• Reset • Write 00h and then FFh to the WDTR register. (3) • Underflow
Count start conditions	The operation of the watchdog timer after a reset is selected by the WDTON bit (1) in the OFS register (address 0FFFFh). • When the WDTON bit is set to 1 (watchdog timer is stopped after reset). The watchdog timer and prescaler are stopped after a reset and start counting when the WDTS register is written to. • When the WDTON bit is set to 0 (watchdog timer starts automatically after reset). The watchdog timer and prescaler start counting automatically after a reset.
Count stop condition	None (Count does not stop even in wait mode once it starts. The MCU does not enter stop mode.)
Operation at underflow	Watchdog timer reset (Refer to **5.5 Watchdog Timer Reset.**)
Registers, bits	• When the CSPPRO bit in the CSPR register is set to 1 (count source protection mode enabled) (2), the following are set automatically: - The low-speed on-chip oscillator for the watchdog timer is on. - The PM12 bit in the PM1 register is set to 1 (watchdog timer reset when the watchdog timer underflows).

Notes:
1. The WDTON bit cannot be changed by a program. To set this bit, write 0 to bit 0 of address 0FFFFh with a flash programmer.
2. Even if 0 is written to the CSPROINI bit in the OFS register, the CSPRO bit is set to 1. The CSPROINI bit cannot be changed by a program. To set this bit, write 0 to bit 7 of address 0FFFFh with a flash programmer.
3. Write the WDTR register during the count operation of the watchdog timer.

16. DTC

The DTC (data transfer controller) is a function that transfers data between the SFR and on-chip memory without using the CPU. This chip incorporates one DTC channel. The DTC is activated by a peripheral function interrupt to perform data transfers. The DTC and CPU use the same bus, and the DTC takes priority over the CPU in using the bus.
To control DTC data transfers, control data comprised of a transfer source address, a transfer destination address, and operating modes are allocated in the DTC control data area. Each time the DTC is activated, the DTC reads control data to perform data transfers.

16.1 Overview

Table 16.1 lists the DTC Specifications and Figure 16.1 shows DTC Block Diagram.

Table 16.1 DTC Specifications

Item		Specification
Activation sources		38 sources
Allocatable control data		24 sets
Address space which can be transferred		64 Kbytes (00000h to 0FFFFh)
Maximum number of transfer times	Normal mode	256 times
	Repeat mode	255 times
Maximum size of block to be transferred	Normal mode	256 bytes
	Repeat mode	255 bytes
Unit of transfers		Byte
Transfer mode	Normal mode	Transfers end on completion of the transfer causing the DTCCTj register value to change from 1 to 0.
	Repeat mode	On completion of the transfer causing the DTCCTj register value to change from 1 to 0, the repeat area address is initialized and the DTRLDj register value is reloaded to the DTCCTj register to continue transfers.
Address control	Normal mode	Fixed or incremented
	Repeat mode	Addresses of the area not selected as the repeat area are fixed or incremented.
Priority of activation sources		See **Table 16.5 DTC Activation Sources and DTC Vector Addresses**.
Interrupt request	Normal mode	When the data transfer causing the DTCCTj register value to change from 1 to 0 is performed, the activation source interrupt request is generated for the CPU, and interrupt handling is performed on completion of the data transfer.
	Repeat mode	When the data transfer causing the DTCCTj register value to change from 1 to 0 is performed while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled), the activation source interrupt request is generated for the CPU, and interrupt handling is performed on completion of the transfer.
Transfer start		When bits DTCENi0 to DTCENi7 in the DTCENi registers are 1 (activation enabled), data transfer is started each time the corresponding DTC activation sources are generated.
Transfer stop	Normal mode	• When bits DTCENi0 to DTCENi7 are set to 0 (activation disabled). • When the data transfer causing the DTCCTj register value to change from 1 to 0 is completed.
	Repeat mode	• When bits DTCENi0 to DTCENi7 are set to 0 (activation disabled). • When the data transfer causing the DTCCTj register value to change from 1 to 0 is completed while the RPTINT bit is 1 (interrupt generation enabled).

i = 0 to 6, j = 0 to 23

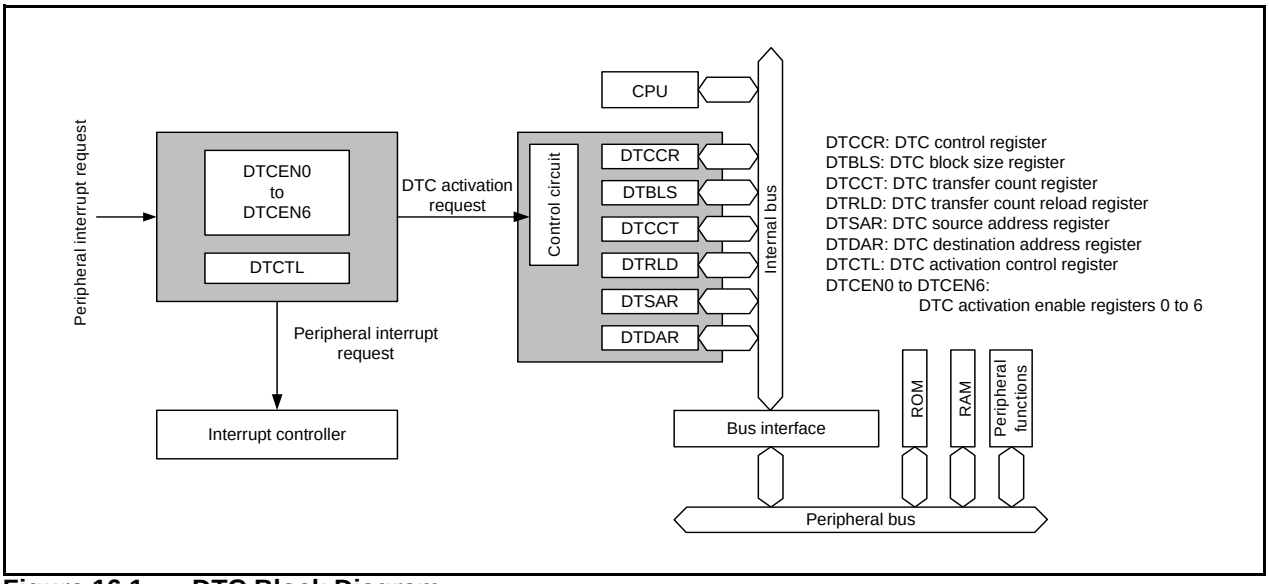


Figure 16.1 DTC Block Diagram

16.2 Registers

When the DTC is activated, control data (DTCCRj, DTBLSj, DTCCTj, DTRLDj, DTSARj, and DTDARj, j = 0 to 23) allocated in the control data area is read, and then transferred to the control registers (DTCCR, DTBLS, DTCCT, DTRLD, DTSAR, and DTDAR) in the DTC. On completion of the DTC data transfer, the contents of the DTC control registers are written back to the control data area.

Each DTCCR, DTBLS, DTCCT, DTRLD, DTSAR, and DTDAR register cannot be directly read or written to. DTCCRj, DTBLSj, DTCCTj, DTRLDj, DTSARj, and DTDARj are allocated as control data at addresses from 2C40h to 2CFFh in the DTC control data area, and can be directly accessed.
Also, registers DTCTL and DTCENi (i = 0 to 6) can be directly accessed.

16.2.1 DTC Control Register j (DTCCRj) (j = 0 to 23)

Address See **Table 16.4 Control Data Allocation Addresses**.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	RPTINT	CHNE	DAMOD	SAMOD	RPTSEL	MODE
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	MODE	Transfer mode select bit	0: Normal mode 1: Repeat mode	R/W
b1	RPTSEL	Repeat area select bit (1)	0: Transfer destination is the repeat area. 1: Transfer source is the repeat area.	R/W
b2	SAMOD	Source address control bit (2)	0: Fixed 1: Incremented	R/W
b3	DAMOD	Destination address control bit (2)	0: Fixed 1: Incremented	R/W
b4	CHNE	Chain transfer enable bit (3)	0: Chain transfers disabled 1: Chain transfers enabled	R/W
b5	RPTINT	Repeat mode interrupt enable bit (1)	0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b6	—	Reserved bits	Set to 0.	R/W
b7	—			

Notes:
1. This bit is valid when the MODE bit is 1 (repeat mode).
2. Settings of bits SAMOD and DAMOD are invalid for the repeat area.
3. Set the CHNE bit in the DTCCR23 register to 0 (chain transfers disabled).

16.2.2 DTC Block Size Register j (DTBLSj) (j = 0 to 23)

Address See **Table 16.4 Control Data Allocation Addresses**.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7 to b0	These bits specify the size of the data block to be transferred by one activation.	00h to FFh (1)	R/W

Note:
1. When the DTBLS register is set to 00h, the block size is 256 bytes.

16.2.3 DTC Transfer Count Register j (DTCCTj) (j = 0 to 23)

Address See **Table 16.4 Control Data Allocation Addresses**.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7 to b0	These bits specify the number of times of DTC data transfers.	00h to FFh (1)	R/W

Note:
1. When the DTCCT register is set to 00h, the number of transfer times is 256. Each time the DTC is activated, the DTCCT register is decremented by 1.

16.2.4 DTC Transfer Count Reload Register j (DTRLDj) (j = 0 to 23)

Address See **Table 16.4 Control Data Allocation Addresses**.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7 to b0	This register value is reloaded to the DTCCT register in repeat mode.	00h to FFh (1)	R/W

Note:
1. Set the initial value for the DTCCT register.

16.2.5 DTC Source Address Register j (DTSARj) (j = 0 to 23)

Address See **Table 16.4 Control Data Allocation Addresses**.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b15 to b0	These bits specify a transfer source address for data transfer.	0000h to FFFFh	R/W

16.2.6 DTC Destination Register j (DTDARj) (j = 0 to 23)

Address See **Table 16.4 Control Data Allocation Addresses**.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b15 to b0	These bits specify a transfer destination address for data transfer.	0000h to FFFFh	R/W

16.2.7 DTC Activation Enable Registers i (DTCENi) (i = 0 to 6)

Address 0088h (DTCEN0), 0089h (DTCEN1), 008Ah (DTCEN2), 008Bh (DTCEN3), 008Ch (DTCEN4), 008Dh (DTCEN5), 008Eh (DTCEN6)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DTCENi7	DTCENi6	DTCENi5	DTCENi4	DTCENi3	DTCENi2	DTCENi1	DTCENi0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DTCENi0	DTC activation enable bit	0: Activation disabled 1: Activation enabled	R/W
b1	DTCENi1			R/W
b2	DTCENi2			R/W
b3	DTCENi3			R/W
b4	DTCENi4			R/W
b5	DTCENi5			R/W
b6	DTCENi6			R/W
b7	DTCENi7			R/W

i = 0 to 6

The DTCENi registers enable/disable DTC activation by interrupt sources. Table 16.2 shows Correspondences between Bits DTCENi0 to DTCENi7 (i = 0 to 6) and Interrupt Sources.

Table 16.2 Correspondences between Bits DTCENi0 to DTCENi7 (i = 0 to 6) and Interrupt Sources

Register	DTCENi7 Bit	DTCENi6 Bit	DTCENi5 Bit	DTCENi4 Bit	DTCENi3 Bit	DTCENi2 Bit	DTCENi1 Bit	DTCENi0 Bit
DTCEN0	$\overline{\text{INT0}}$	$\overline{\text{INT1}}$	$\overline{\text{INT2}}$	$\overline{\text{INT3}}$	$\overline{\text{INT4}}$	$\overline{\text{INT5}}$	$\overline{\text{INT6}}$	$\overline{\text{INT7}}$
DTCEN1	Key input	A/D conversion	UART0 reception	UART0 transmission	UART1 reception	UART1 transmission	UART2 reception	UART2 transmission
DTCEN2	SSU/I²C bus receive data full	SSU/I²C bus transmit data empty	Comparator A2	Comparator A1	—	—	Timer RC input-capture/ compare-match A	Timer RC input-capture/ compare-match B
DTCEN3	Timer RC input-capture/ compare-match C	Timer RC input-capture/ compare-match D	Timer RD0 input-capture/ compare-match A	Timer RD0 input-capture/ compare-match B	Timer RD0 input-capture/ compare-match C	Timer RD0 input-capture/ compare-match D	Timer RD1 input-capture/ compare-match A	Timer RD1 input-capture/ compare-match B
DTCEN4	Timer RD1 input-capture/ compare-match C	Timer RD1 input-capture/ compare-match D	—	—	—	—	—	—
DTCEN5	—	—	Timer RE	—	—	—	—	Timer RG input-capture/ compare-match A
DTCEN6	Timer RG input-capture/ compare-match B	Timer RA	—	Timer RB	Flash memory ready status	—	—	—

16.2.8 DTC Activation Control Register (DTCTL)

Address 0080h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	NMIF	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bit	Set to 0.	R/W
b1	NMIF	Non-maskable interrupt generation bit (1)	0: Non-maskable interrupts not generated 1: Non-maskable interrupts generated	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

Note:

1. The results of writing to these bits are as follows:
   - The bit is set to 0 when it is first read as 1 and then 0 is written to it.
   - The bit remains unchanged even if it is first read as 0 and then 0 is written to it because its previous value is retained. (The bit's value remains 1 even if it is set to 1 from 0 after being read as 0 and having 0 written to it because its previous value is retained.)
   - The bit's value remains unchanged if 1 is written to it.

The DTCTL register controls DTC activation when a non-maskable interrupt (an interrupt by the watchdog timer, oscillation stop detection, voltage monitor 1, or voltage monitor 2) is generated.

NMIF Bit (Non-Maskable Interrupt Generation Bit)

The NMIF bit is set to 1 when a watchdog timer interrupt, an oscillation stop detection interrupt, a voltage monitor 1 interrupt, or a voltage monitor 2 interrupt is generated.
When the NMIF bit is 1, the DTC is not activated even if the interrupt which enables DTC activation is generated. If the NMIF bit is changed to 1 during DTC transfer, the transfer is continued until it is completed.

16.3 Function Description

16.3.1 Overview

When the DTC is activated, control data is read from the DTC control data area to perform data transfers and control data after data transfer is written back to the DTC control data area. 24 sets of control data can be stored in the DTC control data area, which allows 24 types of data transfers to be performed.
There are two transfer modes: normal mode and repeat mode. When the CHNE bit in the DTCCRj (j = 0 to 23) register is set to 1 (chain transfers enabled), multiple control data is read and data transfers are continuously performed by one activation source (chain transfers).
A transfer source address is specified by the 16-bit register DTSARj, and a transfer destination address is specified by the 16-bit register DTDARj. The values in the registers DTSARj and DTDARj are separately fixed or incremented according to the control data on completion of the data transfer.

16.3.2 Activation Sources

The DTC is activated by an interrupt source. Figure 16.2 is a Block Diagram Showing Control of DTC Activation Sources.
The interrupt sources to activate the DTC are selected with the DTCENi (i = 0 to 6) register.
The DTC sets 0 (activation disabled) to the corresponding bit among bits DTCENi0 to DTCENi7 in the DTCENi register during operation when the setting of data transfer (the first transfer in chain transfers) is either of the following:

- Transfer causing the DTCCTj (j = 0 to 23) register value to change to 0 in normal mode
- Transfer causing the DTCCTj register value to change to 0 while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled) in repeat mode

If the data transfer setting is not either of the above and the activation source is an interrupt source for timer RC, timer RD, or the flash memory, the DTC sets 0 to the interrupt source flag corresponding to the activation source during operation.
Table 16.3 shows the DTC Activation Sources and Interrupt Source Flags for Setting to 0 during DTC Operation.
If multiple activation sources are simultaneously generated, DTC activation will be performed according to the DTC activation source priority.
If multiple activation sources are simultaneously generated on completion of DTC operation, the next transfer will be performed according to the priority.
DTC activation is not affected by the I flag or interrupt control register, unlike with interrupt request operation. Therefore, even if interrupt requests cannot be acknowledged because interrupts are disabled, DTC activation requests can be acknowledged. The IR bit in the interrupt control register does not change even when an interrupt source to enable DTC activation is generated.

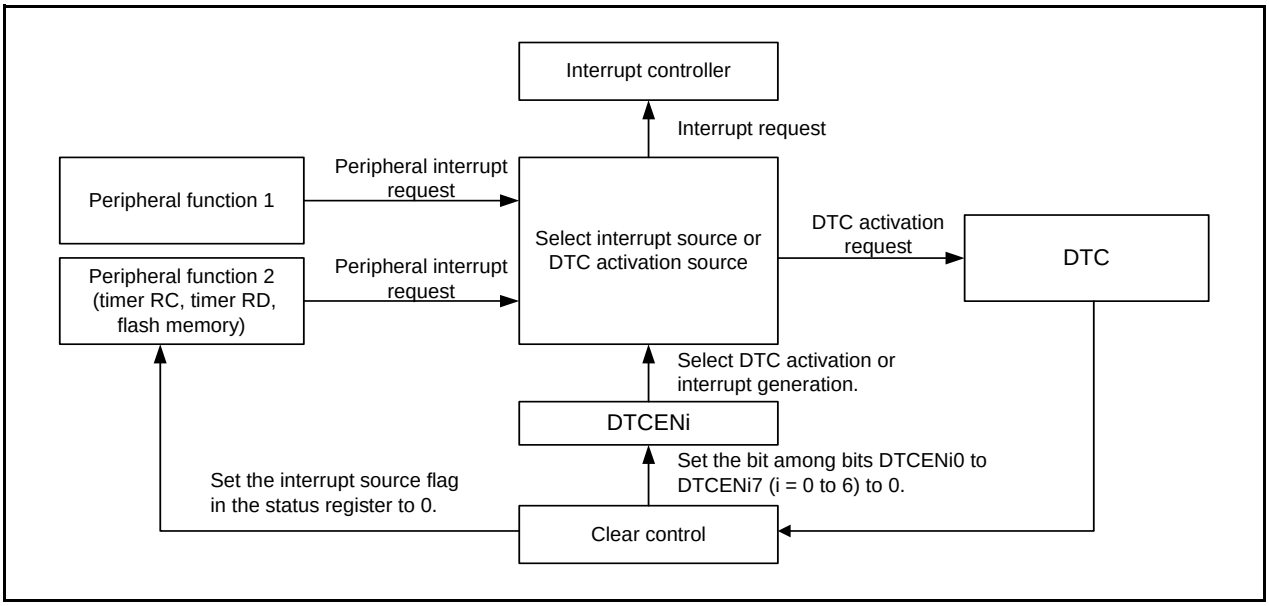


Figure 16.2 Block Diagram Showing Control of DTC Activation Sources

Table 16.3 DTC Activation Sources and Interrupt Source Flags for Setting to 0 during DTC Operation

DTC activation source generation	Interrupt Source Flag for Setting to 0
Timer RC input-capture/compare-match A	IMFA bit in TRCSR register
Timer RC input-capture/compare-match B	IMFB bit in TRCSR register
Timer RC input-capture/compare-match C	IMFC bit in TRCSR register
Timer RC input-capture/compare-match D	IMFD bit in TRCSR register
Timer RD0 input-capture/compare-match A	IMFA bit in TRDSR0 register
Timer RD0 input-capture/compare-match B	IMFB bit in TRDSR0 register
Timer RD0 input-capture/compare-match C	IMFC bit in TRDSR0 register
Timer RD0 input-capture/compare-match D	IMFD bit in TRDSR0 register
Timer RD1 input-capture/compare-match A	IMFA bit in TRDSR1 register
Timer RD1 input-capture/compare-match B	IMFB bit in TRDSR1 register
Timer RD1 input-capture/compare-match C	IMFC bit in TRDSR1 register
Timer RD1 input-capture/compare-match D	IMFD bit in TRDSR1 register
Flash memory ready status	RDYSTI bit in FST register

16.3.3 Control Data Allocation and DTC Vector Table

Control data is allocated in the following order: registers DTCCRj, DTBLSj, DTCCTj, DTRLDj, DTSARj, and DTDARj (j = 0 to 23). Table 16.4 shows the Control Data Allocation Addresses.

Table 16.4 Control Data Allocation Addresses

Register Symbol	Control Data No.	Address	DTCCRj Register	DTBLSj Register	DTCCTj Register	DTRLDj Register	DTSARj Register (Lower 8 Bits)	DTSARj Register (Higher 8 Bits)	DTDARj Register (Lower 8 Bits)	DTDARj Register (Higher 8 Bits)
DTCD0	Control Data 0	2C40h to 2C47h	2C40h	2C41h	2C42h	2C43h	2C44h	2C45h	2C46h	2C47h
DTCD1	Control Data 1	2C48h to 2C4Fh	2C48h	2C49h	2C4Ah	2C4Bh	2C4Ch	2C4Dh	2C4Eh	2C4Fh
DTCD2	Control Data 2	2C50h to 2C57h	2C50h	2C51h	2C52h	2C53h	2C54h	2C55h	2C56h	2C57h
DTCD3	Control Data 3	2C58h to 2C5Fh	2C58h	2C59h	2C5Ah	2C5Bh	2C5Ch	2C5Dh	2C5Eh	2C5Fh
DTCD4	Control Data 4	2C60h to 2C67h	2C60h	2C61h	2C62h	2C63h	2C64h	2C65h	2C66h	2C67h
DTCD5	Control Data 5	2C68h to 2C6Fh	2C68h	2C69h	2C6Ah	2C6Bh	2C6Ch	2C6Dh	2C6Eh	2C6Fh
DTCD6	Control Data 6	2C70h to 2C77h	2C70h	2C71h	2C72h	2C73h	2C74h	2C75h	2C76h	2C77h
DTCD7	Control Data 7	2C78h to 2C7Fh	2C78h	2C79h	2C7Ah	2C7Bh	2C7Ch	2C7Dh	2C7Eh	2C7Fh
DTCD8	Control Data 8	2C80h to 2C87h	2C80h	2C81h	2C82h	2C83h	2C84h	2C85h	2C86h	2C87h
DTCD9	Control Data 9	2C88h to 2C8Fh	2C88h	2C89h	2C8Ah	2C8Bh	2C8Ch	2C8Dh	2C8Eh	2C8Fh
DTCD10	Control Data 10	2C90h to 2C97h	2C90h	2C91h	2C92h	2C93h	2C94h	2C95h	2C96h	2C97h
DTCD11	Control Data 11	2C98h to 2C9Fh	2C98h	2C99h	2C9Ah	2C9Bh	2C9Ch	2C9Dh	2C9Eh	2C9Fh
DTCD12	Control Data 12	2CA0h to 2CA7h	2CA0h	2CA1h	2CA2h	2CA3h	2CA4h	2CA5h	2CA6h	2CA7h
DTCD13	Control Data 13	2CA8h to 2CAFh	2CA8h	2CA9h	2CAAh	2CABh	2CACh	2CADh	2CAEh	2CAFh
DTCD14	Control Data 14	2CB0h to 2CB7h	2CB0h	2CB1h	2CB2h	2CB3h	2CB4h	2CB5h	2CB6h	2CB7h
DTCD15	Control Data 15	2CB8h to 2CBFh	2CB8h	2CB9h	2CBAh	2CBBh	2CBCh	2CBDh	2CBEh	2CBFh
DTCD16	Control Data 16	2CC0h to 2CC7h	2CC0h	2CC1h	2CC2h	2CC3h	2CC4h	2CC5h	2CC6h	2CC7h
DTCD17	Control Data 17	2CC8h to 2CCFh	2CC8h	2CC9h	2CCAh	2CCBh	2CCCh	2CCDh	2CCEh	2CCFh
DTCD18	Control Data 18	2CD0h to 2CD7h	2CD0h	2CD1h	2CD2h	2CD3h	2CD4h	2CD5h	2CD6h	2CD7h
DTCD19	Control Data 19	2CD8h to 2CDFh	2CD8h	2CD9h	2CDAh	2CDBh	2CDCh	2CDDh	2CDEh	2CDFh
DTCD20	Control Data 20	2CE0h to 2CE7h	2CE0h	2CE1h	2CE2h	2CE3h	2CE4h	2CE5h	2CE6h	2CE7h
DTCD21	Control Data 21	2CE8h to 2CEFh	2CE8h	2CE9h	2CEAh	2CEBh	2CECh	2CEDh	2CEEh	2CEFh
DTCD22	Control Data 22	2CF0h to 2CF7h	2CF0h	2CF1h	2CF2h	2CF3h	2CF4h	2CF5h	2CF6h	2CF7h
DTCD23	Control Data 23	2CF8h to 2CFFh	2CF8h	2CF9h	2CFAh	2CFBh	2CFCh	2CFDh	2CFEh	2CFFh

j = 0 to 23

When the DTC is activated, one control data is selected according to the data read from the vector table which has been assigned to each activation source, and the selected control data is read from the DTC control data area.
Table 16.5 shows the DTC Activation Sources and DTC Vector Addresses. A one-byte vector table area is assigned to each activation source and one value from 00000000b to 00010111b (control data numbers in Table 16.4) is stored in each area to select one of the 24 control data sets.
Figures 16.3 to 16.6 show the DTC Internal Operation Flowchart.

Table 16.5 DTC Activation Sources and DTC Vector Addresses

Interrupt Request Source	Interrupt Name	Source No.	DTC Vector Address	Priority
External input	$\overline{\text{INT0}}$	0	2C00h	High
	$\overline{\text{INT1}}$	1	2C01h	
	$\overline{\text{INT2}}$	2	2C02h	
	$\overline{\text{INT3}}$	3	2C03h	
	$\overline{\text{INT4}}$	4	2C04h	
	$\overline{\text{INT5}}$	5	2C05h	
	$\overline{\text{INT6}}$	6	2C06h	
	$\overline{\text{INT7}}$	7	2C07h	
Key input	Key input	8	2C08h	
A/D	A/D conversion	9	2C09h	
UART0	UART0 reception	10	2C0Ah	
	UART0 transmission	11	2C0Bh	
UART1	UART1 reception	12	2C0Ch	
	UART1 transmission	13	2C0Dh	
UART2	UART2 reception	14	2C0Eh	
	UART2 transmission	15	2C0Fh	
SSU/I^2C bus	Receive data full	16	2C10h	
	Transmit data empty	17	2C11h	
Voltage detection circuit	Comparator A2	18	2C12h	
	Comparator A1	19	2C13h	
Timer RC	Input-capture/compare-match A	22	2C16h	
	Input-capture/compare-match B	23	2C17h	
	Input-capture/compare-match C	24	2C18h	
	Input-capture/compare-match D	25	2C19h	
Timer RD0	Input-capture/compare-match A	26	2C1Ah	
	Input-capture/compare-match B	27	2C1Bh	
	Input-capture/compare-match C	28	2C1Ch	
	Input-capture/compare-match D	29	2C1Dh	
Timer RD1	Input-capture/compare-match A	30	2C1Eh	
	Input-capture/compare-match B	31	2C1Fh	
	Input-capture/compare-match C	32	2C20h	
	Input-capture/compare-match D	33	2C21h	
Timer RE	Timer RE	42	2C2Ah	
Timer RG	Input-capture/compare-match A	47	2C2Fh	
	Input-capture/compare-match B	48	2C30h	
Timer RA	Timer RA	49	2C31h	
Timer RB	Timer RB	51	2C33h	
Flash memory	Flash memory ready status	52	2C34h	Low

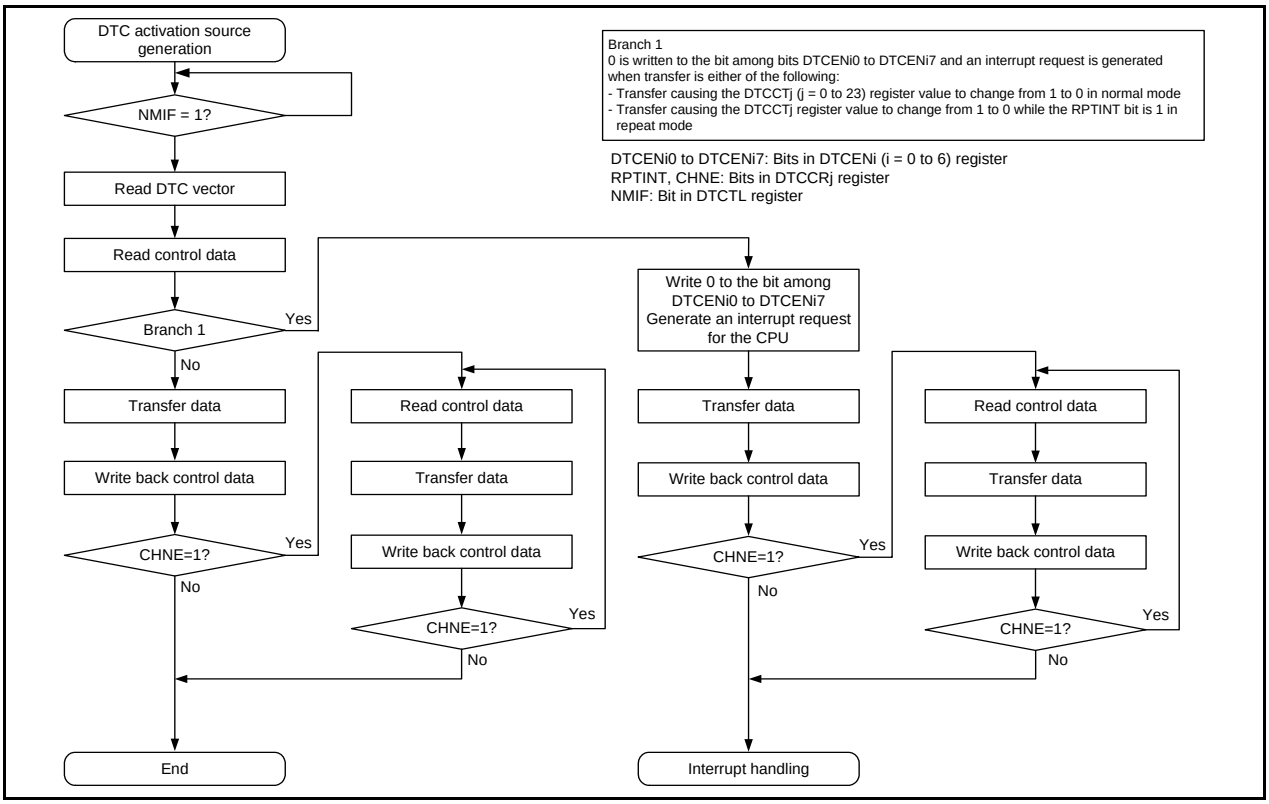


Figure 16.3 DTC Internal Operation Flowchart When DTC Activation Source is not SSU/I²C bus, Timer RC, Timer RD, or Flash Memory Interrupt Source

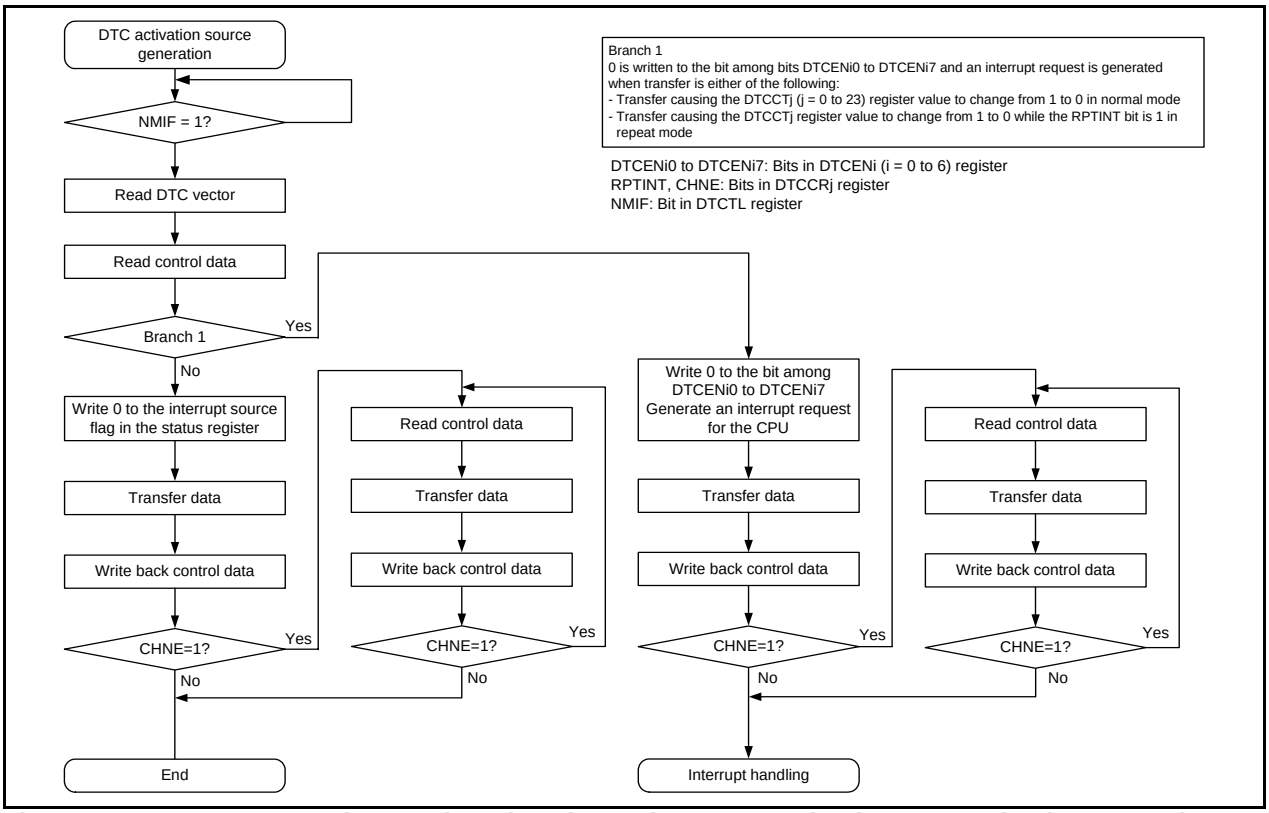
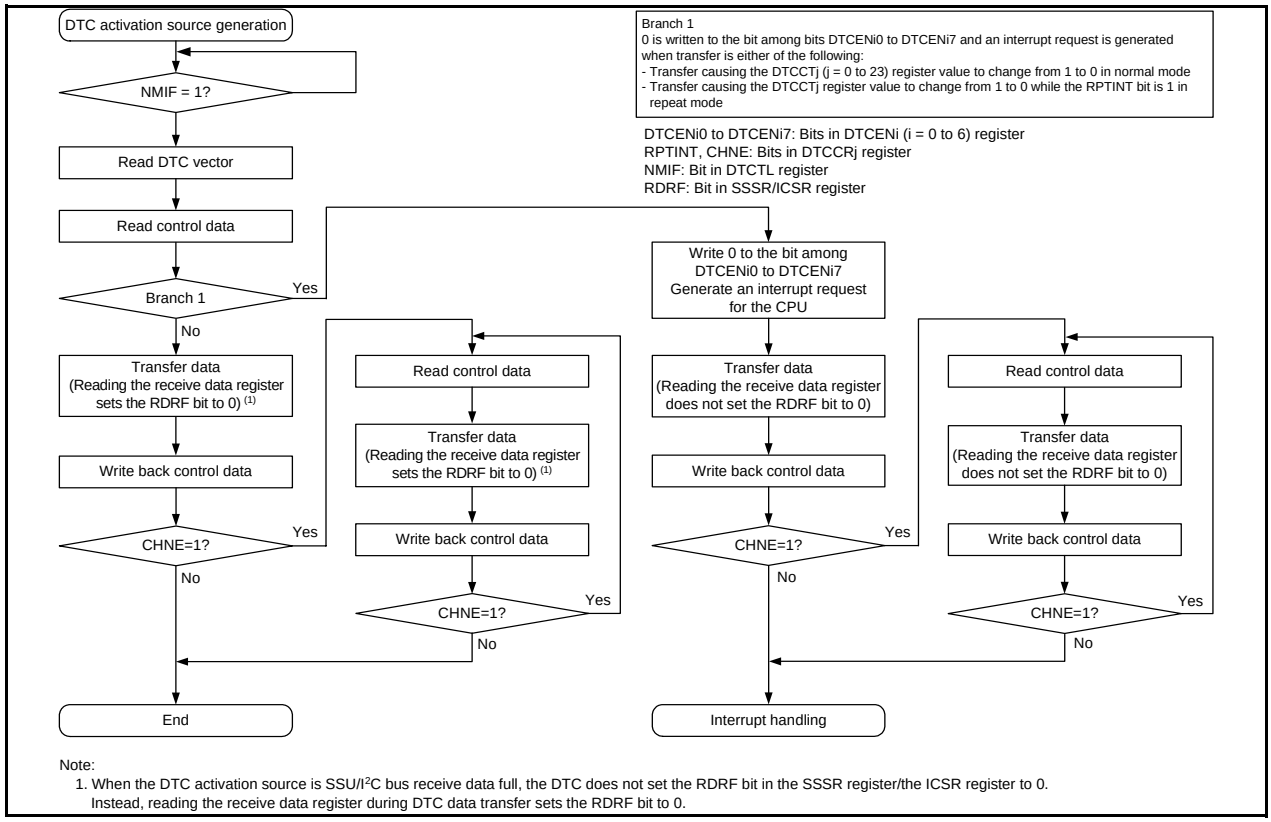
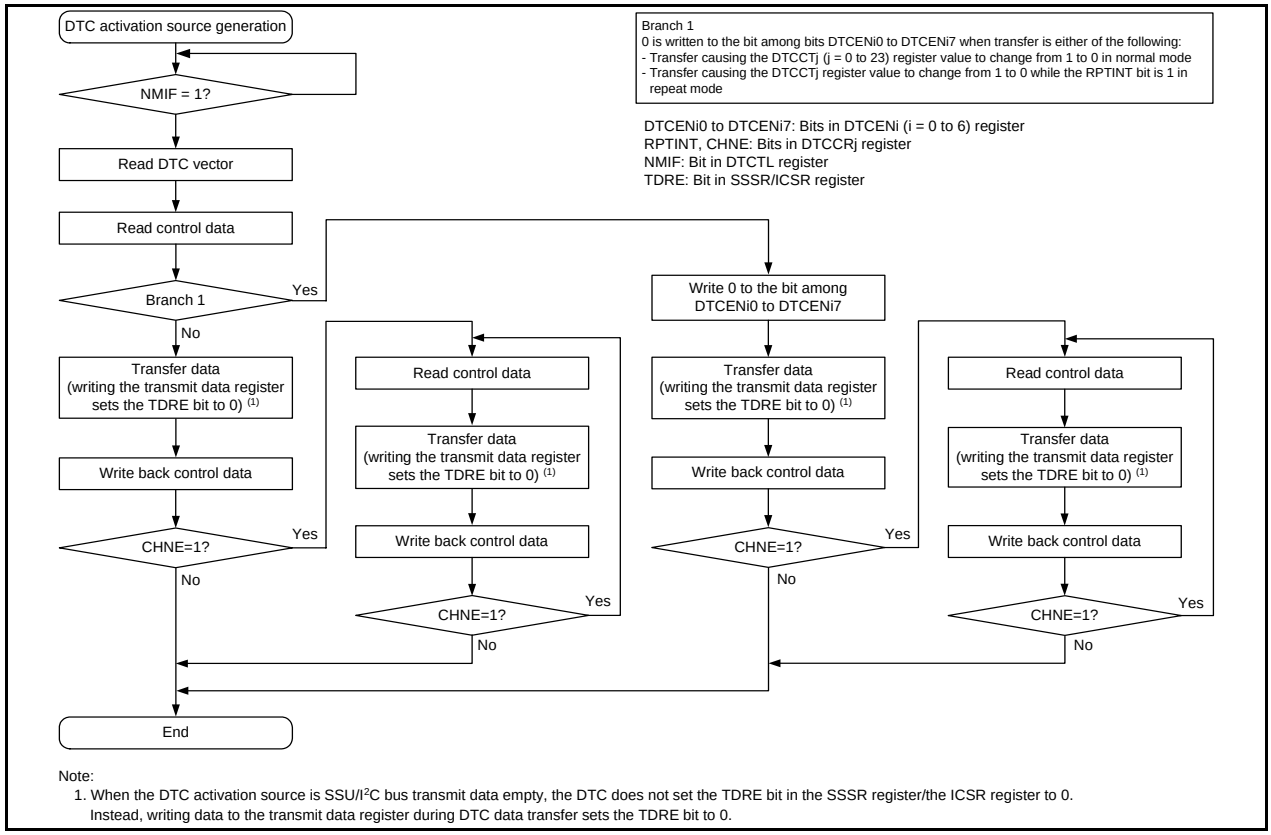


Figure 16.4 DTC Internal Operation Flowchart When DTC Activation Source is Timer RC, Timer RD, or Flash Memory Interrupt Source



Note:
1. When the DTC activation source is SSU/I²C bus receive data full, the DTC does not set the RDRF bit in the SSSR register/the ICSR register to 0. Instead, reading the receive data register during DTC data transfer sets the RDRF bit to 0.

Figure 16.5 DTC Internal Operation Flowchart When DTC Activation Source is SSU/I²C bus Receive Data Full



Note:
1. When the DTC activation source is SSU/I²C bus transmit data empty, the DTC does not set the TDRE bit in the SSSR register/the ICSR register to 0. Instead, writing data to the transmit data register during DTC data transfer sets the TDRE bit to 0.

Figure 16.6 DTC Internal Operation Flowchart When DTC Activation Source is SSU/I²C bus Transmit Data Empty

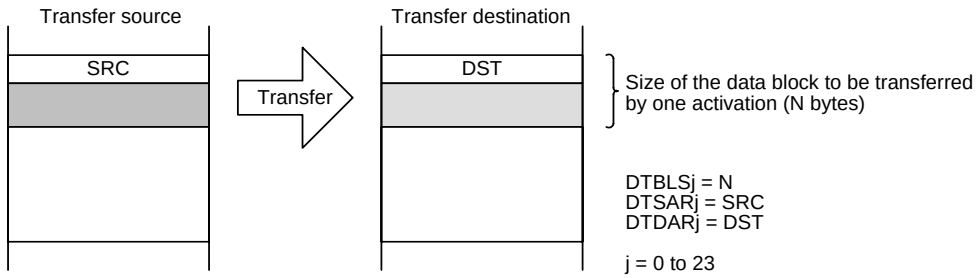
16.3.4 Normal Mode

One to 256 bytes of data are transferred by one activation. The number of transfer times can be 1 to 256. When the data transfer causing the DTCCTj (j = 0 to 23) register value to change to 0 is performed, an interrupt request for the CPU is generated during DTC operation.
Table 16.6 shows Register Functions in Normal Mode.
Figure 16.7 shows Data Transfers in Normal Mode.

Table 16.6 Register Functions in Normal Mode

Register	Symbol	Function
DTC block size register j	DTBLSj	Size of the data block to be transferred by one activation
DTC transfer count register j	DTCCTj	Number of times of data transfers
DTC transfer count reload register j	DTRLDj	Not used
DTC source address register j	DTSARj	Data transfer source address
DTC destination address register j	DTDARj	Data transfer destination address

j =0 to 23



Bits b3 to b0 in DTCCR register	Source address control	Destination address control	Source address after transfer	Destination address after transfer
00X0b	Fixed	Fixed	SRC	DST
01X0b	Incremented	Fixed	SRC+N	DST
10X0b	Fixed	Incremented	SRC	DST+N
11X0b	Incremented	Incremented	SRC+N	DST+N

X: 0 or 1

Figure 16.7 Data Transfers in Normal Mode

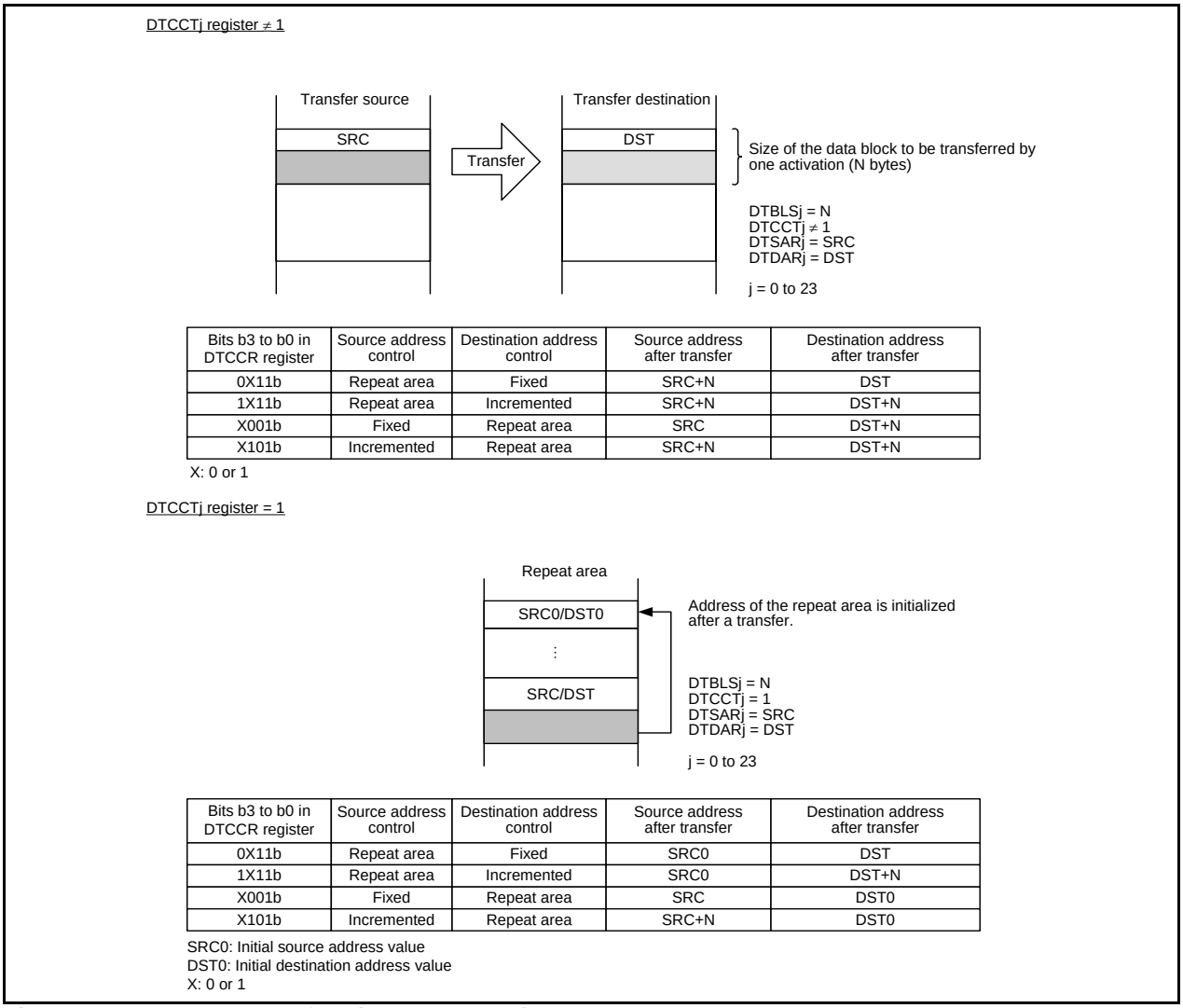
16.3.5 Repeat Mode

One to 255 bytes of data are transferred by one activation. Either of the transfer source or destination should be specified as the repeat area. The number of transfer times can be 1 to 255. On completion of the specified number of transfer times, the DTCCTj (i =0 to 23) register and the address specified for the repeat area are initialized to continue transfers. When the data transfer causing the DTCCTj register value to change to 0 is performed while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled), an interrupt request for the CPU is generated during DTC operation.
The lower 8 bits of the initial value for the repeat area address must be 00h. The size of data to be transferred must be set to 255 bytes or less before the specified number of transfer times is completed.
Table 16.7 shows Register Functions in Repeat Mode.
Figure 16.8 shows Data Transfers in Repeat Mode.

Table 16.7 Register Functions in Repeat Mode

Register	Symbol	Function
DTC block size register j	DTBLSj	Size of the data block to be transferred by one activation
DTC transfer count register j	DTCCTj	Number of times of data transfers
DTC transfer count reload register j	DTRLDj	This register value is reloaded to the DTCCT register. (Data transfer count is initialized.)
DTC source address register j	DTSARj	Data transfer source address
DTC destination address register j	DTDARj	Data transfer destination address

j =0 to 23



Bits b3 to b0 in DTCCR register	Source address control	Destination address control	Source address after transfer	Destination address after transfer
0X11b	Repeat area	Fixed	SRC+N	DST
1X11b	Repeat area	Incremented	SRC+N	DST+N
X001b	Fixed	Repeat area	SRC	DST+N
X101b	Incremented	Repeat area	SRC+N	DST+N

X: 0 or 1

Bits b3 to b0 in DTCCR register	Source address control	Destination address control	Source address after transfer	Destination address after transfer
0X11b	Repeat area	Fixed	SRC0	DST
1X11b	Repeat area	Incremented	SRC0	DST+N
X001b	Fixed	Repeat area	SRC	DST0
X101b	Incremented	Repeat area	SRC+N	DST0

SRC0: Initial source address value
DST0: Initial destination address value
X: 0 or 1

Figure 16.8 Data Transfers in Repeat Mode

16.3.6 Chain Transfers

When the CHNE bit in the DTCCRj (j = 0 to 22) register is 1 (chain transfers enabled), multiple data transfers can be continuously performed by one activation source. Figure 16.9 shows a Flow of Chain Transfers.
When the DTC is activated, one control data is selected according to the data read from the DTC vector address corresponding to the activation source, and the selected control data is read from the DTC control data area. When the CHNE bit for the control data is 1 (chain transfers enabled), the next control data immediately following the current control data is read and transferred after the current transfer is completed. This operation is repeated until the data transfer with the control data for which the CHNE bit is 0 (chain transfers disabled) is completed.
Set the CHNE bit in the DTCCR23 register to 0 (chain transfers disabled).

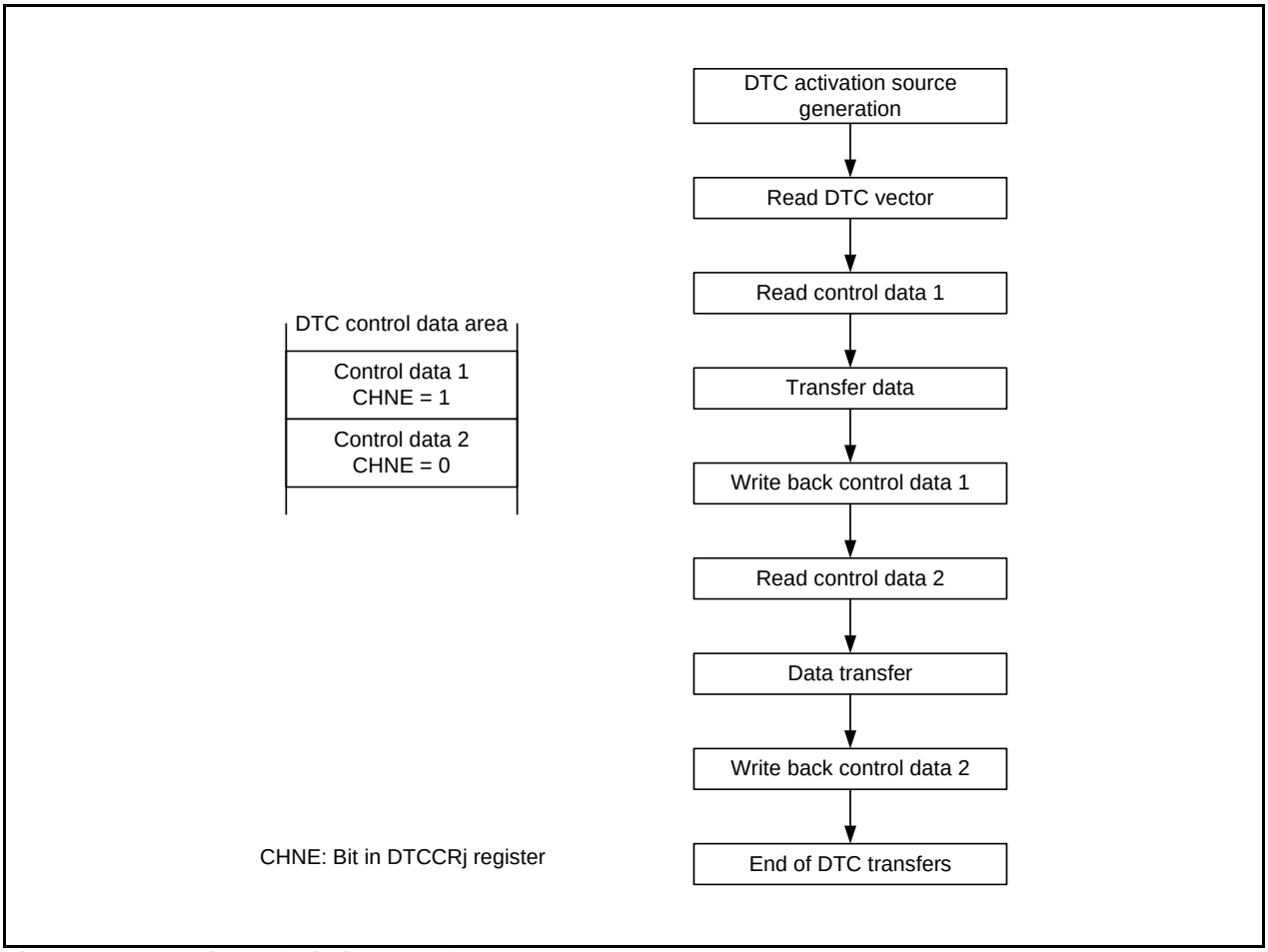


Figure 16.9 Flow of Chain Transfers

16.3.7 Interrupt Sources

When the data transfer causing the DTCCTj (j = 0 to 23) register value to change to 0 is performed in normal mode, and when the data transfer causing the DTCCTj register value to change to 0 is performed while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled) in repeat mode, the interrupt request corresponding to the activation source is generated for the CPU during DTC operation. However, no interrupt request is generated for the CPU when the activation source is SSU/I^2C bus transmit data empty.
Interrupt requests for the CPU are affected by the I flag or interrupt control register. In chain transfers, whether the interrupt request is generated or not is determined either by the number of transfer times specified for the first type of the transfer or the RPTINT bit. When an interrupt request is generated for the CPU, the bit among bits DTCENi0 to DTCENi7 in the DTCENi (i = 0 to 6) registers corresponding to the activation source are set to 0 (activation disabled).

16.3.8 Operation Timings

The DTC requires four clock cycles to read control data allocated in the DTC control data area. The number of clock cycles required to write back control data differs depending on the control data settings.
Figure 16.10 shows an Example of DTC Operation Timings and Figure 16.11 shows an Example of DTC Operation Timings in Chain Transfers.
Table 16.8 shows the Specifications of Control Data Write-Back Operation.

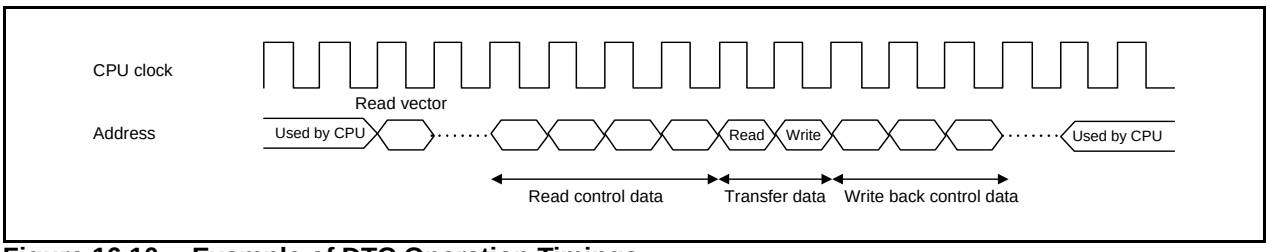


Figure 16.10 Example of DTC Operation Timings

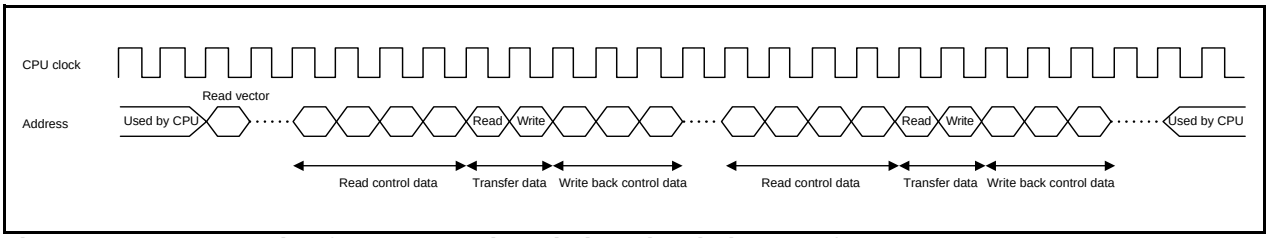


Figure 16.11 Example of DTC Operation Timings in Chain Transfers

Table 16.8 Specifications of Control Data Write-Back Operation

Bits b3 to b0 in DTCCR Register	Operating Mode	Address Control		Control Data to be Written Back				Number of Clock Cycles
		Source	Destination	DTCCTj Register	DTRLDj Register	DTSARj Register	DTDARj Register	
00X0b	Normal mode	Fixed	Fixed	Written back	Written back	Not written back	Not written back	1
01X0b		Incremented	Fixed	Written back	Written back	Written back	Not written back	2
10X0b		Fixed	Incremented	Written back	Written back	Not written back	Written back	2
11X0b		Incremented	Incremented	Written back	Written back	Written back	Written back	3
0X11b	Repeat mode	Repeat area	Fixed	Written back	Written back	Written back	Not written back	2
1X11b			Incremented	Written back	Written back	Written back	Written back	3
X001b		Fixed	Repeat area	Written back	Written back	Not written back	Written back	2
X101b		Incremented		Written back	Written back	Written back	Written back	3

j = 0 to 23
X: 0 or 1

16.3.9 Number of DTC Execution Cycles

Table 16.9 shows the Operations Following DTC Activation and Required Number of Cycles for each operation.
Table 16.10 shows the Number of Clock Cycles Required for Data Transfers.

Table 16.9 Operations Following DTC Activation and Required Number of Cycles

Vector Read	Control Data Read/Write (J)	Data Read	Data Write	Internal Operation
1	5 to 7	(Note 1)	(Note 1)	2
1	5 to 7	(Note 1)	(Note 1)	2

Note:
1. For the number of clock cycles required for data read/write, see **Table 16.10 Number of Clock Cycles Required for Data Transfers**.

Data is transferred as described below, when the DTBLSj (j = 0 to 23) register = N,
(1) When N = 2n (even), two-byte transfers are performed n times.
(2) When N = 2n + 1 (odd), 2-byte transfers are performed n times followed by one 1-byte transfer.

Table 16.10 Number of Clock Cycles Required for Data Transfers

Operation	Unit of Transfers	On-Chip RAM (During DTC Transfers)		On-Chip ROM (User Area)	On-Chip ROM (Data Area)	SFR (Word Access)		SFR (Byte Access)
		Even Address	Odd Address			Even Address	Odd Address	
Data read	1-byte SK1	1		1	2	2		2
	2-byte SK2	1	2	2	4	2	4	4
Data write	1-byte SL1	1		—	—	2		2
	2-byte SL2	1	2	—	—	2	4	4

From Tables 16.9 and 16.10, the total number of required execution cycles can be obtained by the following formula:

Number of required execution cycles = 1 + Σ[formula A] + 2
Σ: Sum of the cycles for the number of transfer times performed by one activation source ([the number of transfer times for which CHNE is set to 1] + 1)

(1) For N = 2n (even)
Formula A = J + n • SK2 + n • SL2
(2) For N = 2n+1 (odd)
Formula A = J + n • SK2 + 1 • SK1 + n • SL2 + 1 • SL1
J: Number of cycles required to read or write back control data

16.3.10 DTC Activation Source Acknowledgement and Interrupt Source Flags

16.3.10.1 Interrupt Sources Except for Flash Memory, Timer RC, Timer RD, and Synchronous Serial Communication Unit (SSU)/I²C bus

When the DTC activation source is an interrupt source except for the flash memory, timer RC, timer RD, or the synchronous serial communication unit/I²C bus, the same DTC activation source cannot be acknowledged for 8 to 12 cycles of the CPU clock after the interrupt source is generated. If a DTC activation source is generated during DTC operation and acknowledged, the same DTC activation source cannot be acknowledged for 8 to 12 cycles of the CPU clock on completion of the DTC transfer immediately before the DTC is activated by the source.

16.3.10.2 Flash Memory

When the DTC activation source is flash memory ready status, even if a flash memory ready status interrupt request is generated, it is not acknowledged as the DTC activation source after the RDYSTI bit in the FST register is set to 1 (flash memory ready status interrupt request) and before the DTC sets the RDYSTI bit to 0 (no flash memory ready status interrupt request). If a flash memory ready status interrupt request is generated after the DTC sets the RDYSTI bit to 0, the DTC acknowledges it as the activation source. 8 to 12 cycles of the CPU clock are required after the RDYSTI bit is set to 1 and before the DTC sets the interrupt request flag to 0. If a flash memory ready status interrupt request is generated during DTC operation and acknowledged as the DTC activation source, the RDYSTI bit is set to 0 after 8 to 12 cycles of the CPU clock on completion of the DTC transfer immediately before the DTC is activated by the source.

16.3.10.3 Timer RC, Timer RD

When the DTC activation source is an interrupt source for timer RC or timer RD, even if an input capture/compare match in individual timers occurs, it is not acknowledged as the DTC activation source after the interrupt source flag is set to 1 and before the DTC sets the flag to 0. If an input capture/compare match occurs after the DTC sets the interrupt source flag to 0, the DTC acknowledges it as the activation source. 8 to 12 cycles of the CPU clock plus 0.5 to 1.5 cycles of the timer operating clock are required after the interrupt source flag is set to 1 and before the DTC sets the flag to 0. If individual DTC activation sources are generated for timer C and timer D during DTC operation and acknowledged, the interrupt source flag is set to 0 after 8 to 12 cycles of the CPU clock plus 0.5 to 1.5 cycles of the timer operating clock on completion of the DTC transfer immediately before the DTC is activated by the source.

16.3.10.4 SSU/I²C bus Receive Data Full

When the DTC activation source is SSU/I²C bus receive data full, read the SSRDR register/the ICDRR register using a data transfer. The RDRF bit in the SSSR register/the ICSR register is set to 0 (no data in SSRDR/ICDRR register) by reading the SSRDR register/ the ICDRR register. If an interrupt source for receive data full is subsequently generated, the DTC acknowledges it as the activation source.

16.3.10.5 SSU/I²C bus Transmit Data Empty

When the DTC activation source is SSU/I²C bus transmit data empty, write to the SSTDR register/the ICDRT register using a data transfer. The TDRE bit in the SSSR register/the ICSR register is set to 0 (data is not transferred from registers SSTDR/ICDRT to SSTRSR/ICDRS) by writing to the SSTDR register/the ICDRT register. If an interrupt source for transmit data empty is subsequently generated, the DTC acknowledges it as the activation source.

16.4 Notes on DTC

16.4.1 DTC activation source

- Do not generate any DTC activation sources before entering wait mode or during wait mode.
- Do not generate any DTC activation sources before entering stop mode or during stop mode.

16.4.2 DTCENi (i = 0 to 6) Registers

- Modify bits DTCENi0 to DTCENi7 only while an interrupt request corresponding to the bit is not generated.
- When the interrupt source flag in the status register for the peripheral function is 1, do not modify the corresponding activation source bit among bits DTCENi0 to DTCENi7.
- Do not access the DTCENi register using a DTC transfer.

16.4.3 Peripheral Modules

- Do not set the status register bit for the peripheral function to 0 using a DTC transfer.
- When the DTC activation source is SSU/I^{2}C bus receive data full, read the SSRDR register/the ICDRR register using a DTC transfer.
  The RDRF bit in the SSSR register/the ICSR register is set to 0 (no data in SSRDR/ICDRR register) by reading the SSRDR register/the ICDRR register.
  However, the RDRF bit is not set to 0 by reading the SSRDR register/the ICDRR register when the DTC data transfer setting is either of the following:
  - Transfer causing the DTCCTj (j = 0 to 23) register value to change from 1 to 0 in normal mode
  - Transfer causing the DTCCRj register value to change from 1 to 0 while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled) in repeat mode.
- When the DTC activation source is SSU/I^{2}C bus transmit data empty, write to the SSTDR register/the ICDRT register using a DTC transfer. The TDRE bit in the SSSR register/the ICSR register is set to 0 (data is not transferred from registers SSTDR/ICDRT to SSTRSR/ICDRS) by writing to the SSTDR register/the ICDRT register.

17. Timers

The following six types of timers are available:

- Timer RA: 8-bit timer with an 8-bit prescaler
- Timer RB: 8-bit timer with an 8-bit prescaler
- Timer RC: 16-bit timer
- Timer RD: Two 16-bit timers
- Timer RE: 4-bit counter and 8-bit counter
- Timer RG: 16-bit timer

All these timers operate independently.

Table 17.1 Functional Comparison of Timers

Item		Timer RA0	Timer RB	Timer RC	Timer RD	Timer RE	Timer RG
Configuration		8-bit timer with 8-bit prescaler (with reload register)	8-bit timer with 8-bit prescaler (with reload register)	16-bit timer (with input capture and output compare)	16-bit timer × 2 (with input capture and output compare)	4-bit counter 8-bit counter	16-bit timer (with input capture and output compare)
Count		Decrement	Decrement	Increment	Increment/Decrement	Increment	Increment/ Decrement
Count sources		• f1 • f2 • f8 • fOCO • fC32 • fC	• f1 • f2 • f8 • Timer RA underflow	• f1 • f2 • f4 • f8 • f32 • fOCO40M • fOCO-F • TRCCLK	• f1 • f2 • f4 • f8 • f32 • fOCO40M • fOCO-F • TRDCLK	• f4 • f8 • f32 • fC4	• f1 • f2 • f4 • f8 • f32 • fOCO40M • TRGCLKA • TRGCLKB
Function	Count of the internal count source	Timer mode	Timer mode	Timer mode (output compare function)	Timer mode (output compare function)	—	Timer mode (output compare function)
	Count of the external count source	Event counter mode	—	Timer mode (output compare function)	Timer mode (output compare function)	—	Timer mode (output compare function), Please counting mode
	External pulse width/period measurement	Pulse width measurement mode, pulse period measurement mode	—	Timer mode (input capture function; 4 pins)	Timer mode (input compare function; 2 × 4 pins)	—	Timer mode (Input capture function; 2 pins)
	PWM output	Pulse output mode (1), Event counter mode (1)	Programmable waveform generation mode	Timer mode (output compare function; 4 pins) (1), PWM mode (3 pins), PWM2 mode (1 pin)	Timer mode (output compare function; 2 × 4 pins) (1), PWM mode (2 × 3 pins), PWM3 mode (2 × 2 pins)	Output compare mode (1)	Timer mode (output compare function; 2 pins), PWM mode (1 pin)
	One-shot waveform output	—	Programmable one-shot generation mode, Programmable wait one-shot generation mode	PWM mode (3 pins)	PWM mode (2 × 3 pins)	—	—
	Three-phase waveforms output	—	—	—	Reset synchronous PWM mode (2 × 3 pins, Sawtooth wave modulation), Complementary PWM mode (2 × 3 pins, triangular wave modulation, dead time)	—	—
	Timer	Timer mode (only fC32 count)	—	—	—	Real-time clock mode	—
Input pin		TRAIO	$\overline{\text{INT0}}$	$\overline{\text{INT0}}$, TRCCLK, TRCTRG, TRCIOA, TRCIOB, TRCIOC, TRCIOD	$\overline{\text{INT0}}$, TRDCLK, TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1	—	TRGCLKA, TRGCLKB, TRGIOA, TRGIOB
Output pin		TRAO TRAIO	TRBO	TRCIOA, TRCIOB, TRCIOC, TRCIOD	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1	TREO	TRGIOA, TRGIOB
Related interrupt		Timer RA interrupt	Timer RB interrupt, INT0 interrupt	Compare match/input capture A to D interrupt, Overflow interrupt, $\overline{\text{INT0}}$ interrupt	Compare match/input capture A0 to D0 interrupt, Compare match/input capture A1 to D1 interrupt, Overflow interrupt, Underflow interrupt (2), $\overline{\text{INT0}}$ interrupt	Timer RE interrupt	Compare match/ input capture A to B interrupt, Underflow interrupt (2), Overflow interrupt
Timer stop		Provided	Provided	Provided	Provided	Provided	Provided

Notes:
1. Rectangular waves are output in these modes. Since the waves are inverted at each overflow, the “H” and “L” level widths of the pulses are the same.
2. The underflow interrupt can be set to timer RD1 and timer RG.

18. Timer RA

Timer RA is an 8-bit timer with an 8-bit prescaler.

18.1 Introduction

The prescaler and timer each consist of a reload register and counter. The reload register and counter are allocated at the same address, and can be accessed when accessing registers TRAPRE and TRA (refer to **Tables 18.2 to 18.6 the Specifications of Each Mode**).
The count source for timer RA is the operating clock that regulates the timing of timer operations such as counting and reloading.
Figure 18.1 shows the Timer RA Block Diagram. Table 18.1 lists the Timer RA Pin Configuration.

Timer RA supports the following five operating modes:

- Timer mode: The timer counts an internal count source.
- Pulse output mode: The timer counts an internal count source and outputs pulses which invert the polarity by underflow of the timer.
- Event counter mode: The timer counts external pulses.
- Pulse width measurement mode: The timer measures the pulse width of an external pulse.
- Pulse period measurement mode: The timer measures the pulse period of an external pulse.

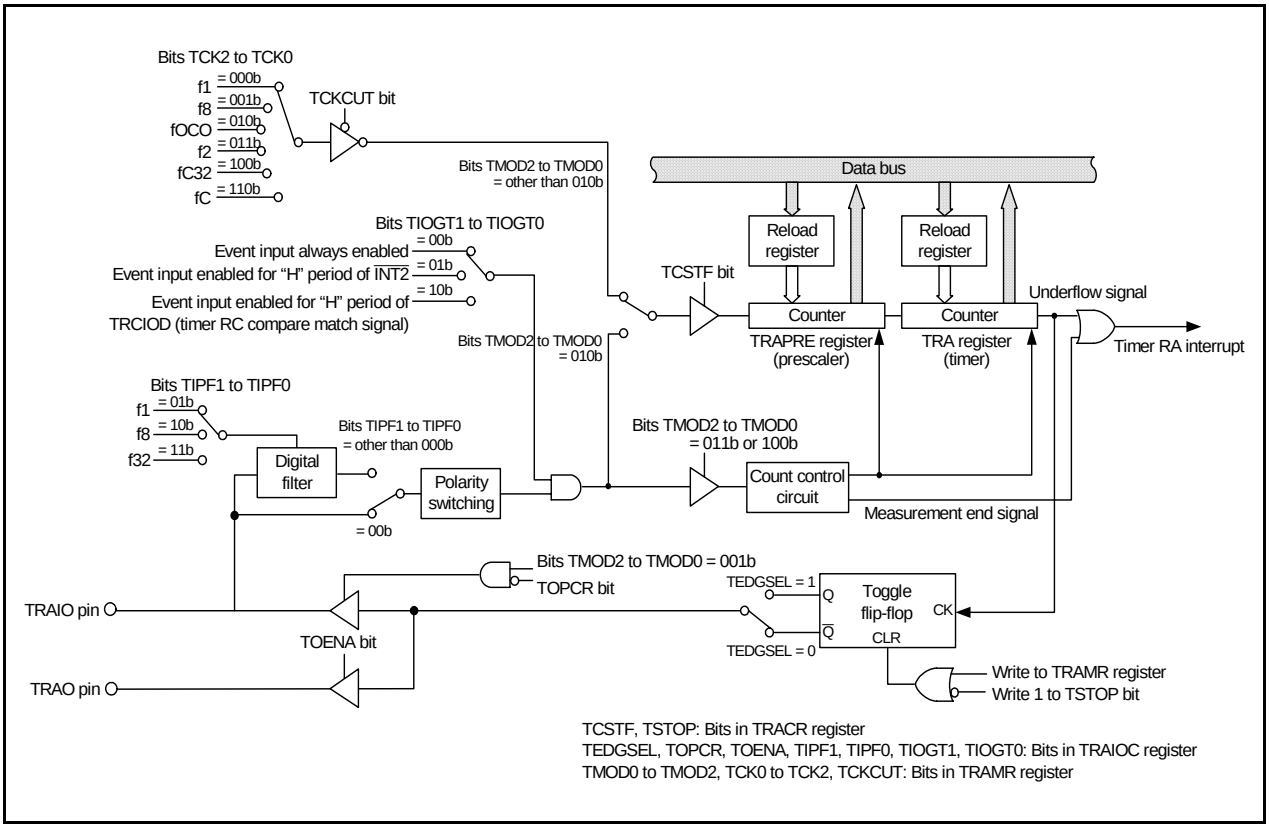


Figure 18.1 Timer RA Block Diagram

Table 18.1 Timer RA Pin Configuration

Pin Name	Assigned Pin	I/O	Function
TRAIO	P11_4	I/O	Function differs according to the mode. Refer to descriptions of individual modes for details.
TRAO	P11_5	Output	

18.2 Registers

18.2.1 Timer RA Control Register (TRACR)

Address 0100h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	TUNDF	TEDGF	—	TSTOP	TCSTF	TSTART
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RA count start bit (1)	0: Count stops 1: Count starts	R/W
b1	TCSTF	Timer RA count status flag (1)	0: Count stops 1: During count operation	R
b2	TSTOP	Timer RA count forcible stop bit (2)	When this bit is set to 1, the count is forcibly stopped. When read, the content is 0.	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TEDGF	Active edge judgment flag (3, 4)	0: Active edge not received 1: Active edge received (end of measurement period)	R/W
b5	TUNDF	Timer RA underflow flag (3, 4)	0: No underflow 1: Underflow	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

Notes:
1. Refer to **18.8 Notes on Timer RA** for notes regarding bits TSTART and TCSTF.
2. When 1 is written to the TSTOP bit, bits TSTART and TCSTF and registers TPRAPRE and TRA are set to the values after a reset.
3. Bits TEDGF and TUNDF can be set to 0 by writing 0 to these bits by a program. However, their value remains unchanged when 1 is written.
4. Set to 0 in timer mode, pulse output mode, and event counter mode.

In pulse width measurement mode and pulse period measurement mode, use the MOV instruction to set the TRACR register. If it is necessary to avoid changing the values of bits TEDGF and TUNDF, write 1 to them.

18.2.2 Timer RA I/O Control Register (TRAIOC)

Address 0101h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	TIOSEL	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIO polarity switch bit	Function varies according to the operating mode.	R/W
b1	TOPCR	TRAIO output control bit		R/W
b2	TOENA	TRAO output enable bit		R/W
b3	TIOSEL	Hardware LIN function select bit		R/W
b4	TIPF0	TRAIO input filter select bit		R/W
b5	TIPF1			R/W
b6	TIOGT0	TRAIO event input control bit		R/W
b7	TIOGT1			R/W

18.2.3 Timer RA Mode Register (TRAMR)

Address 0102h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCKCUT	TCK2	TCK1	TCK0	—	TMOD2	TMOD1	TMOD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TMOD0	Timer RA operating mode select bit	b2 b1 b0 0 0 0: Timer mode 0 0 1: Pulse output mode 0 1 0: Event counter mode 0 1 1: Pulse width measurement mode 1 0 0: Pulse period measurement mode 1 0 1: Do not set. 1 1 0: Do not set. 1 1 1: Do not set.	R/W
b1	TMOD1			R/W
b2	TMOD2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TCK0	Timer RA count source select bit	b6 b5 b4 0 0 0: f1 0 0 1: f8 0 1 0: fOCO 0 1 1: f2 1 0 0: fC32 1 0 1: Do not set. 1 1 0: fC 1 1 1: Do not set.	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	TCKCUT	Timer RA count source cutoff bit	0: Count source provided 1: Count source cut off	R/W

When both the TSTART and TCSTF bits in the TRACR register are set to 0 (count stops), rewrite the TRAMR register.

18.2.4 Timer RA Prescaler Register (TRAPRE)

Address 0103h

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	—	—	—	—	—	—	
After Reset	1	1	1	1	1	1	1	1	(Note 1)

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Counts an internal count source.	00h to FFh	R/W
	Pulse output mode		00h to FFh	R/W
	Event counter mode	Counts an external count source.	00h to FFh	R/W
	Pulse width measurement mode	Measures the pulse width of input pulses from external (counts an internal count source).	00h to FFh	R/W
	Pulse period measurement mode	Measures the pulse period of input pulses from external (counts an internal count source).	00h to FFh	R/W

Note:
1. When 1 is written to the TSTOP bit in the TRACR register, the TRAPRE register is set to FFh.

18.2.5 Timer RA Register (TRA)

Address 0104h

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	—	—	—	—	—	—	
After Reset	1	1	1	1	1	1	1	1	(Note 1)

Bit	Mode	Function	Setting Range	R/W
b7 to b0	All modes	Counts the TRAPRE register underflows.	00h to FFh	R/W

Note:
1. When 1 is written to the TSTOP bit in the TRACR register, the TRAPRE register is set to FFh.

18.2.6 Timer RA Pin Select Register (TRASR)

Address 0180h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	TRAIOSEL1	TRAIOSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRAIOSEL0	TRAIO pin select bit	b1 b0 0 0: TRAIO pin not used 0 1: P11_4 assigned 1 0: $\overline{\text{INT4}}$ assigned 1 1: Do not set.	R/W
b1	TRAIOSEL1			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. To use hardware LIN, set 01b to bits TRAIOSEL1 to TRAIOSEL0.

To use the I/O pin for timer RA, set the TRASR register.
Set this register before setting the timer RA associated registers. Also, do not change the setting value of this register during timer RA operation.

18.3 Timer Mode

In this mode, the timer counts an internally generated count source (refer to **Table 18.2**).

Table 18.2 Timer Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO, fC32
Count operations	• Decrement • When the timer underflows, the contents of the reload register are reloaded and the count is continued.
Division ratio	1/(n+1)(m+1) n: Value set in TRAPRE register, m: Value set in TRA register
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.
Interrupt request generation timing	When timer RA underflows [timer RA interrupt].
TRAIO pin function	Programmable I/O port
TRAO pin function	Programmable I/O port
Read from timer	The count value can be read out by reading registers TRA and TRAPRE.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during count operation, values are written to the reload register and counter (refer to **18.3.2 Timer Write Control during Count Operation**).

18.3.1 Timer RA I/O Control Register (TRAIOC) in Timer Mode

Address 0101h

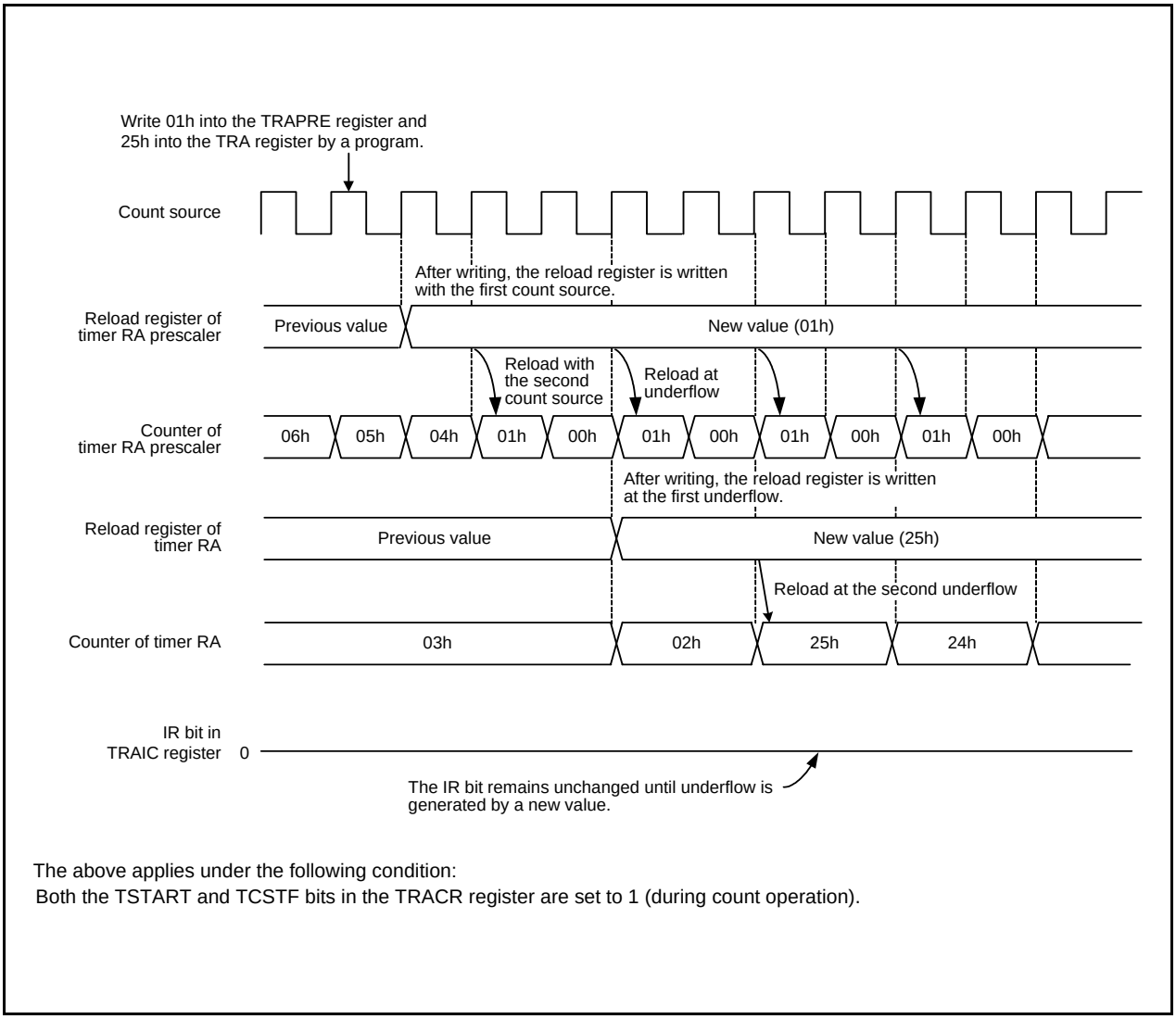
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	TIOSEL	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIO polarity switch bit	Set to 0 in timer mode.	R/W
b1	TOPCR	TRAIO output control bit		R/W
b2	TOENA	TRAO output enable bit		R/W
b3	TIOSEL	Hardware LIN function select bit	Set to 0. However, set to 1 when the hardware LIN function is used.	R/W
b4	TIPF0	TRAIO input filter select bit	Set to 0 in timer mode.	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRAIO event input control bit		R/W
b7	TIOGT1			R/W

18.3.2 Timer Write Control during Count Operation

Timer RA has a prescaler and a timer (which counts the prescaler underflows). The prescaler and timer each consist of a reload register and a counter. When writing to the prescaler or timer, values are written to both the reload register and counter.

However, values are transferred from the reload register to the counter of the prescaler in synchronization with the count source. In addition, values are transferred from the reload register to the counter of the timer in synchronization with prescaler underflows. Therefore, if the prescaler or timer is written to when count operation is in progress, the counter value is not updated immediately after the WRITE instruction is executed. Figure 18.2 shows an Operating Example of Timer RA when Counter Value is Rewritten during Count Operation.



The above applies under the following condition:
Both the TSTART and TCSTF bits in the TRACR register are set to 1 (during count operation).

Figure 18.2 Operating Example of Timer RA when Counter Value is Rewritten during Count Operation

18.4 Pulse Output Mode

In pulse output mode, an internally generated count source is counted, and a pulse with inverted polarity is output from the TRAIO pin each time the timer underflows (refer to **Table 18.3**).

Table 18.3 Pulse Output Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO, fC32, fC
Count operations	• Decrement • When the timer underflows, the contents of the reload register are reloaded and the count is continued.
Division ratio	1/(n+1)(m+1) n: Value set in TRAPRE register, m: Value set in TRA register
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.
Interrupt request generation timing	When timer RA underflows [timer RA interrupt].
TRAIO pin function	Pulse output or programmable output port
TRAO pin function	Programmable I/O port or inverted output of TRAIO
Read from timer	The count value can be read out by reading registers TRA and TRAPRE.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during count operation, values are written to the reload register and counter (refer to **18.3.2 Timer Write Control during Count Operation**).
Selectable functions	• TRAIO signal polarity switch function The level when the pulse output starts is selected by the TEDGSEL bit in the TRAIOC register. (1) • TRAO output function Pulses inverted from the TRAIO output polarity can be output from the TRAO pin (selectable by the TOENA bit in the TRAIOC register). • Pulse output stop function Output from the TRAIO pin is stopped by the TOPCR bit in the TRAIOC register. • TRAIO pin select function Use of the TRAIO pin is selected by the TRAIOSEL0 bit in the TRASR register.

Note:
1. By writing to the TRAMR register, the output pulse is set to the level when the pulse output starts.

18.4.1 Timer RA I/O Control Register (TRAIOC) in Pulse Output Mode

Address 0101h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	TIOSEL	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIO polarity switch bit	0: TRAIO output starts at high 1: TRAIO output starts at low	R/W
b1	TOPCR	TRAIO output control bit	0: TRAIO output 1: Port P11_4	R/W
b2	TOENA	TRAO output enable bit	0: Port P11_5 1: TRAO output (inverted TRAIO output is output from P11_5)	R/W
b3	TIOSEL	Hardware LIN function select bit	Set to 0.	R/W
b4	TIPF0	TRAIO input filter select bit	Set to 0 in pulse output mode.	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRAIO event input control bit		R/W
b7	TIOGT1			R/W

18.5 Event Counter Mode

In event counter mode, external signal inputs to the TRAIO pin are counted (refer to **Table 18.4**).

Table 18.4 Event Counter Mode Specifications

Item	Specification
Count source	External signal input to the TRAIO pin (active edge selectable by a program)
Count operations	• Decrement • When the timer underflows, the contents of the reload register are reloaded and the count is continued.
Division ratio	1/(n+1)(m+1) n: Value set in TRAPRE register, m: Value set in TRA register
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.
Interrupt request generation timing	When timer RA underflows [timer RA interrupt].
TRAIO pin function	Count source input
TRAO pin function	Programmable I/O port or pulse output (1)
Read from timer	The count value can be read out by reading registers TRA and TRAPRE.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during count operation, values are written to the reload register and counter (refer to **18.3.2 Timer Write Control during Count Operation**).
Selectable functions	• $\overline{\text{INT2}}$ input polarity switch function The active edge of the count source is selected by the TEDGSEL bit in the TRAIOC register. • Count source input pin select function Use of the TRAIO pin is selected by the TRAIOSEL0 bit in the TRASR register. • Pulse output function Pulses of inverted polarity can be output from the TRAO pin each time the timer underflows (selectable by the TOENA bit in the TRAIOC register). (1) • Digital filter function Whether enabling or disabling the digital filter and the sampling frequency is selected by bits TIPF0 and TIPF1 in the TRAIOC register. • Event input control function The enabled period for the event input to the TRAIO pin is selected by bits TIOGT0 and TIOGT1 in the TRAIOC register.

Note:
1. By writing to the TRAMR register, the output pulse is set to the level when the pulse output starts.

18.5.1 Timer RA I/O Control Register (TRAIOC) in Event Counter Mode

Address 0101h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	TIOSEL	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIO polarity switch bit	0: Count at the rising edge of TRAIO input and TRAO output starts at low 1: Count at the falling edge of TRAIO input and TRAO output starts at high	R/W
b1	TOPCR	TRAIO output control bit	Set to 0 in event counter mode.	R/W
b2	TOENA	TRAO output enable bit	0: Port P11_05 1: TRAO output	R/W
b3	TIOSEL	Hardware LIN function select bit	Set to 0.	R/W
b4	TIPF0	TRAIO input filter select bit (1)	b5 b4 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRAIO event input control bit	b7 b6 0 0: Event input always enabled 0 1: Event input enabled for high-level period of $\overline{\text{INT2}}$ 1 0: Event input enabled for low-level period of timer RC compare match signal 1 1: Do not set.	R/W
b7	TIOGT1			R/W

Note:
1. When the same value from the TRAIO pin is sampled three times continuously, the input is determined.

18.6 Pulse Width Measurement Mode

In pulse width measurement mode, the pulse width of an external signal input to the TRAIO pin is measured (refer to **Table 18.5**).
Figure 18.3 shows an Operating Example in Pulse Width Measurement Mode.

Table 18.5 Pulse Width Measurement Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO, fC32, fC
Count operations	• Decrement • The count is continued only while the measured pulse is high or low level. • When the timer underflows, the contents of the reload register are reloaded and the count is continued.
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.
Interrupt request generation timing	• When timer RA underflows [timer RA interrupt]. • Rising or falling of the TRAIO input (end of measurement period) [timer RA interrupt]
TRAIO pin function	Measured pulse input
TRAO pin function	Programmable I/O port
Read from timer	The count value can be read out by reading registers TRA and TRAPRE.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during count operation, values are written to the reload register and counter (refer to **18.3.2 Timer Write Control during Count Operation**).
Selectable functions	• Measurement level setting A high-level or low-level period is selected by the TEDGSEL bit in the TRAIOC register. • Measured pulse input pin select function Use of the TRAIO pin is selected by bits TRAIOSEL0 in the TRASR register. • Digital filter function Whether enabling or disabling the digital filter and the sampling frequency is selected by bits TIPF0 and TIPF1 in the TRAIOC register.

18.6.1 Timer RA I/O Control Register (TRAIOC) in Pulse Width Measurement Mode

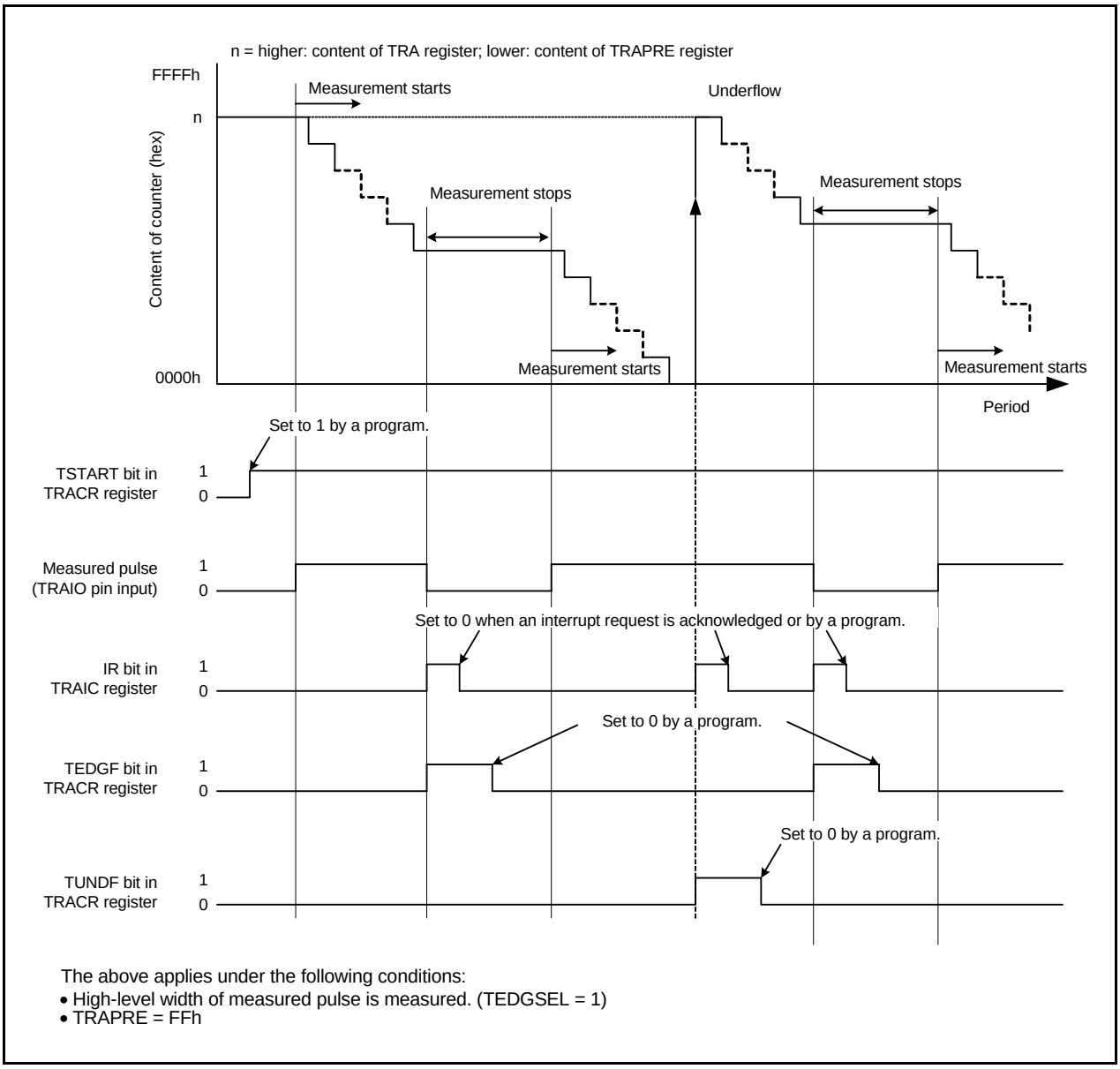
Address 0101h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	TIOSEL	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIO polarity switch bit	0: Low-level width of TRAIO input is measured 1: High-level width of TRAIO input is measured	R/W
b1	TOPCR	TRAIO output control bit	Set to 0 in pulse width measurement mode.	R/W
b2	TOENA	TRAO output enable bit		R/W
b3	TIOSEL	Hardware LIN function select bit	Set to 0. However, set to 1 when the hardware LIN function is used.	R/W
b4	TIPF0	TRAIO input filter select bit (1)	b5 b4 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRAIO event input control bit	Set to 0 in pulse width measurement mode.	R/W
b7	TIOGT1			R/W

Note:
1. When the same value from the TRAIO pin is sampled three times continuously, the input is determined.

18.6.2 Operating Example



The above applies under the following conditions:
- High-level width of measured pulse is measured. (TEDGSEL = 1)
- TRAPRE = FFh

Figure 18.3 Operating Example in Pulse Width Measurement Mode

18.7 Pulse Period Measurement Mode

In pulse period measurement mode, the pulse period of an external signal input to the TRAIO pin is measured (refer to **Table 18.6**).
Figure 18.4 shows an Operating Example in Pulse Period Measurement Mode.

Table 18.6 Pulse Period Measurement Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO, fC32, fC
Count operations	• Decrement • After the active edge of the measured pulse is input, the contents of the read-out buffer are retained at the first underflow of timer RA prescaler. Then timer RA reloads the contents of the reload register at the second underflow of timer RA prescaler and continues counting.
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.
Count stop conditions	• 0 (count stops) is written to TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.
Interrupt request generation timing	• When timer RA underflows or reloads [timer RA interrupt]. • Rising or falling of the TRAIO input (end of measurement period) [timer RA interrupt]
TRAIO pin function	Measured pulse input (1)
TRAO pin function	Programmable I/O port
Read from timer	The count value can be read out by reading registers TRA and TRAPRE.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during count operation, values are written to the reload register and counter (refer to **18.3.2 Timer Write Control during Count Operation**).
Selectable functions	• Measurement period selection The measurement period of the input pulse is selected by the TEDGSEL in the TRAIOC register. • Measured pulse input pin select function Use of the TRAIO pin is selected by bits TRAIOSEL0 in the TRASR register. • Digital filter function Whether enabling or disabling the digital filter and the sampling frequency is selected by bits TIPF0 and TIPF1 in the TRAIOC register.

Note:
1. Input a pulse with a period longer than twice the timer RA prescaler period. Also, input a pulse with a longer high-/low-level width than the timer RA prescaler period. If a pulse with a shorter period is input to the TRAIO pin, the input may be ignored.

18.7.1 Timer RA I/O Control Register (TRAIOC) in Pulse Period Measurement Mode

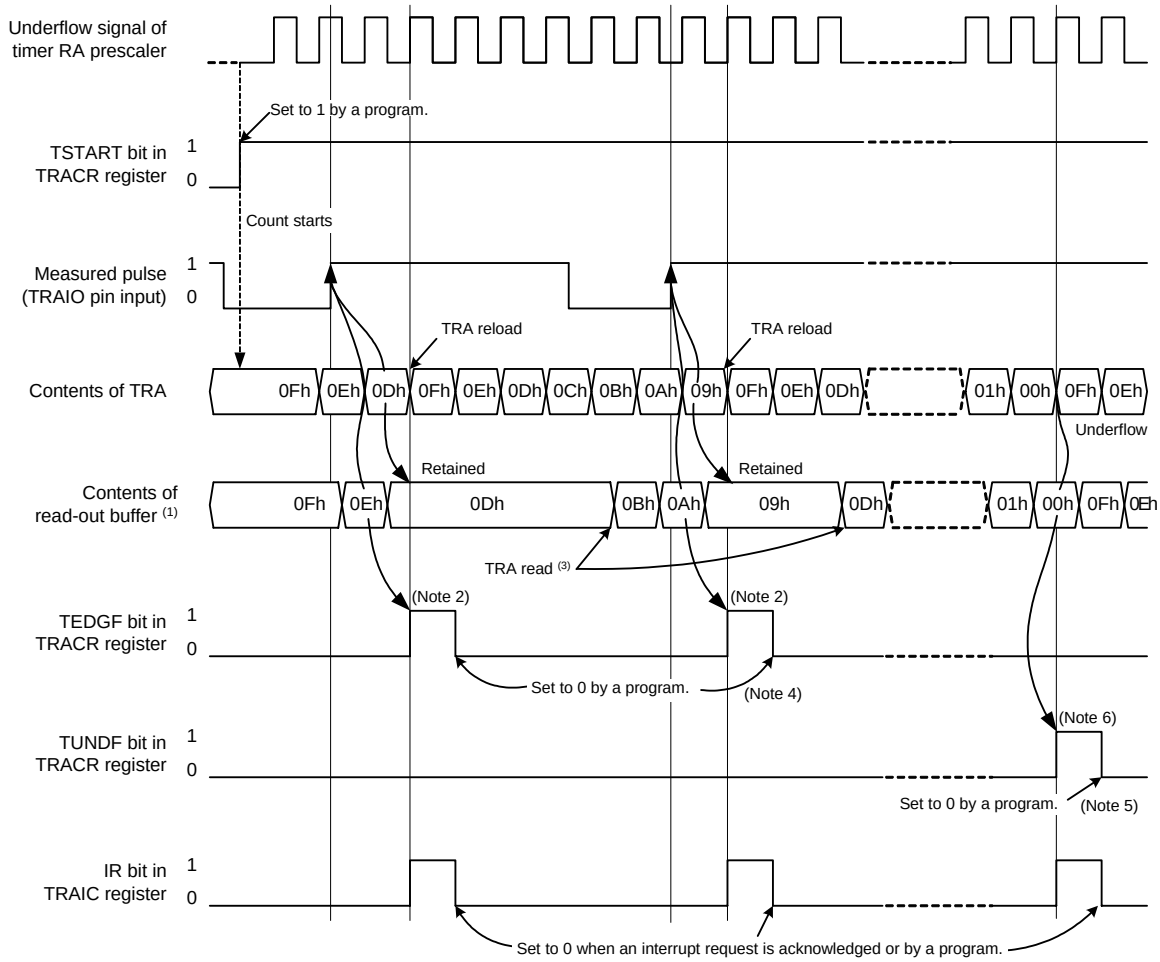
Address 0101h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	TIOSEL	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIO polarity switch bit	0: Period from one rising edge to next rising edge of measured pulse is measured 1: Period from one falling edge to next falling edge of measured pulse is measured	R/W
b1	TOPCR	TRAIO output control bit	Set to 0 in pulse period measurement mode.	R/W
b2	TOENA	TRAO output enable bit		R/W
b3	TIOSEL	Hardware LIN function select bit	Set to 0.	R/W
b4	TIPF0	TRAIO input filter select bit (1)	b5 b4 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRAIO event input control bit	Set to 0 in pulse period measurement mode.	R/W
b7	TIOGT1			R/W

Note:
1. When the same value from the TRAIO pin is sampled three times continuously, the input is determined.

18.7.2 Operating Example



The above applies when the period from one rising edge to the next rising edge of the measured pulse is measured (TEDGSEL = 0) with the initial value of the TRA register as 0Fh.

Notes:
1. The content of the read-out buffer can be read by reading the TRA register in pulse period measurement mode.
2. After an active edge of the measured pulse is input, the TEDGF bit in the TRACR register is set to 1 (active edge received) when the timer RA prescaler underflows for the second time.
3. The TRA register should be read before the next active edge is input after the TEDGF bit is set to 1 (active edge received). The contents of the read-out buffer are retained until the TRA register is read. If the TRA register is not read before the next active edge is input, the measured result of the previous period is retained.
4. To set to 0 by a program, use a MOV instruction to write 0 to the TEDGF bit in the TRACR register. At the same time, write 1 to the TUNDF bit in the TRACR register.
5. To set to 0 by a program, use a MOV instruction to write 0 to the TUNDF bit. At the same time, write 1 to the TEDGF bit.
6. Bits TUNDF and TEDGF are both set to 1 if timer RA underflows and reloads on an active edge simultaneously.

Figure 18.4 Operating Example in Pulse Period Measurement Mode

18.8 Notes on Timer RA

- Timer RA stops counting after a reset. Set the values in the timer RA and timer RA prescalers before the count starts.
- Even if the prescaler and timer RA are read out in 16-bit units, these registers are read 1 byte at a time in the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In pulse period measurement mode, bits TEDGF and TUNDF in the TRACR register can be set to 0 by writing 0 to these bits by a program. However, these bits remain unchanged if 1 is written. When using the READ-MODIFY-WRITE instruction for the TRACR register, the TEDGF or TUNDF bit may be set to 0 although these bits are set to 1 while the instruction is being executed. In this case, write 1 to the TEDGF or TUNDF bit which is not supposed to be set to 0 with the MOV instruction.
- When changing to pulse period measurement mode from another mode, the contents of bits TEDGF and TUNDF are undefined. Write 0 to bits TEDGF and TUNDF before the count starts.
- The TEDGF bit may be set to 1 by the first timer RA prescaler underflow generated after the count starts.
- When using the pulse period measurement mode, leave two or more periods of the timer RA prescaler immediately after the count starts, then set the TEDGF bit to 0.
- The TCSTF bit remains 0 (count stops) for zero or one cycle of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.

  During this time, do not access registers associated with timer RA (1) other than the TCSTF bit. Timer RA starts counting at the first active edge of the count source after The TCSTF bit is set to 1 (during count operation).
  The TCSTF bit remains 1 for zero or one cycle of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RA counting is stopped when the TCSTF bit is set to 0.
  During this time, do not access registers associated with timer RA (1) other than the TCSTF bit.

  Note:
  1. Registers associated with timer RA:
     TRACR, TRAIOC, TRAMR, TRAPRE, and TRA

- When the TRAPRE register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source clock for each write interval.
- When the TRA register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the prescaler underflow for each write interval.

19. Timer RB

Timer RB is an 8-bit timer with an 8-bit prescaler.

19.1 Introduction

The prescaler and timer each consist of a reload register and counter (refer to **Tables 19.2 to 19.5 for the Specifications of Each Mode**) for accessing the reload register and counter. Timer RB has timer RB primary and timer RB secondary as reload registers.
The count source for timer RB is the operating clock that regulates the timing of timer operations such as counting and reloading.
Figure 19.1 shows the Timer RB Block Diagram. Table 19.1 lists the Timer RB Pin Configuration.

Timer RB supports the four operating modes:

- Timer mode: The timer counts an internal count source (peripheral function clock or timer RA underflows).
- Programmable waveform generation mode: The timer outputs pulses of a given width successively.
- Programmable one-shot generation mode: The timer outputs a one-shot pulse.
- Programmable wait one-shot generation mode: The timer outputs a delayed one-shot pulse.

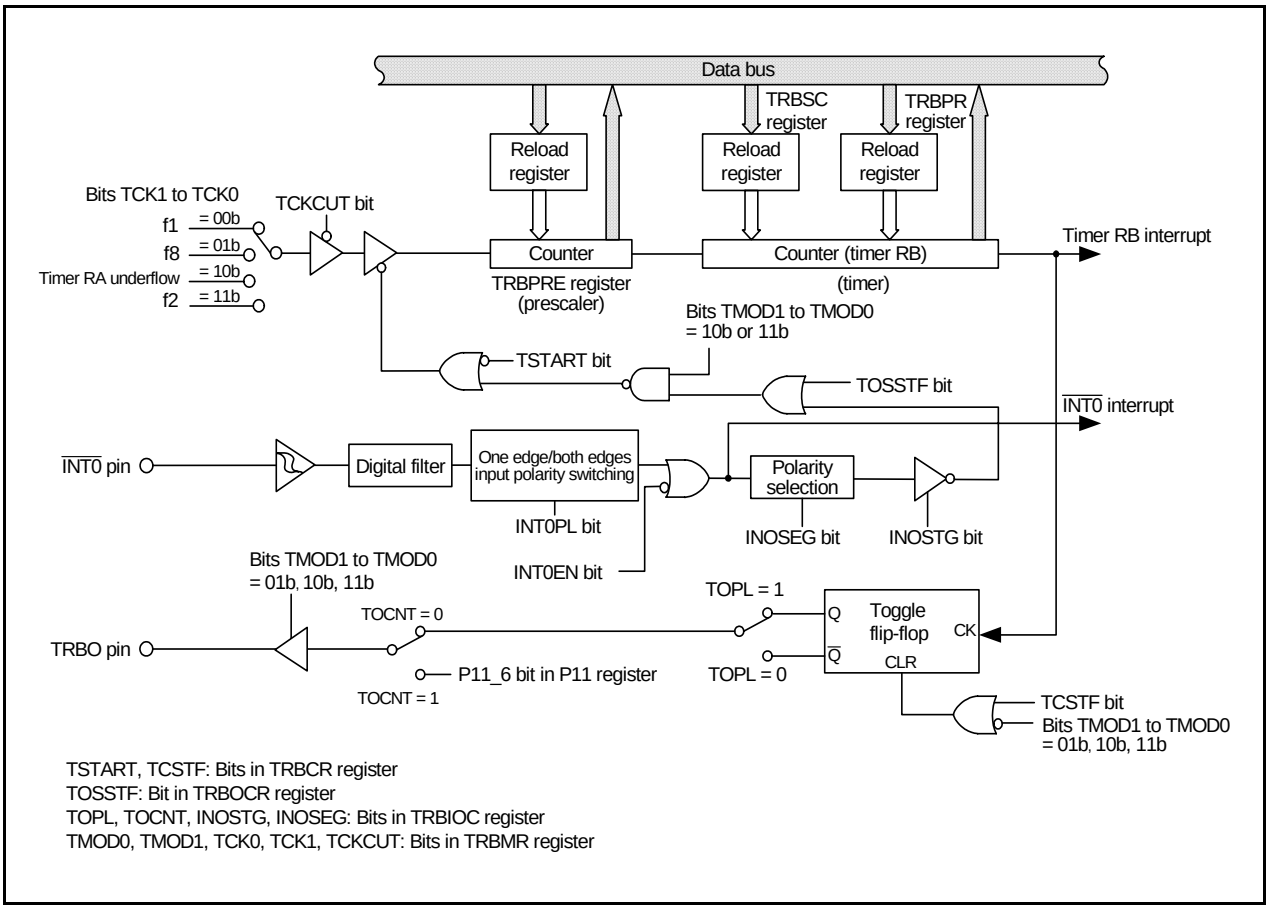


Figure 19.1 Timer RB Block Diagram

Table 19.1 Timer RB Pin Configuration

Pin Name	Assigned Pin	I/O	Function
TRBO	P11_6	Output	Pulse output (programmable waveform generation mode, programmable one-shot generation mode, programmable wait one-shot generation mode)

19.2 Registers

19.2.1 Timer RB Control Register (TRBCR)

Address 0108h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	TSTOP	TCSTF	TSTART
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RB count start bit (1)	0: Count stops 1: Count starts	R/W
b1	TCSTF	Timer RB count status flag (1)	0: Count stops 1: During count operation (3)	R
b2	TSTOP	Timer RB count forcible stop bit (1, 2)	When this bit is set to 1, the count is forcibly stopped. When read, the content is 0.	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Notes:
1. Refer to **19.7 Notes on Timer RB** for precautions regarding bits TSTART, TCSTF and TSTOP.
2. When 1 is written to the TSTOP bit, registers TRBPRE, TRBSC, TRBPR, and bits TSTART and TCSTF, and the TOSSTF bit in the TRBOCR register are set to values after a reset.
3. Indicates that count operation is in progress in timer mode or programmable waveform mode. In programmable one-shot generation mode or programmable wait one-shot generation mode, it indicates that a one-shot pulse trigger has been acknowledged.

19.2.2 Timer RB One-Shot Control Register (TRBOCR)

Address 0109h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	TOSSTF	TOSSP	TOSST
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOSST	Timer RB one-shot start bit	When this bit is set to 1, one-shot trigger generated. When read, the content is 0.	R/W
b1	TOSSP	Timer RB one-shot stop bit	When this bit is set to 1, counting of one-shot pulses (including programmable wait one-shot pulses) stops. When read, the content is 0.	R/W
b2	TOSSTF	Timer RB one-shot status flag (1)	0: One-shot stopped 1: One-shot operating (including wait period)	R
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. When 1 is written to the TSTOP bit in the TRBCR register, the TOSSTF bit is set to 0.

The TRBOCR register is enabled when bits TMOD1 to TMOD0 in the TRBMR register is set to 10b (programmable one-shot generation mode) or 11b (programmable wait one-shot generation mode).

19.2.3 Timer RB I/O Control Register (TRBIOC)

Address 010Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RB output level select bit	Function varies according to the operating mode.	R/W
b1	TOCNT	Timer RB output switch bit		R/W
b2	INOSTG	One-shot trigger control bit		R/W
b3	INOSEG	One-shot trigger polarity select bit		R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

19.2.4 Timer RB Mode Register (TRBMR)

Address 010Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCKCUT	—	TCK1	TCK0	TWRC	—	TMOD1	TMOD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TMOD0	Timer RB operating mode select bit (1)	b1 b0 0 0: Timer mode 0 1: Programmable waveform generation mode 1 0: Programmable one-shot generation mode 1 1: Programmable wait one-shot generation mode	R/W
b1	TMOD1			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	TWRC	Timer RB write control bit (2)	0: Write to reload register and counter 1: Write to reload register only	R/W
b4	TCK0	Timer RB count source select bit (1)	b5 b4 0 0: f1 0 1: f8 1 0: Timer RA underflow 1 1: f2	R/W
b5	TCK1			R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	TCKCUT	Timer RB count source cutoff bit (1)	0: Count source provided 1: Count source cut off	R/W

Notes:
1. Change bits TMOD0 and TMOD1, TCK0 and TCK1, and TCKCUT when both the TSTART and TCSTF bits in the TRBCR register set to 0 (count stops).
2. The TWRC bit can be set to either 0 or 1 in timer mode. In programmable waveform generation mode, programmable one-shot generation mode, or programmable wait one-shot generation mode, the TWRC bit must be set to 1 (write to reload register only).

19.2.5 Timer RB Prescaler Register (TRBPRE)

Address 010Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Counts an internal count source or timer RA underflows.	00h to FFh	R/W
	Programmable waveform generation mode		00h to FFh	R/W
	Programmable one-shot generation mode		00h to FFh	R/W
	Programmable wait one-shot generation mode		00h to FFh	R/W

When 1 is written to the TSTOP bit in the TRBCR register, the TRBPRE register is set to FFh.

19.2.6 Timer RB Secondary Register (TRBSC)

Address 010Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Disabled	00h to FFh	—
	Programmable waveform generation mode	Counts timer RB prescaler underflows (1)	00h to FFh	W (2)
	Programmable one-shot generation mode	Disabled	00h to FFh	—
	Programmable wait one-shot generation mode	Counts timer RB prescaler underflows (one-shot width is counted)	00h to FFh	W (2)

Notes:
1. The values of registers TRBPR and TRBSC are reloaded to the counter alternately and counted.
2. The count value can be read by reading the TRBPR register even when the secondary period is being counted.

When 1 is written to the TSTOP bit in the TRBCR register, the TRBSC register is set to FFh.
To write to the TRBSC register, perform the following steps.
(1) Write the value into the TRBSC register.
(2) Write the value into the TRBPR register. (If the value does not change, write the same value second time.)

19.2.7 Timer RB Primary Register (TRBPR)

Address 010Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Counts timer RB prescaler underflows.	00h to FFh	R/W
	Programmable waveform generation mode	Counts timer RB prescaler underflows. (1)	00h to FFh	R/W
	Programmable one-shot generation mode	Counts timer RB prescaler underflows (one-shot width is counted)	00h to FFh	R/W
	Programmable wait one-shot generation mode	Counts timer RB prescaler underflows (wait period width is counted)	00h to FFh	R/W

Note:
1. The values of registers TRBPR and TRBSC are reloaded to the counter alternately and counted.

When 1 is written to the TSTOP bit in the TRBCR register, the TRBPR register is set to FFh.

19.2.8 Timer RB/RC Pin Select Register (TRBRCSR)

Address 0181h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRCTRGSEL1	TRCTRGSEL0	—	TRCCLKSEL0	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	—			
b4	TRCCLKSEL0	TRCCLK pin select bit	0: TRCCLK pin not used 1: TRCCLK pin used	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	TRCTRGSEL0	TRCTRG pin select bit	b7 b6 0 0: TRCTRG pin not used 0 1: P3_7 assigned 1 0: P4_3 assigned 1 1: P4_4 assigned	R/W
b7	TRCTRGSEL1			R/W

The register function for timer RB is not implemented.
To use the I/O pins for timer RC, set the TRBRCSR register.
Set this register before setting the timer RC associated registers. Also, do not change the setting value of the TRCCLKSEL0 bit during timer RC operation.

19.3 Timer Mode

In timer mode, a internally generated count source or timer RA underflows are counted (refer to **Table 19.2**). Registers TRBOCR and TRBSC are not used in this mode.

Table 19.2 Timer Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RA underflow
Count operations	• Decrement • When the timer underflows, it reloads the reload register content before the count continues (when timer RB underflows, the content of timer RB primary reload register is reloaded).
Division ratio	1/(n+1)(m+1) n: Value set in TRBPRE register, m: Value set in TRBPR register
Count start condition	1 (count starts) is written to the TSTART bit in the TRBCR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRBCR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRBCR register.
Interrupt request generation timing	When timer RB underflows [timer RB interrupt].
TRBO pin function	Programmable I/O port
$\overline{\text{INT0}}$ pin function	Programmable I/O port or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read out by reading registers TRBPR and TRBPRE.
Write to timer	• When registers TRBPRE and TRBPR are written while the count is stopped, values are written to both the reload register and counter. • When registers TRBPRE and TRBPR are written during count operation: If the TWRC bit in the TRBMR register is set to 0, the value is written to both the reload register and the counter. If the TWRC bit is set to 1, the value is written to the reload register only. (Refer to **19.3.2 Timer Write Control during Count Operation**.)

19.3.1 Timer RB I/O Control Register (TRBIOC) in Timer Mode

Address 010Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

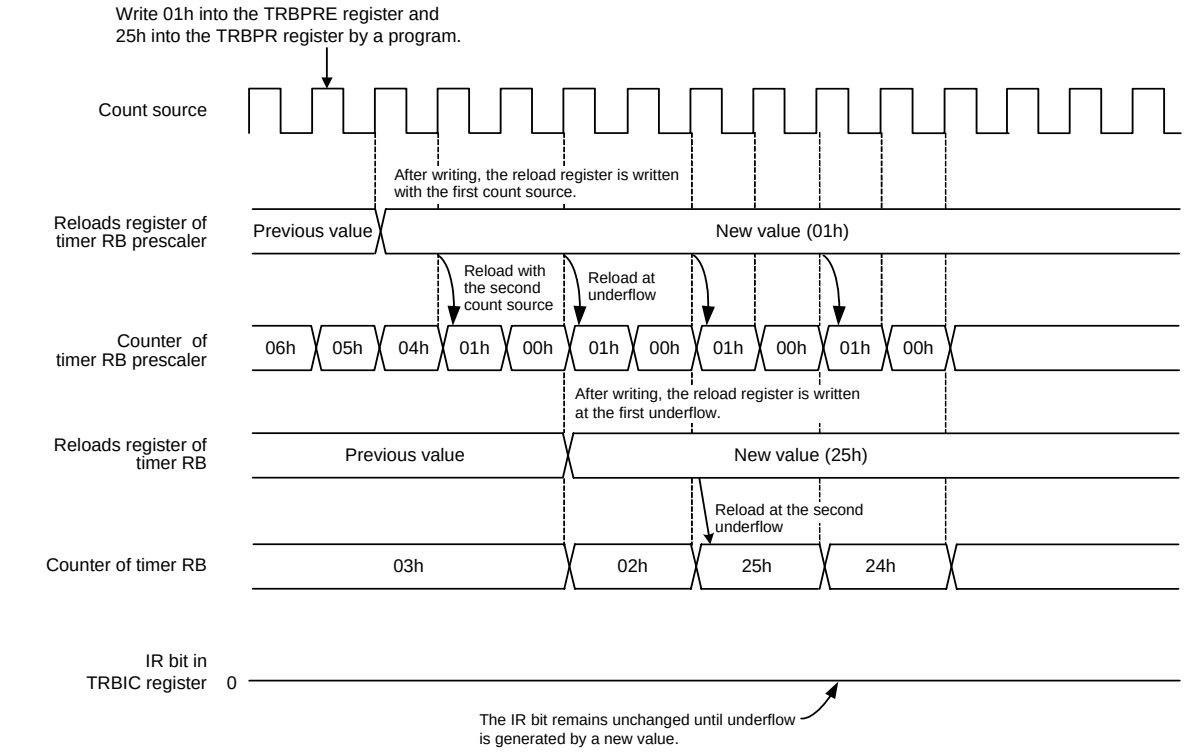
Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RB output level select bit	Set to 0 in timer mode.	R/W
b1	TOCNT	Timer RB output switch bit		R/W
b2	INOSTG	One-shot trigger control bit		R/W
b3	INOSEG	One-shot trigger polarity select bit		R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

19.3.2 Timer Write Control during Count Operation

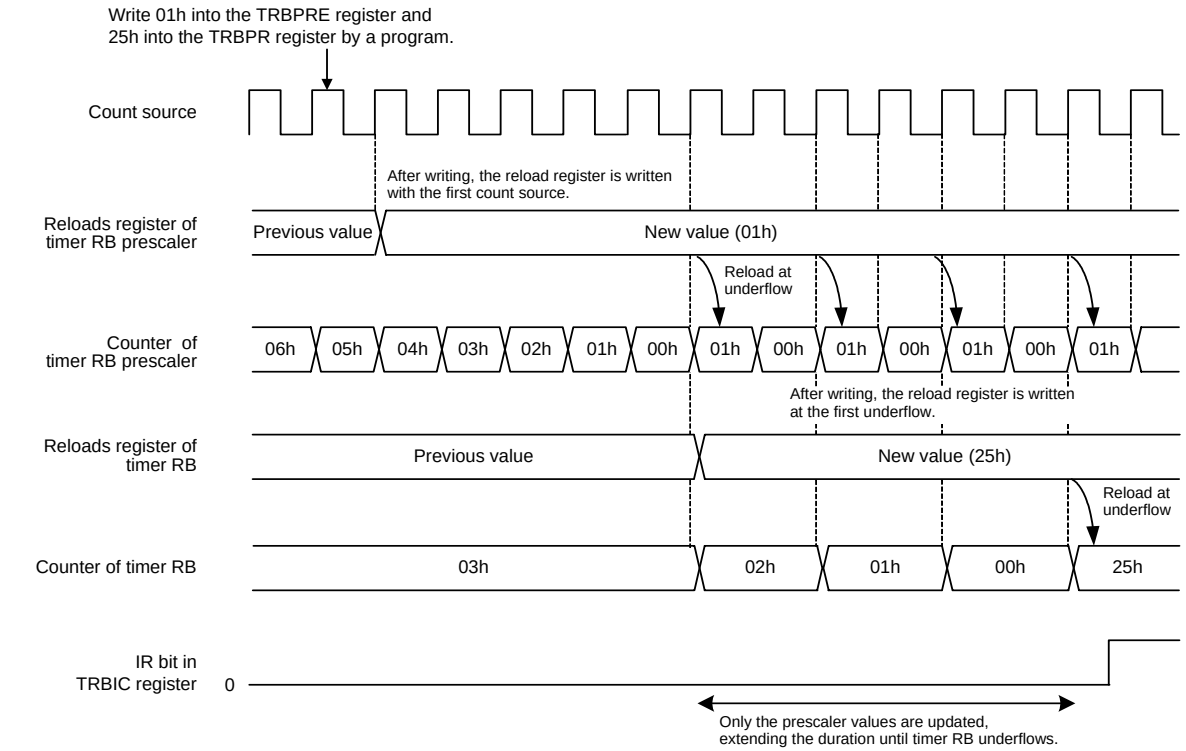
Timer RB has a prescaler and a timer (which counts the prescaler underflows). The prescaler and timer each consist of a reload register and a counter. In timer mode, the TWRC bit in the TRBMR register can be used to select whether writing to the prescaler or timer during count operation is performed to both the reload register and counter or only to the reload register.

However, values are transferred from the reload register to the counter of the prescaler in synchronization with the count source. In addition, values are transferred from the reload register to the counter of the timer in synchronization with prescaler underflows. Therefore, even if the TWRC bit is set for writing to both the reload register and counter, the counter value is not updated immediately after the WRITE instruction is executed. If the TWRC bit is set for writing to the reload register only, the synchronization of the writing will be shifted when the prescaler value changes. Figure 19.2 shows an Operating Example of Timer RB when Counter Value is Rewritten during Count Operation.

When the TWRC bit is set to 0 (write to reload register and counter)



When the TWRC bit is set to 1 (write to reload register only)



The above applies under the following condition:
Both the TSTART and TCSTF bits in the TRBCR register are set to 1 (during count operation).

Figure 19.2 Operating Example of Timer RB when Counter Value is Rewritten during Count Operation

19.4 Programmable Waveform Generation Mode

In programmable waveform generation mode, the signal output from the TRBO pin is inverted each time the counter underflows, while the values in registers TRBPR and TRBSC are counted alternately (refer to **Table 19.3**). Counting starts by counting the setting value of the TRBPR register. The TRBOCR register is unused in this mode. Figure 19.3 shows an Operating Example in Timer RB in Programmable Waveform Generation Mode.

Table 19.3 Programmable Waveform Generation Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RA underflow
Count operations	• Decrement • When the timer underflows, it reloads the contents of the primary reload and secondary reload registers alternately before the count continues.
Width and period of output waveform	Primary period: (n+1)(m+1)/fi Secondary period: (n+1)(p+1)/fi Period: (n+1){(m+1)+(p+1)}/fi fi: Frequency of count source n: Value set in TRBPRE register m: Value set in TRBPR register p: Value set in TRBSC register
Count start condition	1 (count starts) is written to the TSTART bit in the TRBCR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRBCR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRBCR register.
Interrupt request generation timing	In half a cycle of the count source, after timer RB underflows during the secondary period (at the same time as the TRBO output change) [timer RB interrupt]
TRBO pin function	Programmable output port or pulse output
$\overline{\text{INT0}}$ pin function	Programmable I/O port or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read out by reading registers TRBPR and TRBPRE (1).
Write to timer	• When registers TRBPRE, TRBSC, and TRBPR are written while the count is stopped, values are written to both the reload register and counter. • When registers TRBPRE, TRBSC, and TRBPR are written to during count operation, values are written to the reload registers only. (2)
Selectable function	• Output level select function The output level during primary and secondary periods is selected by the TOPL bit in the TRBIOC register.

Notes:
1. Even when the secondary period is being counted, the TRBPR register may be read.
2. The set values are reflected in the waveform output beginning with the following primary period after writing to the TRBPR register.

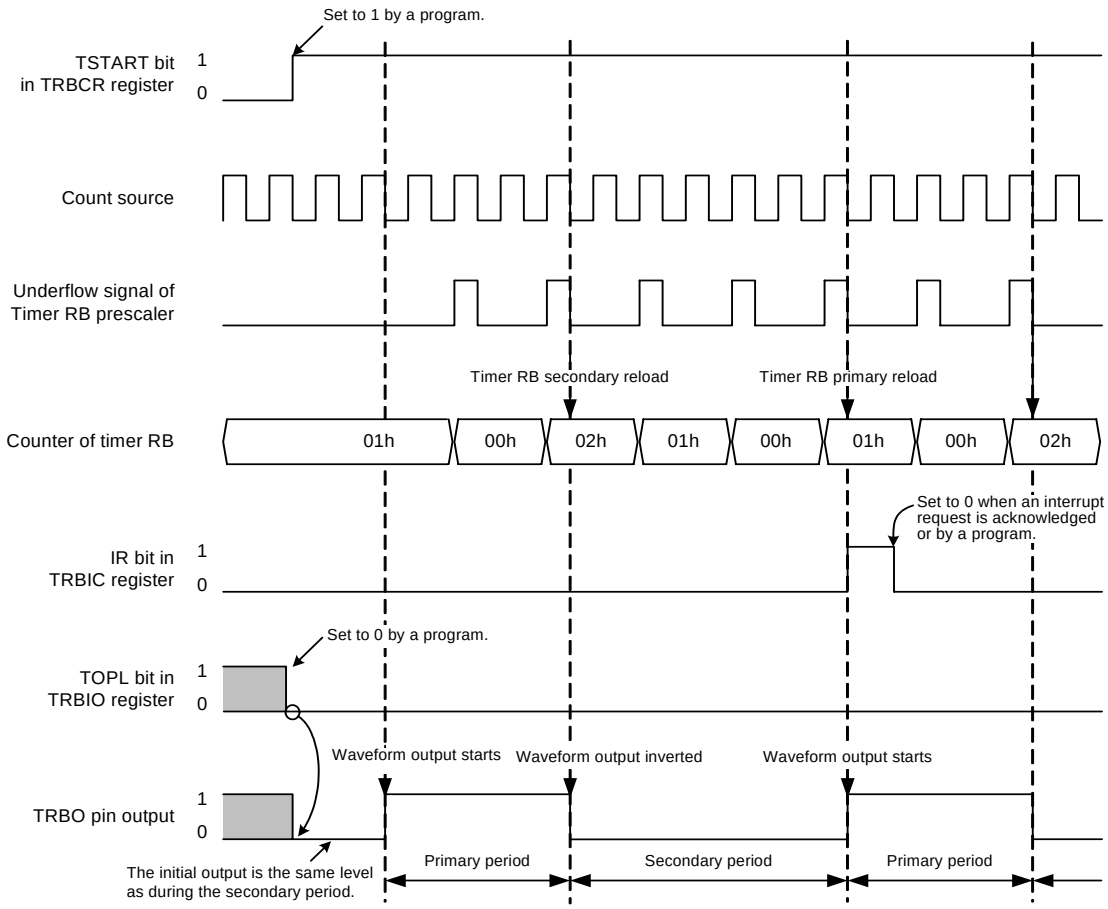
19.4.1 Timer RB I/O Control Register (TRBIOC) in Programmable Waveform Generation Mode

Address 010Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RB output level select bit	0: High-level output for the primary period, low-level output for the secondary period Low-level output when the timer is stopped 1: Low-level output for the primary period, high-level output for the secondary period High-level output when the timer is stopped	R/W
b1	TOCNT	Timer RB output switch bit	0: Timer RB waveform is output 1: P11_6 port latch value is output	R/W
b2	INOSTG	One-shot trigger control bit	Set to 0 in programmable waveform generation mode.	R/W
b3	INOSEG	One-shot trigger polarity select bit		R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

19.4.2 Operating Example



The above applies under the following conditions:

TRBPRE = 01h, TRBPR = 01h, TRBSC = 02h
TOCNT in TRBIOC register = 0 (timer RB waveform output from the TRBO pin)

Figure 19.3 Operating Example in Timer RB in Programmable Waveform Generation Mode

19.5 Programmable One-shot Generation Mode

In programmable one-shot generation mode, a one-shot pulse is output from the TRBO pin by a program or an external trigger input (input to the $\overline{\text{INT0}}$ pin) (refer to **Table 19.4**). When a trigger is generated, the timer starts operating from the point only once for a given period equal to the set value in the TRBPR register. The TRBSC register is not used in this mode.
Figure 19.4 shows an Operating Example in Programmable One-Shot Generation Mode.

Table 19.4 Programmable One-Shot Generation Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RA underflow
Count operations	• The setting value of the TRBPR register is decremented. • When the timer underflows, it reloads the contents of the reload register before the count completes and the TOSSTF bit is set to 0 (one-shot stops). • When the count stops, the timer reloads the content of the reload register before it stops.
One-shot pulse output time	(n+1)(m+1)/fi fi: Frequency of count source n: Value set in TRBPRE register, m: Value set in TRBPR register
Count start conditions	• The TSTART bit in the TRBCR register is set to 1 (count starts) and the next trigger is generated. • 1 (one-shot starts) is written to the TOSST bit in the TRBOCR register. • Trigger input to the $\overline{\text{INT0}}$ pin
Count stop conditions	• When reloading completes after timer RB underflows during the primary period • 1 (one-shot stops) is written to the TOSSP bit in the TRBOCR register. • 0 (count stops) is written to the TSTART bit in the TRBCR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRBCR register.
Interrupt request generation timing	In half a cycle of the count source, after the timer underflows (at the same time as the waveform output from the TRBO pin ends) [timer RB interrupt]
TRBP pin function	Pulse output
$\overline{\text{INT0}}$ pin functions	• When the INOSTG bit in the TRBIOC register is set to 0 ($\overline{\text{INT0}}$ one-shot trigger disabled): programmable I/O port or $\overline{\text{INT0}}$ interrupt input • When the INOSTG bit in the TRBIOC register is set to 1 ($\overline{\text{INT0}}$ one-shot trigger enabled): external trigger ($\overline{\text{INT0}}$ interrupt input)
Read from timer	The count value can be read out by reading registers TRBPR and TRBPRE.
Write to timer	• When registers TRBPRE and TRBPR are written while the count is stopped, values are written to both the reload register and counter. • When registers TRBPRE and TRBPR are written during count operation, values are written to the reload register only (1).
Selectable functions	• Output level select function The output level of the one-shot pulse waveform is selected by the TOPL bit in the TRBIOC register. • One-shot trigger select function Refer to **19.5.3 One-Shot Trigger Selection**.

Note:
1. The set value is reflected at the following one-shot pulse after writing to the TRBPR register.

19.5.1 Timer RB I/O Control Register (TRBIOC) in Programmable One-Shot Generation Mode

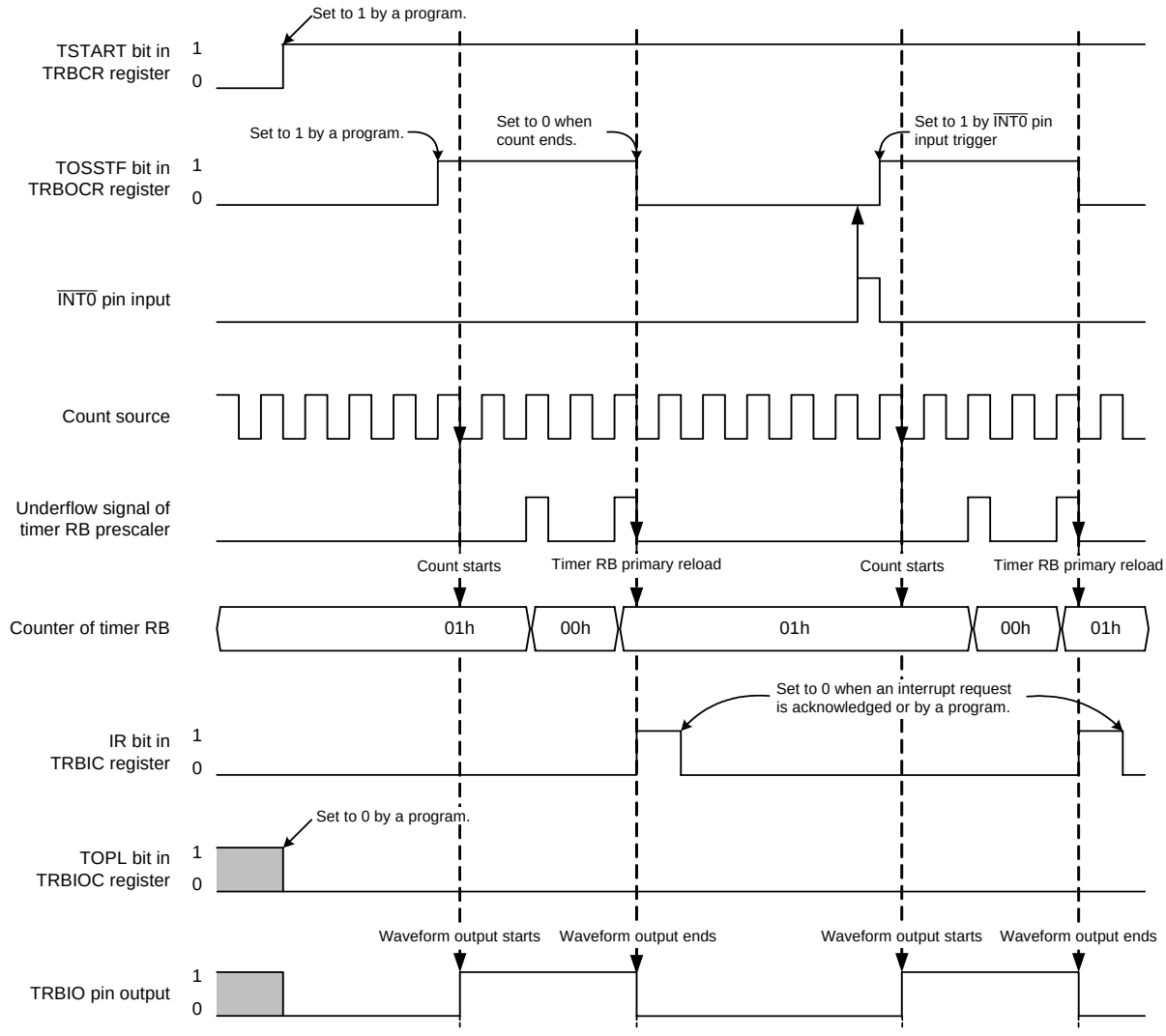
Address 010Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RB output level select bit	0: High-level output of a one-shot pulse, low-level output when the timer is stopped 1: Low-level output of a one-shot pulse, high-level output when the timer is stopped	R/W
b1	TOCNT	Timer RB output switch bit	Set to 0 in programmable one-shot generation mode.	R/W
b2	INOSTG	One-shot trigger control bit (1)	0: $\overline{\text{INT0}}$ pin one-shot trigger disabled 1: $\overline{\text{INT0}}$ pin one-shot trigger enabled	R/W
b3	INOSEG	One-shot trigger polarity select bit (1)	0: Falling edge trigger 1: Rising edge trigger	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

Note:
1. Refer to **19.5.3 One-Shot Trigger Selection**.

19.5.2 Operating Example



The above applies under the following conditions:

TRBPRE = 01h, TRBPR = 01h
TOPL in TRBIOC register = 0, TOCNT = 0
INOSTG = 1 (INT0 one-shot trigger enabled)
INOSEG = 1 (edge trigger at the rising edge)

Figure 19.4 Operating Example in Programmable One-Shot Generation Mode

19.5.3 One-Shot Trigger Selection

In programmable one-shot generation mode and programmable wait one-shot generation mode, operation starts when a one-shot trigger is generated while the TCSTF bit in the TRBCR register is set to 1 (count starts).
A one-shot trigger can be generated by either of the following causes:

- 1 is written to the TOSST bit in the TRBOCR register by a program.
- Trigger input from the $\overline{\text{INT0}}$ pin.

When a one-shot trigger occurs, the TOSSTF bit in the TRBOCR register is set to 1 (one-shot operation in progress) after one or two cycles of the count source have elapsed. Then, in programmable one-shot generation mode, count operation begins and one-shot waveform output starts. (In programmable wait one-shot generation mode, count operation starts for the wait period.) If a one-shot trigger occurs while the TOSSTF bit is set to 1, no retriggering occurs.

To use trigger input from the $\overline{\text{INT0}}$ pin, input the trigger after making the following settings:

- Set the PD4_5 bit in the PD4 register to 0 (input port).
- Select the $\overline{\text{INT0}}$ digital filter with bits INT0F0 and INT0F1 in the INTF register.
- Select both edges or one edge with the INT0PL bit in INTEN register. If one edge is selected, further select falling or rising edge with the INOSEG bit in TRBIOC register.
- Set the INT0EN bit in the INTEN register to 0 (enabled).
- After completing the above, set the INOSTG bit in the TRBIOC register to 1 ($\overline{\text{INT}}$ pin one-shot trigger enabled).

Note the following points with regard to generating interrupt requests by trigger input from the $\overline{\text{INT0}}$ pin.

- Processing to handle the interrupts is required. Refer to **12. Interrupts**, for details.
- If one edge is selected, use the POL bit in the INT0IC register to select falling or rising edge. (The INOSEG bit in the TRBIOC register does not affect $\overline{\text{INT0}}$ interrupts).
- If a one-shot trigger occurs while the TOSSTF bit is set to 1, timer RB operation is not affected, but the value of the IR bit in the INT0IC register changes.

19.6 Programmable Wait One-Shot Generation Mode

In programmable wait one-shot generation mode, a one-shot pulse is output from the TRBO pin by a program or an external trigger input (input to the $\overline{\text{INT0}}$ pin) (refer to **Table 19.5**). When a trigger is generated from that point, the timer outputs a pulse only once for a given length of time equal to the setting value of the TRBSC register after waiting for a given length of time equal to the setting value of the TRBPR register.
Figure 19.5 shows an Operating Example in Programmable Wait One-Shot Generation Mode.

Table 19.5 Programmable Wait One-Shot Generation Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RA underflow
Count operations	• The setting value of the timer RB primary is decremented. • When a count of the timer RB primary underflows, the timer reloads the contents of timer RB secondary before the count continues. • When a count of the timer RB secondary underflows, the timer reloads the contents of timer RB primary before the count completes and the TOSSTF bit is set to 0 (one-shot stops). • When the count stops, the timer reloads the content of the reload register before it stops.
Wait time	(n+1)(m+1)/fi fi: Frequency of count source n: Value set in TRBPRE register, m: Value set in TRBPR register
One-shot pulse output time	(n+1)(p+1)/fi fi: Frequency of count source n: Value set in TRBPRE register, p: Value set in TRBSC register
Count start conditions	• The TSTART bit in the TRBCR register is set to 1 (count starts) and the next trigger is generated. • 1 (one-shot starts) is written to the TOSST bit in the TRBOCR register. • Trigger input to the $\overline{\text{INT0}}$ pin
Count stop conditions	• When reloading completes after timer RB underflows during the secondary period. • 1 (one-shot stops) is written to the TOSSP bit in the TRBOCR register. • 0 (count stops) is written to the TSTART bit in the TRBCR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRBCR register.
Interrupt request generation timing	In half a cycle of the count source after timer RB underflows during secondary period (at the same time as the waveform output from the TRBO pin ends) [timer RB interrupt].
TRBO pin function	Pulse output
$\overline{\text{INT0}}$ pin functions	• When the INOSTG bit in the TRBIOC register is set to 0 ($\overline{\text{INT0}}$ one-shot trigger disabled): programmable I/O port or $\overline{\text{INT0}}$ interrupt input • When the INOSTG bit in the TRBIOC register is set to 1 ($\overline{\text{INT0}}$ one-shot trigger enabled): external trigger ($\overline{\text{INT0}}$ interrupt input)
Read from timer	The count value can be read out by reading registers TRBPR and TRBPRE.
Write to timer	• When registers TRBPRE, TRBSC, and TRBPR are written while the count is stopped, values are written to both the reload register and counter. • When registers TRBPRE, TRBSC, and TRBPR are written during count operation, values are written to the reload registers only. (1)
Selectable functions	• Output level select function The output level of the one-shot pulse waveform is selected by the TOPL bit in the TRBIOC register. • One-shot trigger select function Refer to **19.5.3 One-Shot Trigger Selection**.

Note:
1. The set value is reflected at the following one-shot pulse after writing to registers TRBSC and TRBPR.

19.6.1 Timer RB I/O Control Register (TRBIOC) in Programmable Wait One-Shot Generation Mode

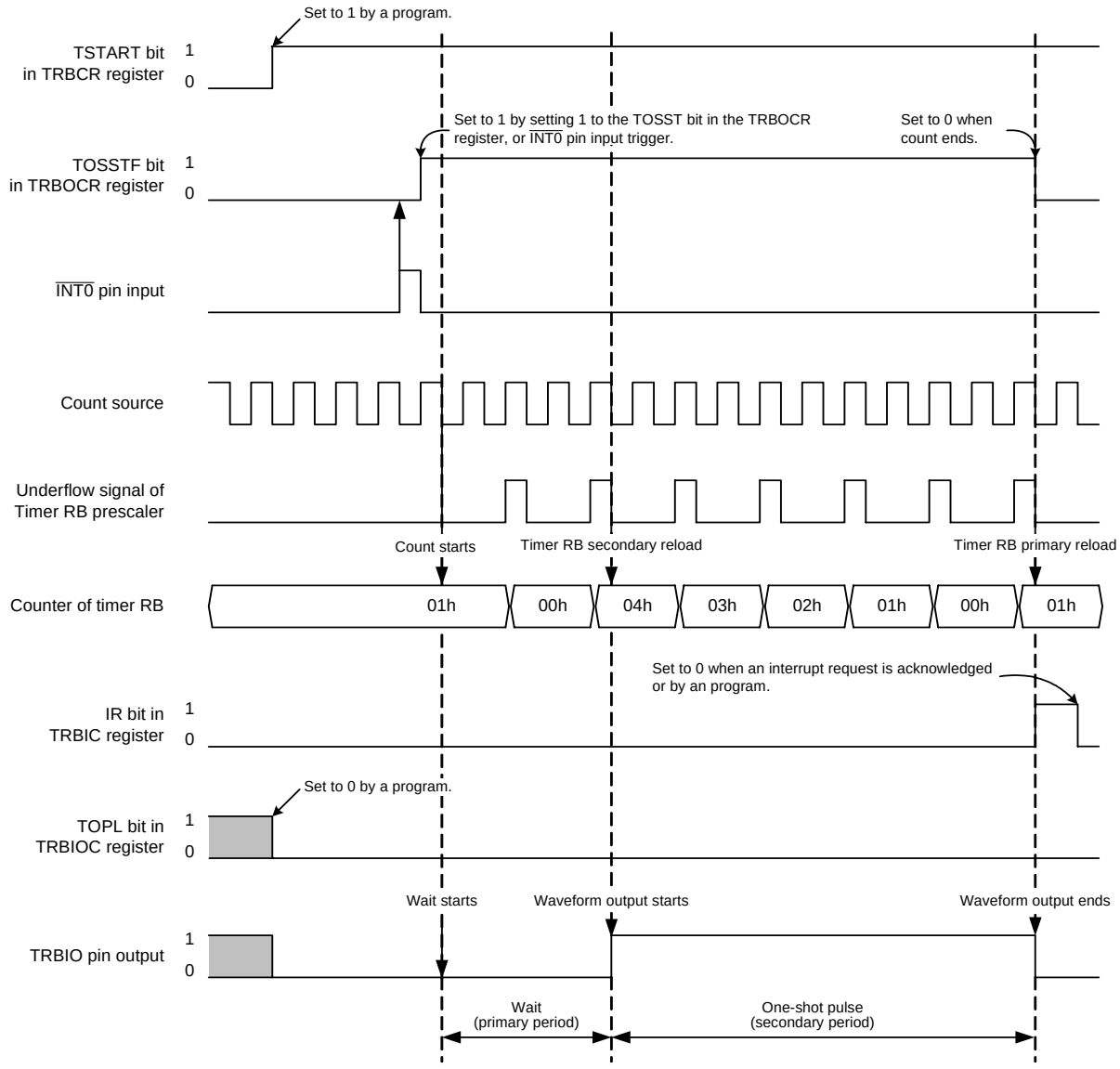
Address 010Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RB output level select bit	0: High-level output of a one-shot pulse, low-level output when the timer stops or during wait 1: Low-level output of a one-shot pulse, low-level output when the timer stops or during wait	R/W
b1	TOCNT	Timer RB output switch bit	Set to 0 in programmable wait one-shot generation mode.	R/W
b2	INOSTG	One-shot trigger control bit (1)	0: $\overline{\text{INT0}}$ pin one-shot trigger disabled 1: $\overline{\text{INT0}}$ pin one-shot trigger enabled	R/W
b3	INOSEG	One-shot trigger polarity select bit (1)	0: Falling edge trigger 1: Rising edge trigger	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

Note:
1. Refer to **19.5.3 One-Shot Trigger Selection**.

19.6.2 Operating Example



The above applies under the following conditions:

TRBPRE = 01h, TRBPR = 01h, TRBSC = 04h
INOSTG = 1 (INT0 one-shot trigger enabled)
INOSEG = 1 (edge trigger at the rising edge)

Figure 19.5 Operating Example in Programmable Wait One-Shot Generation Mode

19.7 Notes on Timer RB

- Timer RB stops counting after a reset. Set the values in the timer RB and timer RB prescalers before the count starts.
- Even if the prescaler and timer RB is read out in 16-bit units, these registers are read 1 byte at a time in the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In programmable one-shot generation mode and programmable wait one-shot generation mode, when setting the TSTART bit in the TRBCR register to 0 (count stops) or setting the TOSSP bit in the TRBOCR register to 1 (one-shot stops), the timer reloads the value of reload register and stops. Therefore, in programmable one-shot generation mode and programmable wait one-shot generation mode, read the timer count value before the timer stops.
- The TCSTF bit remains 0 (count stops) for one or two cycles of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.
  During this time, do not access registers associated with timer RB (1) other than the TCSTF bit. Timer RB starts counting at the first active edge of the count source after the TCSTF bit is set to 1 (during count operation).
  The TCSTF bit remains 1 for one or two cycles of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RB counting is stopped when the TCSTF bit is set to 0.
  During this time, do not access registers associated with timer RB (1) other than the TCSTF bit.

  Note:
  1. Registers associated with timer RB:
     TRBCR, TRBOCR, TRBIOC, TRBMR, TRBPRE, TRBSC, and TRBPR

- When the TSTOP bit in the TRBCR register is set to 1 during timer operation, timer RB stops immediately.
- When 1 is written to the TOSST or TOSSP bit in the TRBOCR register, the value of the TOSSTF bit changes after one or two cycles of the count source have elapsed. When 1 is written to the TOSSP bit during the period between when 1 is written to the TOSST bit and when the TOSSTF bit is set to 1, the TOSSTF bit may be set to either 0 or 1 depending on the content state. Likewise, when 1 is written to the TOSST bit during the period between when 1 is written to the TOSSP bit and when the TOSSTF bit is set to 0, the TOSSTF bit may be set to either 0 or 1.

19.7.1 Timer Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

19.7.2 Programmable Waveform Generation Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

19.7.3 Programmable One-Shot Generation Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following:

- When the TRBPRE register is written continuously during count operation, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously during count operation, allow three or more cycles of the prescaler underflow for each write interval.

19.7.4 Programmable Wait One-shot Generation Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

20. Timer RC

Timer RC is a 16-bit timer with four I/O pins.

20.1 Introduction

Timer RC uses either f1 or fOCO40M as its operating clock. Table 20.1 lists the Timer RC Operating Clocks.

Table 20.1 Timer RC Operating Clocks

Condition	Timer RC Operating Clock
The count source is f1, f2, f4, f8, f32, or TRCCLK input. (Bits TCK2 to TCK0 in the TRCCR1 register are set to 000b to 101b.)	f1
The count source is fOCO40M. (Bits TCK2 to TCK0 in the TRCCR1 register are set to 110b.)	fOCO40M

Table 20.2 lists the Timer RC Pin Configuration. Figure 20.1 shows the Timer RC Block Diagram.

Timer RC supports the following three modes:

- Timer mode
  - Input capture function — The counter value is captured to a register, using an external signal as the trigger.
  - Output compare function — A match between the values of a counter and a register is detected. (Pin output can be changed at detection.)

The following two modes use the output compare function:

- PWM mode — Pulses of a given width are output continuously.
- PWM2 mode — A one-shot waveform or PWM waveform is output following the trigger after the wait time has elapsed.

For the input capture function, the output compare function, and in PWM mode, settings may be selected independently for each pin.
In PWM2 mode, waveforms are output based on a combination of the counter or the register.

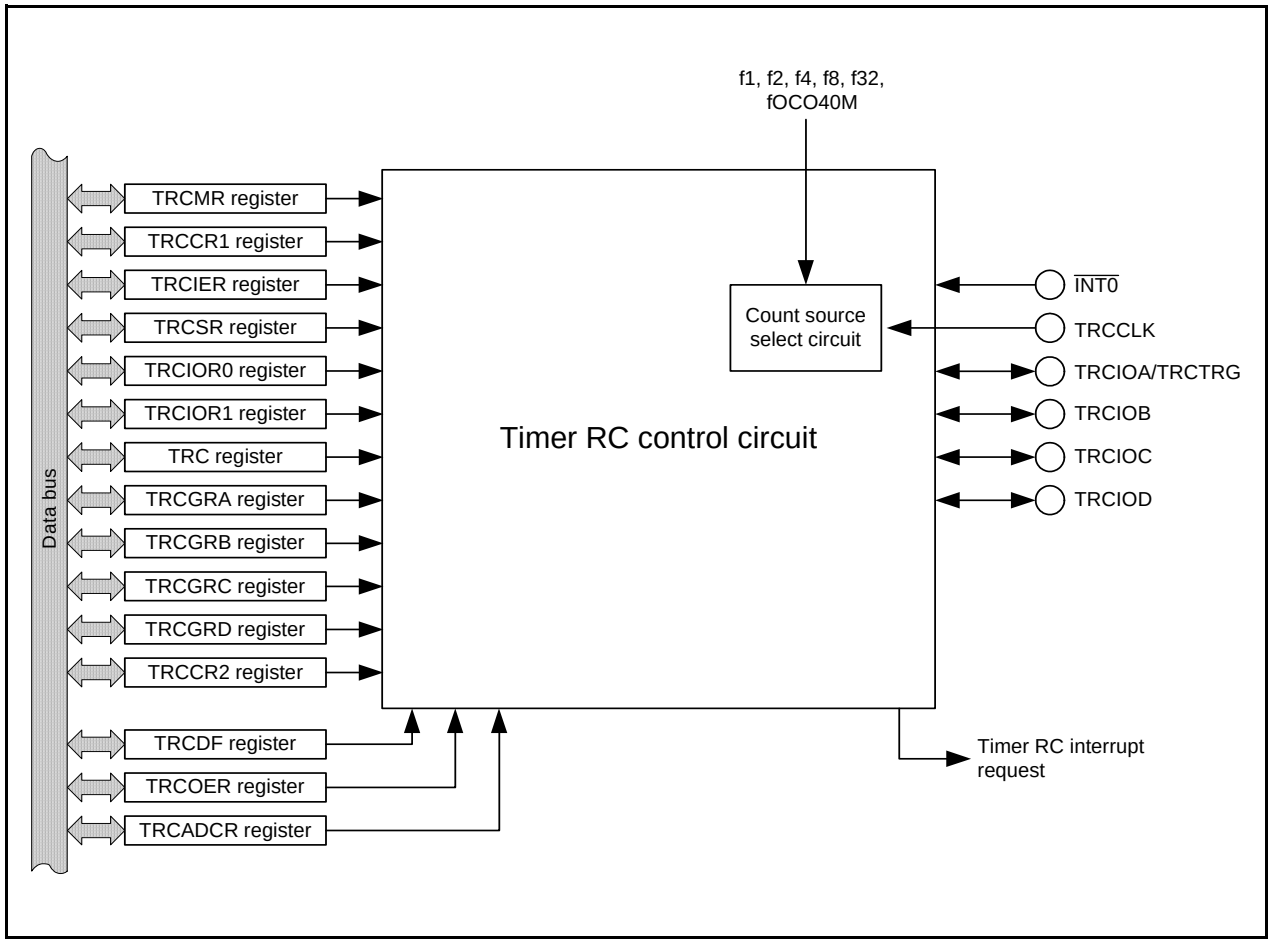


Figure 20.1 Timer RC Block Diagram

Table 20.2 Timer RC Pin Configuration

Pin Name	Assigned Pin	I/O	Function
TRCIOA	P4_4	I/O	Function differs according to the mode. Refer to descriptions of individual modes for details.
TRCIOB	P4_5, P4_6, or P4_7		
TRCIOC	P4_6		
TRCIOD	P4_7		
TRCCLK	P4_3	Input	External clock input
TRCTRG	P3_7, P4_3, or P4_4	Input	PWM2 mode external trigger input

20.2 Registers

Table 20.3 lists the Registers Associated with Timer RC.

Table 20.3 Registers Associated with Timer RC

Address	Symbol	Mode				Related Information
		Timer		PWM	PWM2	
		Input Capture Function	Output Compare Function			
0008h	MSTCR	Valid	Valid	Valid	Valid	20.2.1 Module Standby Control Register (MSTCR)
0120h	TRCMR	Valid	Valid	Valid	Valid	20.2.2 Timer RC Mode Register (TRCMR)
0121h	TRCCR1	Valid	Valid	Valid	Valid	Timer RC control register 1 20.2.3 Timer RC Control Register 1 (TRCCR1) 20.5.1 Timer RC Control Register 1 (TRCCR1) in Timer Mode (Output Compare Function) 20.6.1 Timer RC Control Register 1 (TRCCR1) in PWM Mode 20.7.1 Timer RC Control Register 1 (TRCCR1) in PWM2 Mode
0122h	TRCIER	Valid	Valid	Valid	Valid	20.2.4 Timer RC Interrupt Enable Register (TRCIER)
0123h	TRCSR	Valid	Valid	Valid	Valid	20.2.5 Timer RC Status Register (TRCSR)
0124h	TRCIOR0	Valid	Valid	–	–	Timer RC I/O control register 0, timer RC I/O control register 1 20.2.6 Timer RC I/O Control Register 0 (TRCIOR0) 20.2.7 Timer RC I/O Control Register 1 (TRCIOR1) 20.4.1 Timer RC I/O Control Register 0 (TRCIOR0) in Timer Mode (Input Capture Function) 20.4.2 Timer RC I/O Control Register 1 (TRCIOR1) in Timer Mode (Input Capture Function) 20.5.2 Timer RC I/O Control Register 0 (TRCIOR0) in Timer Mode (Output Compare Function) 20.5.3 Timer RC I/O Control Register 1 (TRCIOR1) in Timer Mode (Output Compare Function)
0125h	TRCIOR1					
0126h 0127h	TRC	Valid	Valid	Valid	Valid	20.2.8 Timer RC Counter (TRC)
0128h 0129h	TRCGRA	Valid	Valid	Valid	Valid	20.2.9 Timer RC General Registers A, B, C, and D (TRCGRA, TRCGRB, TRCGRC, TRCGRD)
012Ah 012Bh	TRCGRB					
012Ch 012Dh	TRCGRC					
012Eh 012Fh	TRCGRD					
0130h	TRCCR2	–	–	–	Valid	20.2.10 Timer RC Control Register 2 (TRCCR2)
0131h	TRCDF	Valid	–	–	Valid	20.2.11 Timer RC Digital Filter Function Select Register (TRCDF)
0132h	TRCOER	–	Valid	Valid	Valid	20.2.12 Timer RC Output Master Enable Register (TRCOER)
0133h	TRCADCR	–	Valid	Valid	Valid	20.2.13 Timer RC Trigger Control Register (TRCADCR)
0181h	TRBRCSR	Valid	Valid	Valid	Valid	20.2.14 Timer RB/RC Pin Select Register (TRBRCSR)
0182h	TRCPSR0	Valid	Valid	Valid	Valid	20.2.15 Timer RC Pin Select Register 0 (TRCPSR0)
0183h	TRCPSR1	Valid	Valid	Valid	Valid	20.2.16 Timer RC Pin Select Register 1 (TRCPSR1)

–: Invalid

20.2.1 Module Standby Control Register (MSTCR)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	MSTTRG	MSTTRC	MSTTRD	MSTIIC	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	MSTIIC	SSU, I2C bus standby bit	0: Active 1: Standby (1)	R/W
b4	MSTTRD	Timer RD standby bit	0: Active 1: Standby (2)	R/W
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (3)	R/W
b6	MSTTRG	Timer RG standby bit	0: Active 1: Standby (4)	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. When the MSTIIC bit is set to 1 (standby), any access to the SSU or the I2C bus associated registers (addresses 0193h to 019Dh) is disabled.
2. When the MSTTRD bit is set to 1 (standby), any access to the timer RD associated registers (addresses 0135h to 015Fh) is disabled.
3. When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0133h) is disabled.
4. When the MSTTRG bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0170h to 017Fh) is disabled.

20.2.2 Timer RC Mode Register (TRCMR)

Address 0120h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TSTART	—	BFD	BFC	PWM2	PWMD	PWMC	PWMB
After Reset	0	1	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PWMB	PWM mode of TRCIOB select bit (1)	0: Timer mode 1: PWM mode	R/W
b1	PWMC	PWM mode of TRCIOC select bit (1)	0: Timer mode 1: PWM mode	R/W
b2	PWMD	PWM mode of TRCIOD select bit (1)	0: Timer mode 1: PWM mode	R/W
b3	PWM2	PWM2 mode select bit	0: PWM 2 mode 1: Timer mode or PWM mode	R/W
b4	BFC	TRCGRC register function select bit (2)	0: General register 1: Buffer register of TRCGRA register	R/W
b5	BFD	TRCGRD register function select bit	0: General register 1: Buffer register of TRCGRB register	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b7	TSTART	TRC count start bit	0: Count stops 1: Count starts	R/W

Notes:
1. These bits are enabled when the PWM2 bit is set to 1 (timer mode or PWM mode).
2. Set the BFC bit to 0 (general register) in PWM2 mode.

For notes on the TRCMR register in PWM2 mode, refer to **20.9.6 TRCMR Register in PWM2 Mode**.

20.2.3 Timer RC Control Register 1 (TRCCR1)

Address 0121h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR	TCK2	TCK1	TCK0	TOD	TOC	TOB	TOA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA	TRCIOA output level select bit (1)	Function varies according to the operating mode (function).	R/W
b1	TOB	TRCIOB output level select bit (1)		R/W
b2	TOC	TRCIOC output level select bit (1)		R/W
b3	TOD	TRCIOD output level select bit (1)		R/W
b4	TCK0	Count source select bit (1)	b6 b5 b4 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRCCLK input rising edge 1 1 0: fOCO40M 1 1 1: fOCO-F (2)	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	CCLR	TRC counter clear select bit	0: Clear disabled (free-running operation) 1: TRC counter cleared by input capture or by compare match with the TRCGRA register	R/W

Note:
1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).
2. To select fOCO-F, set it to the clock frequency higher than the CPU clock frequency.

20.2.4 Timer RC Interrupt Enable Register (TRCIER)

Address 0122h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	OVIE	—	—	—	IMIED	IMIEC	IMIEB	IMIEA
After Reset	0	1	1	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input-capture/compare-match interrupt enable bit A	0: Interrupt (IMIA) by IMFA bit disabled 1: Interrupt (IMIA) by IMFA bit enabled	R/W
b1	IMIEB	Input-capture/compare-match interrupt enable bit B	0: Interrupt (IMIB) by IMFB bit disabled 1: Interrupt (IMIB) by IMFB bit enabled	R/W
b2	IMIEC	Input-capture/compare-match interrupt enable bit C	0: Interrupt (IMIC) by IMFC bit disabled 1: Interrupt (IMIC) by IMFC bit enabled	R/W
b3	IMIED	Input-capture/compare-match interrupt enable bit D	0: Interrupt (IMID) by IMFD bit disabled 1: Interrupt (IMID) by IMFD bit enabled	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	OVIE	Overflow interrupt enable bit	0: Interrupt (OVI) by OVF bit disabled 1: Interrupt (OVI) by OVF bit enabled	R/W

20.2.5 Timer RC Status Register (TRCSR)

Address 0123h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	OVF	—	—	—	IMFD	IMFC	IMFB	IMFA
After Reset	0	1	1	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input-capture/compare-match flag A	[Condition for setting to 0] Write 0 after reading. (1) [Condition for setting to 1] Refer to **Table 20.4 Conditions for Setting Bit of Each Flag to 1**.	R/W
b1	IMFB	Input-capture/compare-match flag B		R/W
b2	IMFC	Input-capture/compare-match flag C		R/W
b3	IMFD	Input-capture/compare-match flag D		R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	OVF	Overflow flag	[Condition for setting to 0] Write 0 after reading. (1) [Condition for setting to 1] Refer to **Table 20.4 Conditions for Setting Bit of Each Flag to 1**.	R/W

Note:
1. The results of writing to these bits are as follows:
   - The bit is set to 0 when it is first read as 1 and then 0 is written to it.
   - The bit remains unchanged even if it is first read as 0 and then 0 is written to it. (The bit's value remains 1 even if it is set to 1 from 0 after being read as 0 and having 0 written to it.)
   - The bit's value remains unchanged if 1 is written to it.

Table 20.4 Conditions for Setting Bit of Each Flag to 1

Bit Symbol	Timer Mode		PWM Mode	PWM2 Mode
	Input capture Function	Output Compare Function		
IMFA	TRCIOA pin input edge (1)	When the values of registers TRC and TRCGRA match.		
IMFB	TRCIOB pin input edge (1)	When the values of registers TRC and TRCGRB match.		
IMFC	TRCIOC pin input edge (1)	When the values of registers TRC and TRCGRC match. (2)		
IMFD	TRCIOD pin input edge (1)	When the values of registers TRC and TRCGRD match. (2)		
OVF	When the TRC register overflows.			

Notes:
1. Edge selected by bits IOj0 and IOj1 (j = A, B, C, or D) in registers TRCIOR0 and TRCIOR1.
2. Includes the condition that bits BFC and BFD are set to 1 (buffer registers of registers TRCGRA and TRCGRB).

20.2.6 Timer RC I/O Control Register 0 (TRCIOR0)

Address 0124h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	IOB2	IOB1	IOB0	—	IOA2	IOA1	IOA0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRCGRA control bit	Function varies according to the operating mode (function).	R/W
b1	IOA1			R/W
b2	IOA2	TRCGRA mode select bit (1)	0: Output compare function 1: Input capture function	R/W
b3	—	Reserved bit	Set to 1.	R/W
b4	IOB0	TRCGRB control bit	Function varies according to the operating mode (function).	R/W
b5	IOB1			R/W
b6	IOB2	TRCGRB mode select bit (2)	0: Output compare function 1: Input capture function	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

The TRCIOR0 register is enabled in timer mode. It is disabled in PWM mode and PWM2 mode.

20.2.7 Timer RC I/O Control Register 1 (TRCIOR1)

Address 0125h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOC0	TRCGRC control bit	Function varies according to the operating mode (function).	R/W
b1	IOC1			R/W
b2	IOC2	TRCGRC mode select bit (1)	0: Output compare function 1: Input capture function	R/W
b3	IOC3	TRCGRC register function select bit	0: TRCIOA output register 1: General register or buffer register	R/W
b4	IOD0	TRCGRD control bit	Function varies according to the operating mode (function).	R/W
b5	IOD1			R/W
b6	IOD2	TRCGRD mode select bit (2)	0: Output compare function 1: Input capture function	R/W
b7	IOD3	TRCGRD register function select bit	0: TRCIOB output register 1: General register or buffer register	R/W

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

The TRCIOR1 register is enabled in timer mode. It is disabled in PWM mode and PWM2 mode.

20.2.8 Timer RC Counter (TRC)

Address 0127h to 0126h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	Counts a count source. Count operation is increment. When an overflow occurs, the OVF bit in the TRCSR register is set to 1.	0000h to FFFFh	R/W

Access the TRC register in 16-bit units. Do not access it in 8-bit units.

20.2.9 Timer RC General Registers A, B, C, and D (TRCGRA, TRCGRB, TRCGRC, TRCGRD)

Address 0129h to 0128h (TRCGRA), 012Bh to 012Ah (TRCGRB),
012Dh to 012Ch (TRCGRC), 012Fh to 012Eh (TRCGRD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b15 to b0	Function varies according to the operating mode.	R/W

Access registers TRCGRA to TRCGRD in 16-bit units. Do not access them in 8-bit units.

20.2.10 Timer RC Control Register 2 (TRCCR2)

Address 0130h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCEG1	TCEG0	CSEL	—	—	POLD	POLC	POLB
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POLB	PWM mode output level control bit B (1)	0: TRCIOB output level selected as low active 1: TRCIOB output level selected as high active	R/W
b1	POLC	PWM mode output level control bit C (1)	0: TRCIOC output level selected as low active 1: TRCIOC output level selected as high active	R/W
b2	POLD	PWM mode output level control bit D (1)	0: TRCIOD output level selected as low active 1: TRCIOD output level selected as high active	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b4	—			
b5	CSEL	TRC count operation select bit (2)	0: Count continues at compare match with the TRCGRA register 1: Count stops at compare match with the TRCGRA register	R/W
b6	TCEG0	TRCTRG input edge select bit (3)	b7 b6 0 0: Trigger input from the TRCTRG pin disabled 0 1: Rising edge selected 1 0: Falling edge selected 1 1: Both edges selected	R/W
b7	TCEG1			R/W

Notes:
1. Enabled when in PWM mode.
2. For notes on PWM2 mode, refer to **20.9.6 TRCMR Register in PWM2 Mode**.
3. In timer mode and PWM mode, these bits are disabled.

20.2.11 Timer RC Digital Filter Function Select Register (TRCDF)

Address 0131h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DFCK1	DFCK0	—	DFTRG	DFD	DFC	DFB	DFA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DFA	TRCIOA pin digital filter function select bit (1)	0: Function is not used 1: Function is used	R/W
b1	DFB	TRCIOB pin digital filter function select bit (1)	0: Function is not used 1: Function is used	R/W
b2	DFC	TRCIOC pin digital filter function select bit (1)	0: Function is not used 1: Function is used	R/W
b3	DFD	TRCIOD pin digital filter function select bit (1)	0: Function is not used 1: Function is used	R/W
b4	DFTRG	TRCTRG pin digital filter function select bit (2)	0: Function is not used 1: Function is used	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	DFCK0	Digital filter function clock select bit (1, 2)	b7 b6 0 0: f32 0 1: f8 1 0: f1 1 1: Count source (clock selected by bits TCK0 to TCK2 in the TRCCR1 register)	R/W
b7	DFCK1			R/W

Notes:
1. These bits are enabled for the input capture function.
2. These bits are enabled when in PWM2 mode and bits TCEG1 to TCEG0 in the TRCCR2 register are set to 01b, 10b, or 11b (TRCTRG trigger input enabled).

20.2.12 Timer RC Output Master Enable Register (TRCOER)

Address 0132h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PTO	—	—	—	ED	EC	EB	EA
After Reset	0	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	EA	TRCIOA output disable bit (1)	0: Output enabled 1: Output disabled (TRCIOA pin functions as a programmable I/O port)	R/W
b1	EB	TRCIOB output disable bit (1)	0: Output enabled 1: Output disabled (TRCIOB pin functions as a programmable I/O port)	R/W
b2	EC	TRCIOC output disable bit (1)	0: Output enabled 1: Output disabled (TRCIOC pin functions as a programmable I/O port)	R/W
b3	ED	TRCIOD output disable bit (1)	0: Output enabled 1: Output disabled (TRCIOD pin functions as a programmable I/O port)	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	PTO	$\overline{\text{INT0}}$ of pulse output forced cutoff signal input enabled bit	0: Pulse output forced cutoff input disabled 1: Pulse output forced cutoff input enabled (Bits EA, EB, EC, and ED are set to 1 (output disabled) when a low-level signal is applied to the $\overline{\text{INT0}}$ pin)	R/W

Note:
1. These bits are disabled for pins set as input-capture input.

20.2.13 Timer RC Trigger Control Register (TRCADCR)

Address 0133h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	ADTRGDE	ADTRGCE	ADTRGBE	ADTRGAE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADTRGAE	A/D trigger A enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match between registers TRC and TRCGRA	R/W
b1	ADTRGBE	A/D trigger B enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match between registers TRC and TRCGRB	R/W
b2	ADTRGCE	A/D trigger C enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match between registers TRC and TRCGRC	R/W
b3	ADTRGDE	A/D trigger D enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match between registers TRC and TRCGRD	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

20.2.14 Timer RB/RC Pin Select Register (TRBRCSR)

Address 0181h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRCTRGSEL1	TRCTRGSEL0	—	TRCCLKSEL0	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	—			
b4	TRCCLKSEL0	TRCCLK pin select bit	0: TRCCLK pin not used 1: TRCCLK pin used	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	TRCTRGSEL0	TRCTRG pin select bit	b7 b6 0 0: TRCTRG pin not used 0 1: P3_7 assigned 1 0: P4_3 assigned 1 1: P4_4 assigned	R/W
b7	TRCTRGSEL1			R/W

The register function for timer RB is not implemented.
To use the I/O pins for timer RC, set the TRBRCSR register.
Set this register before setting the timer RC associated registers. Also, do not change the setting value of the TRCCLKSEL0 bit during timer RC operation.

20.2.15 Timer RC Pin Select Register 0 (TRCPSR0)

Address 0182h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	TRCIOBSEL1	TRCIOBSEL0	—	—	—	TRCIOASEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCIOASEL0	TRCIOA pin select bit	0: TRCIOA pin not used 1: TRCIOA pin used	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—			
b4	TRCIOBSEL0	TRCIOB pin select bit	b5 b4 0 0: TRCIOB pin not used 0 1: P4_5 assigned 1 0: P4_6 assigned 1 1: P4_7 assigned	R/W
b5	TRCIOBSEL1			R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

The TRCPSR0 register selects whether to use the timer RC input. To use the I/O pins for timer RC, set this register.
Set the TRCPSR0 register before setting the timer RC associated registers. Also, do not change the setting value of this register during timer RC operation.

20.2.16 Timer RC Pin Select Register 1 (TRCPSR1)

Address 0183h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	TRCIODSEL0	—	—	—	TRCIOCSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCIOCSEL0	TRCIOC pin select bit (1)	0: TRCIOC pin not used 1: P4_6 assigned	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—			
b4	TRCIODSEL0	TRCIOD pin select bit (2)	0: TRCIOD pin not used 1: P4_7 assigned	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	—			
b7	—			

Notes:
1. When bits TRCIOBSEL1 to TRCIOBSEL0 in the TRCPSR0 register are set to 10b (P4_6 assigned as TRCIOB pin), P4_6 functions as the TRCIOB pin regardless of the content of the TRCIOCSEL0 bit.
2. When bits TRCIOBSEL1 to TRCIOBSEL0 in the TRCPSR0 register are set to 11b (P4_7 assigned as TRCIOB pin), P4_7 functions as the TRCIOB pin regardless of the content of the TRCIODSEL0 bit.

The TRCPSR1 register selects whether to use the timer RC input. To use the I/O pins for timer RC, set this register.
Set the TRCPSR1 register before setting the timer RC associated registers. Also, do not change the setting value of this register during timer RC operation.

20.3 Common Items for Multiple Modes

20.3.1 Count Source

The method of selecting the count source is common to all modes.
Table 20.5 lists the Count Source Selection, and Figure 20.2 shows the Count Source Block Diagram.

Table 20.5 Count Source Selection

Count Source	Selection Method
f1, f2, f4, f8, f32	The count source is selected by bits TCK0 to TCK2 in TRCCR1 register
fOCO40M	- The FRA00 bit in the FRA0 register set to 1 (high-speed on-chip oscillator on). - Bits TCK2 to TCK0 in the TRCCR1 register are set to 110b (fOCO40M).
External signal input to TRCCLK pin	- Bits TCK2 to TCK0 in TRCCR1 register are set to 101b (count source is rising edge of external clock) - The corresponding direction bit in the direction register is set is set to 0 (input mode)

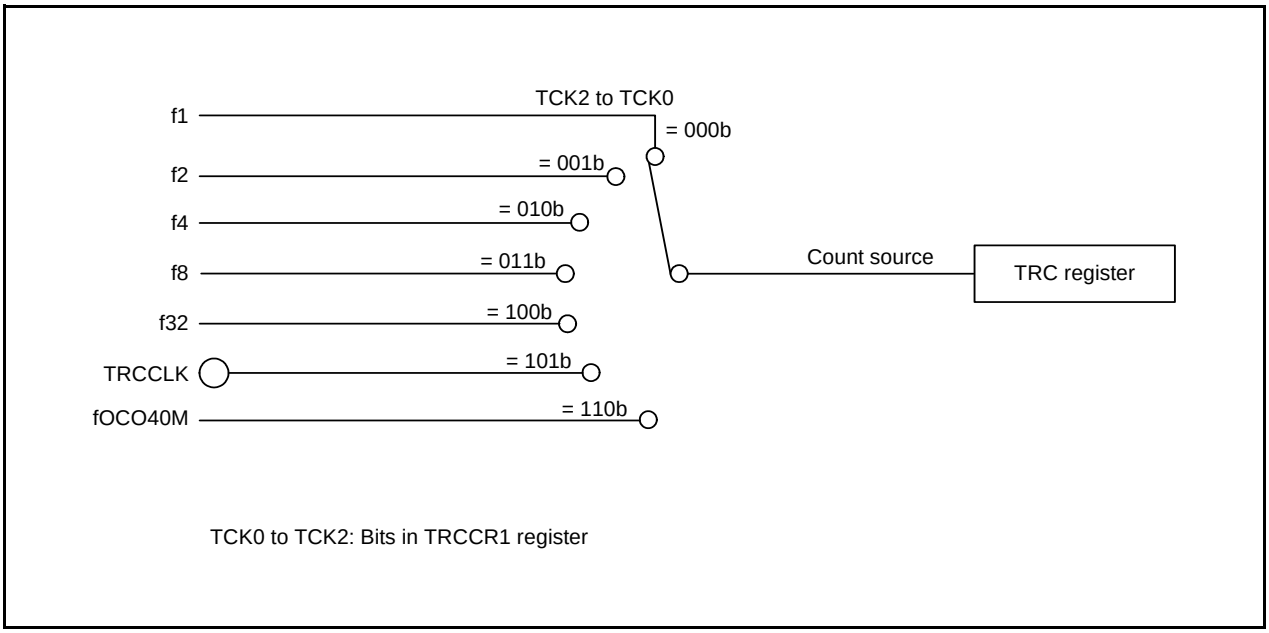


Figure 20.2 Count Source Block Diagram

The pulse width of the external clock input to the TRCCLK pin should be set to three cycles or more of the timer RC operation clock. (See **Table 20.1 Timer RC Operating Clocks.**)
To select fOCO40M as the count source, set the FRA00 bit in the FRA0 register set to 1 (high-speed on-chip oscillator on), and then set bits TCK2 to TCK0 in the TRCCR1 register to 110b (fOCO40M).

20.3.2 Buffer Operation

Bits BFC and BFD in the TRCMR register are used to select the TRCGRC or TRCGRD register as the buffer register of the TRCGRA or TRCGRB register.

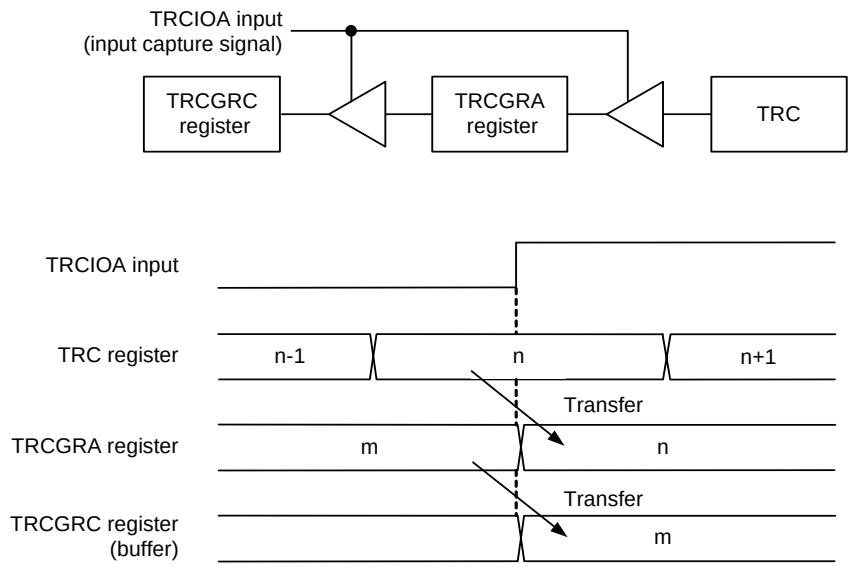
- Buffer register of TRCGRA register: TRCGRC register
- Buffer register of TRCGRB register: TRCGRD register

Buffer operation differs depending on the mode.

Table 20.6 lists the Buffer Operation in Each Mode, Figure 20.3 shows the Buffer Operation of Input Capture Function, and Figure 20.4 shows the Buffer Operation of Output Compare Function.

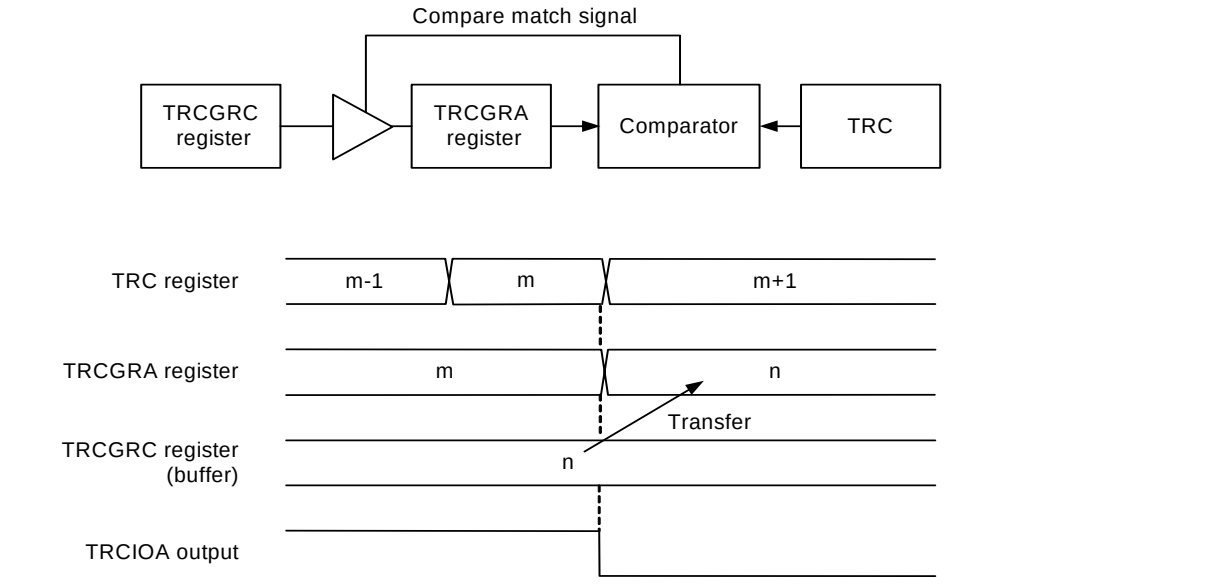
Table 20.6 Buffer Operation in Each Mode

Function, Mode	Transfer Timing	Transfer Destination Register
Input capture function	Input capture signal input	The content of the TRCGRA (TRCGRB) register is transferred to the buffer register.
Output compare function PWM mode	Compare match between the TRC register and the TRCGRA (TRCGRB) register	The content of the buffer register is transferred to the TRCGRA (TRCGRB) register.
PWM2 mode	• Compare match between the TRC register and the TRCGRA register • TRCTRG pin trigger input	The content of the buffer register (TRCGRD) is transferred to the TRCGRB register.



The above applies under the following conditions:
- The BFC bit in the TRCMR register is set to 1 (TRCGRC register is used as the buffer register of the TRCGRA register).
- Bits IOA2 to IOA0 in the TRCIOR0 register are set to 100b (input capture at the rising edge).

Figure 20.3 Buffer Operation of Input Capture Function



The above applies under the following conditions:
- The BFC bit in the TRCMR register is set to 1 (TRCGRC register is used as the buffer register of the TRCGRA register).
- Bits IOA2 to IOA0 in the TRCIOR0 register are set to 001b (low-level output at compare match).

Figure 20.4 Buffer Operation of Output Compare Function

Make the following settings in timer mode.
- To use the TRCGRC register as the buffer register of the TRCGRA register:
  Set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
- To use the TRCGRD register as the buffer register of the TRCGRB register:
  Set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

When the TRCGRC or TRCGRD register is also used as the buffer register for the output compare function, in PWM mode, or PWM2 mode, the IMFC or IMFD bit in the TRCSR register is set to 1 by a compare match with the TRC register.
When the TRCGRC register or TRCGRD register is also used as the buffer register for the input capture function, the IMFC or IMFD bit in the TRCSR register is set to 1 at the input edge of a signal input to the TRCIOC or TRCIOD pin.

20.3.3 Digital Filter

The input to TRCTRG or TRCIOj (j = A, B, C, or D) is sampled, and the level is determined when three matches occur. The digital filter function and sampling clock can be selected using the TRCDF register. Figure 20.5 shows a Block Diagram of Digital Filter.

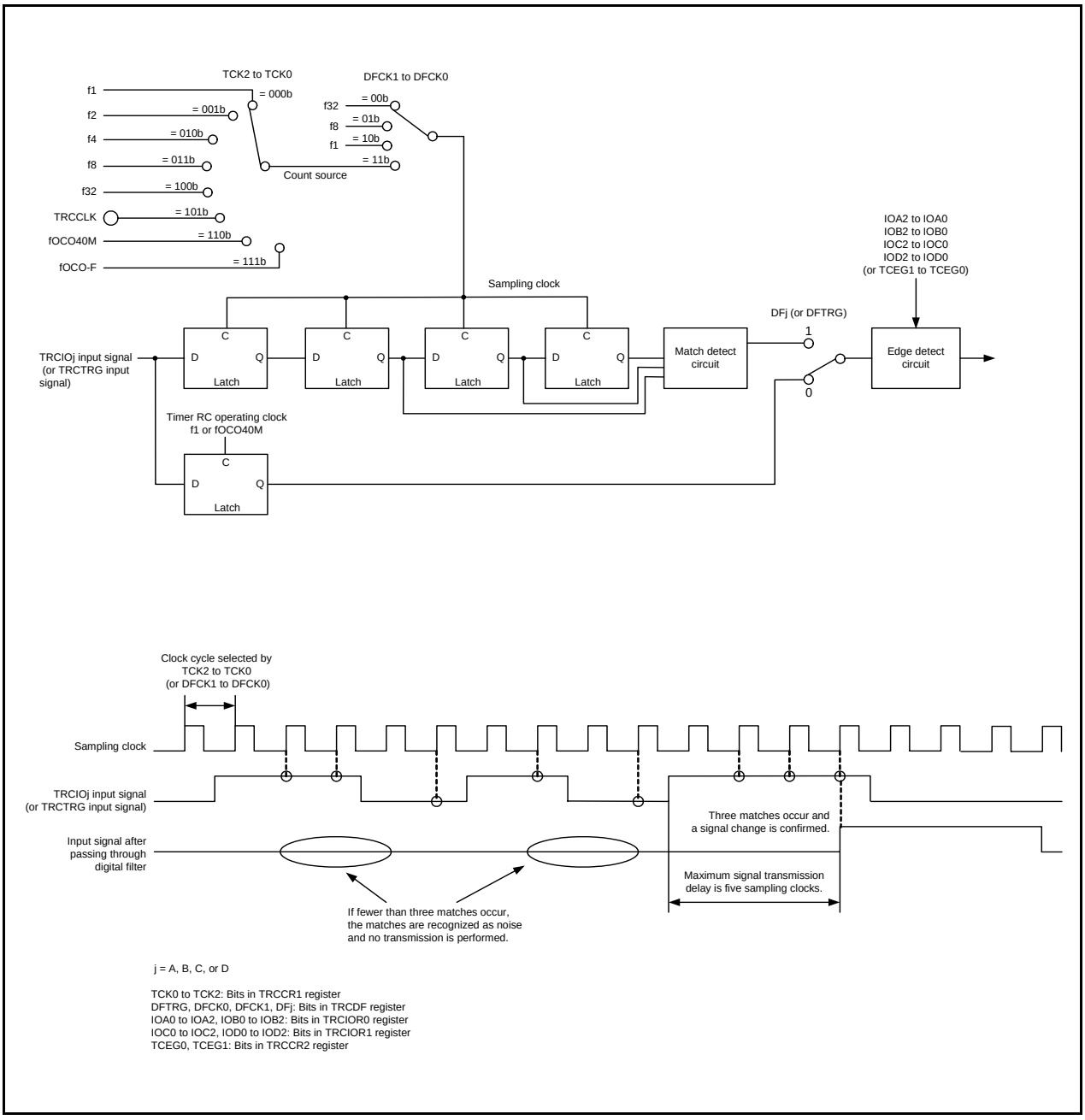


Figure 20.5 Block Diagram of Digital Filter

20.3.4 Forced Cutoff of Pulse Output

When using the timer mode's output compare function, PWM mode, or PWM2 mode, pulse output from the TRCIOj (j = A, B, C, or D) output pin can be forcibly cut off and the TRCIOj pin set to function as a programmable I/O port by means of input to the $\overline{\text{INT0}}$ pin.
A pin used for output by the timer mode's output compare function, PWM mode, or PWM2 mode can be set to function as the timer RC output pin by setting the Ej bit in the TRCOER register to 0 (timer RC output enabled). If a low-level signal is input to the $\overline{\text{INT0}}$ pin while the PTO bit in the TRCOER register is set to 1 (pulse output forced cutoff signal input $\overline{\text{INT0}}$ enabled), bits EA, EB, EC, and ED in the TRCOER register are all set to 1 (timer RC output disabled, TRCIOj output pin functions as a programmable I/O port). When one or two cycles of the timer RC operation clock after a low-level signal input to the $\overline{\text{INT0}}$ pin (refer to **Table 20.1 Timer RC Operating Clocks**) has elapsed, the TRCIOj output pin functions as a programmable I/O port.

Make the following settings to use this function.

- Set the pin state following forced cutoff of pulse output (high impedance (input), low-level output, or high-level output). (Refer to **7. I/O Ports**.)
- Set the INT0EN bit to 1 ($\overline{\text{INT0}}$ input enabled) and the INT0PL bit to 0 (one edge) in the INTEN register.
- Set the direction registers for the I/O ports selected as $\overline{\text{INT0}}$ to input mode:
  When INT0 is assigned to P3_0 by the INT0SEL0 bit in the INTSR register, set the PD3_0 bit in the PD3 register to 0 (input mode).
  When INT0 is assigned to P11_0 by the INT0SEL0 bit in the INTSR register, set the PD11_0 bit in the PD11 register to 0 (input mode).
- Select the $\overline{\text{INT0}}$ digital filter with bits INT0F0 and INT0F1 in the INTF register.
- Set the PTO bit in the TRCOER register to 1 (pulse output forced cutoff signal input $\overline{\text{INT0}}$ enabled).

The IR bit in the INT0IC register is set to 1 (interrupt requested) in accordance with the setting of the POL bit and a change in the $\overline{\text{INT0}}$ pin input (refer to **12.8 Notes on Interrupts**).
For details on interrupts, refer to **12. Interrupts**.

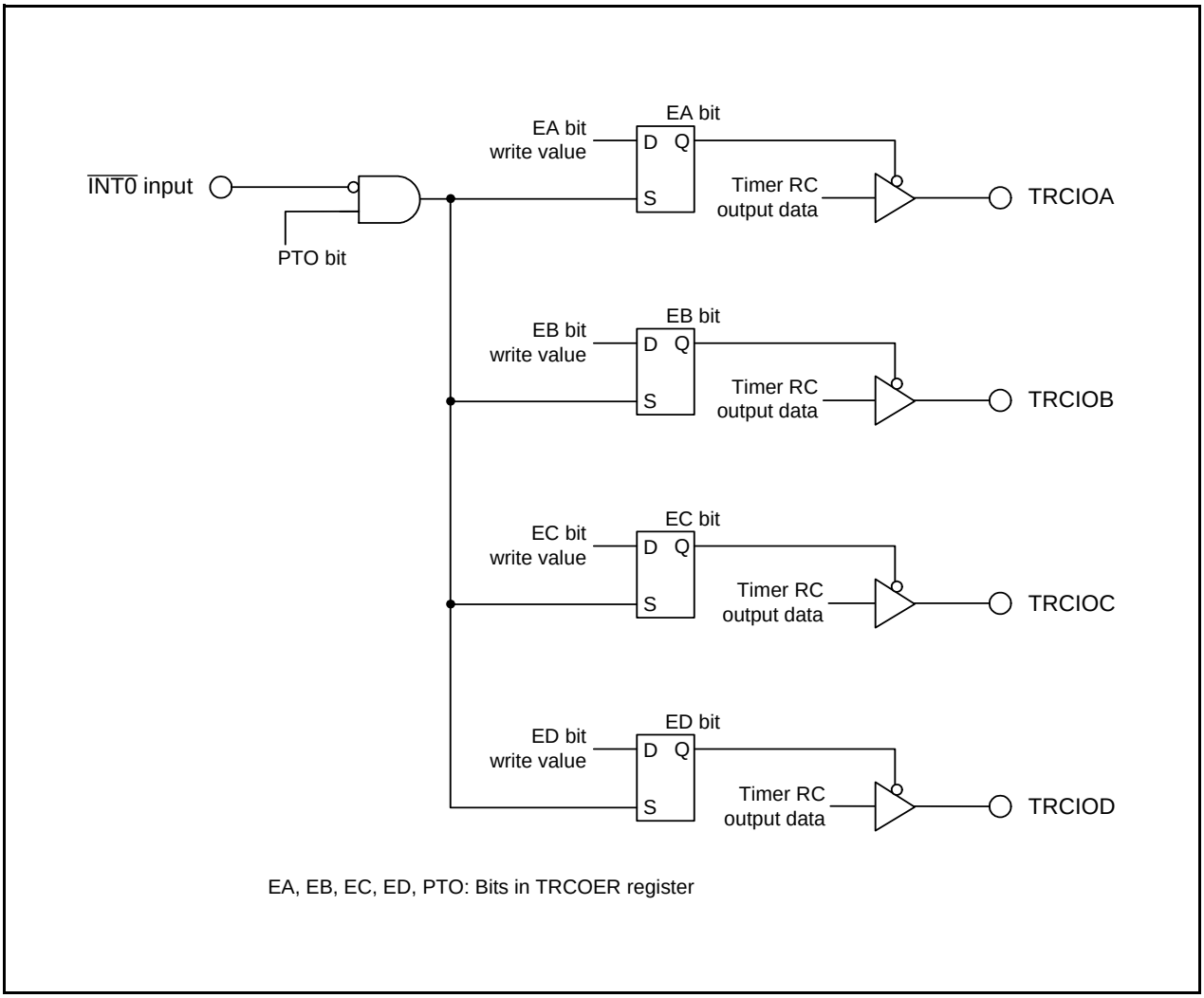


Figure 20.6 Forced Cutoff of Pulse Output

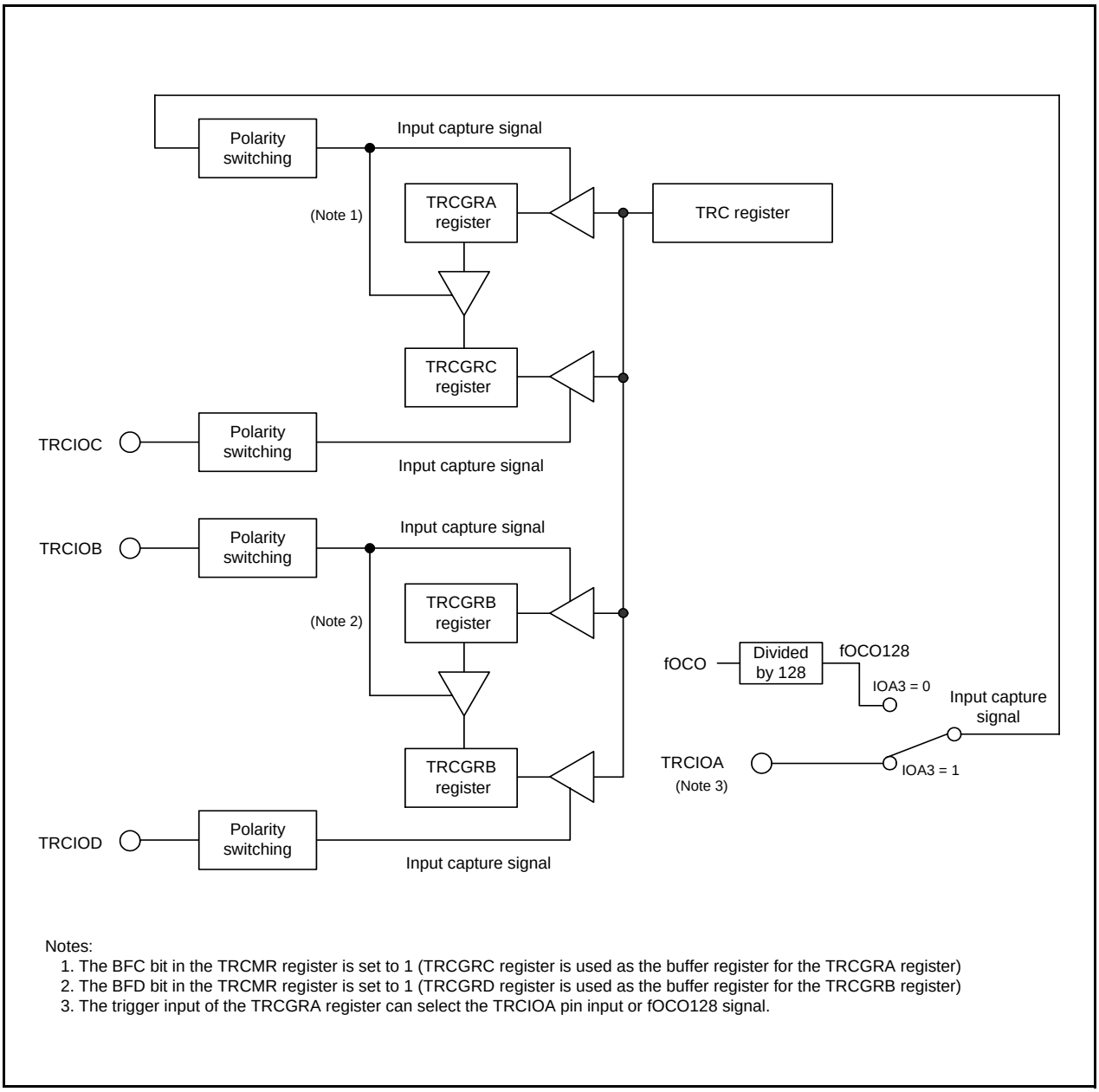
20.4 Timer Mode (Input Capture Function)

This function measures the width or period of an external signal. An external signal input to the TRCIOj (j = A, B, C, or D) pin acts as a trigger for transferring the content of the TRC register (counter) to the TRCGRj register (input capture). The input capture function, or any other mode or function, can be selected for each individual pin. Table 20.7 lists the Input Capture Function Specifications, Figure 20.7 shows a Block Diagram of Input Capture Function, Table 20.8 lists the Functions of TRCGRj Register when Using Input Capture Function, and Figure 20.8 shows an Operating Example of Input Capture Function.

Table 20.7 Input Capture Function Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, fOCO40M External signal (rising edge) input to the TRCCLK pin
Count operation	Increment
Count period	1/fk × 65,536 fk: Frequency of count source
Count start condition	1 (count starts) is written to the TSTART bit in the TRCMR register.
Count stop condition	0 (count stops) is written to the TSTART bit in the TRCMR register. The TRC register retains a value before the count stops.
Interrupt request generation timing	• Input capture (active edge of the TRCIOj input) • TRC register overflows
TRCIOA, TRCIOB, TRCIOC, and TRCIOD pins function	Programmable I/O port or input capture input (selectable for each individual pin)
$\overline{\text{INT0}}$ pin function	Programmable I/O port or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading TRC register.
Write to timer	The TRC register can be written to.
Selectable functions	• Input-capture input pin selection One or more of pins TRCIOA, TRCIOB, TRCIOC, and TRCIOD • Input-capture input active edge selection Rising edge, falling edge, or both rising and falling edges • Buffer operation (Refer to **20.3.2 Buffer Operation**.) • Digital filter (Refer to **20.3.3 Digital Filter**.) • Timing for setting the TRC register to 0000h Overflow or input capture

j = A, B, C, or D



Notes:
1. The BFC bit in the TRCMR register is set to 1 (TRCGRC register is used as the buffer register for the TRCGRA register)
2. The BFD bit in the TRCMR register is set to 1 (TRCGRD register is used as the buffer register for the TRCGRB register)
3. The trigger input of the TRCGRA register can select the TRCIOA pin input or fOCO128 signal.

Figure 20.7 Block Diagram of Input Capture Function

20.4.1 Timer RC I/O Control Register 0 (TRCIOR0) in Timer Mode (Input Capture Function)

Address 0124h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRCGRA control bit	b1 b0 0 0: Input capture to the TRCGRA register at the rising edge 0 1: Input capture to the TRCGRA register at the falling edge 1 0: Input capture to the TRCGRA register at both edges 1 1: Do not set.	R/W
b1	IOA1			R/W
b2	IOA2	TRCGRA mode select bit (1)	Set to 1 (input capture) for the input capture function.	R/W
b3	IOA3	TRCGRA input-capture input switch bit (3)	0: fOCO128 signal 1: TRCIOA pin input	R/W
b4	IOB0	TRCGRB control bit	b5 b4 0 0: Input capture to the TRCGRB register at the rising edge 0 1: Input capture to the TRCGRB register at the falling edge 1 0: Input capture to the TRCGRB register at both edges 1 1: Do not set.	R/W
b5	IOB1			R/W
b6	IOB2	TRCGRB mode select bit (2)	Set to 1 (input capture) for the input capture function.	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.
3. The IOA3 bit is enabled when the IOA2 bit is set to 1 (input capture function).

20.4.2 Timer RC I/O Control Register 1 (TRCIOR1) in Timer Mode (Input Capture Function)

Address 0125h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOC0	TRCGRC control bit	b1 b0 0 0: Input capture to the TRCGRC register at the rising edge 0 1: Input capture to the TRCGRC register at the falling edge 1 0: Input capture to the TRCGRC register at both edges 1 1: Do not set.	R/W
b1	IOC1			R/W
b2	IOC2	TRCGRC mode select bit (1)	Set to 1 (input capture) for the input capture function.	R/W
b3	IOC3	TRCGRC register function select bit	Set to 1.	R/W
b4	IOD0	TRCGRD control bit	b5 b4 0 0: Input capture to the TRCGRD register at the rising edge 0 1: Input capture to the TRCGRD register at the falling edge 1 0: Input capture to the TRCGRD register at both edges 1 1: Do not set.	R/W
b5	IOD1			R/W
b6	IOD2	TRCGRD mode select bit (2)	Set to 1 (input capture) for the input capture function.	R/W
b7	IOD3	TRCGRD register function select bit	Set to 1.	R/W

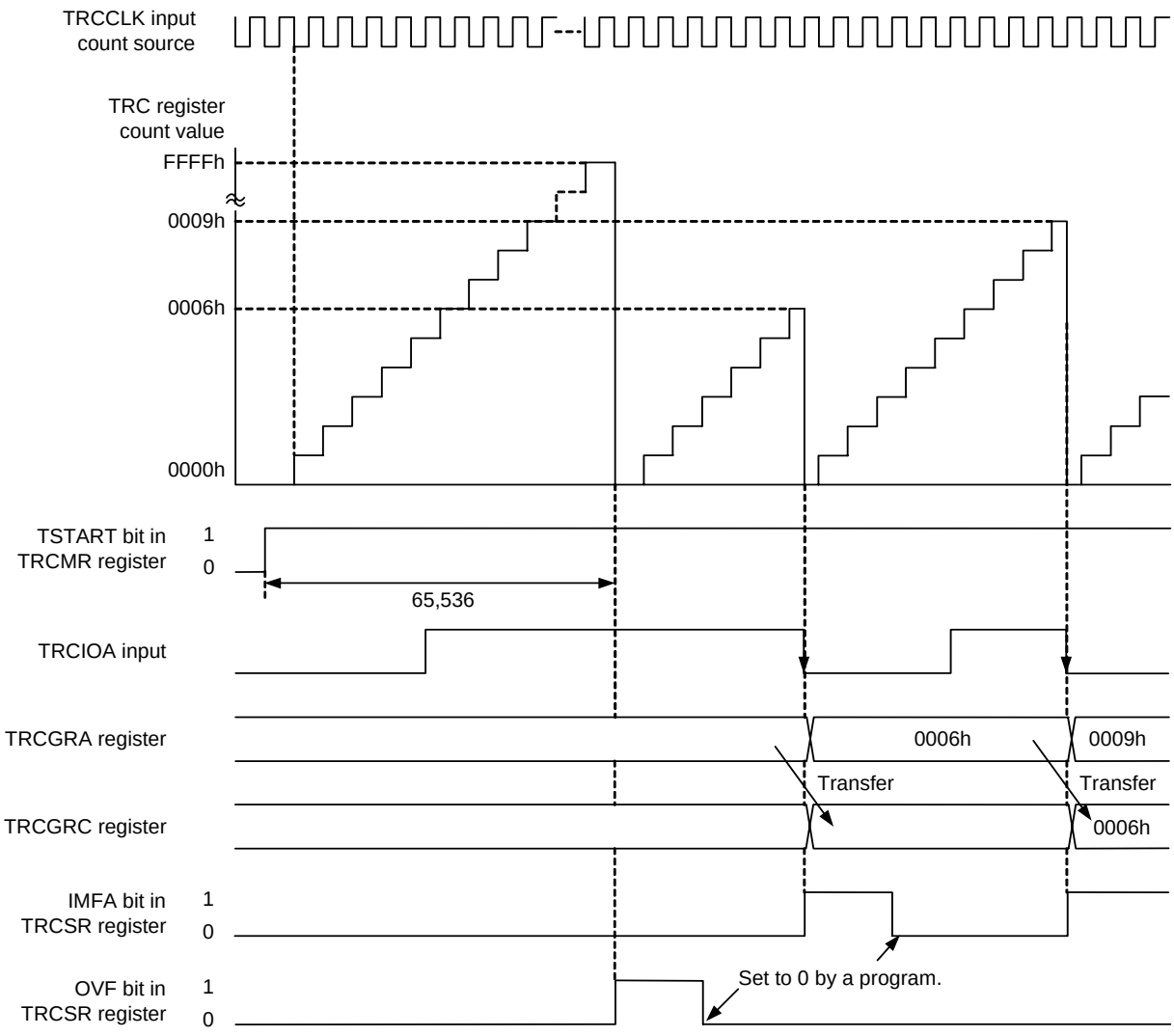
Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

Table 20.8 Functions of TRCGRj Register when Using Input Capture Function

Register	Setting	Register Function	Input Capture Input Pin
TRCGRA	–	General register. Can be used to read the TRC register value at input capture.	TRCIOA
TRCGRB			TRCIOB
TRCGRC	BFC = 0	General register. Can be used to read the TRC register value at input capture.	TRCIOC
TRCGRD	BFD = 0		TRCIOD
TRCGRC	BFC = 1	Buffer registers. Can be used to retain the transferred value from the general register. (Refer to **20.3.2 Buffer Operation**.)	TRCIOA
TRCGRD	BFD = 1		TRCIOB

j = A, B, C, or D
BFC, BFD: Bits in TRCMR register

20.4.3 Operating Example



The above applies under the following conditions:
- The CCLR bit in the TRCCR1 register is set to 1 (TRC counter cleared by input capture).
- Bits TCK2 to TCK0 in the TRCCR1 register are set to 101b (TRCCLK input selected as the count source).
- Bits IOA2 to IOA0 in the TRCIORA register are set to 101b (input capture at the falling edge of the TRCIOA input).
- The BFC bit in the TRCMR register is set to 1 (TRCGRC register functions as the buffer register of the TRCGRA register).

Figure 20.8 Operating Example of Input Capture Function

20.5 Timer Mode (Output Compare Function)

This function detects when the contents of the TRC register (counter) and the TRCGRj register (j = A, B, C, or D) match (compare match). When a match occurs, a signal is output from the TRCIOj pin at a given level. The output compare function, or other mode or function, can be selected for each individual pin.
Table 20.9 lists the Output Compare Function Specifications, Figure 20.9 shows a Block Diagram of Output Compare Function, Table 20.10 lists the Functions of TRCGRj Register when Using Output Compare Function, and Figure 20.10 shows an Operating Example of Output Compare Function.

Table 20.9 Output Compare Function Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, fOCO40M, fOCO-F External signal input to the TRCCLK pin (rising edge)
Count operation	Increment
Count periods	• The CCLR bit in the TRCCR1 register is set to 0 (free-running operation): 1/fk × 65,536 fk: Frequency of count source • The CCLR bit in the TRCCR1 register is set to 1 (TRC register is set to 0000h by TRCGRA compare match): 1/fk × (n + 1) n: Value set in TRCGRA register
Waveform output timing	Compare match
Count start condition	1 (count starts) is written to the TSTART bit in the TRCMR register.
Count stop condition	• When the CSEL bit in the TRCCR2 register is set to 0 (count continues after compare match with the TRCGRA register). 0 (count stops) is written to the TSTART bit in the TRCMR register. The output compare output pin retains the output level before the count stops, the TRC register retains a value before the count stops. • When the CSEL bit in the TRCCR2 register is set to 1 (count stops at compare match with the TRCGRA register). The count stops at a compare match with the TRCGRA register. The output-compare output pin retains the level after the output is changed by the compare match.
Interrupt request generation timing	• Compare match (the contents of the TRC register and the TRCGRj register match.) • TRC register overflow
TRCIOA, TRCIOB, TRCIOC, and TRCIOD pins function	Programmable I/O port or output compare output (selectable for each individual pin)
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRC register.
Write to timer	The TRC register can be written to.
Selectable functions	• Output-compare output pin selection One or more of pins TRCIOA, TRCIOB, TRCIOC, and TRCIOD • Output level selection at the compare match Low-level output, High-level output, or toggle output • Initial output level selection Selectable output level for the period from the count start to the compare match • Timing for setting the TRC register to 0000h Overflow or compare match with the TRCGRA register • Buffer operation (Refer to **20.3.2 Buffer Operation**.) • Pulse output forced cutoff signal input (Refer to **20.3.4 Forced Cutoff of Pulse Output**.) • Timer RC can be used as an internal timer by disabling the timer RC output • Changing output pins for registers TRCGRC and TRCGRD TRCGRC can be used for output control of the TRCIOA pin and TRCGRD can be used for output control of the TRCIOB pin. • A/D trigger generation

j = A, B, C, or D

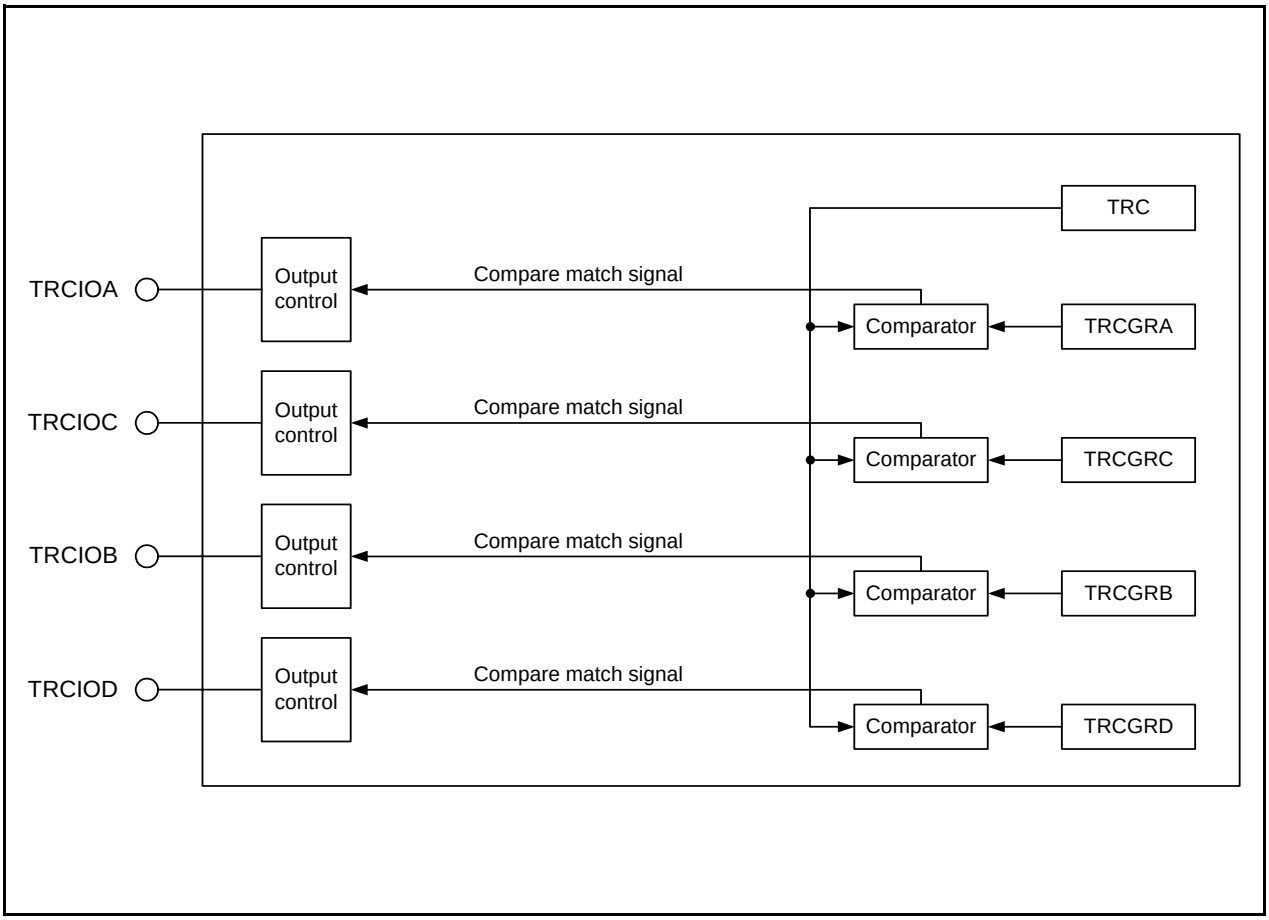


Figure 20.9 Block Diagram of Output Compare Function

20.5.1 Timer RC Control Register 1 (TRCCR1) in Timer Mode (Output Compare Function)

Address 0121h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR	TCK2	TCK1	TCK0	TOD	TOC	TOB	TOA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA	TRCIOA output level select bit (1, 2)	0: Initial output at low 1: Initial output at high	R/W
b1	TOB	TRCIOB output level select bit (1, 2)		R/W
b2	TOC	TRCIOC output level select bit (1, 2)		R/W
b3	TOD	TRCIOD output level select bit (1, 2)		R/W
b4	TCK0	Count source select bit (1)	b6 b5 b4 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRCCLK input rising edge 1 1 0: fOCO40M 1 1 1: Do not set.	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	CCLR	TRC counter clear select bit	0: Clear disabled (free-running operation) 1: Clear by compare match with the TRCGRA register	R/W

Notes:
1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).
2. If the pin function is set for waveform output (refer to **7.5 Port Settings**), the initial output level is output when the TRCCR1 register is set.

Table 20.10 Functions of TRCGRj Register when Using Output Compare Function

Register	Setting	Register Function	Output Compare Output Pin
TRCGRA	–	General register. Write a compare value to one of these registers.	TRCIOA
TRCGRB			TRCIOB
TRCGRC	BFC = 0	General register. Write a compare value to one of these registers.	TRCIOC
TRCGRD	BFD = 0		TRCIOD
TRCGRC	BFC = 1	Buffer register. Write the next compare value to one of these registers. (Refer to **20.3.2 Buffer Operation**.)	TRCIOA
TRCGRD	BFD = 1		TRCIOB

j = A, B, C, or D
BFC, BFD: Bits in TRCMR register

20.5.2 Timer RC I/O Control Register 0 (TRCIOR0) in Timer Mode (Output Compare Function)

Address 0124h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRCGRA control bit	b1 b0	R/W
b1	IOA1		0 0: Pin output by compare match is disabled (TRCIOA pin functions as a programmable I/O port) 0 1: Low-level output at compare match with the TRCGRA register 1 0: High-level output at compare match with the TRCGRA register 1 1: Toggle output at compare match with the TRCGRA register	R/W
b2	IOA2	TRCGRA mode select bit (1)	Set to 0 (output compare) for the output compare function.	R/W
b3	IOA3	TRCGRA input capture input switch bit	Set to 1.	R/W
b4	IOB0	TRCGRB control bit	b5 b4	R/W
b5	IOB1		0 0: Pin output by compare match is disabled (TRCIOB pin functions as a programmable I/O port) 0 1: Low-level output at compare match with the TRCGRB register 1 0: High-level output at compare match with the TRCGRB register 1 1: Toggle output at compare match with the TRCGRB register	R/W
b6	IOB2	TRCGRB mode select bit (2)	Set to 0 (output compare) for the output compare function.	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in theTRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

20.5.3 Timer RC I/O Control Register 1 (TRCIOR1) in Timer Mode (Output Compare Function)

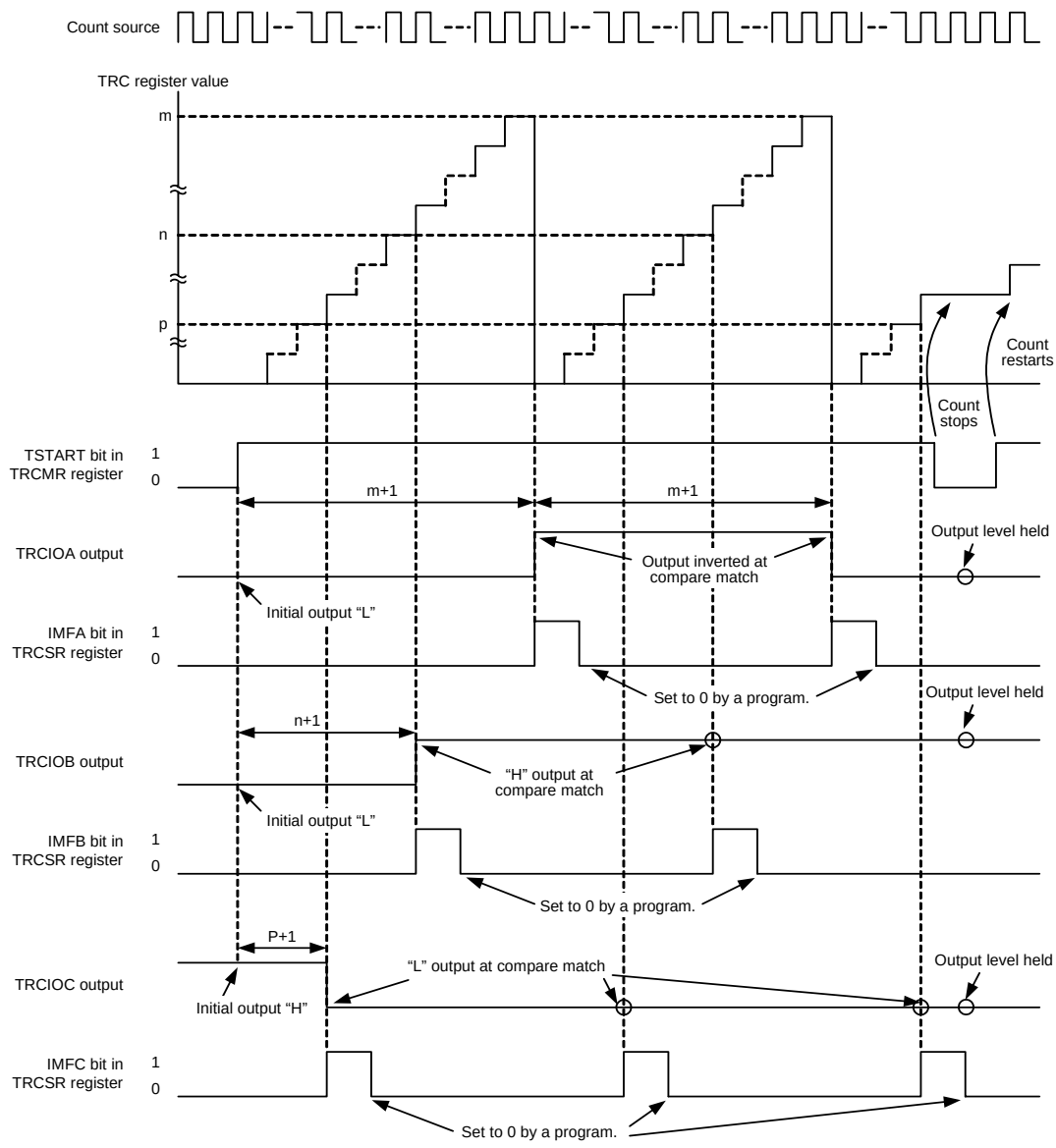
Address 0125h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOC0	TRCGRC control bit	b1 b0 0 0: Pin output by compare match is disabled 0 1: Low-level output at compare match with the TRCGRC register 1 0: High-level output at compare match with the TRCGRC register 1 1: Toggle output at compare match with the TRCGRC register	R/W
b1	IOC1			R/W
b2	IOC2	TRCGRC mode select bit (1)	Set to 0 (output compare) for the output compare function.	R/W
b3	IOC3	TRCGRC register function select bit	0: TRCIOA output register 1: General register or buffer register	R/W
b4	IOD0	TRCGRD control bit	b5 b4 0 0: Pin output by compare match is disabled 0 1: Low-level output at compare match with the TRCGRD register 1 0: High-level output at compare match with the TRCGRD register 1 1: Toggle output at compare match with the TRCGRD register	R/W
b5	IOD1			R/W
b6	IOD2	TRCGRD mode select bit (2)	Set to 0 (output compare) for the output compare function.	R/W
b7	IOD3	TRCGRD register function select bit	0: TRCIOB output register 1: General register or buffer register	R/W

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in theTRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in theTRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

20.5.4 Operating Example



m: Value set in TRCGRA register
n: Value set in TRCGRB register
p: Value set in TRCGRC register

The above applies under the following conditions:

- Bits BFC and BFD in the TRCMR register are set to 0 (registers TRCGRC and TRCGRD are not used as buffer registers).
- Bits EA, EB, and EC in the TRCOER register are set to 0 (TRCIOA, TRCIOB, and TRCIOC pin output enabled).
- The CCLR bit in the TRCCR1 register is set to 1 (TRC register is set to 0000h by compare match with TRCGRA register).
- Bits TOA and TOB in the TRCCR1 register are are set to 0 (initial output at low until compare match) and the TOC bit is set to 1 (initial output at high until compare match).
- Bits IOA2 to IOA0 in the TRCIOR0 register are set to 011b (TRCIOA output inverted by TRCGRA compare match).
- Bits IOB2 to IOB0 in the TRCIOR0 register are set to 010b (TRCIOB high-level output at TRCGRB compare match).
- Bits IOC2 to IOC2 in the TRCIOR1 register are set to 001b (TRCIOC low-level output at TRCGRC compare match).
- The CSEL bit in the TRCCR2 register is set to 0 (TRC count continues after TRCGRA compare match).

Figure 20.10 Operating Example of Output Compare Function

20.5.5 Changing Output Pins in Registers TRCGRC and TRCGRD

The TRCGRC register can be used for output control of the TRCIOA pin, and the TRCGRD register can be used for output control of the TRCIOB pin. Each pin output can be controlled as follows:

- TRCIOA output is controlled by the values of registers TRCGRA and TRCGRC.
- TRCIOB output is controlled by the values of registers TRCGRB and TRCGRD.

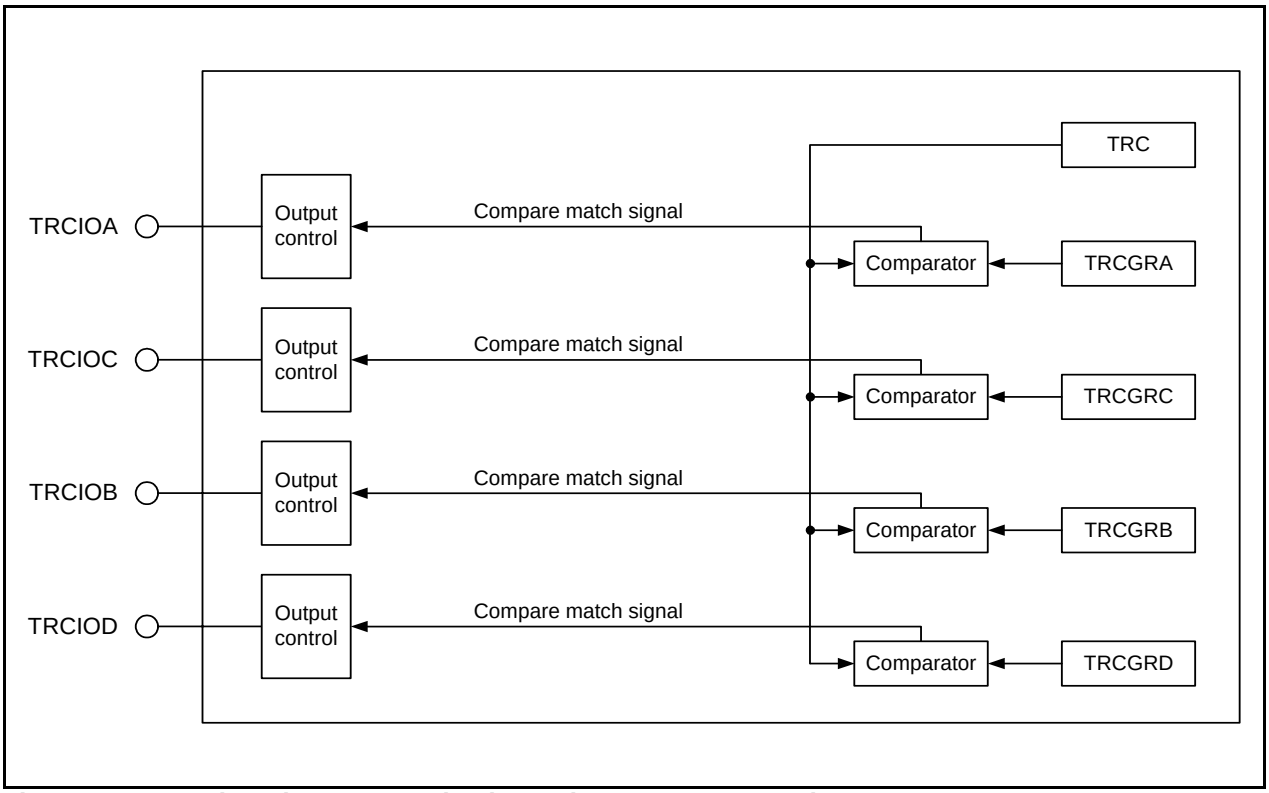
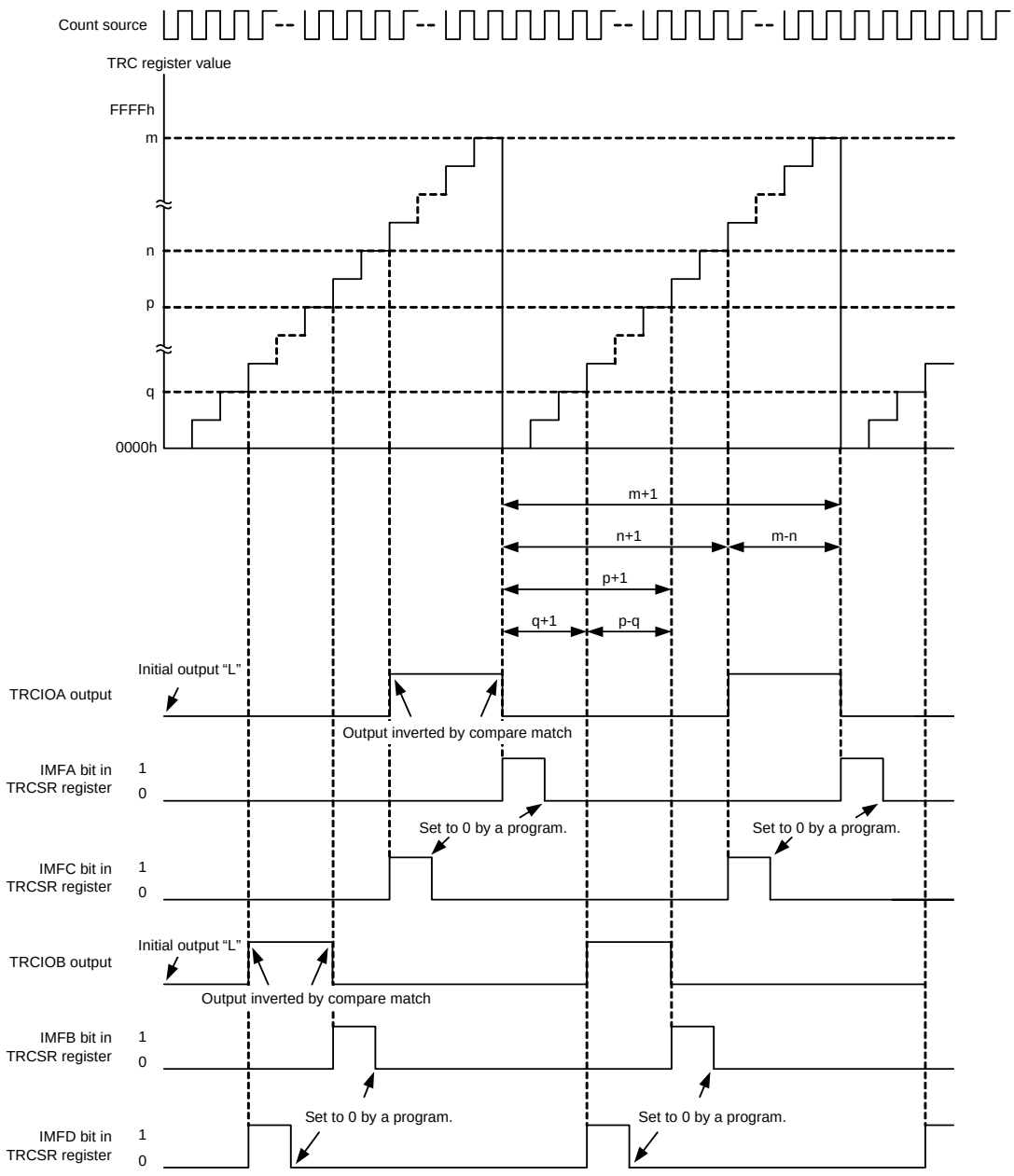


Figure 20.11 Changing Output Pins in Registers TRCGRC and TRCGRD

Change output pins in registers TRCGRC and TRCGRD as follows:

- Set the IOC3 bit in the TRCIOR1 register to 0 (TRCIOA output register) and set the IOD3 bit to 0 (TRCIOB output register).
- Set bits BFC and BFD in the TRCMR register to 0 (general register).
- Set different values in registers TRCGRC and TRCGRA. Also, set different values in registers TRCGRD and TRCGRB.

Figure 20.12 shows an Operating Example When TRCGRC Register is Used for Output Control of TRCIOA Pin and TRCGRD Register is Used for Output Control of TRCIOB Pin.



m: Value set in TRCGRA register
n: Value set in TRCGRC register
p: Value set in TRCGRB register
q: Value set in TRCGRD register

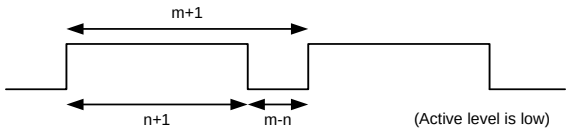
The above applies under the following conditions:
Bits BFC and BFD in the TRCMR register are set to 0 (registers TRCGRC and TRCGRD are not used as buffer registers).
Bits EA and EB in the TRCOER register are set to 0 (TRCIOA and TRCIOB pin output enabled).
The CCLR bit in the TRCCR1 register are set to 1 (TRC register is set to 0000h by compare match with the TRCGRA register).
Bits TOA and TOB in the TRCCR1 register are set to 0 (initial output at low until compare match).
Bits IOA2 to IOA0 in the TRCIOR0 register are set to 011b (TRCIOA output inverted by TRCGRA register compare match).
Bits IOB2 to IOB0 in the TRCIOR0 register are set to 011b (TRCIOB output inverted by TRCGRB register compare match).
Bits IOC2 to IOC0 in the TRCIOR1 register are set to 011b (TRCIOA output inverted by TRCGRC register compare match).
The IOC3 bit in the TRCIOR1 register are set to 0 (TRCIOA output register).
Bits IOD2 to IOD0 in the TRCIOR1 register are set to 011b (TRCIOB output inverted by TRCGRD register compare match).
The IOD3 bit in the TRCIOR1 register are set to 0 (TRCIOB output register).
The CSEL bit in the TRCCR2 register are set to 0 (TRC count continues after compare match).

Figure 20.12 Operating Example When TRCGRC Register is Used for Output Control of TRCIOA Pin and TRCGRD Register is Used for Output Control of TRCIOB Pin

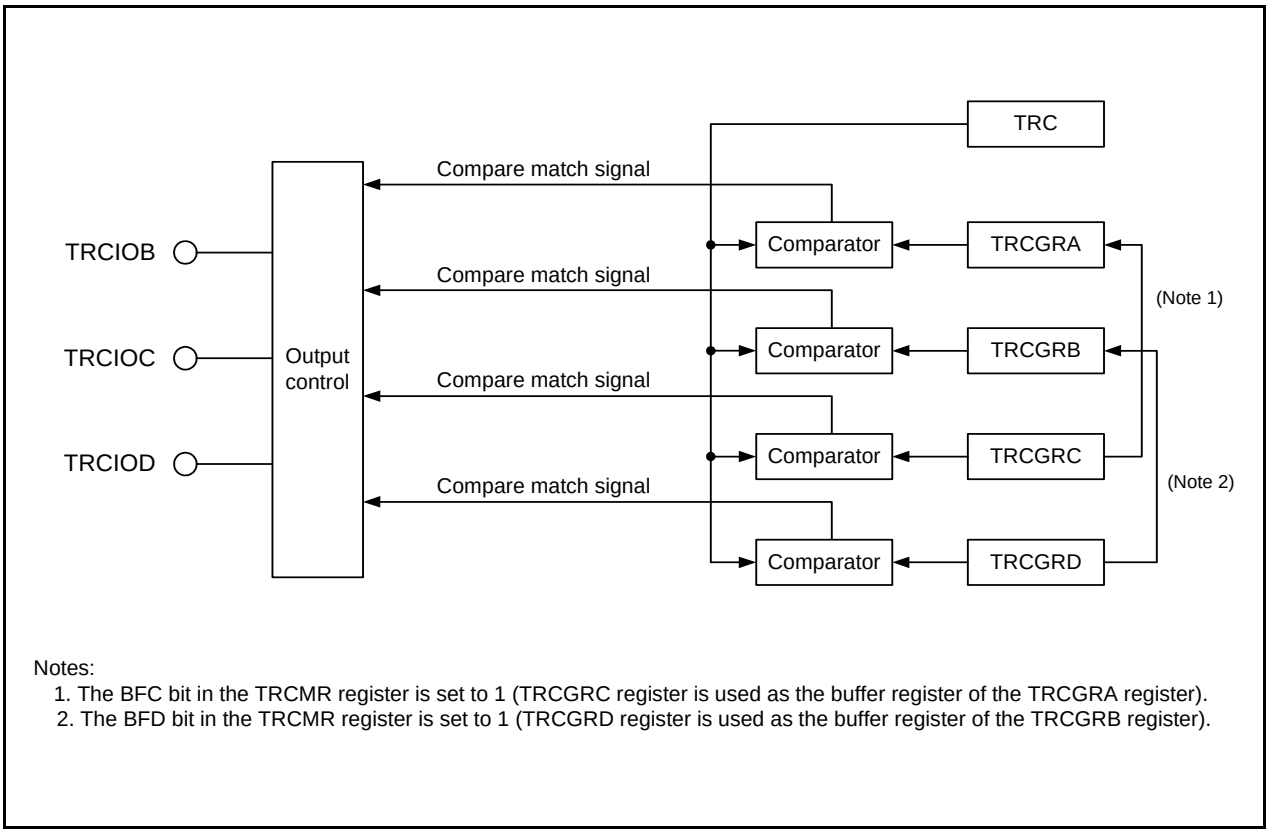
20.6 PWM Mode

This mode outputs PWM waveforms. A maximum of three PWM waveforms with the same period are output. PWM mode or timer mode can be selected for each individual pin. (However, the TRCGRA register cannot be used for timer mode since the register is used when using any pin for PWM mode.)
Table 20.11 lists the PWM Mode Specifications, Figure 20.13 shows a Block Diagram of PWM Mode, Table 20.12 lists the Functions of TRCGRh Register in PWM Mode, and Figures 20.14 and 20.15 show Operating Examples in PWM Mode.

Table 20.11 PWM Mode Specifications

Item	Specification
Count source	f1, f2, f4, f8, f32, fOCO40M, fOCO-F External signal (rising edge) input to the TRCCLK pin
Count operation	Increment
PWM waveform	PWM period: 1/fk × (m + 1) Active level width: 1/fk × (m - n) Inactive width: 1/fk × (n + 1) fk: Frequency of count source m: Value set in TRCGRA register n: Value set in TRCGRj register 
Count start condition	1 (count starts) is written to the TSTART bit in the TRCMR register.
Count stop condition	• When the CSEL bit in the TRCCR2 register is set to 0 (count continues after compare match with the TRCGRA register). 0 (count stops) is written to the TSTART bit in the TRCMR register. The PWM output pin retains the output level before the count stops, The TRC register retains a value before the count stops. • When the CSEL bit in the TRCCR2 register is set to 1 (count stops at compare match with the TRCGRA register). The count stops at a compare match with the TRCGRA register. The PWM output pin retains the level after the output is changed by the compare match.
Interrupt request generation timing	• Compare match (the contents of the TRC register and the TRCGRj register match) • TRC register overflow
TRCIOA pin function	Programmable I/O port
TRCIOB, TRCIOC, and TRCIOD pins function	Programmable I/O port or PWM output (selectable for each individual pin)
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRC register.
Write to timer	The TRC register can be written to.
Selectable functions	• One to three pins selectable as PWM pins One or more of pins TRCIOB, TRCIOC, and TRCIOD • Active level selectable for each individual pin • Initial level selectable for each individual pin • Buffer operation (Refer to **20.3.2 Buffer Operation**.) • Pulse output forced cutoff signal input (Refer to **20.3.4 Forced Cutoff of Pulse Output**.) • A/D trigger generation

j = B, C, or D
h = A, B, C, or D



Notes:
1. The BFC bit in the TRCMR register is set to 1 (TRCGRC register is used as the buffer register of the TRCGRA register).
2. The BFD bit in the TRCMR register is set to 1 (TRCGRD register is used as the buffer register of the TRCGRB register).

Figure 20.13 Block Diagram of PWM Mode

20.6.1 Timer RC Control Register 1 (TRCCR1) in PWM Mode

Address 0121h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR	TCK2	TCK1	TCK0	TOD	TOC	TOB	TOA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA	TRCIOA output level select bit (1)	Disabled in PWM mode.	R/W
b1	TOB	TRCIOB output level select bit (1, 2)	0: Initial output selected as non-active level 1: Initial output selected as active level	R/W
b2	TOC	TRCIOC output level select bit (1, 2)		R/W
b3	TOD	TRCIOD output level select bit (1, 2)		R/W
b4	TCK0	Count source select bit (1)	b6 b5 b4 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRCCLK input rising edge 1 1 0: fOCO40M 1 1 1: Do not set.	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	CCLR	TRC counter clear select bit	0: Clear disabled (free-running operation) 1: Clear by compare match with the TRCGRA register	R/W

Notes:
1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).
2. If the pin function is set for waveform output (refer to **7.5 Port Settings**), the initial output level is output when the TRCCR1 register is set.

20.6.2 Timer RC Control Register 2 (TRCCR2) in PWM Mode

Address 0130h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCEG1	TCEG0	CSEL	—	—	POLD	POLC	POLB
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POLB	PWM mode output level control bit B (1)	0: TRCIOB output level selected as low active 1: TRCIOB output level selected as high active	R/W
b1	POLC	PWM mode output level control bit C (1)	0: TRCIOC output level selected as low active 1: TRCIOC output level selected as high active	R/W
b2	POLD	PWM mode output level control bit D (1)	0: TRCIOD output level selected as low active 1: TRCIOD output level selected as high active	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b4	—			
b5	CSEL	TRC count operation select bit (2)	0: Count continues at compare match with the TRCGRA register 1: Count stops at compare match with the TRCGRA register	R/W
b6	TCEG0	TRCTRG input edge select bit (3)	b7 b6 0 0: Trigger input from the TRCTRG pin disabled 0 1: Rising edge selected 1 0: Falling edge selected 1 1: Both edges selected	R/W
b7	TCEG1			R/W

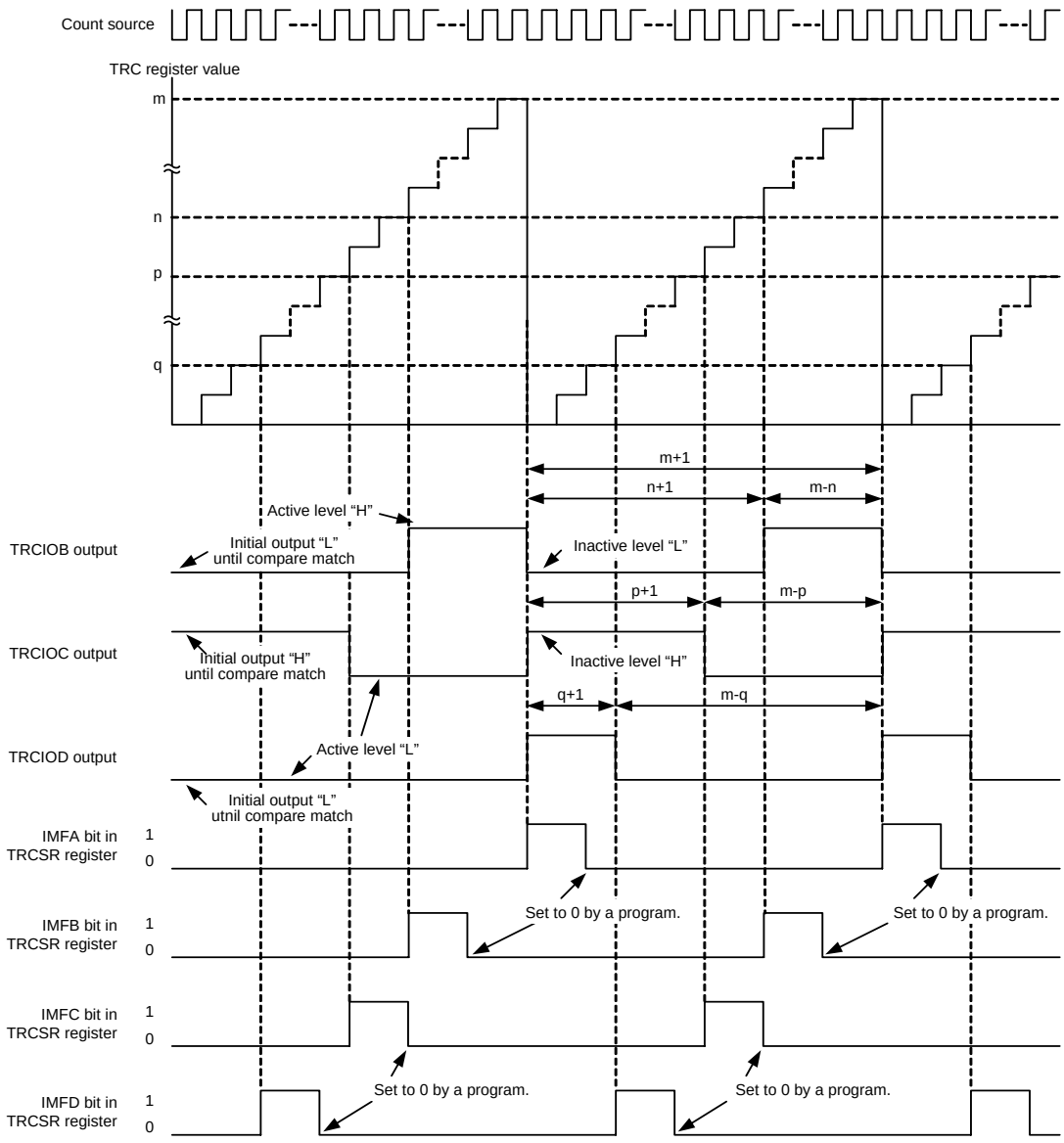
Notes:
1. Enabled when in PWM mode.
2. For notes on PWM2 mode, refer to **20.9.6 TRCMR Register in PWM2 Mode**.
3. In timer mode and PWM mode these bits are disabled.

Table 20.12 Functions of TRCGRh Register in PWM Mode

Register	Setting	Register Function	PWM Output Pin
TRCGRA	–	General register. Set the PWM period.	–
TRCGRB	–	General register. Set the PWM output change point.	TRCIOB
TRCGRC	BFC = 0	General register. Set the PWM output change point.	TRCIOC
TRCGRD	BFD = 0		TRCIOD
TRCGRC	BFC = 1	Buffer register. Set the next PWM period. (Refer to **20.3.2 Buffer Operation**.)	–
TRCGRD	BFD = 1	Buffer register. Set the next PWM output change point. (Refer to **20.3.2 Buffer Operation**.)	TRCIOB

j = A, B, C, or D
BFC, BFD: Bits in TRCMR register
Note:
1. The output level does not change even if a compare match occurs when the TRCGRA register value (PWM period) is the same as the TRCGRB, TRCGRC, or TRCGRD register value.

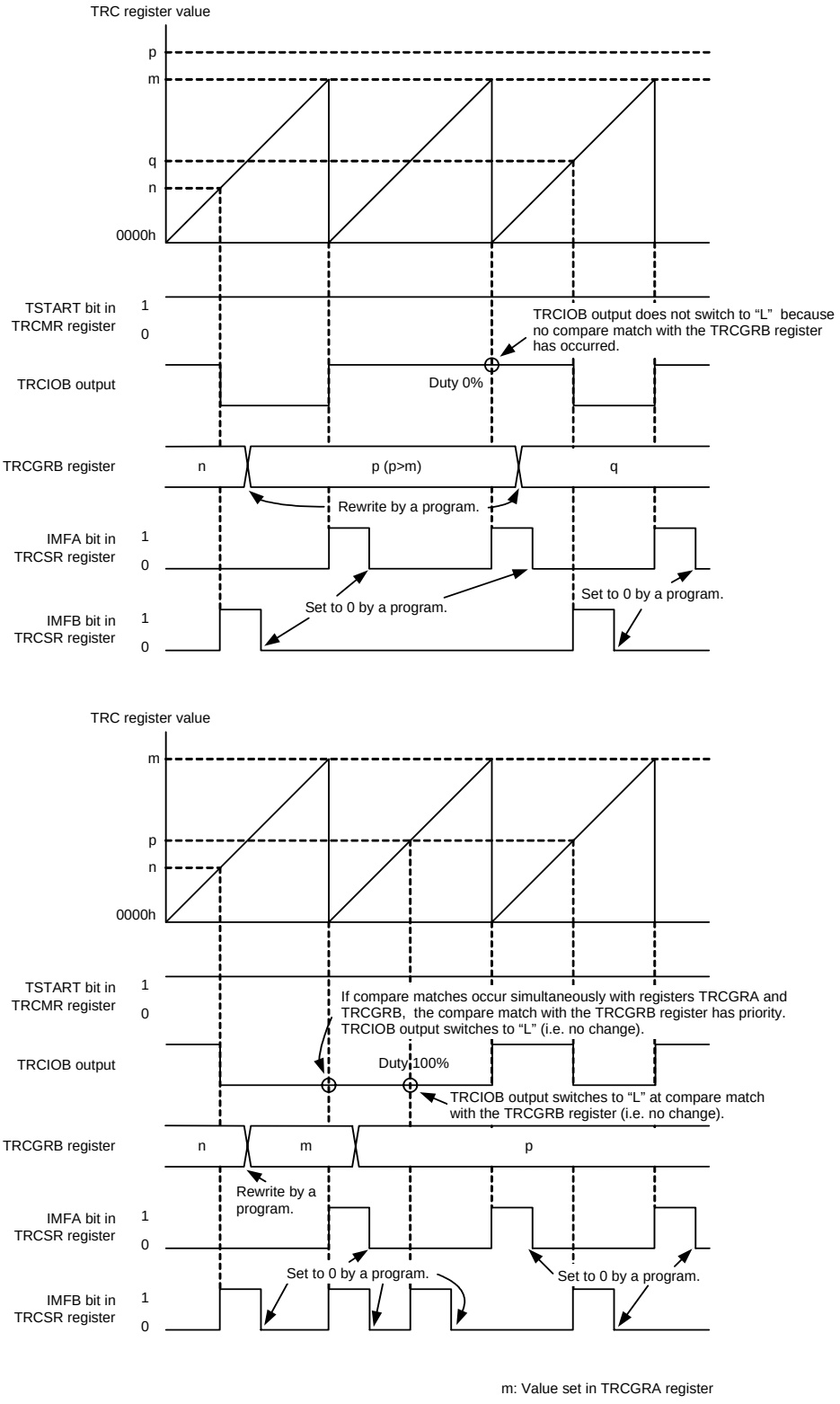
20.6.3 Operating Example



m: Value set in TRCGRA register
n: Value set in TRCGRB register
p: Value set in TRCGRC register
q: Value set in TRCGRD register

The above applies under the following conditions:
- Bits BFC and BFD in the TRCMR register are set to 0 (registers TRCGRC and TRCGRD are not used as buffer registers).
- Bits EB, EC, and ED in the TRCOER register are set to 0 (TRCIOB, TRCIOC, and TRCIOD pin output enabled).
- Bits TOB and TOC in the TRCCR1 register are set to 0 (inactive level) and the TOD bit is set to 1 (active level).
- The POLB bit in the TRCCR2 register is set to 1 (high active), bits POLC and POLD are set to 0 (low active).

Figure 20.14 Operating Example in PWM Mode

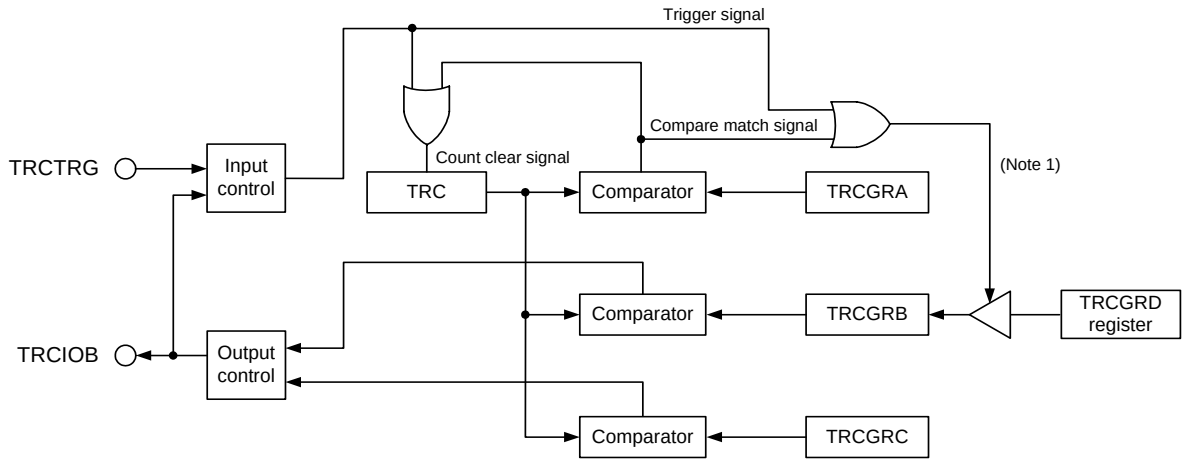


The above applies under the following conditions:
- The EB bit in the TRCOER register is set to 0 (TRCIOB pin output enabled).
- The POLB bit in the TRCCR2 register is set to 0 (low active).

Figure 20.15 Operating Example in PWM Mode (Duty 0% and Duty 100%)

20.7 PWM2 Mode

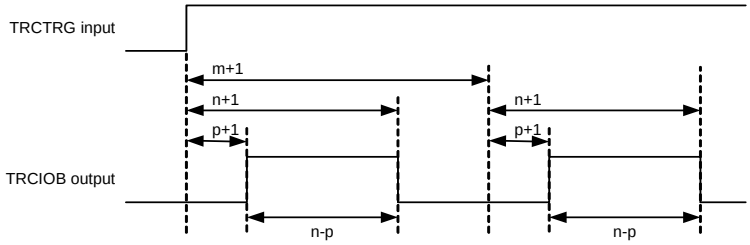
This mode outputs a single PWM waveform. After a given wait time has elapsed following the trigger, the pin output switches to active level. Then, after a given duration, the output switches back to inactive level. Furthermore, the counter stops at the same time the output returns to inactive level, making it possible to use PWM2 mode to output a programmable wait one-shot waveform.
Since timer RC uses multiple general registers in PWM2 mode, other modes cannot be used in conjunction with it. Figure 20.16 shows a Block Diagram of PWM2 Mode, Table 20.13 lists the PWM2 Mode Specifications, Table 20.14 lists the Functions of TRCGRj Register in PWM2 Mode, and Figures 20.17 to 20.19 show Operating Examples in PWM2 Mode.



Note:
1. The BFD bit in the TRCMR register is set to 1 (TRCGRD register is used as the buffer register of the TRCGRB register).

Figure 20.16 Block Diagram of PWM2 Mode

Table 20.13 PWM2 Mode Specifications

Item	Specification
Count source	f1, f2, f4, f8, f32, fOCO40M, fOCO-F External signal input to TRCCLK pin (rising edge)
Count operation	TRC register increment
PWM waveform	PWM period: 1/fk × (m + 1) (no TRCTRG input) Active level width: 1/fk × (n - p) Wait time from count start or trigger: 1/fk × (p + 1) fk: Frequency of count source m: Value set in TRCGRA register n: Value set in TRCGRB register p: Value set in TRCGRC register  (TRCTRG: Rising edge, active level is high)
Count start conditions	• Bits TCEG1 to TCEG0 in the TRCCR2 register are set to 00b (TRCTRG trigger disabled) or the CSEL bit in the TRCCR2 register is set to 0 (count continues). 1 (count starts) is written to the TSTART bit in the TRCMR register. • Bits TCEG1 to TCEG0 in the TRCCR2 register are set to 01b, 10b, or 11b (TRCTRG trigger enabled) and the TSTART bit in the TRCMR register is set to 1 (count starts). A trigger is input to the TRCTRG pin.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRCMR register while the CSEL bit in the TRCCR2 register is set to 0 or 1. The TRCIOB pin outputs the initial level in accordance with the value of the TOB bit in the TRCCR1 register. The TRC register retains the value before the count stops. • The count stops at a compare match with TRCGRA while the CSEL bit in the TRCCR2 register is set to 1 The TRCIOB pin outputs the initial level. The TRC register retains the value before the count stops when the CCLR bit in the TRCCR1 register is set to 0. The TRC register is set to 0000h when the CCLR bit in the TRCCR1 register is set to 1.
Interrupt request generation timing	• Compare match (the contents of the TRC register and the TRCGRj register match.) • TRC register overflow
TRCIOA/TRCTRG pins function	Programmable I/O port or TRCTRG input
TRCIOB pin function	PWM output
TRCIOC/TRCIOD pins function	Programmable I/O port
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRC register.
Write to timer	The TRC register can be written to.
Selectable functions	• External trigger and active edge selection The edge or edges of the signal input to the TRCTRG pin can be used as the PWM output trigger: rising edge, falling edge, or both rising and falling edges • Buffer operation (Refer to **20.3.2 Buffer Operation**.) • Pulse output forced cutoff signal input (Refer to **20.3.4 Forced Cutoff of Pulse Output**.) • Digital filter (Refer to **20.3.3 Digital Filter**.) • A/D trigger generation

j = A, B, or C

20.7.1 Timer RC Control Register 1 (TRCCR1) in PWM2 Mode

Address 0121h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR	TCK2	TCK1	TCK0	TOD	TOC	TOB	TOA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA	TRCIOA output level select bit (1)	Disabled in PWM2 mode.	R/W
b1	TOB	TRCIOB output level select bit (1, 2)	0: Active level is high (Initial output at low High-level output at compare match with the TRCGRC register Low-level output at compare match with the TRCGRB register) 1: Active level is low (Initial output at high Low-level output at compare match with the TRCGRC register High-level output at compare match with the TRCGRB register)	R/W
b2	TOC	TRCIOC output level select bit (1)	Disabled in PWM2 mode.	R/W
b3	TOD	TRCIOD output level select bit (1)		R/W
b4	TCK0	Count source select bit (1)	b6 b5 b4 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRCCLK input rising edge 1 1 0: fOCO40M 1 1 1: Do not set.	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	CCLR	TRC counter clear select bit	0: Clear disabled (free-running operation) 1: Clear by compare match with the TRCGRA register	R/W

Notes:
1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).
2. If the pin function is set for waveform output (refer to **7.5 Port Settings**), the initial output level is output when the TRCCR1 register is set.

Table 20.14 Functions of TRCGRj Register in PWM2 Mode

Register	Setting	Register Function	PWM2 Output Pin
TRCGRA	–	General register. Set the PWM period.	TRCIOB pin
TRCGRB	–	General register. Set the PWM output change point.	
TRCGRC	BFC = 0	General register. Set the PWM output change point (wait time after trigger).	
TRCGRD	BFD = 0	(Not used in PWM2 mode.)	–
TRCGRD	BFD = 1	Buffer register. Set the next PWM output change point. (Refer to **20.3.2 Buffer Operation**.)	TRCIOB pin

j = A, B, C, or D
BFC, BFD: Bits in TRCMR register
Note:
1. Do not set registers TRCGRB and TRCGRC to the same value.

20.7.2 Timer RC Control Register 2 (TRCCR2) in PWM2 Mode

Address 0130h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCEG1	TCEG0	CSEL	—	—	POLD	POLC	POLB
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POLB	PWM mode output level control bit B (1)	0: TRCIOB output level selected as low active 1: TRCIOB output level selected as high active	R/W
b1	POLC	PWM mode output level control bit C (1)	0: TRCIOC output level selected as low active 1: TRCIOC output level selected as high active	R/W
b2	POLD	PWM mode output level control bit D (1)	0: TRCIOD output level selected as low active 1: TRCIOD output level selected as high active	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b4	—			
b5	CSEL	TRC count operation select bit (2)	0: Count continues at compare match with the TRCGRA register 1: Count stops at compare match with the TRCGRA register	R/W
b6	TCEG0	TRCTRG input edge select bit (3)	b7 b6 0 0: Trigger input from the TRCTRG pin disabled 0 1: Rising edge selected 1 0: Falling edge selected 1 1: Both edges selected	R/W
b7	TCEG1			R/W

Notes:
1. Enabled when in PWM mode.
2. For notes on PWM2 mode, refer to **20.9.6 TRCMR Register in PWM2 Mode**.
3. In timer mode and PWM mode, these bits are disabled.

20.7.3 Timer RC Digital Filter Function Select Register (TRCDF) in PWM2 Mode

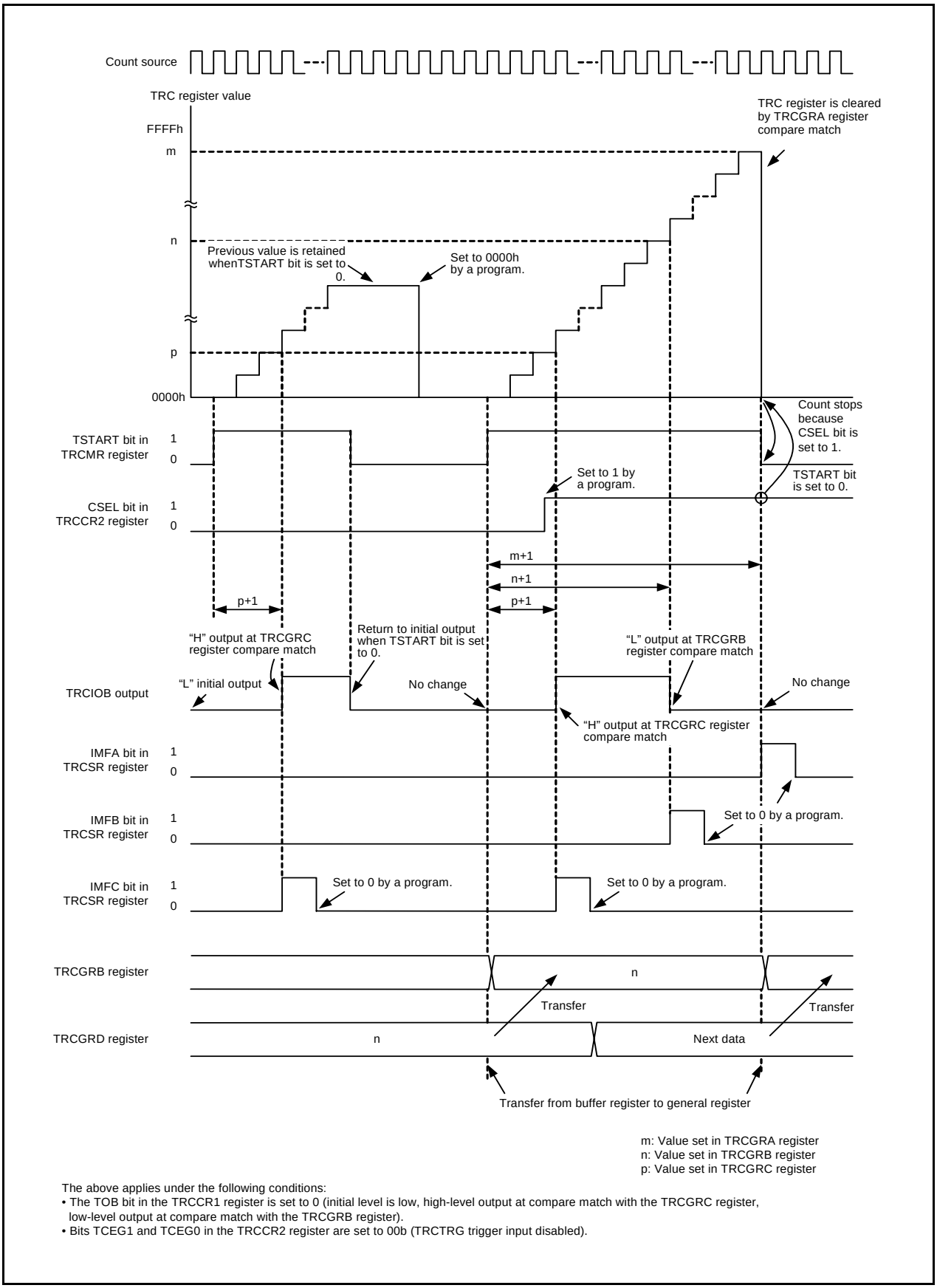
Address 0131h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DFCK1	DFCK0	—	DFTRG	DFD	DFC	DFB	DFA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DFA	TRCIOA pin digital filter function select bit (1)	0: Function is not used 1: Function is used	R/W
b1	DFB	TRCIOB pin digital filter function select bit (1)	0: Function is not used 1: Function is used	R/W
b2	DFC	TRCIOC pin digital filter function select bit (1)	0: Function is not used 1: Function is used	R/W
b3	DFD	TRCIOD pin digital filter function select bit (1)	0: Function is not used 1: Function is used	R/W
b4	DFTRG	TRCTRG pin digital filter function select bit (2)	0: Function is not used 1: Function is used	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	DFCK0	Digital filter function clock select bit (1, 2)	b7 b6 0 0: f32 0 1: f8 1 0: f1 1 1: Count source (clock selected by bits TCK0 to TCK2 in the TRCCR1 register)	R/W
b7	DFCK1			R/W

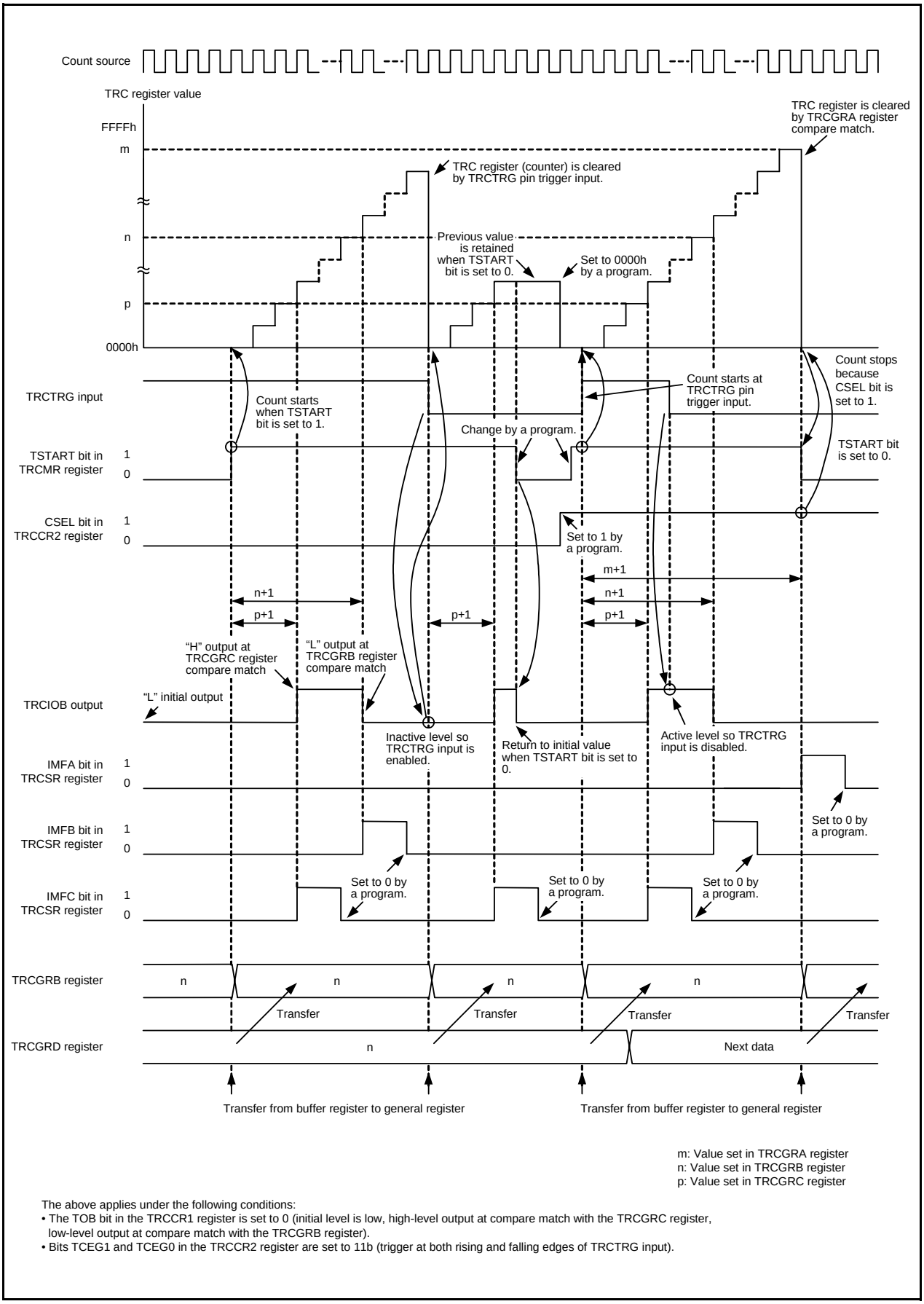
Notes:
1. These bits are enabled for the input capture function.
2. These bits are enabled when in PWM2 mode and bits TCEG1 to TCEG0 in the TRCCR2 register are set to 01b, 10b, or 11b (TRCTRG trigger input enabled).

20.7.4 Operating Example



The above applies under the following conditions:
- The TOB bit in the TRCCR1 register is set to 0 (initial level is low, high-level output at compare match with the TRCGRC register, low-level output at compare match with the TRCGRB register).
- Bits TCEG1 and TCEG0 in the TRCCR2 register are set to 00b (TRCTRG trigger input disabled).

Figure 20.17 Operating Example in PWM2 Mode (TRCTRG Trigger Input Disabled)



The above applies under the following conditions:
- The TOB bit in the TRCCR1 register is set to 0 (initial level is low, high-level output at compare match with the TRCGRC register, low-level output at compare match with the TRCGRB register).
- Bits TCEG1 and TCEG0 in the TRCCR2 register are set to 11b (trigger at both rising and falling edges of TRCTRG input).

Figure 20.18 Operating Example in PWM2 Mode (TRCTRG Trigger Input Enabled)

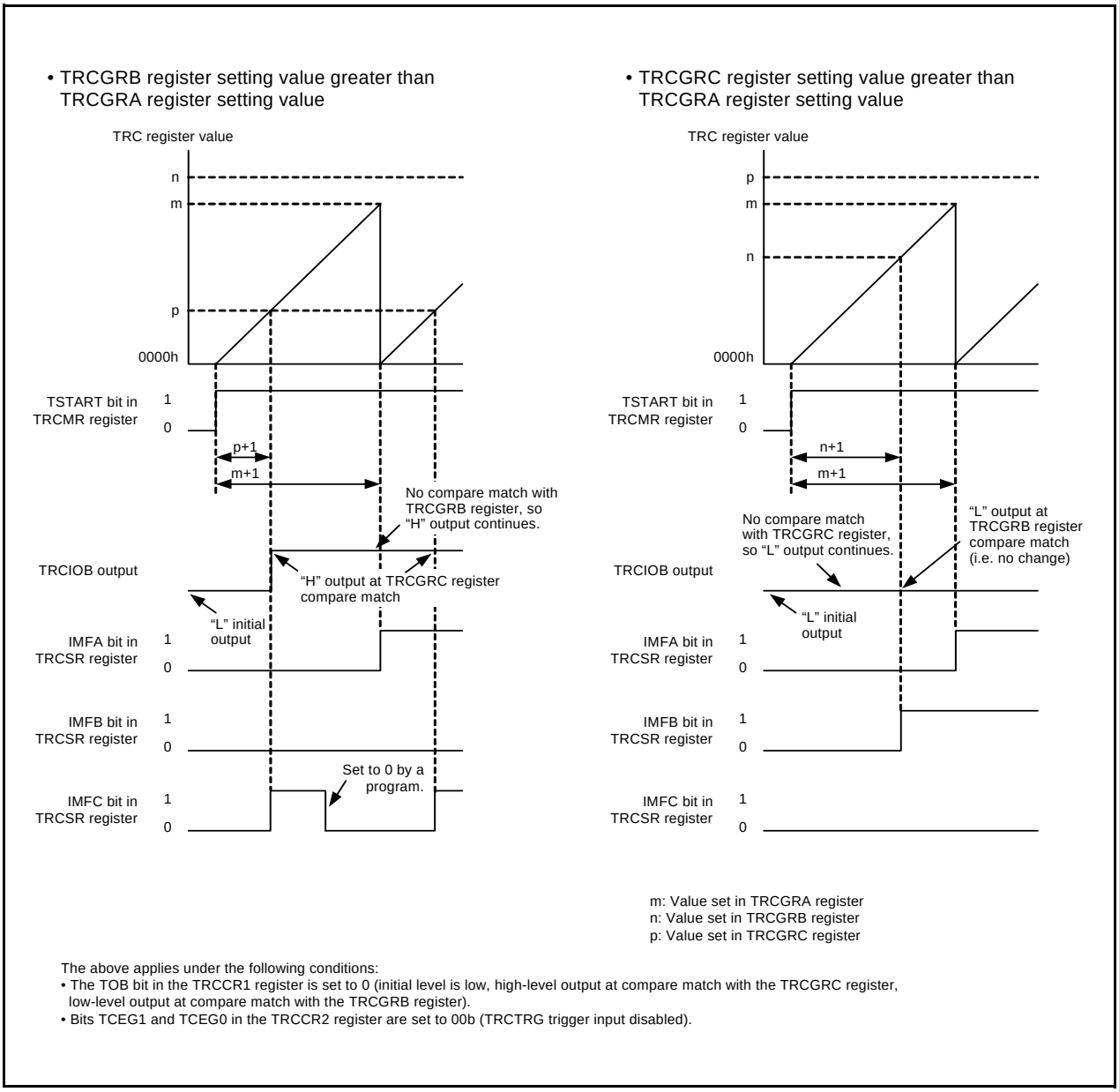


Figure 20.19 Operating Example in PWM2 Mode (Duty 0% and Duty 100%)

20.8 Timer RC Interrupt

Timer RC generates a timer RC interrupt request from five sources. The timer RC interrupt uses the single TRCIC register (bits IR and ILVL0 to ILVL2) and a single vector.
Table 20.15 lists the Registers Associated with Timer RC Interrupt and Figure 20.20 shows a Block Diagram of Timer RC Interrupt.

Table 20.15 Registers Associated with Timer RC Interrupt

Timer RC Status Register	Timer RC Interrupt Enable Register	Timer RC Interrupt Control Register
TRCSR	TRCIER	TRCIC

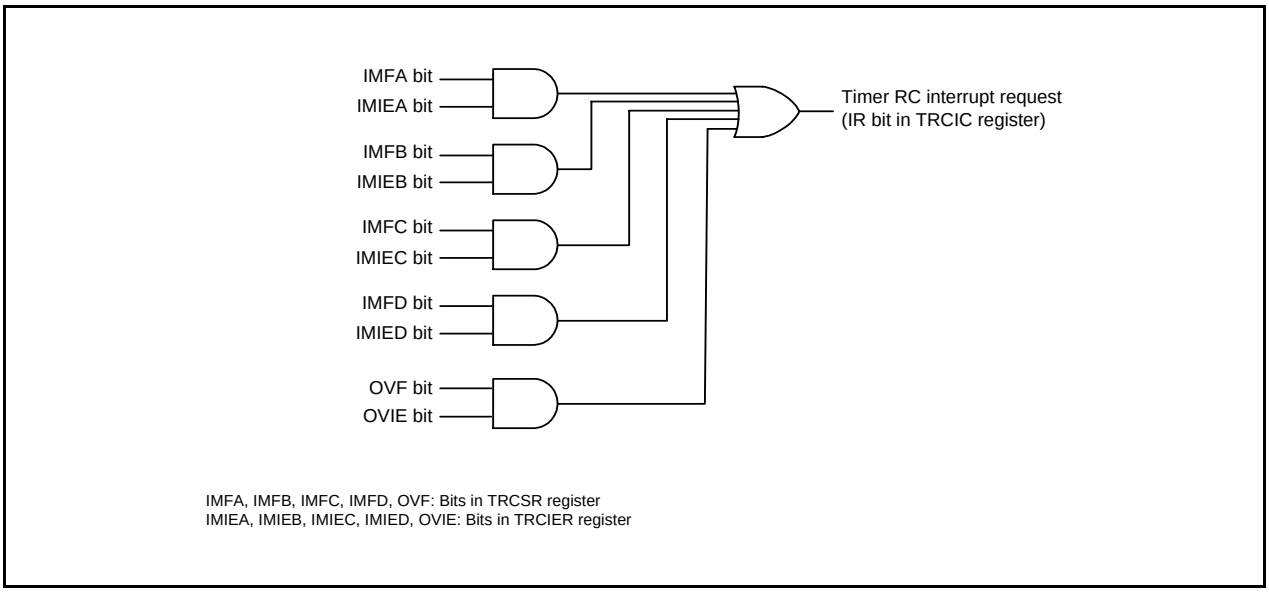


Figure 20.20 Block Diagram of Timer RC Interrupt

Like other maskable interrupts, the timer RC interrupt is controlled by the combination of the I flag, IR bit, bits ILVL0 to ILVL2, and IPL. However, it differs from other maskable interrupts in the following respects because a single interrupt source (timer RC interrupt) is generated from multiple interrupt request sources.

- The IR bit in the TRCIC register is set to 1 (interrupt requested) when a bit in the TRCSR register is set to 1 and the corresponding bit in the TRCIER register is also set to 1 (interrupt enabled).
- The IR bit is set to 0 (no interrupt requested) when the bit in the TRCSR register or the corresponding bit in the TRCIER register is set to 0, or both are set to 0. In other words, the interrupt request is not maintained if the IR bit is once set to 1 but the interrupt is not acknowledged.
- If another interrupt source is triggered after the IR bit is set to 1, the IR bit remains set to 1 and does not change.
- If multiple bits in the TRCIER register are set to 1, use the TRCSR register to determine the source of the interrupt request.
- The bits in the TRCSR register are not automatically set to 0 when an interrupt is acknowledged. Set them to 0 within the interrupt routine. Refer to **20.2.5 Timer RC Status Register (TRCSR)**, for the procedure for setting these bits to 0.

Refer to **20.2.4 Timer RC Interrupt Enable Register (TRCIER)**, for details of the TRCIER register.
Refer to **12.3 Interrupt Control**, for details of the TRCIC register and **12.1.5.2 Relocatable Vector Tables**, for information on interrupt vectors.

20.9 Notes on Timer RC

20.9.1 TRC Register

- The following note applies when the CCLR bit in the TRCCR1 register is set to 1 (TRC register cleared by compare match with TRCGRA register).
  When using a program to write a value to the TRC register while the TSTART bit in the TRCMR register is set to 1 (count starts), ensure that the write does not overlap with the timing with which the TRC register is set to 0000h.
  If the timing of the write to the TRC register and the setting of the TRC register to 0000h coincide, the write value will not be written to the TRC register and the TRC register will be set to 0000h.

- Reading from the TRC register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```
Program Example     MOV.W   #XXXXh, TRC     ;Write
                    JMP.B   L1              ;JMP.B instruction
                L1: MOV.W   TRC,DATA        ;Read
```

20.9.2 TRCSR Register

Reading from the TRCSR register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```
Program Example     MOV.B   #XXh, TRCSR     ;Write
                    JMP.B   L1              ;JMP.B instruction
                L1: MOV.B   TRCSR,DATA      ;Read
```

20.9.3 TRCCR1 Register

To set bits TCK2 to TCK0 in the TRCCR1 register to 111b (fOCO-F), set fOCO-F to the clock frequency higher than the CPU clock frequency.

20.9.4 Count Source Switching

- Stop the count before switching the count source.

Switching procedure
(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.

- After switching the count source from fOCO40M to another clock, allow two or more cycles of f1 to elapse after changing the clock setting before stopping fOCO40M.

Switching procedure
(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.
(3) Wait for two or more cycles of f1.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

20.9.5 Input Capture Function

- The pulse width of the input capture signal should be set to three cycles or more of the timer RC operation clock (refer to **Table 20.1 Timer RC Operating Clocks**).
- The value of the TRC register is transferred to the TRCGRj register one or two cycles of the timer RC operation clock after the input capture signal is input to the TRCIOj (j = A, B, C, or D) pin (when the digital filter function is not used).

20.9.6 TRCMR Register in PWM2 Mode

When the CSEL bit in the TRCCR2 register is set to 1 (count stops at compare match with the TRCGRA register), do not set the TRCMR register at compare match timing of registers TRC and TRCGRA.

21. Timer RD

Timer RD has two 16-bit timers (timer RD0 and timer RD1).

21.1 Introduction

Timer RDi (i = 0 or 1) has four I/O pins.
Timer RD uses either f1 or fOCO40M as its operating clock. Table 21.1 lists the Timer RD Operating Clocks.

Table 21.1 Timer RD Operating Clocks

Condition	Timer RD Operating Clock
The count source is f1, f2, f4, f8, f32, fC2, or TRDCLK input. (Bits TCK2 to TCK0 in registers TRDCR0 and TRDCR1 are set to 000b to 101b.)	f1
The count source is fOCO40M. (Bits TCK2 to TCK0 in registers TRDCR0 and TRDCR1 are set to 110b.)	fOCO40M

Figure 21.1 shows the Timer RD Block Diagram, and Table 21.2 lists the Timer RD Pin Configuration.

Timer RD supports the following five modes:

- Timer mode
  - Input capture function — The counter value is transferred to a register with an external signal as the trigger.
  - Output compare function — A match between the values of a counter and a register is detected. (Pin output can be changed at detection.)

The following four modes use the output compare function:

- PWM mode — Pulse of any width are continuously.
- Reset synchronous PWM mode — Three-phase waveforms (6) without sawtooth wave modulation and dead time are output.
- Complementary PWM mode — Three-phase waveforms (6) with triangular wave modulation and dead time are output.
- PWM3 mode — PWM waveforms (2) with a fixed period are output.

For the input capture function, the output compare function, and in PWM mode, timer RD0 and timer RD1 have the equivalent functions, and functions or modes can be selected individually for each pin. Also, a combination of these functions and modes can be used in timer RDi.
In reset synchronous PWM mode, complementary PWM mode, and PWM3 mode, a waveform is output with a combination of counters and registers in timer RD0 and timer RD1.

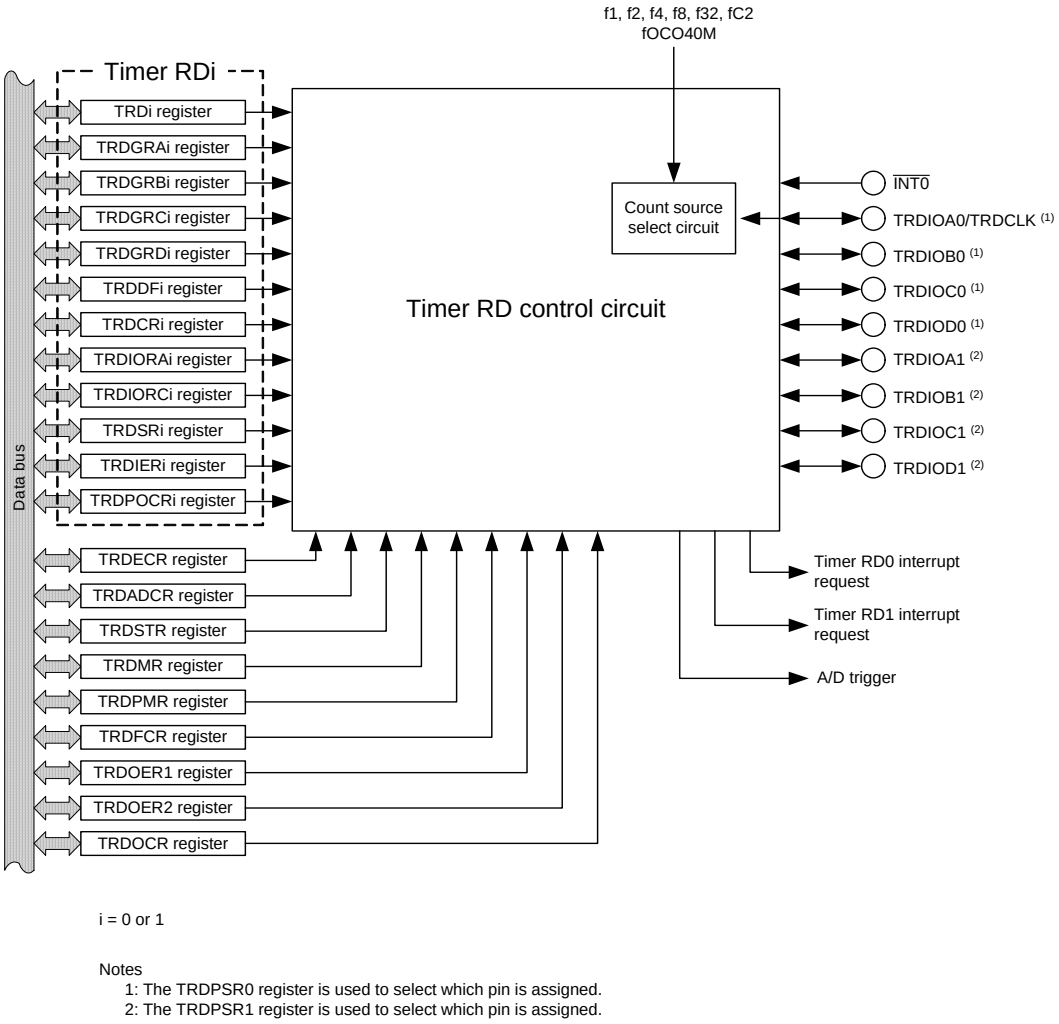


Figure 21.1 Timer RD Block Diagram

Table 21.2 Timer RD Pin Configuration

Pin Name	Assigned Pin	I/O	Function
TRDIOA0/TRDCLK	P6_0 or P10_0	I/O	Function varies according to the mode. Refer to descriptions of individual modes for details.
TRDIOB0	P6_1 or P10_1	I/O	
TRDIOC0	P6_2 or P10_2	I/O	
TRDIOD0	P6_3 or P10_3	I/O	
TRDIOA1	P6_4 or P10_4	I/O	
TRDIOB1	P6_5 or P10_5	I/O	
TRDIOC1	P6_6 or P10_6	I/O	
TRDIOD1	P6_7 or P10_7	I/O	

21.2 Common Items for Multiple Modes

21.2.1 Count Sources

The count source selection method is the same in all modes. However, the external clock cannot be selected in PWM3 mode.

Table 21.3 Count Source Selection

Count Source	Selection
f1, f2, f4, f8, f32	The count source is selected by bits TCK0 to TCK2 in the TRDCRi register.
fOCO40M (1)	The FRA00 bit in the FRA0 register is set to 1 (high-speed on-chip oscillator on). Bits TCK2 to TCK0 in the TRDCRi register is set to 110b (fOCO40M).
fC2	Bits TCK2 to TCK0 in the TRDCRi register is set to 101b (TRDCLKi input or fC2) The ITCLKi bit in the TRDECR register is set to 1 (fC2)
External signal input to TRDCLK pin	The STCLK bit in the TRDFCR register is set to 1 (external clock input enabled). Bits TCK2 to TCK0 in the TRDCRi register are set to 101b (count source: external clock). The active edge is selected by bits CKEG0 and CKEG1 in the TRDCRi register. The PD2_0 bit in the PD2 register is set to 0 (input mode).

i = 0 or 1

Note:

1. The count source fOCO40M can be used with VCC = 3.0 to 5.5 V.

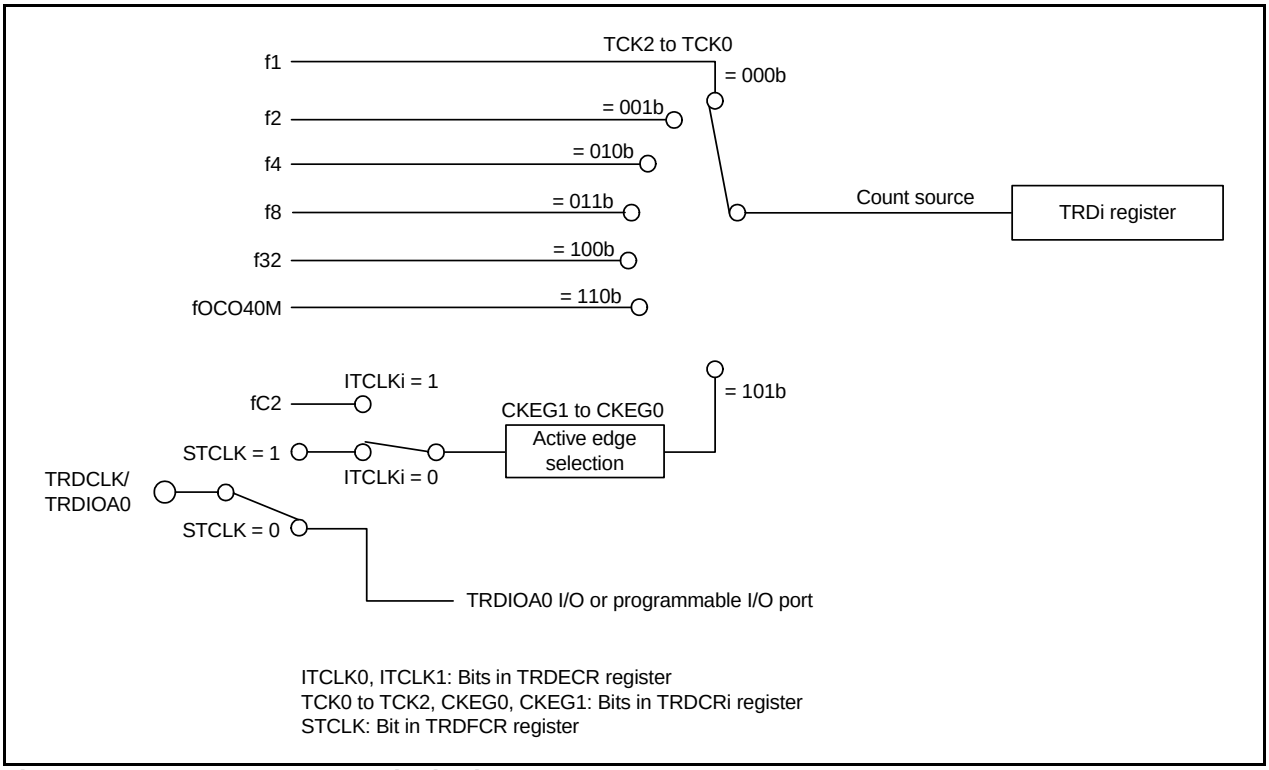


Figure 21.2 Count Source Block Diagram

The pulse width of the external clock input to the TRDCLK pin should be set to three or more cycles of the timer RD operating clock. (See **Table 21.1 Timer RD Operating Clocks**.)

To select fOCO40M or fOCO-F as the count source, set the FRA00 bit in the FRA0 register to 1 (high-speed on-chip oscillator on) before setting bits TCK2 to TCK0 in the TRDCRi register (i = 0 or 1) to 110b (fOCO40M).

21.2.2 Buffer Operation

The TRDGRCi (i = 0 or 1) register can be used as the buffer register of the TRDGRAi register, and the TRDGRDi register can be used as the buffer register of the TRDGRBi register by means of bits BFCi and BFDi in the TRDMR register.

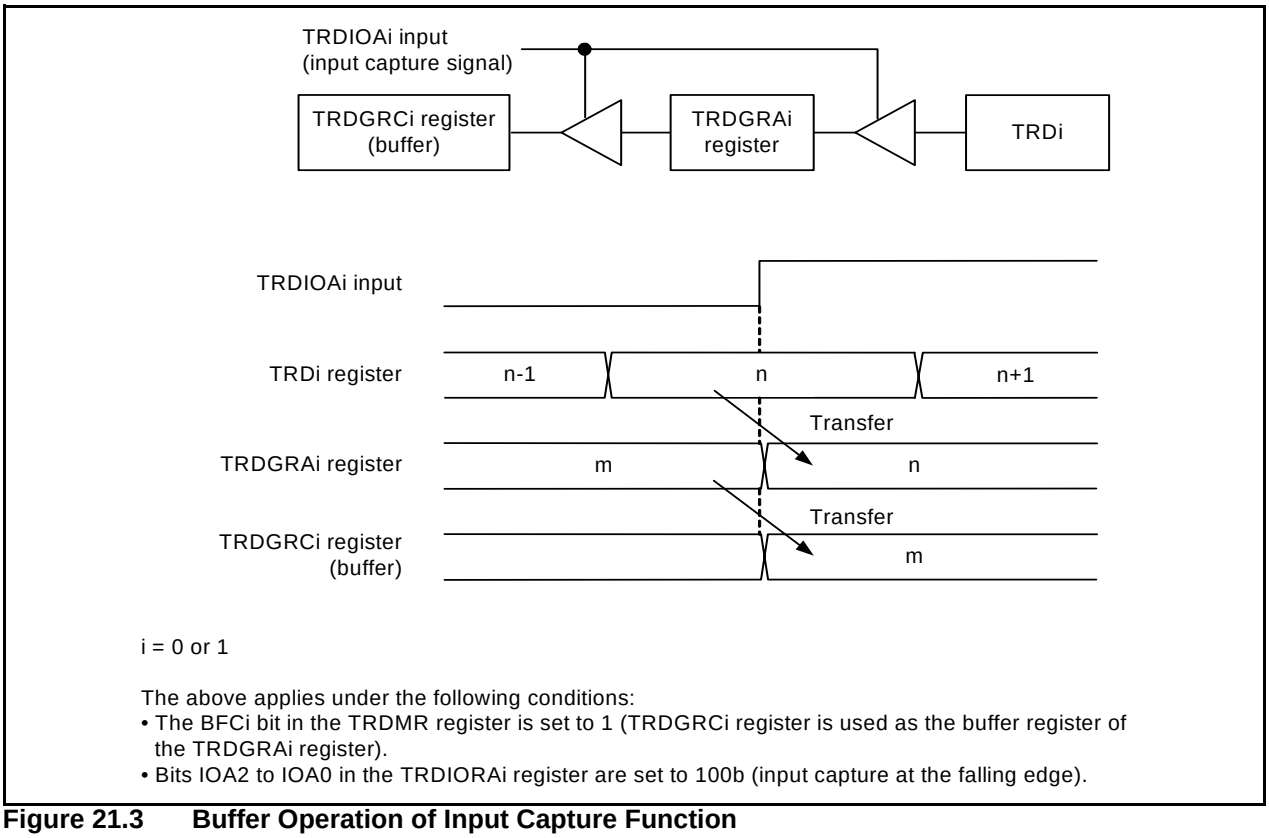
- Buffer register of TRDGRAi: TRDGRCi register
- Buffer register of TRDGRBi: TRDGRDi register

Buffer operation depends on the mode.
Table 21.4 lists the Buffer Operation in Each Mode.

Table 21.4 Buffer Operation in Each Mode

Function and Mode	Transfer Timing	Transfer Register
Input capture function	Input capture signal input	The content of the TRDGRAi (TRDGRBi) register is transferred to the buffer register.
Output compare function PWM mode	Compare match between the TRDi register and the TRDGRAi (TRDGRBi) register	The content of the buffer register is transferred to the TRDGRAi (TRDGRBi) register.
Reset synchronous PWM mode	Compare match between the TRD0 register and the TRDGRA0 register	The content of the buffer register is transferred to the TRDGRAi (TRDGRBi) register.
Complementary PWM mode	• Compare match between the TRD0 register and the TRDGRA0 register • TRD1 register underflow	The content of the buffer register is transferred to registers TRDGRB0, TRDGRA1, and TRDGRB1.
PWM3 mode	Compare match between the TRD0 register and the TRDGRA0 register	The content of the buffer register is transferred to registers TRDGRA0, TRDGRB0, TRDGRA1, and TRDGRB1.

i = 0 or 1



i = 0 or 1

The above applies under the following conditions:
- The BFCi bit in the TRDMR register is set to 1 (TRDGRCi register is used as the buffer register of the TRDGRAi register).
- Bits IOA2 to IOA0 in the TRDIORAi register are set to 100b (input capture at the falling edge).

Figure 21.3 Buffer Operation of Input Capture Function

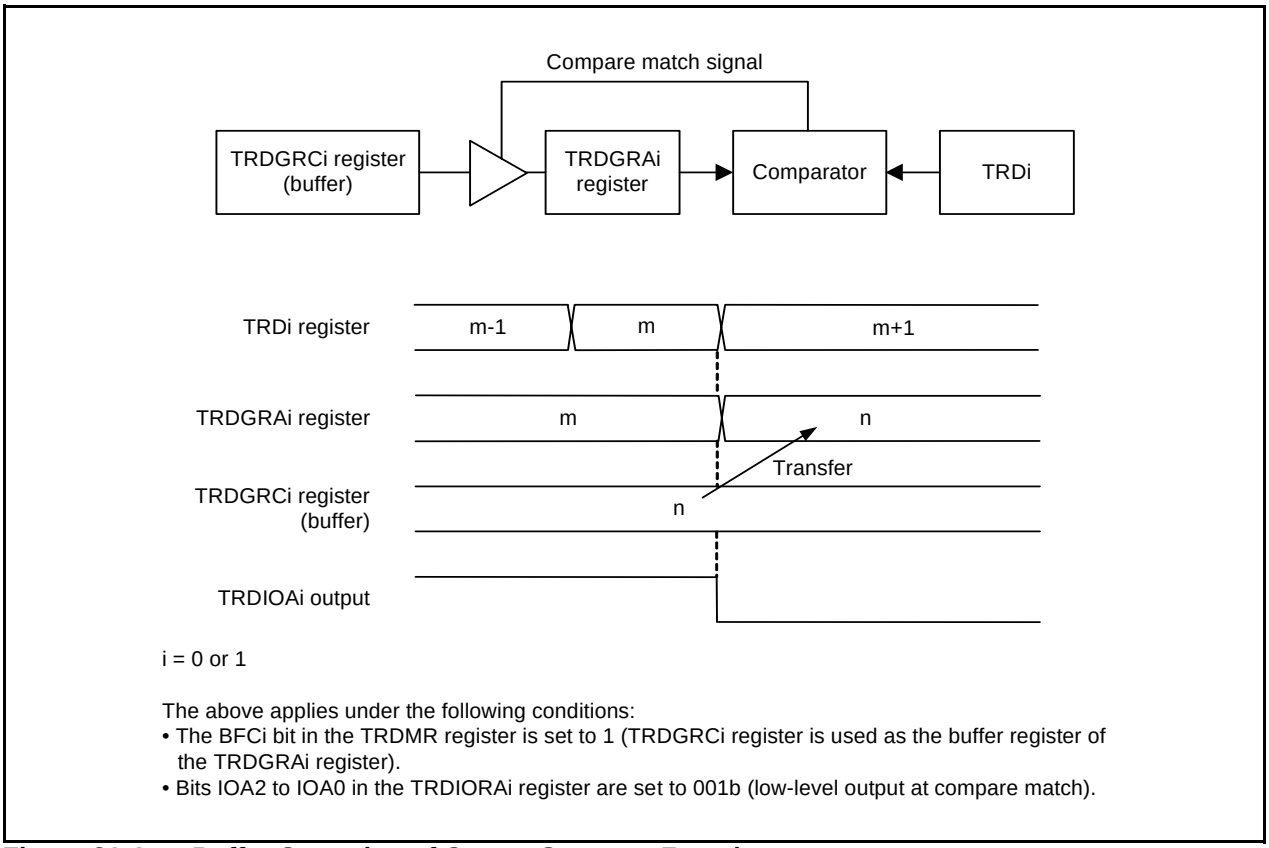


Figure 21.4 Buffer Operation of Output Compare Function

Perform the following in timer mode (input capture and output compare functions).
To use the TRDGRCi (i = 0 or 1) register as the buffer register of the TRDGRAi register:
- Set the IOC3 bit in the TRDIORCi register to 1 (general register or buffer register).
- Set the IOC2 bit in the TRDIORCi register to the same value as the IOA2 bit in the TRDIORAi register.

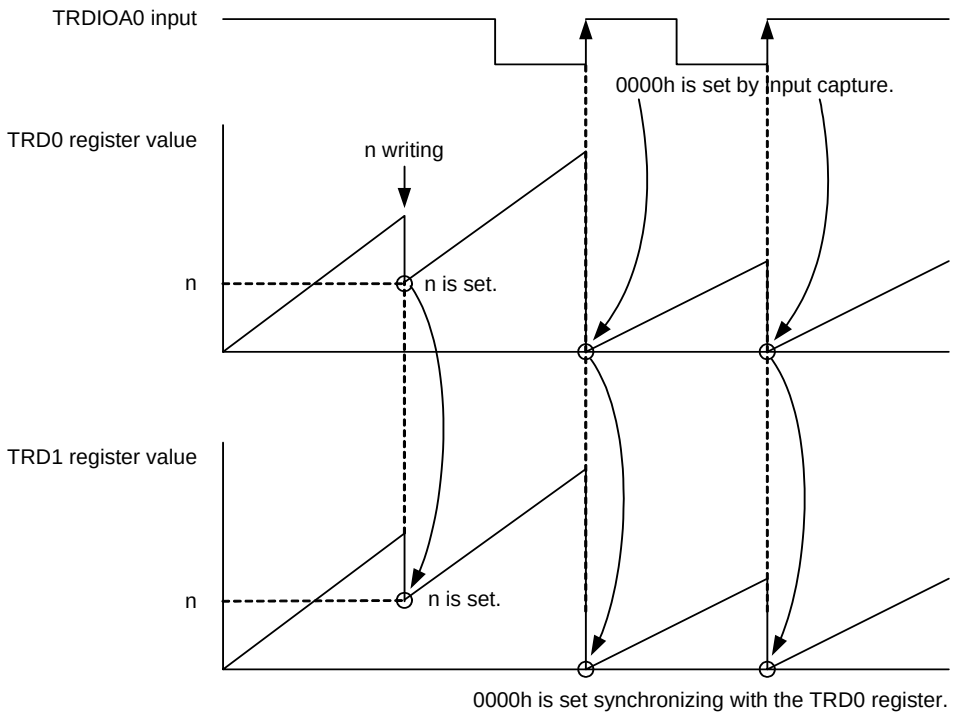
To use the TRDGRDi register as the buffer register of the TRDGRBi register:
- Set the IOD3 bit in the TRDIORDi register to 1 (general register or buffer register).
- Set the IOD2 bit in the TRDIORCi register to the same value as the IOB2 bit in the TRDIORAi register.

For the input capture function, bits IMFC and IMFD in the TRDSRi register are set to 1 at the input edge of the TRDIOCi pin when registers TRDGRCi and TRDGRDi are also used as buffer registers.
For the output compare function, in reset synchronous PWM mode, complementary PWM mode, and PWM3 mode, bits IMFC and IMFD in the TRDSRi register are set to 1 by a compare match with the TRDi register when registers TRDGRCi and TRDGRDi are also as buffer registers.

21.2.3 Synchronous Operation

The TRD1 register is synchronized with the TRD0 register.

- Synchronous preset
  When the SYNC bit in the TRDMR register is set to 1 (synchronous operation), the data is written to both the TRD0 and TRD1 registers after writing to the TRDi register.
- Synchronous clear
  When the SYNC bit in the TRDMR register is set to 1 and bits CCLR2 to CCLR0 in the TRDCRi register are set to 011b (synchronous clear), the TRD0 register is set to 0000h at the same time as the TRD1 register is set to 0000h.
  Also, when the SYNC bit in the TRDMR register is set to 1 and bits CCLR2 to CCLR0 in the TRDCRi register are set to 011b (synchronous clear), the TRD1 register is set to 0000h at the same time as the TRD0 register is set to 0000h.



The above applies under the following conditions:

- The SYNC bit in the TRDMR register is set to 1 (synchronous operation).
- Bits CCLR2 to CCLR0 in the TRDCR0 register are set to 001b (TRD0 register is set to 0000h by input capture).
  Bits CCLR2 to CCLR0 in the TRDCR1 register are set to 011b (TRD1 register is set to 0000h synchronizing with the TRD0 register).
- Bits IOA2 to IOA0 in the TRDIORA0 register are set to 100b.
- Bits CMD1 to CMD0 in the TRDFCR register are set to 00b.
  The PWM 3 bit in the TRDFCR register is set to 1.

} (Input capture at the rising edge of the TRDIOA0 input)

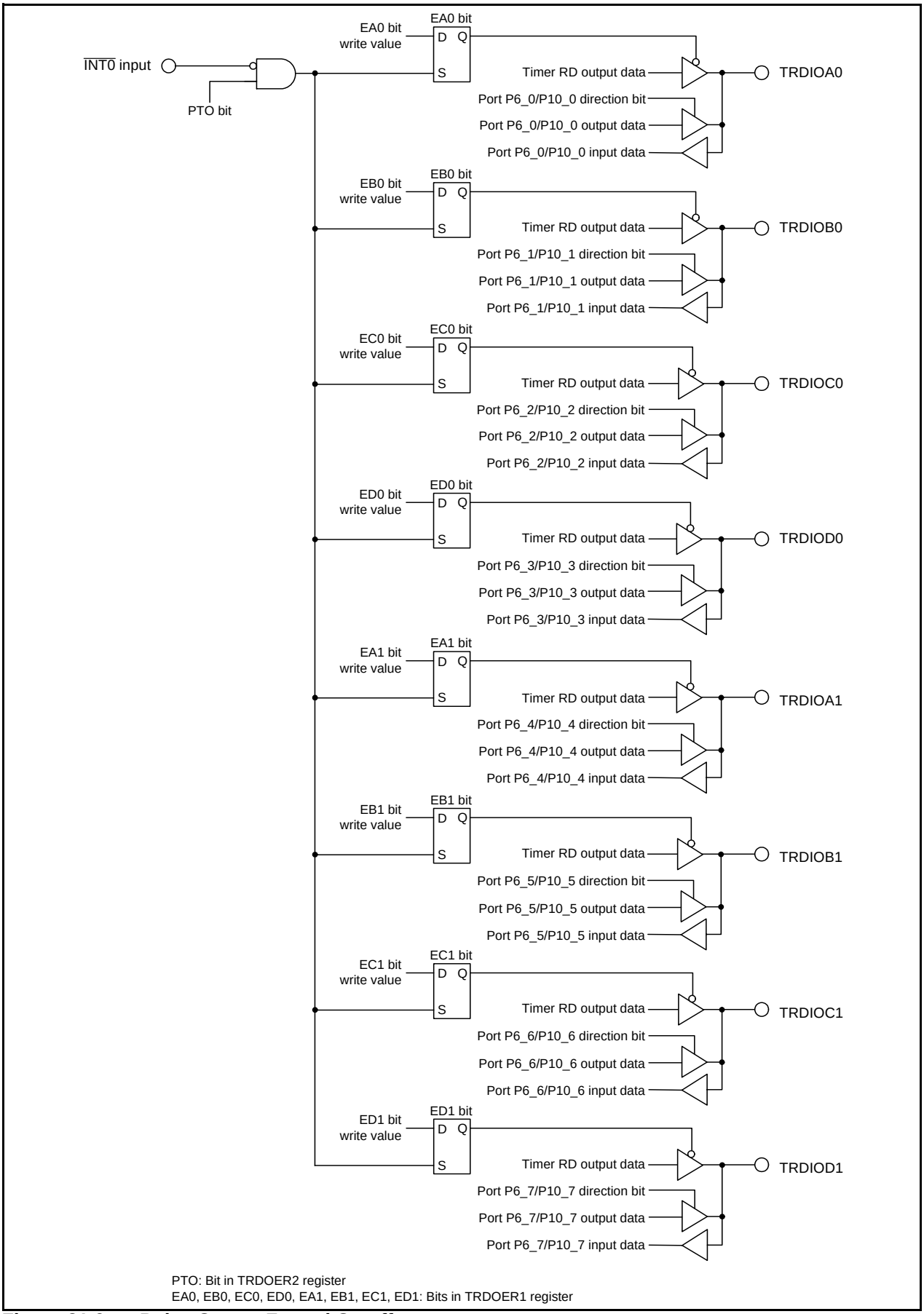
Figure 21.5 Synchronous Operation

21.2.4 Pulse Output Forced Cutoff

In the output compare function, PWM mode, reset synchronous PWM mode, complementary PWM mode, and PWM3 mode, the TRDIOji (i = 0 or 1, j = either A, B, C, or D) output pin can be forcibly set to a programmable I/O port by the $\overline{\text{INT0}}$ pin input, and pulse output can be cut off.
The pins used for output in the above function or modes can function as the output pin of timer RD when the applicable bit in the TRDOER1 register is set to 0 (timer RD output enabled). When the PTO bit in the TRDOER2 register to 1 (pulse output forced cutoff signal input $\overline{\text{INT0}}$ enabled), all bits in the TRDOER1 register are set to 1 (timer RD output disabled, TRDIOji output pin functions as a programmable I/O port) after a low-level signal is applied to the $\overline{\text{INT0}}$ pin. The TRDIOji output pin is set to a programmable I/O port after a low-level signal is applied to the $\overline{\text{INT0}}$ pin and waiting for one or two cycles of the timer RD operating clock (refer to **Table 21.1 Timer RD Operating Clocks**).

Set the following to use this function:
- Set the pin status (high impedance, low-level, or high-level output) to pulse output forced cutoff by registers P2 and PD2.
- Set the INT0EN bit in the INTEN register to 1 ($\overline{\text{INT0}}$ input enabled) and the INT0PL bit to 0 (one edge).
- Set the PD4_5 bit in the PD4 register to 0 (input mode).
- Set the $\overline{\text{INT0}}$ digital filter by bits INT0F0 and INT0F1 in the INTF register.
- Set the PTO bit in the TRDOER2 register to 1 (pulse output forced cutoff signal input $\overline{\text{INT0}}$ enabled).

According to the selection of the POL bit in the INT0IC register and change of the $\overline{\text{INT0}}$ pin input, the IR bit in the INT0IC register is set to 1 (interrupt requested). Refer to **12. Interrupts** for details of interrupts.



PTO: Bit in TRDOER2 register
EA0, EB0, EC0, ED0, EA1, EB1, EC1, ED1: Bits in TRDOER1 register

Figure 21.6 Pulse Output Forced Cutoff

21.3 Input Capture Function

The input capture function measures the external signal width and period. The content of the TRDi register (counter) is transferred to the TRDGRji register as a trigger of the TRDIOji (i = 0 or 1, j = either A, B, C, or D) pin external signal (input capture). Since this function is enabled with a combination of the TRDIOji pin and TRDGRji register, the input capture function, or any other mode or function, can be selected for each individual pin.
The TRDGRA0 register can also select the fOCO128 signal as input-capture trigger input.
Figure 21.7 shows a Block Diagram of Input Capture Function, Table 21.5 lists the Input Capture Function Specifications. Figure 21.8 shows an Operating Example of Input Capture Function.

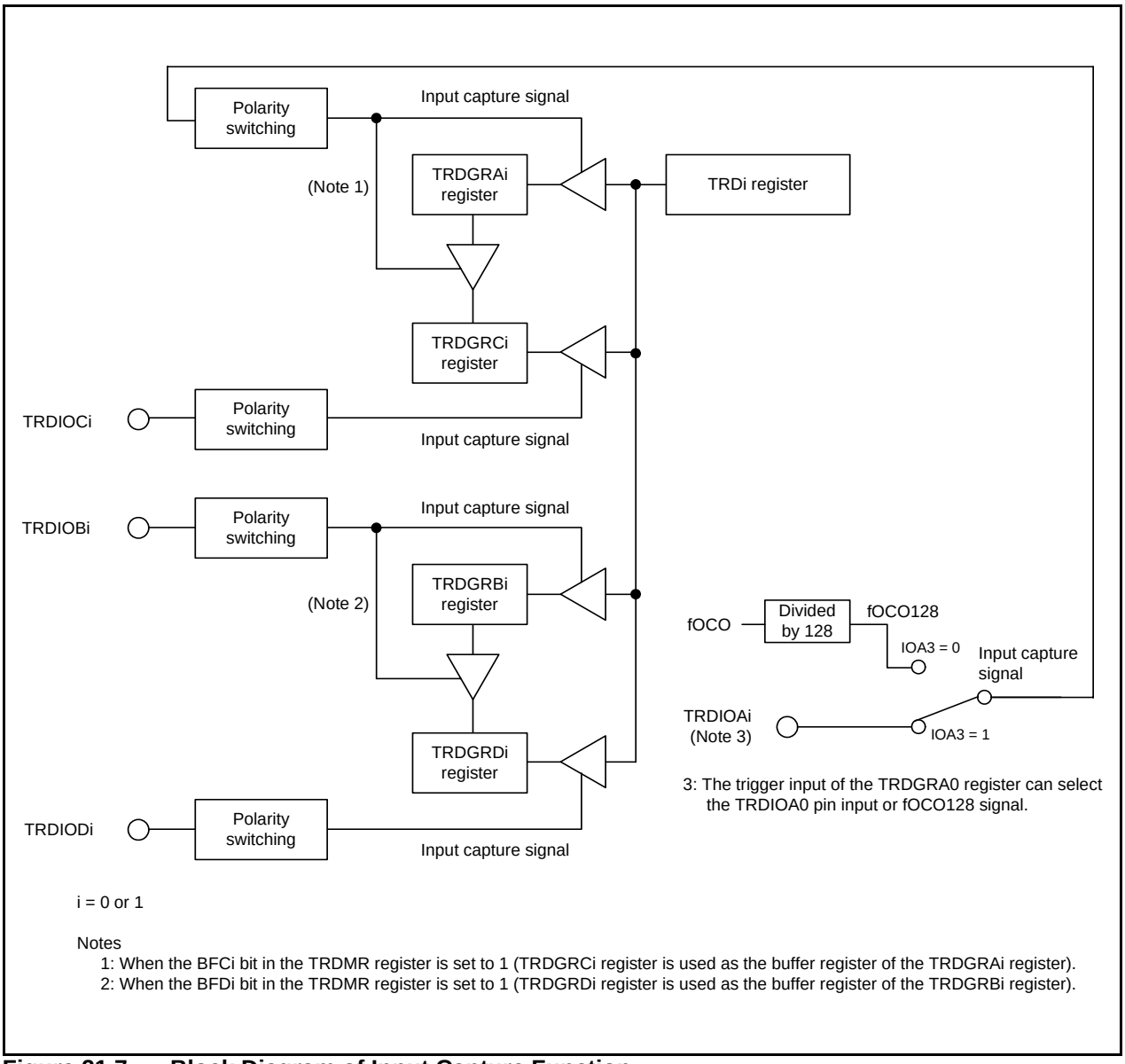


Figure 21.7 Block Diagram of Input Capture Function

Table 21.5 Input Capture Function Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, fC2, fOCO40M External signal input to the TRDCLK pin (active edge selectable by a program)
Count operations	Increment
Count period	When bits CCLR2 to CCLR0 in the TRDCRi register are set to 000b (free-running operation). 1/fk × 65,536 fk: Frequency of count source
Count start condition	1 (count starts) is written to the TSTARTi bit in the TRDSTR register.
Count stop condition	0 (count stops) is written to the TSTARTi bit in the TRDSTR register when the CSELi bit in the TRDSTR register is set to 1.
Interrupt request generation timing	• Input capture (active edge of the TRDIOji input or fOCO128 signal edge) • TRDi register overflows
TRDIOA0 pin function	Programmable I/O port, input-capture input, or TRDCLK (external clock) input
TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1 to TRDIOD1 pins function	Programmable I/O port, or input-capture input (selectable for each individual pin)
$\overline{\text{INT0}}$ pin function	Programmable I/O port or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRDi register.
Write to timer	• When the SYNC bit in the TRDMR register is set to 0 (timer RD0 and timer RD1 operate independently). Data can be written to the TRDi register. • When the SYNC bit in the TRDMR register is set to 1 (timer RD0 and timer RD1 operate synchronously). Data can be written to both the TRD0 and TRD1 registers by writing to the TRDi register.
Selectable functions	• Input-capture input pin selection Either one pin or multiple pins among TRDIOAi, TRDIOBi, TRDIOCi, or TRDIODi. • Input-capture input active edge selection The rising edge, falling edge, or both the rising and falling edges • Timing for setting the TRDi register to 0000h Overflow or input capture • Buffer operation (Refer to **21.2.2 Buffer Operation.**) • Synchronous operation (Refer to **21.2.3 Synchronous Operation.**) • Digital filter The TRDIOji input is sampled and the level is determined when the sampled input level match as three times. • Input-capture trigger selection fOCO128 can be selected for input-capture trigger input of the TRDGRA0 register.

i = 0 or 1, j = either A, B, C, or D

21.3.1 Module Standby Control Register (MSTCR)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	MSTTRG	MSTTRC	MSTTRD	MSTIIC	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	MSTIIC	SSU, I2C bus standby bit	0: Active 1: Standby (1)	R/W
b4	MSTTRD	Timer RD standby bit	0: Active 1: Standby (2)	R/W
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (3)	R/W
b6	MSTTRG	Timer RG standby bit	0: Active 1: Standby (4)	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. When the MSTIIC bit is set to 1 (standby), any access to the SSU or the I2C bus associated registers (addresses 0193h to 019Dh) is disabled.
2. When the MSTTRD bit is set to 1 (standby), any access to the timer RD associated registers (addresses 0135h to 015Fh) is disabled.
3. When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0133h) is disabled.
4. When the MSTTRG bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0170h to 017Fh) is disabled.

21.3.2 Timer RD Control Expansion Register (TRDECR)

Address 0135h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ITCLK1	—	—	—	ITCLK0	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	ITCLK0	Timer RD0 fC2 select bit	0: TRDCLK input selected 1: fC2 selected	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	ITCLK1	Timer RD1 fC2 select bit	0: TRDCLK input selected 1: fC2 selected	R/W

21.3.3 Timer RD Start Register (TRDSTR) for Input Capture Function

Address 0137h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	CSEL1	CSEL0	TSTART1	TSTART0
After Reset	1	1	1	1	1	1	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART0	TRD0 count start flag	0: Count stops 1: Count starts	R/W
b1	TSTART1	TRD1 count start flag		R/W
b2	CSEL0	TRD0 count operation select bit	Set to 1 for the input capture function.	R/W
b3	CSEL1	TRD1 count operation select bit		R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	—			

Set the TRDSTR register using the MOV instruction (do not use the bit handling instruction). Refer to **21.10.1 TRDSTR Register** for **Notes on Timer RD**.

21.3.4 Timer RD Mode Register (TRDMR) for Input Capture Function

Address 0138h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BFD1	BFC1	BFD0	BFC0	—	—	—	SYNC
After Reset	0	0	0	0	1	1	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	SYNC	Timer RD synchronous bit	0: Registers TRD0 and TRD1 operate independently 1: Registers TRD0 and TRD1 operate synchronously	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b2	—			
b3	—			
b4	BFC0	TRDGRC0 register function select bit	0: General register 1: Buffer register of TRDGRA0 register	R/W
b5	BFD0	TRDGRD0 register function select bit	0: General register 1: Buffer register of TRDGRB0 register	R/W
b6	BFC1	TRDGRC1 register function select bit	0: General register 1: Buffer register of TRDGRA1 register	R/W
b7	BFD1	TRDGRD1 register function select bit	0: General register 1: Buffer register of TRDGRB1 register	R/W

21.3.5 Timer RD PWM Mode Register (TRDPMR) for Input Capture Function

Address 0139h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	PWMD1	PWMC1	PWMB1	—	PWMD0	PWMC0	PWMB0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PWMB0	PWM mode of TRDIOB0 select bit	Set to 0 (timer mode) for the input capture function.	R/W
b1	PWMC0	PWM mode of TRDIOC0 select bit		R/W
b2	PWMD0	PWM mode of TRDIOD0 select bit		R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b4	PWMB1	PWM mode of TRDIOB1 select bit	Set to 0 (timer mode) for the input capture function.	R/W
b5	PWMC1	PWM mode of TRDIOC1 select bit		R/W
b6	PWMD1	PWM mode of TRDIOD1 select bit		R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

21.3.6 Timer RD Function Control Register (TRDFCR) for Input Capture Function

Address 013Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PWM3	STCLK	ADEG	ADTRG	OLS1	OLS0	CMD1	CMD0
After Reset	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CMD0	Combination mode select bit (1)	Set to 00b (timer mode, PWM mode, or PWM3 mode) for the input capture function.	R/W
b1	CMD1			R/W
b2	OLS0	Normal-phase output level select bit (in reset synchronous PWM mode or complementary PWM mode)	Disabled for the input capture function.	R/W
b3	OLS1	Counter-phase output level select bit (in reset synchronous PWM mode or complementary PWM mode)		R/W
b4	ADTRG	A/D trigger enable bit (in complementary PWM mode)		R/W
b5	ADEG	A/D trigger edge select bit (in complementary PWM mode)		R/W
b6	STCLK	External clock input select bit	0: External clock input disabled 1: External clock input enabled	R/W
b7	PWM3	PWM3 mode select bit (2)	Set to 1 (other than PWM3 mode) for the input capture function.	R/W

Notes:
1. Set bits CMD1 to CMD0 when both the TSTART0 and TSTART1 bits in the TRDSTR register are set to 0 (count stops).
2. When bits CMD1 to CMD0 are set to 00b (timer mode, PWM mode, or PWM3 mode), the setting of the PWM3 bit is enabled.

21.3.7 Timer RD Digital Filter Function Select Register i (TRDDFi) (i = 0 or 1) for Input Capture Function

Address 013Eh (TRDDF0), 013Fh (TRDDF1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DFCK1	DFCK0	—	—	DFD	DFC	DFB	DFA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DFA	TRDIOA pin digital filter function select bit	0: Function is not used 1: Function is used	R/W
b1	DFB	TRDIOB pin digital filter function select bit		R/W
b2	DFC	TRDIOC pin digital filter function select bit		R/W
b3	DFD	TRDIOD pin digital filter function select bit		R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	DFCK0	Clock select bits for digital filter function	b7 b6 0 0: f32 0 1: f8 1 0: f1 1 1: Count source (clock selected by bits TCK0 to TCK2 in the TRCCRi register)	R/W
b7	DFCK1			R/W

21.3.8 Timer RD Control Register i (TRDCRi) (i = 0 or 1) for Input Capture Function

Address 0140h (TRDCR0), 0150h (TRDCR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TCK2	TCK1	TCK0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TCK0	Count source select bit	b2 b1 b0 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRDCLK input (1) or fC2 (2) 1 1 0: fOCO40M 1 1 1: Do not set.	R/W
b1	TCK1			R/W
b2	TCK2			R/W
b3	CKEG0	External clock edge select bit (3)	b4 b3 0 0: Count at the rising edge 0 1: Count at the falling edge 1 0: Count at both edges 1 1: Do not set.	R/W
b4	CKEG1			R/W
b5	CCLR0	TRDi counter clear select bit	b7 b6 b5 0 0 0: Clear disabled (free-running operation) 0 0 1: Clear by input capture to the TRDGRAi register 0 1 0: Clear by input capture to the TRDGRBi register 0 1 1: Synchronous clear (clear simultaneously with other timer RDi counter) (4) 1 0 0: Do not set. 1 0 1: Clear by input capture to the TRDGRCi register 1 1 0: Clear by input capture to the TRDGRDi register 1 1 1: Do not set.	R/W
b6	CCLR1			R/W
b7	CCLR2			R/W

Notes:
1. Enabled when the ITCLKi bit in the TRDECR register is set to 0 (TRDCLK input) and the STCLK bit in the TRDFCR register is 1 (external clock input enabled).
2. Enabled when the ITCLKi bit in the TRDECR register is set to 1 (fC2).
3. Enabled when bits TCK2 to TCK0 are set to 101b (TRDCLK input or fC2), the ITCLKi bit in the TRDECR is set to 0 (TRDCLK input), and the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).
4. Enabled when the SYNC bit in the TRDMR register is set to 1 (registers TRD0 and TRD1 operate synchronously).

21.3.9 Timer RD I/O Control Register Ai (TRDIORAi) (i = 0 or 1) for Input Capture Function

Address 0141h (TRDIORA0), 0151h (TRDIORA1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRDGRA control bit	b1 b0 0 0: Input capture to the TRDGRAi register at the rising edge 0 1: Input capture to the TRDGRAi register at the falling edge 1 0: Input capture to the TRDGRAi register at both edges 1 1: Do not set.	R/W
b1	IOA1			R/W
b2	IOA2	TRDGRA mode select bit (1)	Set to 1 (input capture) for the input capture function.	R/W
b3	IOA3	Input capture input switch bit (3, 4)	0: fOCO128 signal 1: TRDIOA0 pin input	R/W
b4	IOB0	TRDGRB control bit	b5 b4 0 0: Input capture to the TRDGRBi register at the rising edge 0 1: Input capture to the TRDGRBi register at the falling edge 1 0: Input capture to the TRDGRBi register at both edges 1 1: Do not set.	R/W
b5	IOB1			R/W
b6	IOB2	TRDGRB mode select bit (2)	Set to 1 (input capture) for the input capture function.	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Notes:
1. To select 1 (TRDGRCi register is used as the buffer register of the TRDGRAi register) for this bit by the BFCi bit in the TRDMR register, set the IOC2 bit in the TRDIORCi register to the same value as the IOA2 bit in the TRDIORAi register.
2. To select 1 (TRDGRDi register is used as the buffer register of the TRDGRBi register) for this bit by the BFDi bit in the TRDMR register, set the IOD2 bit in the TRDIORCi register to the same value as the IOB2 bit in the TRDIORAi register.
3. The IOA3 bit is enabled in the TRDIORA0 register only. Set to the IOA3 bit in TRDIORA1 to 1.
4. The IOA3 bit is enabled when the IOA2 bit is set to 1 (input capture function).

21.3.10 Timer RD I/O Control Register Ci (TRDIORCi) (i = 0 or 1) for Input Capture Function

Address 0142h (TRDIORC0), 0152h (TRDIORC1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOC0	TRDGRC control bit	b1 b0 0 0: Input capture to the TRDGRCi register at the rising edge 0 1: Input capture to the TRDGRCi register at the falling edge 1 0: Input capture to the TRDGRCi register at both edges 1 1: Do not set.	R/W
b1	IOC1			R/W
b2	IOC2	TRDGRC mode select bit (1)	Set to 1 (input capture) for the input capture function.	R/W
b3	IOC3	TRDGRC register function select bit	Set to 1 (general register or buffer register) for the input capture function.	R/W
b4	IOD0	TRDGRD control bit	b5 b4 0 0: Input capture to the TRDGRDi register at the rising edge 0 1: Input capture to the TRDGRDi register at the falling edge 1 0: Input capture to the TRDGRDi register at both edges 1 1: Do not set.	R/W
b5	IOD1			R/W
b6	IOD2	TRDGRD mode select bit (2)	Set to 1 (input capture) for the input capture function.	R/W
b7	IOD3	TRDGRD register function select bit	Set to 1 (general register or buffer register) for the input capture function.	R/W

Notes:
1. To select 1 (TRDGRCi register is used as the buffer register of the TRDGRAi register) for this bit by the BFCi bit in the TRDMR register, set the IOC2 bit in the TRDIORCi register to the same value as the IOA2 bit in the TRDIORAi register.
2. To select 1 (TRDGRDi register is used as the buffer register of the TRDGRBi register) for this bit by the BFDi bit in the TRDMR register, set the IOD2 bit in the TRDIORCi register to the same value as the IOB2 bit in the TRDIORAi register.

21.3.11 Timer RD Status Register i (TRDSRi) (i = 0 or 1) for Input Capture Function

Address 0143h (TRDSR0), 0153h (TRDSR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	UDF	OVF	IMFD	IMFC	IMFB	IMFA	
After Reset	1	1	1	0	0	0	0	0	TRDSR0 register
After Reset	1	1	0	0	0	0	0	0	TRDSR1 register

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input-capture/compare-match flag A	[Condition for setting this bit to 0] Write 0 after reading. (2) [Condition for setting this bit to 1]. TRDSR0 register: fOCO128 signal edge when the IOA3 bit in the TRDIORA0 register is set to 0 (fOCO128 signal). Input edge of TRDIOA0 pin when the IOA3 bit in the TRDIORA0 register is set to 1 (TRDIOA0 input) (3). TRDSR1 register: Input edge of TRDIOA1 pin (3).	R/W
b1	IMFB	Input-capture/compare-match flag B	[Condition for setting this bit to 0] Write 0 after reading. (2) [Condition for setting this bit to 1] Input edge of TRDIOBi pin (3).	R/W
b2	IMFC	Input-capture/compare-match flag C	[Condition for setting this bit to 0] Write 0 after reading. (2) [Condition for setting this bit to 1] Input edge of TRDIOCi pin (4).	R/W
b3	IMFD	Input-capture/compare-match flag D	[Condition for setting this bit to 0] Write 0 after reading. (2) [Condition for setting this bit to 1] Input edge of TRDIODi pin (4).	R/W
b4	OVF	Overflow flag	[Condition for setting this bit to 0] Write 0 after reading. (2) [Condition for setting this bit to 1] When the TRDi register overflows.	R/W
b5	UDF	Underflow flag (1)	Disabled for the input capture function.	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b7	—			

Notes:
1. Nothing is assigned to b5 in the TRDSR0 register. If necessary, write 0 to b5. When read, the content is 1.
2. The results of writing to these bits are as follows:
   - The bit is set to 0 when it is first read as 1 and then 0 is written to it.
   - The bit remains unchanged even if it is first read as 0 and then 0 is written to it because its previous value is retained. (The bit's value remains 1 even if it is set to 1 from 0 after being read as 0 and having 0 written to it because its previous value is retained.)
   - The bit's value remains unchanged if 1 is written to it.
3. Edge selected by bits IOj0 and IOj1 (j = A or B) in the TRDIORAi register.
4. Edge selected by bits IOk0 and IOk1 (k = C or D) in the TRDIORCi register.
   Including when the BFki bit in the TRDMR register is set to 1 (TRDGRki is used as a buffer register)

21.3.12 Timer RD Interrupt Enable Register i (TRDIERi) (i = 0 or 1) for Input Capture Function

Address 0144h (TRDIER0), 0154h (TRDIER1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	OVIE	IMIED	IMIEC	IMIEB	IMIEA
After Reset	1	1	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input-capture/compare-match interrupt enable bit A	0: Interrupt (IMIA) by IMFA bit disabled 1: Interrupt (IMIA) by IMFA bit enabled	R/W
b1	IMIEB	Input-capture/compare-match interrupt enable bit B	0: Interrupt (IMIB) by IMFB bit disabled 1: Interrupt (IMIB) by IMFB bit enabled	R/W
b2	IMIEC	Input-capture/compare-match interrupt enable bit C	0: Interrupt (IMIC) by IMFC bit disabled 1: Interrupt (IMIC) by IMFC bit enabled	R/W
b3	IMIED	Input-capture/compare-match interrupt enable bit D	0: Interrupt (IMID) by IMFD bit disabled 1: Interrupt (IMID) by the IMFD bit enabled	R/W
b4	OVIE	Overflow/underflow interrupt enable bit	0: Interrupt (OVI) by OVF bit disabled 1: Interrupt (OVI) by OVF bit enabled	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b6	—			
b7	—			

21.3.13 Timer RD Counter i (TRDi) (i = 0 or 1) for Input Capture Function

Address 0147h to 0146h (TRD0), 0157h to 0156h (TRD1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	Counts an count source. Count operation is increment. When an overflow occurs, the OVF bit in the TRDSRi register is set to 1.	0000h to FFFFh	R/W

Access the TRDi register in 16-bit units. Do not access it in 8-bit units.

21.3.14 Timer RD General Registers Ai, Bi, Ci, and Di (TRDGRAi, TRDGRBi, TRDGRCi, TRDGRDi) (i = 0 or 1) for Input Capture Function

Address 0149h to 0148h (TRDGRA0), 014Bh to 014Ah (TRDGRB0),
014Dh to 014Ch (TRDGRC0), 014Fh to 014Eh (TRDGRD0),
0159h to 0158h (TRDGRA1), 015Bh to 015Ah (TRDGRB1),
015Dh to 015Ch (TRDGRC1), 015Fh to 015Eh (TRDGRD1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b15 to b0	Refer to **Table 21.6 TRDGRji Register Functions for Input Capture Function**	R/W

Access registers TRDGRAi to TRDGRDi in 16-bit units. Do not access them in 8-bit units.

The following registers are disabled for the input capture function:
TRDOER1, TRDOER2, TRDOCR, TRDPOCR0, and TRDPOCR1.

Table 21.6 TRDGRji Register Functions for Input Capture Function

Register	Setting	Register Function	Input-Capture Input Pin
TRDGRAi	–	General register The value of the TRDi register can be read at input capture.	TRDIOAi
TRDGRBi			TRDIOBi
TRDGRCi	BFCi = 0	General register The value of the TRDi register can be read at input capture.	TRDIOCi
TRDGRDi	BFDi = 0		TRDIODi
TRDGRCi	BFCi = 1	Buffer register The value of the TRDi register can be read at input capture. (Refer to **21.2.2 Buffer Operation**)	TRDIOAi
TRDGRDi	BFDi = 1		TRDIOBi

i = 0 or 1, j = either A, B, C, or D
BFCi, BFDi: Bits in TRDMR register

The pulse width of the input capture signal input to the TRDIOji pin should be set to three or more cycles of the timer RD operating clock (refer to **Table 21.1 Timer RD Operating Clocks**) when the digital filter is not used (the DFj bit in the TRDDFi register is set to 0).

21.3.15 Timer RD Pin Select Register 0 (TRDPSR0)

Address 0184h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRDIOD0SEL1	TRDIOD0SEL0	TRDIOC0SEL1	TRDIOC0SEL0	TRDIOB0SEL1	TRDIOB0SEL0	TRDIOA0SEL1	TRDIOA0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRDIOA0SEL0	TRDIOA0/TRDCLK pin select bit	b1 b0 0 0: TRDIOA0/TRDCLK pin not used 0 1: P6_0 assigned 1 0: P10_0 assigned 1 1: Do not set.	R/W
b1	TRDIOA0SEL1			R/W
b2	TRDIOB0SEL0	TRDIOB0 pin select bit	b3 b2 0 0: TRDIOB0 pin not used 0 1: P6_1 assigned 1 0: P10_1 assigned 1 1: Do not set.	R/W
b3	TRDIOB0SEL1			R/W
b4	TRDIOC0SEL0	TRDIOC0 pin select bit	b5 b4 0 0: TRDIOC0 pin not used 0 1: P6_2 assigned 1 0: P10_2 assigned 1 1: Do not set.	R/W
b5	TRDIOC0SEL1			R/W
b6	TRDIOD0SEL0	TRDIOD0 pin select bit	b7 b6 0 0: TRDIOC0 pin not used 0 1: P6_3 assigned 1 0: P10_3 assigned 1 1: Do not set.	R/W
b7	TRDIOD0SEL1			R/W

The TRDPSR0 register selects which pin is assigned as the timer RD input/output. To use the I/O pins for timer RD, set this register.

Set the TRDPSR0 register before setting the timer RD associated registers. Also, do not change the setting value of this register during timer RD operation.

21.3.16 Timer RD Pin Select Register 1 (TRDPSR1)

Address 0185h

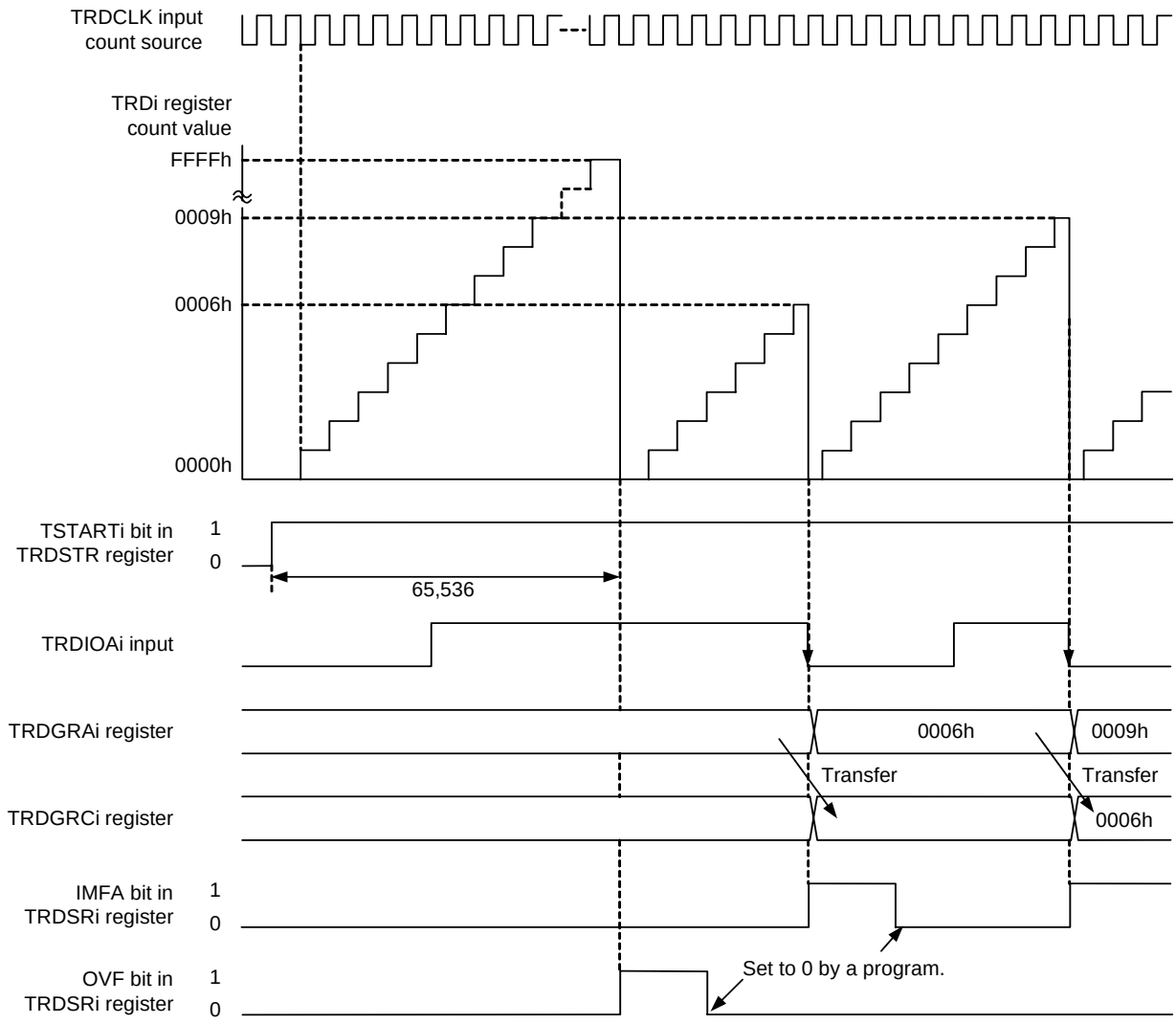
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRDIOD1SEL1	TRDIOD1SEL0	TRDIOC1SEL1	TRDIOC1SEL0	TRDIOB1SEL1	TRDIOB1SEL0	TRDIOA1SEL1	TRDIOA1SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRDIOA1SEL0	TRDIOA1 pin select bit	b1 b0 0 0: TRDIOA1 pin not used 0 1: P6_4 assigned 1 0: P10_4 assigned 1 1: Do not set.	R/W
b1	TRDIOA1SEL1			R/W
b2	TRDIOB1SEL0	TRDIOB1 pin select bit	b3 b2 0 0: TRDIOB1 pin not used 0 1: P6_5 assigned 1 0: P10_5 assigned 1 1: Do not set.	R/W
b3	TRDIOB1SEL1			R/W
b4	TRDIOC1SEL0	TRDIOC1 pin select bit	b5 b4 0 0: TRDIOC1 pin not used 0 1: P6_6 assigned 1 0: P10_6 assigned 1 1: Do not set.	R/W
b5	TRDIOC1SEL1			R/W
b6	TRDIOD1SEL0	TRDIOD1 pin select bit	b7 b6 0 0: TRDIOC1 pin not used 0 1: P6_7 assigned 1 0: P10_7 assigned 1 1: Do not set.	R/W
b7	TRDIOD1SEL1			R/W

The TRDPSR1 register selects which pin is assigned as the timer RD input/output. To use the I/O pins for timer RD, set this register.

Set the TRDPSR1 register before setting the timer RD associated registers. Also, do not change the setting value of this register during timer RD operation.

21.3.17 Operating Example



i = 0 or 1

The above applies under the following conditions:
Bits CCLR2 to CCLR0 in the TRDCRi register are set to 001b. (TRDi register set to 0000h by TRDGRAi register input capture).
Bits TCK2 to TCK0 in the TRDCRi register are set to 101b (TRDCLK input selected as the count source).
Bits CKEG1 to CKEG0 in the TRDCRi register are set to 01b (count at the falling edge selected as the count source).
Bits IOA2 to IOA0 in the TRDIORAi register are set to 101b (input capture at the falling edge of the TRDIOAi input).
The BFCi bit in the TRDMR register is set to 1 (TRDGRCi register is used as the buffer register of the TRDGRAi register).

Figure 21.8 Operating Example of Input Capture Function

21.3.18 Digital Filter

The TRDIOji input is sampled and the level is determined when the sampled input level matches three times. The digital filter function and sampling clock can be selected using the TRDDFi register.
Figure 21.9 shows a Block Diagram of Digital Filter.

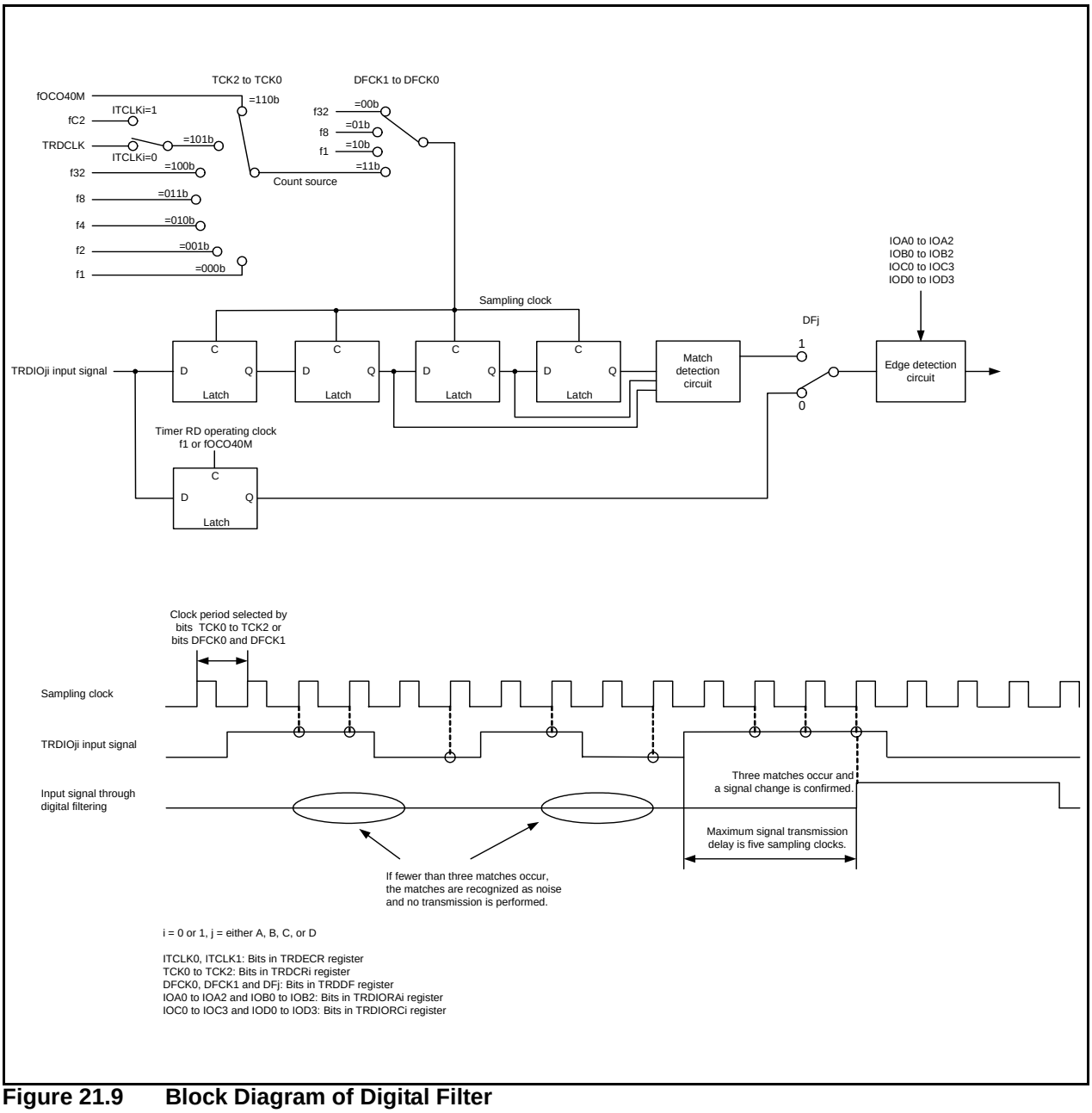


Figure 21.9 Block Diagram of Digital Filter

21.4 Output Compare Function

This function detects matches (compare match) between the content of the TRDGRji (j = either A, B, C, or D) register and the content of the TRDi (i = 0 or 1) register. When the content matches, a user-set level is output from the TRDIOji pin. Since this function is enabled with a combination of the TRDIOji pin and TRDGRji register, the output compare function, or any other mode or function, can be selected for each individual pin.
Figure 21.10 shows a Block Diagram of Output Compare Function, Table 21.7 lists the Output Compare Function Specifications. Figure 21.11 shows an Operating Example of Output Compare Function.

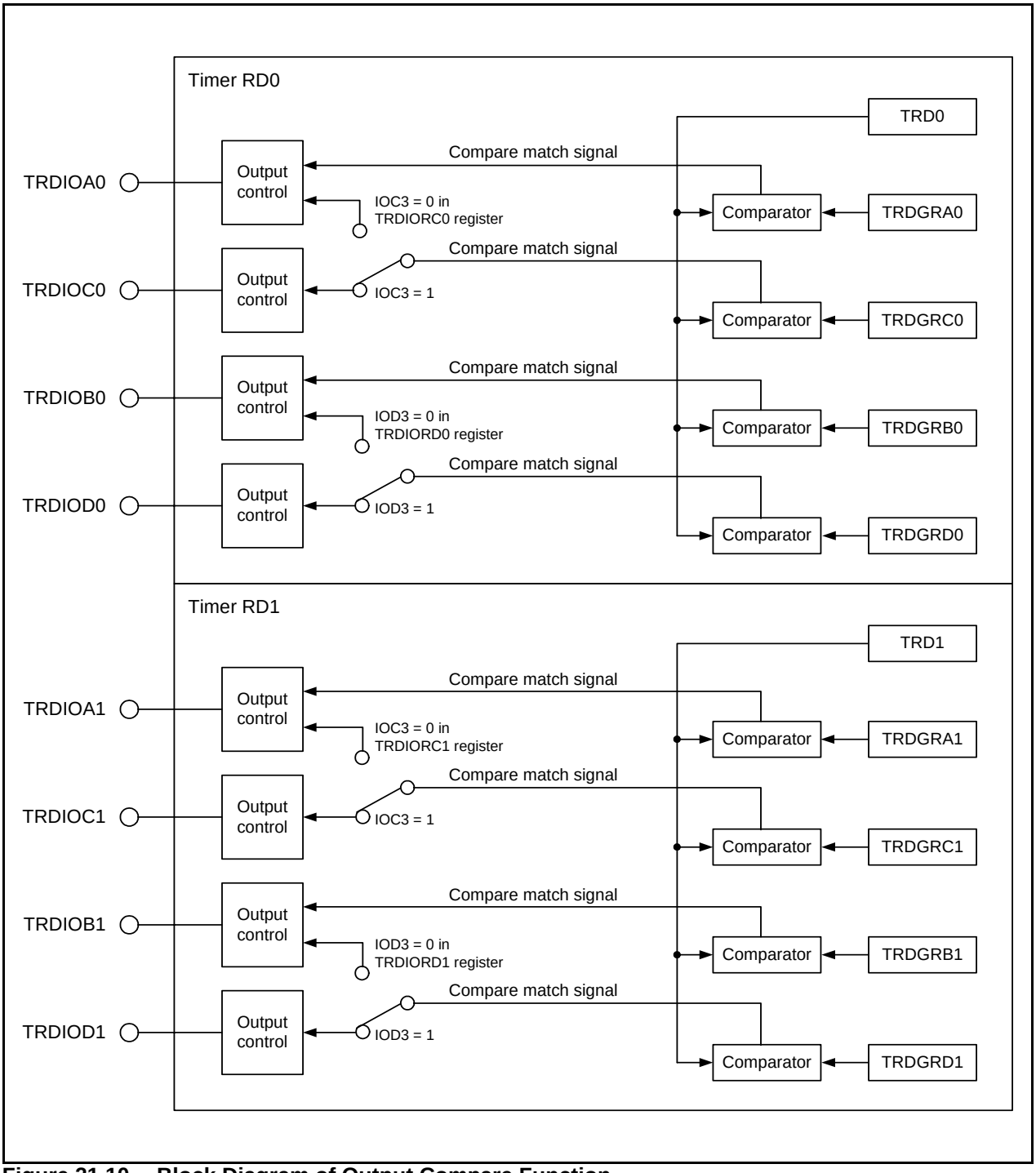


Figure 21.10 Block Diagram of Output Compare Function

Table 21.7 Output Compare Function Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, fC2, fOCO40M, External signal input to the TRDCLK pin (active edge selectable by a program)
Count operations	Increment
Count period	• When bits CCLR2 to CCLR0 in the TRDCRi register are set to 000b (free-running operation) 1/fk × 65,536 fk: Frequency of count source • Bits CCLR1 to CCLR0 in the TRDCRi register are set to 01b or 10b (TRDi register is set to 0000h at compare match with the TRDGRji register). Frequency of count source x (n+1) n: Value set in TRDGRji register
Waveform output timing	Compare match
Count start condition	1 (count starts) is written to the TSTARTi bit in the TRDSTR register.
Count stop conditions	• 0 (count stops) is written to the TSTARTi bit in the TRDSTR register when the CSELi bit in the TRDSTR register is set to 1. The output compare output pin holds output level before the count stops. • When the CSELi bit in the TRDSTR register is set to 0, the count stops at the compare match with the TRDGRAi register. The output compare output pin holds the level after the output changes by the compare match.
Interrupt request generation timing	• Compare match (the contents of the TRDi register and the TRDGRji register match.) • TRDi register overflow
TRDIOA0 pin function	Programmable I/O port, output-compare output, or TRDCLK (external clock) input
TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1 to TRDIOD1 pins function	Programmable I/O port or output-compare output (selectable for each individual pin)
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRDi register.
Write to timer	• When the SYNC bit in the TRDMR register is set to 0 (timer RD0 and timer RD1 operate independently). Data can be written to the TRDi register. • When the SYNC bit in the TRDMR register is set to 1 (timer RD0 and timer RD1 operate synchronously). Data can be written to both the TRD0 and TRD1 registers by writing to the TRDi register.
Selectable functions	• Output-compare output pin selection Either one or multiple pins among TRDIOAi, TRDIOBi, TRDIOCi, or TRDIODi. • Output level selection at the compare match Low-level output, high-level output, or output level inversion • Initial output level selected Selectable level for the period from the count start to the compare match • Timing for setting the TRDi register to 0000h Overflow or compare match with the TRDGRAi register • Buffer operation (Refer to **21.2.2 Buffer Operation.**) • Synchronous operation (Refer to **21.2.3 Synchronous Operation.**) • Changing output pins for registers TRDGRCi and TRDGRDi The TRDGRCi register can be used as output control of the TRDIOAi pin and the TRDGRDi register can be used as output control of the TRDIOBi pin. • Pulse output forced cutoff signal input (Refer to **21.2.4 Pulse Output Forced Cutoff.**) • Timer RD can be used as the internal timer without output. • A/D trigger generation

i = 0 or 1, j = either A, B, C, or D

21.4.1 Module Standby Control Register (MSTCR)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	MSTTRG	MSTTRC	MSTTRD	MSTIIC	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	MSTIIC	SSU, I^2C bus standby bit	0: Active 1: Standby (1)	R/W
b4	MSTTRD	Timer RD standby bit	0: Active 1: Standby (2)	R/W
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (3)	R/W
b6	MSTTRG	Timer RG standby bit	0: Active 1: Standby (4)	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. When the MSTIIC bit is set to 1 (standby), any access to the SSU or the I^2C bus associated registers (addresses 0193h to 019Dh) is disabled.
2. When the MSTTRD bit is set to 1 (standby), any access to the timer RD associated registers (addresses 0135h to 015Fh) is disabled.
3. When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0133h) is disabled.
4. When the MSTTRG bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0170h to 017Fh) is disabled.

21.4.2 Timer RD Control Expansion Register (TRDECR)

Address 0135h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ITCLK1	—	—	—	ITCLK0	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	ITCLK0	Timer RD0 fC2 select bit	0: TRDCLK input selected 1: fC2 selected	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	ITCLK1	Timer RD1 fC2 select bit	0: TRDCLK input selected 1: fC2 selected	R/W

21.4.3 Timer RD Trigger Control Register (TRDADCR)

Address 0136h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADTRGD1E	ADTRGC1E	ADTRGB1E	ADTRGA1E	ADTRGD0E	ADTRGC0E	ADTRGB0E	ADTRGA0E
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADTRGA0E	A/D trigger A0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRA0	R/W
b1	ADTRGB0E	A/D trigger B0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRB0	R/W
b2	ADTRGC0E	A/D trigger C0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRC0	R/W
b3	ADTRGD0E	A/D trigger D0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRD0	R/W
b4	ADTRGA1E	A/D trigger A1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRA1	R/W
b5	ADTRGB1E	A/D trigger B1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRB1	R/W
b6	ADTRGC1E	A/D trigger C1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRC1	R/W
b7	ADTRGD1E	A/D trigger D1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRD1	R/W

21.4.4 Timer RD Start Register (TRDSTR) for Output Compare Function

Address 0137h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	CSEL1	CSEL0	TSTART1	TSTART0
After Reset	1	1	1	1	1	1	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART0	TRD0 count start flag (3)	0: Count stops (1) 1: Count starts	R/W
b1	TSTART1	TRD1 count start flag (4)	0: Count stops (2) 1: Count starts	R/W
b2	CSEL0	TRD0 count operation select bit	0: Count stops at compare match with the TRDGRA0 register 1: Count continues after compare match with the TRDGRA0 register	R/W
b3	CSEL1	TRD1 count operation select bit	0: Count stops at compare match with the TRDGRA1 register 1: Count continues after compare match with the TRDGRA1 register	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	—			

Notes:
1. When the CSEL0 bit is set to 1, write 0 to the TSTART0 bit.
2. When the CSEL1 bit is set to 1, write 0 to the TSTART1 bit.
3. When the CSEL0 bit is set to 0 and the compare match signal (TRDIOA0) is generated, this bit is set to 0 (count stops).
4. When the CSEL1 bit is set to 0 and the compare match signal (TRDIOA1) is generated, this bit is set to 0 (count stops).

Set the TRDSTR register using the MOV instruction (do not use the bit handling instruction). Refer to **21.10.1 TRDSTR Register** for **Notes on Timer RD**.

21.4.5 Timer RD Mode Register (TRDMR) for Output Compare Function

Address 0138h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BFD1	BFC1	BFD0	BFC0	—	—	—	SYNC
After Reset	0	0	0	0	1	1	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	SYNC	Timer RD synchronous bit	0: Registers TRD0 and TRD1 operate independently 1: Registers TRD0 and TRD1 operate synchronously	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b2	—			
b3	—			
b4	BFC0	TRDGRC0 register function select bit (1)	0: General register 1: Buffer register of TRDGRA0 register	R/W
b5	BFD0	TRDGRD0 register function select bit (1)	0: General register 1: Buffer register of TRDGRB0 register	R/W
b6	BFC1	TRDGRC1 register function select bit (1)	0: General register 1: Buffer register of TRDGRA1 register	R/W
b7	BFD1	TRDGRD1 register function select bit (1)	0: General register 1: Buffer register of TRDGRB1 register	R/W

Note:
1. When selecting 0 (change the TRDGRji register output pin) by the IOj3 (j = C or D) bit in the TRDIORCi (i = 0 or 1) register, set the BFji bit in the TRDMR register to 0.

21.4.6 Timer RD PWM Mode Register (TRDPMR) for Output Compare Function

Address 0139h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	PWMD1	PWMC1	PWMB1	—	PWMD0	PWMC0	PWMB0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PWMB0	PWM mode of TRDIOB0 select bit	Set to 0 (timer mode) for the output compare function.	R/W
b1	PWMC0	PWM mode of TRDIOC0 select bit		R/W
b2	PWMD0	PWM mode of TRDIOD0 select bit		R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b4	PWMB1	PWM mode of TRDIOB1 select bit	Set to 0 (timer mode) for the output compare function.	R/W
b5	PWMC1	PWM mode of TRDIOC1 select bit		R/W
b6	PWMD1	PWM mode of TRDIOD1 select bit		R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

21.4.7 Timer RD Function Control Register (TRDFCR) for Output Compare Function

Address 013Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PWM3	STCLK	ADEG	ADTRG	OLS1	OLS0	CMD1	CMD0
After Reset	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CMD0	Combination mode select bit (1)	Set to 00b (timer mode, PWM mode, or PWM3 mode) for the output compare function.	R/W
b1	CMD1			R/W
b2	OLS0	Normal-phase output level select bit (in reset synchronous PWM mode or complementary PWM mode)	Disabled for the output compare function.	R/W
b3	OLS1	Counter-phase output level select bit (in reset synchronous PWM mode or complementary PWM mode)		R/W
b4	ADTRG	A/D trigger enable bit (in complementary PWM mode)		R/W
b5	ADEG	A/D trigger edge select bit (in complementary PWM mode)		R/W
b6	STCLK	External clock input select bit	0: External clock input disabled 1: External clock input enabled	R/W
b7	PWM3	PWM3 mode select bit (2)	Set to 1 (other than PWM3 mode) for the output compare function.	R/W

Notes:
1. Set bits CMD1 to CMD0 when both the TSTART0 and TSTART1 bits in the TRDSTR register are set to 0 (count stops).
2. When bits CMD1 to CMD0 are set to 00b (timer mode, PWM mode, or PWM3 mode), the setting of the PWM3 bit is enabled.

21.4.8 Timer RD Output Master Enable Register 1 (TRDOER1) for Output Compare Function

Address 013Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ED1	EC1	EB1	EA1	ED0	EC0	EB0	EA0
After Reset	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	EA0	TRDIOA0 output disable bit	0: Output enabled 1: Output disabled (TRDIOA0 pin is used as a programmable I/O port)	R/W
b1	EB0	TRDIOB0 output disable bit	0: Output enabled 1: Output disabled (TRDIOB0 pin is used as a programmable I/O port)	R/W
b2	EC0	TRDIOC0 output disable bit	0: Output enabled 1: Output disabled (TRDIOC0 pin is used as a programmable I/O port)	R/W
b3	ED0	TRDIOD0 output disable bit	0: Output enabled 1: Output disabled (TRDIOD0 pin is used as a programmable I/O port)	R/W
b4	EA1	TRDIOA1 output disable bit	0: Output enabled 1: Output disabled (TRDIOA1 pin is used as a programmable I/O port)	R/W
b5	EB1	TRDIOB1 output disable bit	0: Output enabled 1: Output disabled (TRDIOB1 pin is used as a programmable I/O port)	R/W
b6	EC1	TRDIOC1 output disable bit	0: Output enabled 1: Output disabled (TRDIOC1 pin is used as a programmable I/O port)	R/W
b7	ED1	TRDIOD1 output disable bit	0: Output enabled 1: Output disabled (TRDIOD1 pin is used as a programmable I/O port)	R/W

21.4.9 Timer RD Output Master Enable Register 2 (TRDOER2) for Output Compare Function

Address 013Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PTO	—	—	—	—	—	—	—
After Reset	0	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b1	—			—
b2	—			—
b3	—			—
b4	—			—
b5	—			—
b6	—			—
b7	PTO	$\overline{\text{INT0}}$ of pulse output forced cutoff signal input enabled bit (1)	0: Pulse output forced cutoff input disabled 1: Pulse output forced cutoff input enabled (All bits in the TRDOER1 register are set to 1 (output disabled) when a low-level signal is applied to the $\overline{\text{INT0}}$ pin.)	R/W

Note:
1. Refer to **21.2.4 Pulse Output Forced Cutoff**.

21.4.10 Timer RD Output Control Register (TRDOCR) for Output Compare Function

Address 013Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TOD1	TOC1	TOB1	TOA1	TOD0	TOC0	TOB0	TOA0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA0	TRDIOA0 output level select bit	0: Initial output at low 1: Initial output at high	R/W
b1	TOB0	TRDIOB0 output level select bit		R/W
b2	TOC0	TRDIOC0 initial output level select bit	0: Low 1: High	R/W
b3	TOD0	TRDIOD0 initial output level select bit		R/W
b4	TOA1	TRDIOA1 initial output level select bit		R/W
b5	TOB1	TRDIOB1 initial output level select bit		R/W
b6	TOC1	TRDIOC1 initial output level select bit		R/W
b7	TOD1	TRDIOD1 initial output level select bit		R/W

Write to the TRDOCR register when both the TSTART0 and TSTART1 bits in the TRDSTR register are set to 0 (count stops).
If the pin function is set for waveform output (refer to **7.5 Port Settings**), the initial output level is output when the TRDOCR register is set.

21.4.11 Timer RD Control Register i (TRDCRi) (i = 0 or 1) for Output Compare Function

Address 0140h (TRDCR0), 0150h (TRDCR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TCK2	TCK1	TCK0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TCK0	Count source select bit	b2 b1 b0 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRDCLK input (1) or fC2 (2) 1 1 0: fOCO40M 1 1 1: Do not set.	R/W
b1	TCK1			R/W
b2	TCK2			R/W
b3	CKEG0	External clock edge select bit (3)	b4 b3 0 0: Count at the rising edge 0 1: Count at the falling edge 1 0: Count at both edges 1 1: Do not set.	R/W
b4	CKEG1			R/W
b5	CCLR0	TRDi counter clear select bit	b7 b6 b5 0 0 0: Clear disabled (free-running operation) 0 0 1: Clear by compare match with the TRDGRAi register 0 1 0: Clear by compare match with the TRDGRBi register 0 1 1: Synchronous clear (clear simultaneously with other timer RDi counter) (4) 1 0 0: Do not set. 1 0 1: Clear by compare match with the TRDGRCi register 1 1 0: Clear by compare match with the TRDGRDi register 1 1 1: Do not set.	R/W
b6	CCLR1			R/W
b7	CCLR2			R/W

Notes:
1. Enabled when the ITCLKi bit in the TRDECR register is set to 0 (TRDCLK input) and the STCLK bit in the TRDFCR register is 1 (external clock input enabled).
2. This setting is enabled when the ITCLKi bit in the TRDECR register is set to 1 (fC2).
3. Enabled when bits TCK2 to TCK0 are set to 101b (TRDCLK input or fC2), the ITCLKi bit in the TRDECR is set to 0 (TRDCLK input), and the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).
4. This setting is enabled when the SYNC bit in the TRDMR register is set to 1 (registers TRD0 and TRD1 operate synchronously).

21.4.12 Timer RD I/O Control Register Ai (TRDIORAi) (i = 0 or 1) for Output Compare Function

Address 0141h (TRDIORA0), 0151h (TRDIORA1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRDGRA control bit	b1 b0 0 0: Pin output by compare match is disabled (TRDIOAi pin functions as a programmable I/O port) 0 1: Low-level output at compare match with the TRDGRAi register 1 0: High-level output at compare match with the TRDGRAi register 1 1: Toggle output at compare match with the TRDGRAi register	R/W
b1	IOA1			R/W
b2	IOA2	TRDGRA mode select bit (1)	Set to 0 (output compare) for the output compare function.	R/W
b3	IOA3	Input capture input switch bit	Set to 1.	R/W
b4	IOB0	TRDGRB control bit	b5 b4 0 0: Pin output by compare match is disabled (TRDIOBi pin functions as a programmable I/O port) 0 1: Low-level output at compare match with the TRDGRBi register 1 0: High-level output at compare match with the TRDGRBi register 1 1: Toggle output at compare match with the TRDGRBi register	R/W
b5	IOB1			R/W
b6	IOB2	TRDGRB mode select bit (2)	Set to 0 (output compare) for the output compare function.	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Notes:
1. To select 1 (TRDGRCi register is used as the buffer register of the TRDGRAi register) for this bit by the BFCi bit in the TRDMR register, set the IOC2 bit in the TRDIORCi register to the same value as the IOA2 bit in the TRDIORAi register.
2. To select 1 (TRDGRDi register is used as the buffer register of the TRDGRBi register) for this bit by the BFDi bit in the TRDMR register, set the IOD2 bit in the TRDIORCi register to the same value as the IOB2 bit in the TRDIORAi register.

21.4.13 Timer RD I/O Control Register Ci (TRDIORCi) (i = 0 or 1) for Output Compare Function

Address 0142h (TRDIORC0), 0152h (TRDIORC1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOC0	TRDGRC control bit	b1 b0 0 0: Pin output by compare match is disabled 0 1: Low-level output at compare match with the TRDGRCi register 1 0: High-level output at compare match with the TRDGRCi register 1 1: Toggle output at compare match with the TRDGRCi register	R/W
b1	IOC1			R/W
b2	IOC2	TRDGRC mode select bit (1)	Set to 0 (output compare) for the output compare function.	R/W
b3	IOC3	TRDGRC register function select bit	0: TRDIOA output register (Refer to **21.4.21 Changing Output Pins in Registers TRDGRCi (i = 0 or 1) and TRDGRDi**.) 1: General register or buffer register	R/W
b4	IOD0	TRDGRD control bit	b5 b4 0 0: Pin output by compare match is disabled 0 1: Low-level output at compare match with the TRDGRDi register 1 0: High-level output at compare match with the TRDGRDi register 1 1: Toggle output at compare match with the TRDGRDi register	R/W
b5	IOD1			R/W
b6	IOD2	TRDGRD mode select bit (2)	Set to 0 (output compare) for the output compare function.	R/W
b7	IOD3	TRDGRD register function select bit	0: TRDIOB output register (Refer to **21.4.21 Changing Output Pins in Registers TRDGRCi (i = 0 or 1) and TRDGRDi**.) 1: General register or buffer register	R/W

Notes:
1. To select 1 (TRDGRCi register is used as a buffer register of the TRDGRAi register) for this bit by the BFCi bit in the TRDMR register, set the IOC2 bit in the TRDIORCi register to the same value as the IOA2 bit in the TRDIORAi register.
2. To select 1 (TRDGRDi register is used as a buffer register of the TRDGRBi register) for this bit by the BFDi bit in the TRDMR register, set the IOD2 bit in the TRDIORCi register to the same value as the IOB2 bit in the TRDIORAi register.

21.4.14 Timer RD Status Register i (TRDSRi) (i = 0 or 1) for Output Compare Function

Address 0143h (TRDSR0), 0153h (TRDSR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	UDF	OVF	IMFD	IMFC	IMFB	IMFA	
After Reset	1	1	1	0	0	0	0	0	TRDSR0 register
After Reset	1	1	0	0	0	0	0	0	TRDSR1 register

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input-capture/compare-match flag A	[Condition for setting this bit to 0] Write 0 after reading. (2) [Condition for setting this bit to 1] When the TRDi register value matches the TRDGRAi register value.	R/W
b1	IMFB	Input-capture/compare-match flag B	[Condition for setting this bit to 0] Write 0 after reading. (2) [Condition for setting this bit to 1] When the TRDi register value matches the TRDGRBi register value.	R/W
b2	IMFC	Input-capture/compare-match flag C	[Condition for setting this bit to 0] Write 0 after reading. (2) [Condition for setting this bit to 1] When the TRDi register value matches the TRDGRCi register value (3).	R/W
b3	IMFD	Input-capture/compare-match flag D	[Condition for setting this bit to 0] Write 0 after reading. (2) [Condition for setting this bit to 1] When the TRDi register value matches the TRDGRDi register value (3).	R/W
b4	OVF	Overflow flag	[Condition for setting this bit to 0] Write 0 after reading. (2) [Condition for setting this bit to 1] When the TRDi register overflows.	R/W
b5	UDF	Underflow flag (1)	This bit is disabled for the output compare function.	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b7	—			

Notes:
1. Nothing is assigned to b5 in the TRDSR0 register. If necessary, write 0 to b5. When read, the content is 1.
2. The results of writing to these bits are as follows:
   - The bit is set to 0 when it is first read as 1 and then 0 is written to it.
   - The bit remains unchanged even if it is first read as 0 and then 0 is written to it because its previous value is retained. (The bit's value remains 1 even if it is set to 1 from 0 after being read as 0 and having 0 written to it because its previous value is retained.)
   - The bit's value remains unchanged if 1 is written to it.
3. Including when the BFji bit in the TRDMR register is set to 1 (TRDGRji is used as a buffer register).

21.4.15 Timer RD Interrupt Enable Register i (TRDIERi) (i = 0 or 1) for Output Compare Function

Address 0144h (TRDIER0), 0154h (TRDIER1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	OVIE	IMIED	IMIEC	IMIEB	IMIEA
After Reset	1	1	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input-capture/compare-match interrupt enable bit A	0: Interrupt (IMIA) by IMFA bit disabled 1: Interrupt (IMIA) by IMFA bit enabled	R/W
b1	IMIEB	Input-capture/compare-match interrupt enable bit B	0: Interrupt (IMIB) by IMFB bit disabled 1: Interrupt (IMIB) by IMFB bit enabled	R/W
b2	IMIEC	Input-capture/compare-match interrupt enable bit C	0: Interrupt (IMIC) by IMFC bit disabled 1: Interrupt (IMIC) by IMFC bit enabled	R/W
b3	IMIED	Input-capture/compare-match interrupt enable bit D	0: Interrupt (IMID) by IMFD bit disabled 1: Interrupt (IMID) by the IMFD bit enabled	R/W
b4	OVIE	Overflow/underflow interrupt enable bit	0: Interrupt (OVI) by OVF bit disabled 1: Interrupt (OVI) by OVF bit enabled	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b6	—			
b7	—			

21.4.16 Timer RD Counter i (TRDi) (i = 0 or 1) for Output Compare Function

Address 0147h to 0146h (TRD0), 0157h to 0156h (TRD1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	A count source is counted. Count operation is increment. When an overflow occurs, the OVF bit in the TRDSRi register is set to 1.	0000h to FFFFh	R/W

Access the TRDi register in 16-bit units. Do not access it in 8-bit units.

21.4.17 Timer RD General Registers Ai, Bi, Ci, and Di (TRDGRAi, TRDGRBi, TRDGRCi, TRDGRDi) (i = 0 or 1) for Output Compare Function

Address 0149h to 0148h (TRDGRA0), 014Bh to 014Ah (TRDGRB0),
014Dh to 014Ch (TRDGRC0), 014Fh to 014Eh (TRDGRD0),
0159h to 0158h (TRDGRA1), 015Bh to 015Ah (TRDGRB1),
015Dh to 015Ch (TRDGRC1), 015Fh to 015Eh (TRDGRD1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b15 to b0	Refer to **Table 21.8 TRDGRji Register Function for Output Compare Function**	R/W

Access registers TRDGRAi to TRDGRDi in 16-bit units. Do not access them in 8-bit units.

The following registers are disabled for the output compare function:
TRDDF0, TRDDF1, TRDPOCR0, and TRDPOCR1.

Table 21.8 TRDGRji Register Function for Output Compare Function

Register	Setting		Register Function	Output-Compare Output Pin
	BFji	IOj3		
TRDGRAi	–	–	General register. Write the compare value.	TRDIOAi
TRDGRBi				TRDIOBi
TRDGRCi	0	1	General register. Write the compare value.	TRDIOCi
TRDGRDi				TRDIODi
TRDGRCi	1	1	Buffer register. Write the next compare value. (Refer to **21.2.2 Buffer Operation**.)	TRDIOAi
TRDGRDi				TRDIOBi
TRDGRCi	0	0	TRDIOAi output control (Refer to **21.4.21 Changing Output Pins in Registers TRDGRCi (i = 0 or 1) and TRDGRDi**.)	TRDIOAi
TRDGRDi				TRDIOBi

i = 0 or 1, j = either A, B, C, or D
BFji: Bit in TRDMR register IOj3: Bit in TRDIORCi register

21.4.18 Timer RD Pin Select Register 0 (TRDPSR0)

Address 0184h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRDIOD0SEL1	TRDIOD0SEL0	TRDIOC0SEL1	TRDIOC0SEL0	TRDIOB0SEL1	TRDIOB0SEL0	TRDIOA0SEL1	TRDIOA0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRDIOA0SEL0	TRDIOA0/TRDCLK pin select bit	b1 b0 0 0: TRDIOA0/TRDCLK pin not used 0 1: P6_0 assigned 1 0: P10_0 assigned 1 1: Do not set.	R/W
b1	TRDIOA0SEL1			R/W
b2	TRDIOB0SEL0	TRDIOB0 pin select bit	b3 b2 0 0: TRDIOB0 pin not used 0 1: P6_1 assigned 1 0: P10_1 assigned 1 1: Do not set.	R/W
b3	TRDIOB0SEL1			R/W
b4	TRDIOC0SEL0	TRDIOC0 pin select bit	b5 b4 0 0: TRDIOC0 pin not used 0 1: P6_2 assigned 1 0: P10_2 assigned 1 1: Do not set.	R/W
b5	TRDIOC0SEL1			R/W
b6	TRDIOD0SEL0	TRDIOD0 pin select bit	b7 b6 0 0: TRDIOC0 pin not used 0 1: P6_3 assigned 1 0: P10_3 assigned 1 1: Do not set.	R/W
b7	TRDIOD0SEL1			R/W

The TRDPSR0 register selects which pin is assigned as the timer RD input/output. To use the I/O pins for timer RD, set this register.

Set the TRDPSR0 register before setting the timer RD associated registers. Also, do not change the setting value of this register during timer RD operation.

21.4.19 Timer RD Pin Select Register 1 (TRDPSR1)

Address 0185h

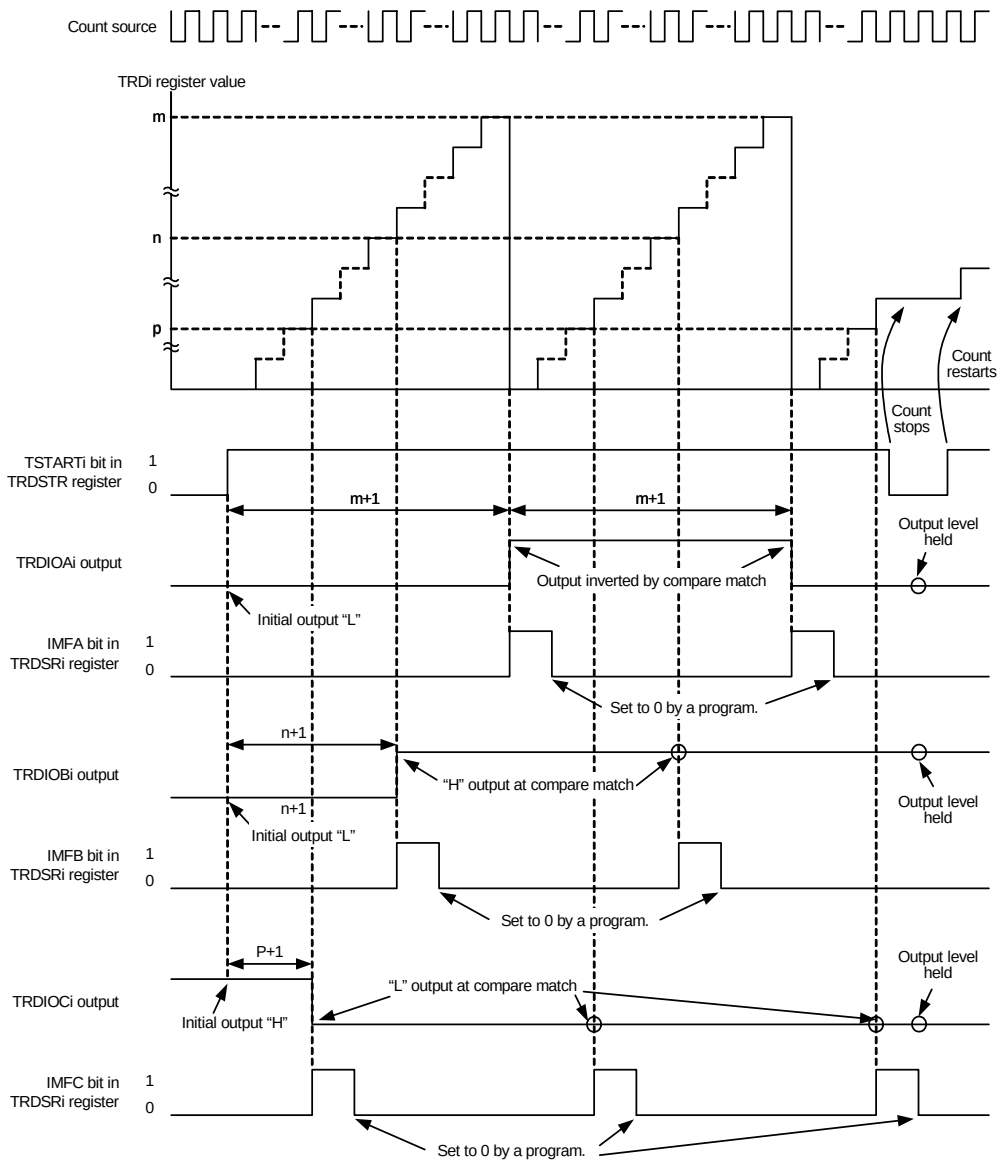
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRDIOD1SEL1	TRDIOD1SEL0	TRDIOC1SEL1	TRDIOC1SEL0	TRDIOB1SEL1	TRDIOB1SEL0	TRDIOA1SEL1	TRDIOA1SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRDIOA1SEL0	TRDIOA1 pin select bit	b1 b0 0 0: TRDIOA1 pin not used 0 1: P6_4 assigned 1 0: P10_4 assigned 1 1: Do not set.	R/W
b1	TRDIOA1SEL1			R/W
b2	TRDIOB1SEL0	TRDIOB1 pin select bit	b3 b2 0 0: TRDIOB1 pin not used 0 1: P6_5 assigned 1 0: P10_5 assigned 1 1: Do not set.	R/W
b3	TRDIOB1SEL1			R/W
b4	TRDIOC1SEL0	TRDIOC1 pin select bit	b5 b4 0 0: TRDIOC1 pin not used 0 1: P6_6 assigned 1 0: P10_6 assigned 1 1: Do not set.	R/W
b5	TRDIOC1SEL1			R/W
b6	TRDIOD1SEL0	TRDIOD1 pin select bit	b7 b6 0 0: TRDIOC1 pin not used 0 1: P6_7 assigned 1 0: P10_7 assigned 1 1: Do not set.	R/W
b7	TRDIOD1SEL1			R/W

The TRDPSR1 register selects which pin is assigned as the timer RD input/output. To use the I/O pins for timer RD, set this register.

Set the TRDPSR1 register before setting the timer RD associated registers. Also, do not change the setting value of this register during timer RD operation.

21.4.20 Operating Example



i = 0 or 1

M: Value set in TRDGRAi register
n: Value set in TRDGRBi register
p: Value set in TRDGRCi register

The above applies under the following conditions:
The CSELi bit in the TRDSTR register is set to 1 (TRDi register count continues after compare match).
Bits BFCi and BFDi in the TRDMR register are set to 0 (registers TRDGRCi and TRDGRDi are not used as buffer registers).
Bits EAi, EBi, and ECi in the TRDOER1 register are set to 0 (TRDIOAi, TRDIOBi and TRDIOCi pin output enabled).
Bits CCLR2 to CCLR0 in the TRDCRi register are set to 001b (TRDi register is set to 000h by compare match with the TRDGRAi register).
Bits TOAi and TOBi in the TRDOCR register is set to 0 (initial output at low until compare match), the TOCi bit is set to 1 (initial output at high until compare match).
Bits IOA2 to IOA0 in the TRDIORAi register are set to 011b (TRDIOAi output inverted by TRDGRAi register compare match).
Bits IOB2 to IOB0 in the TRDIORAi register are set to 010b (TRDIOBi high-level output at TRDGRBi register compare match).
Bits IOC3 to IOC0 in the TRDIORCi register are set to 1001b (TRDIOCi low-level output at TRDGRCi register compare match).
The IOD3 bit in the TRDIORCi register is set to 1 (TRDGRDi register does not control TRDIOBi pin output).

Figure 21.11 Operating Example of Output Compare Function

21.4.21 Changing Output Pins in Registers TRDGRCi (i = 0 or 1) and TRDGRDi

The TRDGRCi register can be used for output control of the TRDIOAi pin, and the TRDGRDi register can be used for output control of the TRDIOBi pin. Therefore, each pin output can be controlled as follows:

- TRDIOAi output is controlled by the values of registers TRDGRAi and TRDGRCi.
- TRDIOBi output is controlled by the values of registers TRDGRBi and TRDGRDi.

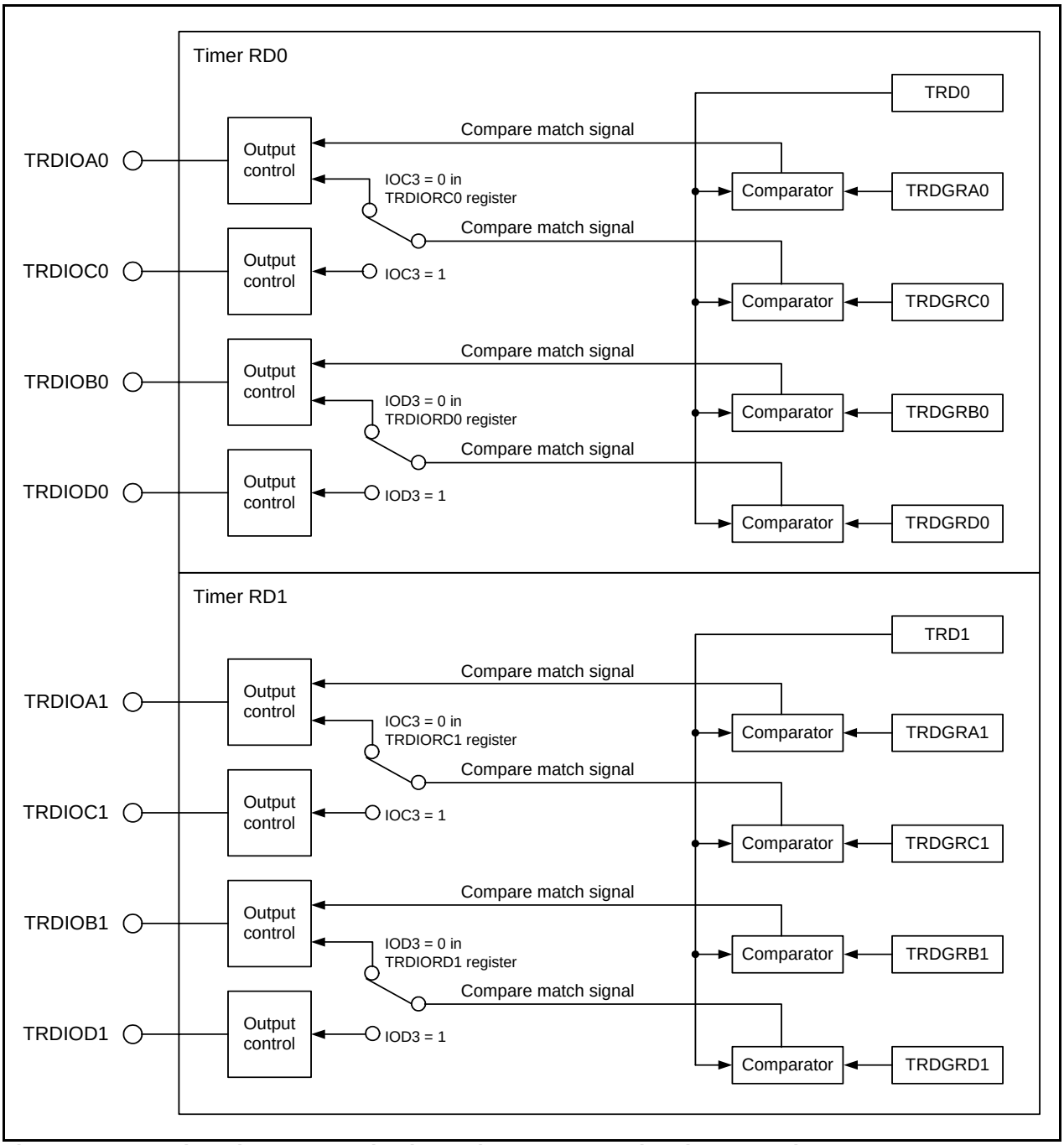
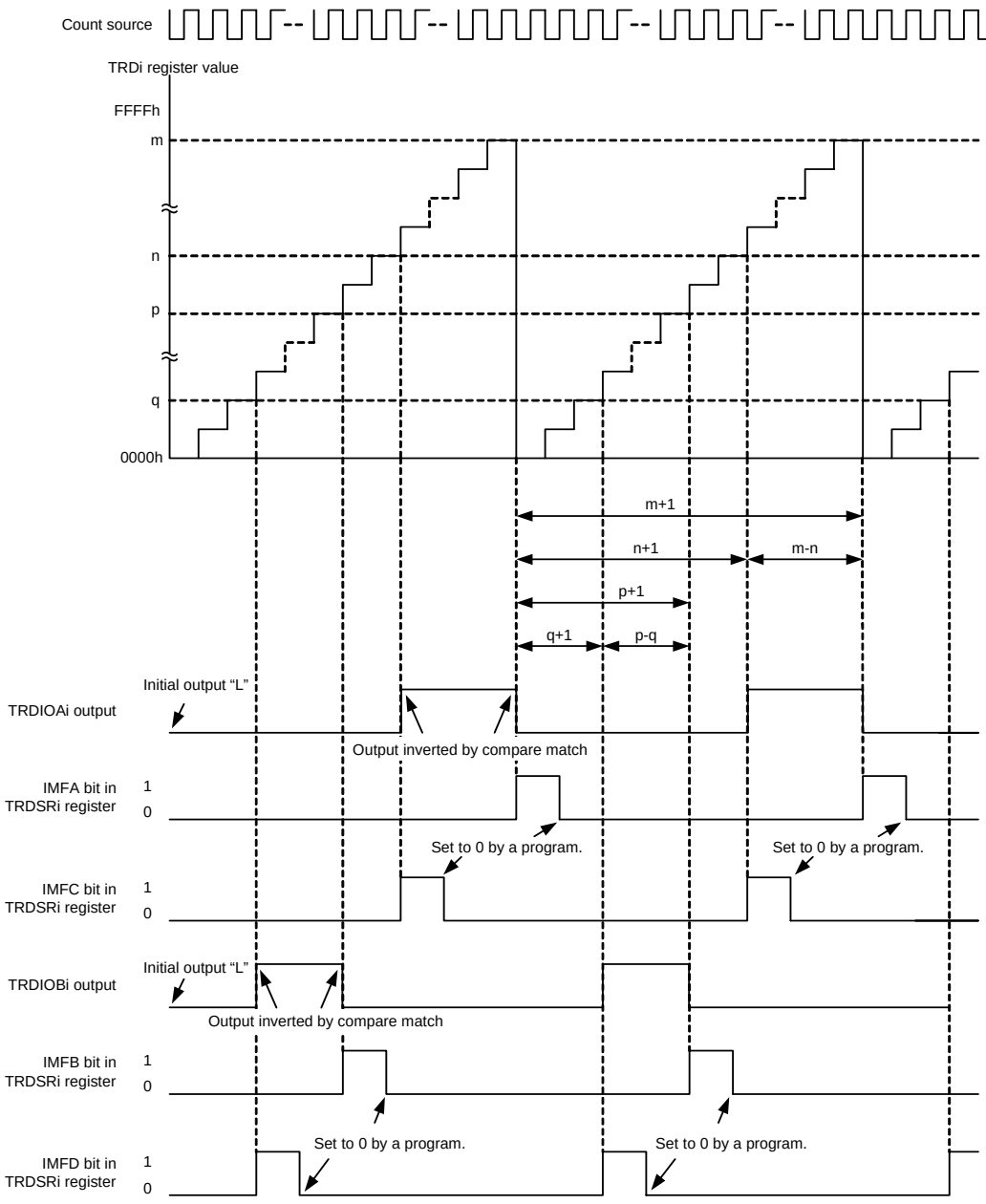


Figure 21.12 Changing Output Pins in Registers TRDGRCi and TRDGRDi

Change output pins in registers TRDGRCi and TRDGRDi as follows:

- Select 0 (change TRDGRji register output pin) by the IOj3 (j = C or D) bit in the TRDIORCi register.
- Set the BFji bit in the TRDMR register to 0 (general register).
- Set different values in registers TRDGRCi and TRDGRAi. Also, set different values in registers TRDGRDi and TRDGRBi.

Figure 21.13 shows an Operating Example When TRDGRCi Register is Used for Output Control of TRDIOAi Pin and TRDGRDi Register is Used for Output Control of TRDIOBi Pin.



The above applies under the following conditions:
The CSELi bit in the TRDSTR register is set to 1 (TRDi register count continues after compare match).
Bits BFCi and BFDi in the TRDMR register are set to 0 (registers TRDGRCi and TRDGRDi are not used as buffer registers).
Bits EAi and EBi in the TRDOER1 register are set to 0 (TRDIOAi and TRDIOBi pin output enabled).
Bits CCLR2 to CCLR0 in the TRDCRi register are set to 001b (TRDi register is set to 0000h by compare match with the TRDGRAi register).
Bits TOAi and TOBi in the TRDOCR register are set to 0 (initial output at low until compare match).
Bits IOA2 to IOA0 in the TRDIORAi register are set to 011b (TRDIOAi output inverted by TRDGRAi register compare match).
Bits IOB2 to IOB0 in the TRDIORAi register are set to 011b (TRDIOBi output inverted by TRDGRBi register compare match).
Bits IOC3 to IOC0 in the TRDIORCi register are set to 0011b (TRDIOAi output inverted by TRDGRCi register compare match).
Bits IOD3 to IOD0 in the TRDIORCi register are set to 0011b (TRDIOBi output inverted by TRDGRDi register compare match).

Figure 21.13 Operating Example When TRDGRCi Register is Used for Output Control of TRDIOAi Pin and TRDGRDi Register is Used for Output Control of TRDIOBi Pin

21.4.22 A/D Trigger Generation

A compare match signal with registers TRDi (i = 0 or 1) and TRDGRji (j = A, B, C, or D) can be used as the conversion start trigger of the A/D converter.
The TRDADCR register is used to select which compare match is used.

21.5 PWM Mode

In PWM mode, a PWM waveform is output. Up to three PWM waveforms with the same period can be output by timer RDi (i = 0 or 1). Also, up to six PWM waveforms with the same period can be output by synchronizing timer RD0 and timer RD1. Since this mode functions by a combination of the TRDIOji (i = 0 or 1, j = B, C, or D) pin and TRDGRji register, PWM mode, or any other mode or function, can be selected for each individual pin. (However, since the TRDGRAi register is used when using any pin for PWM mode, the TRDGRAi register cannot be used for other modes.)
Figure 21.14 shows a Block Diagram of PWM Mode, and Table 21.9 lists the PWM Mode Specifications. Figures 21.15 and 21.16 show Operation Examples in PWM Mode.

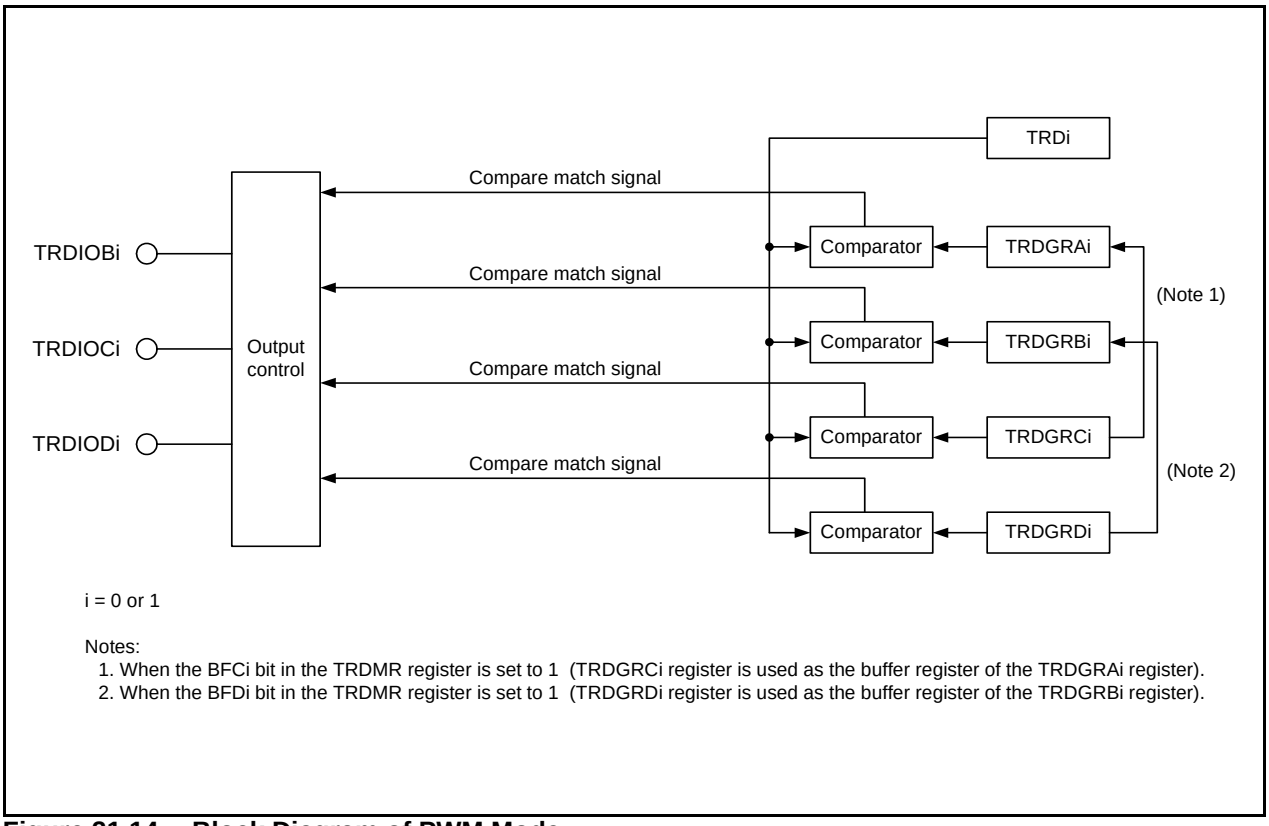
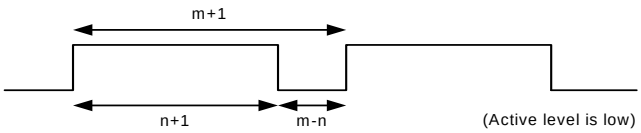


Figure 21.14 Block Diagram of PWM Mode

Table 21.9 PWM Mode Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, fC2, fOCO40M External signal input to the TRDCLK pin (active edge selectable by a program)
Count operations	Increment
PWM waveform	PWM period: 1/fk x (m+1) Active level width: 1/fk x (m-n) Inactive level width: 1/fk x (n+1) fk: Frequency of count source m: Value set in TRDGRAi register n: Value set in TRDGRji register 
Count start condition	1 (count starts) is written to the TSTARTi bit in the TRDSTR register.
Count stop conditions	• 0 (count stops) is written to the TSTARTi bit in the TRDSTR register when the CSELi bit in the TRDSTR register is set to 1. The PWM output pin holds output level before the count stops. • When the CSELi bit in the TRDSTR register is set to 0, the count stops at the compare match with the TRDGRAi register. The PWM output pin holds the level after the output changes by the compare match.
Interrupt request generation timing	• Compare match (the contents of the TRDi register and the TRDGRhi register match.) • TRDi register overflow
TRDIOA0 pin function	Programmable I/O port or TRDCLK (external clock) input
TRDIOA1 pin function	Programmable I/O port
TRDIOB0, TRDIOC0, TRDIOD0, TRDIOB1, TRDIOC1, TRDIOD1 pins function	Programmable I/O port or pulse output (selectable for each individual pin)
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRDi register.
Write to timer	The value can be written to the TRDi register.
Selectable functions	• One to three PWM output pins selectable per timer RDi Either one pin or multiple pins of the TRDIOBi, TRDIOCi or TRDIODi pin. • Active level selectable for each individual pin. • Initial output level selectable for each individual pin. • Synchronous operation (Refer to **21.2.3 Synchronous Operation**.) • Buffer operation (Refer to **21.2.2 Buffer Operation**.) • Pulse output forced cutoff signal input (Refer to **21.2.4 Pulse Output Forced Cutoff**.) • A/D trigger generation

i = 0 or 1
j = either B, C, or D
h = either A, B, C, or D

21.5.1 Module Standby Control Register (MSTCR)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	MSTTRG	MSTTRC	MSTTRD	MSTIIC	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	MSTIIC	SSU, I2C bus standby bit	0: Active 1: Standby (1)	R/W
b4	MSTTRD	Timer RD standby bit	0: Active 1: Standby (2)	R/W
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (3)	R/W
b6	MSTTRG	Timer RG standby bit	0: Active 1: Standby (4)	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. When the MSTIIC bit is set to 1 (standby), any access to the SSU or the I2C bus associated registers (addresses 0193h to 019Dh) is disabled.
2. When the MSTTRD bit is set to 1 (standby), any access to the timer RD associated registers (addresses 0135h to 015Fh) is disabled.
3. When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0133h) is disabled.
4. When the MSTTRG bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0170h to 017Fh) is disabled.

21.5.2 Timer RD Control Expansion Register (TRDECR)

Address 0135h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ITCLK1	—	—	—	ITCLK0	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	ITCLK0	Timer RD0 fC2 select bit	0: TRDCLK input selected 1: fC2 selected	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	ITCLK1	Timer RD1 fC2 select bit	0: TRDCLK input selected 1: fC2 selected	R/W

21.5.3 Timer RD Trigger Control Register (TRDADCR)

Address 0136h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADTRGD1E	ADTRGC1E	ADTRGB1E	ADTRGA1E	ADTRGD0E	ADTRGC0E	ADTRGB0E	ADTRGA0E
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADTRGA0E	A/D trigger A0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRA0	R/W
b1	ADTRGB0E	A/D trigger B0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRB0	R/W
b2	ADTRGC0E	A/D trigger C0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRC0	R/W
b3	ADTRGD0E	A/D trigger D0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRD0	R/W
b4	ADTRGA1E	A/D trigger A1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRA1	R/W
b5	ADTRGB1E	A/D trigger B1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRB1	R/W
b6	ADTRGC1E	A/D trigger C1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRC1	R/W
b7	ADTRGD1E	A/D trigger D1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRD1	R/W

21.5.4 Timer RD Start Register (TRDSTR) in PWM Mode

Address 0137h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	CSEL1	CSEL0	TSTART1	TSTART0
After Reset	1	1	1	1	1	1	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART0	TRD0 count start flag (3)	0: Count stops (1) 1: Count starts	R/W
b1	TSTART1	TRD1 count start flag (4)	0: Count stops (2) 1: Count starts	R/W
b2	CSEL0	TRD0 count operation select bit	0: Count stops at compare match with the TRDGRA0 register 1: Count continues after compare match with the TRDGRA0 register	R/W
b3	CSEL1	TRD1 count operation select bit	0: Count stops at compare match with the TRDGRA1 register 1: Count continues after compare match with the TRDGRA1 register	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	—			

Notes:
1. When the CSEL0 bit is set to 1, write 0 to the TSTART0 bit.
2. When the CSEL1 bit is set to 1, write 0 to the TSTART1 bit.
3. When the CSEL0 bit is set to 0 and the compare match signal (TRDIOA0) is generated, this bit is set to 0 (count stops).
4. When the CSEL1 bit is set to 0 and the compare match signal (TRDIOA1) is generated, this bit is set to 0 (count stops).

Set the TRDSTR register using the MOV instruction (do not use the bit handling instruction). Refer to **21.10.1 TRDSTR Register** for **Notes on Timer RD**.

21.5.5 Timer RD Mode Register (TRDMR) in PWM Mode

Address 0138h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BFD1	BFC1	BFD0	BFC0	—	—	—	SYNC
After Reset	0	0	0	0	1	1	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	SYNC	Timer RD synchronous bit	0: Registers TRD0 and TRD1 operate independently 1: Registers TRD0 and TRD1 operate synchronously	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b2	—			
b3	—			
b4	BFC0	TRDGRC0 register function select bit	0: General register 1: Buffer register of TRDGRA0 register	R/W
b5	BFD0	TRDGRD0 register function select bit	0: General register 1: Buffer register of TRDGRB0 register	R/W
b6	BFC1	TRDGRC1 register function select bit	0: General register 1: Buffer register of TRDGRA1 register	R/W
b7	BFD1	TRDGRD1 register function select bit	0: General register 1: Buffer register of TRDGRB1 register	R/W

21.5.6 Timer RD PWM Mode Register (TRDPMR) in PWM Mode

Address 0139h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	PWMD1	PWMC1	PWMB1	—	PWMD0	PWMC0	PWMB0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PWMB0	PWM mode of TRDIOB0 select bit	0: Timer mode 1: PWM mode	R/W
b1	PWMC0	PWM mode of TRDIOC0 select bit		R/W
b2	PWMD0	PWM mode of TRDIOD0 select bit		R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b4	PWMB1	PWM mode of TRDIOB1 select bit	0: Timer mode 1: PWM mode	R/W
b5	PWMC1	PWM mode of TRDIOC1 select bit		R/W
b6	PWMD1	PWM mode of TRDIOD1 select bit		R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

21.5.7 Timer RD Function Control Register (TRDFCR) in PWM Mode

Address 013Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PWM3	STCLK	ADEG	ADTRG	OLS1	OLS0	CMD1	CMD0
After Reset	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CMD0	Combination mode select bit (1)	Set to 00b (timer mode, PWM mode, or PWM3 mode) in PWM mode.	R/W
b1	CMD1			R/W
b2	OLS0	Normal-phase output level select bit (in reset synchronous PWM mode or complementary PWM mode)	Disabled in PWM mode.	R/W
b3	OLS1	Counter-phase output level select bit (in reset synchronous PWM mode or complementary PWM mode)		R/W
b4	ADTRG	A/D trigger enable bit (in complementary PWM mode)		R/W
b5	ADEG	A/D trigger edge select bit (in complementary PWM mode)		R/W
b6	STCLK	External clock input select bit	0: External clock input disabled 1: External clock input enabled	R/W
b7	PWM3	PWM3 mode select bit (2)	Set to 1 (other than PWM3 mode) in PWM mode.	R/W

Notes:
1. Set bits CMD1 to CMD0 when both the TSTART0 and TSTART1 bits in the TRDSTR register are set to 0 (count stops).
2. When bits CMD1 to CMD0 are set to 00b (timer mode, PWM mode, or PWM3 mode), the setting of the PWM3 bit is enabled.

21.5.8 Timer RD Output Master Enable Register 1 (TRDOER1) in PWM Mode

Address 013Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ED1	EC1	EB1	EA1	ED0	EC0	EB0	EA0
After Reset	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	EA0	TRDIOA0 output disable bit	Set to 1 (TRDIOA0 pin is used as a programmable I/O port) in PWM mode.	R/W
b1	EB0	TRDIOB0 output disable bit	0: Output enabled 1: Output disabled (TRDIOB0 pin is used as a programmable I/O port)	R/W
b2	EC0	TRDIOC0 output disable bit	0: Output enabled 1: Output disabled (TRDIOC0 pin is used as a programmable I/O port)	R/W
b3	ED0	TRDIOD0 output disable bit	0: Output enabled 1: Output disabled (TRDIOD0 pin is used as a programmable I/O port)	R/W
b4	EA1	TRDIOA1 output disable bit	Set to 1 (TRDIOA1 pin is used as a programmable I/O port) in PWM mode.	R/W
b5	EB1	TRDIOB1 output disable bit	0: Output enabled 1: Output disabled (TRDIOB1 pin is used as a programmable I/O port)	R/W
b6	EC1	TRDIOC1 output disable bit	0: Output enabled 1: Output disabled (TRDIOC1 pin is used as a programmable I/O port)	R/W
b7	ED1	TRDIOD1 output disable bit	0: Output enabled 1: Output disabled (TRDIOD1 pin is used as a programmable I/O port)	R/W

21.5.9 Timer RD Output Master Enable Register 2 (TRDOER2) in PWM Mode

Address 013Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PTO	—	—	—	—	—	—	—
After Reset	0	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b1	—			—
b2	—			—
b3	—			—
b4	—			—
b5	—			—
b6	—			—
b7	PTO	$\overline{\text{INT0}}$ of pulse output forced cutoff signal input enabled bit (1)	0: Pulse output forced cutoff input disabled 1: Pulse output forced cutoff input enabled (All bits in the TRDOER1 register are set to 1 (output disabled) when a low-level signal is applied to the $\overline{\text{INT0}}$ pin.)	R/W

Note:
1. Refer to **21.2.4 Pulse Output Forced Cutoff**.

21.5.10 Timer RD Output Control Register (TRDOCR) in PWM Mode

Address 013Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TOD1	TOC1	TOB1	TOA1	TOD0	TOC0	TOB0	TOA0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA0	TRDIOA0 output level select bit	Set to 0 (output enabled) in PWM mode.	R/W
b1	TOB0	TRDIOB0 output level select bit (1)	0: Initial output is inactive level 1: Initial output is active level	R/W
b2	TOC0	TRDIOC0 initial output level select bit (1)		R/W
b3	TOD0	TRDIOD0 initial output level select bit (1)		R/W
b4	TOA1	TRDIOA1 initial output level select bit	Set this bit to 0 (output enabled) in PWM mode.	R/W
b5	TOB1	TRDIOB1 initial output level select bit (1)	0: Inactive level 1: Active level	R/W
b6	TOC1	TRDIOC1 initial output level select bit (1)		R/W
b7	TOD1	TRDIOD1 initial output level select bit (1)		R/W

Note:
1. If the pin function is set for waveform output (refer to **7.5 Port Settings**), the initial output level is output when the TRDOCR register is set.

   Write to the TRDOCR register when both the TSTART0 and TSTART1 bits in the TRDSTR register are set to 0 (count stops).

21.5.11 Timer RD Control Register i (TRDCRi) (i = 0 or 1) in PWM Mode

Address 0140h (TRDCR0), 0150h (TRDCR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TCK2	TCK1	TCK0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TCK0	Count source select bit	b2 b1 b0 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRDCLK input (1) or fC2 (2) 1 1 0: fOCO40M 1 1 1: Do not set.	R/W
b1	TCK1			R/W
b2	TCK2			R/W
b3	CKEG0	External clock edge select bit (3)	b4 b3 0 0: Count at the rising edge 0 1: Count at the falling edge 1 0: Count at both edges 1 1: Do not set.	R/W
b4	CKEG1			R/W
b5	CCLR0	TRDi counter clear select bit	Set to 001b (TRDi register cleared by compare match with TRDGRAi register) in PWM mode.	R/W
b6	CCLR1			R/W
b7	CCLR2			R/W

Notes:
1. Enabled when the ITCLKi bit in the TRDECR register is set to 0 (TRDCLK input) and the STCLK bit in the TRDFCR register is 1 (external clock input enabled).
2. Enabled when the ITCLKi bit in the TRDECR register is set to 1 (fC2).
3. Enabled when bits TCK2 to TCK0 are set to 101b (TRDCLK input or fC2), the ITCLKi bit in the TRDECR is set to 0 (TRDCLK input), and the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).

21.5.12 Timer RD Status Register i (TRDSRi) (i = 0 or 1) in PWM Mode

Address 0143h (TRDSR0), 0153h (TRDSR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	UDF	OVF	IMFD	IMFC	IMFB	IMFA	
After Reset	1	1	1	0	0	0	0	0	TRDSR0 register
After Reset	1	1	0	0	0	0	0	0	TRDSR1 register

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input-capture/compare-match flag A	[Condition for setting this bit to 0] Write 0 after reading. (2) [Condition for setting this bit to 1] When the TRDi register value matches the TRDGRAi register value.	R/W
b1	IMFB	Input-capture/compare-match flag B	[Condition for setting this bit to 0] Write 0 after reading. (2) [Condition for setting this bit to 1] When the TRDi register value matches the TRDGRBi register value.	R/W
b2	IMFC	Input-capture/compare-match flag C	[Condition for setting this bit to 0] Write 0 after reading. (2) [Condition for setting this bit to 1] When the TRDi register value matches the TRDGRCi register value. (3)	R/W
b3	IMFD	Input-capture/compare-match flag D	[Condition for setting this bit to 0] Write 0 after reading. (2) [Condition for setting this bit to 1] When the TRDi register value matches the TRDGRDi register value. (3)	R/W
b4	OVF	Overflow flag	[Condition for setting this bit to 0] Write 0 after reading. (2) [Condition for setting this bit to 1] When the TRDi register overflows.	R/W
b5	UDF	Underflow flag (1)	This bit is disabled in PWM Mode.	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b7	—			

Notes:
1. Nothing is assigned to b5 in the TRDSR0 register. If necessary, write 0 to b5. When read, the content is 1.
2. The results of writing to these bits are as follows:
   - The bit is set to 0 when it is first read as 1 and then 0 is written to it.
   - The bit remains unchanged even if it is first read as 0 and then 0 is written to it because its previous value is retained. (The bit's value remains 1 even if it is set to 1 from 0 after being read as 0 and having 0 written to it because its previous value is retained.)
   - The bit's value remains unchanged if 1 is written to it.
3. Including when the BFji bit in the TRDMR register is set to 1 (TRDGRji is used as a buffer register).

21.5.13 Timer RD Interrupt Enable Register i (TRDIERi) (i = 0 or 1) in PWM Mode

Address 0144h (TRDIER0), 0154h (TRDIER1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	OVIE	IMIED	IMIEC	IMIEB	IMIEA
After Reset	1	1	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input-capture/compare-match interrupt enable bit A	0: Interrupt (IMIA) by IMFA bit disabled 1: Interrupt (IMIA) by IMFA bit enabled	R/W
b1	IMIEB	Input-capture/compare-match interrupt enable bit B	0: Interrupt (IMIB) by IMFB bit disabled 1: Interrupt (IMIB) by IMFB bit enabled	R/W
b2	IMIEC	Input-capture/compare-match interrupt enable bit C	0: Interrupt (IMIC) by IMFC bit disabled 1: Interrupt (IMIC) by IMFC bit enabled	R/W
b3	IMIED	Input-capture/compare-match interrupt enable bit D	0: Interrupt (IMID) by IMFD bit disabled 1: Interrupt (IMID) by IMFD bit enabled	R/W
b4	OVIE	Overflow/underflow interrupt enable bit	0: Interrupt (OVI) by OVF bit disabled 1: Interrupt (OVI) by OVF bit enabled	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b6	—			
b7	—			

21.5.14 Timer RD PWM Mode Output Level Control Register i (TRDPOCRi) (i = 0 or 1) in PWM Mode

Address 0145h (TRDPOCR0), 0155h (TRDPOCR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	POLD	POLC	POLB
After Reset	1	1	1	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POLB	PWM mode output level control bit B	0: TRDIOBi output level is selected as low active 1: TRDIOBi output level is selected as high active	R/W
b1	POLC	PWM mode output level control bit C	0: TRDIOCi output level is selected as low active 1: TRDIOCi output level is selected as high active	R/W
b2	POLD	PWM mode output level control bit D	0: TRDIODi output level is selected as low active 1: TRDIODi output level is selected as high active	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b4	—			
b5	—			
b6	—			
b7	—			

21.5.15 Timer RD Counter i (TRDi) (i = 0 or 1) in PWM Mode

Address 0147h to 0146h (TRD0), 0157h to 0156h (TRD1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	A count source is counted. Count operation is increment. When an overflow occurs, the OVF bit in the TRDSRi register is set to 1.	0000h to FFFFh	R/W

Access the TRDi register in 16-bit units. Do not access it in 8-bit units.

21.5.16 Timer RD General Registers Ai, Bi, Ci, and Di (TRDGRAi, TRDGRBi, TRDGRCi, TRDGRDi) (i = 0 or 1) in PWM Mode

Address 0149h to 0148h (TRDGRA0), 014Bh to 014Ah (TRDGRB0),
014Dh to 014Ch (TRDGRC0), 014Fh to 014Eh (TRDGRD0),
0159h to 0158h (TRDGRA1), 015Bh to 015Ah (TRDGRB1),
015Dh to 015Ch (TRDGRC1), 015Fh to 015Eh (TRDGRD1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b15 to b0	Refer to **Table 21.10 TRDGRji Register Functions in PWM Mode**	R/W

Access registers TRDGRAi to TRDGRDi in 16-bit units. Do not access them in 8-bit units.

The following registers are disabled in PWM mode:
TRDDF0, TRDDF1, TRDIORA0, TRDIORC0, TRDIORA1, and TRDIORC1.

Table 21.10 TRDGRji Register Functions in PWM Mode

Register	Setting	Register Function	PWM Output Pin
TRDGRAi	–	General register. Set the PWM period	–
TRDGRBi	–	General register. Set the changing point of PWM output	TRDIOBi
TRDGRCi	BFCi = 0	General register. Set the changing point of PWM output	TRDIOCi
TRDGRDi	BFDi = 0		TRDIODi
TRDGRCi	BFCi = 1	Buffer register. Set the next PWM period (Refer to **21.2.2 Buffer Operation**.)	–
TRDGRDi	BFDi = 1	Buffer register. Set the changing point of the next PWM output (Refer to **21.2.2 Buffer Operation**.)	TRDIOBi

i = 0 or 1
BFCi, BFDi: Bits in TRDMR register

21.5.17 Timer RD Pin Select Register 0 (TRDPSR0)

Address 0184h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRDIOD0SEL1	TRDIOD0SEL0	TRDIOC0SEL1	TRDIOC0SEL0	TRDIOB0SEL1	TRDIOB0SEL0	TRDIOA0SEL1	TRDIOA0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRDIOA0SEL0	TRDIOA0/TRDCLK pin select bit	b1 b0 0 0: TRDIOA0/TRDCLK pin not used 0 1: P6_0 assigned 1 0: P10_0 assigned 1 1: Do not set.	R/W
b1	TRDIOA0SEL1			R/W
b2	TRDIOB0SEL0	TRDIOB0 pin select bit	b3 b2 0 0: TRDIOB0 pin not used 0 1: P6_1 assigned 1 0: P10_1 assigned 1 1: Do not set.	R/W
b3	TRDIOB0SEL1			R/W
b4	TRDIOC0SEL0	TRDIOC0 pin select bit	b5 b4 0 0: TRDIOC0 pin not used 0 1: P6_2 assigned 1 0: P10_2 assigned 1 1: Do not set.	R/W
b5	TRDIOC0SEL1			R/W
b6	TRDIOD0SEL0	TRDIOD0 pin select bit	b7 b6 0 0: TRDIOC0 pin not used 0 1: P6_3 assigned 1 0: P10_3 assigned 1 1: Do not set.	R/W
b7	TRDIOD0SEL1			R/W

The TRDPSR0 register selects which pin is assigned as the timer RD input/output. To use the I/O pins for timer RD, set this register.

Set the TRDPSR0 register before setting the timer RD associated registers. Also, do not change the setting value of this register during timer RD operation.

21.5.18 Timer RD Pin Select Register 1 (TRDPSR1)

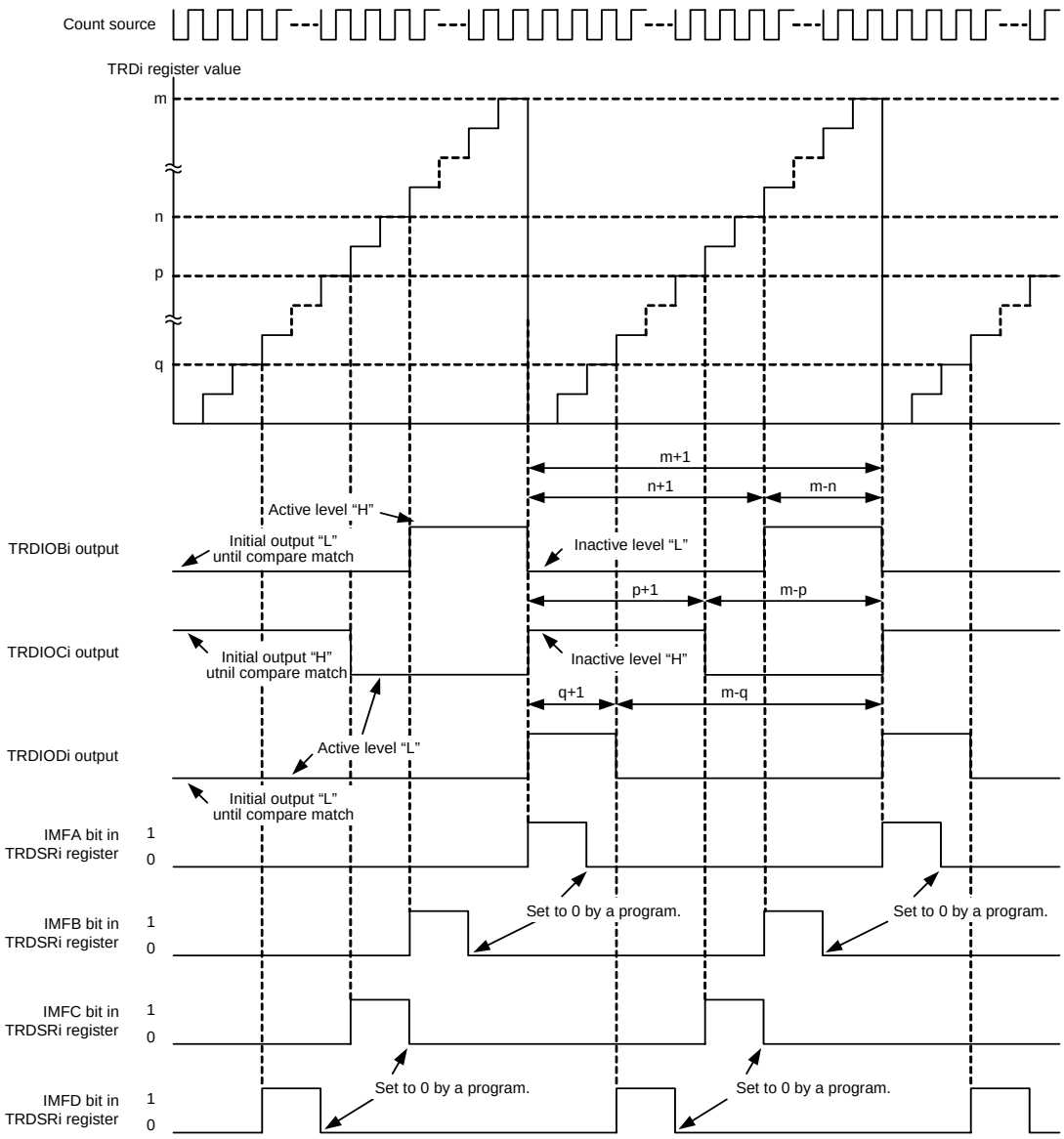
Address 0185h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRDIOD1SEL1	TRDIOD1SEL0	TRDIOC1SEL1	TRDIOC1SEL0	TRDIOB1SEL1	TRDIOB1SEL0	TRDIOA1SEL1	TRDIOA1SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRDIOA1SEL0	TRDIOA1 pin select bit	b1 b0 0 0: TRDIOA1 pin not used 0 1: P6_4 assigned 1 0: P10_4 assigned 1 1: Do not set.	R/W
b1	TRDIOA1SEL1			R/W
b2	TRDIOB1SEL0	TRDIOB1 pin select bit	b3 b2 0 0: TRDIOB1 pin not used 0 1: P6_5 assigned 1 0: P10_5 assigned 1 1: Do not set.	R/W
b3	TRDIOB1SEL1			R/W
b4	TRDIOC1SEL0	TRDIOC1 pin select bit	b5 b4 0 0: TRDIOC1 pin not used 0 1: P6_6 assigned 1 0: P10_6 assigned 1 1: Do not set.	R/W
b5	TRDIOC1SEL1			R/W
b6	TRDIOD1SEL0	TRDIOD1 pin select bit	b7 b6 0 0: TRDIOC1 pin not used 0 1: P6_7 assigned 1 0: P10_7 assigned 1 1: Do not set.	R/W
b7	TRDIOD1SEL1			R/W

The TRDPSR1 register selects which pin is assigned as the timer RD input/output. To use the I/O pins for timer RD, set this register.
Set the TRDPSR1 register before setting the timer RD associated registers. Also, do not change the setting value of this register during timer RD operation.

21.5.19 Operating Example

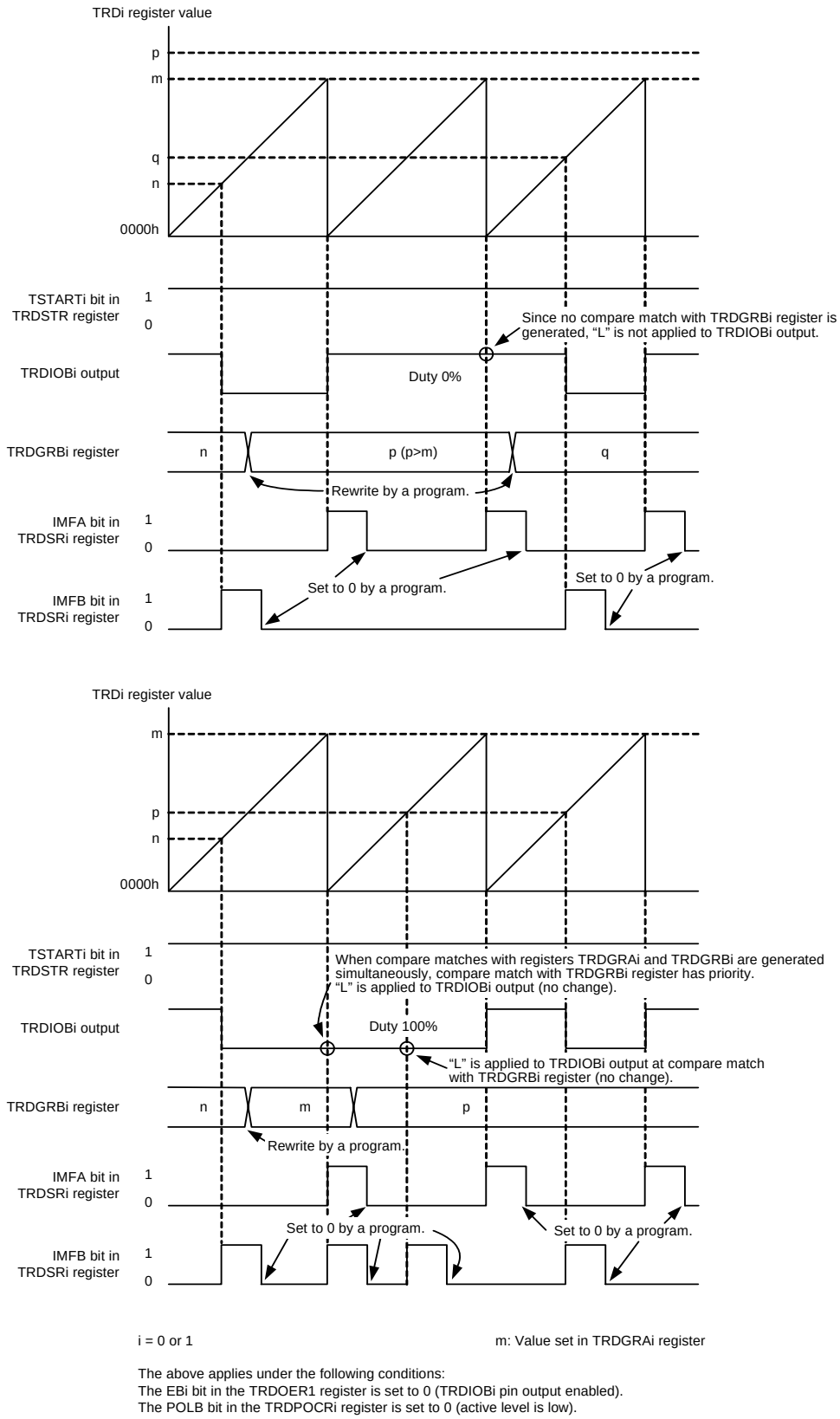


i = 0 or 1

m: Value set in TRDGRAi register
n: Value set in TRDGRBi register
p: Value set in TRDGRCi register
q: Value set in TRDGRDi register

The above applies under the following conditions:
Bits BFCi and BFDi in the TRDMR register are set to 0 (registers TRDGRCi and TRDGRDi are not used as buffer registers).
Bits EBi, ECi and EDi in the TRDOER1 register are set to 0 (TRDIOBi, TRDIOCi and TRDIODi pin output enabled).
Bits TOBi and TOCi in the TRDOCR register are set to 0 (inactive level), the TODi bit is set to 1 (active level).
The POLB bit in the TRDPOCRi register is set to 1 (active level is high), bits POLC and POLD are set to 0 (active level is low).

Figure 21.15 Operating Example in PWM Mode



i = 0 or 1

m: Value set in TRDGRAi register

The above applies under the following conditions:
The EBi bit in the TRDOER1 register is set to 0 (TRDIOBi pin output enabled).
The POLB bit in the TRDPOCRi register is set to 0 (active level is low).

Figure 21.16 Operating Example in PWM Mode (Duty 0%, Duty 100%)

21.5.20 A/D Trigger Generation

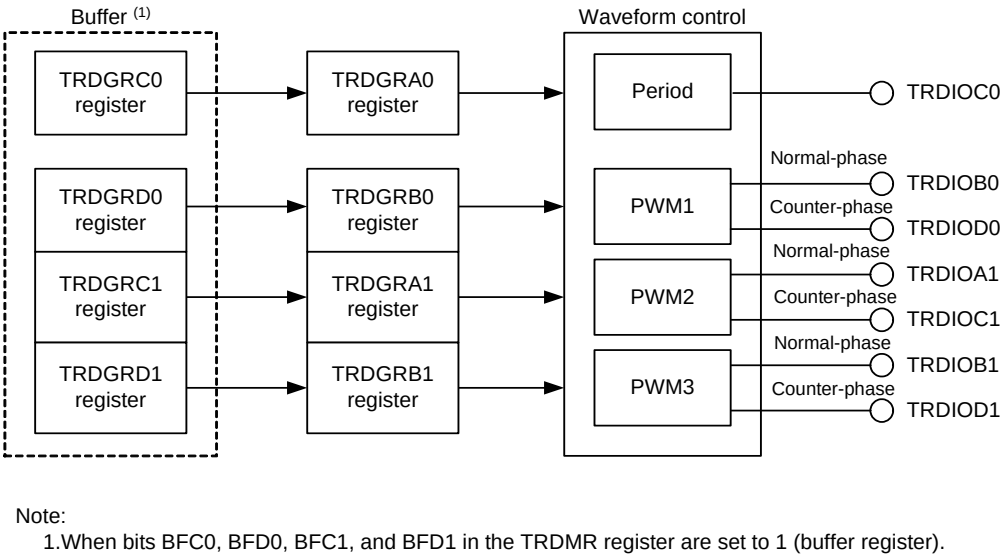
A compare match signal with registers TRDi (i = 0 or 1) and TRDGRji (j = A, B, C, or D) can be used as the conversion start trigger of the A/D converter.
The TRDADCR register is used to select which compare match is used.

21.6 Reset Synchronous PWM Mode

In this mode, three normal-phases and three counter-phases of the PWM waveform are output with the same period (three-phase, sawtooth wave modulation, and no dead time).

Figure 21.17 shows a Block Diagram of Reset Synchronous PWM Mode, and Table 21.11 lists the Reset Synchronous PWM Mode Specifications. Figure 21.18 shows an Operating Example in Reset Synchronous PWM Mode.

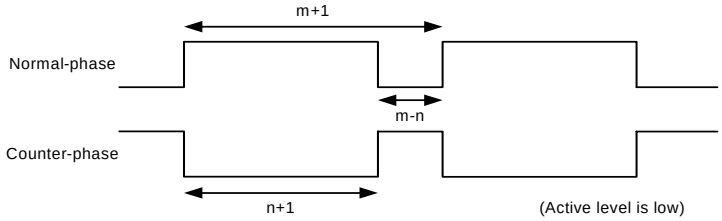
Refer to **Figure 21.16 Operating Example in PWM Mode (Duty 0%, Duty 100%)** for an operating example in PWM Mode with duty 0% and duty 100%.



Note:
1.When bits BFC0, BFD0, BFC1, and BFD1 in the TRDMR register are set to 1 (buffer register).

Figure 21.17 Block Diagram of Reset Synchronous PWM Mode

Table 21.11 Reset Synchronous PWM Mode Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, fC2, fOCO40M External signal input to the TRDCLK pin (active edge selectable by a program)
Count operations	The TRD0 register is incremented (TRD1 register is not used).
PWM waveform	PWM period : 1/fk × (m+1) Active level width of normal-phase : 1/fk × (m-n) Active level width of counter-phase: 1/fk × (n+1) fk: Frequency of count source m: Value set in TRDGRA0 register n: Value set in TRDGRB0 register (PWM1 output), Value set in TRDGRA1 register (PWM2 output), Value set in TRDGRB1 register (PWM3 output) 
Count start condition	1 (count starts) is written to the TSTART0 bit in the TRDSTR register.
Count stop conditions	• 0 (count stops) is written to the TSTART0 bit in the TRDSTR register when the CSEL0 bit in the TRDSTR register is set to 1. The PWM output pin holds the output level before the count stops • When the CSEL0 bit in the TRDSTR register is set to 0, the count stops at the compare match with the TRDGRA0 register. The PWM output pin holds the level after the output changes by the compare match.
Interrupt request generation timing	• Compare match (the content of the TRD0 register matches the contents of registers TRDGRj0, TRDGRA1, and TRDGRB1). • TRD0 register overflow
TRDIOA0 pin function	Programmable I/O port or TRDCLK (external clock) input
TRDIOB0 pin function	PWM1 output normal-phase output
TRDIOD0 pin function	PWM1 output counter-phase output
TRDIOA1 pin function	PWM2 output normal-phase output
TRDIOC1 pin function	PWM2 output counter-phase output
TRDIOB1 pin function	PWM3 output normal-phase output
TRDIOD1 pin function	PWM3 output counter-phase output
TRDIOC0 pin function	Output inverted every PWM period
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRD0 register.
Write to timer	The value can be written to the TRD0 register.
Selectable functions	• The normal-phase and counter-phase active level and initial output level can be selected individually. • Buffer operation (Refer to **21.2.2 Buffer Operation**.) • Pulse output forced cutoff signal input (Refer to **21.2.4 Pulse Output Forced Cutoff**.) • A/D trigger generation

j = either A, B, C, or D

21.6.1 Module Standby Control Register (MSTCR)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	MSTTRG	MSTTRC	MSTTRD	MSTIIC	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	MSTIIC	SSU, I^2C bus standby bit	0: Active 1: Standby (1)	R/W
b4	MSTTRD	Timer RD standby bit	0: Active 1: Standby (2)	R/W
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (3)	R/W
b6	MSTTRG	Timer RG standby bit	0: Active 1: Standby (4)	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. When the MSTIIC bit is set to 1 (standby), any access to the SSU or the I^2C bus associated registers (addresses 0193h to 019Dh) is disabled.
2. When the MSTTRD bit is set to 1 (standby), any access to the timer RD associated registers (addresses 0135h to 015Fh) is disabled.
3. When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0133h) is disabled.
4. When the MSTTRG bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0170h to 017Fh) is disabled.

21.6.2 Timer RD Control Expansion Register (TRDECR)

Address 0135h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ITCLK1	—	—	—	ITCLK0	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	ITCLK0	Timer RD0 fC2 select bit	0: TRDCLK input selected 1: fC2 selected	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	ITCLK1	Timer RD1 fC2 select bit	0: TRDCLK input selected 1: fC2 selected	R/W

21.6.3 Timer RD Trigger Control Register (TRDADCR)

Address 0136h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADTRGD1E	ADTRGC1E	ADTRGB1E	ADTRGA1E	ADTRGD0E	ADTRGC0E	ADTRGB0E	ADTRGA0E
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADTRGA0E	A/D trigger A0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRA0	R/W
b1	ADTRGB0E	A/D trigger B0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRB0	R/W
b2	ADTRGC0E	A/D trigger C0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRC0	R/W
b3	ADTRGD0E	A/D trigger D0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRD0	R/W
b4	ADTRGA1E	A/D trigger A1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRA1	R/W
b5	ADTRGB1E	A/D trigger B1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRB1	R/W
b6	ADTRGC1E	A/D trigger C1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRC1	R/W
b7	ADTRGD1E	A/D trigger D1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRD1	R/W

21.6.4 Timer RD Start Register (TRDSTR) in Reset Synchronous PWM Mode

Address 0137h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	CSEL1	CSEL0	TSTART1	TSTART0
After Reset	1	1	1	1	1	1	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART0	TRD0 count start flag (3)	0: Count stops (1) 1: Count starts	R/W
b1	TSTART1	TRD1 count start flag (4)	0: Count stops (2) 1: Count starts	R/W
b2	CSEL0	TRD0 count operation select bit	0: Count stops at compare match with the TRDGRA0 register 1: Count continues after compare match with the TRDGRA0 register	R/W
b3	CSEL1	TRD1 count operation select bit	0: Count stops at compare match with the TRDGRA1 register 1: Count continues after compare match with the TRDGRA1 register	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	—			

Notes:
1. When the CSEL0 bit is set to 1, write 0 to the TSTART0 bit.
2. When the CSEL1 bit is set to 1, write 0 to the TSTART1 bit.
3. When the CSEL0 bit is set to 0 and the compare match signal (TRDIOA0) is generated, this bit is set to 0 (count stops).
4. When the CSEL1 bit is set to 0 and the compare match signal (TRDIOA1) is generated, this bit is set to 0 (count stops).

Set the TRDSTR register using the MOV instruction (do not use the bit handling instruction). Refer to **21.10.1 TRDSTR Register** for **Notes on Timer RD**.

21.6.5 Timer RD Mode Register (TRDMR) in Reset Synchronous PWM Mode

Address 0138h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BFD1	BFC1	BFD0	BFC0	—	—	—	SYNC
After Reset	0	0	0	0	1	1	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	SYNC	Timer RD synchronous bit	Set to 0 (registers TRD and TRD1 operate independently) in reset synchronous PWM mode.	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b2	—			
b3	—			
b4	BFC0	TRDGRC0 register function select bit	0: General register 1: Buffer register of TRDGRA0 register	R/W
b5	BFD0	TRDGRD0 register function select bit	0: General register 1: Buffer register of TRDGRB0 register	R/W
b6	BFC1	TRDGRC1 register function select bit	0: General register 1: Buffer register of TRDGRA1 register	R/W
b7	BFD1	TRDGRD1 register function select bit	0: General register 1: Buffer register of TRDGRB1 register	R/W

21.6.6 Timer RD Function Control Register (TRDFCR) in Reset Synchronous PWM Mode

Address 013Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PWM3	STCLK	ADEG	ADTRG	OLS1	OLS0	CMD1	CMD0
After Reset	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CMD0	Combination mode select bit (1, 2)	Set to 01b (reset synchronous PWM mode) in reset synchronous PWM mode.	R/W
b1	CMD1			R/W
b2	OLS0	Normal-phase output level select bit (in reset synchronous PWM mode or complementary PWM mode)	0: Initial output at high, active level is low 1: Initial output at low, active level is high	R/W
b3	OLS1	Counter-phase output level select bit (in reset synchronous PWM mode or complementary PWM mode)		R/W
b4	ADTRG	A/D trigger enable bit (in complementary PWM mode)	Disabled in reset synchronous PWM mode.	R/W
b5	ADEG	A/D trigger edge select bit (in complementary PWM mode)		R/W
b6	STCLK	External clock input select bit	0: External clock input disabled 1: External clock input enabled	R/W
b7	PWM3	PWM3 mode select bit (3)	Disabled in reset synchronous PWM mode.	R/W

Notes:
1. When bits CMD1 to CMD0 are set to 01b, 10b, or 11b, the MCU enters reset synchronous PWM mode or complementary PWM mode in spite of the setting of the TRDPMR register.
2. Set bits CMD1 to CMD0 when both the TSTART0 and TSTART1 bits are set to 0 (count stops).
3. When bits CMD1 to CMD0 are set to 00b (timer mode, PWM mode, or PWM3 mode), the setting of the PWM3 bit is enabled.

21.6.7 Timer RD Output Master Enable Register 1 (TRDOER1) in Reset Synchronous PWM Mode

Address 013Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ED1	EC1	EB1	EA1	ED0	EC0	EB0	EA0
After Reset	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	EA0	TRDIOA0 output disable bit	Set to 1 (TRDIOA0 pin is used as a programmable I/O port) in reset synchronous PWM mode.	R/W
b1	EB0	TRDIOB0 output disable bit	0: Output enabled 1: Output disabled (TRDIOB0 pin is used as a programmable I/O port)	R/W
b2	EC0	TRDIOC0 output disable bit	0: Output enabled 1: Output disabled (TRDIOC0 pin is used as a programmable I/O port)	R/W
b3	ED0	TRDIOD0 output disable bit	0: Output enabled 1: Output disabled (TRDIOD0 pin is used as a programmable I/O port)	R/W
b4	EA1	TRDIOA1 output disable bit	0: Output enabled 1: Output disabled (TRDIOA1 pin is used as a programmable I/O port)	R/W
b5	EB1	TRDIOB1 output disable bit	0: Output enabled 1: Output disabled (TRDIOB1 pin is used as a programmable I/O port)	R/W
b6	EC1	TRDIOC1 output disable bit	0: Output enabled 1: Output disabled (TRDIOC1 pin is used as a programmable I/O port)	R/W
b7	ED1	TRDIOD1 output disable bit	0: Output enabled 1: Output disabled (TRDIOD1 pin is used as a programmable I/O port)	R/W

21.6.8 Timer RD Output Master Enable Register 2 (TRDOER2) in Reset Synchronous PWM Mode

Address 013Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PTO	—	—	—	—	—	—	—
After Reset	0	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b1	—			—
b2	—			—
b3	—			—
b4	—			—
b5	—			—
b6	—			—
b7	PTO	$\overline{\text{INT0}}$ of pulse output forced cutoff signal input enabled bit (1)	0: Pulse output forced cutoff input disabled 1: Pulse output forced cutoff input enabled (All bits in the TRDOER1 register are set to 1 (output disabled) when a low-level signal is applied to the $\overline{\text{INT0}}$ pin.)	R/W

Note:
1. Refer to **21.2.4 Pulse Output Forced Cutoff**.

21.6.9 Timer RD Control Register 0 (TRDCR0) in Reset Synchronous PWM Mode

Address 0140h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TCK2	TCK1	TCK0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TCK0	Count source select bit	b2 b1 b0 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRDCLK input (1) or fC2 (2) 1 1 0: fOCO40M 1 1 1: Do not set.	R/W
b1	TCK1			R/W
b2	TCK2			R/W
b3	CKEG0	External clock edge select bit (3)	b4 b3 0 0: Count at the rising edge 0 1: Count at the falling edge 1 0: Count at both edges 1 1: Do not set.	R/W
b4	CKEG1			R/W
b5	CCLR0	TRD0 counter clear select bit	Set to 001b (TRD0 register cleared at compare match with TRDGRA0 register) in reset synchronous PWM mode.	R/W
b6	CCLR1			R/W
b7	CCLR2			R/W

Notes:
1. Enabled when the ITCLKi bit in the TRDECR register is set to 0 (TRDCLK input) and the STCLK bit in the TRDFCR register is 1 (external clock input enabled).
2. Enabled when the ITCLKi bit in the TRDECR register is set to 1 (fC2).
3. Enabled when bits TCK2 to TCK0 are set to 101b (TRDCLK input or fC2), the ITCLKi bit in the TRDECR is set to 0 (TRDCLK input), and the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).

The TRDCR1 register is not used in reset synchronous PWM mode.

21.6.10 Timer RD Status Register i (TRDSRi) (i = 0 or 1) in Reset Synchronous PWM Mode

Address 0143h (TRDSR0), 0153h (TRDSR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	UDF	OVF	IMFD	IMFC	IMFB	IMFA	
After Reset	1	1	1	0	0	0	0	0	TRDSR0 register
After Reset	1	1	0	0	0	0	0	0	TRDSR1 register

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input-capture/compare-match flag A	[Condition for setting this bit to 0] Write 0 after reading. (2) [Condition for setting this bit to 1] When the TRDi register value matches the TRDGRAi register value.	R/W
b1	IMFB	Input-capture/compare-match flag B	[Condition for setting this bit to 0] Write 0 after reading. (2) [Condition for setting this bit to 1] When the TRDi register value matches the TRDGRBi register value.	R/W
b2	IMFC	Input-capture/compare-match flag C	[Condition for setting this bit to 0] Write 0 after reading. (2) [Condition for setting this bit to 1] When the TRDi register value matches the TRDGRCi register value (3).	R/W
b3	IMFD	Input-capture/compare-match flag D	[Condition for setting this bit to 0] Write 0 after reading. (2) [Condition for setting this bit to 1] When the TRDi register value matches the TRDGRDi register value (3).	R/W
b4	OVF	Overflow flag	[Condition for setting this bit to 0] Write 0 after reading (2) [Condition for setting this bit to 1] When the TRDi register overflows.	R/W
b5	UDF	Underflow flag (1)	This bit is disabled in reset synchronous PWM mode.	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b7	—			

Notes:
1. Nothing is assigned to b5 in the TRDSR0 register. If necessary, write 0 to b5. When read, the content is 1.
2. The results of writing to these bits are as follows:
   - The bit is set to 0 when it is first read as 1 and then 0 is written to it.
   - The bit remains unchanged even if it is first read as 0 and then 0 is written to it because its previous value is retained. (The bit's value remains 1 even if it is set to 1 from 0 after being read as 0 and having 0 written to it because its previous value is retained.)
   - The bit's value remains unchanged if 1 is written to it.
3. Including when the BFji bit in the TRDMR register is set to 1 (TRDGRji is used as a buffer register).

21.6.11 Timer RD Interrupt Enable Register i (TRDIERi) (i = 0 or 1) in Reset Synchronous PWM Mode

Address 0144h (TRDIER0), 0154h (TRDIER1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	OVIE	IMIED	IMIEC	IMIEB	IMIEA
After Reset	1	1	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input-capture/compare-match interrupt enable bit A	0: Interrupt (IMIA) by IMFA bit disabled 1: Interrupt (IMIA) by IMFA bit enabled	R/W
b1	IMIEB	Input-capture/compare-match interrupt enable bit B	0: Interrupt (IMIB) by IMFB bit disabled 1: Interrupt (IMIB) by IMFB bit enabled	R/W
b2	IMIEC	Input-capture/compare-match interrupt enable bit C	0: Interrupt (IMIC) by IMFC bit disabled 1: Interrupt (IMIC) by IMFC bit enabled	R/W
b3	IMIED	Input-capture/compare-match interrupt enable bit D	0: Interrupt (IMID) by IMFD bit disabled 1: Interrupt (IMID) by the IMFD bit enabled	R/W
b4	OVIE	Overflow/underflow interrupt enable bit	0: Interrupt (OVI) by OVF bit disabled 1: Interrupt (OVI) by OVF bit enabled	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b6	—			
b7	—			

21.6.12 Timer RD Counter 0 (TRD0) in Reset Synchronous PWM Mode

Address 0147h to 0146h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	A count source is counted. Count operation is increment. When an overflow occurs, the OVF bit in the TRDSR0 register is set to 1.	0000h to FFFFh	R/W

Access the TRD0 register in 16-bit units. Do not access it in 8-bit units.
The TRD1 register is not used in reset synchronous PWM mode.

21.6.13 Timer RD General Registers Ai, Bi, Ci, and Di (TRDGRAi, TRDGRBi, TRDGRCi, TRDGRDi) (i = 0 or 1) in Reset Synchronous PWM Mode

Address 0149h to 0148h (TRDGRA0), 014Bh to 014Ah (TRDGRB0),
014Dh to 014Ch (TRDGRC0), 014Fh to 014Eh (TRDGRD0),
0159h to 0158h (TRDGRA1), 015Bh to 015Ah (TRDGRB1),
015Dh to 015Ch (TRDGRC1), 015Fh to 015Eh (TRDGRD1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b15 to b0	Refer to **Table 21.12 TRDGRji Register Functions in Reset Synchronous PWM Mode**	R/W

Access registers TRDGRAi to TRDGRDi in 16-bit units. Do not access them in 8-bit units.

The following registers are disabled in reset synchronous PWM mode:
TRDPMR, TRDOCR, TRDDF0, TRDDF1, TRDIORA0, TRDIORC0, TRDPOCR0, TRDIORA1, TRDIORC1, and TRDPOCR1.

Table 21.12 TRDGRji Register Functions in Reset Synchronous PWM Mode

Register	Setting	Register Function	PWM Output Pin
TRDGRA0	–	General register. Set the PWM period.	(Output inverted every PWM period and TRDIOC0 pin)
TRDGRB0	–	General register. Set the changing point of PWM1 output.	TRDIOB0 TRDIOD0
TRDGRC0	BFC0 = 0	(These registers are not used in reset synchronous PWM mode.)	–
TRDGRD0	BFD0 = 0		
TRDGRA1	–	General register. Set the changing point of PWM2 output.	TRDIOA1 TRDIOC1
TRDGRB1	–	General register. Set the changing point of PWM3 output.	TRDIOB1 TRDIOD1
TRDGRC1	BFC1 = 0	(These points are not used in reset synchronous PWM mode.)	–
TRDGRD1	BFD1 = 0		
TRDGRC0	BFC0 = 1	Buffer register. Set the next PWM period. (Refer to **21.2.2 Buffer Operation.**)	(Output inverted every PWM period and TRDIOC0 pin)
TRDGRD0	BFD0 = 1	Buffer register. Set the changing point of the next PWM1 output. (Refer to **21.2.2 Buffer Operation**.)	TRDIOB0 TRDIOD0
TRDGRC1	BFC1 = 1	Buffer register. Set the changing point of the next PWM2 output. (Refer to **21.2.2 Buffer Operation**.)	TRDIOA1 TRDIOC1
TRDGRD1	BFD1 = 1	Buffer register. Set the changing point of the next PWM3 output. (Refer to **21.2.2 Buffer Operation**.)	TRDIOB1 TRDIOD1

BFC0, BFD0, BFC1, BFD1: Bits in TRDMR register

21.6.14 Timer RD Pin Select Register 0 (TRDPSR0)

Address 0184h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRDIOD0SEL1	TRDIOD0SEL0	TRDIOC0SEL1	TRDIOC0SEL0	TRDIOB0SEL1	TRDIOB0SEL0	TRDIOA0SEL1	TRDIOA0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRDIOA0SEL0	TRDIOA0/TRDCLK pin select bit	b1 b0 0 0: TRDIOA0/TRDCLK pin not used 0 1: P6_0 assigned 1 0: P10_0 assigned 1 1: Do not set.	R/W
b1	TRDIOA0SEL1			R/W
b2	TRDIOB0SEL0	TRDIOB0 pin select bit	b3 b2 0 0: TRDIOB0 pin not used 0 1: P6_1 assigned 1 0: P10_1 assigned 1 1: Do not set.	R/W
b3	TRDIOB0SEL1			R/W
b4	TRDIOC0SEL0	TRDIOC0 pin select bit	b5 b4 0 0: TRDIOC0 pin not used 0 1: P6_2 assigned 1 0: P10_2 assigned 1 1: Do not set.	R/W
b5	TRDIOC0SEL1			R/W
b6	TRDIOD0SEL0	TRDIOD0 pin select bit	b7 b6 0 0: TRDIOC0 pin not used 0 1: P6_3 assigned 1 0: P10_3 assigned 1 1: Do not set.	R/W
b7	TRDIOD0SEL1			R/W

The TRDPSR0 register selects which pin is assigned as the timer RD input/output. To use the I/O pins for timer RD, set this register.

Set the TRDPSR0 register before setting the timer RD associated registers. Also, do not change the setting value of this register during timer RD operation.

21.6.15 Timer RD Pin Select Register 1 (TRDPSR1)

Address 0185h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRDIOD1SEL1	TRDIOD1SEL0	TRDIOC1SEL1	TRDIOC1SEL0	TRDIOB1SEL1	TRDIOB1SEL0	TRDIOA1SEL1	TRDIOA1SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRDIOA1SEL0	TRDIOA1 pin select bit	b1 b0 0 0: TRDIOA1 pin not used 0 1: P6_4 assigned 1 0: P10_4 assigned 1 1: Do not set.	R/W
b1	TRDIOA1SEL1			R/W
b2	TRDIOB1SEL0	TRDIOB1 pin select bit	b3 b2 0 0: TRDIOB1 pin not used 0 1: P6_5 assigned 1 0: P10_5 assigned 1 1: Do not set.	R/W
b3	TRDIOB1SEL1			R/W
b4	TRDIOC1SEL0	TRDIOC1 pin select bit	b5 b4 0 0: TRDIOC1 pin not used 0 1: P6_6 assigned 1 0: P10_6 assigned 1 1: Do not set.	R/W
b5	TRDIOC1SEL1			R/W
b6	TRDIOD1SEL0	TRDIOD1 pin select bit	b7 b6 0 0: TRDIOC1 pin not used 0 1: P6_7 assigned 1 0: P10_7 assigned 1 1: Do not set.	R/W
b7	TRDIOD1SEL1			R/W

The TRDPSR1 register selects which pin is assigned as the timer RD input/output. To use the I/O pins for timer RD, set this register.

Set the TRDPSR1 register before setting the timer RD associated registers. Also, do not change the setting value of this register during timer RD operation.

21.6.16 Operating Example

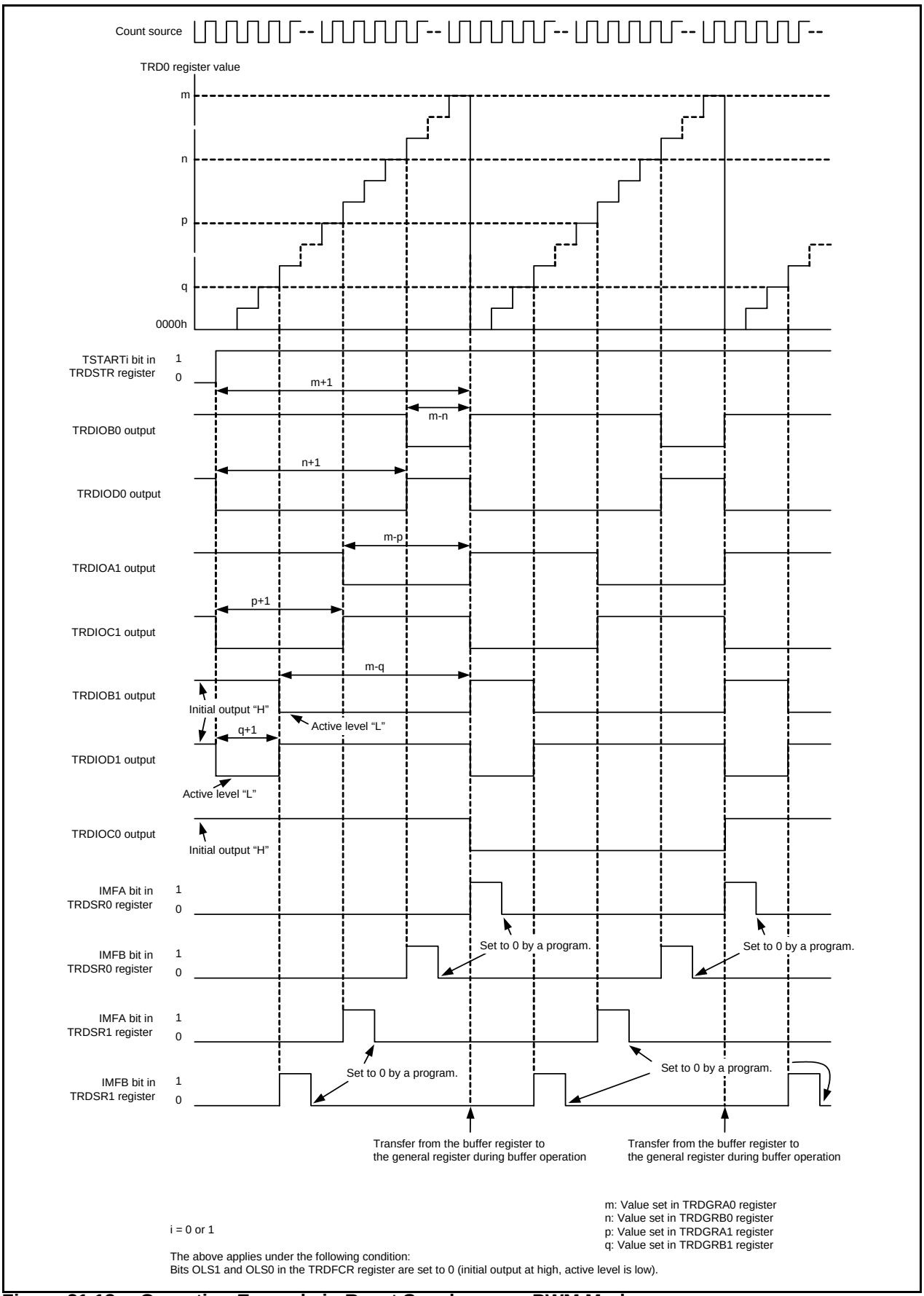


Figure 21.18 Operating Example in Reset Synchronous PWM Mode

21.6.17 A/D Trigger Generation

A compare match signal with registers TRDi (i = 0 or 1) and TRDGRji (j = A, B, C, or D) can be used as the conversion start trigger of the A/D converter.
The TRDADCR register is used to select which compare match is used.

21.7 Complementary PWM Mode

In this mode, three normal-phases and three counter-phases of the PWM waveform are output with the same period (three-phase, triangular wave modulation, and with dead time).
Figure 21.19 shows a Block Diagram of Complementary PWM Mode, and Table 21.13 lists the Complementary PWM Mode Specifications. Figure 21.20 shows the Output Model in Complementary PWM Mode, and Figure 21.21 shows an Operating Example in Complementary PWM Mode.

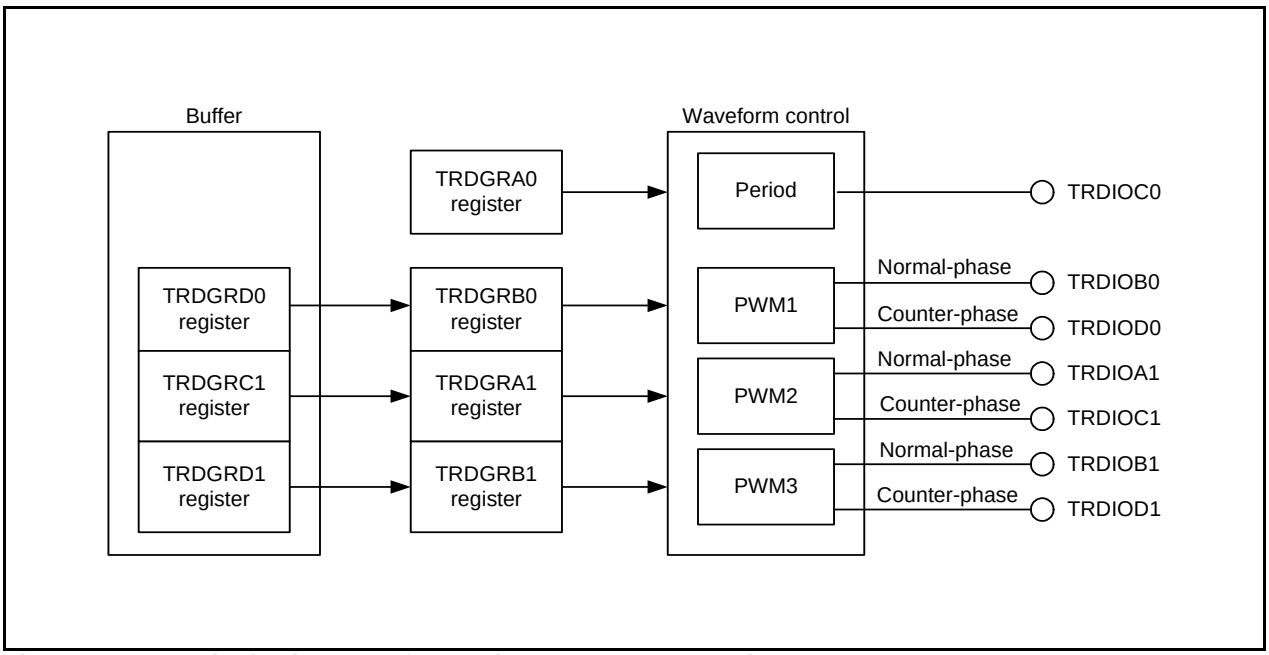
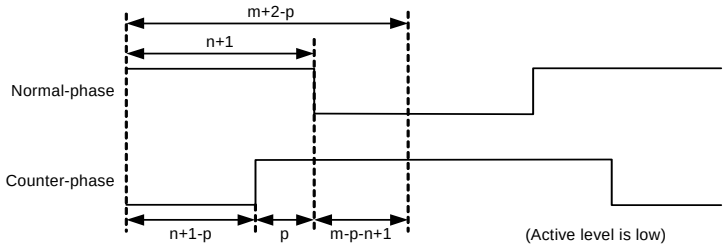


Figure 21.19 Block Diagram of Complementary PWM Mode

Table 21.13 Complementary PWM Mode Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, fC2, fOCO40M External signal input to the TRDCLK pin (active edge selectable by a program) Set bits TCK2 to TCK0 in the TRDCR1 register to the same value (same count source) as bits TCK2 to TCK0 in the TRDCR0 register.
Count operations	Increment or decrement Registers TRD0 and TRD1 are decremented by the compare match with registers TRD0 and TRDGRA0 during increment operation. The TRD1 register value is changed from 0000h to FFFFh during decrement operation, and registers TRD0 and TRD1 are incremented.
PWM operations	PWM period: 1/fk × (m+2-p) × 2 (1) Dead time: p Active level width of normal-phase: 1/fk × (m-n-p+1) × 2 Active level width of counter-phase: 1/fk × (n+1-p) × 2 fk: Frequency of count source m: Value set in TRDGRA0 register n: Value set in TRDGRB0 register (PWM1 output) Value set in TRDGRA1 register (PWM2 output) Value set in TRDGRB1 register (PWM3 output) p: Value set in TRD0 register 
Count start condition	1 (count starts) is written to bits TSTART0 and TSTART1 in the TRDSTR register.
Count stop conditions	0 (count stops) is written to bits TSTART0 and TSTART1 in the TRDSTR register when the CSEL0 bit in the TRDSTR register is set to 1. (The PWM output pin holds the output level before the count stops.)
Interrupt request generation timing	• Compare match (The contents of the TRDi register and the TRDGRji register match.) • TRD1 register underflow
TRDIOA0 pin function	Programmable I/O port or TRDCLK (external clock) input
TRDIOB0 pin function	PWM1 output normal-phase output
TRDIOD0 pin function	PWM1 output counter-phase output
TRDIOA1 pin function	PWM2 output normal-phase output
TRDIOC1 pin function	PWM2 output counter-phase output
TRDIOB1 pin function	PWM3 output normal-phase output
TRDIOD1 pin function	PWM3 output counter-phase output
TRDIOC0 pin function	Output inverted every 1/2 period of PWM
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRDi register.
Write to timer	The value can be written to the TRDi register.
Selectable functions	• Pulse output forced cutoff signal input (Refer to **21.2.4 Pulse Output Forced Cutoff.**) • The normal-phase and counter-phase active level and initial output level can selected individually. • Selectable transfer timing from the buffer register • A/D trigger generation

i = 0 or 1, j = either A, B, C, or D

Note:

1. After a count starts, the PWM period is fixed.

21.7.1 Module Standby Control Register (MSTCR)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	MSTTRG	MSTTRC	MSTTRD	MSTIIC	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	MSTIIC	SSU, I2C bus standby bit	0: Active 1: Standby (1)	R/W
b4	MSTTRD	Timer RD standby bit	0: Active 1: Standby (2)	R/W
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (3)	R/W
b6	MSTTRG	Timer RG standby bit	0: Active 1: Standby (4)	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. When the MSTIIC bit is set to 1 (standby), any access to the SSU or the I2C bus associated registers (addresses 0193h to 019Dh) is disabled.
2. When the MSTTRD bit is set to 1 (standby), any access to the timer RD associated registers (addresses 0135h to 015Fh) is disabled.
3. When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0133h) is disabled.
4. When the MSTTRG bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0170h to 017Fh) is disabled.

21.7.2 Timer RD Control Expansion Register (TRDECR)

Address 0135h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ITCLK1	—	—	—	ITCLK0	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	ITCLK0	Timer RD0 fC2 select bit	0: TRDCLK input selected 1: fC2 selected	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	ITCLK1	Timer RD1 fC2 select bit	0: TRDCLK input selected 1: fC2 selected	R/W

21.7.3 Timer RD Trigger Control Register (TRDADCR)

Address 0136h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADTRGD1E	ADTRGC1E	ADTRGB1E	ADTRGA1E	ADTRGD0E	ADTRGC0E	ADTRGB0E	ADTRGA0E
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADTRGA0E	A/D trigger A0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRA0	R/W
b1	ADTRGB0E	A/D trigger B0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRB0	R/W
b2	ADTRGC0E	A/D trigger C0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRC0	R/W
b3	ADTRGD0E	A/D trigger D0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRD0	R/W
b4	ADTRGA1E	A/D trigger A1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRA1	R/W
b5	ADTRGB1E	A/D trigger B1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRB1	R/W
b6	ADTRGC1E	A/D trigger C1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRC1	R/W
b7	ADTRGD1E	A/D trigger D1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRD1	R/W

21.7.4 Timer RD Start Register (TRDSTR) in Complementary PWM Mode

Address 0137h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	CSEL1	CSEL0	TSTART1	TSTART0
After Reset	1	1	1	1	1	1	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART0	TRD0 count start flag (3)	0: Count stops (1) 1: Count starts	R/W
b1	TSTART1	TRD1 count start flag (4)	0: Count stops (2) 1: Count starts	R/W
b2	CSEL0	TRD0 count operation select bit	0: Count stops at compare match with the TRDGRA0 register 1: Count continues after compare match with the TRDGRA0 register	R/W
b3	CSEL1	TRD1 count operation select bit	0: Count stops at compare match with the TRDGRA1 register 1: Count continues after compare match with the TRDGRA1 register	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	—			

Notes:
1. When the CSEL0 bit is set to 1, write 0 to the TSTART0 bit.
2. When the CSEL1 bit is set to 1, write 0 to the TSTART1 bit.
3. When the CSEL0 bit is set to 0 and the compare match signal (TRDIOA0) is generated, this bit is set to 0 (count stops).
4. When the CSEL1 bit is set to 0 and the compare match signal (TRDIOA1) is generated, this bit is set to 0 (count stops).

Set the TRDSTR register using the MOV instruction (do not use the bit handling instruction). Refer to **21.10.1 TRDSTR Register** for Notes on Timer RD.

21.7.5 Timer RD Mode Register (TRDMR) in Complementary PWM Mode

Address 0138h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BFD1	BFC1	BFD0	BFC0	—	—	—	SYNC
After Reset	0	0	0	0	1	1	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	SYNC	Timer RD synchronous bit	Set to 0 (registers TRD0 and TRD1 operate independently) in complementary PWM mode.	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b2	—			
b3	—			
b4	BFC0	TRDGRC0 register function select bit	Set to 0 (general register) in complementary PWM mode.	R/W
b5	BFD0	TRDGRD0 register function select bit	0: General register 1: Buffer register of TRDGRB0 register	R/W
b6	BFC1	TRDGRC1 register function select bit	0: General register 1: Buffer register of TRDGRA1 register	R/W
b7	BFD1	TRDGRD1 register function select bit	0: General register 1: Buffer register of TRDGRB1 register	R/W

21.7.6 Timer RD Function Control Register (TRDFCR) in Complementary PWM Mode

Address 013Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PWM3	STCLK	ADEG	ADTRG	OLS1	OLS0	CMD1	CMD0
After Reset	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CMD0	Combination mode select bit (1, 2)	b1 b0 1 0: Complementary PWM mode (transfer from the buffer register to the general register at TRD1 register underflow) 1 1: Complementary PWM mode (transfer from the buffer register to the general register at compare match with registers TRD0 and TRDGRA0.) Other than above: Do not set.	R/W
b1	CMD1			R/W
b2	OLS0	Normal-phase output level select bit (in reset synchronous PWM mode or complementary PWM mode)	0: Initial output at high, active level is low 1: Initial output at low, active level is high	R/W
b3	OLS1	Counter-phase output level select bit (in reset synchronous PWM mode or complementary PWM mode)	0: Initial output at high, active level is low 1: Initial output at low, active level is high	R/W
b4	ADTRG	A/D trigger enable bit (in complementary PWM mode)	0: A/D trigger disabled 1: A/D trigger enabled (3)	R/W
b5	ADEG	A/D trigger edge select bit (in complementary PWM mode)	0: A/D trigger is generated at compare match between registers TRD0 and TRDGRA0 1: A/D trigger is generated at underflow in the TRD1 register	R/W
b6	STCLK	External clock input select bit	0: External clock input disabled 1: External clock input enabled	R/W
b7	PWM3	PWM3 mode select bit (4)	Disabled in complementary PWM mode.	R/W

Notes:
1. When setting bits CMD1 to CMD0 to 10b or 11b, the MCU enters complementary PWM mode in spite of the setting of the TRDPMR register.
2. Set bits CMD1 to CMD0 when both the TSTART0 and TSTART1 bits in the TRDSTR register are set to 0 (count stops).
3. Set the ADCAP bit in the ADCON0 register to 1 (start by timer RD).
4. When bits CMD1 to CMD0 are set to 00b (timer mode, PWM mode, or PWM3 mode), the setting of the PWM3 bit is enabled.

21.7.7 Timer RD Output Master Enable Register 1 (TRDOER1) in Complementary PWM Mode

Address 013Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ED1	EC1	EB1	EA1	ED0	EC0	EB0	EA0
After Reset	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	EA0	TRDIOA0 output disable bit	Set to 1 (TRDIOA0 pin is used as a programmable I/O port) in complementary PWM mode.	R/W
b1	EB0	TRDIOB0 output disable bit	0: Output enabled 1: Output disabled (TRDIOB0 pin is used as a programmable I/O port)	R/W
b2	EC0	TRDIOC0 output disable bit	0: Output enabled 1: Output disabled (TRDIOC0 pin is used as a programmable I/O port)	R/W
b3	ED0	TRDIOD0 output disable bit	0: Output enabled 1: Output disabled (TRDIOD0 pin is used as a programmable I/O port)	R/W
b4	EA1	TRDIOA1 output disable bit	0: Output enabled 1: Output disabled (TRDIOA1 pin is used as a programmable I/O port)	R/W
b5	EB1	TRDIOB1 output disable bit	0: Output enabled 1: Output disabled (TRDIOB1 pin is used as a programmable I/O port)	R/W
b6	EC1	TRDIOC1 output disable bit	0: Output enabled 1: Output disabled (TRDIOC1 pin is used as a programmable I/O port)	R/W
b7	ED1	TRDIOD1 output disable bit	0: Output enabled 1: Output disabled (TRDIOD1 pin is used as a programmable I/O port)	R/W

21.7.8 Timer RD Output Master Enable Register 2 (TRDOER2) in Complementary PWM Mode

Address 013Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PTO	—	—	—	—	—	—	—
After Reset	0	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b1	—			—
b2	—			—
b3	—			—
b4	—			—
b5	—			—
b6	—			—
b7	PTO	$\overline{\text{INT0}}$ of pulse output forced cutoff signal input enabled bit (1)	0: Pulse output forced cutoff input disabled 1: Pulse output forced cutoff input enabled (All bits in the TRDOER1 register are set to 1 (output disabled) when a low-level signal is applied to the $\overline{\text{INT0}}$ pin.)	R/W

Note:
1. Refer to **21.2.4 Pulse Output Forced Cutoff**.

21.7.9 Timer RD Control Register i (TRDCRi) (i = 0 or 1) in Complementary PWM Mode

Address 0140h (TRDCR0), 0150h (TRDCR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TCK2	TCK1	TCK0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TCK0	Count source select bit (3)	b2 b1 b0 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRDCLK input (1) or fC2 (2) 1 1 0: fOCO40M 1 1 1: Do not set.	R/W
b1	TCK1			R/W
b2	TCK2			R/W
b3	CKEG0	External clock edge select bit (3, 4)	b4 b3 0 0: Count at the rising edge 0 1: Count at the falling edge 1 0: Count at both edges 1 1: Do not set.	R/W
b4	CKEG1			R/W
b5	CCLR0	TRDi counter clear select bit	Set to 000b (clear disabled (free-running operation)) in complementary PWM mode.	R/W
b6	CCLR1			R/W
b7	CCLR2			R/W

Notes:
1. Enabled when the ITCLKi bit in the TRDECR register is set to 0 (TRDCLK input) and the STCLK bit in the TRDFCR register is 1 (external clock input enabled).
2. Enabled when the ITCLKi bit in the TRDECR register is set to 1 (fC2).
3. Set bits TCK2 to TCK0 and bits CKEG1 to CKEG0 in registers TRDCR0 and TRDCR1 to the same values.
4. Enabled when bits TCK2 to TCK0 are set to 101b (TRDCLK input or fC2), the ITCLKi bit in the TRDECR is set to 0 (TRDCLK input), and the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).

21.7.10 Timer RD Status Register i (TRDSRi) (i = 0 or 1) in Complementary PWM Mode

Address 0143h (TRDSR0), 0153h (TRDSR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	UDF	OVF	IMFD	IMFC	IMFB	IMFA	
After Reset	1	1	1	0	0	0	0	0	TRDSR0 register
After Reset	1	1	0	0	0	0	0	0	TRDSR1 register

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input-capture/compare-match flag A	[Condition for setting this bit to 0] Write 0 after reading. (2) [Condition for setting this bit to 1] When the TRDi register value matches the TRDGRAi register value.	R/W
b1	IMFB	Input-capture/compare-match flag B	[Condition for setting this bit to 0] Write 0 after reading. (2) [Condition for setting this bit to 1] When the TRDi register value matches the TRDGRBi register value.	R/W
b2	IMFC	Input-capture/compare-match flag C	[Condition for setting this bit to 0] Write 0 after reading. (2) [Condition for setting this bit to 1] When the TRDi register value matches the TRDGRCi register value (3).	R/W
b3	IMFD	Input-capture/compare-match flag D	[Condition for setting this bit to 0] Write 0 after reading. (2) [Condition for setting this bit to 1] When the TRDi register value matches the TRDGRDi register value (3).	R/W
b4	OVF	Overflow flag	[Condition for setting this bit to 0] Write 0 after reading. (2) [Condition for setting this bit to 1] When the TRDi register overflows.	R/W
b5	UDF	Underflow flag (1)	[Condition for setting this bit to 0] Write 0 after reading. (2) [Condition for setting this bit to 1] When the TRD1 register underflows.	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b7	—			

Notes:
1. Nothing is assigned to b5 in the TRDSR0 register. If necessary, write 0 to b5. When read, the content is 1.
2. The results of writing to these bits are as follows:
   - The bit is set to 0 when it is first read as 1 and then 0 is written to it.
   - The bit remains unchanged even if it is first read as 0 and then 0 is written to it because its previous value is retained. (The bit's value remains 1 even if it is set to 1 from 0 after being read as 0 and having 0 written to it because its previous value is retained.)
   - The bit's value remains unchanged if 1 is written to it.
3. Including when the BFji bit in the TRDMR register is set to 1 (TRDGRji is used as a buffer register).

21.7.11 Timer RD Interrupt Enable Register i (TRDIERi) (i = 0 or 1) in Complementary PWM Mode

Address 0144h (TRDIER0), 0154h (TRDIER1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	OVIE	IMIED	IMIEC	IMIEB	IMIEA
After Reset	1	1	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input-capture/compare-match interrupt enable bit A	0: Interrupt (IMIA) by IMFA bit disabled 1: Interrupt (IMIA) by IMFA bit enabled	R/W
b1	IMIEB	Input-capture/compare-match interrupt enable bit B	0: Interrupt (IMIB) by IMFB bit disabled 1: Interrupt (IMIB) by IMFB bit enabled	R/W
b2	IMIEC	Input-capture/compare-match interrupt enable bit C	0: Interrupt (IMIC) by IMFC bit disabled 1: Interrupt (IMIC) by IMFC bit enabled	R/W
b3	IMIED	Input-capture/compare-match interrupt enable bit D	0: Interrupt (IMID) by IMFD bit disabled 1: Interrupt (IMID) by the IMFD bit enabled	R/W
b4	OVIE	Overflow/underflow interrupt enable bit	0: Interrupt (OVI) by OVF bit disabled 1: Interrupt (OVI) by OVF bit enabled	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b6	—			
b7	—			

21.7.12 Timer RD Counter 0 (TRD0) in Complementary PWM Mode

Address 0147h to 0146h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	Set the dead time. A count source is counted. Count operation is increment or decrement. When an overflow occurs, the OVF bit in the TRDSR0 register is set to 1.	0000h to FFFFh	R/W

Access the TRD0 register in 16-bit units. Do not access it in 8-bit units.

21.7.13 Timer RD Counter 1 (TRD1) in Complementary PWM Mode

Address 0157h to 0156h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	Set 0000h. A count source is counted. Count operation is increment or decrement. When an underflow occurs, the UDF bit in the TRDSR1 register is set to 1.	0000h to FFFFh	R/W

Access the TRD1 register in 16-bit units. Do not access it in 8-bit units.

21.7.14 Timer RD General Registers Ai, Bi, C1, and Di (TRDGRAi, TRDGRBi, TRDGRC1, TRDGRDi) (i = 0 or 1) in Complementary PWM Mode

Address 0149h to 0148h (TRDGRA0), 014Bh to 014Ah (TRDGRB0),
014Fh to 014Eh (TRDGRD0),
0159h to 0158h (TRDGRA1), 015Bh to 015Ah (TRDGRB1),
015Dh to 015Ch (TRDGRC1), 015Fh to 015Eh (TRDGRD1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b15 to b0	Refer to **Table 21.14 TRDGRji Register Functions in Complementary PWM Mode**	R/W

Access registers TRDGRAi to TRDGRDi in 16-bit units. Do not access them in 8-bit units.
The TRDGRC0 register is not used in complementary PWM mode.

The following registers are disabled in complementary PWM mode:
TRDPMR, TRDOCR, TRDDF0, TRDDF1, TRDIORA0, TRDIORC0, TRDPOCR0, TRDIORA1, TRDIORC1, and TRDPOCR1.

Table 21.14 TRDGRji Register Functions in Complementary PWM Mode

Register	Setting	Register Function	PWM Output Pin
TRDGRA0	–	General register. Set the PWM period at initialization. Setting range: TRD0 register setting value or above, FFFFh - TRD0 register setting value or below Do not write to this register when the TSTART0 and TSTART1 bits in the TRDSTR register are set to 1 (count starts).	(Output inverted every half period of TRDIOC0 pin)
TRDGRB0	–	General register. Set the changing point of PWM1 output at initialization. Setting range: TRD0 register setting value or above, TRDGRA0 register - TRD0 register setting value or below Do not write to this register when the TSTART0 and TSTART1 bits in the TRDSTR register are set to 1 (count starts).	TRDIOB0 TRDIOD0
TRDGRA1	–	General register. Set the changing point of PWM2 output at initialization. Setting range: TRD0 register setting value or above, TRDGRA0 register - TRD0 register setting value or below Do not write to this register when the TSTART0 and TSTART1 bits in the TRDSTR register are set to 1 (count starts).	TRDIOA1 TRDIOC1
TRDGRB1	–	General register. Set the changing point of PWM3 output at initialization. Setting range: TRD0 register setting value or above, TRDGRA0 register - TRD0 register setting value or below Do not write to this register when the TSTART0 and TSTART1 bits in the TRDSTR register are set to 1 (count starts).	TRDIOB1 TRDIOD1
TRDGRC0	–	This register is not used in complementary PWM mode.	–
TRDGRD0	BFD0 = 1	Buffer register. Set the changing point of next PWM1 output. (Refer to **21.2.2 Buffer Operation.**) Setting range: TRD0 register setting value or above, TRDGRA0 register - TRD0 register setting value or below Set this register to the same value as the TRDGRB0 register for initialization.	TRDIOB0 TRDIOD0
TRDGRC1	BFC1 = 1	Buffer register. Set the changing point of next PWM2 output. (Refer to **21.2.2 Buffer Operation.**) Setting range: TRD0 register setting value or above, TRDGRA0 register - TRD0 register setting value or below Set this register to the same value as the TRDGRA1 register for initialization.	TRDIOA1 TRDIOC1
TRDGRD1	BFD1 = 1	Buffer register. Set the changing point of next PWM3 output. (Refer to **21.2.2 Buffer Operation.**) Setting range: TRD0 register setting value or above, TRDGRA0 register - TRD0 register setting value or below Set this register to the same value as the TRDGRB1 register for initialization.	TRDIOB1 TRDIOD1

BFC0, BFD0, BFC1, BFD1: Bits in TRDMR register

Since values cannot be written to the TRDGRB0, TRDGRA1, or TRDGRB1 register directly after count operation starts (prohibited item), use the TRDGRD0, TRDGRC1, or TRDGRD1 register as a buffer register. However, to write data to the TRDGRD0, TRDGRC1, or TRDGRD1 register, set bits BFD0, BFC1, and BFD1 to 0 (general register). After this, bits BFD0, BFC1, and BFD1 may be set to 1 (buffer register).

21.7.15 Timer RD Pin Select Register 0 (TRDPSR0)

Address 0184h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRDIOD0SEL1	TRDIOD0SEL0	TRDIOC0SEL1	TRDIOC0SEL0	TRDIOB0SEL1	TRDIOB0SEL0	TRDIOA0SEL1	TRDIOA0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRDIOA0SEL0	TRDIOA0/TRDCLK pin select bit	b1 b0 0 0: TRDIOA0/TRDCLK pin not used 0 1: P6_0 assigned 1 0: P10_0 assigned 1 1: Do not set.	R/W
b1	TRDIOA0SEL1			R/W
b2	TRDIOB0SEL0	TRDIOB0 pin select bit	b3 b2 0 0: TRDIOB0 pin not used 0 1: P6_1 assigned 1 0: P10_1 assigned 1 1: Do not set.	R/W
b3	TRDIOB0SEL1			R/W
b4	TRDIOC0SEL0	TRDIOC0 pin select bit	b5 b4 0 0: TRDIOC0 pin not used 0 1: P6_2 assigned 1 0: P10_2 assigned 1 1: Do not set.	R/W
b5	TRDIOC0SEL1			R/W
b6	TRDIOD0SEL0	TRDIOD0 pin select bit	b7 b6 0 0: TRDIOC0 pin not used 0 1: P6_3 assigned 1 0: P10_3 assigned 1 1: Do not set.	R/W
b7	TRDIOD0SEL1			R/W

The TRDPSR0 register selects which pin is assigned as the timer RD input/output. To use the I/O pins for timer RD, set this register.

Set the TRDPSR0 register before setting the timer RD associated registers. Also, do not change the setting value of this register during timer RD operation.

21.7.16 Timer RD Pin Select Register 1 (TRDPSR1)

Address 0185h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRDIOD1SEL1	TRDIOD1SEL0	TRDIOC1SEL1	TRDIOC1SEL0	TRDIOB1SEL1	TRDIOB1SEL0	TRDIOA1SEL1	TRDIOA1SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRDIOA1SEL0	TRDIOA1 pin select bit	b1 b0 0 0: TRDIOA1 pin not used 0 1: P6_4 assigned 1 0: P10_4 assigned 1 1: Do not set.	R/W
b1	TRDIOA1SEL1			R/W
b2	TRDIOB1SEL0	TRDIOB1 pin select bit	b3 b2 0 0: TRDIOB1 pin not used 0 1: P6_5 assigned 1 0: P10_5 assigned 1 1: Do not set.	R/W
b3	TRDIOB1SEL1			R/W
b4	TRDIOC1SEL0	TRDIOC1 pin select bit	b5 b4 0 0: TRDIOC1 pin not used 0 1: P6_6 assigned 1 0: P10_6 assigned 1 1: Do not set.	R/W
b5	TRDIOC1SEL1			R/W
b6	TRDIOD1SEL0	TRDIOD1 pin select bit	b7 b6 0 0: TRDIOC1 pin not used 0 1: P6_7 assigned 1 0: P10_7 assigned 1 1: Do not set.	R/W
b7	TRDIOD1SEL1			R/W

The TRDPSR1 register selects which pin is assigned as the timer RD input/output. To use the I/O pins for timer RD, set this register.

Set the TRDPSR1 register before setting the timer RD associated registers. Also, do not change the setting value of this register during timer RD operation.

21.7.17 Operating Example

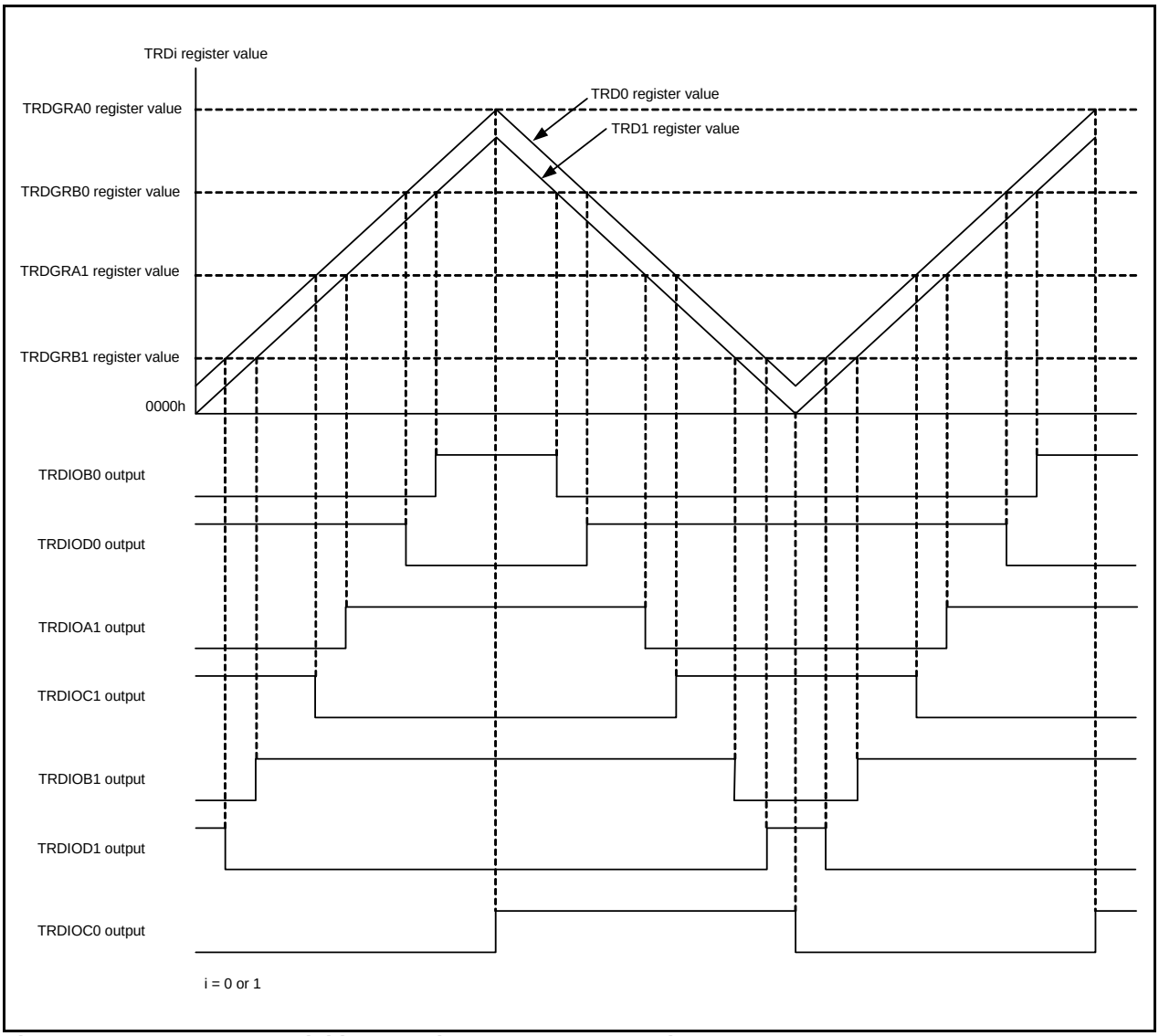
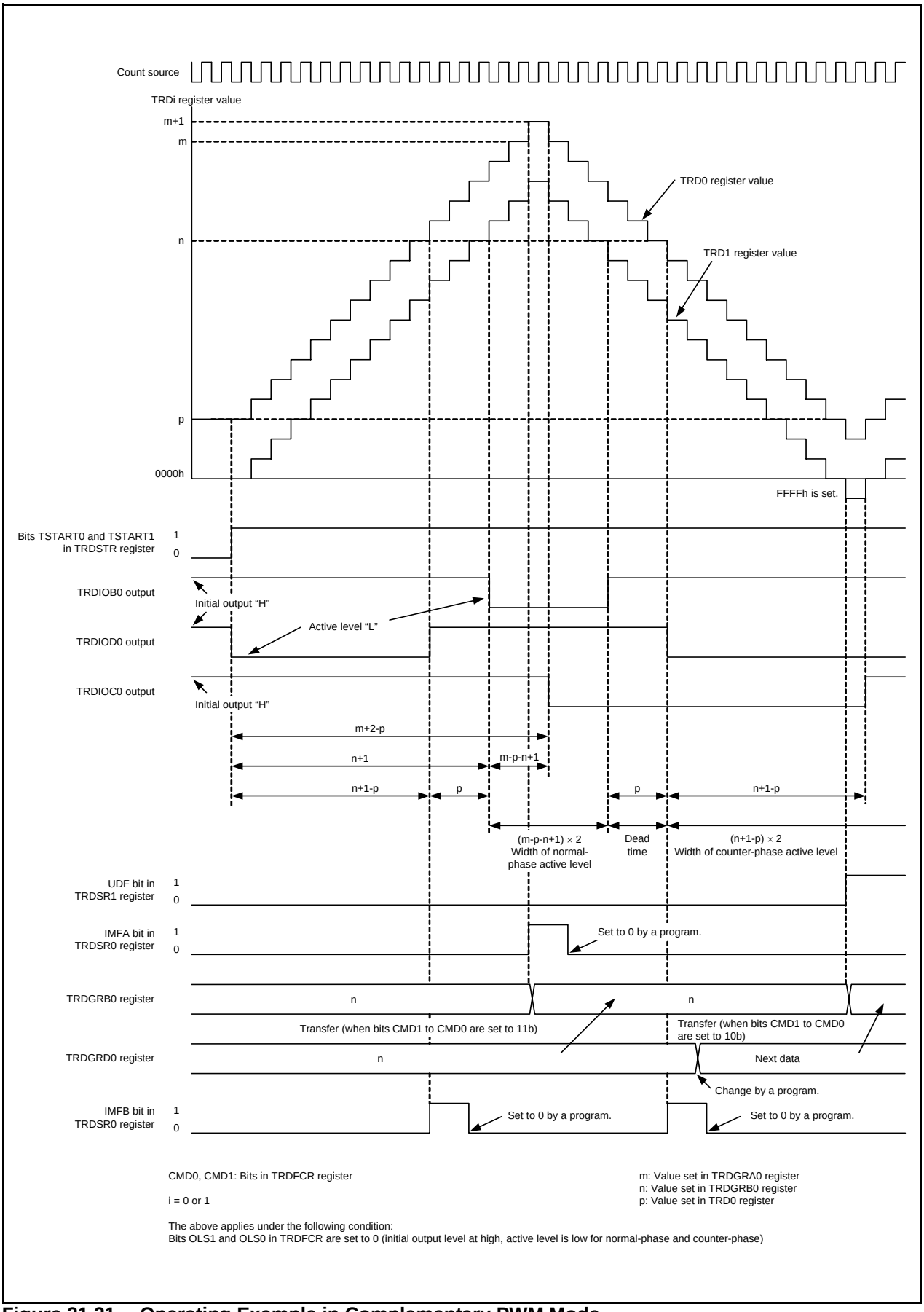


Figure 21.20 Output Model in Complementary PWM Mode



CMD0, CMD1: Bits in TRDFCR register

i = 0 or 1

m: Value set in TRDGRA0 register
n: Value set in TRDGRB0 register
p: Value set in TRD0 register

The above applies under the following condition:
Bits OLS1 and OLS0 in TRDFCR are set to 0 (initial output level at high, active level is low for normal-phase and counter-phase)

Figure 21.21 Operating Example in Complementary PWM Mode

21.7.18 Transfer Timing from Buffer Register

- Transfer from the TRDGRD0, TRDGRC1, or TRDGRD1 register to the TRDGRB0, TRDGRA1, or TRDGRB1 register.
  When bits CMD1 to CMD0 in the TRDFCR register are set to 10b, the content is transferred when the TRD1 register underflows.
  When bits CMD1 to CMD0 are set to 11b, the content is transferred at compare match between registers TRD0 and TRDGRA0.

21.7.19 A/D Trigger Generation

A compare match between registers TRD0 and TRDGRA0 and TRD1 underflow can be used as the conversion start trigger of the A/D converter. The trigger is selected by bits ADEG and ADTRG in the TRDFCR register. In addition, set bits ADCAP1 to ADCAP0 in the ADMOD register to 01b (start by timer RD).

21.8 PWM3 Mode

In this mode, 2 PWM waveforms are output with the same period.
Figure 21.22 shows a Block Diagram of PWM3 Mode, and Table 21.15 lists the PWM3 Mode Specifications.
Figure 21.23 shows an Operating Example in PWM3 Mode.

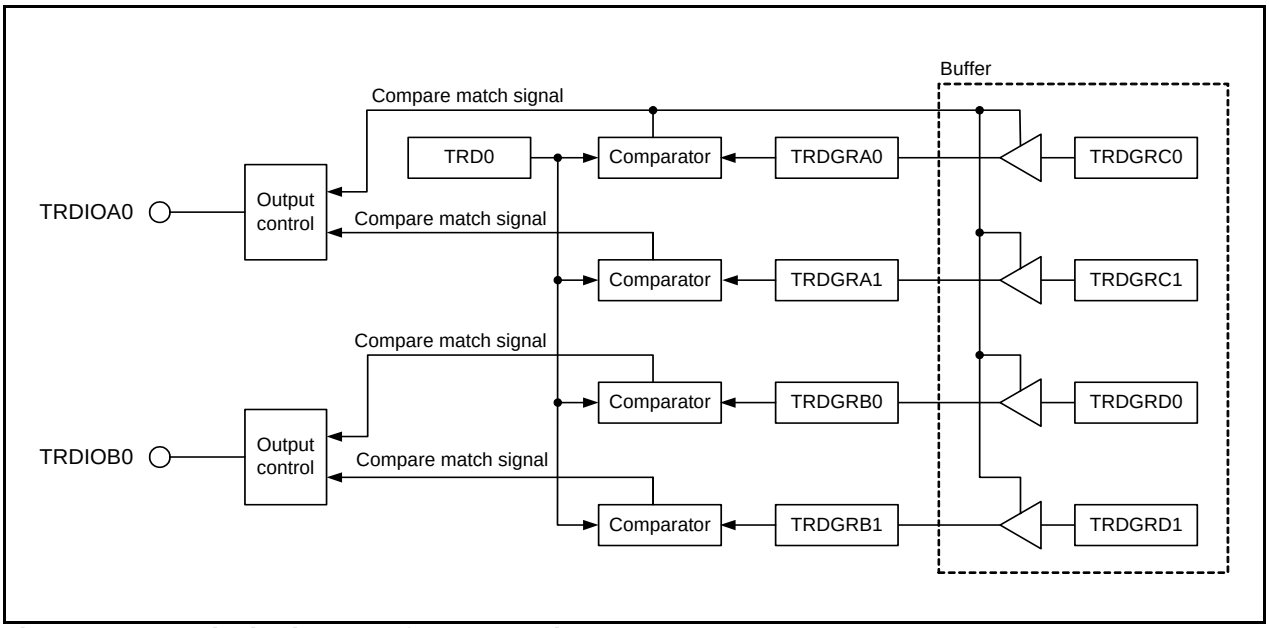
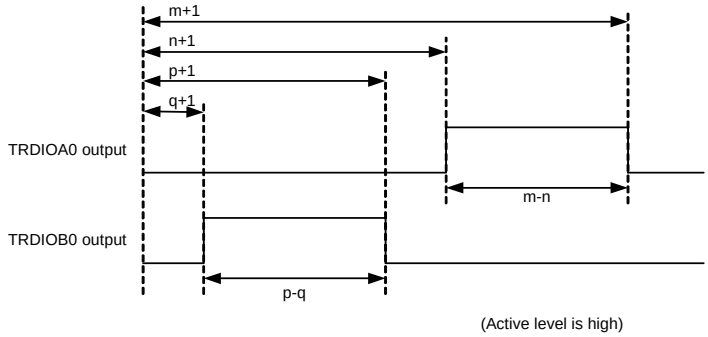


Figure 21.22 Block Diagram of PWM3 Mode

Table 21.15 PWM3 Mode Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, fC2, fOCO40M
Count operations	The TRD0 register is incremented (TRD1 register is not used).
PWM waveform	PWM period: 1/fk × (m+1) Active level width of TRDIOA0 output: 1/fk × (m-n) Active level width of TRDIOB0 output: 1/fk × (p-q) fk: Frequency of count source m: Value set in TRDGRA0 register n: Value set in TRDGRA1 register p: Value set in TRDGRB0 register q: Value set in TRDGRB1 register  (Active level is high)
Count start condition	1 (count starts) is written to the TSTART0 bit in the TRDSTR register.
Count stop conditions	• 0 (count stops) is written to the TSTART0 bit in the TRDSTR register when the CSEL0 bit in the TRDSTR register is set to 1. The PWM output pin holds output level before the count stops • When the CSEL0 bit in the TRDSTR register is set to 0, the count stops at compare match with the TRDGRA0 register. The PWM output pin holds the level after the output changes by the compare match.
Interrupt request generation timing	• Compare match (The contents of the TRDi register and the TRDGRji register match.) • TRD0 register overflow
TRDIOA0, TRDIOB0 pins function	PWM output
TRDIOC0, TRDIOD0, TRDIOA1 to TRDIOD1 pins function	Programmable I/O port
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRD0 register.
Write to timer	The value can be written to the TRD0 register.
Selectable functions	• Pulse output forced cutoff signal input (Refer to **21.2.4 Pulse Output Forced Cutoff.**) • Buffer operation (Refer to **21.2.2 Buffer Operation.**) • Active level selectable for each individual pin • A/D trigger generation

i = 0 or 1, j = either A, B, C, or D

21.8.1 Module Standby Control Register (MSTCR)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	MSTTRG	MSTTRC	MSTTRD	MSTIIC	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	MSTIIC	SSU, I2C bus standby bit	0: Active 1: Standby (1)	R/W
b4	MSTTRD	Timer RD standby bit	0: Active 1: Standby (2)	R/W
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (3)	R/W
b6	MSTTRG	Timer RG standby bit	0: Active 1: Standby (4)	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. When the MSTIIC bit is set to 1 (standby), any access to the SSU or the I2C bus associated registers (addresses 0193h to 019Dh) is disabled.
2. When the MSTTRD bit is set to 1 (standby), any access to the timer RD associated registers (addresses 0135h to 015Fh) is disabled.
3. When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0133h) is disabled.
4. When the MSTTRG bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0170h to 017Fh) is disabled.

21.8.2 Timer RD Control Expansion Register (TRDECR)

Address 0135h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ITCLK1	—	—	—	ITCLK0	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	ITCLK0	Timer RD0 fC2 select bit	0: TRDCLK input selected 1: fC2 selected	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	ITCLK1	Timer RD1 fC2 select bit	0: TRDCLK input selected 1: fC2 selected	R/W

21.8.3 Timer RD Trigger Control Register (TRDADCR)

Address 0136h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADTRGD1E	ADTRGC1E	ADTRGB1E	ADTRGA1E	ADTRGD0E	ADTRGC0E	ADTRGB0E	ADTRGA0E
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADTRGA0E	A/D trigger A0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRA0	R/W
b1	ADTRGB0E	A/D trigger B0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRB0	R/W
b2	ADTRGC0E	A/D trigger C0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRC0	R/W
b3	ADTRGD0E	A/D trigger D0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRD0	R/W
b4	ADTRGA1E	A/D trigger A1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRA1	R/W
b5	ADTRGB1E	A/D trigger B1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRB1	R/W
b6	ADTRGC1E	A/D trigger C1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRC1	R/W
b7	ADTRGD1E	A/D trigger D1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRD1	R/W

21.8.4 Timer RD Start Register (TRDSTR) in PWM3 Mode

Address 0137h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	CSEL1	CSEL0	TSTART1	TSTART0
After Reset	1	1	1	1	1	1	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART0	TRD0 count start flag (3)	0: Count stops (1) 1: Count starts	R/W
b1	TSTART1	TRD1 count start flag (4)	0: Count stops (2) 1: Count starts	R/W
b2	CSEL0	TRD0 count operation select bit	0: Count stops at compare match with the TRDGRA0 register 1: Count continues after compare match with the TRDGRA0 register	R/W
b3	CSEL1	TRD1 count operation select bit [not used in PWM3 mode]	0: Count stops at compare match with the TRDGRA1 register 1: Count continues after compare match with the TRDGRA1 register	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	—			

Notes:
1. When the CSEL0 bit is set to 1, write 0 to the TSTART0 bit.
2. When the CSEL1 bit is set to 1, write 0 to the TSTART1 bit.
3. When the CSEL0 bit is set to 0 and the compare match signal (TRDIOA0) is generated, this bit is set to 0 (count stops).
4. When the CSEL1 bit is set to 0 and the compare match signal (TRDIOA1) is generated, this bit is set to 0 (count stops).

Set the TRDSTR register using the MOV instruction (do not use the bit handling instruction). Refer to **21.10.1 TRDSTR Register** for Notes on Timer RD.

21.8.5 Timer RD Mode Register (TRDMR) in PWM3 Mode

Address 0138h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BFD1	BFC1	BFD0	BFC0	—	—	—	SYNC
After Reset	0	0	0	0	1	1	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	SYNC	Timer RD synchronous bit	Set to 0 (TRD0 and TRD1 operate independently) in PWM3 mode.	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b2	—			
b3	—			
b4	BFC0	TRDGRC0 register function select bit	0: General register 1: Buffer register of TRDGRA0 register	R/W
b5	BFD0	TRDGRD0 register function select bit	0: General register 1: Buffer register of TRDGRB0 register	R/W
b6	BFC1	TRDGRC1 register function select bit	0: General register 1: Buffer register of TRDGRA1 register	R/W
b7	BFD1	TRDGRD1 register function select bit	0: General register 1: Buffer register of TRDGRB1 register	R/W

21.8.6 Timer RD Function Control Register (TRDFCR) in PWM3 Mode

Address 013Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PWM3	STCLK	ADEG	ADTRG	OLS1	OLS0	CMD1	CMD0
After Reset	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CMD0	Combination mode select bit (1)	Set to 00b (timer mode, PWM mode, or PWM3 mode) in PWM3 mode.	R/W
b1	CMD1			R/W
b2	OLS0	Normal-phase output level select bit (enabled in reset synchronous PWM mode or complementary PWM mode)	Disabled in PWM3 mode.	R/W
b3	OLS1	Counter-phase output level select bit (enabled in reset synchronous PWM mode or complementary PWM mode)		R/W
b4	ADTRG	A/D trigger enable bit (enabled in complementary PWM mode)		R/W
b5	ADEG	A/D trigger edge select bit (enabled in complementary PWM mode)		R/W
b6	STCLK	External clock input select bit	Set to 0 (external clock input disabled) in PWM3 mode.	R/W
b7	PWM3	PWM3 mode select bit (2)	Set to 0 (PWM3 mode) in PWM3 mode.	R/W

Notes:
1. Set bits CMD1 to CMD0 when both the TSTART0 and TSTART1 bits in the TRDSTR register are set to 0 (count stops).
2. When bits CMD1 to CMD0 are set to 00b (timer mode, PWM mode, or PWM3 mode), the setting of the PWM3 bit is enabled.

21.8.7 Timer RD Output Master Enable Register 1 (TRDOER1) in PWM3 Mode

Address 013Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ED1	EC1	EB1	EA1	ED0	EC0	EB0	EA0
After Reset	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	EA0	TRDIOA0 output disable bit	0: Output enabled 1: Output disabled (TRDIOA0 pin is used as a programmable I/O port)	R/W
b1	EB0	TRDIOB0 output disable bit	0: Output enabled 1: Output disabled (TRDIOB0 pin is used as a programmable I/O port)	R/W
b2	EC0	TRDIOC0 output disable bit	Set to 1 (programmable I/O port) in PWM3 mode.	R/W
b3	ED0	TRDIOD0 output disable bit		R/W
b4	EA1	TRDIOA1 output disable bit		R/W
b5	EB1	TRDIOB1 output disable bit		R/W
b6	EC1	TRDIOC1 output disable bit		R/W
b7	ED1	TRDIOD1 output disable bit		R/W

21.8.8 Timer RD Output Master Enable Register 2 (TRDOER2) in PWM3 Mode

Address 013Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PTO	—	—	—	—	—	—	—
After Reset	0	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b1	—			—
b2	—			—
b3	—			—
b4	—			—
b5	—			—
b6	—			—
b7	PTO	$\overline{\text{INT0}}$ of pulse output forced cutoff signal input enabled bit (1)	0: Pulse output forced cutoff input disabled 1: Pulse output forced cutoff input enabled (All bits in the TRDOER1 register are set to 1 (output disabled) when a low-level signal is applied to the $\overline{\text{INT0}}$ pin.)	R/W

Note:
1. Refer to **21.2.4 Pulse Output Forced Cutoff**.

21.8.9 Timer RD Output Control Register (TRDOCR) in PWM3 Mode

Address 013Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TOD1	TOC1	TOB1	TOA1	TOD0	TOC0	TOB0	TOA0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA0	TRDIOA0 output level select bit (1)	0: Active level is high, initial output at low, high-level output at compare match with the TRDGRA1 register, low-level output at compare match with the TRDGRA0 register 1: Active level is low, initial output at high, low-level output at compare match with the TRDGRA1 register, high-level output at compare match with the TRDGRA0 register	R/W
b1	TOB0	TRDIOB0 output level select bit (1)	0: Active level is high, initial output at low, high-level output at compare match with the TRDGRB1register, low-level output at compare match with the TRDGRB0 register 1: Active level is low, initial output at high, low-level output at compare match with the TRDGRB1 register, high-level output at compare match with the TRDGRB0 register	R/W
b2	TOC0	TRDIOC0 initial output level select bit	Disabled in PWM3 mode.	R/W
b3	TOD0	TRDIOD0 initial output level select bit		R/W
b4	TOA1	TRDIOA1 initial output level select bit		R/W
b5	TOB1	TRDIOB1 initial output level select bit		R/W
b6	TOC1	TRDIOC1 initial output level select bit		R/W
b7	TOD1	TRDIOD1 initial output level select bit		R/W

Note:

1. If the pin function is set for waveform output (refer to **7.5 Port Settings**), the initial output level is output when the TRDOCR register is set.

   Write to the TRDOCR register when both the TSTART0 and TSTART1 bits in the TRDSTR register are set to 0 (count stops).

21.8.10 Timer RD Control Register 0 (TRDCR0) in PWM3 Mode

Address 0140h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TCK2	TCK1	TCK0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TCK0	Count source select bit	b2 b1 b0 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: Do not set. 1 1 0: fOCO40M 1 1 1: Do not set.	R/W
b1	TCK1			R/W
b2	TCK2			R/W
b3	CKEG0	External clock edge select bit	Disabled in PWM3 mode.	R/W
b4	CKEG1			R/W
b5	CCLR0	TRD0 counter clear select bit	Set to 001b (TRD0 register cleared at compare match with TRDGRA0 register) in PWM3 mode.	R/W
b6	CCLR1			R/W
b7	CCLR2			R/W

The TRDCR1 register is not used in PWM3 mode for the TRDCR0 register.

21.8.11 Timer RD Status Register i (TRDSRi) (i = 0 or 1) in PWM3 Mode

Address 0143h (TRDSR0), 0153h (TRDSR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	UDF	OVF	IMFD	IMFC	IMFB	IMFA	
After Reset	1	1	1	0	0	0	0	0	TRDSR0 register
After Reset	1	1	0	0	0	0	0	0	TRDSR1 register

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input-capture/compare-match flag A	[Condition for setting this bit to 0] Write 0 after reading. (1) [Condition for setting this bit to 1] When the TRDi register value matches the TRDGRAi register value.	R/W
b1	IMFB	Input-capture/compare-match flag B	[Condition for setting this bit to 0] Write 0 after reading. (1) [Condition for setting this bit to 1] When the TRDi register value matches the TRDGRBi register value.	R/W
b2	IMFC	Input-capture/compare-match flag C	[Condition for setting this bit to 0] Write 0 after reading. (1) [Condition for setting this bit to 1] When the TRDi register value matches the TRDGRCi register value (2).	R/W
b3	IMFD	Input-capture/compare-match flag D	[Condition for setting this bit to 0] Write 0 after reading. (1) [Condition for setting this bit to 1] When the TRDi register value matches the TRDGRDi register value (2).	R/W
b4	OVF	Overflow flag	[Condition for setting this bit to 0] Write 0 after reading. (1) [Condition for setting this bit to 1] When the TRDi register overflows.	R/W
b5	UDF	Underflow flag (1)	This bit is disabled in PWM3 Mode.	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b7	—			

Notes:
1. The results of writing to these bits are as follows:
   - The bit is set to 0 when it is first read as 1 and then 0 is written to it.
   - The bit remains unchanged even if it is first read as 0 and then 0 is written to it because its previous value is retained. (The bit's value remains 1 even if it is set to 1 from 0 after being read as 0 and having 0 written to it because its previous value is retained.)
   - The bit's value remains unchanged if 1 is written to it.
2. Including w hen the BFji (j = C or D) bit in the TRDMR register is set to 1 (TRDGRji is used as a buffer register).

21.8.12 Timer RD Interrupt Enable Register i (TRDIERi) (i = 0 or 1) in PWM3 Mode

Address 0144h (TRDIER0), 0154h (TRDIER1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	OVIE	IMIED	IMIEC	IMIEB	IMIEA
After Reset	1	1	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input-capture/compare-match interrupt enable bit A	0: Interrupt (IMIA) by IMFA bit disabled 1: Interrupt (IMIA) by IMFA bit enabled	R/W
b1	IMIEB	Input-capture/compare-match interrupt enable bit B	0: Interrupt (IMIB) by IMFB bit disabled 1: Interrupt (IMIB) by IMFB bit enabled	R/W
b2	IMIEC	Input-capture/compare-match interrupt enable bit C	0: Interrupt (IMIC) by IMFC bit disabled 1: Interrupt (IMIC) by IMFC bit enabled	R/W
b3	IMIED	Input-capture/compare-match interrupt enable bit D	0: Interrupt (IMID) by IMFD bit disabled 1: Interrupt (IMID) by the IMFD bit enabled	R/W
b4	OVIE	Overflow/underflow interrupt enable bit	0: Interrupt (OVI) by OVF bit disabled 1: Interrupt (OVI) by OVF bit enabled	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b6	—			
b7	—			

21.8.13 Timer RD Counter 0 (TRD0) in PWM3 Mode

Address 0147h to 0146h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	A count source is counted. Count operation is increment. When an overflow occurs, the OVF bit in the TRDSR0 register is set to 1.	0000h to FFFFh	R/W

Access the TRD0 register in 16-bit units. Do not access it in 8-bit units.
The TRD1 register is not used in PWM3 mode.

21.8.14 Timer RD General Registers Ai, Bi, Ci, and Di (TRDGRAi, TRDGRBi, TRDGRCi, TRDGRDi) (i = 0 or 1) in PWM3 Mode

Address 0149h to 0148h (TRDGRA0), 014Bh to 014Ah (TRDGRB0),
014Dh to 014Ch (TRDGRC0), 014Fh to 014Eh (TRDGRD0),
0159h to 0158h (TRDGRA1), 015Bh to 015Ah (TRDGRB1),
015Dh to 015Ch (TRDGRC1), 015Fh to 015Eh (TRDGRD1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b15 to b0	Refer to **Table 21.16 TRDGRji Register Functions in PWM3 Mode**	R/W

Access registers TRDGRAi to TRDGRDi in 16-bit units. Do not access them in 8-bit units.

The following registers are disabled for the PWM3 mode function:
TRDPMR, TRDDF0, TRDDF1, TRDIORA0, TRDIORC0, TRDPOCR0, TRDIORA1, TRDIORC1, and TRDPOCR1.

Table 21.16 TRDGRji Register Functions in PWM3 Mode

Register	Setting	Register Function	PWM Output Pin
TRDGRA0	–	General register. Set the PWM period. Setting range: TRDGRA1 register setting value or above	TRDIOA0
TRDGRA1		General register. Set the changing point (the active level timing) of PWM output. Setting range: TRDGRA0 register setting value or below	
TRDGRB0		General register. Set the changing point (the timing that returns to initial output level) of PWM output. Setting range: TRDGRB1 register setting value or above, TRDGRA0 register setting value or below	TRDIOB0
TRDGRB1		General register. Set the changing point (active level timing) of PWM output. Setting range: TRDGRB0 register setting value or below	
TRDGRC0	BFC0 = 0	(These registers are not used in PWM3 mode.)	–
TRDGRC1	BFC1 = 0		
TRDGRD0	BFD0 = 0		
TRDGRD1	BFD1 = 0		
TRDGRC0	BFC0 = 1	Buffer register. Set the next PWM period. (Refer to **21.2.2 Buffer Operation**.) Setting range: TRDGRC1 register setting value or above	TRDIOA0
TRDGRC1	BFC1 = 1	Buffer register. Set the changing point of next PWM output. (Refer to **21.2.2 Buffer Operation**.) Setting range: TRDGRC0 register setting value or below	
TRDGRD0	BFD0 = 1	Buffer register. Set the changing point of next PWM output. (Refer to **21.2.2 Buffer Operation**.) Setting range: TRDGRD1 register setting value or above, TRDGRC0 register setting value or below	TRDIOB0
TRDGRD1	BFD1 = 1	Buffer register. Set the changing point of next PWM output. (Refer to **21.2.2 Buffer Operation**.) Setting range: TRDGRD0 register setting value or below	

BFC0, BFD0, BFC1, BFD1: Bits in TRDMR register

Registers TRDGRC0, TRDGRC1, TRDGRD0, and TRDGRD1 are not used in PWM3 mode. To use them as buffer registers, set bits BFC0, BFC1, BFD0, and BFD1 to 0 (general register) and write a value to the TRDGRC0, TRDGRC1, TRDGRD0, or TRDGRD1 register. After this, bits BFC0, BFC1, BFD0, and BFD1 may be set to 1 (buffer register).

21.8.15 Timer RD Pin Select Register 0 (TRDPSR0)

Address 0184h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRDIOD0SEL1	TRDIOD0SEL0	TRDIOC0SEL1	TRDIOC0SEL0	TRDIOB0SEL1	TRDIOB0SEL0	TRDIOA0SEL1	TRDIOA0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRDIOA0SEL0	TRDIOA0/TRDCLK pin select bit	b1 b0 0 0: TRDIOA0/TRDCLK pin not used 0 1: P6_0 assigned 1 0: P10_0 assigned 1 1: Do not set.	R/W
b1	TRDIOA0SEL1			R/W
b2	TRDIOB0SEL0	TRDIOB0 pin select bit	b3 b2 0 0: TRDIOB0 pin not used 0 1: P6_1 assigned 1 0: P10_1 assigned 1 1: Do not set.	R/W
b3	TRDIOB0SEL1			R/W
b4	TRDIOC0SEL0	TRDIOC0 pin select bit	b5 b4 0 0: TRDIOC0 pin not used 0 1: P6_2 assigned 1 0: P10_2 assigned 1 1: Do not set.	R/W
b5	TRDIOC0SEL1			R/W
b6	TRDIOD0SEL0	TRDIOD0 pin select bit	b7 b6 0 0: TRDIOC0 pin not used 0 1: P6_3 assigned 1 0: P10_3 assigned 1 1: Do not set.	R/W
b7	TRDIOD0SEL1			R/W

The TRDPSR0 register selects which pin is assigned as the timer RD input/output. To use the I/O pins for timer RD, set this register.

Set the TRDPSR0 register before setting the timer RD associated registers. Also, do not change the setting value of this register during timer RD operation.

21.8.16 Timer RD Pin Select Register 1 (TRDPSR1)

Address 0185h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRDIOD1SEL1	TRDIOD1SEL0	TRDIOC1SEL1	TRDIOC1SEL0	TRDIOB1SEL1	TRDIOB1SEL0	TRDIOA1SEL1	TRDIOA1SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRDIOA1SEL0	TRDIOA1 pin select bit	b1 b0 0 0: TRDIOA1 pin not used 0 1: P6_4 assigned 1 0: P10_4 assigned 1 1: Do not set.	R/W
b1	TRDIOA1SEL1			R/W
b2	TRDIOB1SEL0	TRDIOB1 pin select bit	b3 b2 0 0: TRDIOB1 pin not used 0 1: P6_5 assigned 1 0: P10_5 assigned 1 1: Do not set.	R/W
b3	TRDIOB1SEL1			R/W
b4	TRDIOC1SEL0	TRDIOC1 pin select bit	b5 b4 0 0: TRDIOC1 pin not used 0 1: P6_6 assigned 1 0: P10_6 assigned 1 1: Do not set.	R/W
b5	TRDIOC1SEL1			R/W
b6	TRDIOD1SEL0	TRDIOD1 pin select bit	b7 b6 0 0: TRDIOC1 pin not used 0 1: P6_7 assigned 1 0: P10_7 assigned 1 1: Do not set.	R/W
b7	TRDIOD1SEL1			R/W

The TRDPSR1 register selects which pin is assigned as the timer RD input/output. To use the I/O pins for timer RD, set this register.

Set the TRDPSR1 register before setting the timer RD associated registers. Also, do not change the setting value of this register during timer RD operation.

21.8.17 Operating Example

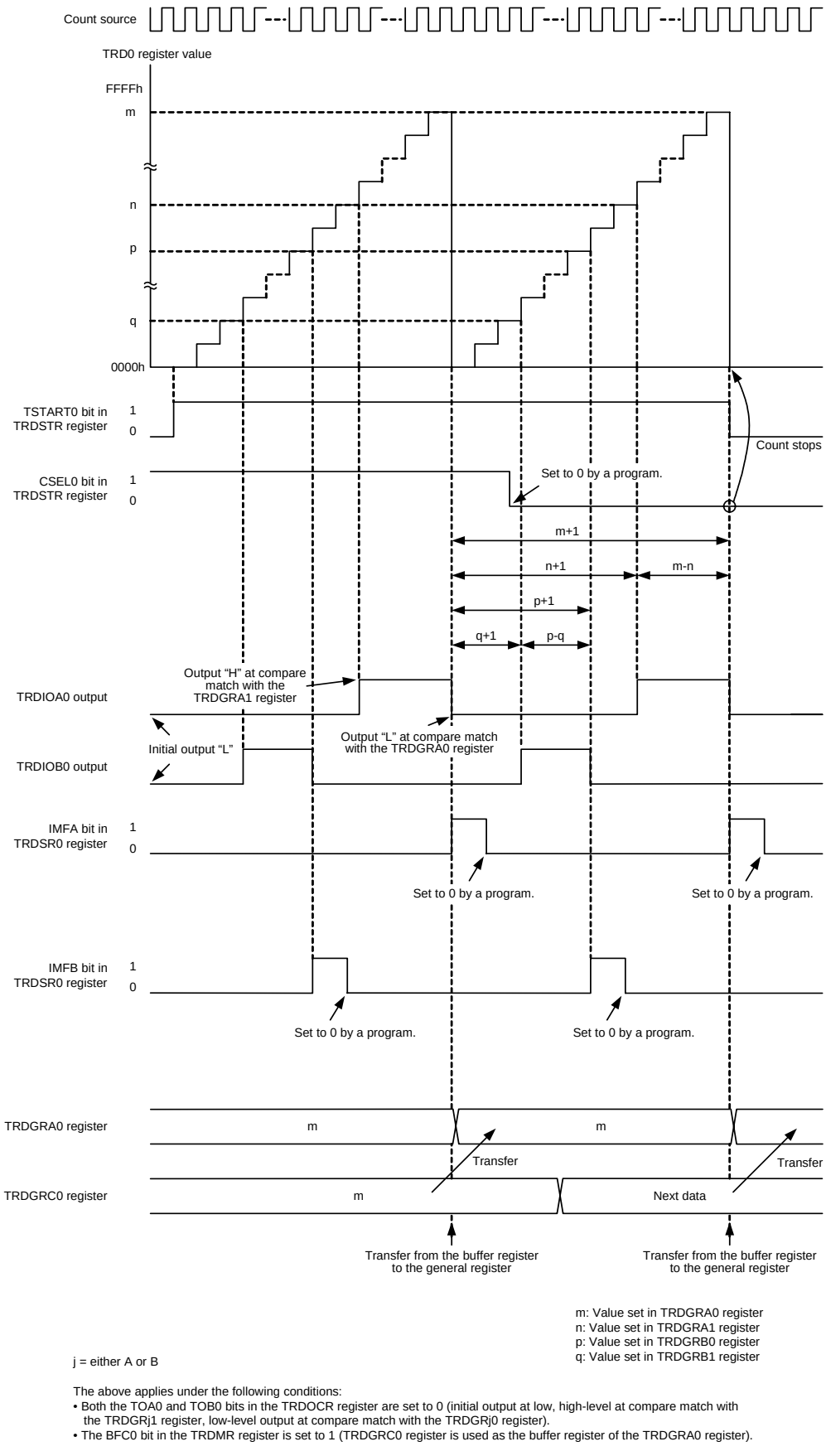


Figure 21.23 Operating Example in PWM3 Mode

21.8.18 A/D Trigger Generation

A compare match signal with registers TRDi (i = 0 or 1) and TRDGRji (j = A, B, C, or D) can be used as the conversion start trigger of the A/D converter.
The TRDADCR register is used to select which compare match is used.

21.9 Timer RD Interrupt

Timer RD generates the timer RDi (i = 0 or 1) interrupt request based on six sources for each timer RD0 and timer RD1. The timer RD interrupt uses the single TRDiIC register (bits IR, and ILVL0 to ILVL2), and a single vector for each timer RD0 and timer RD1. Table 21.17 lists the Registers Associated with Timer RD Interrupt, and Figure 21.24 shows a Block Diagram of Timer RD Interrupt.

Table 21.17 Registers Associated with Timer RD Interrupt

	Timer RD Status Register	Timer RD Interrupt Enable Register	Timer RD Interrupt Control Register
Timer RD0	TRDSR0	TRDIER0	TRD0IC
Timer RD1	TRDSR1	TRDIER1	TRD1IC

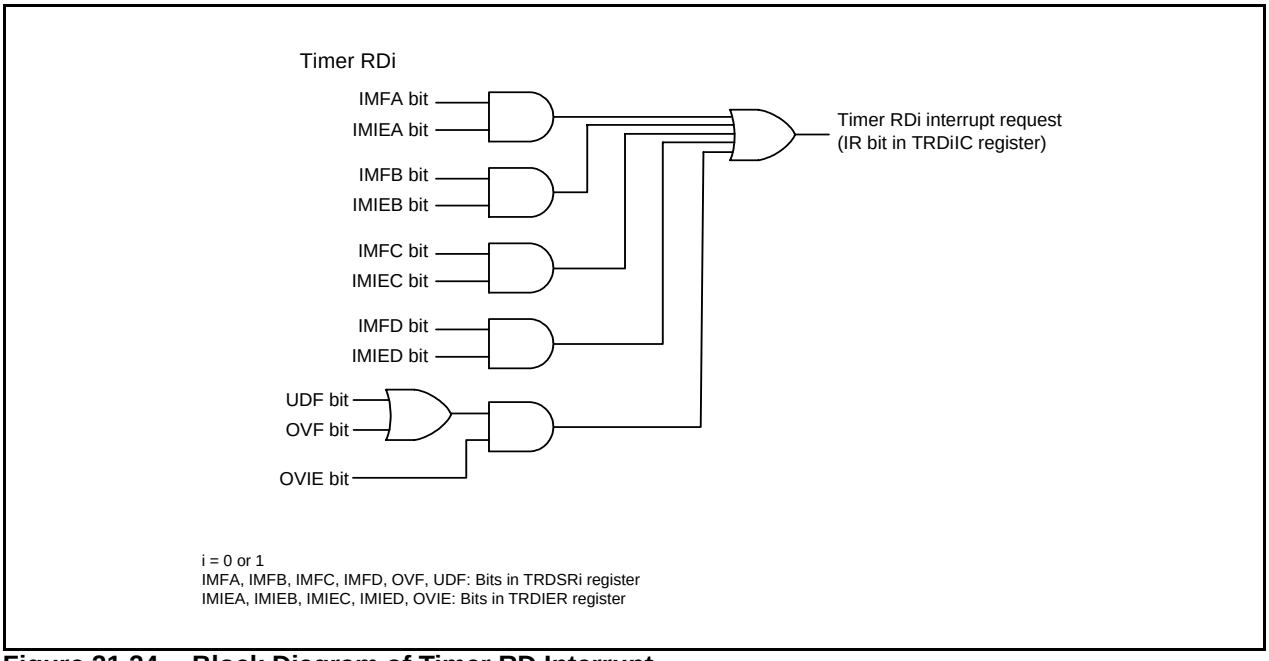


Figure 21.24 Block Diagram of Timer RD Interrupt

As with other maskable interrupts, the timer RD interrupt is controlled by the combination of the I flag, IR bit, bits ILVL0 to ILVL2, and IPL. However, since the interrupt source (timer RD interrupt) is generated by a combination of multiple interrupt request sources, the following differences from other maskable interrupts apply:

- When bits in the TRDSRi register corresponding to bits set to 1 in the TRDIERi register are set to 1 (interrupt enabled), the IR bit in the TRDiIC register is set to 1 (interrupt requested).
- When either bits in the TRDSRi register or bits in the TRDIERi register corresponding to bits in the TRDSRi register, or both of them, are set to 0, the IR bit is set to 0 (no interrupt requested). Therefore, even though the interrupt is not acknowledged after the IR bit is set to 1, the interrupt request will not be maintained.
- When the conditions of other request sources are met, the IR bit remains 1.
- When multiple bits in the TRDIERi register are set to 1, which request source causes an interrupt is determined by the TRDSRi register.
- Since each bit in the TRDSRi register is not automatically set to 0 even if the interrupt is acknowledged, set each bit to 0 in the interrupt routine. For information on how to set these bits to 0, refer to the descriptions of the registers used in different modes (**21.3.11, 21.4.14, 21.5.12, 21.6.10, 21.7.10, and 21.8.11**).

Refer to **Registers TRDSR0 to TRDSR1 in each mode (21.3.11, 21.4.14, 21.5.12, 21.6.10, 21.7.10, and 21.8.11)** for the TRDSRi register. Refer to **Registers TRDIER0 to TRDIER1 in each mode (21.3.12, 21.4.15, 21.5.13, 21.6.11, 21.7.11, and 21.8.12)** for the TRDIERi register.
Refer to **12.3 Interrupt Control** for information on the TRDiIC register and **12.1.5.2 Relocatable Vector Tables** for the interrupt vectors.

21.10 Notes on Timer RD

21.10.1 TRDSTR Register

- Set the TRDSTR register using the MOV instruction.

- When the CSELi (i = 0 or 1) is set to 0 (count stops at compare match between registers TRDi and TRDGRAi), the count does not stop and the TSTARTi bit remains unchanged even if 0 (count stops) is written to the TSTARTi bit.
  When the CSELi bit is set to 0, write 0 to the TSTARTi bit to change other bits without changing the TSTARTi bit.
  To stop counting by a program, write 0 to the TSTARTi bit after setting the CSELi bit to 1. If 1 is written to the CSELi bit and 0 is written to the TSTARTi bit is set to 0 at the same time (with one instruction), the count cannot be stopped.

- Table 21.18 lists the TRDIOji (j = A, B, C, or D) Pin Output Level when Count Stops while the TRDIOji (j = A, B, C, or D) pin is used for the timer RD output.

Table 21.18 TRDIOji (j = A, B, C, or D) Pin Output Level when Count Stops

Stopping Count	TRDIOji Pin Output when Count Stops
When the CSELi bit is set to 1, write 0 to the TSTARTi bit and the count stops.	Holds the output level immediately before the count stops.
When the CSELi bit is set to 0, the count stops at compare match between registers TRDi and TRDGRAi.	Holds the output level after the output changes by the compare match.

21.10.2 TRDi Register (i = 0 or 1)

- When writing the value to the TRDi register by a program while the TSTARTi bit in the TRDSTR register is set to 1 (count starts), avoid overlapping with the timing for setting the TRDi register to 0000h, and then write. If the timing for setting the TRDi register to 0000h overlaps with the timing for writing the value to the TRDi register, the value is not written and the TRDi register is set to 0000h.
  These notes apply when selecting the following by bits CCLR2 to CCLR0 in the TRDCRi register.
  - 001b (Clear by the TRDi register at compare match with the TRDGRAi register.)
  - 010b (Clear by the TRDi register at compare match with the TRDGRBi register.)
  - 011b (Synchronous clear)
  - 101b (Clear by the TRDi register at compare match with the TRDGRCi register.)
  - 110b (Clear by the TRDi register at compare match with the TRDGRDi register.)

- When writing the value to the TRDi register and continuously reading the same register, the value before writing may be read. In this case, execute the JMP.B instruction between the writing and reading.

```
Program example     MOV.W   #XXXXh, TRD0     ;Write
                    JMP.B   L1               ;JMP.B
                L1: MOV.W   TRD0,DATA        ;Read
```

21.10.3 TRDSRi Register (i = 0 or 1)

When writing the value to the TRDSRi register and continuously reading the same register, the value before writing may be read. In this case, execute the JMP.B instruction between the writing and reading.

```
Program example     MOV.B   #XXh, TRDSR0    ;Write
                    JMP.B   L1              ;JMP.B
                L1: MOV.B   TRDSR0,DATA     ;Read
```

21.10.4 Count Source Switching

• Switch the count source after the count stops.

Switching procedure

(1) Set the TSTARTi (i = 0 or 1) bit in the TRDSTR register to 0 (count stops).
(2) Change bits TCK2 to TCK0 in the TRDCRi register.

• When changing the count source from fOCO40M to another source and stopping fOCO40M, wait two or more cycles of f1 after setting the clock switch, and then stop fOCO40M.

Switching procedure

(1) Set the TSTARTi (i = 0 or 1) bit in the TRDSTR register to 0 (count stops).
(2) Change bits TCK2 to TCK0 in the TRDCRi register.
(3) Wait for two or more cycles of f1.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

21.10.5 Input Capture Function

• The pulse width of the input capture signal should be set to three or more cycles of the timer RD operating clock (refer to **Table 21.1 Timer RD Operating Clocks**).
• The value of the TRDi register is transferred to the TRDGRji register two or three cycles of the timer RD operating clock after the input capture signal is applied to the TRDIOji pin (i = 0 or 1, j = either A, B, C, or D) (when the digital filter is not used).

21.10.6 Reset Synchronous PWM Mode

• When reset synchronous PWM mode is used for motor control, make sure OLS0 = OLS1.
• Set to reset synchronous PWM mode by the following procedure:

Switching procedure

(1) Set the TSTART0 bit in the TRDSTR register to 0 (count stops).
(2) Set bits CMD1 to CMD0 in the TRDFCR register to 00b (timer mode, PWM mode, and PWM3 mode).
(3) Set bits CMD1 to CMD0 to 01b (reset synchronous PWM mode).
(4) Set the other registers associated with timer RD again.

21.10.7 Complementary PWM Mode

- When complementary PWM mode is used for motor control, make sure OLS0 = OLS1.
- Change bits CMD1 to CMD0 in the TRDFCR register in the following procedure.

Switching procedure: When setting to complementary PWM mode (including re-set), or changing the transfer timing from the buffer register to the general register in complementary PWM mode.

(1) Set both the TSTART0 and TSTART1 bits in the TRDSTR register to 0 (count stops).
(2) Set bits CMD1 to CMD0 in the TRDFCR register to 00b (timer mode, PWM mode, and PWM3 mode).
(3) Set bits CMD1 to CMD0 to 10b or 11b (complementary PWM mode).
(4) Set the registers associated with other timer RD again.

Switching procedure: When stopping complementary PWM mode

(1) Set both the TSTART0 and TSTART1 bits in the TRDSTR register to 0 (count stops).
(2) Set bits CMD1 to CMD to 00b (timer mode, PWM mode, and PWM3 mode).

- Do not write to TRDGRA0, TRDGRB0, TRDGRA1, or TRDGRB1 register during operation.
  When changing the PWM waveform, transfer the values written to registers TRDGRD0, TRDGRC1, and TRDGRD1 to registers TRDGRB0, TRDGRA1, and TRDGRB1 using the buffer operation.
  However, to write data to the TRDGRD0, TRDGRC1, or TRDGRD1 register, set bits BFD0, BFC1, and BFD1 to 0 (general register). After this, bits BFD0, BFC1, and BFD1 may be set to 1 (buffer register).
  The PWM period cannot be changed.

- If the value set in the TRDGRA0 register is assumed to be m, the TRD0 register counts m-1, m, m+1, m, m-1, in that order, when changing from increment to decrement operation.
  When changing from m to m+1, the IMFA bit is set to 1. Also, bits CMD1 to CMD0 in the TRDFCR register are set to 11b (complementary PWM mode, buffer data transferred at compare match between registers TRD0 and TRDGRA0), the content of the buffer registers (TRDGRD0, TRDGRC1, and TRDGRD1) is transferred to the general registers (TRDGRB0, TRDGRA1, and TRDGRB1).
  During m+1, m, and m-1 operation, the IMFA bit remains unchanged and data are not transferred to registers such as the TRDGRA0 register.

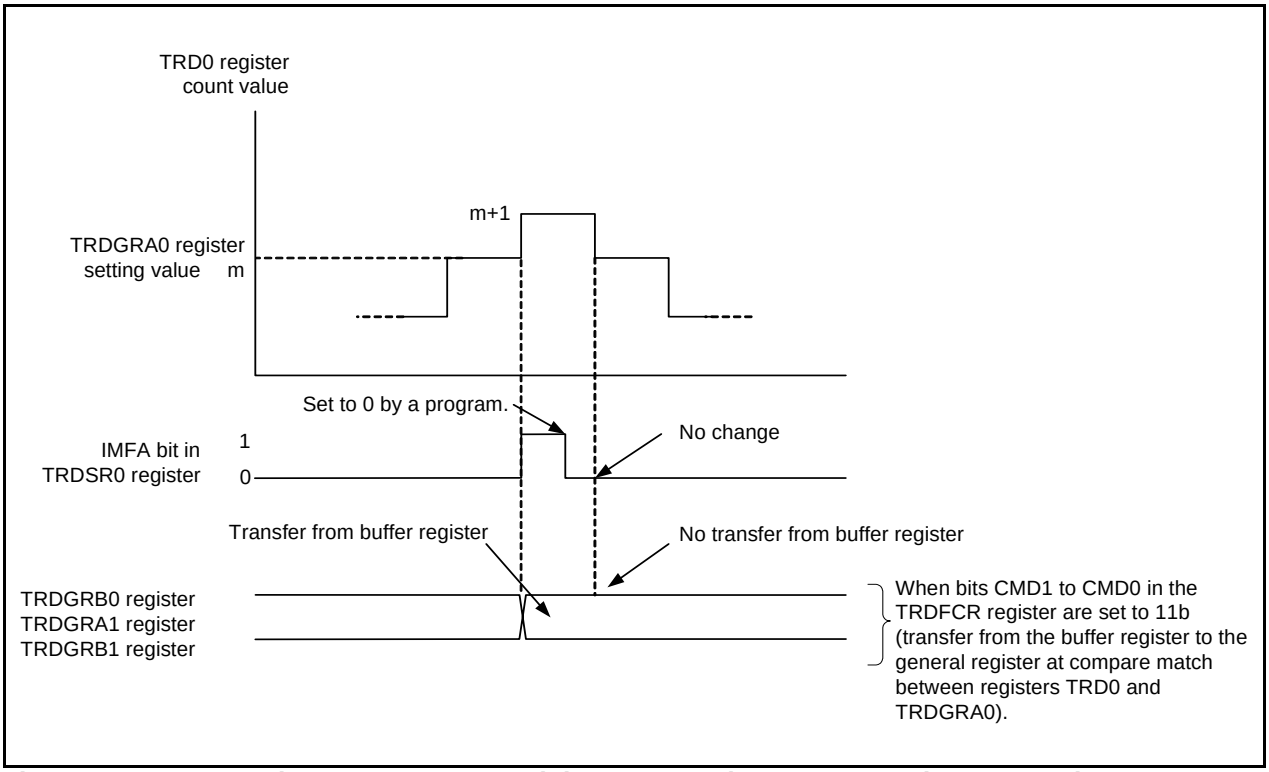


Figure 21.25 Operation at Compare Match between Registers TRD0 and TRDGRA0 in Complementary PWM Mode

- The TRD1 register counts 1, 0, FFFFh, 0, 1, in that order, when changing from decrement to increment operation.

  The UDF bit is set to 1 when changing between 1, 0, and FFFFh operation. Also, when bits CMD1 to CMD0 in the TRDFCR register are set to 10b (complementary PWM mode, buffer data transferred at underflow in the TRD1 register), the content of the buffer registers (TRDGRD0, TRDGRC1, and TRDGRD1) is transferred to the general registers (TRDGRB0, TRDGRA1, and TRDGRB1). During FFFFh, 0, 1 operation, data are not transferred to registers such as the TRDGRB0 register. Also, at this time, the OVF bit remains unchanged.

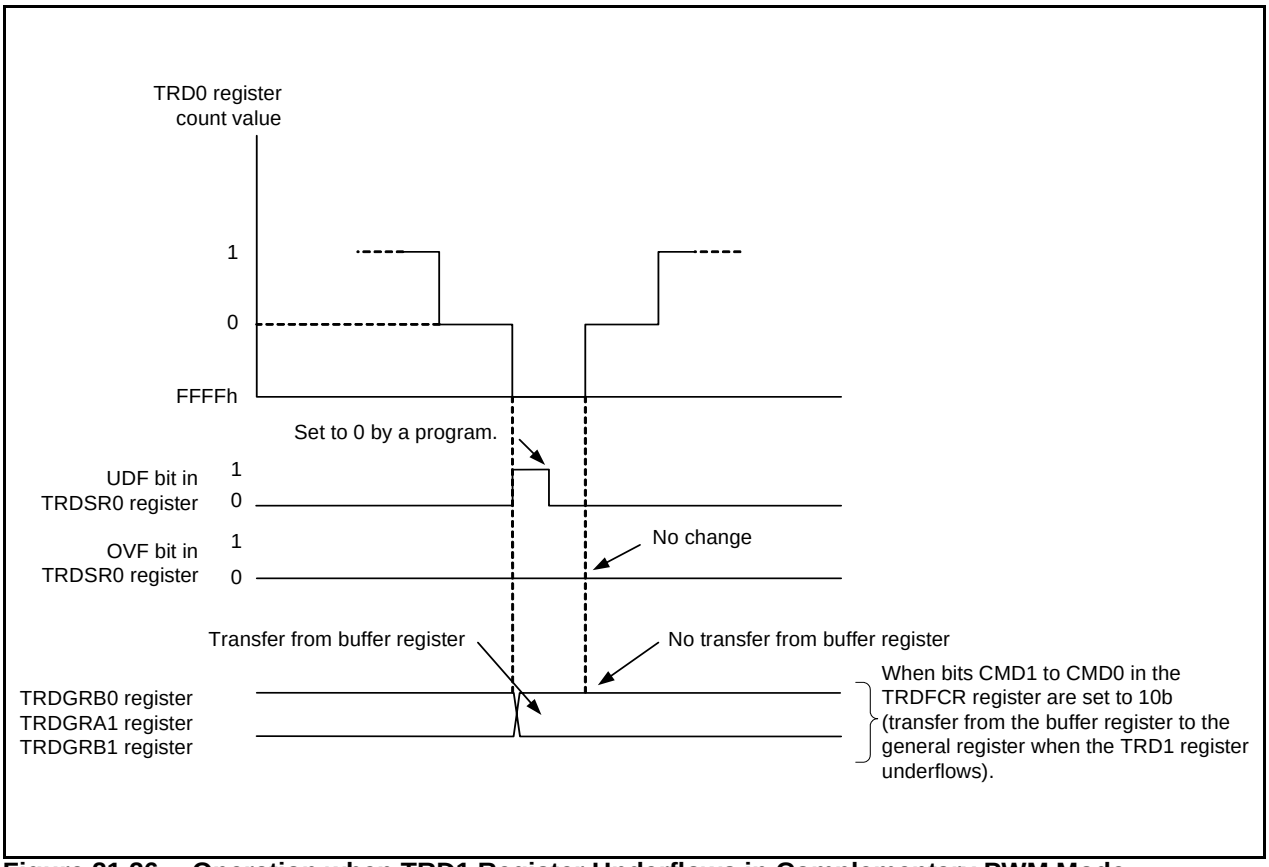


Figure 21.26 Operation when TRD1 Register Underflows in Complementary PWM Mode

- Using bits CMD1 to CMD0, select the timing of data transfer from the buffer register to the general register. However, transfer takes place with the following timing in spite of the values of bits CMD1 to CMD0 in the following cases:

  Buffer register value ≥ TRDGRA0 register value:
  Transfer takes place at underflow of the TRD1 register.
  After this, when the buffer register is set to 0001h or above and a value smaller than the value of the TRDGRA0 register, and the TRD1 register underflows for the first time after setting, the value is transferred to the general register. After that, the value is transferred with the timing selected by bits CMD1 to CMD0.

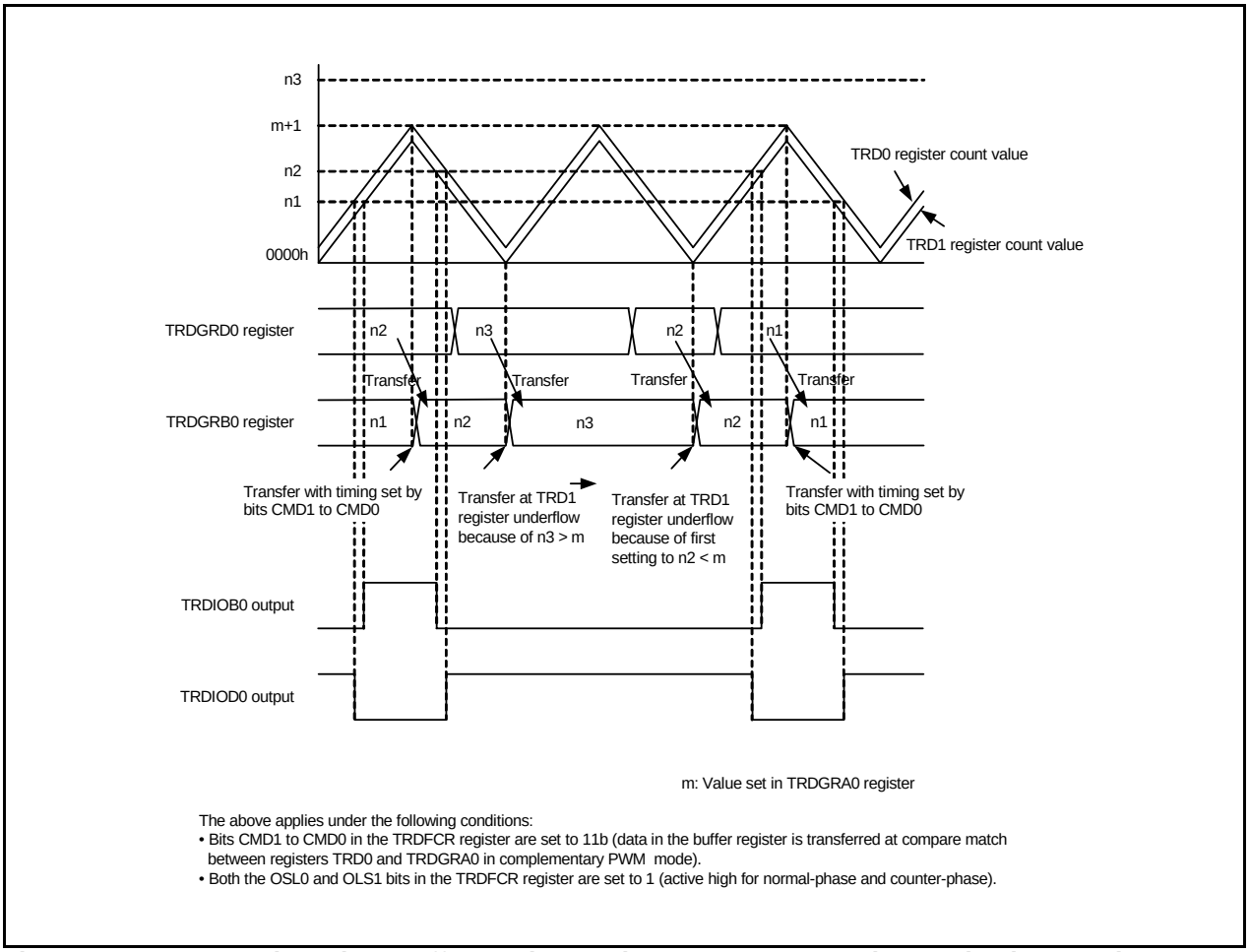
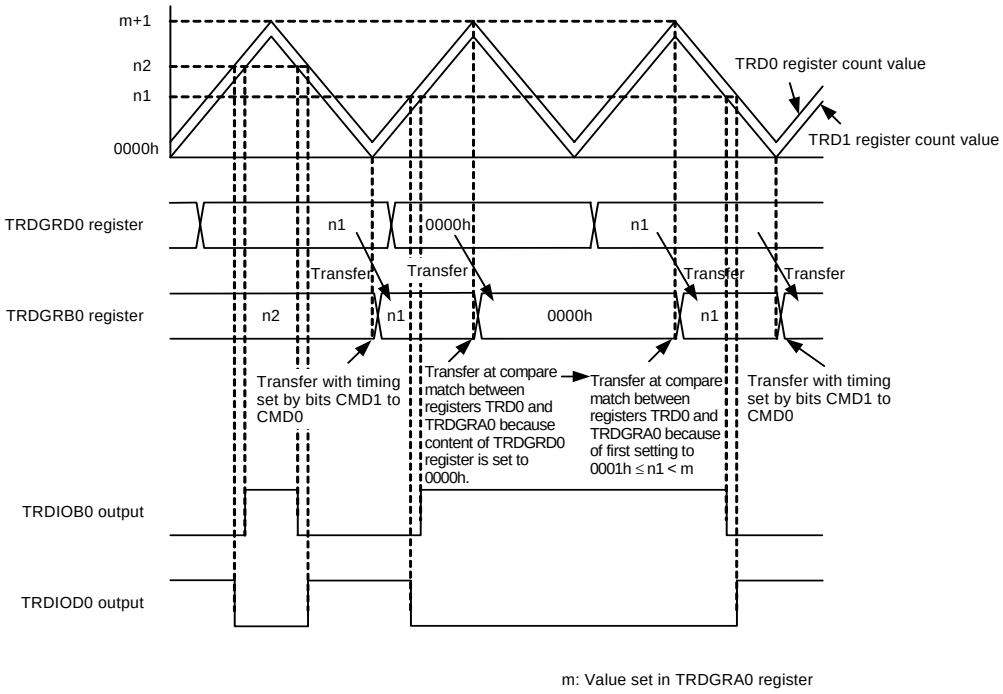


Figure 21.27 Operation when Buffer Register Value ≥ TRDGRA0 Register Value in Complementary PWM Mode

When the value of the buffer register is set to 0000h:
Transfer takes place at compare match between registers TRD0 and TRDGRA0.
After this, when the buffer register is set to 0001h or above and a value than smaller the value of the TRDGRA0 register, and a compare match occurs between registers TRD0 and TRDGRA0 for the first time after setting, the value is transferred to the general register. After that, the value is transferred with the timing selected by bits CMD0 and CMD1.



The above applies under the following conditions:
- Bits CMD1 to CMD0 in the TRDFCR register are set to 10b (data in the buffer register is transferred at TRD1 register underflow in PWM mode).
- Both the OLS0 and OLS1 bits in the TRDFCR register are set to 1 (active high for normal-phase and counter-phase).

Figure 21.28 Operation when Buffer Register Value Is Set to 0000h in Complementary PWM Mode

21.10.8 Count Source fOCO40M

- The count source fOCO40M can be used with supply voltage VCC = 2.7 to 5.5 V. For supply voltage other than that, do not set bits TCK2 to TCK0 in registers TRDCR0 and TRDCR to 110b (fOCO40M selected as the count source).

22. Timer RE

Timer RE has a 4-bit counter and 8-bit counter.

22.1 Introduction

Timer RE supports the following two modes:

- Real-time clock mode — A 1-second signal from fC4 is generated and seconds, minutes, hours, and days of the week are counted.
- Output compare mode — A count source is counted and compare matches are detected.

The count source for timer RE is the operating clock that regulates the timing of timer operations.
Table 22.1 lists the Timer RE Pin Configuration.

Table 22.1 Timer RE Pin Configuration

Pin Name	Assigned Pin	I/O	Function
TREO	P11_7	Output	Function differs according to the mode. Refer to descriptions of individual modes for details.

22.2 Real-Time Clock Mode

In real-time clock mode, a 1-second signal is generated from fC4 using a divide-by-2 frequency divider, 4-bit counter, and 8-bit counter and used to count seconds, minutes, hours, and days of the week. Figure 22.1 shows a Block Diagram of Real-Time Clock Mode, Table 22.2 lists the Real-Time Clock Mode Specifications, and Table 22.3 lists Interrupt Sources. Figure 22.2 shows the Definition of Time Representation and Figure 22.3 shows an Operating Example in Real-Time Clock Mode.

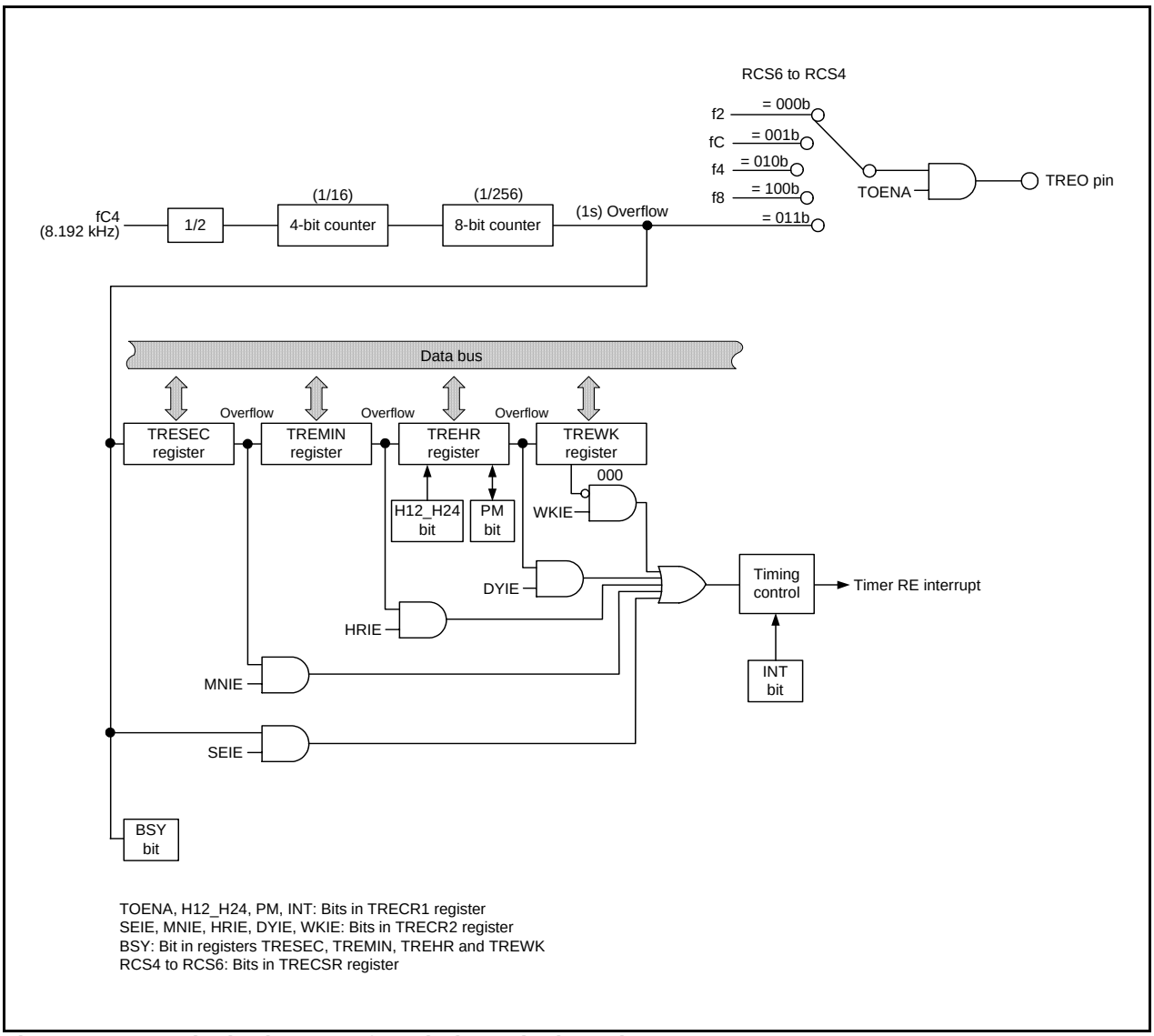


Figure 22.1 Block Diagram of Real-Time Clock Mode

Table 22.2 Real-Time Clock Mode Specifications

Item	Specification
Count source	fC4
Count operation	Increment
Count start condition	1 (count starts) is written to TSTART bit in TRECR1 register.
Count stop condition	0 (count stops) is written to TSTART bit in TRECR1 register.
Interrupt request generation timing	Select either one of the following: • Update of second data • Update of minute data • Update of hour data • Update of day of week data • When day of week data is set to 000b (Sunday).
TREO pin function	Programmable I/O port or output of f2, fC, f4, f8, or 1 Hz
Read from timer	When reading TRESEC, TREMIN, TREHR, or TREWK register, the count value can be read. The values read from registers TRESEC, TREMIN, and TREHR are represented by the BCD code.
Write to timer	When bits TSTART and TCSTF in the TRECR1 register are set to 0 (timer stops), the value can be written to registers TRESEC, TREMIN, TREHR, and TREWK. The values written to registers TRESEC, TREMIN, and TREHR are represented by the BCD codes.
Selectable function	• 12-hour mode/24-hour mode switch function

22.2.1 Timer RE Second Data Register (TRESEC) in Real-Time Clock Mode

Address 0118h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BSY	SC12	SC11	SC10	SC03	SC02	SC01	SC00
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	Setting Range	R/W
b0	SC00	1st digit of second count bit	Count 0 to 9 every second. When the digit moves up, 1 is added to the 2nd digit of second.	0 to 9 (BCD code)	R/W
b1	SC01				R/W
b2	SC02				R/W
b3	SC03				R/W
b4	SC10	2nd digit of second count bit	When counting 0 to 5, 60 seconds are counted.	0 to 5 (BCD code)	R/W
b5	SC11				R/W
b6	SC12				R/W
b7	BSY	Timer RE busy flag	This bit is set to 1 while registers TRESEC, TREMIN, TREHR, and TREWK are being updated.		R

22.2.2 Timer RE Minute Data Register (TREMIN) in Real-Time Clock Mode

Address 0119h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BSY	MN12	MN11	MN10	MN03	MN02	MN01	MN00
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	Setting Range	R/W
b0	MN00	1st digit of minute count bit	Count 0 to 9 every minute. When the digit moves up, 1 is added to the 2nd digit of minute.	0 to 9 (BCD code)	R/W
b1	MN01				R/W
b2	MN02				R/W
b3	MN03				R/W
b4	MN10	2nd digit of minute count bit	When counting 0 to 5, 60 minutes are counted.	0 to 5 (BCD code)	R/W
b5	MN11				R/W
b6	MN12				R/W
b7	BSY	Timer RE busy flag	This bit is set to 1 while registers TRESEC, TREMIN, TREHR, and TREWK are being updated.		R

22.2.3 Timer RE Hour Data Register (TREHR) in Real-Time Clock Mode

Address 011Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BSY	—	HR11	HR10	HR03	HR02	HR01	HR00
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	Setting Range	R/W
b0	HR00	1st digit of hour count bit	Count 0 to 9 every hour. When the digit moves up, 1 is added to the 2nd digit of hour.	0 to 9 (BCD code)	R/W
b1	HR01				R/W
b2	HR02				R/W
b3	HR03				R/W
b4	HR10	2nd digit of hour count bit	Count 0 to 1 when the H12_H24 bit is set to 0 (12-hour mode). Count 0 to 2 when the H12_H24 bit is set to 1 (24-hour mode).	0 to 2 (BCD code)	R/W
b5	HR11				R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.			—
b7	BSY	Timer RE busy flag	This bit is set to 1 while registers TRESEC, TREMIN, TREHR, and TREWK are updated.		R

22.2.4 Timer RE Day of Week Data Register (TREWK) in Real-Time Clock Mode

Address 011Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BSY	—	—	—	—	WK2	WK1	WK0
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	WK0	Day of week count bit	b2 b1 b0 0 0 0: Sunday 0 0 1: Monday 0 1 0: Tuesday 0 1 1: Wednesday 1 0 0: Thursday 1 0 1: Friday 1 1 0: Saturday 1 1 1: Do not set.	R/W
b1	WK1			R/W
b2	WK2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	BSY	Timer RE busy flag	This bit is set to 1 while registers TRESEC, TREMIN, TREHR, and TREWK are updated.	R

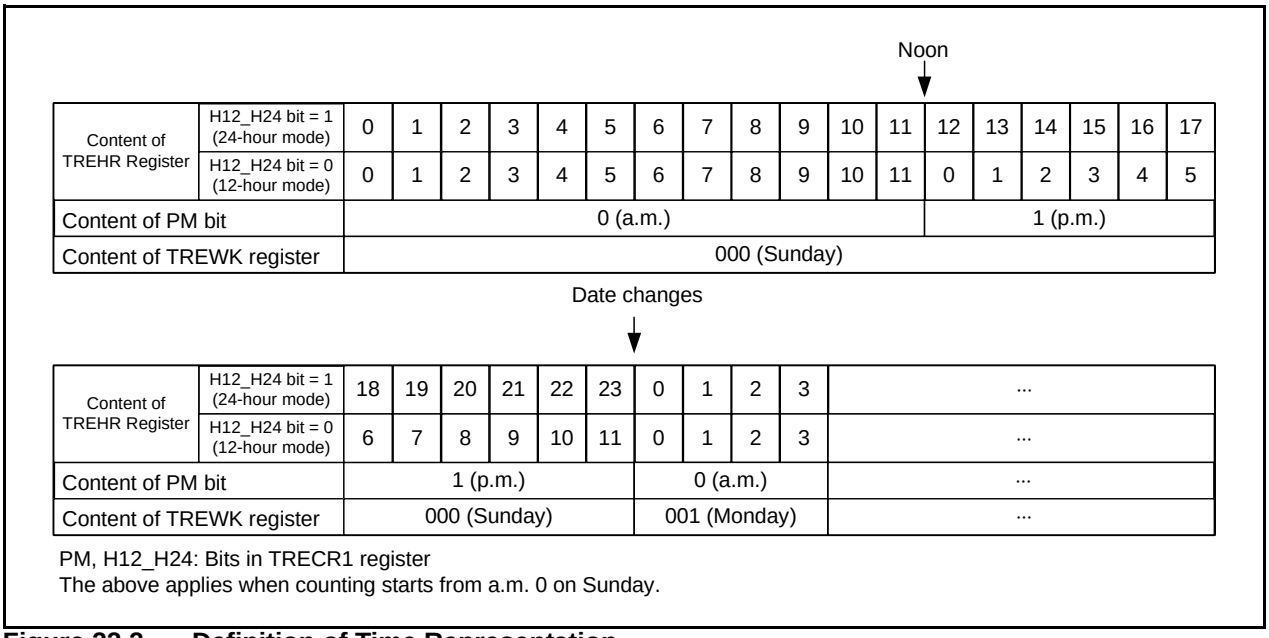
22.2.5 Timer RE Control Register 1 (TRECR1) in Real-Time Clock Mode

Address 011Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TSTART	H12_H24	PM	TRERST	INT	TOENA	TCSTF	—
After Reset	X	X	X	X	X	0	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	TCSTF	Timer RE count status flag	0: Count stopped 1: Counting	R
b2	TOENA	TREO pin output enable bit	0: Clock output disabled 1: Clock output enabled	R/W
b3	INT	Interrupt request timing bit	Set to 1 in real-time clock mode.	R/W
b4	TRERST	Timer RE reset bit	When setting this bit to 0 after setting it to 1, the following will occur: • Registers TRESEC, TREMIN, TREHR, TREWK, and TRECR2 are set to 00h. • Bits TCSTF, INT, PM, H12_H24, and TSTART in the TRECR1 register are set to 0. • The 8-bit counter is set to 00h and the 4-bit counter is set to 0h.	R/W
b5	PM	A.m./p.m. bit	When the H12_H24 bit is set to 0 (12-hour mode) (1) 0: a.m. 1: p.m. When the H12_H24 bit is set to 1 (24-hour mode), its value is undefined.	R/W
b6	H12_H24	Operating mode select bit	0: 12-hour mode 1: 24-hour mode	R/W
b7	TSTART	Timer RE count start bit	0: Count stops 1: Count starts	R/W

Note:
1. This bit is automatically modified while timer RE counts.



PM, H12_H24: Bits in TRECR1 register
The above applies when counting starts from a.m. 0 on Sunday.

Figure 22.2 Definition of Time Representation

22.2.6 Timer RE Control Register 2 (TRECR2) in Real-Time Clock Mode

Address 011Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	COMIE	WKIE	DYIE	HRIE	MNIE	SEIE	SEIE05	SEIE025
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	SEIE025	Periodic interrupt triggered every 0.25 seconds enable bit (1)	0: Periodic interrupt triggered every 0.25 seconds is disabled 1: Periodic interrupt triggered every 0.25 seconds is enabled	R/W
b1	SEIE05	Periodic interrupt triggered every 0.5 seconds enable bit (1)	0: Periodic interrupt triggered every 0.5 seconds is disabled 1: Periodic interrupt triggered every 0.5 seconds is enabled	R/W
b2	SEIE	Periodic interrupt triggered every second enable bit (1)	0: Periodic interrupt triggered every second is disabled 1: Periodic interrupt triggered every second is enabled	R/W
b3	MNIE	Periodic interrupt triggered every minute enable bit (1)	0: Periodic interrupt triggered every minute is disabled 1: Periodic interrupt triggered every minute is enabled	R/W
b4	HRIE	Periodic interrupt triggered every hour enable bit (1)	0: Periodic interrupt triggered every hour is disabled 1: Periodic interrupt triggered every hour is enabled	R/W
b5	DYIE	Periodic interrupt triggered every day enable bit (1)	0: Periodic interrupt triggered every day is disabled 1: Periodic interrupt triggered every day is enabled	R/W
b6	WKIE	Periodic interrupt triggered every week enable bit (1)	0: Periodic interrupt triggered every week is disabled 1: Periodic interrupt triggered every week is enabled	R/W
b7	COMIE	Compare match interrupt enable bit	Set to 0 in real-time clock mode.	R/W

Note:
1. Do not set multiple enable bits to 1 (interrupt enabled).

Table 22.3 Interrupt Sources

Source	Interrupt Source	Interrupt Enable Bit
Periodic interrupt triggered every week	The value of the TREWK register is set to 000b (Sunday) (1-week period).	WKIE
Periodic interrupt triggered every day	The TREWK register is updated (1-day period).	DYIE
Periodic interrupt triggered every hour	The TREHR register is updated (1-hour period).	HRIE
Periodic interrupt triggered every minute	The TREMIN register is updated (1-minute period).	MNIE
Periodic interrupt triggered every second	The TRESEC register is updated (1-second period).	SEIE
Periodic interrupt triggered every 0.5 seconds	The 8-bit counter is updated (0.5-second period).	SEIE05
Periodic interrupt triggered every 0.25 seconds	The 8-bit counter is updated (0.25-second period).	SEIE025

22.2.7 Timer RE Count Source Select Register (TRECSR) in Real-Time Clock Mode

Address 011Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	RCS6	RCS5	RCS4	RCS3	RCS2	RCS1	RCS0
After Reset	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	RCS0	Count source select bit	Set to 00b in real-time clock mode.	R/W
b1	RCS1			R/W
b2	RCS2	4-bit counter select bit	Set to 0 in real-time clock mode.	R/W
b3	RCS3	Real-time clock mode select bit	Set to 1 in real-time clock mode.	R/W
b4	RCS4	Clock output select bit (1)	b6 b5 b4 0 0 0: f2 0 0 1: fC 0 1 0: f4 0 1 1: 1 Hz 1 0 0: f8 Other than above: Do not set.	R/W
b5	RCS5			R/W
b6	RCS6			R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Note:
1. Write to bits RCS4 to RCS6 when the TOENA bit in the TRECR1 register is set to 0 (clock output disabled).

22.2.8 Operating Example

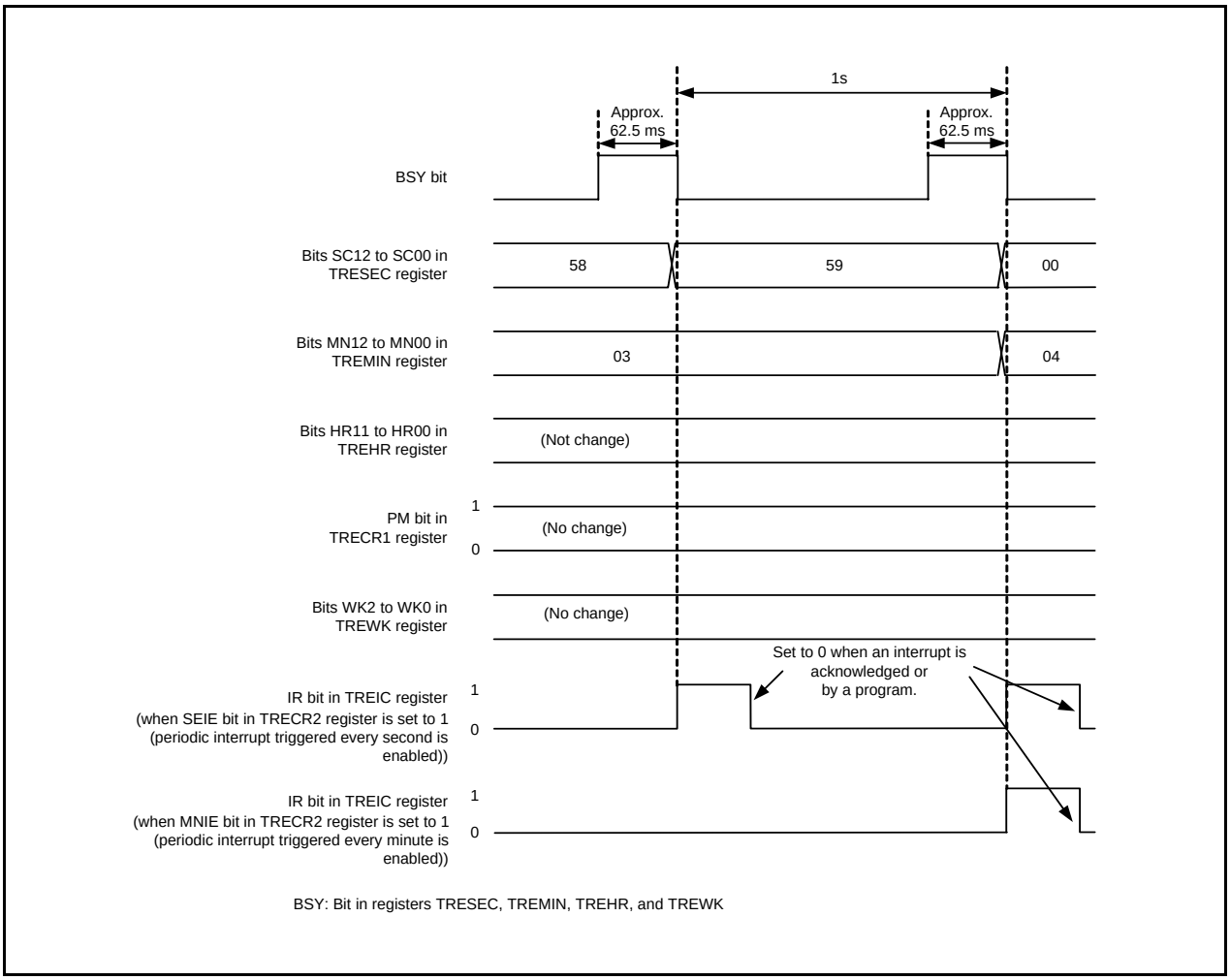


Figure 22.3 Operating Example in Real-Time Clock Mode

22.3 Output Compare Mode

In output compare mode, the internal count source divided by 2 is counted using the 4-bit or 8-bit counter and a compare value match is detected with the 8-bit counter. Figure 22.4 shows a Block Diagram of Output Compare Mode, Table 22.4 lists the Output Compare Mode Specifications, and Figure 22.5 shows an Operating Example in Output Compare Mode.

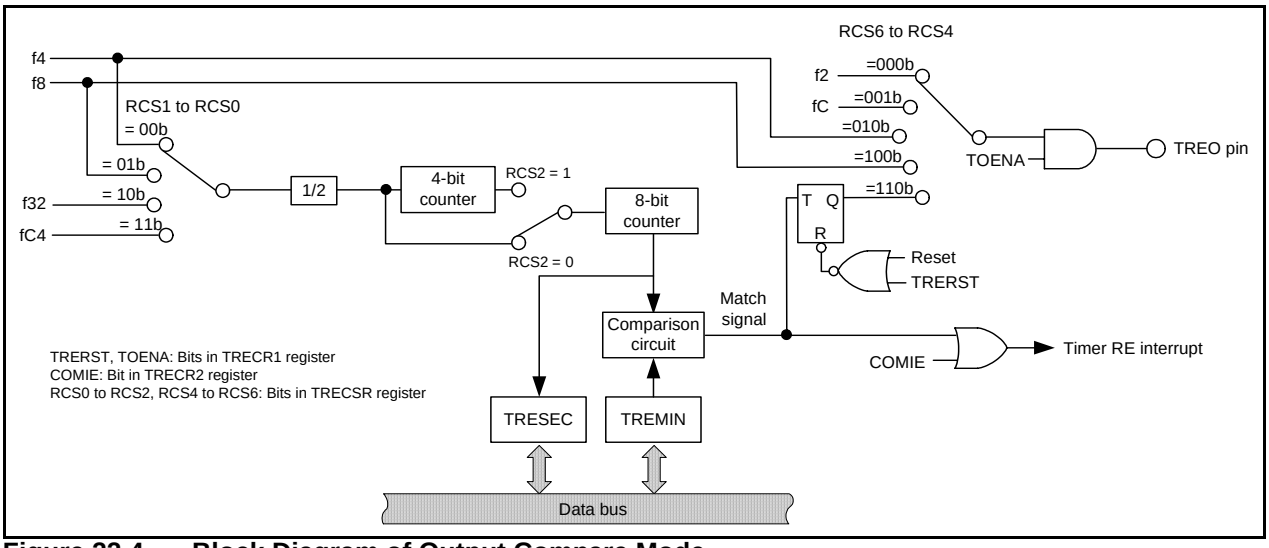


Figure 22.4 Block Diagram of Output Compare Mode

Table 22.4 Output Compare Mode Specifications

Item	Specification
Count sources	f4, f8, f32, fC4
Count operations	• Increment • When the 8-bit counter value matches the TREMIN register content, the value is set back to 00h and the count continues. The count value is retained while the count stops.
Count periods	• When RCS2 = 0 (4-bit counter is not used) 1/fi x 2 x (n+1) • When RCS2 = 1 (4-bit counter is used) 1/fi x 32 x (n+1) fi: Frequency of count source n: Value set in TREMIN register
Count start condition	1 (count starts) is written to the TSTART bit in the TRECR1 register.
Count stop condition	0 (count stops) is write to the TSTART bit in the TRECR1 register.
Interrupt request generation timing	When the contents of the 8-bit counter and the TREMIN register match.
TREO pin function	Select either one of the following: • Programmable I/O port • Output of f2, fC, f4, or f8 • Compare output
Read from timer	When reading the TRESEC register, the 8-bit counter value can be read. When reading the TREMIN register, the compare value can be read.
Write to timer	Writing to the TRESEC register is disabled. When bits TSTART and TCSTF in the TRECR1 register are set to 0 (timer stops), writing to the TREMIN register is enabled.
Selectable functions	• Selectable use of 4-bit counter • Compare output function Every time the 8-bit counter value matches the TREMIN register content, the TREO output polarity is inverted. The TREO pin outputs a low-level signal after reset is deasserted and timer RE is reset by the TRERST bit in the TRECR1 register. The output level is retained by setting the TSTART bit to 0 (count stops).

22.3.1 Timer RE Counter Data Register (TRESEC) in Output Compare Mode

Address 0118h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	R/W
b7 to b0	8-bit counter data can be read. Even if timer RE stops counting, the count value is retained. The TRESEC register is set to 00h at the compare match.	R

22.3.2 Timer RE Compare Data Register (TREMIN) in Output Compare Mode

Address 0119h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	R/W
b7 to b0	8-bit compare data is stored.	R

22.3.3 Timer RE Control Register 1 (TRECR1) in Output Compare Mode

Address 011Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TSTART	H12_H24	PM	TRERST	INT	TOENA	TCSTF	—
After Reset	X	X	X	X	X	0	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	TCSTF	Timer RE count status flag	0: Count stopped 1: Counting	R
b2	TOENA	TREO pin output enable bit	0: Clock output disabled 1: Clock output enabled	R/W
b3	INT	Interrupt request timing bit	Set to 0 in output compare mode.	R/W
b4	TRERST	Timer RE reset bit	When setting this bit to 0 after setting it to 1, the following will occur. • Registers TRESEC, TREMIN, TREHR, TREWK, and TRECR2 are set to 00h. • Bits TCSTF, INT, PM, H12_H24, and TSTART in the TRECR1 register are set to 0. • The 8-bit counter is set to 00h and the 4-bit counter is set to 0h.	R/W
b5	PM	A.m./p.m. bit	Set to 0 in output compare mode.	R/W
b6	H12_H24	Operating mode select bit	Set to 0 in output compare mode.	R/W
b7	TSTART	Timer RE count start bit	0: Count stops 1: Count starts	R/W

22.3.4 Timer RE Control Register 2 (TRECR2) in Output Compare Mode

Address 011Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	COMIE	WKIE	DYIE	HRIE	MNIE	SEIE	SEIE05	SEIE025
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	SEIE025	Periodic interrupt triggered every 0.25 seconds enable bit (1)	Set to 0 in output compare mode.	R/W
b1	SEIE05	Periodic interrupt triggered every 0.5 seconds enable bit (1)		R/W
b2	SEIE	Periodic interrupt triggered every second enable bit (1)		R/W
b3	MNIE	Periodic interrupt triggered every minute enable bit (1)		R/W
b4	HRIE	Periodic interrupt triggered every hour enable bit (1)		R/W
b5	DYIE	Periodic interrupt triggered every day enable bit (1)		R/W
b6	WKIE	Periodic interrupt triggered every week enable bit (1)		R/W
b7	COMIE	Compare match interrupt enable bit	0: Compare match interrupt disabled 1: Compare match interrupt enabled	R/W

Note:
1. Do not set multiple enable bits to 1 (interrupt enabled).

22.3.5 Timer RE Count Source Select Register (TRECSR) in Output Compare Mode

Address 011Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	RCS6	RCS5	RCS4	RCS3	RCS2	RCS1	RCS0
After Reset	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	RCS0	Count source select bit (1)	b1 b0 0 0: f4 0 1: f8 1 0: f32 1 1: fC4	R/W
b1	RCS1			R/W
b2	RCS2	4-bit counter select bit	0: Not used 1: Used	R/W
b3	RCS3	Real-time clock mode select bit	Set to 0 in output compare mode.	R/W
b4	RCS4	Clock output select bit (2)	b6 b5 b4 0 0 0: f2 0 0 1: fC 0 1 0: f4 1 0 0: f8 1 1 0: Compare output Other than above: Do not set.	R/W
b5	RCS5			R/W
b6	RCS6			R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. Write to bits RCS0 to RCS1 when the TCSTF bit in the TRECR1 register is set to 0 (count stopped).
2. Write to bits RCS4 to RCS6 when the TOENA bit in the TRECR1 register is set to 0 (clock output disabled).

22.3.6 Operating Example

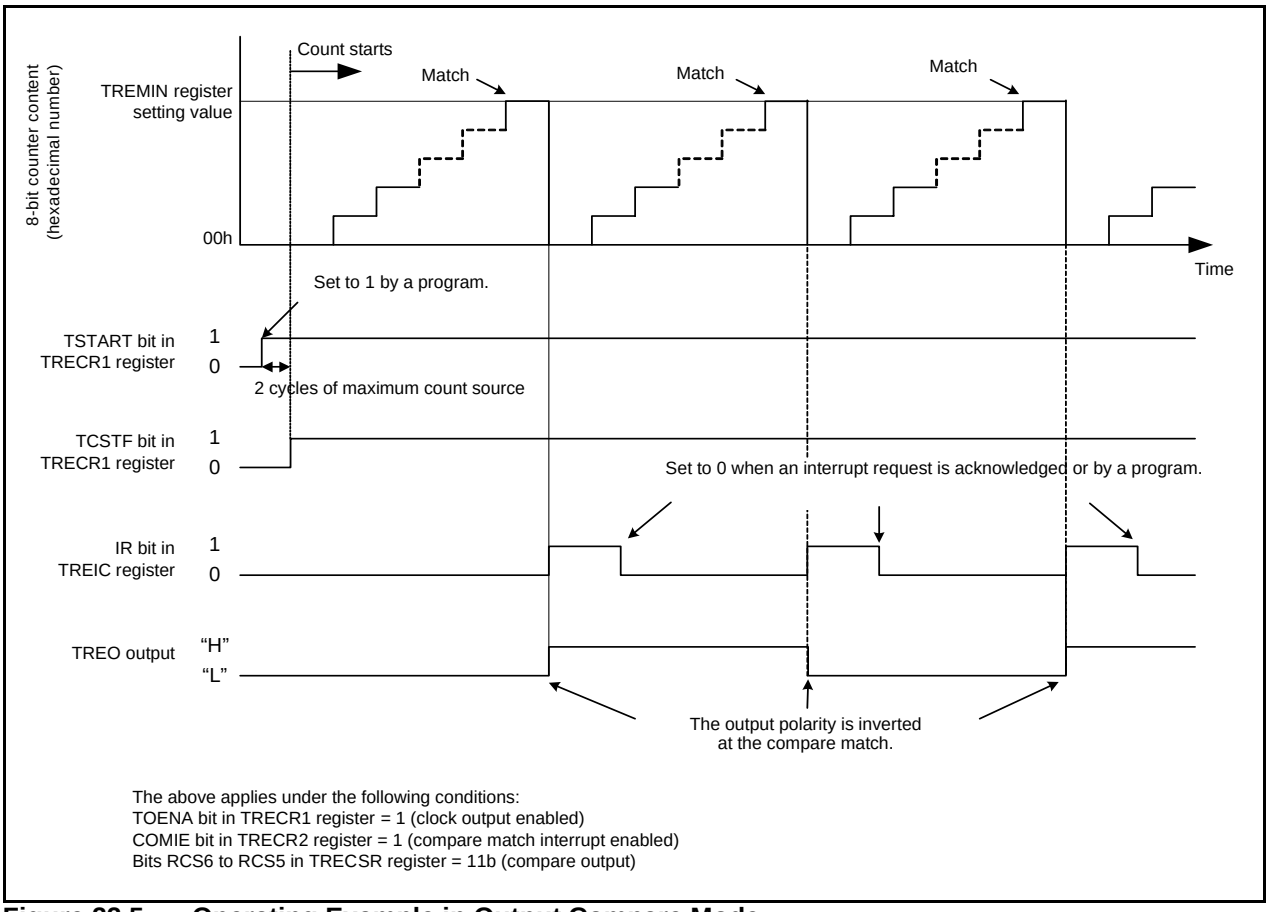


Figure 22.5 Operating Example in Output Compare Mode

22.4 Notes on Timer RE

22.4.1 Reset

A reset input does not reset the timer RE data registers that store data of seconds, minutes, hours, and days of the week. This requires the initial setting of all registers after power on.

22.4.2 Starting and Stopping Count

Timer RE has the TSTART bit for instructing the count to start or stop, and the TCSTF bit, which indicates count start or stop. Bits TSTART and TCSTF are in the TRECR1 register.
When the TSTART bit is set to 1 (count starts), timer RE starts counting and the TCSTF bit is set to 1 (count starts). It takes up to two cycles of the count source until the TCSTF bit is set to 1 after setting the TSTART bit to 1. During this time, do not access registers associated with timer RE (1) other than the TCSTF bit.
Similarly, when the TSTART bit is set to 0 (count stops), timer RE stops counting and the TCSTF bit is set to 0 (count stops). It takes the time for up to two cycles of the count source until the TCSTF bit is set to 0 after setting the TSTART bit to 0. During this time, do not access registers associated with timer RE other than the TCSTF bit.

Note:
1. Registers associated with timer RE:
   TRESEC, TREMIN, TREHR, TREWK, TRECR1, TRECR2, and TRECSR

22.4.3 Register Setting

Write to the following registers or bits while timer RE is stopped.

- Registers TRESEC, TREMIN, TREHR, TREWK, and TRECR2
- Bits H12_H24, PM, and INT in the TRECR1 register
- Bits RCS0 to RCS3 in the TRECSR register

Timer RE is stopped while bits TSTART and TCSTF in the TRECR1 register are set to 0 (timer RE stopped).

Set all above-mentioned registers and bits (immediately before timer RE count starts) before setting the TRECR2 register.
Figure 22.6 shows a Setting Example in Real-Time Clock Mode.

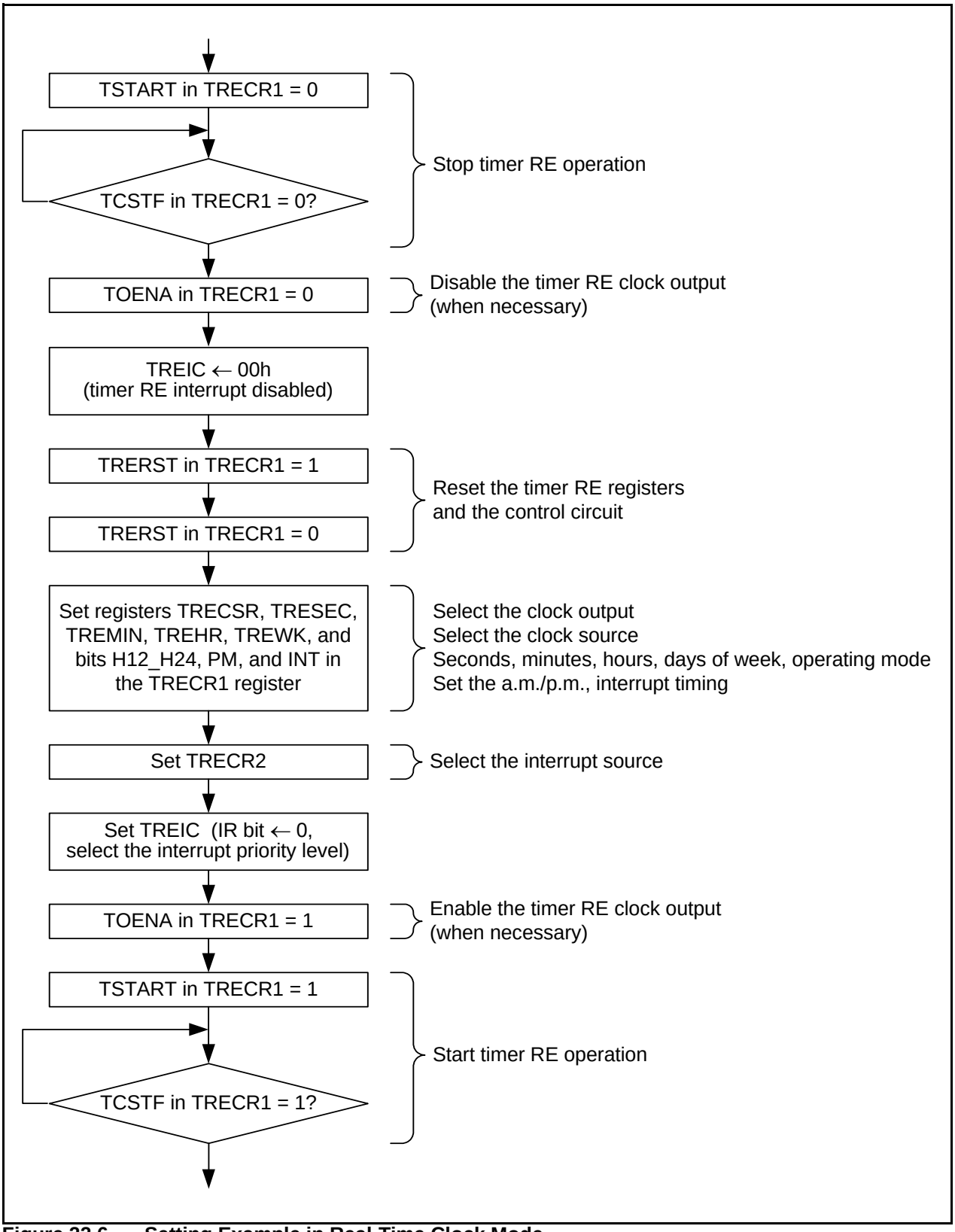


Figure 22.6 Setting Example in Real-Time Clock Mode

22.4.4 Time Reading Procedure in Real-Time Clock Mode

In real-time clock mode, read registers TRESEC, TREMIN, TREHR, and TREWK when time data is updated and read the PM bit in the TRECR1 register when the BSY bit is set to 0 (data is not being updated).
When reading several registers, an incorrect time will be read if data is updated before another register is read after reading any register.
In order to prevent this, use the reading procedure shown below.

- Using an interrupt
  Read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register in the timer RE interrupt routine.

- Monitoring with a program 1
  Monitor the IR bit in the TREIC register with a program and read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register after the IR bit in the TREIC register is set to 1 (timer RE interrupt request generated).

- Monitoring with a program 2

(1) Monitor the BSY bit.
(2) Monitor until the BSY bit is set to 0 after the BSY bit is set to 1 (approximately 62.5 ms while the BSY bit is set to 1).
(3) Read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register after the BSY bit is set to 0.

- Using read results if they are the same value twice

(1) Read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register.
(2) Read the same register as (1) and compare the contents.
(3) Recognize as the correct value if the contents match. If the contents do not match, repeat until the read contents match with the previous contents.

Also, when reading several registers, read them as continuously as possible.

23. Timer RG

Timer RG is a 16-bit timer with two I/O pins.

23.1 Introduction

Timer RG uses either f1 or fOCO40M as its operating clock. Table 23.1 lists the Timer RG Operating Clocks.

Table 23.1 Timer RG Operating Clocks

Condition	Timer RG Operating Clock
The count source is f1, f2, f4, f8, f32, TRGCLKA input, or TRGCLKB input. (Bits TCK2 toTCK0 in the TRGCR register are set to 000b to 101b, and 111b.)	f1
The count source is fOCO40M. (Bits TCK2 toTCK0 in the TRGCR register are set to 110b.)	fOCO40M

Figure 23.1 shows the Timer RG Block Diagram, and Table 23.2 lists the Timer RG Pin Configuration.

Timer RG supports the following three modes:
- Timer mode
  - Input capture function: Count at the rising edge, falling edge, or both rising and falling edges
  - Output compare function: Low-level output, high-level output, or toggle output

- PWM mode: PWM output available with any duty
- Phase counting mode: Automatic measurement available for the counts of the two-phase encoder

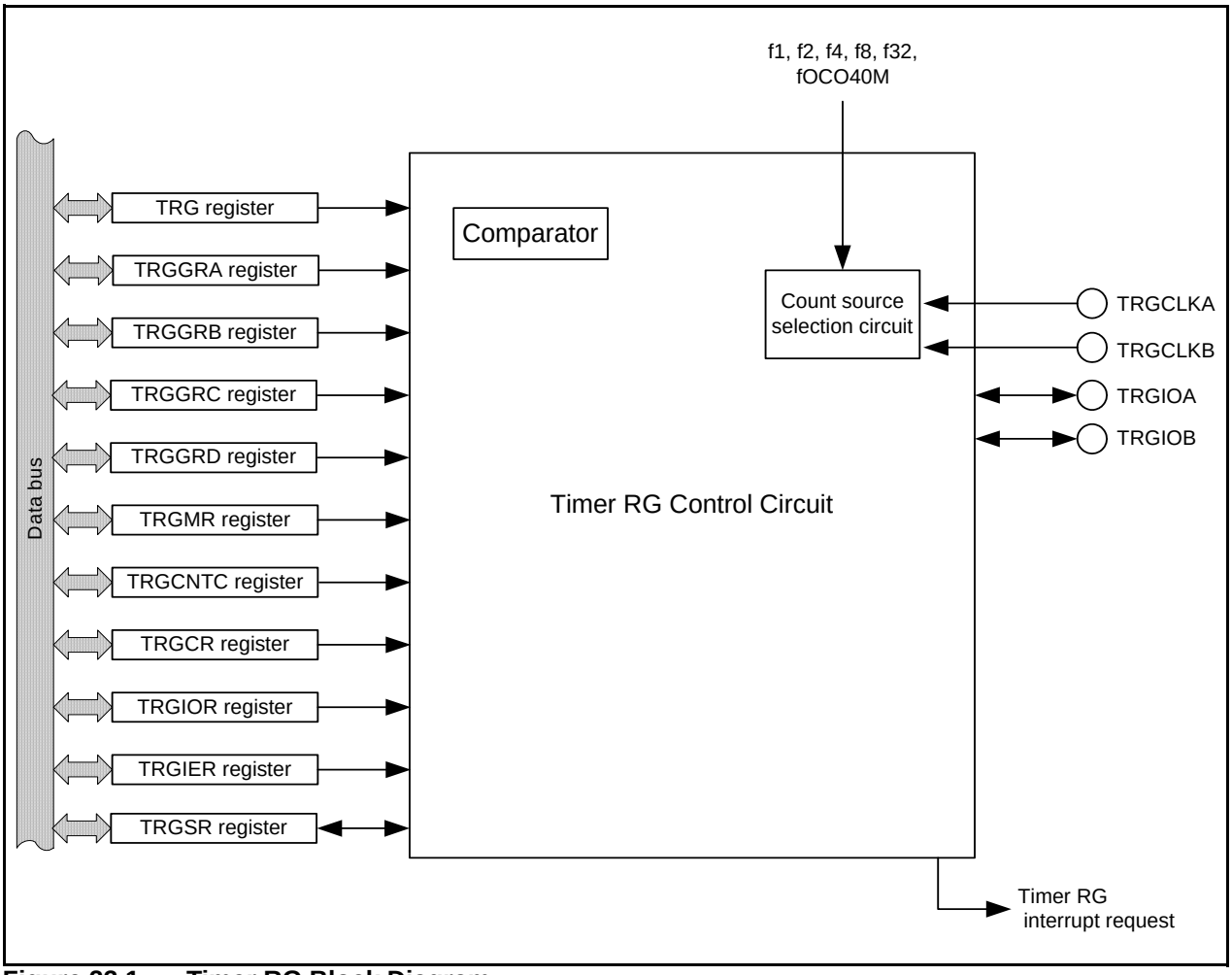


Figure 23.1 Timer RG Block Diagram

Table 23.2 Timer RG Pin Configuration

Pin Name	Assigned Pin	I/O	Function
TRGCLKA	P13_5	Input	• In phase counting mode A-phase input • In other than phase counting mode External clock A input
TRGCLKB	P13_7	Input	• In phase counting mode B-phase input • In other than phase counting mode External clock B input
TRGIOA	P13_4	I/O	• In timer mode (output compare function) TRGGRA output-compare output • In timer mode (input capture function) TRGGRA input-capture input • In PWM mode PWM output
TRGIOB	P13_6	I/O	• In timer mode (output compare function) TRGGRB output-compare output • In timer mode (input capture function) TRGGRB input-capture input

23.2 Registers

23.2.1 Timer RG Mode Register (TRGMR)

Address 0170h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TSTART	—	DFCK1	DFCK0	DFB	DFA	MDF	PWM
After Reset	0	1	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PWM	PWM mode select bit	0: Timer Mode 1: PWM mode	R/W
b1	MDF	Phase counting mode select bit	0: Increment 1: Phase counting mode	R/W
b2	DFA	Digital filer function select bit for TRGIOA pin	0: Digital filter function not used 1: Digital filter function used	R/W
b3	DFB	Digital filer function select bit for TRGIOB pin	0: Digital filter function not used 1: Digital filter function used	R/W
b4	DFCK0	Digital filter function clock select bit	b5 b4 0 0: f32 0 1: f8 1 0: f1 1 1: Clock selected by bits TCK0 to TCK2 in TRGCR register	R/W
b5	DFCK1			R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b7	TSTART	TRG count start bit	0: Count stops 1: Count starts	R/W

MDF Bit (Phase Counting Mode Select Bit)

When the MDF bit is set to 0, the counter counts the count source set by bits TCK0 to TCK2 in the TRGCR register.
When the MDF bit is set to 1, the counter counts the phase of input signals from the TRGCLKj pin (j = A or B) as listed in **Table 23.12 Increment and Decrement Conditions for TRG Register**.

23.2.2 Timer RG Count Control Register (TRGCNTC)

Address 0171h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CNTEN7	CNTEN6	CNTEN5	CNTEN4	CNTEN3	CNTEN2	CNTEN1	CNTEN0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CNTEN0	Counter enable bit 0	0: Disabled 1: Decrement When TRGCLKA input is high and at the rising edge of TRGCLKB input	R/W
b1	CNTEN1	Counter enable bit 1	0: Disabled 1: Decrement When TRGCLKB input is low and at the rising edge of TRGCLKA input	R/W
b2	CNTEN2	Counter enable bit 2	0: Disabled 1: Decrement When TRGCLKA input is low and at the falling edge of TRGCLKB input	R/W
b3	CNTEN3	Counter enable bit 3	0: Disabled 1: Decrement When TRGCLKB input is high and at the falling edge of TRGCLKA input	R/W
b4	CNTEN4	Counter enable bit 4	0: Disabled 1: Increment When TRGCLKB input is low and at the falling edge of TRGCLKA input	R/W
b5	CNTEN5	Counter enable bit 5	0: Disabled 1: Increment When TRGCLKA input is high and at the falling edge of TRGCLKB input	R/W
b6	CNTEN6	Counter enable bit 6	0: Disabled 1: Increment When TRGCLKB input is high and at the rising edge of TRGCLKA input	R/W
b7	CNTEN7	Counter enable bit 7	0: Disabled 1: Increment When TRGCLKA input is low and at the rising edge of TRGCLKB input	R/W

The TRGCNTC register is used in phase counting mode. This register sets its count conditions.

23.2.3 Timer RG Control Register (TRGCR)

Address 0172h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	CCLR1	CCLR0	CKEG1	CKEG0	TCK2	TCK1	TCK0
After Reset	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TCK0	Count source select bit (1)	b2 b1 b0 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRGCLKA input 1 1 0: fOCO40M 1 1 1: TRGCLKB input	R/W
b1	TCK1			R/W
b2	TCK2			R/W
b3	CKEG0	External clock active edge select bit (1)	b4 b3 0 0: Count at the rising edge 0 1: Count at the falling edge 1 0: Count at both the rising/falling edges 1 1: Do not set.	R/W
b4	CKEG1			R/W
b5	CCLR0	TRG register clear source select bit	b6 b5 0 0: Clear disabled 0 1: TRG register cleared by input capture or compare match with TRGGRA register 1 0: TRG register cleared by input capture or compare match with TRGGRB register 1 1: Do not set.	R/W
b6	CCLR1			R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Note:
1. In phase counting mode, the settings of bits TCK0 to TCK2 and bits CKEG0 and CKEG1 are disabled and the operation of phase counting mode has priority.

23.2.4 Timer RG Interrupt Enable Register (TRGIER)

Address 0173h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	OVIE	UDIE	IMIEB	IMIEA
After Reset	1	1	1	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input-capture/compare-match interrupt enable bit A	0: Interrupt by IMFA bit disabled 1: Interrupt by IMFA bit enabled	R/W
b1	IMIEB	Input-capture/compare-match interrupt enable bit B	0: Interrupt by IMFB bit disabled 1: Interrupt by IMFB bit enabled	R/W
b2	UDIE	Underflow interrupt enable bit	0: Interrupt by UDF bit disabled 1: Interrupt by UDF bit enabled	R/W
b3	OVIE	Overflow interrupt enable bit	0: Interrupt by OVF bit disabled 1: Interrupt by OVF bit enabled	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	—			

23.2.5 Timer RG Status Register (TRGSR)

Address 0174h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	DIRF	OVF	UDF	IMFB	IMFA
After Reset	1	1	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input-capture/compare-match flag A	[Condition for setting to 0] Write 0 after reading. (1)	R/W
b1	IMFB	Input-capture/compare-match flag B	[Condition for setting to 1] Refer to **Table 23.3 Conditions for Setting Bit of Each Flag to 1**.	R/W
b2	UDF	Underflow flag		R/W
b3	OVF	Overflow flag		R/W
b4	DIRF	Count direction flag	0: TRG register is decremented 1: TRG register is incremented	R
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b6	—			
b7	—			

Note:

1. The results of writing to these bits are as follows:
   - The bit is set to 0 when it is first read as 1 and then 0 is written to it.
   - The bit remains unchanged even if it is first read as 0 and then 0 is written to it because its previous value is retained. (The bit's value remains 1 even if it is set to 1 from 0 after being read as 0 and having 0 written to it because its previous value is retained.)
   - The bit's value remains unchanged if 1 is written to it.

Table 23.3 Conditions for Setting Bit of Each Flag to 1

Bit Symbol	Timer Mode		PWM Mode
	Input Capture Function	Output Compare Function	
IMFA	TRGIOA pin input edge (1)	When the values of registers TRG and TRGGRA match.	
IMFB	TRGIOB pin input edge (1)	When the values of registers TRG and TRGGRB match.	
UDF	When the TRG register underflows.		
OVF	When the TRG register overflows.		

Note:

1. Edge selected by bits IOj0 and IOj1 (j = A or B) in the TRGIOR register.

23.2.6 Timer RG I/O Control Register (TRGIOR)

Address 0175h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BUFB	IOB2	IOB1	IOB0	BUFA	IOA2	IOA1	IOA0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRGGRA control bit	Function varies depending on the operating mode (function).	R/W
b1	IOA1			R/W
b2	IOA2	TRGGRA mode select bit	0: Output compare function (1) 1: Input capture function (2)	R/W
b3	BUFA	TRGGRC register function select bit	0: Not used as the buffer register of the TRGGRA register 1: Used as the buffer register of the TRGGRA register	R/W
b4	IOB0	TRGGRB control bit	Function varies depending on the operating mode (function).	R/W
b5	IOB1			R/W
b6	IOB2	TRGGRB mode select bit	0: Output compare function (3) 1: Input capture function (4)	R/W
b7	BUFB	TRGGRD register function select bit	0: Not used as the buffer register of the TRGGRB register 1: Used as the buffer register of the TRGGRB register	R/W

Notes:
1. When the IOA2 bit is set to 0 (output compare function), the TRGGRA register functions as a compare match register. After a reset, the TRGIOA pin outputs a low-level signal until the first compare match occurs.
2. When the IOA2 bit is set to 1 (input capture function), the TRGGRA register functions as an input capture register.
3. When the IOB2 bit is set to 0 (output compare function), the TRGGRB register functions as a compare match register. After a reset, the TRGIOB pin outputs a low-level signal the until the first compare match occurs.
4. When the IOB2 bit is set to 1 (input capture function), the TRGGRB register functions as an input capture register.

23.2.7 Timer RG Counter (TRG)

Address 0177h to 0176h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	In phase counting mode, count operation is increment/decrement. In other modes, count operation is increment.	0000h to FFFFh	R/W

The TRG register is connected to the CPU via the internal 16-bit bus and should be always accessed in 16-bit units. This register operates incrementing and can also operate free-running, period counting, or external event counting. It can be cleared to 0000h by a compare match with the corresponding TRGGRA or TRGGRB register, or an input capture to the TRGGRA or TRGGRB register (count clear function).
When the TRGCR register overflows (FFFFh → 0000h), the OVF bit in the TRGSR register is set to 1.
When the TRGCR register underflows (0000h → FFFFh), the UDF bit in the TRGSR register is set to 1.

23.2.8 Timer RG General Register A, B, C, D (TRGGRA, TRGGRB, TRGGRC, TRGGRD)

Address 0179h to 0178h (TRGGRA), 017Bh to 017Ah (TRGGRB),
017Dh to 017Ch (TRGGRC), 017Fh to 017Eh (TRGGRD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b15 to b0	Function varies depending on the operating mode.	R/W

TRGGRA and TRGGRB are 16-bit readable/writable registers with both the output compare and input capture register functions. Switching between these functions is accomplished by means of a setting in the TRGIOR register.

When registers TRGGRA and TRGGRB are used as output compare registers, the values of registers TRGGRA and TRGGRB and the value of the TRG register are always compared. When their values match (compare match), bits IMFA and IMFB in the TRGSR register are set to 1. Compare match output can be selected by setting the TRGIOR register.

When registers TRGGRA and TRGGRB are used as input capture registers, the value of the TRG register is stored when an externally input capture signals is detected. Bits IMFA and IMFB in the TRGSR register are set to 1 at this time. The detection edge of input capture signals is selected by setting the TRGIOR register.
In PWM mode, the settings of the TRGIOR register are ignored.

The TRGGRC register can also be used as the buffer register of the TRGGRA register, and the TRGGRD register can be used as the buffer register of the TRGGRB register, respectively. These functions can be selected by setting bits BUFA and BUFB in the TRGIOR register.
For example, when the TRGGRA register is set as an output compare register and the TRGGRC register is set as the buffer register of the TRGGRA register, the value of the TRGGRC register is transferred to the TRGGRA register each time compare match A occurs.
When the TRGGRA register is set as an input capture register and the TRGGRC register is set as the buffer register of the TRGGRA register, the value of the TRG register is transferred to the TRGGRA register and the value of the TRGGRA register value is transferred to the TRGGRC register each time an input capture occurs.

Registers TRGGRA and TRGGRB are connected to the CPU via the internal 16-bit bus and should be accessed in 16-bit units. These registers are set as output compare registers (pin output disabled) after a reset.

23.2.9 Timer RG Pin Select Register (TRGPSR)

Address 0187h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRGCLKBSEL0	TRGCLKASEL0	TRGIOBSEL0	TRGIOASEL0	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	—			
b4	TRGIOASEL0	TRGIOA pin select bit	0: TRGIOA pin not used 1: TRGIOA pin used	R/W
b5	TRGIOBSEL0	TRGIOB pin select bit	0: TRGIOB pin not used 1: TRGIOB pin used	R/W
b6	TRGCLKASEL0	TRGCLKA pin select bit	0: TRGCLKA pin not used 1: TRGCLKA pin used	R/W
b7	TRGCLKBSEL0	TRGCLKB pin select bit	0: TRGCLKB pin not used 1: TRGCLKB pin used	R/W

The TRGPSR register selects which pin is assigned as the timer RG input/output. To use the I/O pins for timer RG, set this register.
Set the TRGPSR register before setting the timer RG associated registers. Also, do not change the setting value of this register during timer RG operation.

23.3 Common Items for Multiple Modes

23.3.1 Count Sources

Table 23.4 lists the Count Source Selection, and Figure 23.2 shows the Count Source Block Diagram.
When phase counting mode is selected, the settings of bits TCK0 to TCK2 and bits CKEG0 and CKEG1 in the TRGCR register are disabled.

Table 23.4 Count Source Selection

Count Source	Selection Method
f1 f2, f4, f8, f32	The count source is selected by bits TCK0 to TCK2 in the TRGCR register.
fOCO40M	- The FRA00 bit in the FRA0 register is set to 1 (high-speed on-chip oscillator on). - Bits TCK2 to TCK0 in the TRGCR register are set to 110b (fOCO40M).
External signal input to TRGCLKA or TRGCLKB pin	- Bits TCK2 to TCK0 in the TRGCR register are set to 101b (TRGCLKA input) or 111b (TRGCLKB input). - The active edge is selected by bits CKEG0 and CKEG1 in the TRGCR register. - The corresponding bit in the direction register is set to 0 (input mode).

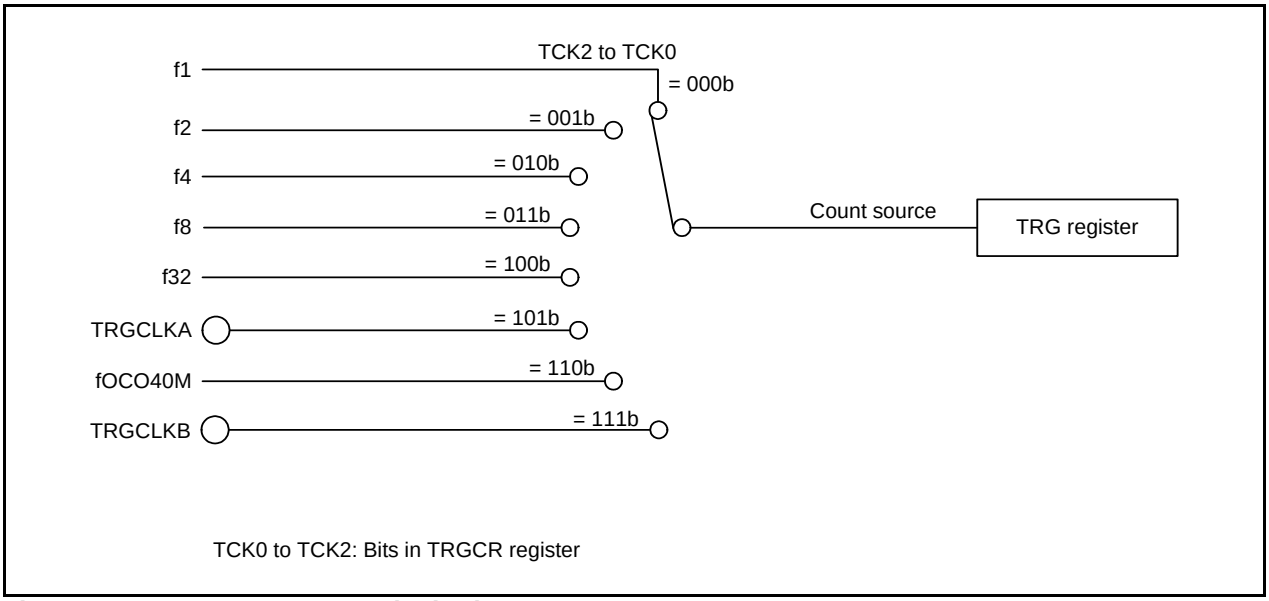


Figure 23.2 Count Source Block Diagram

The pulse width of an external clock input to the TRGCLKj pin (j =A or B) should be set to three cycles or more of the timer RG operating clock. (See **Table 23.1 Timer RG Operating Clocks.**)

23.3.2 Buffer Operation

The BUFA or BUFB bit in the TRGIOR register can be used to select the TRGGRC or TRGGRD register as the buffer register of the TRGGRA or TRGGRB register.

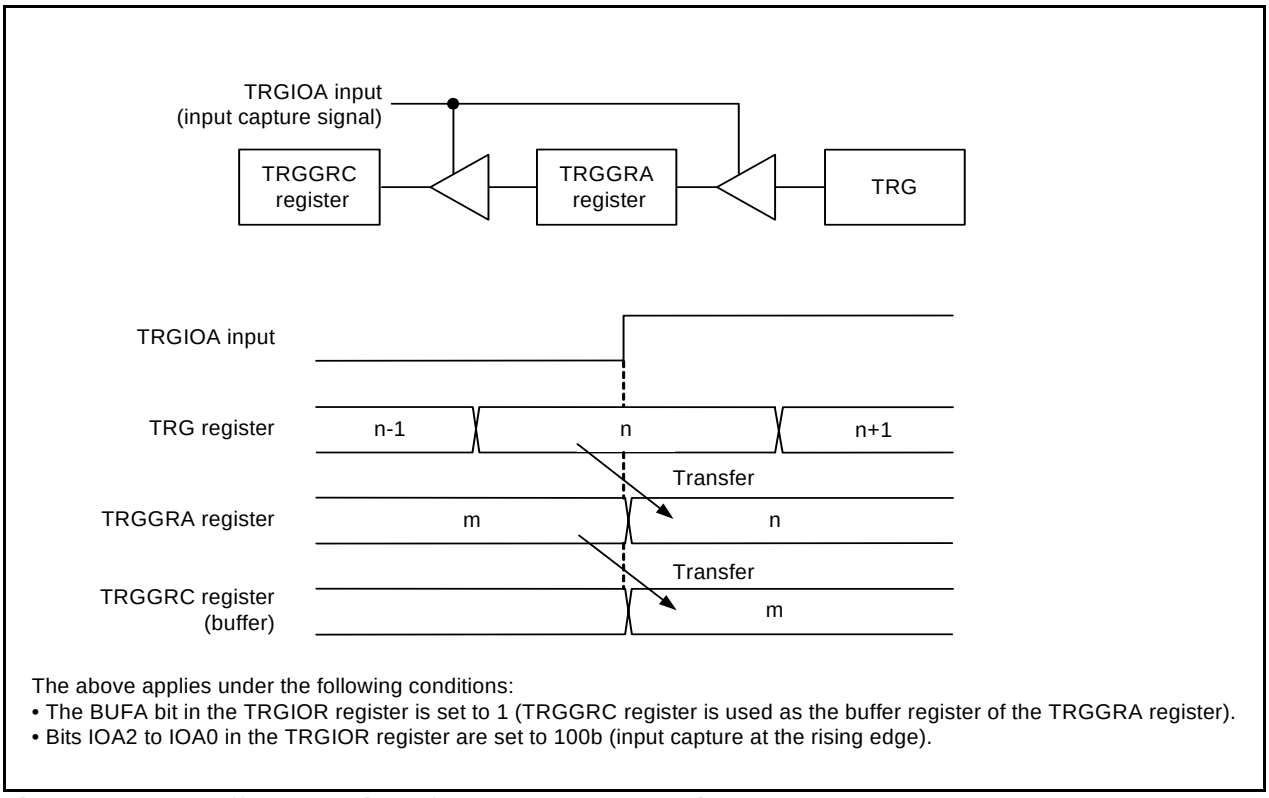
- Buffer register of TRGGRA register: TRGGRC register
- Buffer register of TRGGRB register: TRGGRD register

Buffer operation differs depending on the mode.

Table 23.5 lists the Buffer Operation in Each Mode, Figure 23.3 shows the Buffer Operation of Input Capture Function, and Figure 23.4 shows the Buffer Operation of Output Compare Function.

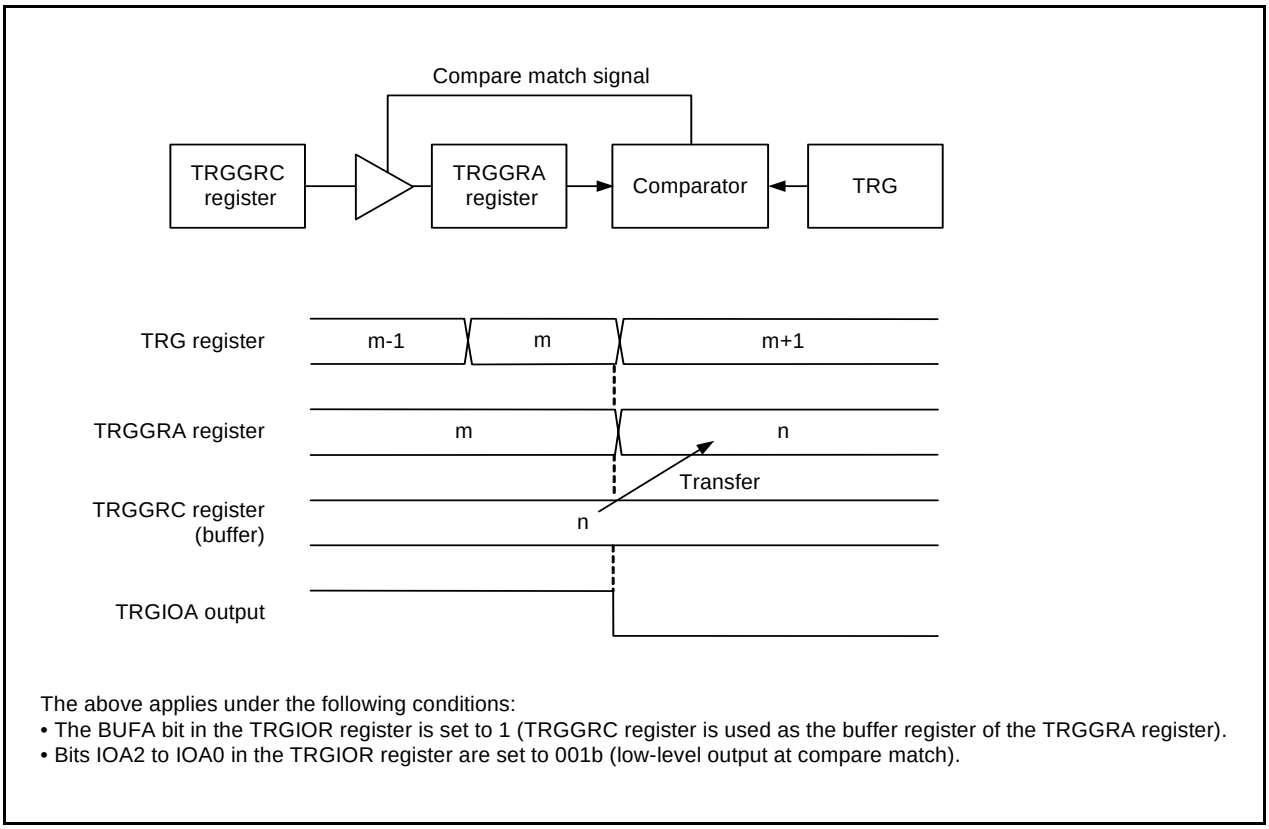
Table 23.5 Buffer Operation in Each Mode

Function, Mode	Transfer Timing	Transfer Destination Register
Input capture function	Input capture signal input	The content of the TRGGRA (TRGGRB) register is transferred to the buffer register.
Output compare function PWM mode	Compare match between the TRG register and the TRGGRA (TRGGRB) register	The content of the buffer register is transferred to the TRGGRA (TRGGRB) register.



The above applies under the following conditions:
- The BUFA bit in the TRGIOR register is set to 1 (TRGGRC register is used as the buffer register of the TRGGRA register).
- Bits IOA2 to IOA0 in the TRGIOR register are set to 100b (input capture at the rising edge).

Figure 23.3 Buffer Operation of Input Capture Function



The above applies under the following conditions:
- The BUFA bit in the TRGIOR register is set to 1 (TRGGRC register is used as the buffer register of the TRGGRA register).
- Bits IOA2 to IOA0 in the TRGIOR register are set to 001b (low-level output at compare match).

Figure 23.4 Buffer Operation of Output Compare Function

23.3.3 Digital Filter

The input to TRGIOj (j = A or B) is sampled and the level is determined when three matches occur. The digital filter function and sampling clock are selected by using the TRGMR register.
Figure 23.5 shows a Block Diagram of Digital Filter.

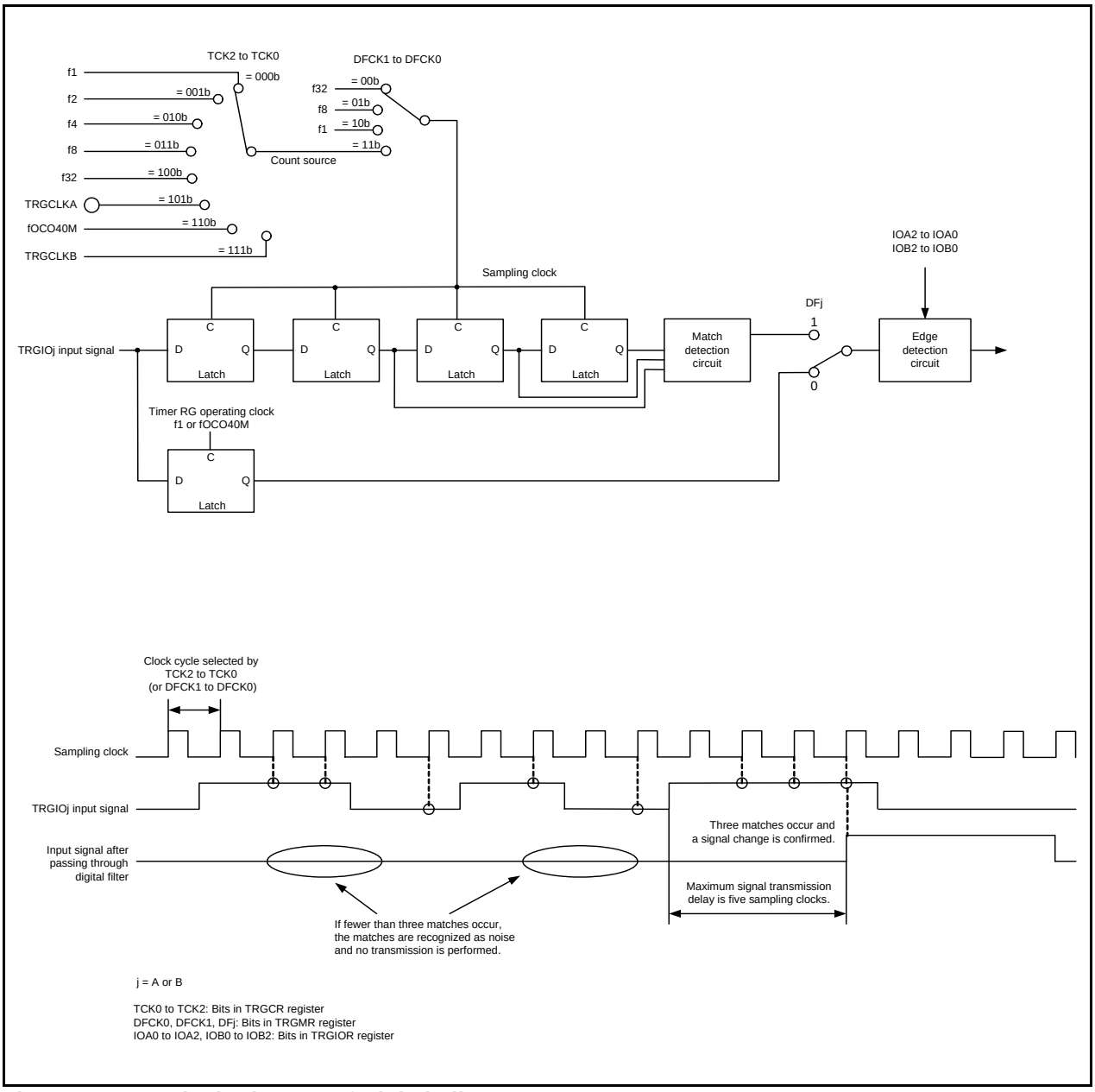


Figure 23.5 Block Diagram of Digital Filter

23.4 Timer Mode (Input Capture Function)

The value of the TRG register can be transferred to the TRGGRA or TRGGRB register when the input edge of the input capture/output compare pin (TRGIOA or TRGIOB) is detected. The detection edge can be selected from the rising edge, falling edge, or both edges.
The input capture function can be used for measuring pulse widths and periods.
Table 23.6 lists the Input Capture Function Specifications.

Table 23.6 Input Capture Function Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, fOCO40M External signal input to the TRGCLKj pin (active edge selectable by a program)
Count operation	Increment
Count period	When bits CCLR1 to CCLR0 in the TRGCR register are set to 00b (free-running operation) 1/fk × 65,536 fk: Frequency of count source
Count start condition	1 (count starts) is written to the TSTART bit in the TRGMR register.
Count stop condition	0 (count stops) is written to the TSTART bit in the TRGMR register.
Interrupt request generation timing	• Input capture (active edge of the TRGIOj input) • TRG register overflow
TRGIOA/TRGIOB pins function	Programmable I/O port or input-capture input (selectable for each individual pin)
TRGCLKA/TRGCLKB pins function	Programmable I/O port or external clock input
Read from timer	The count value can be read by reading the TRG register.
Write to timer	The TRG register can be written to.
Selectable functions	• Input-capture input pin selection Either one or both of pins TRGIOA and TRGIOB • Active edge selection for input-capture input Rising edge, falling edge, or both rising and falling edges • Timing for setting the TRG register to 0000h Overflow or input capture • Buffer operation (Refer to **23.3.2 Buffer Operation**.) • Digital filter (Refer to **23.3.3 Digital Filter**.)

j = A or B

23.4.1 Timer RG I/O Control Register (TRGIOR) in Timer Mode (Input Capture Function)

Address 0175h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BUFB	IOB2	IOB1	IOB0	BUFA	IOA2	IOA1	IOA0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRGGRA control bit	b1 b0 0 0: Input capture to TRGGRA at the rising edge 0 1: Input capture to TRGGRA at the falling edge 1 0: Input capture to TRGGRA at both edges 1 1: Do not set.	R/W
b1	IOA1			R/W
b2	IOA2	TRGGRA mode select bit (1)	Set to 1 (input capture) for the input capture function.	R/W
b3	BUFA	TRGGRC register function select bit	0: Not used as the buffer register of the TRGGRA register 1: Used as the buffer register of the TRGGRA register	R/W
b4	IOB0	TRGGRB control bit	b5 b4 0 0: Input capture to TRGGRB at the rising edge 0 1: Input capture to TRGGRB at the falling edge 1 0: Input capture to TRGGRB at both edges 1 1: Do not set.	R/W
b5	IOB1			R/W
b6	IOB2	TRGGRB mode select bit (2)	Set to 1 (input capture) for the input capture function.	R/W
b7	BUFB	TRGGRD register function select bit	0: Not used as the buffer register of the TRGGRB register 1: Used as the buffer register of the TRGGRB register	R/W

Notes:
1. When the IOA2 bit is set to 1 (input capture function), the TRGGRA register functions as an input capture register.
2. When the IOB2 bit is set to 1 (input capture function), the TRGGRB register functions as an input capture register.

23.4.2 Procedure Example for Setting Input Capture Operation

Figure 23.6 shows a Procedure Example for Setting Input Capture Operation.

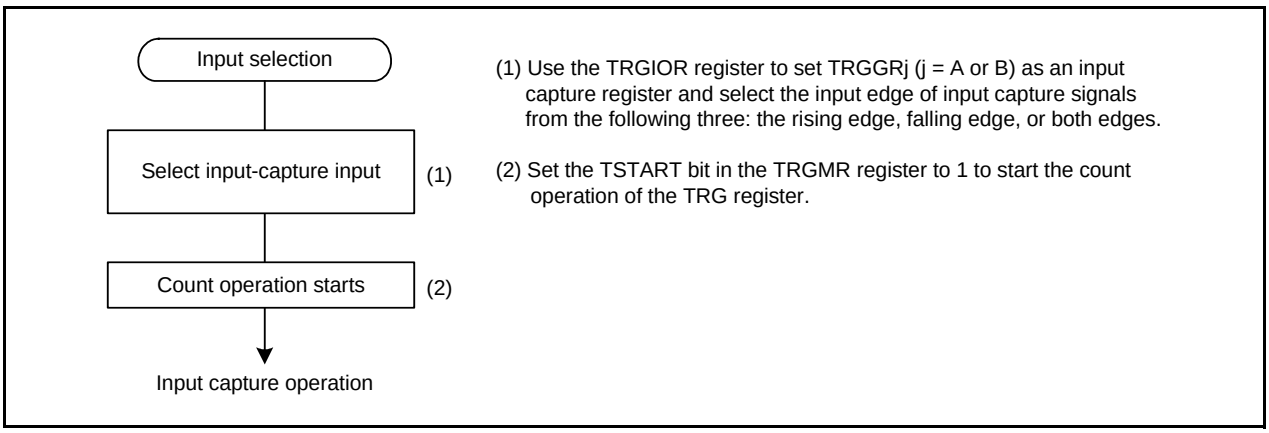


Figure 23.6 Procedure Example for Setting Input Capture Operation

23.4.3 Input Capture Signal Timing

The rising edge, falling edge, or both edges can be selected for input-capture input by setting the TRGIOR register.

Figure 23.7 shows the Input-Capture Input Signal Timing.

The pulse width of input-capture input signals should be 1.5 f1 or more for a single edge and 2.5 f1 or more for both edges.

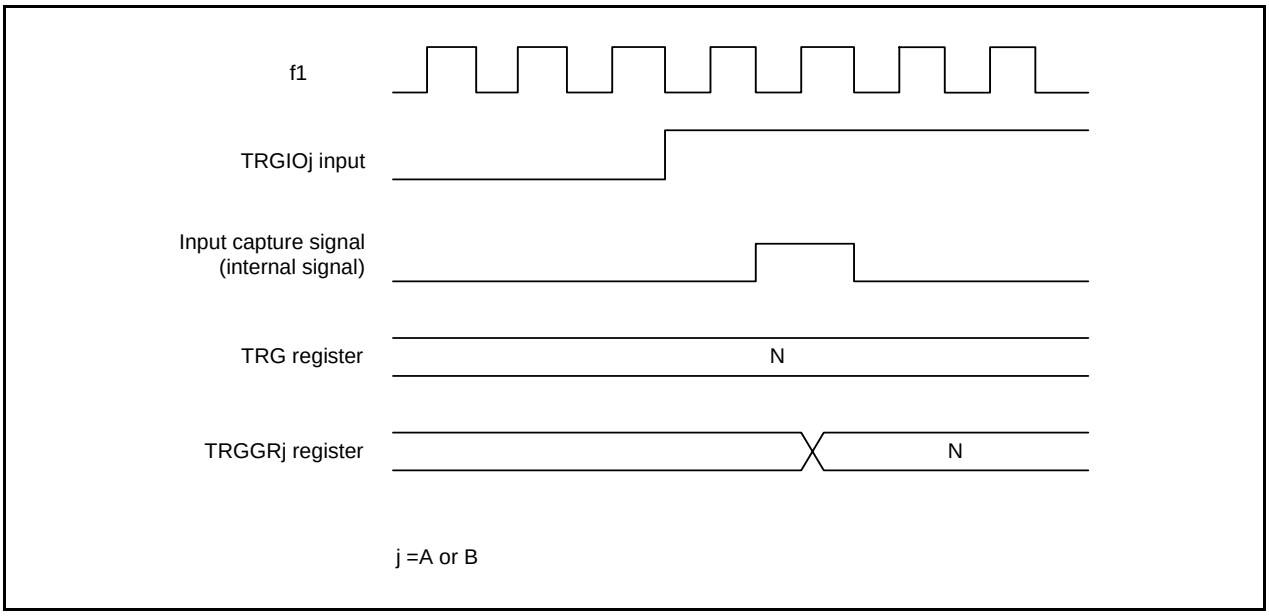


Figure 23.7 Input-Capture Input Signal Timing

23.4.4 Operating Example

Figure 23.8 shows an Operating Example of Input Capture.
This example applies when both the rising and falling edges are selected as the input-capture input edge for the TRGIOA pin, the falling edge is selected as the input-capture input edge for the TRGIOB pin, and the TRG register is set to be cleared by the input capture to the TRGGRB register.

(1) Use the TRGIOR register to set registers TRGGRA and TRGGRB as input capture registers and select the input edge of input capture signals from the following three: the rising edge, falling edge, or both edges.
(2) Set the TSTART bit in TRGMR to 1 and start the count operation of the TRG register.

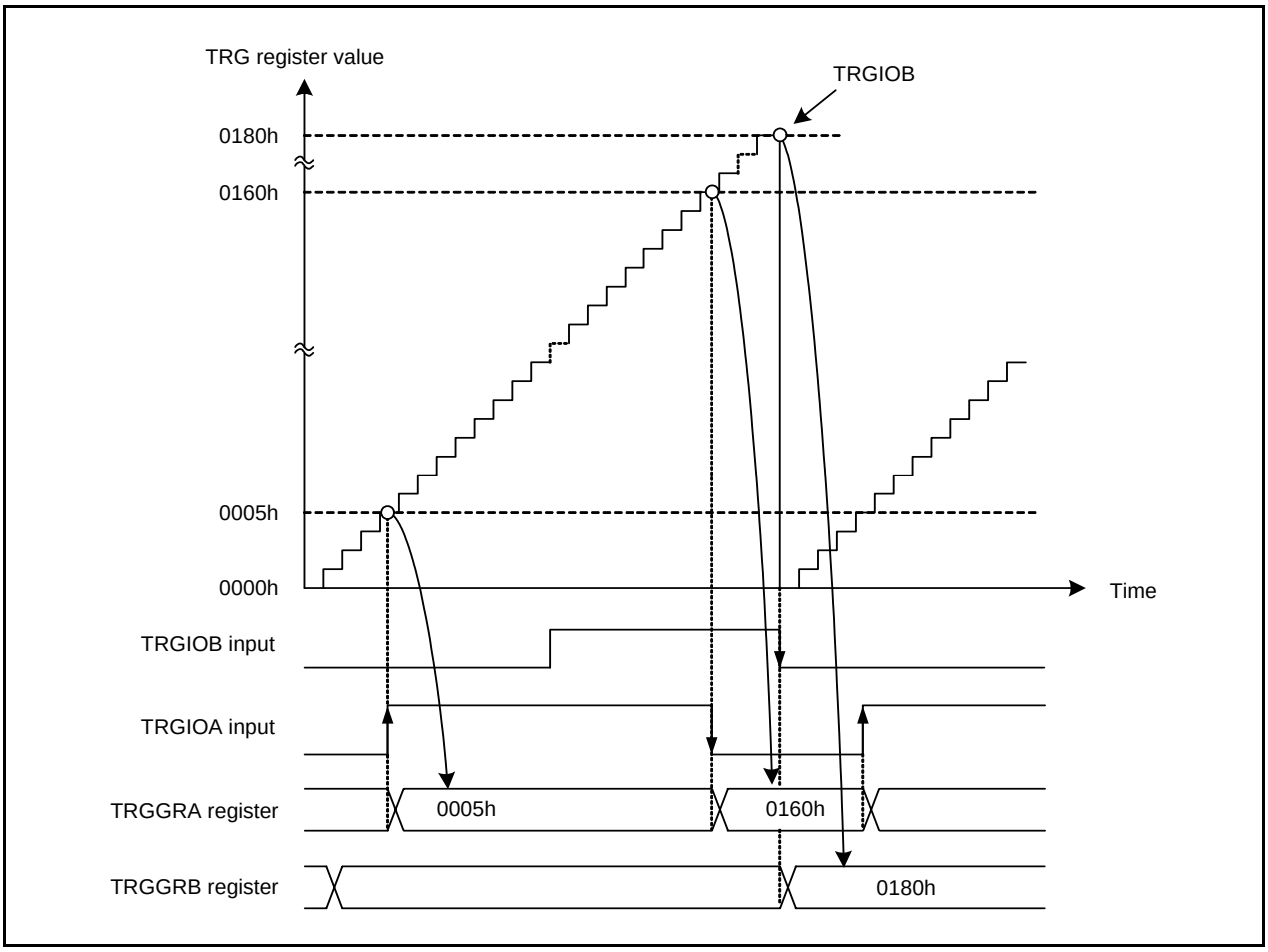


Figure 23.8 Operating Example of Input Capture

23.5 Timer Mode (Output Compare Function)

This mode (output compare function) detects when the contents of the TRG register and the TRGGRA or TRGGRB register match (compare match). When a match occurs, a signal is output from the TRGIOA or TRGIOB pin at a given level.
Table 23.7 lists the Output Compare Function Specifications.

Table 23.7 Output Compare Function Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, fOCO40M External signal input to the TRGCLKj pin (active edge selectable by a program)
Count operation	Increment
Count periods	• When bits CCLR1 to CCLR0 in the TRGCR register are set to 00b (free-running operation) 1/fk × 65,536 fk: Frequency of count source • When bits CCLR1 to CCLR01 in the TRGCR register are set to 01b or 10b (TRG is set to 0000h by a compare match with TRGGRj) 1/fk × (n+1) n: Value set in TRGGRj register
Waveform output timing	Compare match
Count start condition	1 (count starts) is written to the TSTART bit in the TRGMR register.
Count stop condition	0 (count stops) is written to the TSTART bit in the TRGMR register.
Interrupt request generation timing	• Compare match (the contents of the TRG register and the TRGGRj register match) • TRG register overflow
TRGIOA/TRGIOB pins function	Programmable I/O port or output-compare output (selectable for each individual pin)
TRGCLKA/TRGCLKB pins function	Programmable I/O port or external clock input
Read from timer	The count value can be read by reading the TRG register.
Write to timer	The TRG register can be written to.
Selectable functions	• Output-compare output pin selection Either one or both of pins TRGIOA and TRGIOB • Output level selection at compare match Low-level output, high-level output, or inverted output level • Timing for setting the TRG register to 0000h Overflow or compare match with the TRGGRj register • Buffer operation (Refer to **23.3.2 Buffer Operation**.)

j = A or B

23.5.1 Timer RG I/O Control Register (TRGIOR) in Timer Mode (Output Compare Function)

Address 0175h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BUFB	IOB2	IOB1	IOB0	BUFA	IOA2	IOA1	IOA0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRGGRA control bit	b1 b0 0 0: Pin output by compare match is disabled (TRGIOA pin functions as a programmable I/O port) 0 1: Low-level output at compare match with TRGGRA 1 0: High-level output at compare match with TRGGRA 1 1: Toggle output at compare match with TRGGRA	R/W
b1	IOA1			R/W
b2	IOA2	TRGGRA mode select bit (1)	Set to 0 (output compare) for the output compare function.	R/W
b3	BUFA	TRGGRC register function select bit	0: Not used as the buffer register of the TRGGRA register 1: Used as the buffer register of the TRGGRA register	R/W
b4	IOB0	TRGGRB control bit	b5 b4 0 0: Pin output by compare match is disabled (TRGIOB pin functions as a programmable I/O port) 0 1: Low-level output at compare match with TRGGRB 1 0: High-level output at compare match with TRGGRB 1 1: Toggle output at compare match with TRGGRB	R/W
b5	IOB1			R/W
b6	IOB2	TRGGRB mode select bit (2)	Set to 0 (output compare) for the output compare function.	R/W
b7	BUFB	TRGGRD register function select bit	0: Not used as the buffer register of the TRGGRB register 1: Used as the buffer register of the TRGGRB register	R/W

Notes:
1. When the IOA2 bit is set to 0 (output compare function), the TRGGRA register functions as a compare match register. After a reset, the TRGIOA pin outputs as follows until the first compare match occurs.
   IOA1 to IOA0 = 01b: High-level output
   10b: Low-level output
   11b: Low-level output
2. When the IOB2 bit is set to 0 (output compare function), the TRGGRB register functions as a compare match register. After a reset, the TRGIOB pin outputs as follows until the first compare match occurs.
   IOB1 to IOB0 = 01b: High-level output
   10b: Low-level output
   11b: Low-level output

23.5.2 Procedure Example for Setting Waveform Output by Compare Match

Figure 23.9 shows an Operating Example of Waveform Output by Compare Match.

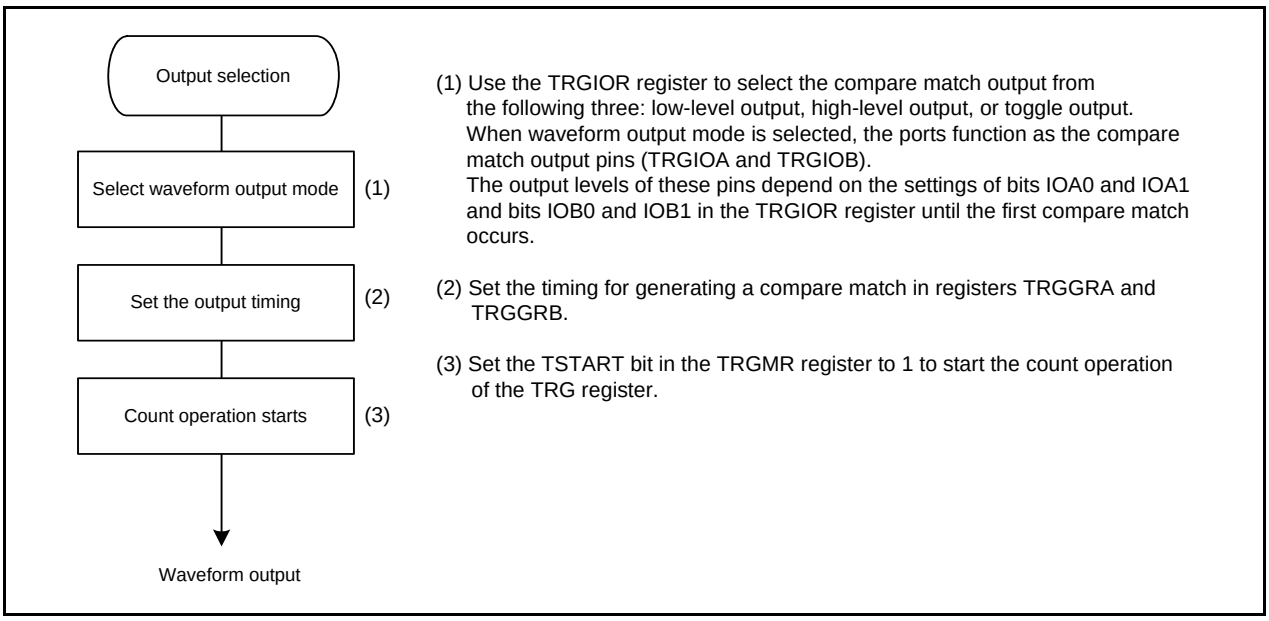


Figure 23.9 Operating Example of Waveform Output by Compare Match

23.5.3 Output-Compare Output Timing

A compare match signal is generated at the last state when the TRG register and the TRGGRA or TRGGRB register match (according to the timing for updating the count value that the TRG register matches). When a compare match signal is generated, the output value set by the TRGIOR register is output to the output-compare output pin (TRGIOA or TRGIOB). After the TRG register and the TRGGRA or TRGGRB register match, no compare match signal is generated until the TRG input clock is generated.
Figure 23.10 shows the Output-Compare Output Timing.

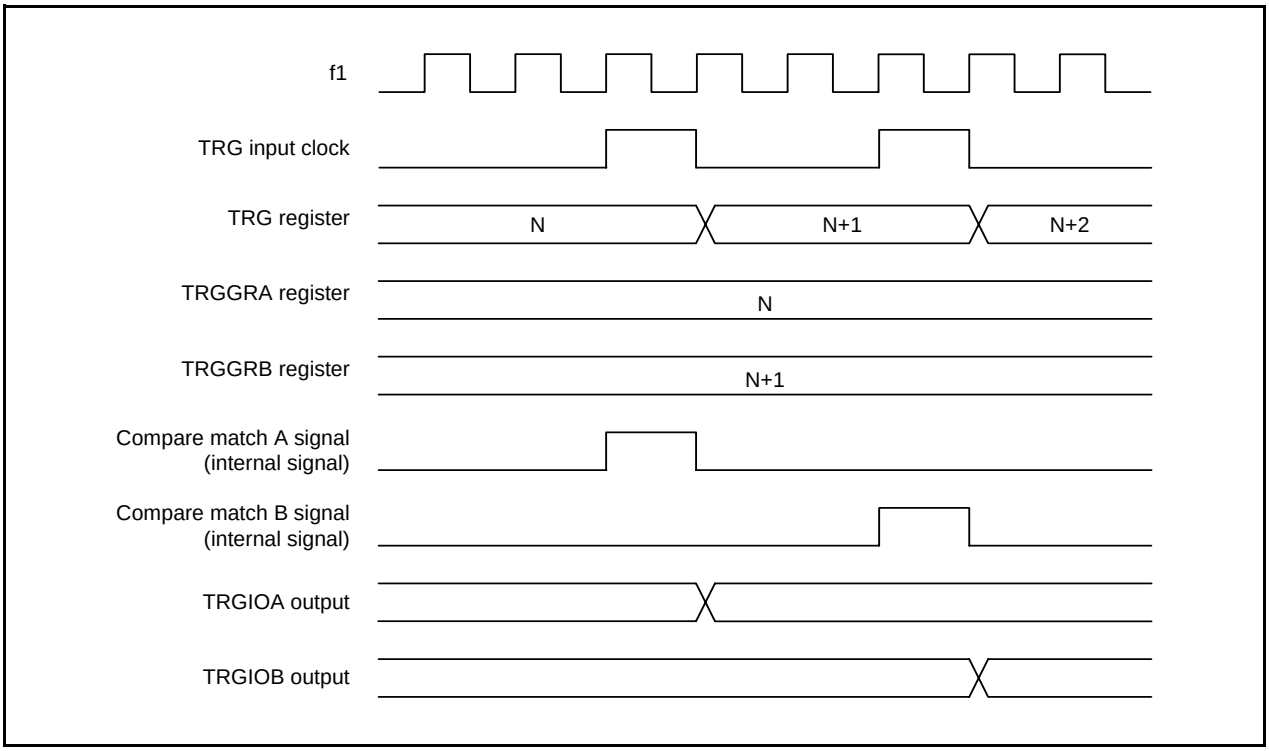


Figure 23.10 Output-Compare Output Timing

23.5.4 Operating Example

Figure 23.11 shows an Operating Example of Low-Level Output and High-Level Output.
This example applies when the TRG register is set for free-running operation, low-level output at compare match A is selected, and high-level output at compare match B is selected. When the selected level and the pin level match, the pin level does not change.

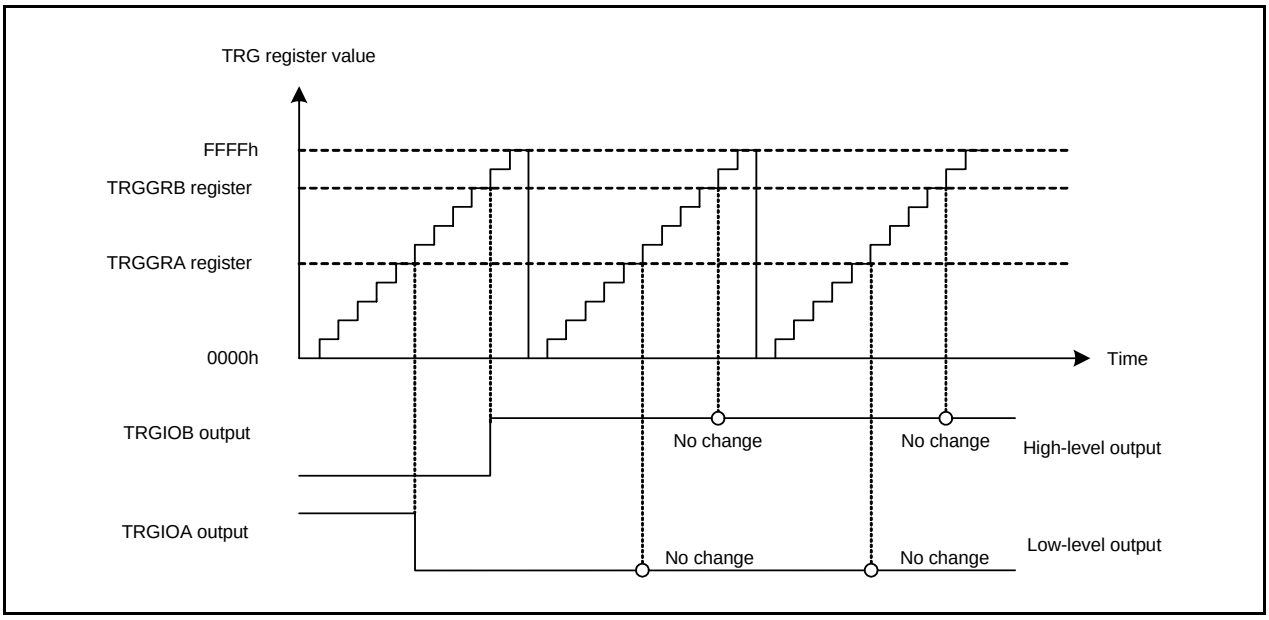


Figure 23.11 Operating Example of Low-Level Output and High-Level Output

Figure 23.12 shows an Operating Example of Toggle Output.
This example applies when the TRG register is set for period counting operation (counter clear by compare match B), and toggle output at both compare match A and B is selected.
Use the TRGIOR register to select the compare match output from the following three: low-level output, high-level output, or toggle output. When waveform output mode is selected, the ports function as the compare match output pins (TRGIOA and TRGIOB).
Set the timing for generating a compare match in registers TRGGRA and TRGGRB.
Set the TSTART bit in the TRGMR register to 1 to start the count operation of the TRG register.

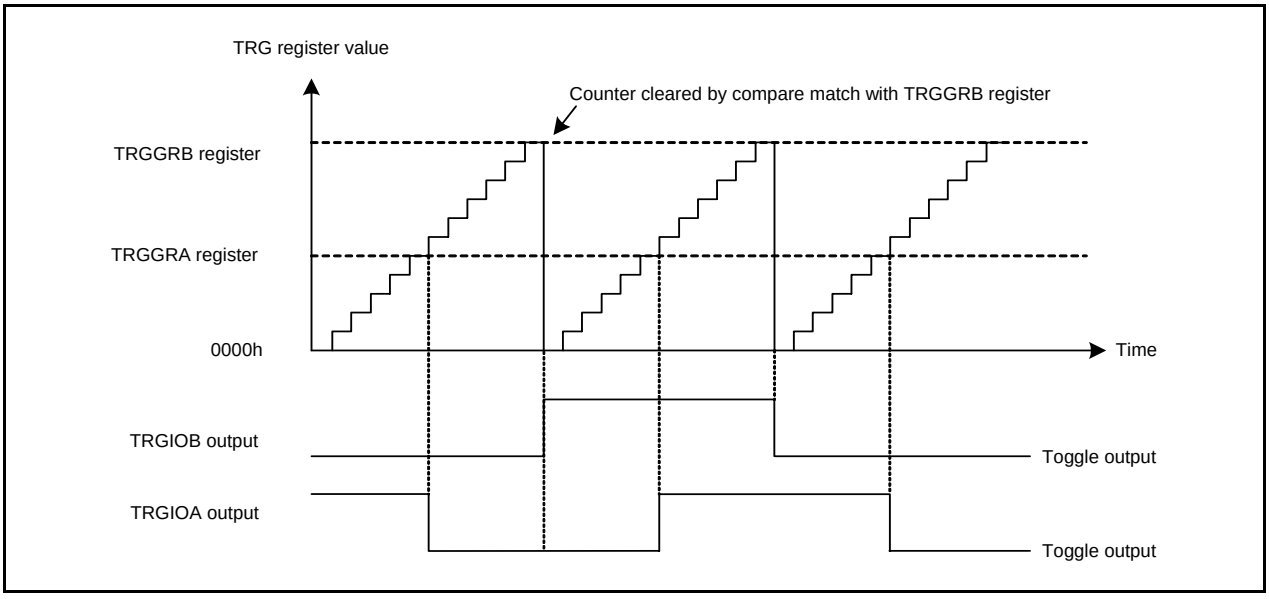


Figure 23.12 Operating Example of Toggle Output

23.6 PWM Mode

In PWM mode, registers TRGGRA and TRGGRB are used as a pair and a PWM waveform is output from the TRGIOA output pin. The output setting in the TRGIOR register is invalid for the pins set to PWM mode. Set the high-level output timing for PWM waveforms in the TRGGRA register and the low-level output timing for PWM waveforms in the TRGGRB register.
By selecting a compare match with either the TRGGRA or TRGGRB register as the counter clear source for the TRG register, a PWM waveform with a duty of 0% to 100% can be output from the TRGIOA pin.

Table 23.8 lists the PWM Mode Specifications, and Table 23.9 lists the Combination of PWM Output Pins and Registers. When the setting values of registers TRGGRA and TRGGRB are the same, the output value does not change even if a compare match occurs.

Table 23.8 PWM Mode Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, fOCO40M External signal input to the TRGCLKj pin (active edge selectable by a program)
Count operation	Increment
PWM waveform	• The high-level output timing for PWM waveforms is set in the TRGGRA register. • The low-level output timing for PWM waveforms is set in the TRGGRB register.
Count start condition	1 (count starts) is written to the TSTART bit in the TRGMR register.
Count stop condition	0 (count stops) is written to the TSTART bit in the TRGMR register.
Interrupt request generation timing	• Compare match (the contents of the TRG register and the TRGRj register match) • TRG register overflow
TRGIOA pin function	PWM output
TRGIOB pin function	Programmable I/O port
TRGCLKA/TRGCLKB pins function	Programmable I/O port or external clock input
Read from timer	The count value can be read by reading the TRG register.
Write to timer	The TRG register can be written to.
Selectable functions	• Timing for setting the TRG register to 0000h Overflow or compare match with the TRGGRj register • Buffer operation (Refer to **23.3.2 Buffer Operation**.)

j = A or B

Table 23.9 Combination of PWM Output Pins and Registers

Output Pin	High-Level Output	Low-Level Output
TRGIOA	TRGGRA	TRGGRB
TRGIOB	I/O port function	

23.6.1 Procedure Example for Setting PWM Mode

Figure 23.13 shows a Procedure Example for Setting PWM Mode.

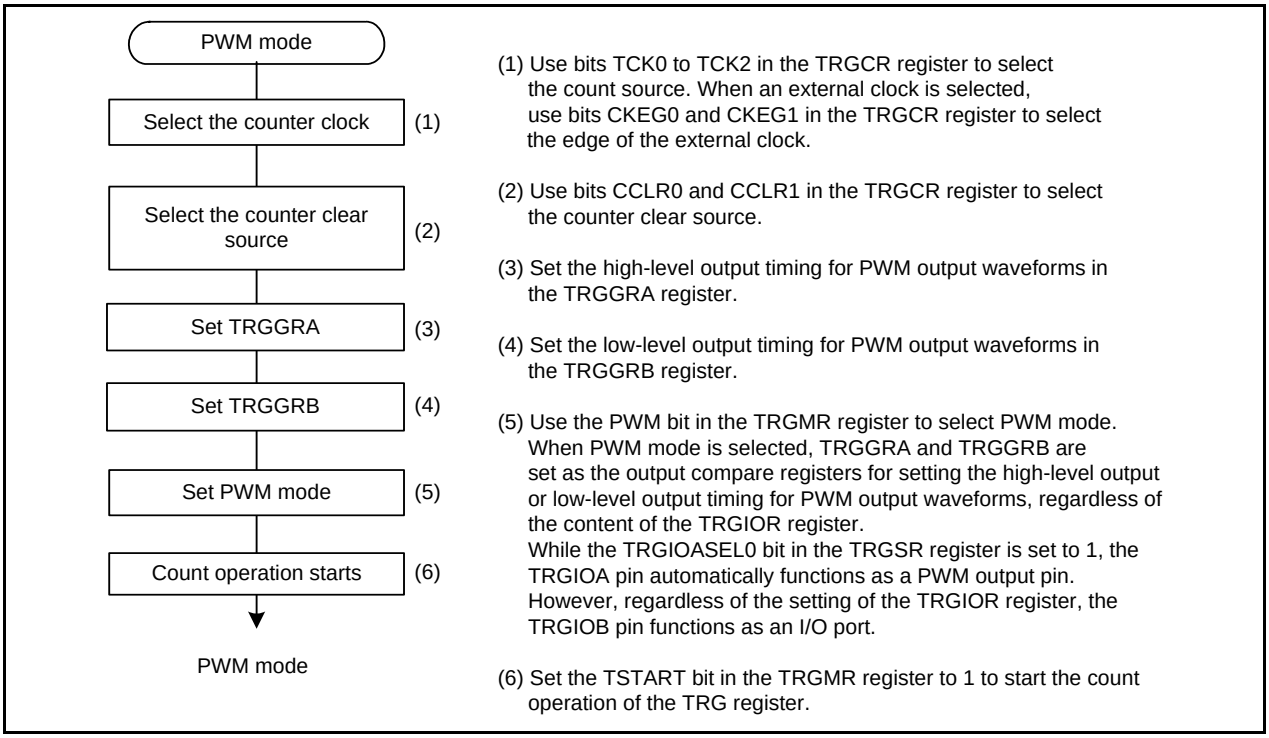


Figure 23.13 Procedure Example for Setting PWM Mode

23.6.2 Operating Example

Figure 23.14 shows an Operating Example in PWM Mode (1).
When PWM mode is selected while the TRGIOASEL0 bit in the TRGSR register is set to 1, the TRGIOA pin automatically functions as an output pin, high-level output at compare match with the TRGGRA register is selected, and low-level output at compare match with the TRGGRB register is selected. However, regardless of the setting of the TRGIOR register, the TRGIOB pin functions as an I/O port.

This example applies when a compare match with the TRGGRA or TRGGRB register is set as the counter clear source for the TRG register. The initial status of the TRGIOA pin depends only on the counter clear sources. This correspondence is shown in Table 23.10.

Table 23.10 Correspondence between Initial Status of TRGIOA Pin and Counter Clear Sources

Counter Clear Source	Initial Status of TRGIOA Pin
Compare match with TRGGRA register	High
Compare match with TRGGRB register	Low

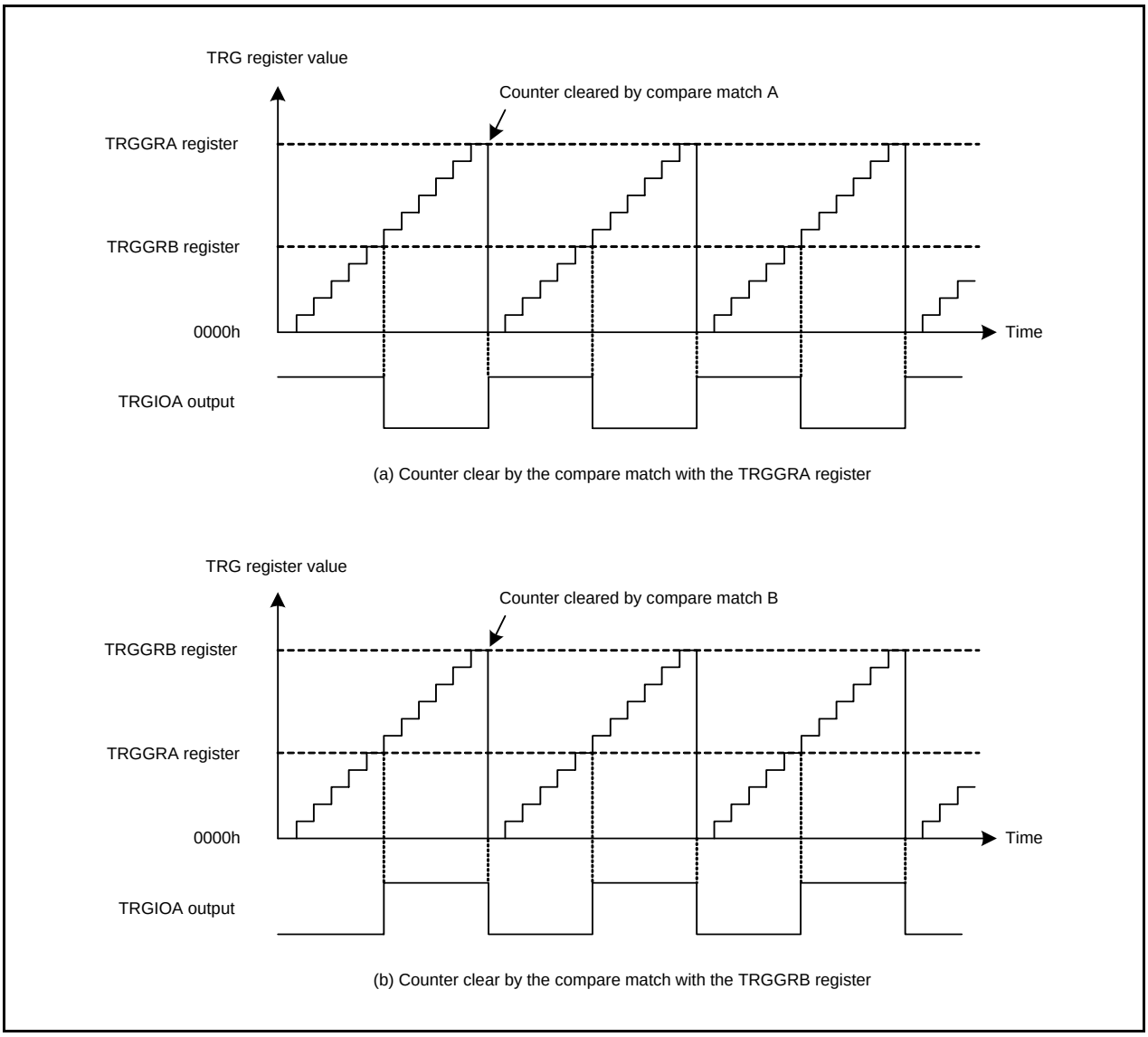


Figure 23.14 Operating Example in PWM Mode (1)

Figure 23.15 shows an example for outputting a PWM waveform with a duty of 0% and 100%.
The PWM waveform duty is set to 0% when a compare match with the TRGGRB register is set as the counter clear source under the following conditions:
• TRGGRA setting value > TRGGRB setting value
The PWM waveform duty is set to 100% when a compare match with TRGGRA register is set as the counter clear source under the following conditions:
• TRGGRB setting value > TRGGRA setting value

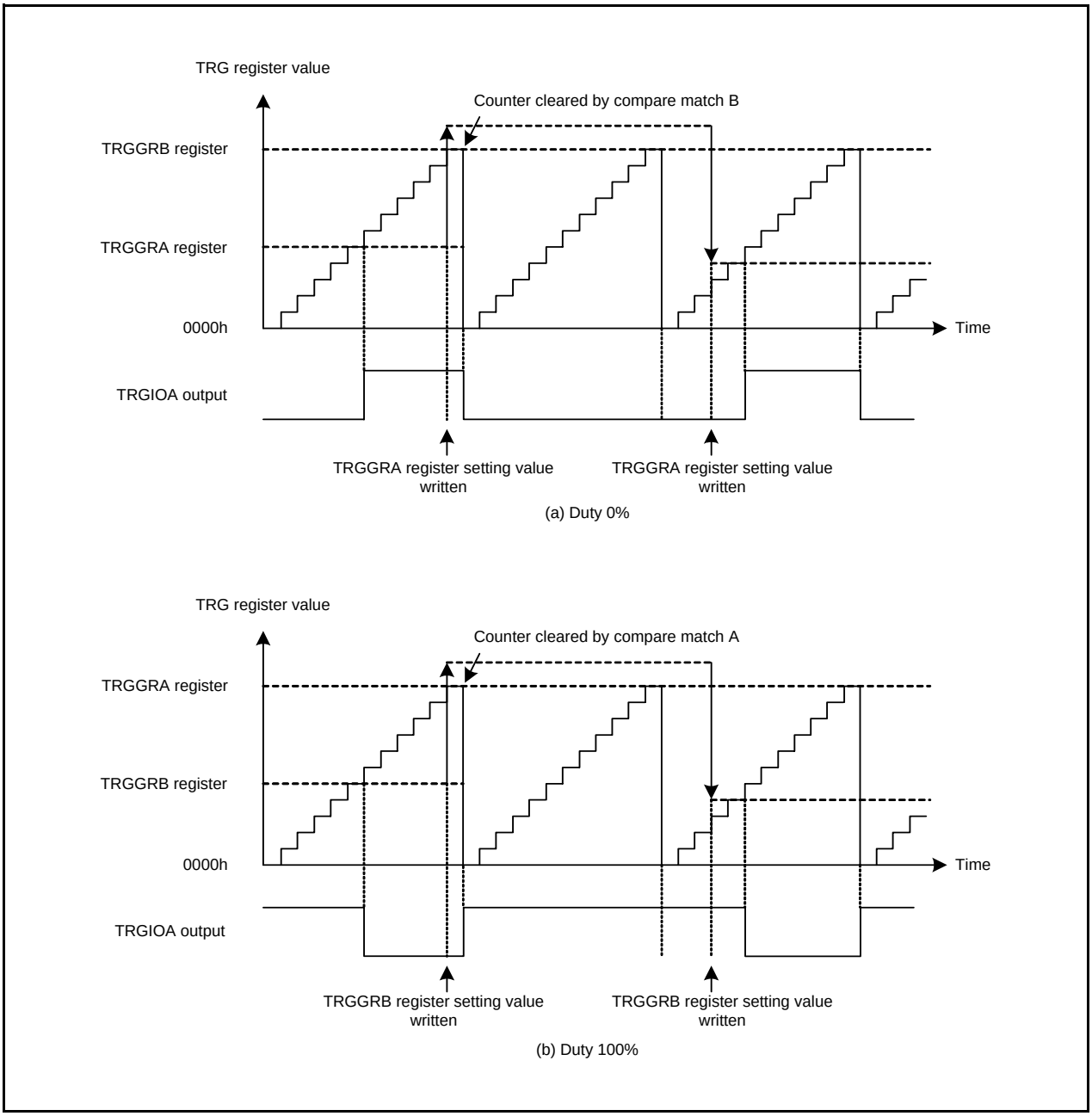


Figure 23.15 Operating Example in PWM Mode (2)

23.7 Phase Counting Mode

In phase counting mode, the phase difference between the external input signals from two pins TRGCLKA and TRGCLKB is detected and the TRG register is incremented or decremented.

When phase counting mode is selected while the bits TRGCLKASEL0 and TRGCLKBSEL0 are set to 1, regardless of the settings of bits TCK0 to TCK2 and bits CKEG0 and CKEG1 in the TRGCR register, pins TRGCLKA and TRGCLKB automatically function as external clock input pins and the TRG register is incrermented or decremented by setting bits CNTEN0 to CNTEN7 in the TRGCNTC register. However, bits CCLR0 and CCLR1 in the TRGCR register and registers TRGIOR, TRGIER, TRGSR, TRGGRA, and TRGGRB are enabled, so the input capture/output compare function, PWM output function, and interrupt sources can be used.

The TRG register operates counting at both the rising and falling edges of the TRGCLKA or TRGCLKB pin by setting bits CNTEN0 to CNTEN7. Table 23.11 lists the Phase Counting Mode Specifications, and Table 23.12 lists the Increment and Decrement Conditions for TRG Register.

Table 23.11 Phase Counting Mode Specifications

Item	Specification
Count source	External signal input to the TRGCLKj pin
Count operations	Increment/decrement
Count start condition	1 (count starts) is written to the TSTART bit in the TRGMR register.
Count stop condition	0 (count stops) is written to the TSTART bit in the TRGMR register.
Interrupt request generation timing	• Input capture (active edge of the TRGIOj input) • Compare match (the contents of the TRG register and the TRGGRj register match) • TRG register underflow • TRG register overflow
TRGIOA pin function	Programmable I/O port, input-capture input, output-compare output, or PWM output
TRGIOB pin function	Programmable I/O port, input-capture input, or output-compare output
TRGCLKA/TRGCLKB pins function	External clock input
Read from timer	The count value can be read by reading the TRG register.
Write to timer	The TRG register can be written to.
Selectable functions	• Selection of counter increment and decrement conditions Selectable by bits CNTEN7 to CNTEN0 bits in the TRGCNTC register. • The input capture/output compare function and PWM function can be used.

j = A or B

Table 23.12 Increment and Decrement Conditions for TRG Register

TRGCLKB pin	↑		High		↓		Low		High		↓		Low		↑	
TRGCLKA pin	Low		↑		High		↓		↓		Low		↑		High	
Bits CNTEN7 to CNTEN0 in TRGCNTC register	CNTEN7		CNTEN6		CNTEN5		CNTEN4		CNTEN3		CNTEN2		CNTEN1		CNTEN0	
Value	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Count direction	–	+1	–	+1	–	+1	–	+1	–	–1	–	–1	–	–1	–	–1

23.7.1 Timer RG Control Register (TRGCR) in Phase Counting Mode

Address 0172h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	CCLR1	CCLR0	CKEG1	CKEG0	TCK2	TCK1	TCK0
After Reset	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TCK0	Count source select bit	Disabled in phase counting mode.	R/W
b1	TCK1			R/W
b2	TCK2			R/W
b3	CKEG0	External clock active edge select bit	Disabled in phase counting mode.	R/W
b4	CKEG1			R/W
b5	CCLR0	TRG register clear select bit	b6 b5 0 0: Clear disabled 0 1: TRG register cleared by input capture or compare match with TRGGRA 1 0: TRG register cleared by input capture or compare match with TRGGRB 1 1: Do not set.	R/W
b6	CCLR1			R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

23.7.2 Procedure Example for Setting Phase Counting Mode

Figure 23.16 shows a Procedure Example for Setting Phase Counting Mode.

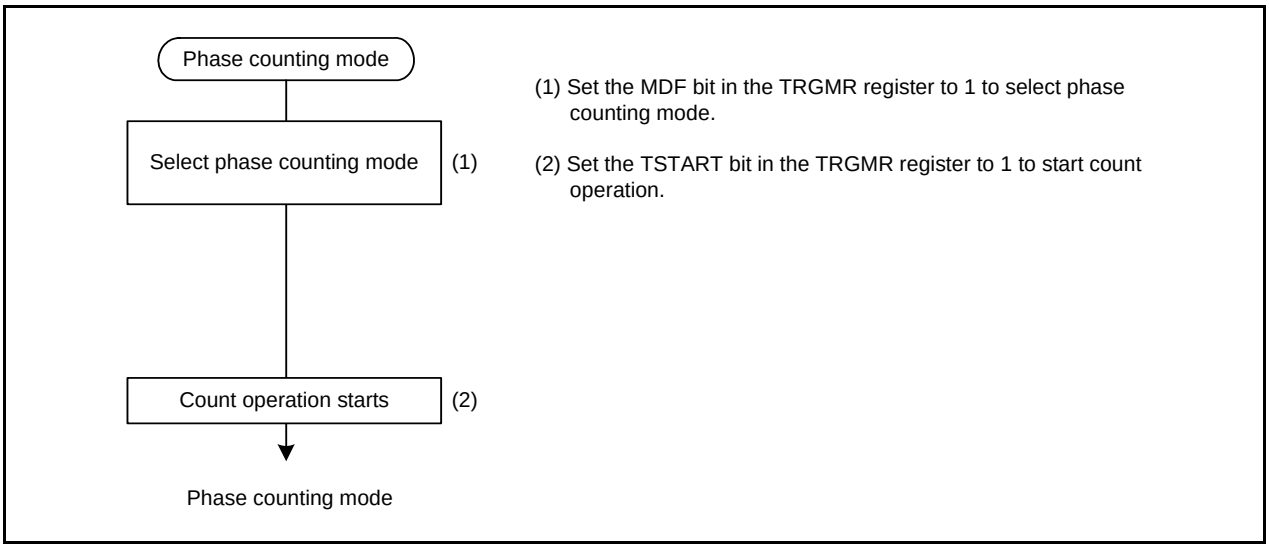


Figure 23.16 Procedure Example for Setting Phase Counting Mode

23.7.3 Operating Example

Figures 23.17 to 23.20 show operating examples in phase counting mode. Table 23.12 lists the Increment and Decrement Conditions for TRG Register.

In phase counting mode, the TRG register is incremented or decremented at both the rising (↑) and falling (↓) edges of the TRGCLKA or TRGCLKB pin by setting bits CNTEN0 to CNTEN7 in the TRGCNTC register.

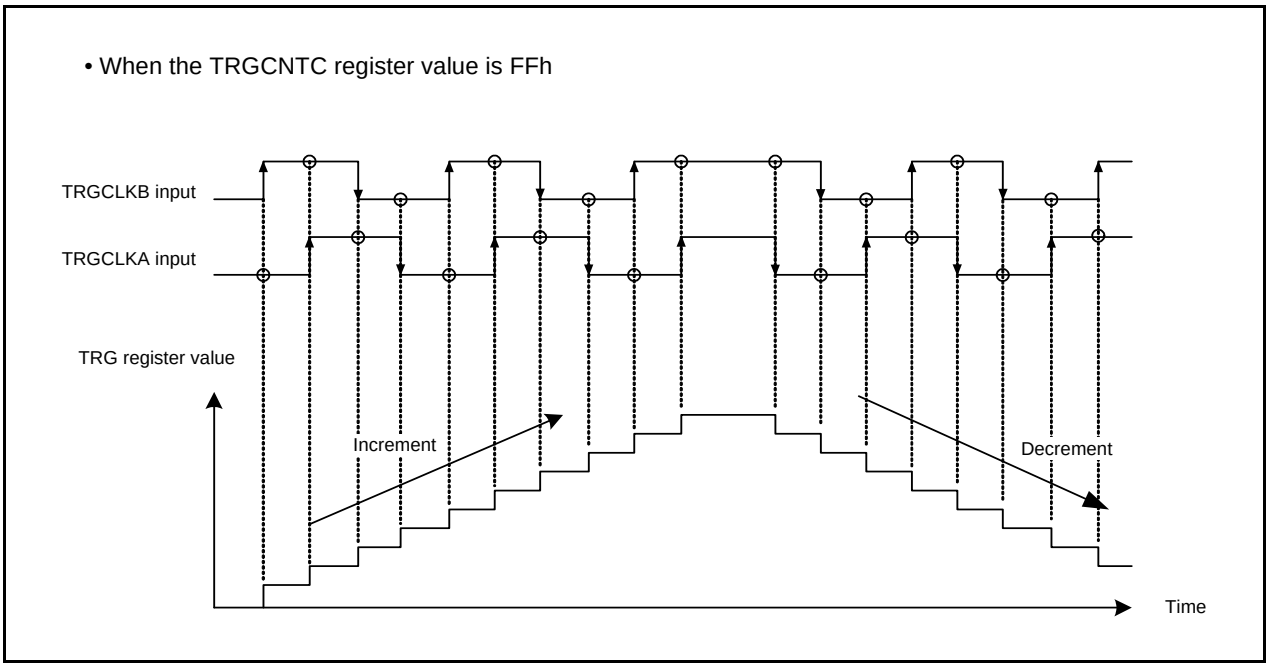


Figure 23.17 Operating Example in Phase Counting Mode 1

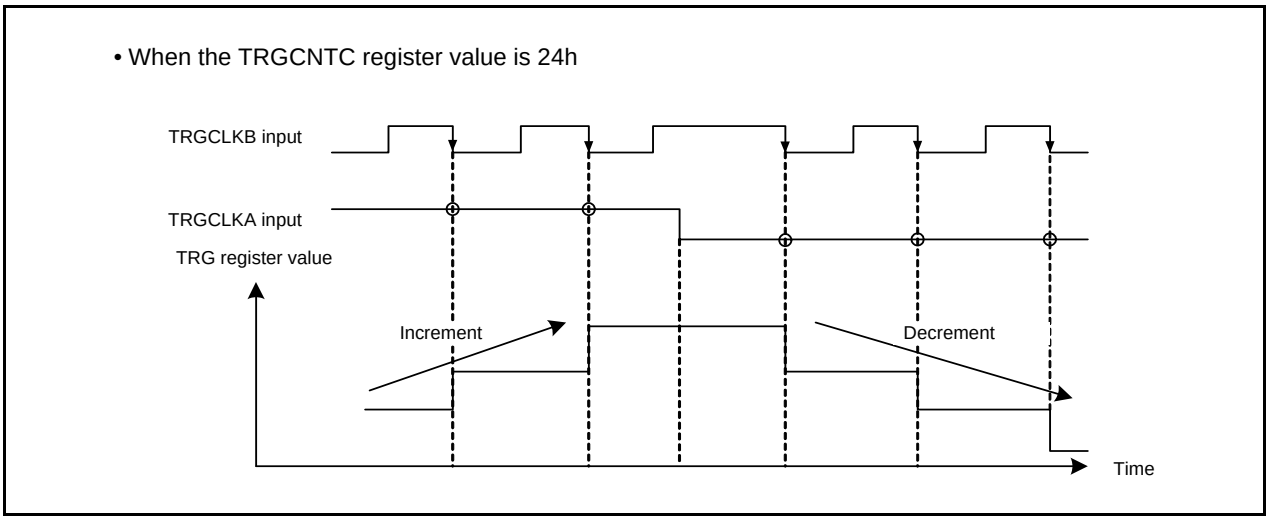


Figure 23.18 Operating Example in Phase Counting Mode 2

• When the TRGCNTC register value is 28h

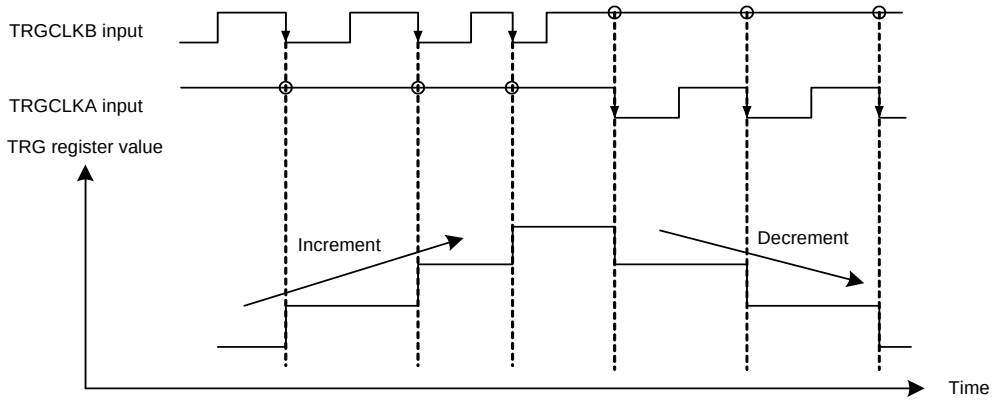


Figure 23.19 Operating Example in Phase Counting Mode 3

• When the TRGCNTC register value is 5Ah

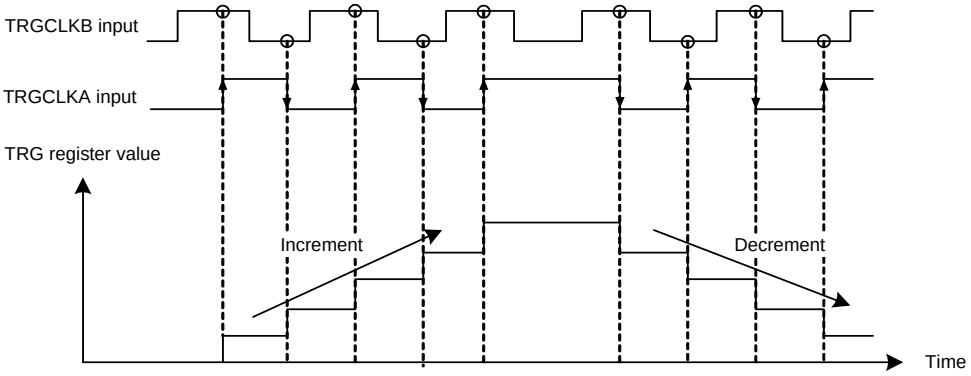


Figure 23.20 Operating Example in Phase Counting Mode 4

23.8 Timer RG Interrupt

Timer RG generates a timer RG interrupt request from four sources. The timer RG interrupt uses the single TRGIC register (bits IR and ILVL0 to ILVL2) and a single vector.
Table 23.13 lists the Registers Associated with Timer RG Interrupt, and Figure 23.21 is a Block Diagram of Timer RG Interrupt.

Table 23.13 Registers Associated with Timer RG Interrupt

Timer RG Status Register	Timer RG Interrupt Enable Register	Timer RG Interrupt Control Register
TRGSR	TRGIER	TRGIC

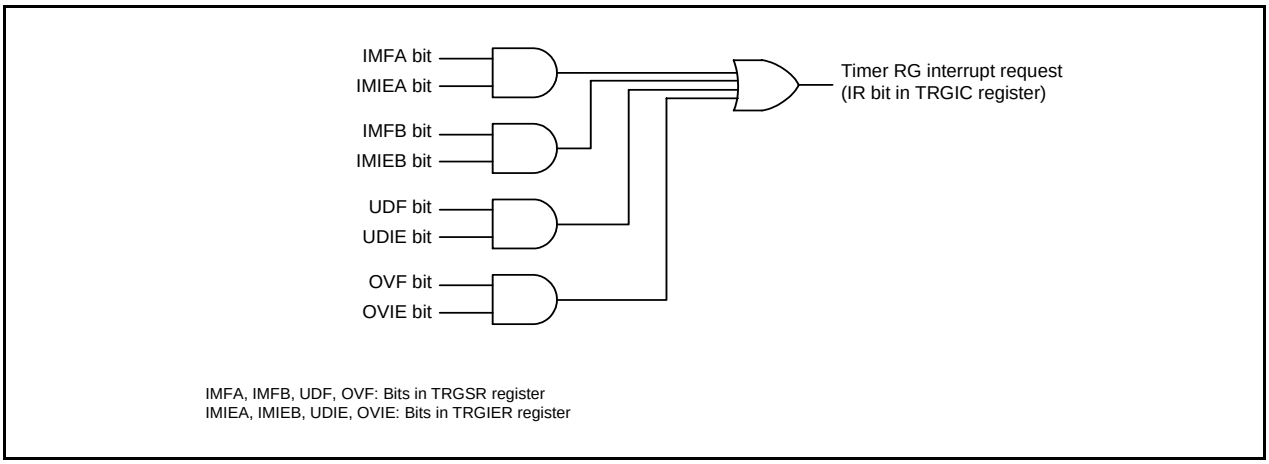


Figure 23.21 Block Diagram of Timer RG Interrupt

Like other maskable interrupts, the timer RG interrupt is controlled by the combination of the I flag, IR bit, bits ILVL0 to ILVL2, and IPL. However, it differs from other maskable interrupts in the following respects because a single interrupt source (timer RG interrupt) is generated from multiple interrupt request sources.

- The IR bit in the TRGIC register is set to 1 (interrupt requested) when a bit in the TRGSR register is set to 1 and the corresponding bit in the TRGIER register is also set to 1 (interrupt enabled).
- The IR bit is set to 0 (no interrupt requested) when either the bit in the TRGSR register or the corresponding bit in the TRGIER register is set to 0, or both are set to 0. In other words, the interrupt request is not maintained even if the IR bit is once set to 1 but the interrupt is not acknowledged.
- If another interrupt source is triggered after the IR bit is set to 1, the IR bit remains set to 1 and does not change.
- If multiple bits in the TRGIER register are set to 1, use the TRGSR register to determine the source of the interrupt request.
- The bits in the TRGSR register are not automatically set to 0 when an interrupt is acknowledged. Set them to 0 within the interrupt routine. Refer to **23.2.5 Timer RG Status Register (TRGSR)**, for the procedure for setting these bits to 0.

Refer to **23.2.4 Timer RG Interrupt Enable Register (TRGIER)**, for details of the TRGIER register.
Refer to **12.3 Interrupt Control**, for details of the TRGIC register and **12.1.5.2 Relocatable Vector Tables**, for information on interrupt vectors.

23.9 Notes on Timer RG

23.9.1 Phase Difference, Overlap, and Pulse Width in Phase Counting Mode

The phase difference and overlap between the external input signals from pins TRGCLKA and TRGCLKB should be 1.5 f1 or more, respectively. The pulse width should be 2.5 f1 or more. Figure 23.22 shows the Phase Difference, Overlap, and Pulse Width in Phase Counting Mode.

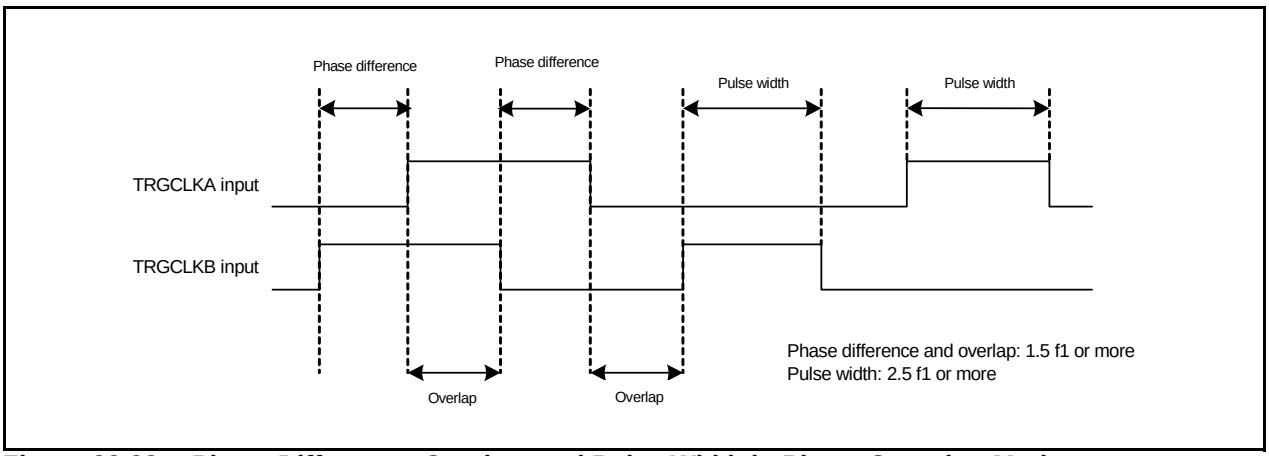


Figure 23.22 Phase Difference, Overlap, and Pulse Width in Phase Counting Mode

24. Serial Interface (UARTi (i = 0 or 1))

The serial interface consists of three channels, UART0 to UART2. This chapter describes UARTi (i = 0 or 1).

24.1 Introduction

UART0 and UART 1 have a dedicated timer to generate a transfer clock and operate independently. Clock synchronous serial I/O mode and clock asynchronous serial I/O mode (UART mode) are supported.
Figure 24.1 shows a Block Diagram of UARTi (i = 0 or 1). Figure 24.2 shows a Block Diagram of UARTi (i = 0 or 1) Transmit/Receive Unit. Table 24.1 lists the Pin Configuration of UARTi (i = 0 or 1).

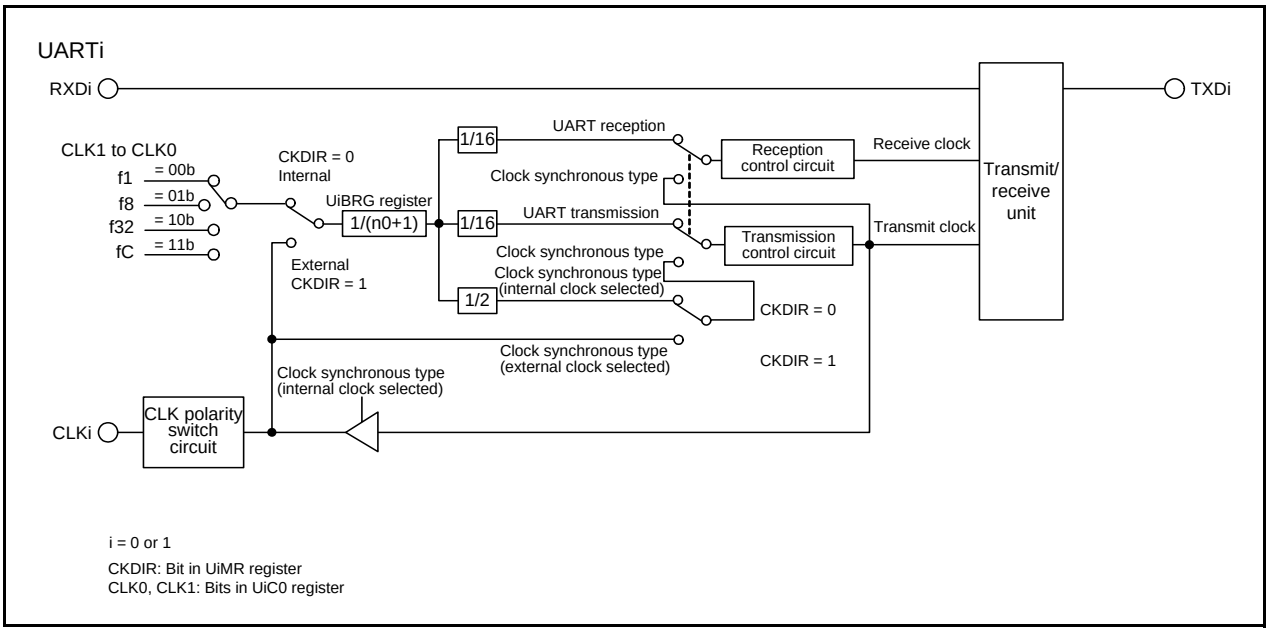


Figure 24.1 Block Diagram of UARTi (i = 0 or 1)

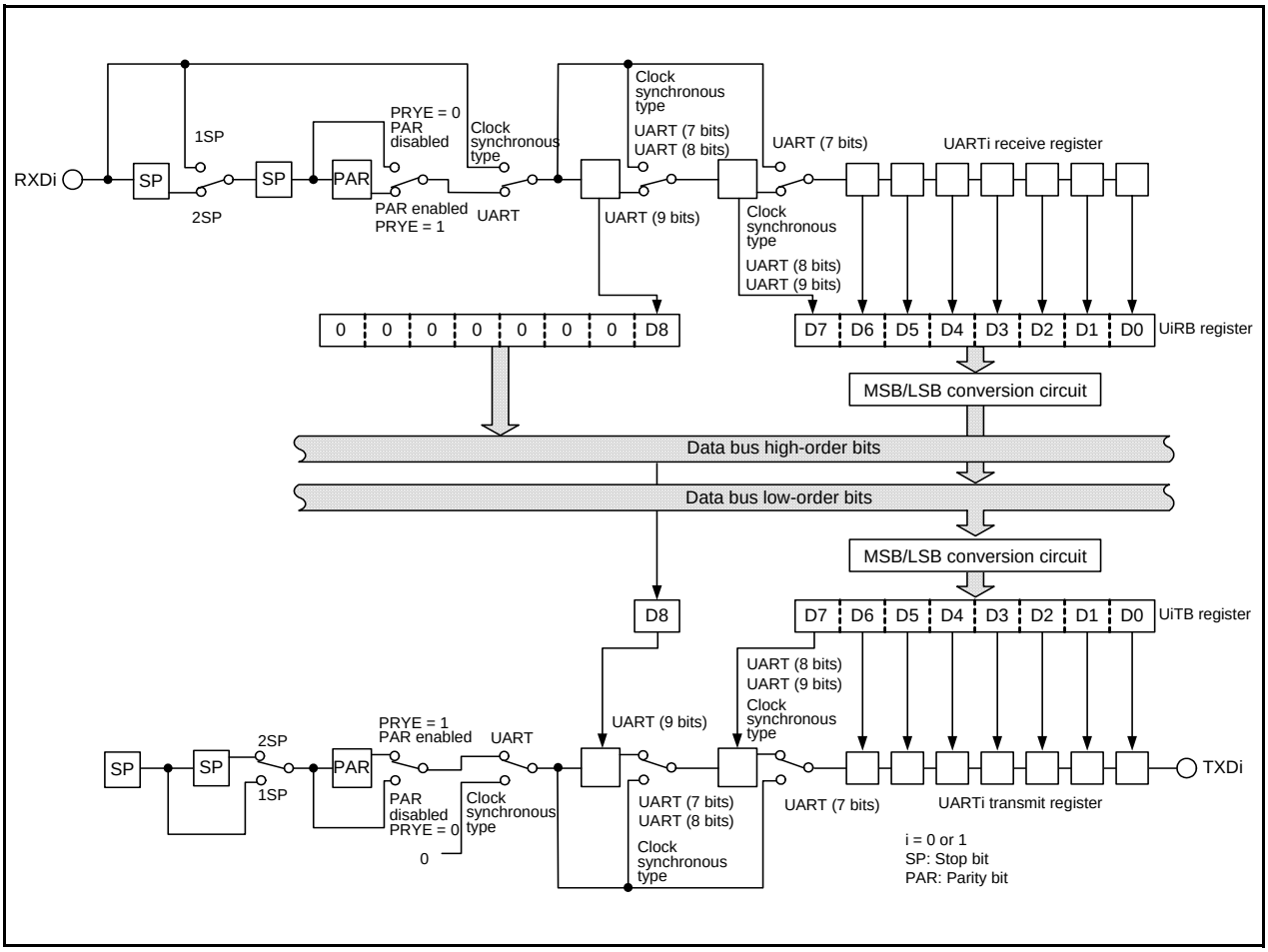


Figure 24.2 Block Diagram of UARTi (i = 0 or 1) Transmit/Receive Unit

Table 24.1 Pin Configuration of UARTi (i = 0 or 1)

Pin Name	Assigned Pin	I/O	Function
TXD0	P13_1	Output	Serial data output
RXD0	P13_2	Input	Serial data input
CLK0	P13_3	I/O	Transfer clock I/O
TXD1	P4_0	Input	Serial data output
RXD1	P4_1	Output	Serial data input
CLK1	P4_2	I/O	Transfer clock I/O

24.2 Registers

24.2.1 UARTi Transmit/Receive Mode Register (UiMR) (i = 0 or 1)

Address 00A0h (U0MR), 0160h (U1MR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	PRYE	PRY	STPS	CKDIR	SMD2	SMD1	SMD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SMD0	Serial I/O mode select bit	b2 b1 b0 0 0 0: Serial interface disabled 0 0 1: Clock synchronous serial I/O mode 1 0 0: UART mode, transfer data 7 bits long 1 0 1: UART mode, transfer data 8 bits long 1 1 0: UART mode, transfer data 9 bits long Other than above: Do not set.	R/W
b1	SMD1			R/W
b2	SMD2			R/W
b3	CKDIR	Internal/external clock select bit	0: Internal clock 1: External clock	R/W
b4	STPS	Stop bit length select bit	0: One stop bit 1: Two stop bits	R/W
b5	PRY	Odd/even parity select bit	Enabled when PRYE = 1 0: Odd parity 1: Even parity	R/W
b6	PRYE	Parity enable bit	0: Parity disabled 1: Parity enabled	R/W
b7	—	Reserved bit	Set to 0.	R/W

24.2.2 UARTi Bit Rate Register (UiBRG) (i = 0 or 1)

Address 00A1h (U0BRG), 0161h (U1BRG)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7 to b0	If the setting value is n, UiBRG divides the count source by n+1.	00h to FFh	W

Write to the UiBRG register while transmission and reception stop.
Use the MOV instruction to write to this register.
Set bits CLK0 and CLK1 in the UiC0 register before writing to the UiBRG register.

24.2.3 UARTi Transmit Buffer Register (UiTB) (i = 0 or 1)

Address 00A3h to 00A2h (U0TB), 0163h to 0162h (U1TB)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Function	R/W
b0	—	Transmit data	W
b1	—		
b2	—		
b3	—		
b4	—		
b5	—		
b6	—		
b7	—		
b8	—		
b9	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.	—
b10	—		
b11	—		
b12	—		
b13	—		
b14	—		
b15	—		

When the transfer data is 9 bits long, write data to the high-order byte first, then low-order byte of the UiTB register.
Use the MOV instruction to write to this register.

24.2.4 UARTi Transmit/Receive Control Register 0 (UiC0) (i = 0 or 1)

Address 00A4h (U0C0), 0164h (U1C0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	UFORM	CKPOL	NCH	—	TXEPT	—	CLK1	CLK0
After Reset	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CLK0	BRG count source select bit (1)	b1 b0 0 0: f1 selected 0 1: f8 selected 1 0: f32 selected 1 1: fC selected	R/W
b1	CLK1			R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	TXEPT	Transmit register empty flag	0: Data in the transmit register (transmission in progress) 1: No data in the transmit register (transmission completed)	R
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	NCH	Data output select bit	0: TXDi pin set as CMOS output 1: TXDi pin set as N-channel open-drain output	R/W
b6	CKPOL	CLK polarity select bit	0: Transmit data output at the falling edge and receive data input at the rising edge of the transfer clock 1: Transmit data output at the rising edge and receive data input at the falling edge of the transfer clock	R/W
b7	UFORM	Transfer format select bit	0: LSB first 1: MSB first	R/W

Note:
1. If the BRG count source is switched, set the UiBRG register again.

24.2.5 UARTi Transmit/Receive Control Register 1 (UiC1) (i = 0 or 1)

Address 00A5h (U0C1), 0165h (U1C1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	UiRRM	UiIRS	RI	RE	TI	TE
After Reset	0	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	TE	Transmission enable bit	0: Transmission disabled 1: Transmission enabled	R/W
b1	TI	Transmit buffer empty flag	0: Data in the UiTB register 1: No data in the UiTB register	R
b2	RE	Reception enable bit	0: Reception disabled 1: Reception enabled	R/W
b3	RI	Reception complete flag (1)	0: No data in the UiRB register 1: Data in the UiRB register	R
b4	UiIRS	UARTi transmit interrupt source select bit	0: Transmit buffer empty (TI = 1) 1: Transmission completed (TXEPT = 1)	R/W
b5	UiRRM	UARTi continuous receive mode enable bit (2)	0: Continuous receive mode disabled 1: Continuous receive mode enabled	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

Notes:
1. The RI bit is set to 0 when the higher byte of the UiRB register is read.
2. In UART mode, set the UiRRM bit to 0 (continuous receive mode disabled).

24.2.6 UARTi Receive Buffer Register (UiRB) (i = 0 or 1)

Address 00A7h to 00A6h (U0RB), 0167h to 0166h (U1RB)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	SUM	PER	FER	OER	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	—	—	Receive data (D7 to D0)	R
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			
b8	—	—	Receive data (D8)	R
b9	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b10	—			
b11	—			
b12	OER	Overrun error flag (1)	0: No overrun error 1: Overrun error	R
b13	FER	Framing error flag (1)	0: No framing error 1: Framing error	R
b14	PER	Parity error flag (1)	0: No parity error 1: Parity error	R
b15	SUM	Error sum flag (1)	0: No error 1: Error	R

Note:
1. Bits SUM, PER, FER, and OER are set to 0 (no error) when either of the following is set:
   - Bits SMD2 to SMD0 in the UiMR register are set to 000b (serial interface disabled).
   - The RE bit in the UiC1 register is set to 0 (reception disabled).

   The SUM bit is set to 0 (no error) when all of bits PER, FER, and OER are set to 0 (no error).
   Bits PER and FER are also set to 0 when the high-order byte of the UiRB register is read.

   Always read the UiRB register in 16-bit units.

24.2.7 UART0 Pin Select Register (U0SR)

Address 0188h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	CLK0SEL0	—	RXD0SEL0	RXD0SEL1	TXD0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TXD0SEL0	TXD0 pin select bit	0: TXD0 pin not used 1: TXD0 pin used	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	RXD0SEL0	RXD0 pin select bit	b3 b2 0 0: RXD0 pin not used 0 1: P13_2 assigned 1 0: P11_4 assigned 1 1: Do not set.	R/W
b3	RXD0SEL1			R/W
b4	CLK0SEL0	CLK0 pin select bit	0: CLK0 pin not used 1: CLK0 pin used	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	—			
b7	—			

The U0SR register selects which pin is assigned as the UART0 input/output. To use the I/O pins for UART0, set this register.
Set the U0SR register before setting the UART0 associated registers. Also, do not change the setting value of this register during UART0 operation.

24.2.8 UART1 Pin Select Register (U1SR)

Address 0189h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	CLK1SEL0	—	RXD1SEL0	—	TXD1SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TXD1SEL0	TXD1 pin select bit	0: TXD1 pin not used 1: TXD1 pin used	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	RXD1SEL0	RXD1 pin select bit	0: RXD1 pin not used 1: RXD1 pin used	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	CLK1SEL0	CLK1 pin select bit	0: CLK1 pin not used 1: CLK1 pin used	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	—			
b7	—			

The U1SR register selects which pin is assigned as the UART1 input/output. To use the I/O pins for UART1, set this register.
Set the U1SR register before setting the UART1 associated registers. Also, do not change the setting value of this register during UART1 operation.

24.3 Clock Synchronous Serial I/O Mode

In clock synchronous serial I/O mode, data is transmitted and received using a transfer clock.
Table 24.2 lists the Clock Synchronous Serial I/O Mode Specifications. Table 24.3 lists the Registers Used and Settings in Clock Synchronous Serial I/O Mode (1).

Table 24.2 Clock Synchronous Serial I/O Mode Specifications

Item	Specification
Transfer data format	• Transfer data length: 8 bits
Transfer clocks	• The CKDIR bit in the UiMR register is set to 0 (internal clock): fi/(2(n+1)) fi = f1, f8, f32, fC n = Value set in UiBRG register: 00h to FFh • The CKDIR bit is set to 1 (external clock): Input from the CLKi pin
Transmit start conditions	• To start transmission, the following requirements must be met: (1) - The TE bit in the UiC1 register is set to 1 (transmission enabled). - The TI bit in the UiC1 register is set to 0 (data in the UiTB register).
Receive start conditions	• To start reception, the following requirements must be met: (1) - The RE bit in the UiC1 register is set to 1 (reception enabled). - The TE bit in the UiC1 register is set to 1 (transmission enabled). - The TI bit in the UiC1 register is set to 0 (data in the UiTB register).
Interrupt request generation timing	• For transmission, one of the following can be selected. - The UiIRS bit is set to 0 (transmit buffer empty): When data is transferred from the UiTB register to the UARTi transmit register (at start of transmission). - The UiIRS bit is set to 1 (transmission completed): When data transmission from the UARTi transmit register is completed. • For reception When data is transferred from the UARTi receive register to the UiRB register (at completion of reception).
Error detection	• Overrun error (2) This error occurs if the serial interface starts receiving the next unit of data before reading the UiRB register and receives the 7th bit of the next unit of data.
Selectable functions	• CLK polarity selection Transfer data input/output can be selected to occur synchronously with the rising or the falling edge of the transfer clock. • LSB first, MSB first selection Whether data transmission/reception begins with bit 0 or begins with bit 7 can be selected. • Continuous receive mode selection Reception is enabled immediately by reading the UiRB register.

i = 0 or 1

Notes:

1. When an external clock is selected, the requirements must be met in either of the following states:
   - The external clock is held high when the CKPOL bit in the UiC0 register is set to 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)
   - The external clock is held low when the CKPOL bit in the UiC0 register is set to 1 (transmit data output at the rising edge and receive data input at the falling edge of the transfer clock)
2. If an overrun error occurs, the receive data (b0 to b8) in the UiRB register will be undefined.
   The IR bit in the SiRIC register remains unchanged.

Table 24.3 Registers Used and Settings in Clock Synchronous Serial I/O Mode (1)

Register	Bit	Function
UiTB	b0 to b7	Set data transmission.
UiRB	b0 to b7	Receive data can be read.
	OER	Overrun error flag
UiBRG	b0 to b7	Set the transfer rate.
UiMR	SMD2 to SMD0	Set to 001b.
	CKDIR	Select an internal clock or external clock.
UiC0	CLK0, CLK1	Select the count source for the UiBRG register.
	TXEPT	Transmit register empty flag
	NCH	Select the output format of the TXDi pin.
	CKPOL	Select the transfer clock polarity.
	UFORM	Select LSB first or MSB first.
UiC1	TE	Set to 1 to enable transmission/reception
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	UiIRS	Select the UARTi transmit interrupt source.
	UiRRM	Set to 1 to use continuous receive mode.

i = 0 or 1

Note:

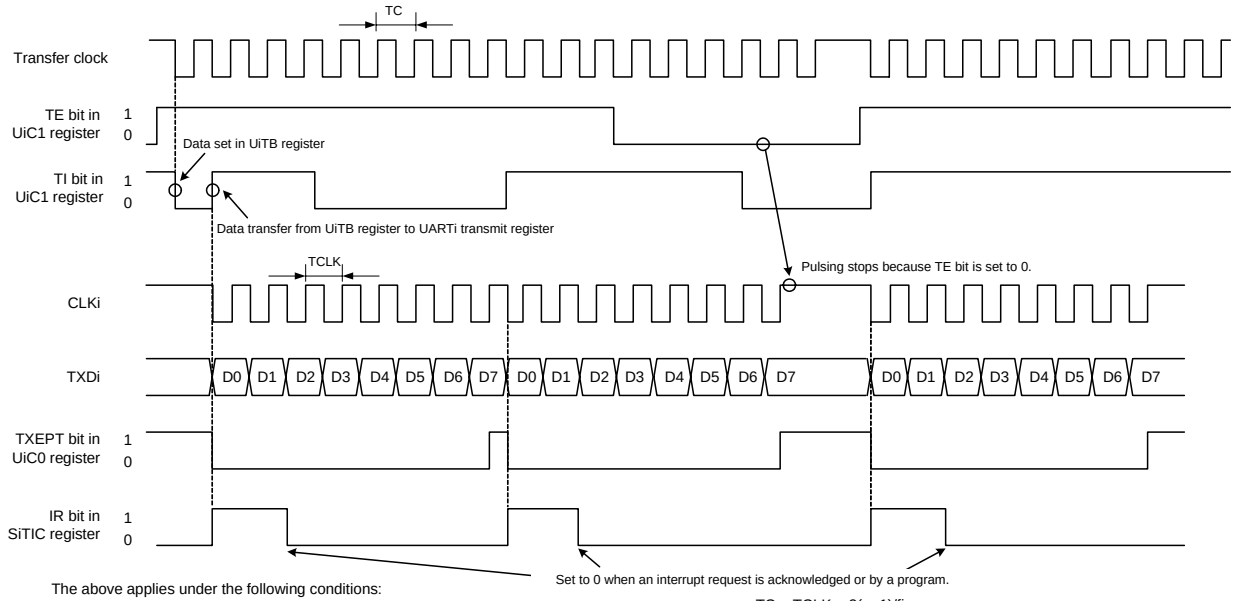
1. Set the bits not listed in this table to 0 when writing to the above registers in clock synchronous serial I/O mode.

Table 24.4 lists the I/O Pin Functions in Clock Synchronous Serial I/O Mode.
After UARTi (i = 0 or 1) operating mode is selected, the TXDi pin outputs a high-level signal until transfer starts. (When the NCH bit is set to 1 (N-channel open-drain output), this pin is in the high-impedance state.)

Table 24.4 I/O Pin Functions in Clock Synchronous Serial I/O Mode

Pin Name	Function	Selection Method
TXD0 (P13_1)	Serial data output	TXD0SEL0 bit in U0SR register = 1 For reception only: P13_1 can be used as a port by setting TXD0SEL0 bit = 0.
RXD0 (P13_2)	Serial data input	Bits RXD0SEL1 and RXD0SEL0 in U0SR register = 01b PD13_2 bit in PD3 register = 0 For transmission only: P13_2 can be used as a port by setting bits RXD0SEL1 to RXD0SEL0 = 00b.
CLK0 (P13_3)	Transfer clock output	CLK0SEL0 bit in U0SR register = 1 CKDIR bit in U0MR register = 0
	Transfer clock input	CLK0SEL0 bit in U0SR register = 1 CKDIR bit in U0MR register = 1 PD13_3 bit in PD3 register = 0
TXD1 (P4_0)	Serial data output	TXD1SEL0 bit in U1SR register = 1 For reception only: P4_0 can be used as a port by setting TXD1SEL0 bit = 0.
RXD1 (P4_1)	Serial data input	Bits RXD0SEL1 and RXD0SEL0 in U1SR register = 10b PD4_1 bit in PD4 register = 0 For transmission only: P4_1 can be used as a port by setting bits RXD0SEL1 to RXD0SEL0 = 00b.
CLK1 (P4_2)	Transfer clock output	CLK1SEL0 bit in U1SR register = 1 CKDIR bit in U1MR register = 0
	Transfer clock input	CLK1SEL0 bit in U1SR register = 1 CKDIR bit in U1MR register = 0 PD4_2 bit in PD4 register = 0

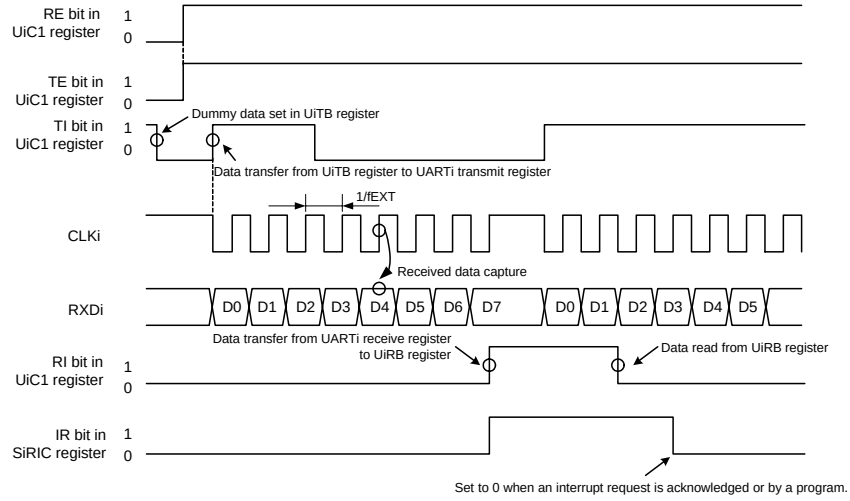
• Transmit Timing Example (Internal Clock Selected)



The above applies under the following conditions:
- CKDIR bit in UiMR register = 0 (internal clock)
- CKPOL bit in UiC0 register = 0
  (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)
- UiIRS bit in UiC1 register = 0
  (interrupt request generation when the transmit buffer is empty)

TC = TCLK = 2(n+1)/fi
fi: Frequency of UiBRG count source (f1, f8, f32, fC)
n: Value set in UiBRG register

• Receive Timing Example (External Clock Selected)



The above applies under the following conditions:
- CKDIR bit in UiMR register = 1 (external clock)
- CKPOL bit in UiC0 register = 0
  (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)

The following should be met when a high-level is applied to the CLKi pin before receiving data:
- TE bit in UiC1 register = 1 (transmission enabled)
- RE bit in UiC1 register = 1 (reception enabled)
- Dummy data write to the UiTB register

fEXT: Frequency of external clock

i = 0 or 1

Figure 24.3 Transmit and Receive Timing in Clock Synchronous Serial I/O Mode

24.3.1 Polarity Select Function

Figure 24.4 shows the Transfer Clock Polarity. The CKPOL bit in the UiC0 (i = 0 or 1) register can be used to select the transfer clock polarity.

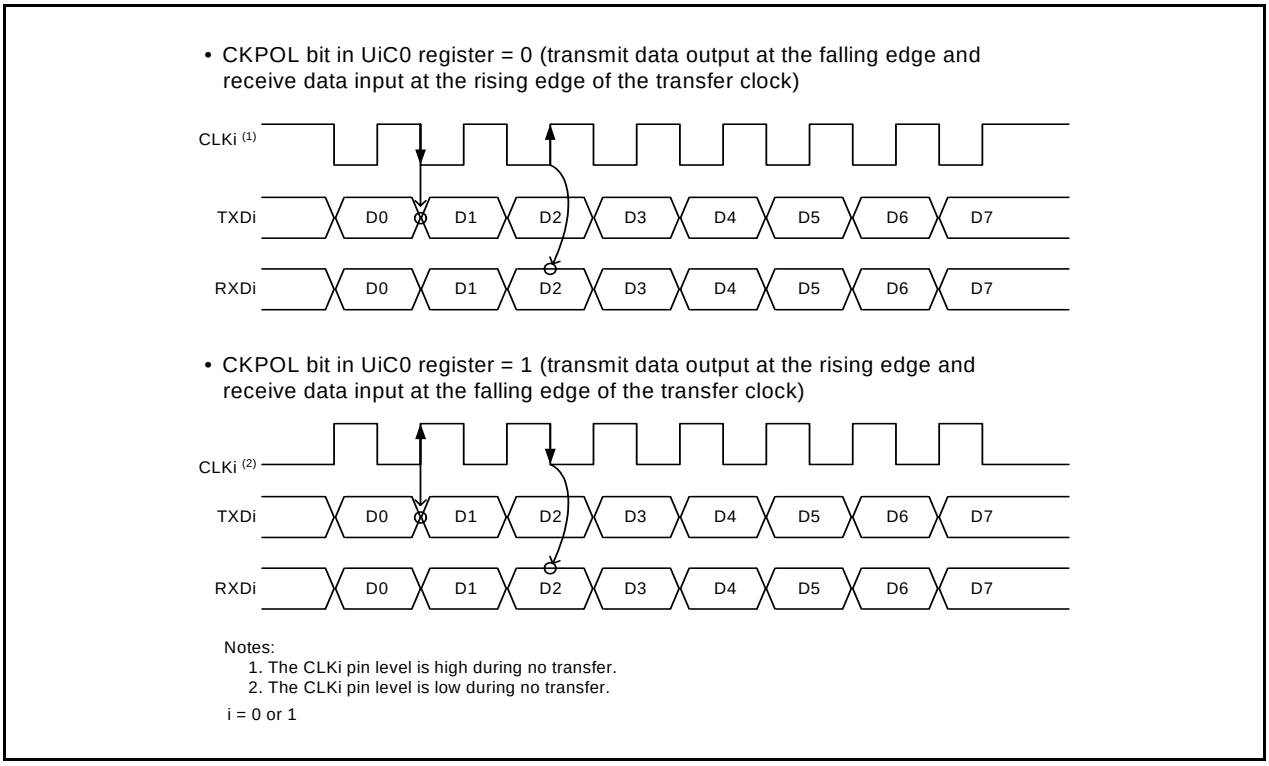


Figure 24.4 Transfer Clock Polarity

24.3.2 LSB First/MSB First Select Function

Figure 24.5 shows the Transfer Format. The UFORM bit in the UiC0 (i = 0 or 1) register can be used to select the transfer format.

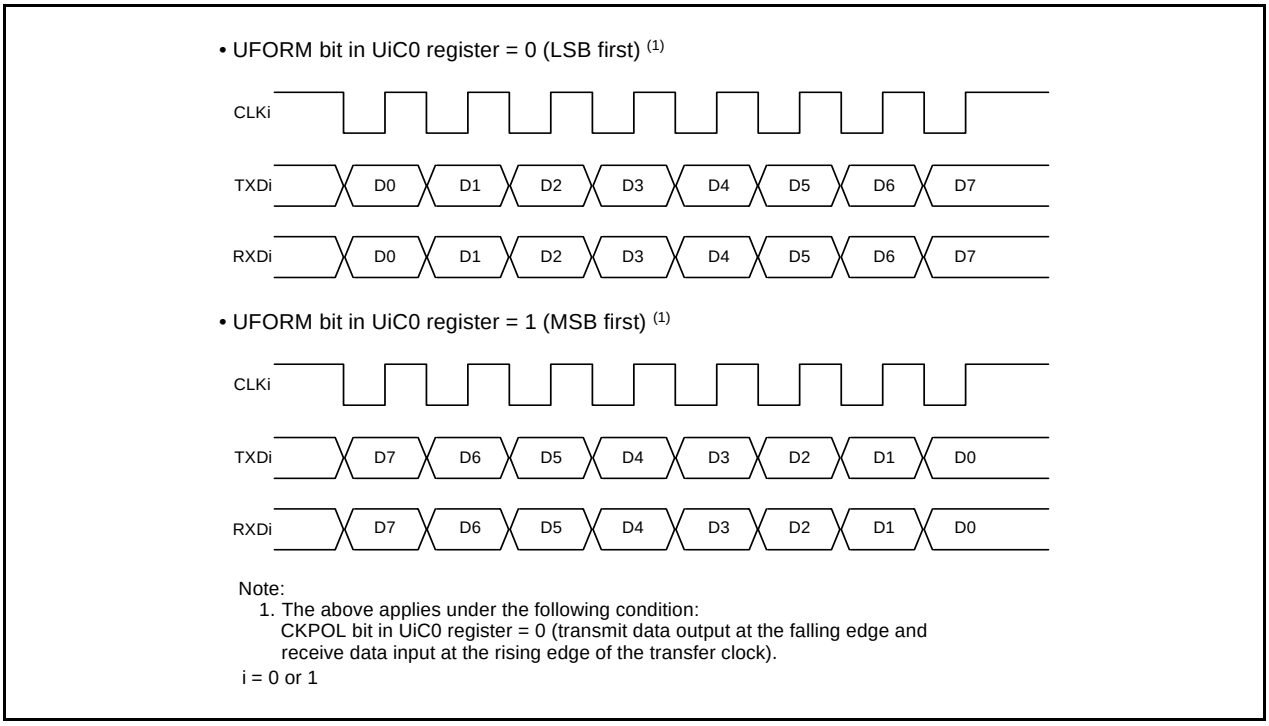


Figure 24.5 Transfer Format

24.3.3 Continuous Receive Mode

Continuous receive mode is selected by setting the UiRRM bit in the UiC1 register (i = 0 or 1) to 1 (continuous receive mode enabled). In this mode, reading the UiRB register sets the TI bit in the UiC1 register to 0 (data in the UiTB register). When the UiRRM bit is set to 1, do not write dummy data to the UiTB register by a program.

24.4 Clock Asynchronous Serial I/O (UART) Mode

The UART mode allows data transmission and reception after setting the desired transfer rate and transfer data format.
Table 24.5 lists the UART Mode Specifications, and Table 24.6 lists the Registers Used and Settings in UART Mode.

Table 24.5 UART Mode Specifications

Item	Specification
Transfer data formats	• Character bits (transfer data): Selectable from 7, 8 or 9 bits • Start bit: 1 bit • Parity bit: Selectable from odd, even, or none • Stop bits: Selectable from 1 or 2 bits
Transfer clocks	• The CKDIR bit in the UiMR register is set to 0 (internal clock): fj/(16(n+1)) fj = f1, f8, f32, fC n = Value set in UiBRG register: 00h to FFh • The CKDIR bit is set to 1 (external clock): fEXT/(16(n+1)) fEXT: Input from CLKi pin, n = Value set in UiBRG register: 00h to FFh
Transmit start conditions	• To start transmission, the following requirements must be met: - The TE bit in the UiC1 register is set to 1 (transmission enabled). - The TI bit in the UiC1 register is set to 0 (data in the UiTB register).
Receive start conditions	• To start reception, the following requirements must be met: - The RE bit in the UiC1 register is set to 1 (reception enabled). - Start bit detection
Interrupt request generation timing	• For transmission, one of the following can be selected. - The UiIRS bit is set to 0 (transmit buffer empty): When data is transferred from the UiTB register to the UARTi transmit register (at start of transmission). - The UiIRS bit is set to 1 (transfer completed): When data transmission from the UARTi transmit register is completed. • For reception When data is transferred from the UARTi receive register to the UiRB register (at completion of reception).
Error detection	• Overrun error (1) This error occurs if the serial interface starts receiving the next unit of data before reading the UiRB register and receive the bit one before the last stop bit of the next unit of data. • Framing error This error occurs when the set number of stop bits is not detected. • Parity error This error occurs when parity is enabled, and the number of 1's in the parity and character bits do not match the set number of 1's. • Error sum flag This flag is set is set to 1 if an overrun, framing, or parity error occurs.

i = 0 or 1
Note:
1. If an overrun error occurs, the receive data (b0 to b8) in the UiRB register will be undefined. The IR bit in the SiRIC register remains unchanged.

Table 24.6 Registers Used and Settings in UART Mode

Register	Bit	Function
UiTB	b0 to b8	Set transmit data. (1)
UiRB	b0 to b8	Receive data can be read. (2)
	OER, FER, PER, SUM	Error flag
UiBRG	b0 to b7	Set the transfer rate.
UiMR	SMD2 to SMD0	Set to 100b when transfer data is 7 bits long. Set to 101b when transfer data is 8 bits long. Set to 110b when transfer data is 9 bits long.
	CKDIR	Select an internal clock or external clock.
	STPS	Select the stop bit(s).
	PRY, PRYE	Select whether parity is included and whether odd or even.
UiC0	CLK0, CLK1	Select the count source for the UiBRG register.
	TXEPT	Transmit register empty flag
	NCH	Select the output format of the TXDi pin.
	CKPOL	Set to 0.
	UFORM	Select LSB first or MSB first when transfer data is 8 bits long. Set to 0 when transfer data is 7 bits or 9 bits long.
UiC1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	UiIRS	Select the UARTi transmit interrupt source.
	UiRRM	Set to 0.

i = 0 or 1

Notes:

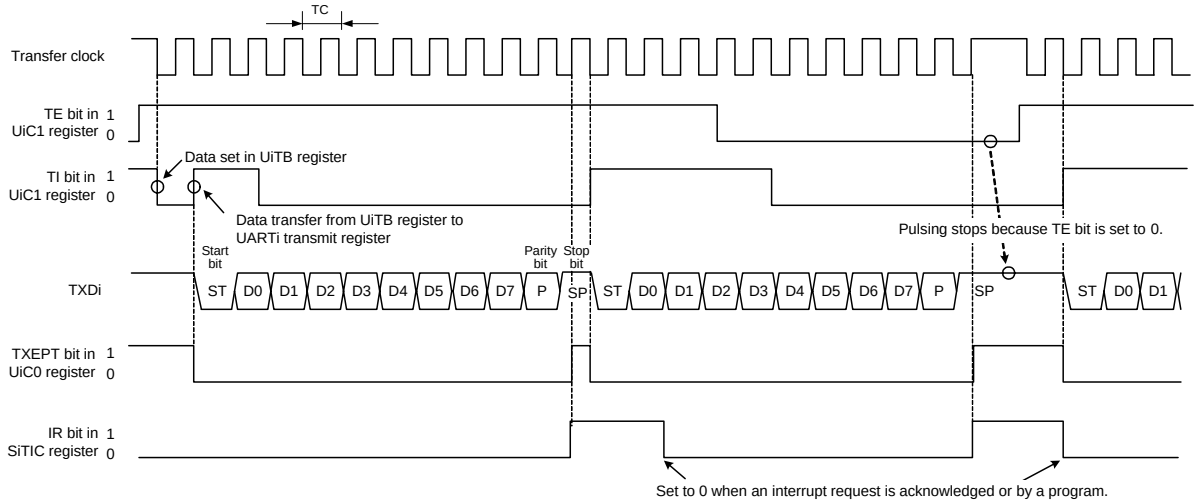
1. The bits used for transmission/receive data are as follows:
   - Bits b0 to b6 when transfer data is 7 bits long
   - Bits b0 to b7 when transfer data is 8 bits long
   - Bits b0 to b8 when transfer data is 9 bits long
2. The contents of the following are undefined:
   - Bits b7 and b8 when the transfer data is 7 bits long
   - Bit b8 when the transfer data is 8 bits long

Table 24.7 lists the I/O Pin Functions in UART Mode.
After the UARTi (i = 0 or 1) operating mode is selected, the TXDi pin outputs a high-level signal until transfer starts. (When the NCH bit is set to 1 (N-channel open-drain output), this pin is in the high-impedance state.)

Table 24.7 I/O Pin Functions in UART Mode

Pin name	Function	Selection Method
TXD0 (P13_1)	Serial data output	TXD0SEL0 bit in U0SR register = 1 For reception only: P13_1 can be used as a port by setting TXD0SEL0 bit = 0.
RXD0 (P13_2)	Serial data input	RXD0SEL0 bit in U0SR register = 1 PD13_2 bit in PD3 register = 0 For transmission only: P13_2 can be used as a port by setting RXD0SEL0 bit = 0.
CLK0 (P13_3)	Programmable I/O port	CLK0SEL0 bit in U0SR register = 0 (CLK0 pin not used)
	Transfer clock input	CLK0SEL0 bit in U0SR register = 1 CKDIR bit in U0MR register = 1 PD13_3 bit in PD3 register = 0
TXD1 (P4_0)	Serial data output	TXD1SEL0 bit in U1SR register = 1 For reception only: P4_0 can be used as a port by setting TXD1SEL0 bit = 0.
RXD1 (P4_1)	Serial data input	RXD1SEL0 bit in U1SR register = 1 PD4_1 bit in PD4 register = 0 For transmission only: P4_1 can be used as a port by setting RXD1SEL0 bit = 0.
CLK1 (P4_2)	Programmable I/O port	CLK1SEL0 bit in U1SR register = 0 (CLK1 pin not used)
	Transfer clock input	CLK1SEL0 bit in U1SR register = 1 CKDIR bit in U1MR register = 0 PD4_2 bit in PD4 register = 0

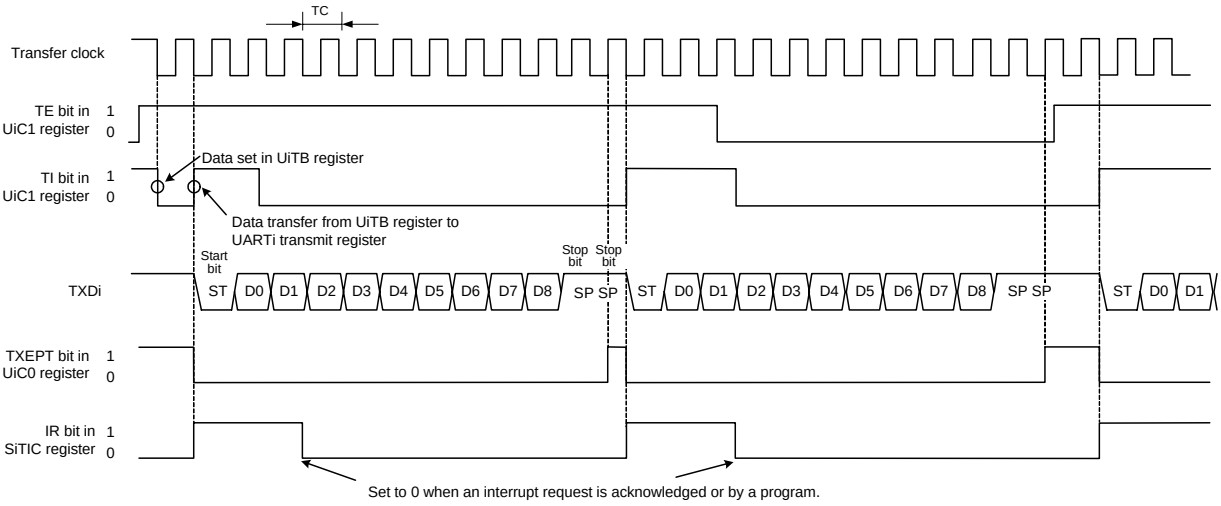
• Transmit Timing Example When Transfer Data 8 Bits is Long (Parity Enabled, One Stop Bit)



The above applies under the following conditions:
- PRYE bit in UiMR register = 1 (parity enabled)
- STPS bit in UiMR register = 0 (one stop bit)
- UiIRS bit in UiC1 register = 1
  (interrupt request generation when transmission is completed)

TC = 16 (n + 1) / fj or 16 (n + 1) / fEXT
fj: Frequency of UiBRG count source (f1, f8, f32, fC)
fEXT: Frequency of UiBRG count source (external clock)
n: Value set in UiBRG register
i = 0 or 1

• Transmit Timing Example When Transfer Data is 9 Bits Long (Parity Disabled, Two Stop Bits)



The above applies under the following conditions:
- PRYE bit in UiMR register = 0 (parity disabled)
- STPS bit in UiMR register = 1 (two stop bits)
- UiIRS bit in UiC1 register = 0
  (interrupt request generation when the transmit buffer is empty)

TC = 16 (n + 1) / fj or 16 (n + 1) / fEXT
fj: Frequency of UiBRG count source (f1, f8, f32, fC)
fEXT: Frequency of UiBRG count source (external clock)
n: Value set in UiBRG register
i = 0 or 1

Figure 24.6 Transmit Timing in UART Mode

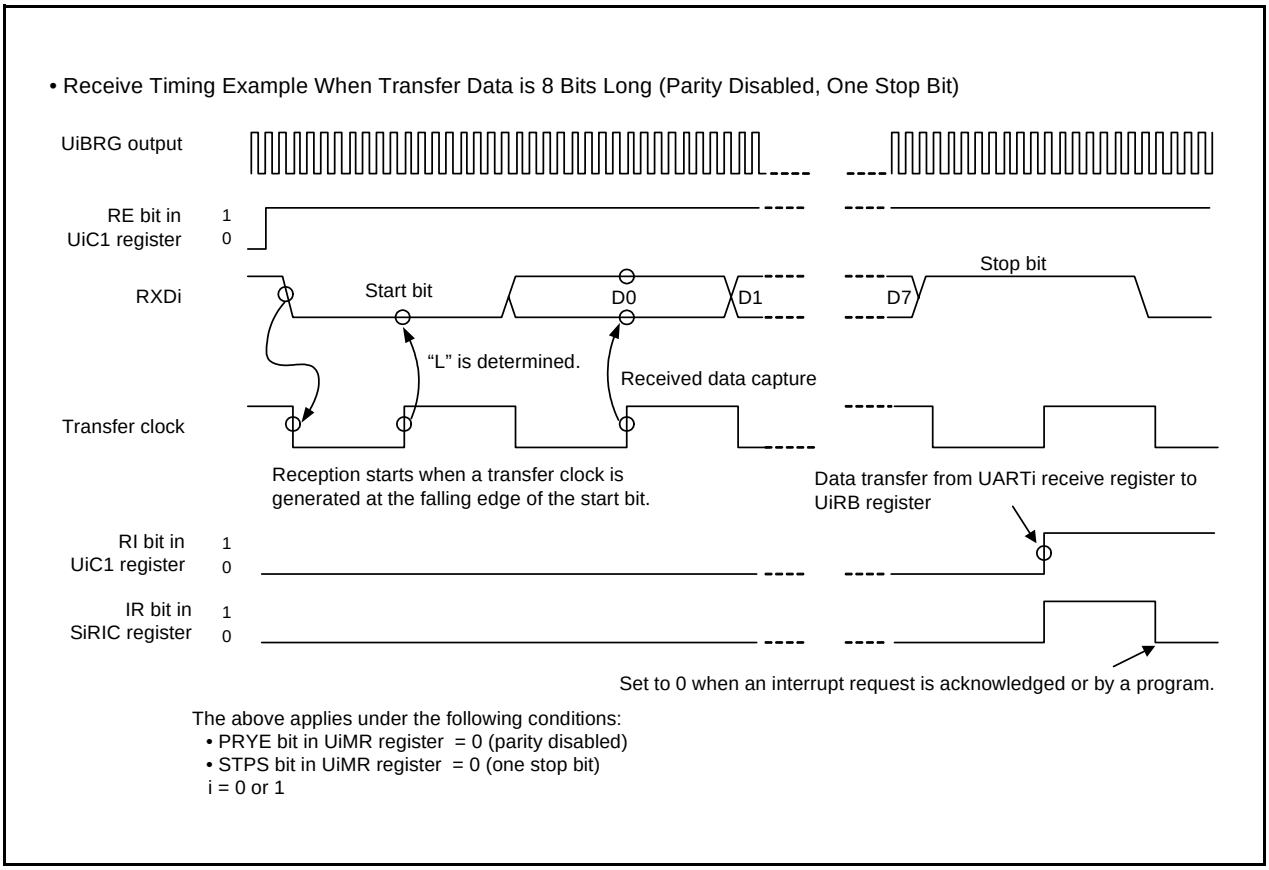


Figure 24.7 Receive Timing in UART Mode

24.4.1 Bit Rate

In UART mode, the bit rate is the frequency (divided by the UiBRG register (i = 0 or 1)) divided by 16.

UART mode

• Internal clock selected

$$\text{Setting value of UiBRG register} = \frac{\text{fj}}{\text{Bit rate} \times 16} - 1$$

fj: Count source frequency of UiBRG register (f1, f8, f32, or fC)

• External clock selected

$$\text{Setting value of UiBRG register} = \frac{\text{fEXT}}{\text{Bit rate} \times 16} - 1$$

fEXT: Count source frequency of UiBRG register (external clock)

i = 0 or 1

Figure 24.8 Formula for Calculating Setting Value of UiBRG Register (i = 0 or 1)

Table 24.8 Bit Rate Setting Example in UART Mode (Internal Clock Selected)

Bit Rate (bps)	UiBRG Count Source	System Clock = 20 MHz			System Clock = 18.432 MHz (1)			System Clock = 8 MHz		
		UiBRG Setting Value	Actual Time (bps)	Setting Error (%)	UiBRG Setting Value	Actual Time (bps)	Setting Error (%)	UiBRG Setting Value	Actual Time (bps)	Setting Error (%)
1200	f8	129 (81h)	1201.92	0.16	119 (77h)	1200.00	0.00	51 (33h)	1201.92	0.16
2400	f8	64 (40h)	2403.85	0.16	59 (3Bh)	2400.00	0.00	25 (19h)	2403.85	0.16
4800	f8	32 (20h)	4734.85	-1.36	29 (1Dh)	4800.00	0.00	12 (0Ch)	4807.69	0.16
9600	f1	129 (81h)	9615.38	0.16	119 (77h)	9600.00	0.00	51 (33h)	9615.38	0.16
14400	f1	86 (56h)	14367.82	-0.22	79 (4Fh)	14400.00	0.00	34 (22h)	14285.71	-0.79
19200	f1	64 (40h)	19230.77	0.16	59 (3Bh)	19200.00	0.00	25 (19h)	19230.77	0.16
28800	f1	42 (2Ah)	29069.77	0.94	39 (27h)	28800.00	0.00	16 (10h)	29411.76	2.12
38400	f1	32 (20h)	37878.79	-1.36	29 (1Dh)	38400.00	0.00	12 (0Ch)	38461.54	0.16
57600	f1	21 (15h)	56818.18	-1.36	19 (13h)	57600.00	0.00	8 (08h)	55555.56	-3.55
115200	f1	10 (0Ah)	113636.36	-1.36	9 (09h)	115200.00	0.00	–	–	–

i = 0 or 1

Note:

1. For the high-speed on-chip oscillator, the correction value of the FRA4 register should be written into the FRA1 register and the correction value of the FRA5 register should be written into the FRA3 register.
   This applies when the high-speed on-chip oscillator is selected as the system clock and bits FRA22 to FRA20 in the FRA2 register are set to 000b (divide-by-2 mode).

24.5 Notes on Serial Interface (UARTi (i = 0 or 1))

- When reading data from the UiRB (i = 0 or 1) register either in clock synchronous serial I/O mode or in clock asynchronous serial I/O mode, always read data in 16-bit units.
  When the high-order byte of the UiRB register is read, bits PER and FER in the UiRB register and the RI bit in the UiC1 register are set to 0.
  To check receive errors, read the UiRB register and then use the read data.

  Program example to read the receive buffer register:
  ```
  MOV.W    00A6H,R0    ; Read the U0RB register
  ```

- When writing data to the UiTB register in clock asynchronous serial I/O mode with 9-bit transfer data length, write data to the high-order byte first and then the low-order byte, in 8-bit units.

  Program example to write to the transmit buffer register:
  ```
  MOV.B    #XXH,00A3H  ; Write to the high-order byte of the U0TB register
  MOV.B    #XXH,00A2H  ; Write to the low-order byte of the U0TB register
  ```

25. Serial Interface (UART2)

The serial interface consists of three channels, UART0 to UART2. This chapter describes UART2.

25.1 Introduction

UART2 has a dedicated timer to generate a transfer clock and operate independently.
Figure 25.1 shows a Block Diagram of UART2. Figure 25.2 shows a Block Diagram of UART2 Transmit/Receive Unit. Table 25.1 lists the UART 2 Pin Configuration.

UART2 supports the following modes:

- Clock synchronous serial I/O mode
- Clock asynchronous serial I/O mode (UART mode)
- Special mode 1 (I^2C mode)
- Multiprocessor communication function

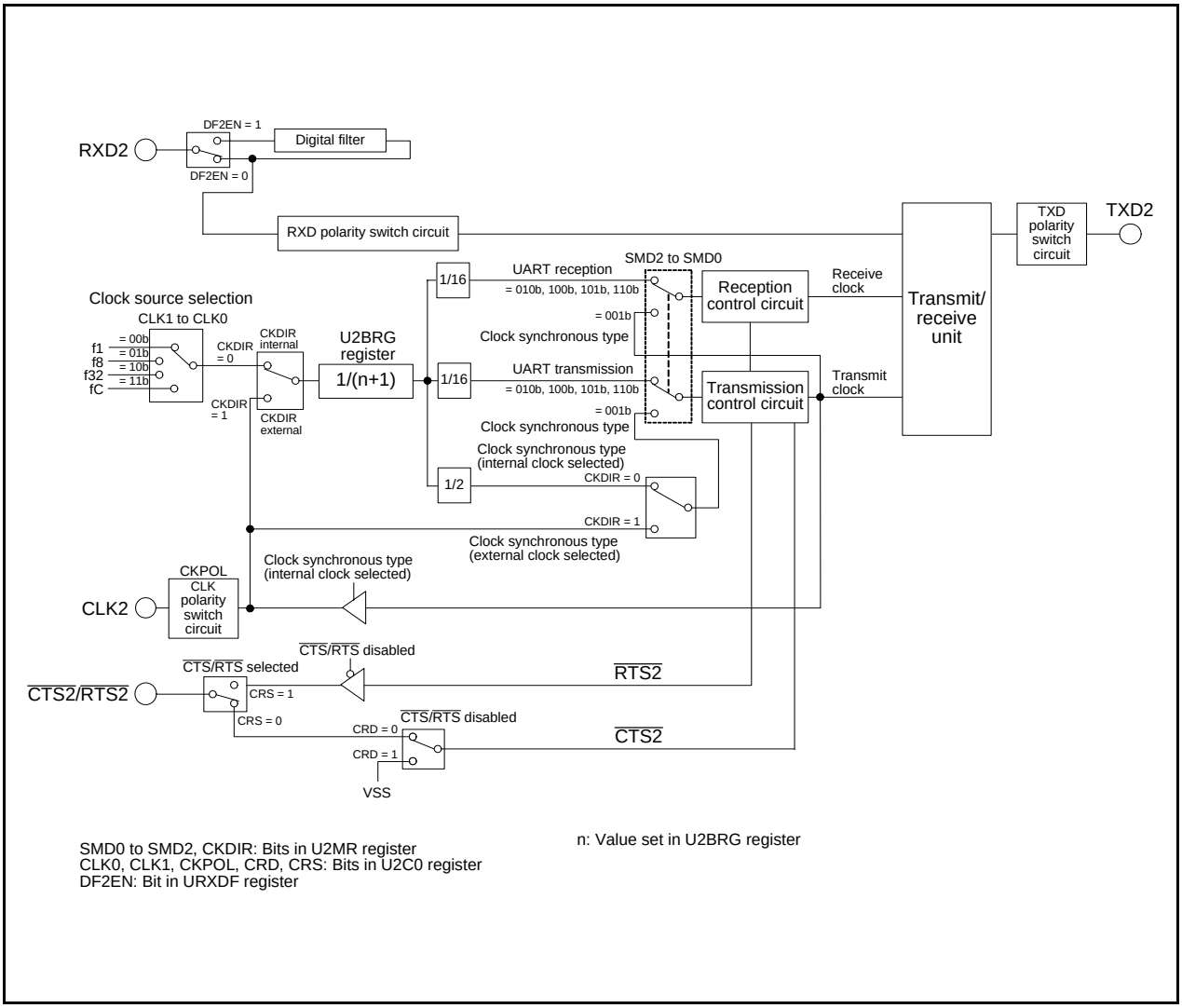


Figure 25.1 Block Diagram of UART2

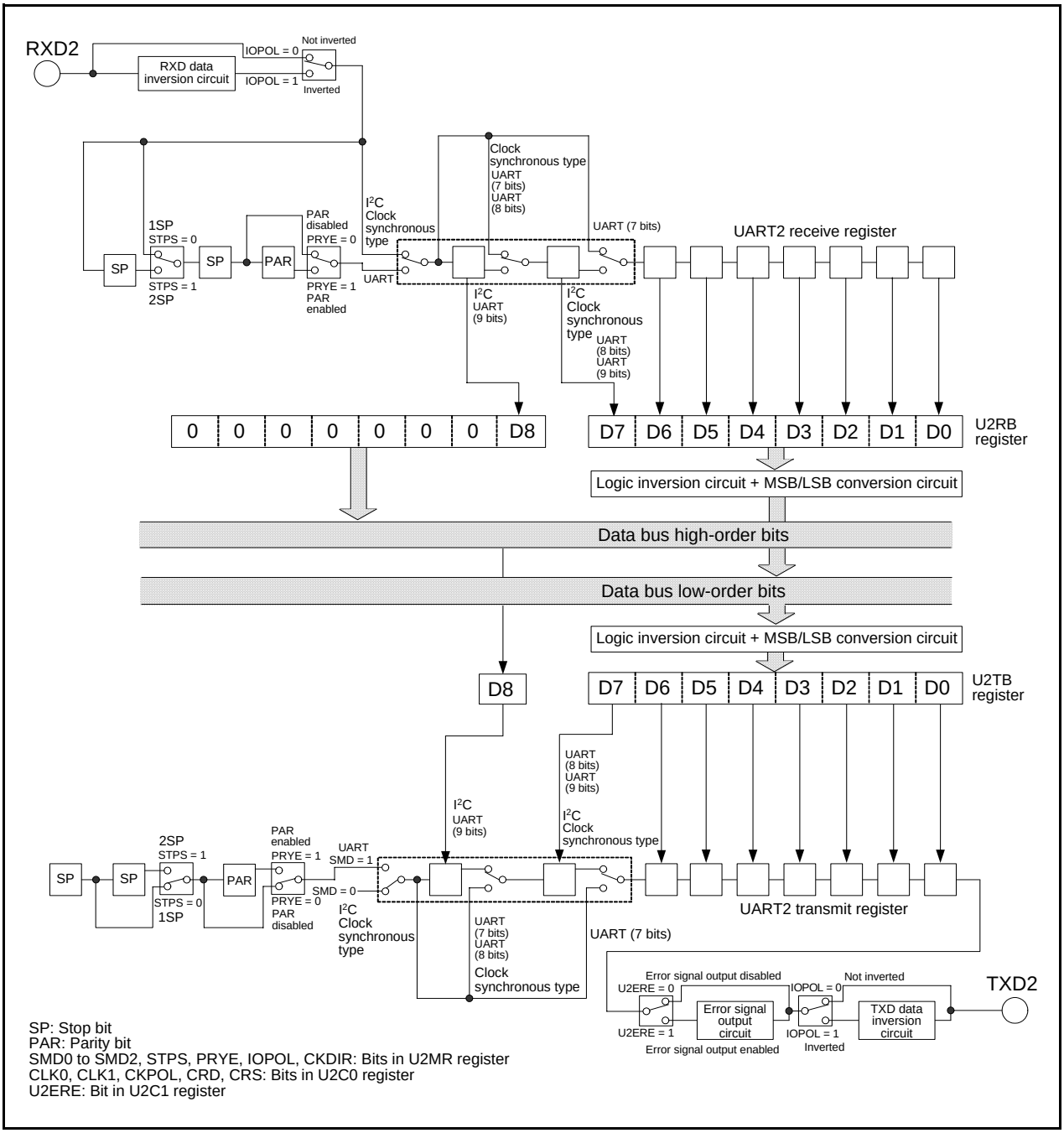


Figure 25.2 Block Diagram of UART2 Transmit/Receive Unit

Table 25.1 UART 2 Pin Configuration

Pin Name	Assigned Pin	I/O	Function
TXD2	P11_1, P11_2	Output	Serial data output
RXD2	P11_1, P11_2	Input	Serial data input
CLK2	P11_0	I/O	Transfer clock I/O
$\overline{\text{CTS2}}$	P11_3	Input	Transmission control input
$\overline{\text{RTS2}}$	P11_3	Output	Reception control input
SCL2	P11_1, P11_2	I/O	I2C mode clock I/O
SDA2	P11_1, P11_2	I/O	I2C mode data I/O

25.2 Registers

25.2.1 UART2 Transmit/Receive Mode Register (U2MR)

Address 00A8h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOPOL	PRYE	PRY	STPS	CKDIR	SMD2	SMD1	SMD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SMD0	Serial I/O mode select bit	b2 b1 b0 0 0 0: Serial interface disabled 0 0 1: Clock synchronous serial I/O mode 0 1 0: I^2C mode 1 0 0: UART mode, transfer data 7 bits long 1 0 1: UART mode, transfer data 8 bits long 1 1 0: UART mode, transfer data 9 bits long Other than above: Do not set.	R/W
b1	SMD1			R/W
b2	SMD2			R/W
b3	CKDIR	Internal/external clock select bit	0: Internal clock 1: External clock	R/W
b4	STPS	Stop bit length select bit	0: One stop bit 1: Two stop bits	R/W
b5	PRY	Odd/even parity select bit	Enabled when PRYE = 1 0: Odd parity 1: Even parity	R/W
b6	PRYE	Parity enable bit	0: Parity disabled 1: Parity enabled	R/W
b7	IOPOL	TXD, RXD I/O polarity switch bit	0: Not inverted 1: Inverted	R/W

25.2.2 UART2 Bit Rate Register (U2BRG)

Address 00A9h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7 to b0	If the setting value is n, U2BRG divides the count source by n+1.	00h to FFh	W

Write to the U2BRG register while transmission and reception stop.
Use the MOV instruction to write to this register.
Set bits CLK1 to CLK0 in the U2C0 register before writing to the U2BRG register.

25.2.3 UART2 Transmit Buffer Register (U2TB)

Address 00ABh to 00AAh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	MPTB
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Function	R/W
b0	—	Transmit data (D7 to D0)	W
b1	—		
b2	—		
b3	—		
b4	—		
b5	—		
b6	—		
b7	—		
b8	MPTB	Transmit data (D8) (1) [When the multiprocessor communication function is not used] Transmit data (D8) [When the multiprocessor communication function is used] • To transfer an ID, set the MPTB bit to 1. • To transfer data, set the MPTB bit to 0.	W
b9	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.	—
b10	—		
b11	—		
b12	—		
b13	—		
b14	—		
b15	—		

Note:
1. Set bits b0 to b7 after setting the MPTB bit.

25.2.4 UART2 Transmit/Receive Control Register 0 (U2C0)

Address 00ACh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	UFORM	CKPOL	NCH	CRD	TXEPT	CRS	CLK1	CLK0
After Reset	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CLK0	U2BRG count source select bit (1)	b1 b0 0 0: f1 selected 0 1: f8 selected 1 0: f32 selected 1 1: fC selected	R/W
b1	CLK1			R/W
b2	CRS	$\overline{\text{CTS}}$/$\overline{\text{RTS}}$ function select bit	Enabled when CRD = 0 0: $\overline{\text{CTS}}$ function selected 1: $\overline{\text{RTS}}$ function selected	R/W
b3	TXEPT	Transmit register empty flag	0: Data in the transmit register (transmission in progress) 1: No data in the transmit register (transmission completed)	R
b4	CRD	$\overline{\text{CTS}}$/$\overline{\text{RTS}}$ disable bit	0: $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ function enabled 1: $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ function disabled	R/W
b5	NCH	Data output select bit	0: Pins TXD2/SDA2, SCL2 set as CMOS output 1: Pins TXD2/SDA2, SCL2 set as N-channel open-drain output	R/W
b6	CKPOL	CLK polarity select bit	0: Transmit data output at the falling edge and receive data input at the rising edge of the transfer clock 1: Transmit data output at the rising edge and receive data input at the falling edge of the transfer clock	R/W
b7	UFORM	Transfer format select bit (2)	0: LSB first 1: MSB first	R/W

Notes:
1. If bits CLK1 to CLK0 are switched, set the U2BRG register again.
2. The UFORM bit is enabled when bits SMD2 to SMD0 in the U2MR register are set to 001b (clock synchronous serial I/O mode), or set to 101b (UART mode, transfer data 8 bits long).
   Set the UFORM bit to 1 when bits SMD2 to SMD0 are set to 010b (I^2C mode), and to 0 when bits SMD2 to SMD0 are set to 100b (UART mode, transfer data 7 bits long) or 110b (UART mode, transfer data 9 bits long).

25.2.5 UART2 Transmit/Receive Control Register 1 (U2C1)

Address 00ADh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	U2ERE	U2LCH	U2RRM	U2IRS	RI	RE	TI	TE
After Reset	0	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	TE	Transmission enable bit	0: Transmission disabled 1: Transmission enabled	R/W
b1	TI	Transmit buffer empty flag	0: Data in the U2TB register 1: No data in the U2TB register	R
b2	RE	Reception enable bit	0: Reception disabled 1: Reception enabled	R/W
b3	RI	Reception complete flag	0: No data in the U2RB register 1: Data in the U2RB register	R
b4	U2IRS	UART2 transmit interrupt source select bit	0: Transmit buffer empty (TI = 1) 1: Transmission completed (TXEPT = 1)	R/W
b5	U2RRM	UART2 continuous receive mode enable bit	0: Continuous receive mode disabled 1: Continuous receive mode enabled	R/W
b6	U2LCH	Data logic select bit (1)	0: Not inverted 1: Inverted	R/W
b7	U2ERE	Error signal output enable bit	0: Output disabled 1: Output enabled	R/W

Note:
1. The U2LCH bit is enabled when bits SMD2 to SMD0 in the U2MR register are set to 001b (clock synchronous serial I/O mode), 100b (UART mode, transfer data 7 bits long), or 101b (UART mode, transfer data 8 bits long). Set the U2LCH bit to 0 when bits SMD2 to SMD0 are set to 010b (I^2C mode) or 110b (UART mode, transfer data 9 bits long).

25.2.6 UART2 Receive Buffer Register (U2RB)

Address 00AFh to 00AEh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	SUM	PER	FER	OER	ABT	—	—	MPRB
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	—	—	Receive data (D7 to D0)	R
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			
b8	MPRB	—	Receive data (D8) (2) [When the multiprocessor communication function is not used] Receive data (D8) [When the multiprocessor communication function is used] • When the MPRB bit is set to 0, received D0 to D7 are data fields. • When the MPRB bit is set to 1, received D0 to D7 are ID fields.	R
b9	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b10	—			
b11	ABT	Arbitration lost detect flag (1)	0: Not detected (won) 1: Detected (lost)	R
b12	OER	Overrun error flag (2)	0: No overrun error 1: Overrun error	R
b13	FER	Framing error flag (2, 3)	0: No framing error 1: Framing error	R
b14	PER	Parity error flag (2, 3)	0: No parity error 1: Parity error	R
b15	SUM	Error sum flag (2, 3)	0: No error 1: Error	R

Notes:
1. The ABT bit is set to 0 by writing 0 by a program. (Writing 1 has no effect.)
2. When bits SMD2 to SMD0 in the U2MR register are set to 000b (serial interface disabled) or the RE bit in the U2C1 register is set to 0 (reception disabled), all of bits SUM, PER, FER, and OER are set to 0 (no error). The SUM bit is set to 0 (no error) when all of bits PER, FER, and OER are set to 0 (no error). Bits PER and FER are set to 0 by reading the lower byte of the U2RB register.
3. These error flags are disabled when bits SMD2 to SMD0 in the U2MR register are set to 001b (clock synchronous serial I/O mode) or to 010b (I^2C mode). When read, the contents are undefined.

25.2.7 UART2 Digital Filter Function Select Register (URXDF)

Address 00B0h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	DF2EN	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	DF2EN	RXD2 digital filter enable bit (1)	0: RXD2 digital filter disabled 1: RXD2 digital filter enabled	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. The RXD2 digital filter can be used only in clock asynchronous serial I/O (UART) mode. When bits SMD2 to SMD0 in the U2MR register are set to 001b (clock synchronous serial I/O mode) or 010b (I^2C mode), set the DF2EN bit to 0 (RXD2 digital filter disabled).

25.2.8 UART2 Special Mode Register 5 (U2SMR5)

Address 00BBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	MPIE	—	—	—	MP
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	MP	Multiprocessor communication enable bit	0: Multiprocessor communication disabled 1: Multiprocessor communication enabled (1)	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—			
b4	MPIE	Multiprocessor communication control bit	When the MP bit is set to 1 (multiprocessor communication enabled), this bit is enabled. When the MPIE bit is set to 1, the following will result: • Receive data in which the multiprocessor bit is 0 is ignored. The settings of the RI bit in the U2C1 register and bits OER and FER in the U2RB register to 1 are disabled. • On receiving receive data in which the multiprocessor bit is 1, the MPIE bit is set to 0 and receive operation other than multiprocessor communication is performed.	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	—			
b7	—	Reserved bit	Set to 0.	R/W

Note:
1. When the MP bit is set to 1 (multiprocessor communication enabled), the settings of bits PRY and PRYE in the U2MR register are disabled. If bits SMD2 to SMD0 in the U2MR register are set to 001b (clock synchronous serial I/O mode), set the MP bit to 0 (multiprocessor communication disabled).

25.2.9 UART2 Special Mode Register 4 (U2SMR4)

Address 00BCh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SWC9	SCLHI	ACKC	ACKD	STSPSEL	STPREQ	RSTAREQ	STAREQ
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	STAREQ	Start condition generate bit (1)	0: Clear 1: Start	R/W
b1	RSTAREQ	Restart condition generate bit (1)	0: Clear 1: Start	R/W
b2	STPREQ	Stop condition generate bit (1)	0: Clear 1: Start	R/W
b3	STSPSEL	SCL, SDA output select bit	0: Start and stop conditions not output 1: Start and stop conditions output	R/W
b4	ACKD	ACK data bit	0: ACK 1: NACK	R/W
b5	ACKC	ACK data output enable bit	0: Serial interface data output 1: ACK data output	R/W
b6	SCLHI	SCL output stop enable bit	0: Disabled 1: Enabled	R/W
b7	SWC9	SCL wait bit 3	0: SCL hold low disabled 1: SCL hold low enabled	R/W

Note:
1. This bit is set to 0 when the condition is generated.

25.2.10 UART2 Special Mode Register 3 (U2SMR3)

Address 00BDh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DL2	DL1	DL0	—	NODC	—	CKPH	—
After Reset	0	0	0	X	0	X	0	X

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b1	CKPH	Clock phase set bit	0: No clock delay 1: With clock delay	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b3	NODC	Clock output select bit	0: CLK2 set as CMOS output 1: CLK2 set as N-channel open-drain output	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b5	DL0	SDA2 digital delay setup bit (1, 2)	b7 b6 b5 0 0 0: No delay 0 0 1: 1 or 2 cycles of U2BRG count source 0 1 0: 2 or 3 cycles of U2BRG count source 0 1 1: 3 or 4 cycles of U2BRG count source 1 0 0: 4 or 5 cycles of U2BRG count source 1 0 1: 5 or6 cycles of U2BRG count source 1 1 0: 6 or 7 cycles of U2BRG count source 1 1 1: 7 or 8 cycles of U2BRG count source	R/W
b6	DL1			R/W
b7	DL2			R/W

Notes:
1. Bits DL2 to DL0 are used to generate a delay in SDA2 output digitally in I^2C mode. In other than I^2C mode, set these bits to 000b (no delay).
2. The amount of delay varies with the load on pins SCL2 and SDA2. When an external clock is used, the amount of delay increases by about 100 ns.

25.2.11 UART2 Special Mode Register 2 (U2SMR2)

Address 00BEh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	SDHI	SWC2	STAC	ALS	SWC	CSC	IICM2
After Reset	X	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IICM2	I²C mode select bit 2	Refer to **Table 25.12 I²C Mode Functions**.	R/W
b1	CSC	Clock synchronization bit	0: Disabled 1: Enabled	R/W
b2	SWC	SCL wait output bit	0: Disabled 1: Enabled	R/W
b3	ALS	SDA output stop bit	0: Disabled 1: Enabled	R/W
b4	STAC	UART2 initialization bit	0: Disabled 1: Enabled	R/W
b5	SWC2	SCL wait output bit 2	0: Transfer clock 1: Low-level output	R/W
b6	SDHI	SDA output disable bit	0: Enabled 1: Disabled (high impedance)	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—

25.2.12 UART2 Special Mode Register (U2SMR)

Address 00BFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	SSS	ACSE	ABSCS	—	BBS	ABC	IICM
After Reset	X	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IICM	I²C mode select bit	0: Other than I²C mode 1: I²C mode	R/W
b1	ABC	Arbitration lost detection flag control bit	0: Update per bit 1: Update per byte	R/W
b2	BBS	Bus busy flag (1)	0: Stop condition detected 1: Start condition detected (busy)	R/W
b3	—	Reserved bit	Set to 0.	R/W
b4	ABSCS	Bus collision detection sampling clock select bit	0: Rising edge of transfer clock 1: Underflow signal of Timer RA (2)	R/W
b5	ACSE	Auto clear function select bit of transmission enable bit	0: No auto clear function 1: Auto clear at bus collision occurrence	R/W
b6	SSS	Transmit start condition select bit	0: Not synchronized to RXD2 1: Synchronized to RXD2 (2)	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—

Notes:
1. The BBS bit is set to 0 by writing 0 by a program (Writing 1 has no effect).
2. When a transfer begins, the SSS bit is set to 0 (not synchronized to RXD2).

25.2.13 UART2 Pin Select Register 0 (U2SR0)

Address 018Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	RXD2SEL1	RXD2SEL0	—	—	TXD2SEL1	TXD2SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TXD2SEL0	TXD2/SDA2 pin select bit	b1 b0 0 0: TXD2/SDA2 pin not used 0 1: P11_2 assigned 1 0: P11_1 assigned 1 1: Do not set.	R/W
b1	TXD2SEL1			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	RXD2SEL0	RXD2/SCL2 pin select bit	b5 b4 0 0: RXD2/SCL2 pin not used 0 1: P11_1 assigned 1 0: P11_2 assigned 1 1: Do not set.	R/W
b5	RXD2SEL1			R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

The U2SR0 register selects which pin is assigned as the UART2 input/output. To use the I/O pins for UART2, set this register.
Set the U2SR0 register before setting the UART2 associated registers. Also, do not change the setting value of this register during UART2 operation.

25.2.14 UART2 Pin Select Register 1 (U2SR1)

Address 018Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	CTS2SEL0	—	—	—	CLK2SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CLK2SEL0	CLK2 pin select bit	0: CLK2 pin not used 1: CLK2 pin used	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—			
b4	CTS2SEL0	$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$ pin select bit	0: $\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$ pin not used 0: $\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$ pin used	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	—			
b7	—			

The U2SR1 register selects which pin is assigned as the UART2 input/output. To use the I/O pins for UART2, set this register.
Set the U2SR1 register before setting the UART2 associated registers. Also, do not change the setting value of this register during UART2 operation.

25.3 Clock Synchronous Serial I/O Mode

In clock synchronous serial I/O mode, data is transmitted and received using a transfer clock.
Table 25.2 lists the Clock Synchronous Serial I/O Mode Specifications. Table 25.3 lists the Registers Used and Settings in Clock Synchronous Serial I/O Mode.

Table 25.2 Clock Synchronous Serial I/O Mode Specifications

Item	Specification
Transfer data format	Transfer data length: 8 bits
Transfer clock	• The CKDIR bit in the U2MR register is set to 0 (internal clock): fj/(2(n+1)) fj = f1, f8, f32, fC n = Value set in U2BRG register: 00h to FFh • The CKDIR bit is set to 1 (external clock): Input from the CLK2 pin
Transmission/reception control	Selectable from the $\overline{\text{CTS}}$ function, $\overline{\text{RTS}}$ function, or $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ function disabled.
Transmit start conditions	To start transmission, the following requirements must be met: (1) • The TE bit in the U2C1 register is set to 1 (transmission enabled) • The TI bit in the U2C1 register is set to 0 (data in the U2TB register) • If the $\overline{\text{CTS}}$ function is selected, input to the $\overline{\text{CTS2}}$ pin is low.
Receive start conditions	To start reception, the following requirements must be met: (1) • The RE bit in the U2C1 register is set to 1 (reception enabled). • The TE bit in the U2C1 register is set to 1 (transmission enabled). • The TI bit in the U2C1 register is set to 0 (data in the U2TB register).
Interrupt request generation timing	For transmission, one of the following conditions can be selected. • The U2IRS bit in the U2C1 register is set to 0 (transmit buffer empty): When data is transferred from the U2TB register to the UART2 transmit register (at start of transmission). • The U2IRS bit is set to 1 (transmission completed): When data transmission from the UART2 transmit register is completed. For reception • When data is transferred from the UART2 receive register to the U2RB register (at completion of reception).
Error detection	Overrun error (2) This error occurs if the serial interface starts receiving the next unit of data before reading the U2RB register and receives the 7th bit of the next unit of data.
Selectable functions	• CLK polarity selection Transfer data I/O can be selected to occur synchronously with the rising or falling edge of the transfer clock. • LSB first, MSB first selection Whether data transmission/reception begins with bit 0 or begins with bit 7 can be selected. • Continuous receive mode selection Receive operation is enabled immediately by reading the U2RB register. • Serial data logic switching This function inverts the logic value of transmit/receive data.

Notes:
1. If an external clock is selected, the requirements must be met in either of the following states:
   - The external clock is held high when the CKPOL bit in the U2C0 register is set to 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)
   - The external clock is held low when the CKPOL bit in the U2C0 register is set to 1 (transmit data output at the rising edge and receive data input at the falling edge of the transfer clock)
2. If an overrun error occurs, the receive data in the U2RB register will be undefined. The IR bit in the S2RIC register does not change to 1 (interrupt requested).

Table 25.3 Registers Used and Settings in Clock Synchronous Serial I/O Mode

Register	Bit	Function
U2TB (1)	b0 to b7	Set transmit data.
U2RB (1)	b0 to b7	Receive data can be read.
	OER	Overrun error flag
U2BRG	b0 to b7	Set the transfer rate.
U2MR (1)	SMD2 to SMD0	Set to 001b.
	CKDIR	Select an internal clock or external clock.
	IOPOL	Set to 0.
U2C0	CLK0, CLK1	Select the count source for the U2BRG register.
	CRS	Select either $\overline{\text{CTS}}$ or $\overline{\text{RTS}}$ to use the function.
	TXEPT	Transmit register empty flag
	CRD	Select the $\overline{\text{CTS}}$ or $\overline{\text{RTS}}$ function enabled or disabled.
	NCH	Select the output format of the TXD2 pin.
	CKPOL	Select the transfer clock polarity.
	UFORM	Select LSB first or MSB first.
U2C1	TE	Set to 1 to enable transmission/reception.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	U2IRS	Select the UART2 transmit interrupt source
	U2RRM	Set to 1 to use continuous receive mode.
	U2LCH	Set to 1 to use inverted data logic.
	U2ERE	Set to 0.
U2SMR	b0 to b7	Set to 0.
U2SMR2	b0 to b7	Set to 0.
U2SMR3	b0 to b2	Set to 0.
	NODC	Select the clock output format.
	b4 to b7	Set to 0.
U2SMR4	b0 to b7	Set to 0.
URXDF	DF2EN	Set to 0.
U2SMR5	MP	Set to 0.

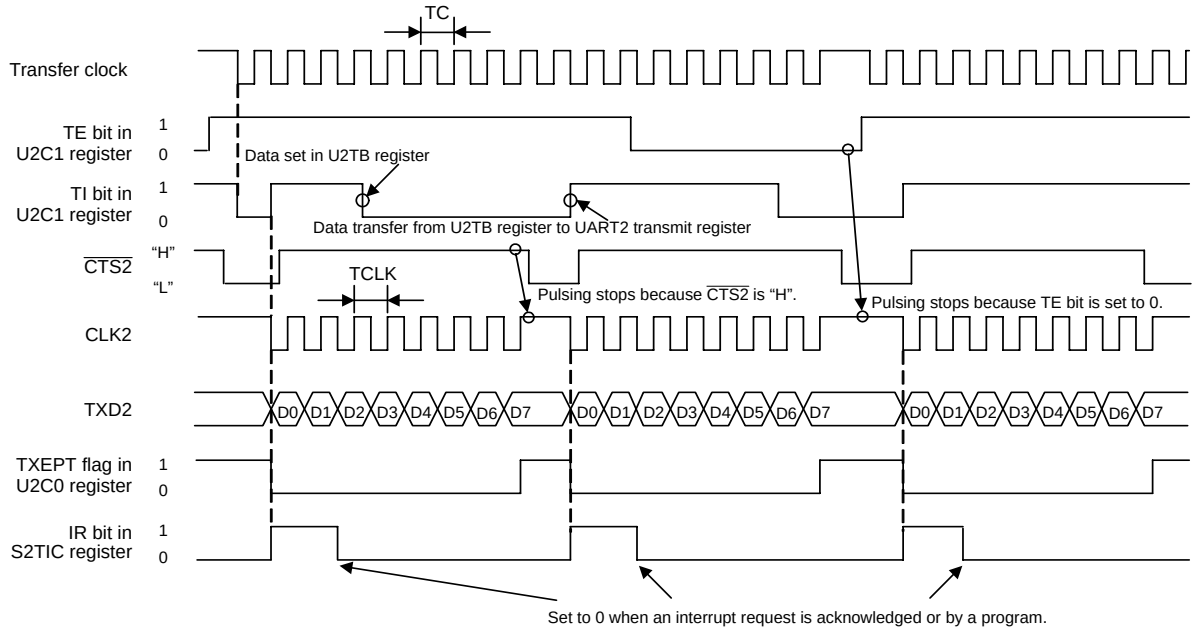
Note:
1. Set the bits not listed in this table to 0 when writing to the above registers in clock synchronous serial I/O mode.

Table 25.4 lists the Pin Functions in Clock Synchronous Serial I/O Mode (Multiple Transfer Clock Output Pin Function Not Selected).
After UART2 operating mode is selected, the TXD2 pin outputs a high-level signal until transfer starts.
(When N-channel open-drain output is selected, this pin is in the high-impedance state.)
Figure 25.3 shows the Transmit and Receive Timing in Clock Synchronous Serial I/O Mode.

Table 25.4 Pin Functions in Clock Synchronous Serial I/O Mode (Multiple Transfer Clock Output Pin Function Not Selected)

Pin Name	Function	Selection Method
TXD2 (P11_1 or P11_2)	Serial data output	• When TXD2 (P11_1) Bits TXD2SEL1 to TXD2SEL0 in U2SR0 register = 10b (P11_1) • When TXD2 (P11_2) Bits TXD2SEL1 to TXD2SEL0 in U2SR0 register = 01b (P11_2) • For reception only: P11_1 and P11_2 can be used as ports by setting TXD2SEL1 to TXD2SEL0 to 00b.
RXD2 (P11_1 or P11_2)	Serial data input	• When RXD2 (P11_1) Bits RXD2SEL1 to RXD2SEL0 in U2SR0 register = 01b (P11_1) PD11_1 bit in PD11 register = 0 • When RXD2 (P11_2) Bits RXD2SEL1 to RXD2SEL0 in U2SR0 register = 10b (P11_2) PD11_2 bit in PD11 register = 0 • For transmission only: P11_1 and P11_2 can be used as ports by setting RXD2SEL1 to RXD2SEL0 to 00b.
CLK2 (P11_0)	Transfer clock output	CLK2SEL0 bit in U2SR1 register = 1 CKDIR bit in U2MR register = 0
	Transfer clock input	CLK2SEL0 bit in U2SR1 register = 1 CKDIR bit in U2MR register = 1 PD11_0 bit in PD11 register = 0
$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$ (P11_3)	$\overline{\text{CTS}}$ input	CTS2SEL0 bit in U2SR1 register = 1 CRD bit in U2C0 register = 0 CRS bit in U2C0 register = 0 PD11_3 bit in PD11 register = 0
	$\overline{\text{RTS}}$ output	CTS2SEL0 bit in U2SR1 register = 1 CRD bit in U2C0 register = 0 CRS bit in U2C0 register = 1
	I/O port	CTS2SEL0 bit in U2SR1 register = 0

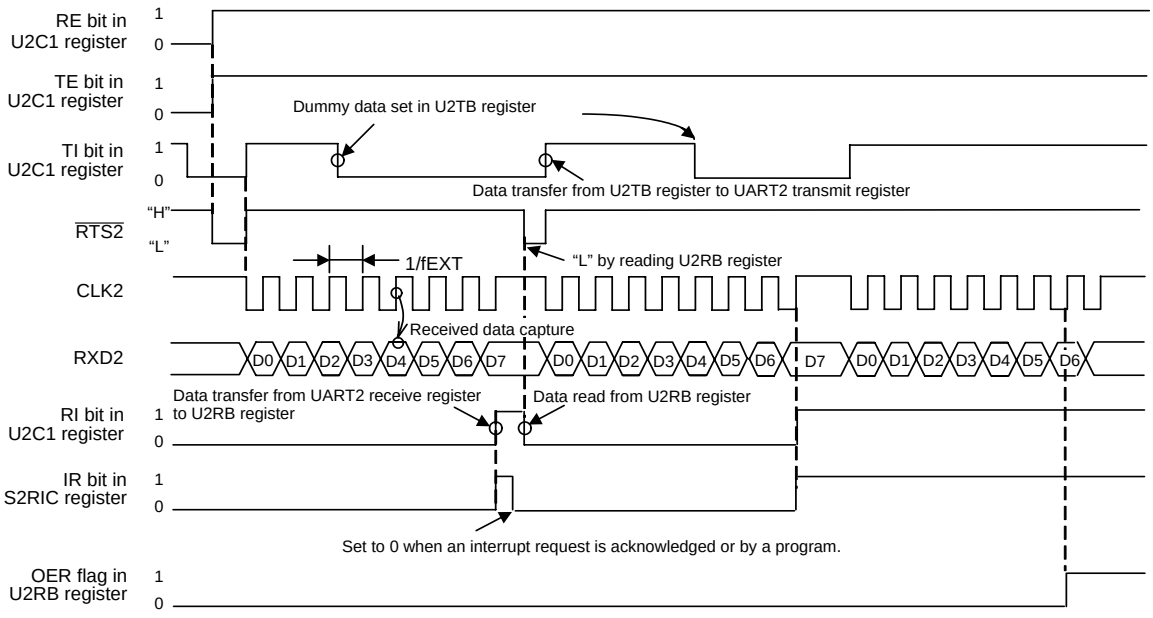
(1) Transmit Timing Example (Internal Clock Selected)



The above applies under the following conditions:
- CKDIR bit in U2MR register = 0 (internal clock)
- CRD bit in U2C0 register = 0 (CTS/RTS function enabled), CRS bit = 0 (CTS function selected)
- CKPOL bit in U2C0 register = 0
  (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)
- U2IRS bit in U2C1 register = 0 (interrupt request generation when the U2TB register is empty)

TC = TCLK = 2(n+1)/fj
fj: Frequency of U2BRG count source
(f1, f8, f32, fC)
n: Value set in U2BRG register

(2) Receive Timing Example (External Clock Selected)



The above applies under the following conditions:
- CKDIR bit in U2MR register = 1 (external clock)
- CRD bit in U2C0 register = 0 (CTS/RTS function enabled), CRS bit = 1 (RTS function selected)
- CKPOL bit in U2C0 register = 0
  (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)

fEXT: Frequency of external clock

Make sure the following conditions are met when the CLK2 pin input is high before receiving data:
- TE bit in U2C0 register = 1 (transmission enabled)
- RE bit in U2C1 register = 1 (reception enabled)
- Dummy data write to the U2TB register

Figure 25.3 Transmit and Receive Timing in Clock Synchronous Serial I/O Mode

25.3.1 Measure for Dealing with Communication Errors

If a communication error occurs while transmitting or receiving in clock synchronous serial I/O mode, follow the procedures below:

• Resetting the U2RB register
(1) Set the RE bit in the U2C1 register to 0 (reception disabled).
(2) Set bits SMD2 to SMD0 in the U2MR register to 000b (serial interface disabled).
(3) Set bits SMD2 to SMD0 in the U2MR register to 001b (clock synchronous serial I/O mode).
(4) Set the RE bit in the U2C1 register to 1 (reception enabled).

• Resetting the U2TB register
(1) Set bits SMD2 to SMD0 in the U2MR register to 000b (serial interface disabled).
(2) Set bits SMD2 to SMD0 in the U2MR register to 001b (clock synchronous serial I/O mode).
(3) Write 1 to the TE bit in the U2C1 register (transmission enabled), regardless of the TE bit value of the U2C2 register.

25.3.2 CLK Polarity Select Function

The CKPOL bit in the U2C0 register can be used to select the transfer clock polarity. Figure 25.4 shows the Transfer Clock Polarity.

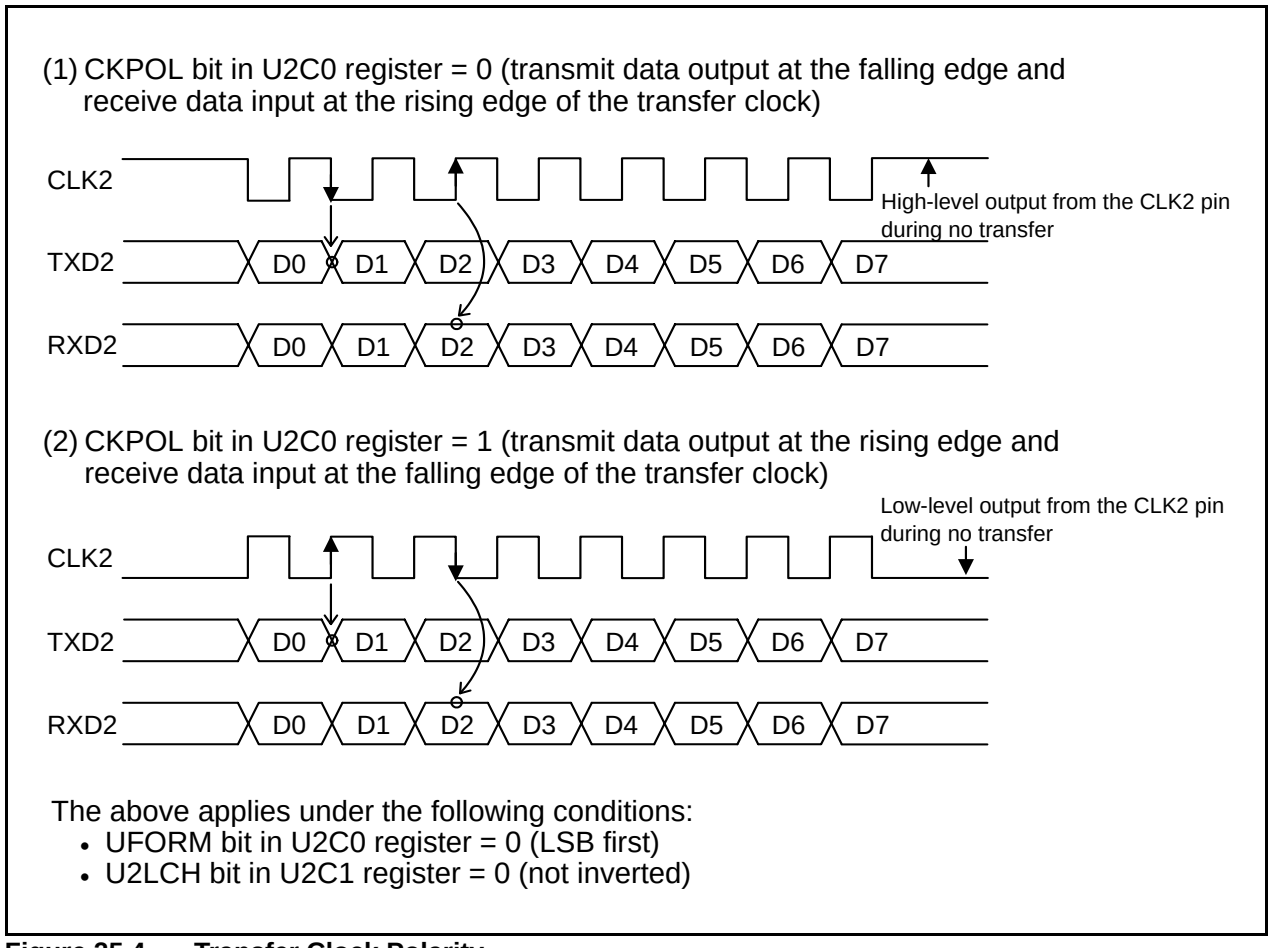


Figure 25.4 Transfer Clock Polarity

25.3.3 LSB First/MSB First Select Function

The UFORM bit in the U2C0 register can be used to select the transfer format. Figure 25.5 shows the Transfer Format.

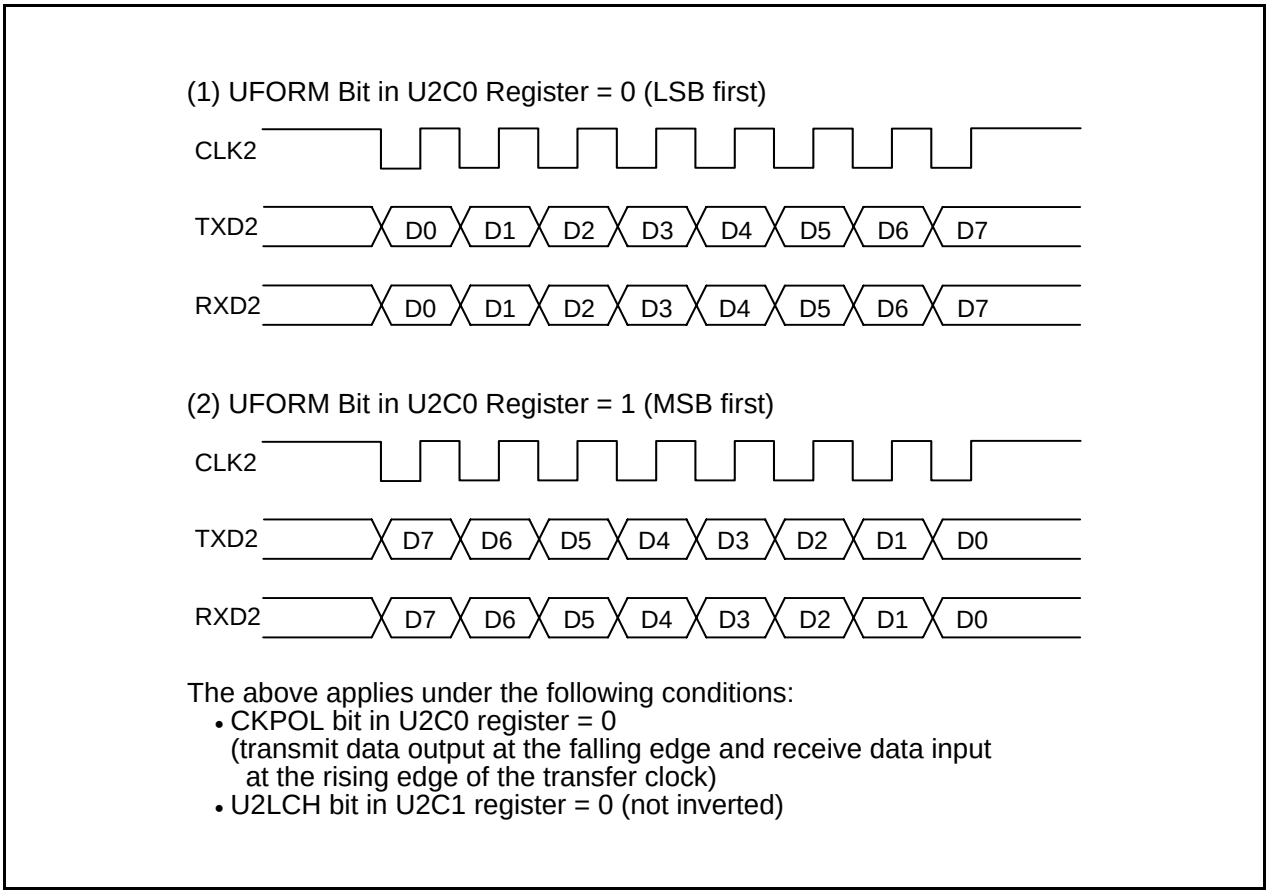


Figure 25.5 Transfer Format

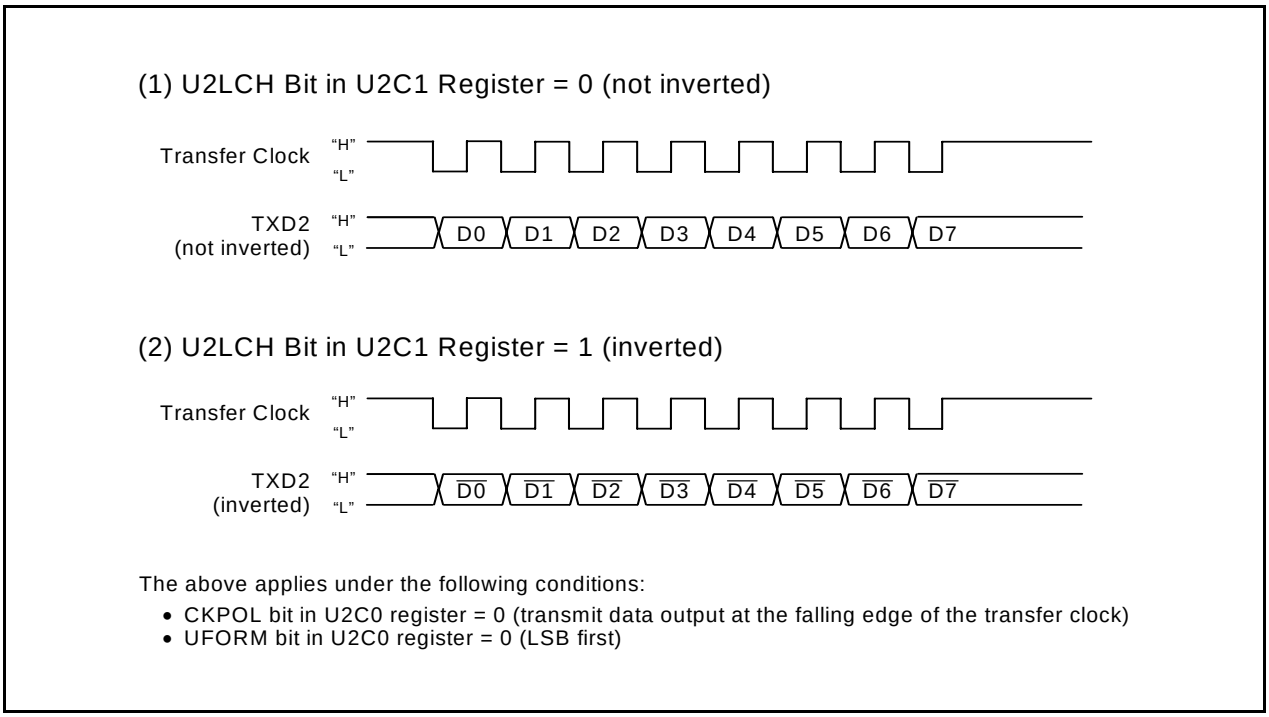
25.3.4 Continuous Receive Mode

In continuous receive mode, receive operation is enabled by reading the receive buffer register. If this mode is selected, writing dummy data to the transmit buffer register is not required to enable receive operation. However, a dummy reading of the receive buffer register is required when starting transmission.

When the U2RRM bit in the U2C1 register is set to 1 (continuous receive mode), the TI bit in the U2C1 register is set to 0 (data in the U2TB register) by reading the U2RB register. When the U2RRM bit is set to 1, do not write dummy data to the U2TB register by a program.

25.3.5 Serial Data Logic Switching Function

When the U2LCH bit in the U2C1 register is set to 1 (inverted), the data written to the U2TB register has its logic inverted before being transmitted. Similarly, the received data has its logic inverted when read from the U2RB register. Figure 25.6 shows the Serial Data Logic Switching.



The above applies under the following conditions:

- CKPOL bit in U2C0 register = 0 (transmit data output at the falling edge of the transfer clock)
- UFORM bit in U2C0 register = 0 (LSB first)

Figure 25.6 Serial Data Logic Switching

25.3.6 $\overline{\text{CTS}}/\overline{\text{RTS}}$ Function

The $\overline{\text{CTS}}$ function is used to start transmit and receive operation when a low-level signal is applied to the $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin. Transmit and receive operation begins when the $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin is held low. If the input level is switched to high during a transmit or receive operation, the operation stops before the next data.
For the $\overline{\text{RTS}}$ function, the $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin outputs a low-level signal when the MCU is ready for a receive operation. The output level goes high at the first falling edge of the CLK2 pin.

- The CRD bit in the U2C0 register = 1 ($\overline{\text{CTS}}/\overline{\text{RTS}}$ function disabled)
  The $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin operates as the programmable I/O function.
- The CRD bit = 0, CRS bit = 0 ($\overline{\text{CTS}}$ function selected)
  The $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin operates as the $\overline{\text{CTS}}$ function.
- The CRD bit = 0, CRS bit = 1 ($\overline{\text{RTS}}$ function selected)
  The $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin operates as the $\overline{\text{RTS}}$ function.

25.4 Clock Asynchronous Serial I/O (UART) Mode

In UART mode, data is transmitted and received after setting the desired transfer rate and transfer data format. Table 25.5 lists the UART Mode Specifications. Table 25.6 lists the Registers Used and Settings in UART Mode.

Table 25.5 UART Mode Specifications

Item	Specification
Transfer data format	• Character bits (transfer data): Selectable from 7, 8, or 9 bits • Start bit:1 bit • Parity bit: Selectable from odd, even, or none • Stop bits: Selectable from 1 bit or 2 bits
Transfer clock	• The CKDIR bit in the U2MR register is set to 0 (internal clock): fj/(16(n + 1)) fj = f1, f8, f32, fC n = Value set in U2BRG register: 00h to FFh • The CKDIR bit is set to 1 (external clock): fEXT/(16(n + 1)) fEXT: Input from CLK2 pin n: Value set in U2BRG register: 00h to FFh
Transmission/reception control	Selectable from the $\overline{\text{CTS}}$ function, $\overline{\text{RTS}}$ function, or $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ function disabled.
Transmit start conditions	To start transmission, the following requirements must be met: • The TE bit in the U2C1 register is set to 1 (transmission enabled). • The TI bit in the U2C1 register is set to 0 (data in the U2TB register). • If the $\overline{\text{CTS}}$ function is selected, input to the $\overline{\text{CTS2}}$ pin is low.
Receive start conditions	To start reception, the following requirements must be met: • The RE bit in the U2C1 register is set to 1 (reception enabled). • Start bit detection
Interrupt request generation timing	For transmission, one of the following conditions can be selected. • The U2IRS bit in the U2C1 register is set to 0 (transmit buffer empty): When data is transferred from the U2TB register to the UART2 transmit register (at start of transmission). • The U2IRS bit is set to 1 (transmission completed): When data transmission from the UART2 transmit register is completed. For reception • When data is transferred from the UART2 receive register to the U2RB register (at completion of reception).
Error detection	• Overrun error (1) This error occurs if the serial interface starts receiving the next unit of data before reading the U2RB register and receives the bit one before the last stop bit of the next unit of data. • Framing error (2) This error occurs when the set number of stop bits is not detected. • Parity error (2) This error occurs when if parity is enabled, the number of 1's in the parity and character bits does not match the set number of 1's. • Error sum flag This flag is set to 1 if an overrun, framing, or parity error occurs.
Selectable functions	• LSB first, MSB first selection Whether data transmission/reception begins with bit 0 or begins with bit 7 can be selected. • Serial data logic switching This function inverts the logic of transmit/receive data. Start and stop bits are not inverted. • TXD, RXD I/O polarity switching This function inverts the polarities of the TXD pin output and RXD pin input. The logic levels of all I/O data are inverted. • RAD2 digital filter selection The digital filter for the RXD2 input signal can be enabled or disabled.

Notes:
1. If an overrun error occurs, the receive data in the U2RB register will be undefined. The IR bit in the S2RIC register remains unchanged.
2. The timing at which the framing error flag and the parity error flag are set is detected when data is transferred from the UART2 receive register to the U2RB register.

Table 25.6 Registers Used and Settings in UART Mode

Register	Bit	Function
U2TB	b0 to b8	Set transmit data. (1)
U2RB	b0 to b8	Receive data can be read. (1, 2)
	OER, FER, PER, SUM	Error flag
U2BRG	b0 to b7	Set the transfer rate.
U2MR	SMD2 to SMD0	Set to 100b when transfer data is 7 bits long. Set to 101b when transfer data is 8 bits long. Set to 110b when transfer data is 9 bits long.
	CKDIR	Select an internal clock or external clock.
	STPS	Select the stop bit(s).
	PRY, PRYE	Select whether parity is included and whether odd or even.
	IOPOL	Select the polarities of the TXD/RXD input/output.
U2C0	CLK0, CLK1	Select the count source for the U2BRG register.
	CRS	Select $\overline{\text{CTS}}$ or $\overline{\text{RTS}}$ to use the function.
	TXEPT	Transmit register empty flag
	CRD	Select the $\overline{\text{CTS}}$ or $\overline{\text{RTS}}$ function enabled or disabled.
	NCH	Select the output format of the TXD2 pin.
	CKPOL	Set to 0.
	UFORM	Select LSB first or MSB first when transfer data is 8 bits long. Set to 0 when transfer data is 7 or 9 bits long.
U2C1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	U2IRS	Select the UART2 transmit interrupt source.
	U2RRM	Set to 0.
	U2LCH	Set to 1 to use inverted data logic.
	U2ERE	Set to 0.
U2SMR	b0 to b7	Set to 0.
U2SMR2	b0 to b7	Set to 0.
U2SMR3	b0 to b7	Set to 0.
U2SMR4	b0 to b7	Set to 0.
URXDF	DF2EN	Select the digital filter disabled or enabled.
U2SMR5	MP	Set to 0.

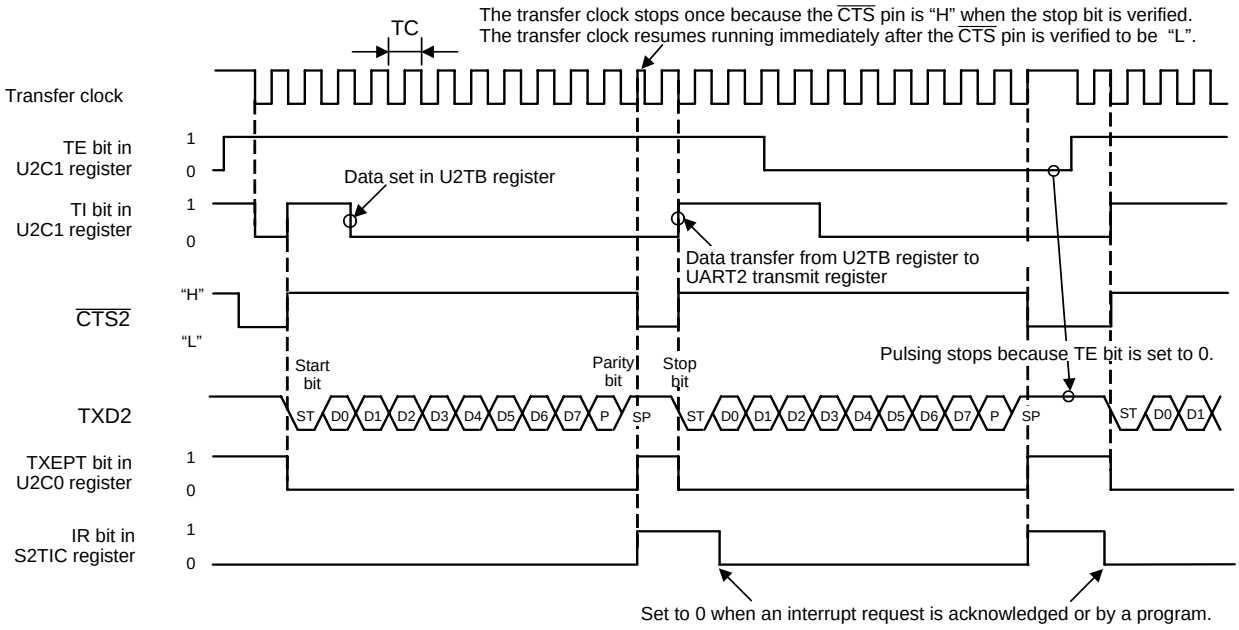
Notes:
1. The bits used for transmit/receive data are as follows:
   - Bits b0 to b6 when transfer data is 7 bits long
   - Bits b0 to b7 when transfer data is 8 bits long
   - Bits b0 to b8 when transfer data is 9 bits long
2. The contents of the following are undefined:
   - Bits b7 and b8 when transfer data is 7 bits long
   - Bit b8 when transfer data is 8 bits long

Table 25.7 lists the I/O Pin Functions in UART Mode.
After UART2 operating mode is selected, the TXD2 pin outputs a high-level signal until transfer starts. (When N-channel open-drain output is selected, this pin is in the high-impedance state.)
Figure 25.7 shows the Transmit Timing in UART Mode. Figure 25.8 shows the Receive Timing in UART Mode.

Table 25.7 I/O Pin Functions in UART Mode

Pin Name	Function	Selection Method
TXD2 (P11_1 or P11_2)	Serial data output	• When TXD2 (P11_1) Bits TXD2SEL1 to TXD2SEL0 in U2SR0 register = 10b (P11_1) • When TXD2 (P11_2) Bits TXD2SEL1 to TXD2SEL0 in U2SR0 register = 01b (P11_2) • For reception only: P11_1 and P11_2 can be used as ports by setting TXD2SEL1 to TXD2SEL0 to 00b.
RXD2 (P11_1 or P11_2)	Serial data input	• When RXD2 (P11_1) Bits RXD2SEL1 to RXD2SEL0 in U2SR0 register = 01b (P11_1) • When RXD2 (P11_2) Bits RXD2SEL1 to RXD2SEL0 in U2SR0 register = 10b (P11_2) PD11_2 bit in PD11 register = 0 • For transmission only: P11_1 and P11_2 can be used as ports by setting RXD2SEL1 to RXD2SEL0 to 00b.
CLK2 (P11_0)	I/O port	CLK2SEL0 bit in U2SR1 register = 0
	Transfer clock input	CLK2SEL0 bit in U2SR1 register = 1 CKDIR bit in U2MR register = 1 PD11_0 bit in PD11 register = 0
$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$ (P11_3)	$\overline{\text{CTS}}$ input	CTS2SEL0 bit in U2SR1 register = 1 CRD bit in U2C0 register = 0 CRS bit in U2C0 register = 0 PD11_3 bit in PD11 register = 0
	$\overline{\text{RTS}}$ output	CTS2SEL0 bit in U2SR1 register = 1 CRD bit in U2C0 register = 0 CRS bit in U2C0 register = 1
	I/O port	CTS2SEL0 bit in U2SR1 register = 0

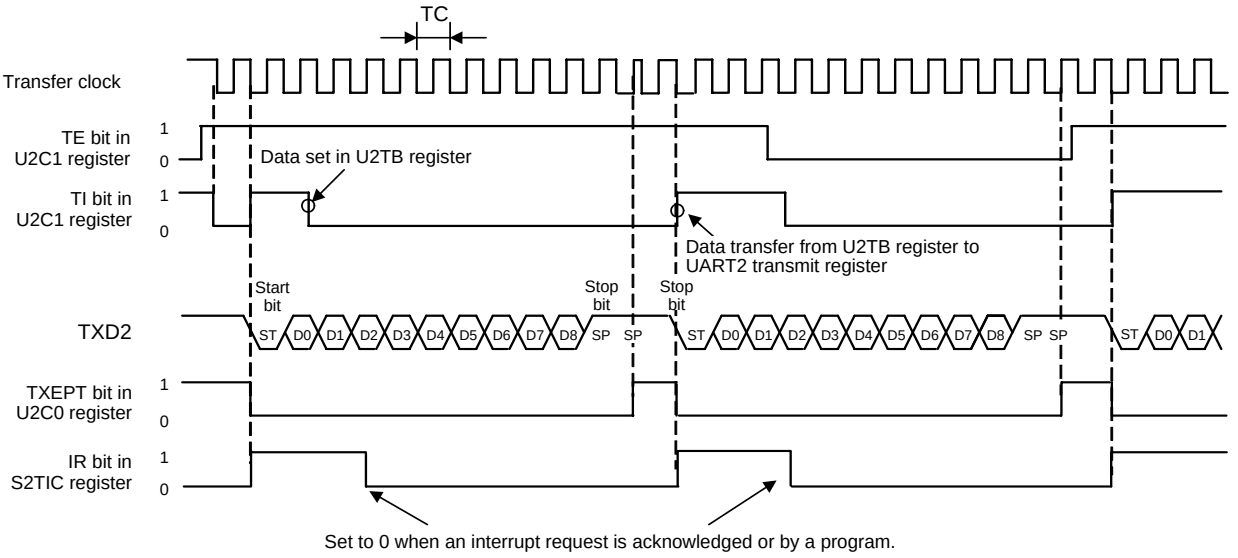
(1) Transmit Timing Example When Transfer Data 8 Bits is Long (Parity Enabled, One Stop Bit)



The above applies under the following conditions:
- PRYE bit in U2MR register = 1 (parity enabled)
- STPS bit in U2MR register = 0 (one stop bit)
- CRD bit in U2C0 register = 0 (CTS/RTS function enabled), CRS bit = 0 (CTS function selected)
- U2IRS bit in U2C1 register = 1 (interrupt request generation when transmission is completed)

TC = 16(n + 1)/fj or 16(n + 1)/fEXT
fj: Frequency of U2BRG count source (f1, f8, f32, fC)
fEXT: Frequency of U2BRG count source (external clock)
n: Value set in U2BRG register

(2) Transmit Timing Example When Transfer Data 9 Bits is Long (Parity Disabled, Two Stop Bits)



The above applies under the following conditions:
- PRYE bit in U2MR register = 0 (parity disabled)
- STPS bit in U2MR register = 1 (two stop bits)
- CRD bit in U2C0 register = 1 (CTS/RTS function disabled)
- U2IRS bit in U2C1 register = 0 (interrupt request generation when the transmit buffer is empty)

TC = 16(n + 1)/fj or 16(n + 1)/fEXT
fj: Frequency of U2BRG count source (f1, f8, f32, fC)
fEXT: Frequency of U2BRG count source (external clock)
n: Value set in U2BRG register

Figure 25.7 Transmit Timing in UART Mode

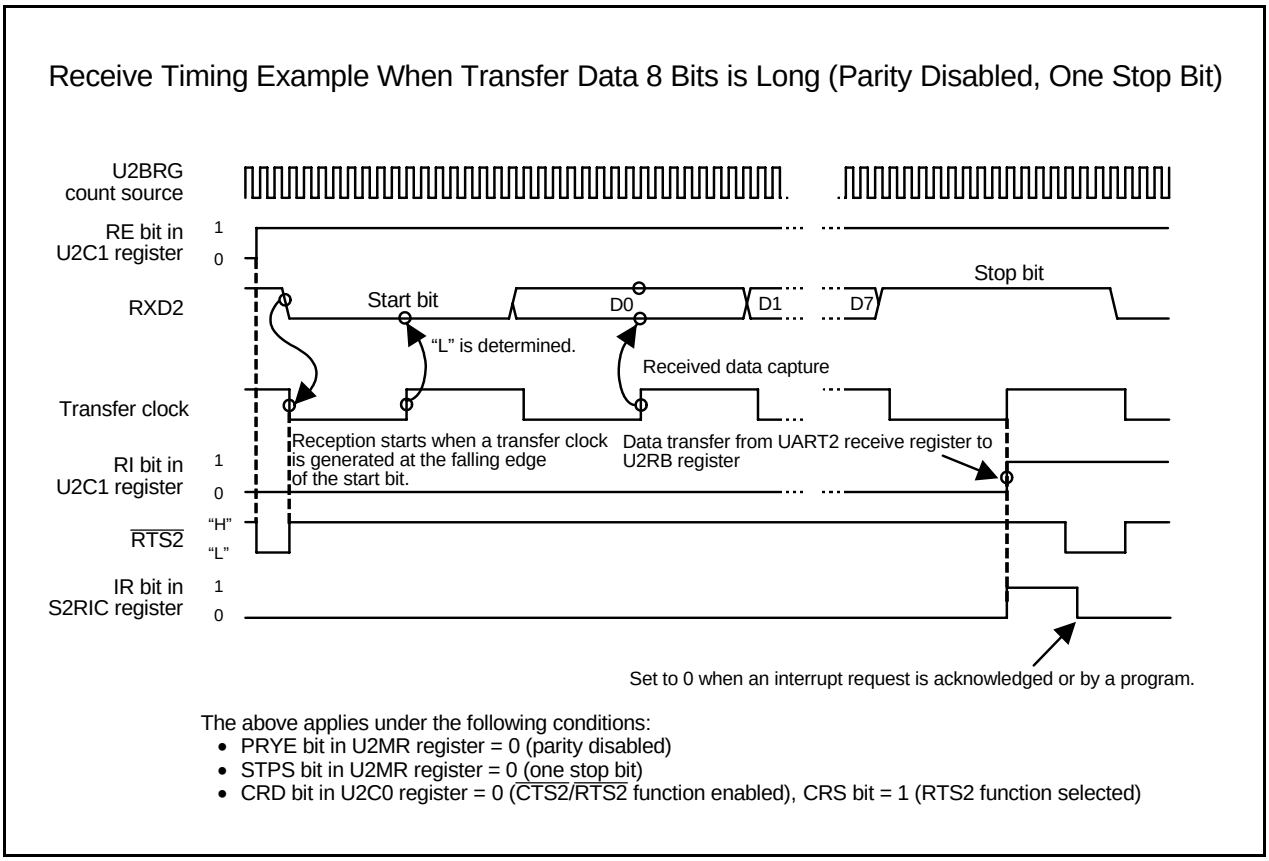


Figure 25.8 Receive Timing in UART Mode

25.4.1 Bit Rate

In UART mode, the bit rate is the frequency divided by the U2BRG register divided by 16. Table 25.8 lists the Bit Rate Setting Example in UART Mode (Internal Clock Selected).

Table 25.8 Bit Rate Setting Example in UART Mode (Internal Clock Selected)

Bit Rate (bps)	U2BRG Count Source	System Clock = 20 MHz			System Clock = 18.432 MHz (1)			System Clock = 8 MHz		
		U2BRG Setting Value	Actual Time (bps)	Setting Error (%)	U2BRG Setting Value	Actual Time (bps)	Setting Error (%)	U2BRG Setting Value	Actual Time (bps)	Setting Error (%)
1200	f8	129 (81h)	1201.92	0.16	119 (77h)	1200.00	0.00	51 (33h)	1201.92	0.16
2400	f8	64 (40h)	2403.85	0.16	59 (3Bh)	2400.00	0.00	25 (19h)	2403.85	0.16
4800	f8	32 (20h)	4734.85	-1.36	29 (1Dh)	4800.00	0.00	12 (0Ch)	4807.69	0.16
9600	f1	129 (81h)	9615.38	0.16	119 (77h)	9600.00	0.00	51 (33h)	9615.38	0.16
14400	f1	86 (56h)	14367.82	-0.22	79 (4Fh)	14400.00	0.00	34 (22h)	14285.71	-0.79
19200	f1	64 (40h)	19230.77	0.16	59 (3Bh)	19200.00	0.00	25 (19h)	19230.77	0.16
28800	f1	42 (2Ah)	29069.77	0.94	39 (27h)	28800.00	0.00	16 (10h)	29411.76	2.12
38400	f1	32 (20h)	37878.79	-1.36	29 (1Dh)	38400.00	0.00	12 (0Ch)	38461.54	0.16
57600	f1	21 (15h)	56818.18	-1.36	19 (13h)	57600.00	0.00	8 (08h)	55555.56	-3.55
115200	f1	10 (0Ah)	113636.36	-1.36	9 (09h)	115200.00	0.00	–	–	–

Note:
1. For the high-speed on-chip oscillator, the correction value of the FRA4 register should be written into the FRA1 register and the correction value of the FRA5 register should be written into the FRA3 register.
This applies when the high-speed on-chip oscillator is selected as the system clock and bits FRA22 to FRA20 in the FRA2 register are set to 000b (divide-by-2 mode).

25.4.2 Measure for Dealing with Communication Errors

If a communication error occurs while transmitting or receiving in UART mode, follow the procedures below:

• Resetting the U2RB register
(1) Set the RE bit in the U2C1 register to 0 (reception disabled).
(2) Set the RE bit in the U2C1 register to 1 (reception enabled).

• Resetting the U2TB register
(1) Set bits SMD2 to SMD0 in the U2MR register to 000b (serial interface disabled).
(2) Reset bits SMD2 to SMD0 in the U2MR register to 001b, 101b, and 110b.
(3) Write 1 to the TE bit in the U2C1 register (transmission enabled), regardless of the TE bit value of the U2C1 register.

25.4.3 LSB First/MSB First Select Function

As shown in Figure 25.9, the UFORM bit in the U2C0 register can be used to select the transfer format. This function is enabled when transfer data is 8 bits long. Figure 25.9 shows the Transfer Format.

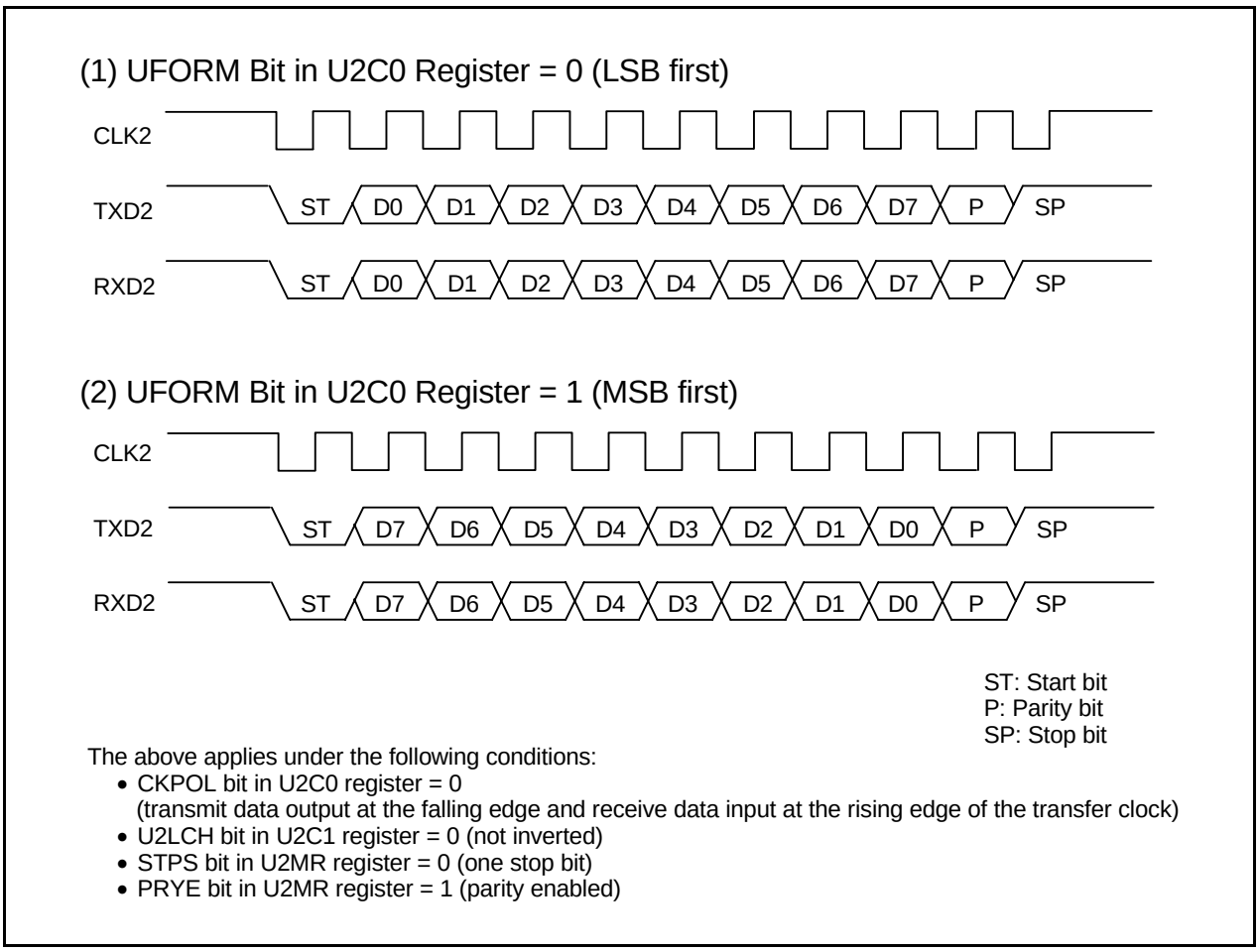


Figure 25.9 Transfer Format

25.4.4 Serial Data Logic Switching Function

The data written to the U2TB register has its logic inverted before being transmitted. Similarly, the received data has its logic inverted when read from the U2RB register. Figure 25.10 shows the Serial Data Logic Switching.

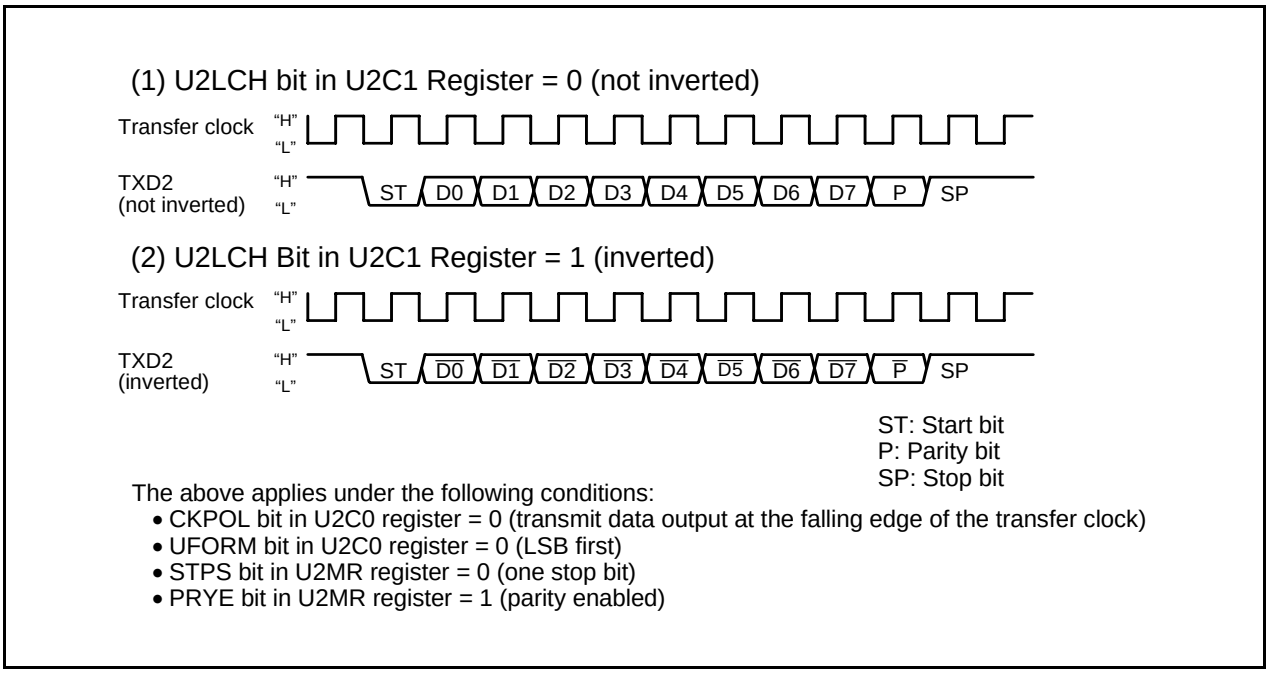


Figure 25.10 Serial Data Logic Switching

25.4.5 TXD and RXD I/O Polarity Inverse Function

This function inverts the polarities of the TXD2 pin output and RXD2 pin input. The logic levels of all I/O data (including bits for start, stop, and parity) are inverted. Figure 25.11 shows the TXD and RXD I/O Inversion.

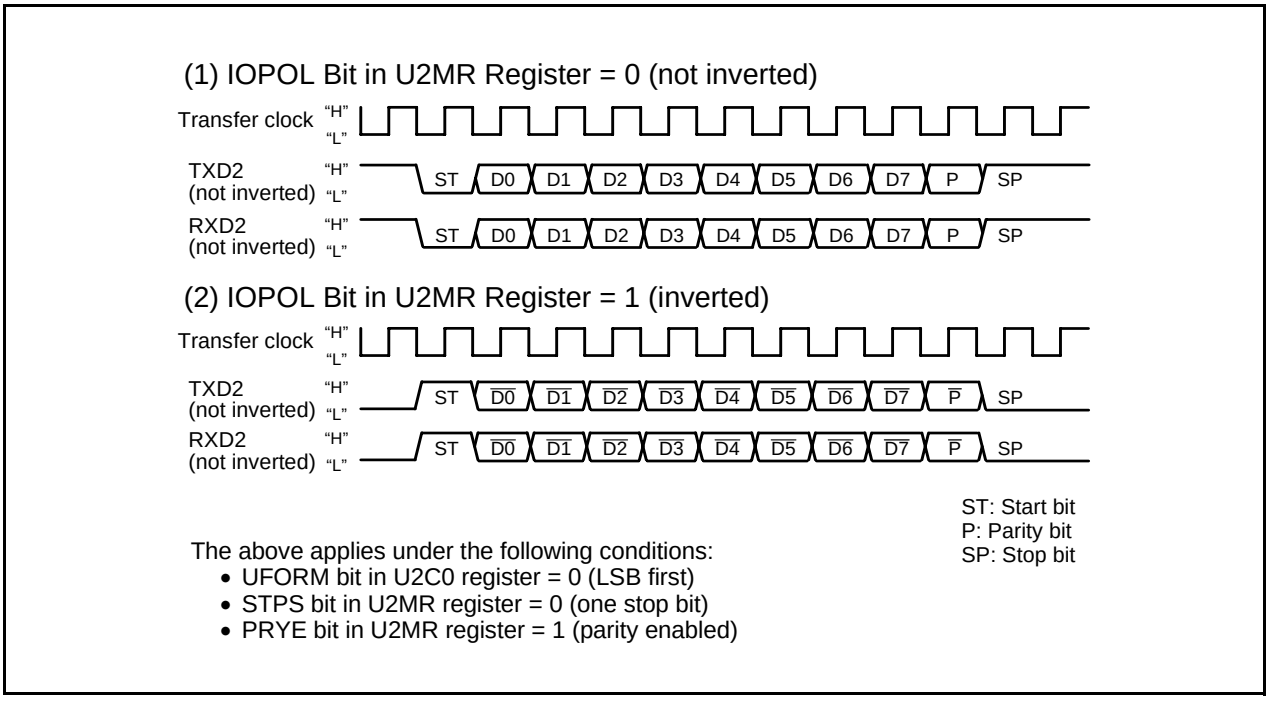


Figure 25.11 TXD and RXD I/O Inversion

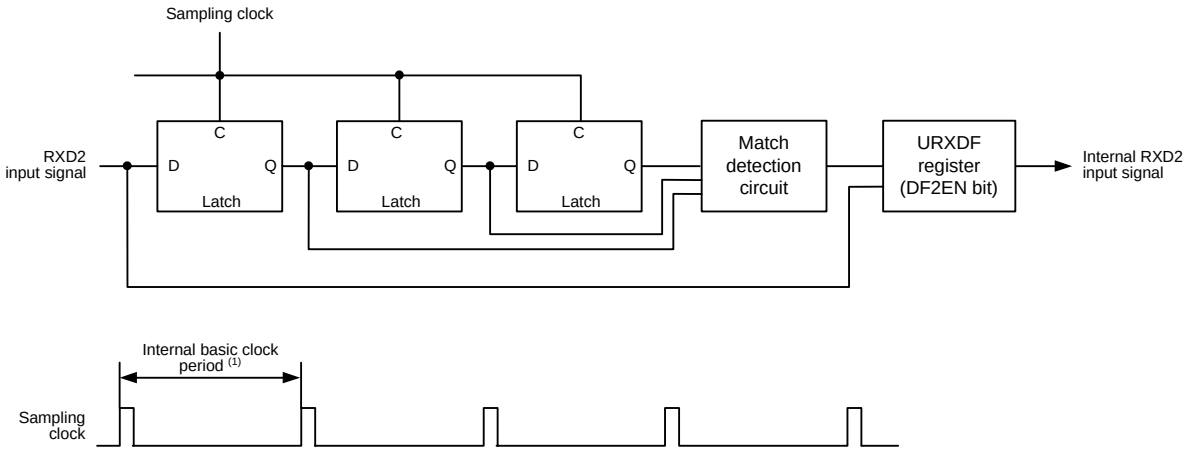
25.4.6 $\overline{\text{CTS}}/\overline{\text{RTS}}$ Function

The $\overline{\text{CTS}}$ function is used to start transmit operation when a low-level signal is applied to the $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin. Transmit operation begins when the $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin is held low. If the input level is switched to high during a transmit operation, the operation stops before the next data.
When the $\overline{\text{RTS}}$ function is used, the $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin outputs a low-level signal when the MCU is ready for a receive operation. The output level goes high at the first falling edge of the CLK2 pin.

- The CRD bit in the U2C0 register = 1 ($\overline{\text{CTS}}/\overline{\text{RTS}}$ function disabled)
  The $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin operates as the programmable I/O function.
- The CRD bit = 0, CRS bit = 0 ($\overline{\text{CTS}}$ function selected)
  The $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin operates as the $\overline{\text{CTS}}$ function.
- The CRD bit = 0, CRS bit = 1 ($\overline{\text{RTS}}$ function selected)
  The $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin operates as the $\overline{\text{RTS}}$ function.

25.4.7 RXD2 Digital Filter Select Function

When the DF2EN bit in the URXDF register is set to 1 (RXD2 digital filer enabled), the RXD2 input signal is loaded internally via the digital filter circuit for noise reduction. The noise canceller consists of three cascaded latch circuits and a match detection circuit. The RXD2 input signal is sampled on the basic clock with a frequency 16 times the bit rate. It is recognized as a signal and the level is passed forward to the next circuit when three latch outputs match. When the outputs do not match, the previous value is retained.
In other words, when the level is changed within three clocks, the change is recognized as not a signal but noise.
Figure 25.12 shows a Block Diagram of RXD2 Digital Filter Circuit.



Note:
1. When the CKDIR bit in the U2MR register is 0 (internal clock), the internal basic clock is set to fj/(n+1)
   (fj = f1, f8, f32, fC; n = setting value in the U2BRG register).
   When the CKDIR bit in the U2MR register is 1 (external clock), the internal basic clock is set to fEXT/(n+1)
   (fEXT is input from the CLK2 pin. n = setting value in the U2BRG register).

Figure 25.12 Block Diagram of RXD2 Digital Filter Circuit

25.5 Special Mode 1 (I^2C Mode)

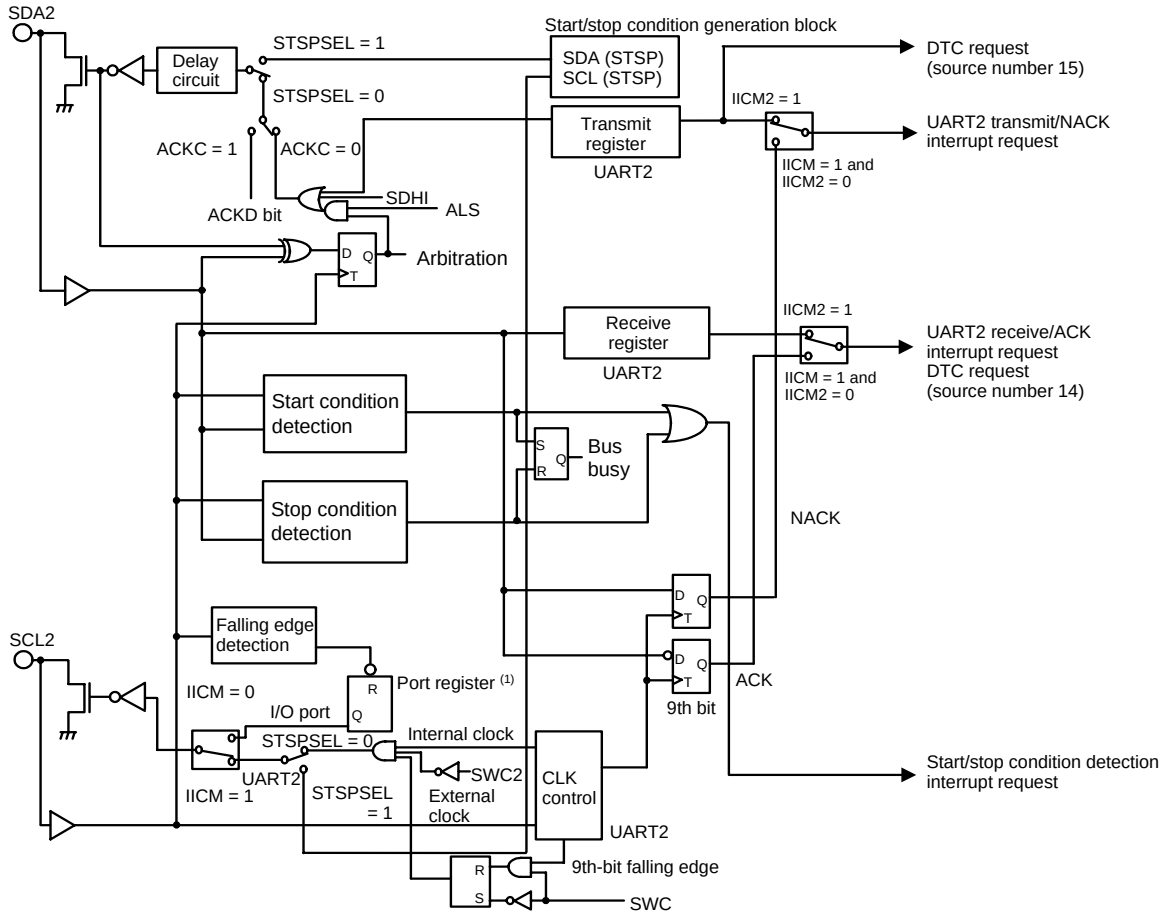
I^2C mode is provided for use as a simplified I^2C interface compatible mode. Table 25.9 lists the I^2C Mode Specifications. Tables 25.10 and 25.11 list the registers used in I^2C mode and the settings. Table 25.12 lists the I^2C Mode Functions, Figure 25.13 shows a Block Diagram of I^2C Mode, and Figure 25.14 shows the Transfer to U2RB Register and Interrupt Timing.

As shown in Table 25.12, the MCU is placed in I^2C mode by setting bits SMD2 to SMD0 to 010b and the IICM bit to 1. Because SDA2 transmit output has a delay circuit attached, SDA2 output does not change state until SCL2 goes low and remains stably low.

Table 25.9 I^2C Mode Specifications

Item	Specification
Transfer data format	Transfer data length: 8 bits
Transfer clock	• Master mode The CKDIR bit in the U2MR register is set to 0 (internal clock): fj/(2(n+1)) fj = f1, f8, f32, fC n = Value set in U2BRG register: 00h to FFh • Slave mode The CKDIR bit is set to 1 (external clock): Input from the SCL2 pin
Transmit start conditions	To start transmission, the following requirements must be met: (1) • The TE bit in the U2C1 register is set to 1 (transmission enabled). • The TI bit in the U2C1 register is set to 0 (data in the U2TB register).
Receive start conditions	To start reception, the following requirements must be met: (1) • The RE bit in the U2C1 register is set to 1 (reception enabled). • The TE bit in the U2C1 register is set to 1 (transmission enabled). • The TI bit in the U2C1 register is set to 0 (data in the U2TB register).
Interrupt request generation timing	Start/stop condition detection, no acknowledgement detection, or acknowledgement detection
Error detection	Overrun error (2) This error occurs if the serial interface starts receiving the next unit of data before reading the U2RB register and receives the 8th bit of the next unit of data.
Selectable functions	• Arbitration lost Timing at which the ABT bit in the U2RB register is updated can be selected. • SDA2 digital delay No digital delay or a delay of 2 to 8 U2BRG count source clock cycles can be selected. • Clock phase setting With or without clock delay can be selected.

Notes:
1. If an external clock is selected, the requirements must be met while the external clock is held high.
2. If an overrun error occurs, the received data in the U2RB register will be undefined. The IR bit in the S2RIC register remains unchanged.



IICM: Bit in U2SMR register
IICM2, SWC, ALS, SWC2, SDHI: Bits in U2SMR2 register
STSPSEL, ACKD, ACKC: Bits in U2SMR4 register

The above applies under the following conditions:
- Bits SMD2 to SMD0 in U2MR register = 010b
- IICM bit in U2SMR register = 1

Note:
1. When the IICM bit is set to 1, the pin level can be read even if the port direction bit corresponding to the SCL2 pin is set to 1 (output mode).

Figure 25.13 Block Diagram of I²C Mode

Table 25.10 Registers Used and Settings in I²C Mode (1)

Register	Bit	Function	
		Master	Slave
U2TB (1)	b0 to b7	Set transmit data.	Set transmit data.
U2RB (1)	b0 to b7	Receive data can be read.	Receive data can be read.
	b8	ACK or NACK is set in this bit.	ACK or NACK is set in this bit.
	ABT	Arbitration lost detect flag	Disabled
	OER	Overrun error flag	Overrun error flag
U2BRG	b0 to b7	Set the transfer rate.	Disabled
U2MR (1)	SMD2 to SMD0	Set to 010b.	Set to 010b.
	CKDIR	Set to 0.	Set to 1.
	IOPOL	Set to 0.	Set to 0.
U2C0	CLK0, CLK1	Select the count source for the U2BRG register.	Disabled
	CRS	Disabled because CRD = 1.	Disabled because CRD = 1.
	TXEPT	Transmit register empty flag	Transmit register empty flag
	CRD	Set to 1.	Set to 1.
	NCH	Set to 1.	Set to 1.
	CKPOL	Set to 0.	Set to 0.
	UFORM	Set to 1.	Set to 1.
U2C1	TE	Set to 1 to enable transmission.	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag	Transmit buffer empty flag
	RE	Set to 1 to enable reception.	Set to 1 to enable reception.
	RI	Reception complete flag	Reception complete flag
	U2IRS	Disabled	Disabled
	U2RRM, U2LCH, U2ERE	Set to 0.	Set to 0.
U2SMR	IICM	Set to 1.	Set to 1.
	ABC	Select the timing at which an arbitration lost is detected.	Disabled
	BBS	Bus busy flag	Bus busy flag
	b3 to b7	Set to 0.	Set to 0.
U2SMR2	IICM2	Refer to **Table 25.12 I²C Mode Functions**.	Refer to **Table 25.12 I²C Mode Functions**.
	CSC	Set to 1 to enable clock synchronization.	Set to 0.
	SWC	Set to 1 to fix SCL2 output low at the falling edge of the 9th bit of clock.	Set to 1 to fix SCL2 output low at the falling edge of the 9th bit of clock.
	ALS	Set to 1 to stop SDA2 output when an arbitration lost is detected.	Set to 0.
	STAC	Set to 0.	Set to 1 to initialize UART2 at start condition detection.
	SWC2	Set to 1 to forcibly pull SCL2 output low.	Set to 1 to forcibly pull SCL2 output low.
	SDHI	Set to 1 to disable SDA2 output.	Set to 1 to disable SDA2 output.
	b7	Set to 0.	Set to 0.

Note:
1. Set the bits not listed in this table to 0 when writing to the above registers in I²C mode.

Table 25.11 Registers Used and Settings in I²C Mode (2)

Register	Bit	Function	
		Master	Slave
U2SMR3	b0, b2, b4, NODC	Set to 0.	Set to 0.
	CKPH	Refer to **Table 25.12 I²C Mode Functions**.	Refer to **Table 25.12 I²C Mode Functions**.
	DL0 to DL2	Set the amount of SDA2 digital delay.	Set the amount of SDA2 digital delay.
U2SMR4	STAREQ	Set to 1 to generate a start condition.	Set to 0.
	RSTAREQ	Set to 1 to generate a restart condition.	Set to 0.
	STPREQ	Set to 1 to generate a stop condition.	Set to 0.
	STSPSEL	Set to 1 to output each condition.	Set to 0.
	ACKD	Select ACK or NACK.	Select ACK or NACK.
	ACKC	Set to 1 to output ACK data.	Set to 1 to output ACK data.
	SCLHI	Set to 1 to stop SCL2 output when a stop condition is detected.	Set to 0.
	SWC9	Set to 0.	Set to 1 to hold SCL2 low at the falling edge of the 9th bit of clock.
URXDF	DF2EN	Set to 0.	Set to 0.
U2SMR5	MP	Set to 0.	Set to 0.

Table 25.12 I²C Mode Functions

Function	Clock Synchronous Serial I/O Mode (SMD2 to SMD0 = 001b, IICM = 0)	I²C Mode (SMD2 to SMD0 = 010b, IICM = 1)			
		IICM2 = 0 (NACK/ACK interrupt)		IICM2 = 1 (UART transmit/receive interrupt)	
		CKPH = 0 (No Clock Delay)	CKPH = 1 (With Clock Delay)	CKPH = 0 (No Clock Delay)	CKPH = 1 (With Clock Delay)
Source of UART2 bus collision interrupt (1, 5)	–	Start condition detection or stop condition detection (Refer to **Table 25.13 STSPSEL Bit Functions**)			
Source of UART2 transmit/ NACK2 interrupt (1, 6)	UART2 transmission Transmission started or completed (selectable by U2IRS bit)	No acknowledgment detection (NACK) Rising edge of SCL2 9th bit		UART2 transmission Rising edge of SCL2 9th bit	UART2 transmission Falling edge of SCL2 next to 9th bit
Source of UART2 receive/ACK2 interrupt (1, 6)	UART2 reception When 8th bit received CKPOL = 0 (rising edge) CKPOL = 1 (falling edge)	Acknowledgment detection (ACK) Rising edge of SCL2 9th bit		UART2 reception Falling edge of SCL2 9th bit	
Timing for transferring data from UART receive shift register to U2RB register	CKPOL = 0 (rising edge) CKPOL = 1 (falling edge)	Rising edge of SCL2 9th bit		Falling edge of SCL2 9th bit	Falling and rising edges of SCL2 9th bit
UART2 transmission output delay	No delay	With delay			
TXD2/SDA2 functions	TXD2 output	SDA2 I/O			
RXD2/SCL2 functions	RXD2 input	SCL2 I/O			
CLK2 function	CLK2 input or output port selected	– (Usable in I²C mode.)			
Read of RXD2 and SCL2 pin levels	Enabled when the corresponding port direction bit = 0	Enabled regardless of the content of the corresponding port direction bit.			
Initial value of TXD2 and SDA2 outputs	CKPOL = 0 (high) CKPOL = 1 (low)	The value set in the port register before setting I²C mode. (2)			
Initial and end values of SCL2	–	High	Low	High	Low
DTC source number 14 (6)	UART2 reception When 8th bit received CKPOL = 0 (rising edge) CKPOL = 1 (falling edge)	Acknowledgment detection (ACK)		UART2 reception Falling edge of SCL2 9th bit	
DTC source number 15 (6)	UART2 transmission Transmission started or completed (selectable by U2IRS bit)	UART2 transmission Rising edge of SCL2 9th bit	UART2 transmission Falling edge of SCL2 next to 9th bit	UART2 transmission Rising edge of SCL2 9th bit	UART2 transmission Falling edge of SCL2 next to 9th bit
Storage of receive data	The 1st to 8th bits of the received data are stored in bits b0 to b7 in the U2RB register.	The 1st to 8th bits of the received data are stored in bits b7 to b0 in the U2RB register.		The 1st to 7th bits of the received data are stored in bits b6 to b0 in the U2RB register. 8th bit is stored in bit b8 in the U2RB register.	
					The 1st to 8th bits are stored in bits b7 to b0 in the U2RB register. (3)
Read of receive data	The U2RB register status is read.				Bits b6 to b0 in the U2RB register are read as bits b7 to b1. Bit b8 in the U2RB register is read as bit b0. (4)

Notes:
1. If the source of any interrupt is changed, the IR bit in the interrupt control register for the changed interrupt may inadvertently be set to 1 (interrupt requested). (Refer to **12.8 Notes on Interrupts**.)
   If one of the bits listed below is changed, the interrupt source, the interrupt timing, and others change. Always be sure to set the IR bit to 0 (interrupt not requested) after changing these bits:
   Bits SMD2 to SMD0 in the U2MR register, the IICM bit in the U2SMR register, the IICM2 bit in the U2SMR2 register, and the CKPH bit in the U2SMR3 register.
2. Set the initial value of SDA2 output while bits SMD2 to SMD0 in the U2MR register are 000b (serial interface disabled).
3. Second data transfer to the U2RB register (rising edge of SCL2 9th bit)
4. First data transfer to the U2RB register (falling edge of SCL2 9th bit)
5. Refer to **Figure 25.16 STSPSEL Bit Functions**.
6. Refer to **Figure 25.14 Transfer to U2RB Register and Interrupt Timing**.

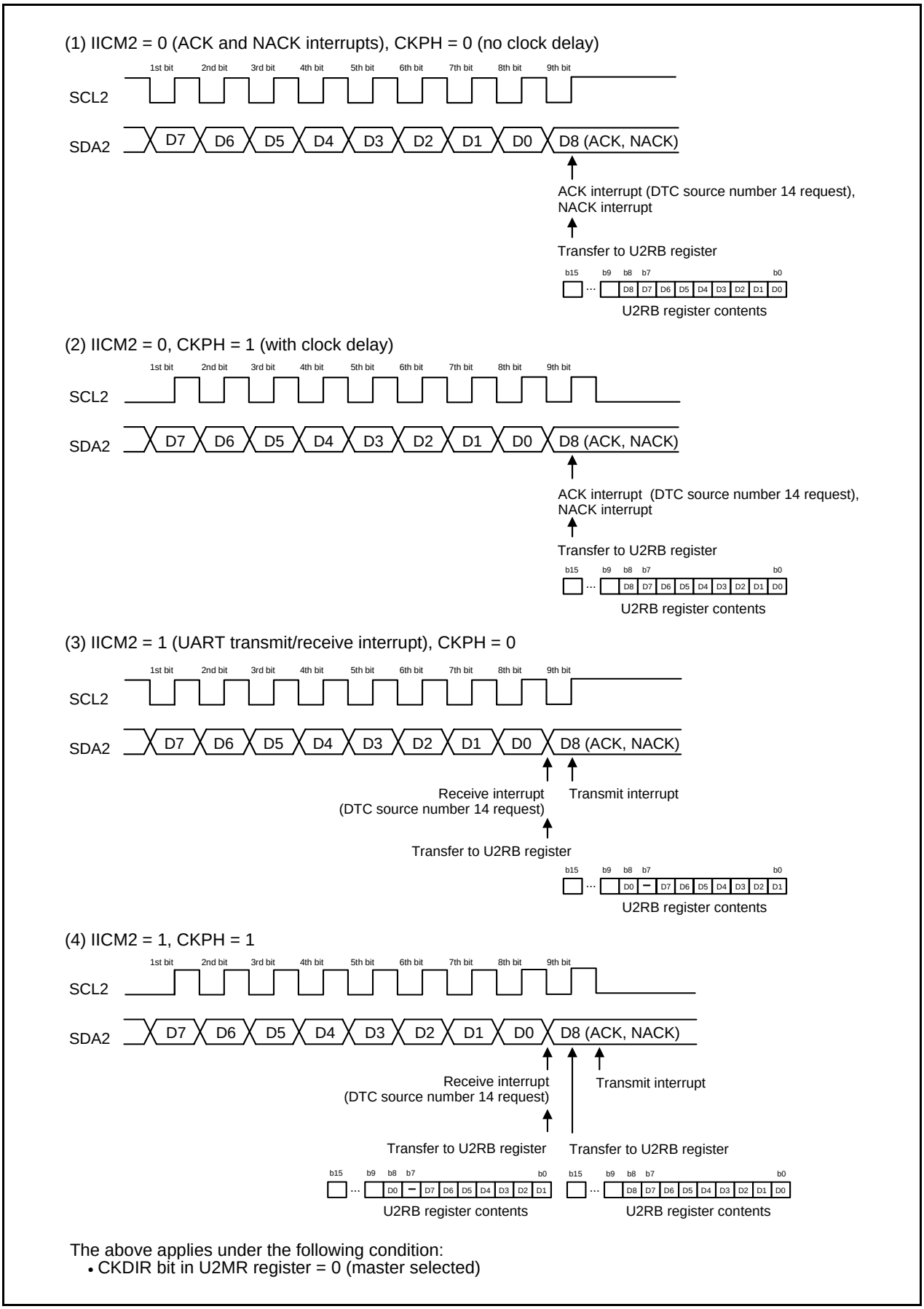


Figure 25.14 Transfer to U2RB Register and Interrupt Timing

25.5.1 Detection of Start and Stop Conditions

Whether a start or a stop condition has been detected is determined.
A start condition detect interrupt request is generated when the SDA2 pin changes state from high to low while the SCL2 pin is in the high state. A stop condition detect interrupt request is generated when the SDA2 pin changes state from low to high while the SCL2 pin is in the high state.
Because the start and stop condition detect interrupts share an interrupt control register and vector, check the BBS bit in the U2SMR register to determine which interrupt source is requesting the interrupt.
Figure 25.15 shows the Detection of Start and Stop Conditions.

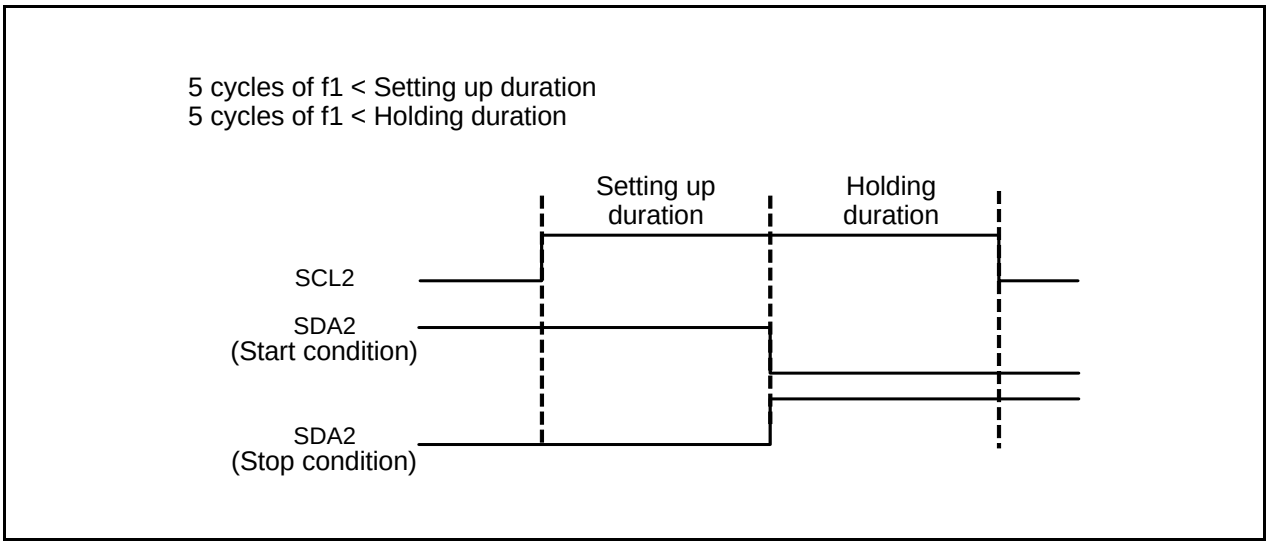


Figure 25.15 Detection of Start and Stop Conditions

25.5.2 Output of Start and Stop Conditions

A start condition is generated by setting the STAREQ bit in the U2SMR4 register to 1 (start).
A restart condition is generated by setting the RSTAREQ bit in the U2SMR4 register to 1 (start).
A stop condition is generated by setting the STPREQ bit in the U2SMR4 register to 1 (start).

The output procedure is as follows:
(1) Set the STAREQ, RSTAREQ, or STPREQ bit to 1 (start).
(2) Set the STSPSEL bit in the U2SMR4 register to 1 (output).
Table 25.13 lists the STSPSEL Bit Functions. Figure 25.16 shows the STSPSEL Bit Functions.

Table 25.13 STSPSEL Bit Functions

Function	STSPSEL = 0	STSPSEL = 1
SCL2/SDA2 pin output	Output of a transfer clock and data. Output of start/stop conditions is accomplished by a program using ports (no automatic generation by hardware)	Output of start/stop conditions according to bits STAREQ, RSTAREQ, and STPREQ
Start/stop condition interrupt request generation timing	Generation of start/stop conditions	Completion of start/stop condition generation

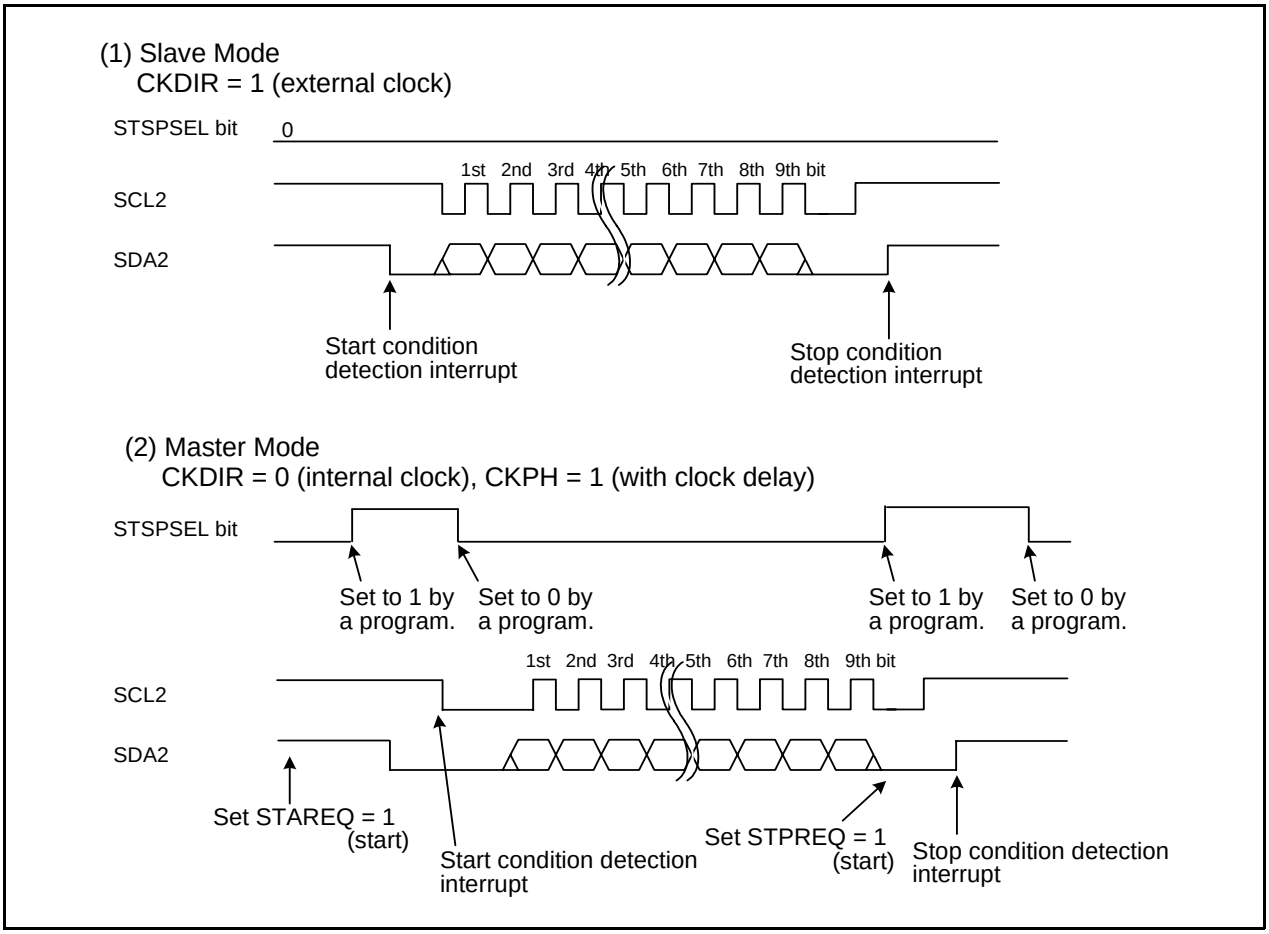


Figure 25.16 STSPSEL Bit Functions

25.5.3 Arbitration

Unmatching of the transmit data and SDA2 pin input data is checked in synchronization with the rising edge of SCL2. The ABC bit in the U2SMR register can be used to select the timing at which the ABT bit in the U2RB register is updated. If the ABC bit is set to 0 (update per bit), the ABT bit is set to 1 at the same time unmatching is detected during check, and is set to 0 when not detected. When the ABC bit is set to 1, if unmatching is ever detected, the ABT bit is set to 1 (unmatching detected) at the falling edge of the clock pulse of the 9th bit. If the ABT bit needs to be updated per byte, set the ABT bit to 0 (not detected) after detecting acknowledge for the first byte, before transferring the next byte.
Setting the ALS bit in the U2SMR2 register to 1 (SDA output stop enabled) causes an arbitration lost to occur, in which case the SDA2 pin is placed in the high-impedance state at the same time the ABT bit is set to 1 (unmatching detected).

25.5.4 Transfer Clock

The transfer clock is used to transmit and receive data as is shown in **Figure 25.14 Transfer to U2RB Register and Interrupt Timing**.
The CSC bit in the U2SMR2 register is used to synchronize an internally generated clock (internal SCL2) and an external clock supplied to the SCL2 pin. When the CSC bit is set to 1 (clock synchronization enabled), if a falling edge on the SCL2 pin is detected while the internal SCL2 is high, the internal SCL2 goes low. The value of the U2BRG register is reloaded and counting of the low-level intervals starts. When the internal SCL2 changes state from low to high while the SCL2 pin is low, counting stops. When the SCL2 pin goes high, counting restarts. In this way, the UART2 transfer clock is equivalent to AND of the internal SCL2 and the clock signal applied to the SCL2 pin. The transfer clock works from a half cycle before the falling edge of the internal SCL2 1st bit to the rising edge of the 9th bit. To use this function, select an internal clock for the transfer clock.

The SWC bit in the U2SMR2 register can be used to select whether the SCL2 pin is fixed low or freed from low-level output at the falling edge of the 9th clock pulse.
If the SCLHI bit in the U2SMR4 register is set to 1 (enabled), SCL2 output is turned off (placed in the high impedance state) when a stop condition is detected.
Setting the SWC2 bit in the U2SMR2 register to 1 (low-level output) allows a low-level signal to be forcibly output from the SCL2 pin even during transmission or reception. Setting the SWC2 bit to 0 (transfer clock) allows the transfer clock to be output from or supplied to the SCL2 pin, instead of outputting a low-level signal.
If the SWC9 bit in the U2SMR4 register is set to 1 (SCL hold low enabled) when the CKPH bit in the U2SMR3 register is 1, the SCL2 pin is fixed low at the falling edge of the clock pulse next to the 9th. Setting the SWC9 bit to 0 (SCL hold low disabled) frees the SCL2 pin from low-level output.

25.5.5 SDA Output

The data written to bits b7 to b0 (D7 to D0) in the U2TB register is output in descending order from D7.
The 9th bit (D8) is ACK or NACK.
Set the initial value of SDA2 transmit output when IICM is set to 1 (I^2C mode) and bits SMD2 to SMD0 in the U2MR register are set to 000b (serial interface disabled).
Bits DL2 to DL0 in the U2SMR3 register allow addition of no delays or a delay of two to eight U2BRG count source clock cycles to the SDA2 output.
Setting the SDHI bit in the U2SMR2 register to 1 (SDA output disabled) forcibly places the SDA2 pin in the high impedance state. Do not write to the SDHI bit at the rising edge of the UART2 transfer clock. This is because the ABT bit may be set to 1 (detected).

25.5.6 SDA Input

When the IICM2 bit is set to 0, the 1st to 8th bits (D7 to D0) of received data are stored in bits b7 to b0 in the U2RB register. The 9th bit (D8) is ACK or NACK.
When the IICM2 bit is set to 1, the 1st to 7th bits (D7 to D1) of received data are stored in bits b6 to b0 in the U2RB register and the 8th bit (D0) is stored in bit b8 in the U2RB register. Even when the IICM2 bit is set to 1, if the CKPH bit is 1, the same data as when the IICM2 bit is 0 can be read by reading the U2RB register after the rising edge of the 9th bit of the clock.

25.5.7 ACK and NACK

When the STSPSEL bit in the U2SMR4 register is set to 0 (start and stop conditions not output) and the ACKC bit in the U2SMR4 register is set to 1 (ACK data output), the value of the ACKD bit in the U2SMR4 register is output from the SDA2 pin.
When the IICM2 bit is set to 0, a NACK interrupt request is generated if the SDA2 pin remains high at the rising edge of the 9th bit of the transmit clock. An ACK interrupt request is generated if the SDA2 pin is low at the rising edge of the 9th bit of the transmit clock.
When ACK2 (UART2 reception) is selected to generate a DTC request source, a DTC transfer can be activated by detection of an acknowledge.

25.5.8 Initialization of Transmission/Reception

When a start condition is detected while the STAC bit is set to 1 (UART2 initialization enabled), the serial interface operates as described below.

- The transmit shift register is initialized, and the contents of the U2TB register are transferred to the transmit shift register. In this way, the serial interface starts sending data when the next clock pulse is applied. However, the UART2 output value does not change state and remains the same as when a start condition was detected until the first bit of data is output in synchronization with the input clock.
- The receive shift register is initialized, and the serial interface starts receiving data when the next clock pulse is applied.
- The SWC bit is set to 1 (SCL wait output enabled). Consequently, the SCL2 pin is pulled low at the falling edge of the 9th clock.

Note that when UART2 transmission/reception is started using this function, the TI bit does not change state. Select the external clock as the transfer clock to start UART2 transmission/reception with this setting.

25.6 Multiprocessor Communication Function

When the multiprocessor communication function is used, data transmission/reception can be performed between a number of processors sharing communication lines by asynchronous serial communication, in which a multiprocessor bit is added to the data. For multiprocessor communication, each receiving station is addressed by a unique ID code. The serial communication cycle consists of two component cycles; an ID transmission cycle for specifying the receiving station, and a data transmission cycle for the specified receiving station. The multiprocessor bit is used to differentiate between the ID transmission cycle and the data transmission cycle. When the multiprocessor bit is set to 1, the cycle is an ID transmission cycle; when the multiprocessor bit is set to 0, the cycle is a data transmission cycle. Figure 25.17 shows a Multiprocessor Communication Example Using Multiprocessor Format (Data AAh Transmission to Receiving Station A).
The transmitting station first sends the ID code of the receiving station to perform communication as communication data with a 1 multiprocessor bit added. It then sends transmit data as communication data with a 0 multiprocessor bit added.
When communication data in which the multiprocessor bit is 1 is received, the receiving station compares that data with its own ID. If they match, the data to be sent next is received. If they do not match, the receive station continues to skip communication data until data in which the multiprocessor bit is 1 is again received.

UART2 uses the MPIE bit in the U2SMR5 register to implement this function. When the MPIE bit is set to 1, data transfer from the UART2 receive register to the U2RB register, receive error detection, and the settings of the status flags, the RI bit in the U2C1 register, bits FER and OER in the U2RB register, are disabled until data in which the multiprocessor bit is 1 is received. On receiving a receive character in which the multiprocessor bit is 1, the MPRB bit in the U2RB register is set to 1 and the MPIE in the U2SMR5 register bit is set to 0, thus normal reception is resumed.

When the multiprocessor format is specified, the parity bit specification is invalid. All other bit settings are the same as those in normal asynchronous mode (UART mode). The clock used for multiprocessor communication is the same as that in normal asynchronous mode (UART mode).

Figure 25.18 shows a Block Diagram of Multiprocessor Communication Function.
Table 25.14 lists the Registers and Settings for Multiprocessor Communication Function.

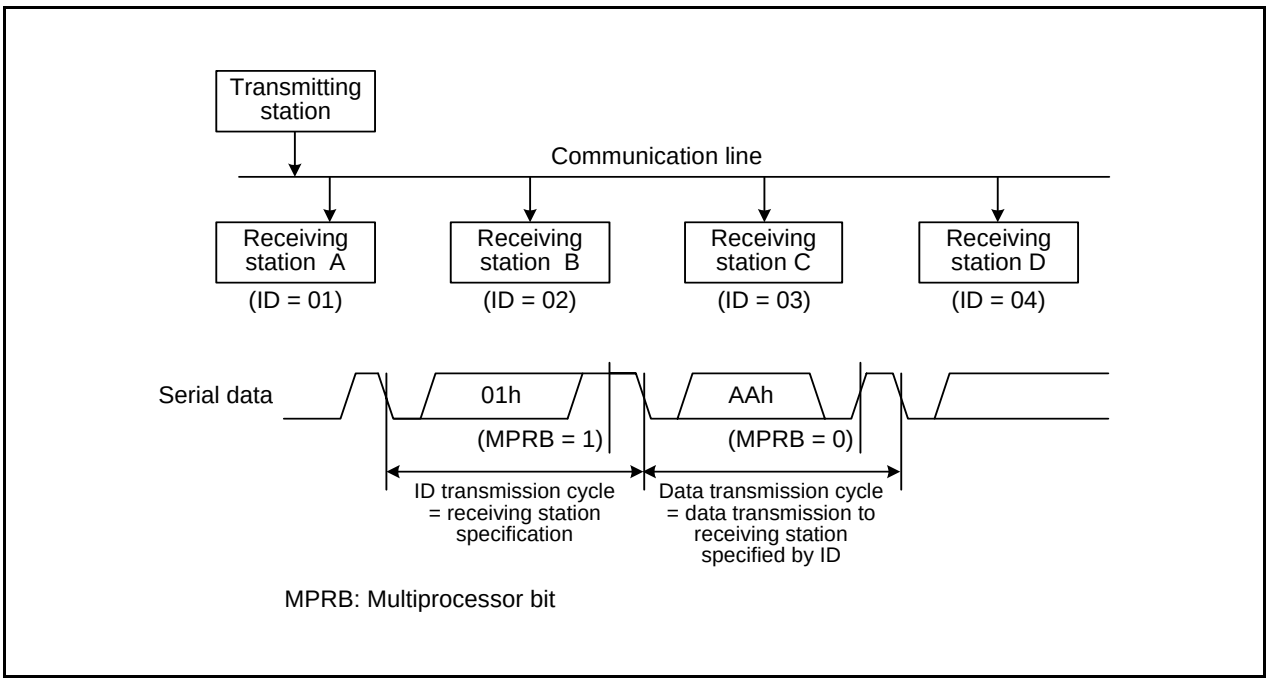
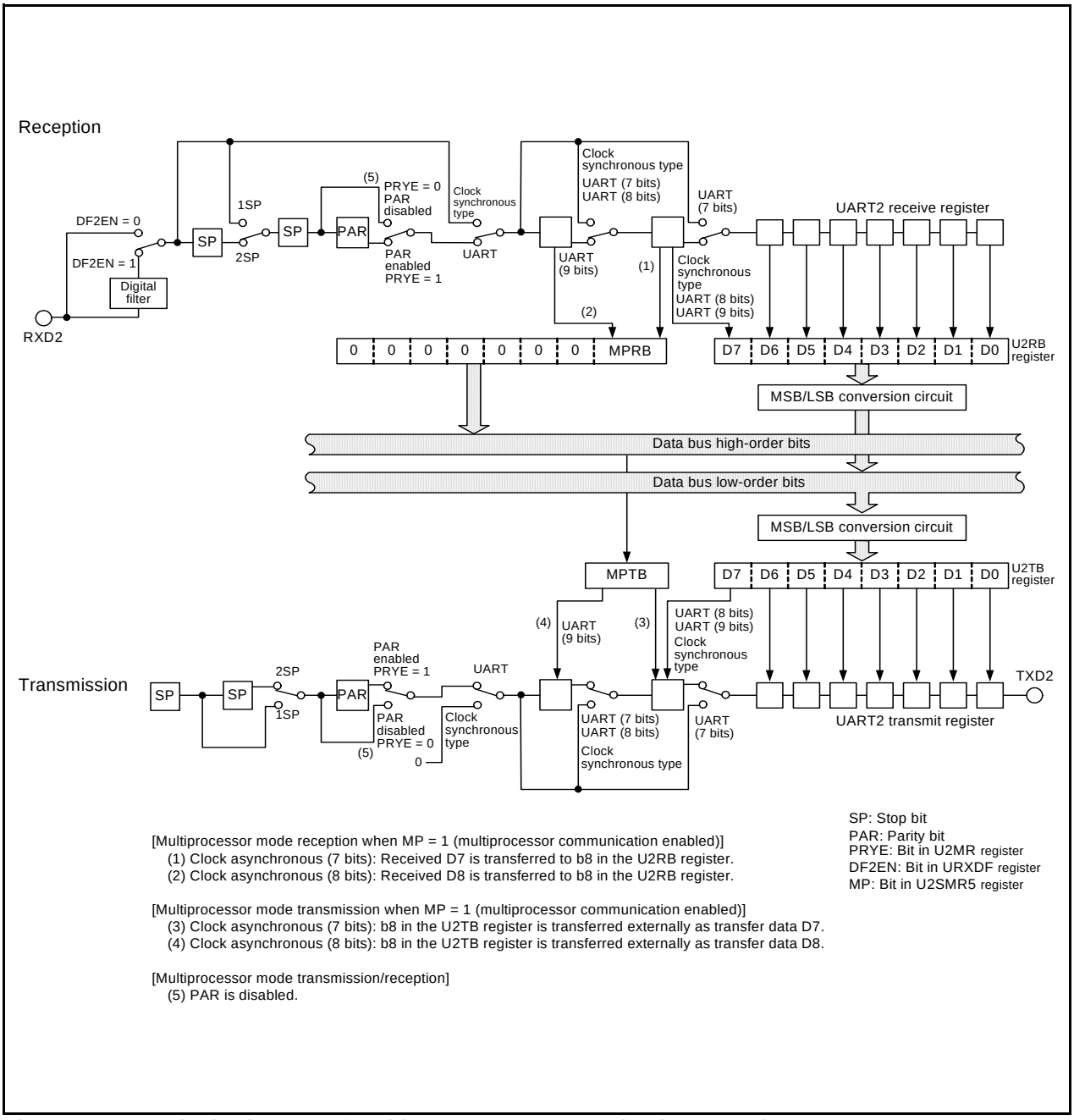


Figure 25.17 Multiprocessor Communication Example Using Multiprocessor Format (Data AAh Transmission to Receiving Station A)



SP: Stop bit
PAR: Parity bit
PRYE: Bit in U2MR register
DF2EN: Bit in URXDF register
MP: Bit in U2SMR5 register

[Multiprocessor mode reception when MP = 1 (multiprocessor communication enabled)]
(1) Clock asynchronous (7 bits): Received D7 is transferred to b8 in the U2RB register.
(2) Clock asynchronous (8 bits): Received D8 is transferred to b8 in the U2RB register.

[Multiprocessor mode transmission when MP = 1 (multiprocessor communication enabled)]
(3) Clock asynchronous (7 bits): b8 in the U2TB register is transferred externally as transfer data D7.
(4) Clock asynchronous (8 bits): b8 in the U2TB register is transferred externally as transfer data D8.

[Multiprocessor mode transmission/reception]
(5) PAR is disabled.

Figure 25.18 Block Diagram of Multiprocessor Communication Function

Table 25.14 Registers and Settings for Multiprocessor Communication Function

Register	Bit	Function
U2TB (1)	b0 to b7	Set transmit data.
	MPTB	Set to 0 or 1.
U2RB (2)	b0 to b7	Receive data can be read.
	MPRB	Multiprocessor bit
	OER, FER, SUM	Error flag
U2BRG	b0 to b7	Set the transfer rate.
U2MR	SMD2 to SMD0	Set to 100b when transfer data is 7 bits long.
		Set to 101b when transfer data is 8 bits long.
	CKDIR	Select an internal clock or external clock.
	STPS	Select the stop bit(s).
	PRY, PRYE	Parity detection function disabled
	IOPOL	Set to 0.
U2C0	CLK0, CLK1	Select the U2BRG count source.
	CRS	$\overline{\text{CTS}}$ or $\overline{\text{RTS}}$ function disabled
	TXEPT	Transmit register empty flag
	CRD	Set to 0.
	NCH	Select the output format of the TXD2 pin.
	CKPOL	Set to 0.
	UFORM	Set to 0.
U2C1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	U2IRS	Select the UART2 transmit interrupt source.
	U2LCH	Set to 0.
	U2ERE	Set to 0.
U2SMR	b0 to b7	Set to 0.
U2SMR2	b0 to b7	Set to 0.
U2SMR3	b0 to b7	Set to 0.
U2SMR4	b0 to b7	Set to 0.
U2SMR5	MP	Set to 1.
	MPIE	Set to 1.
URXDF	DF2EN	Select the digital filter enabled or disabled.

Notes:
1. Set the MPTB bit to 1 when the ID data frame is transmitted. Set this bit to 0 when the data frame is transmitted.
2. When the MPRB bit is set to 1, received D7 to D0 are ID fields. When this bit is set to 0, received D7 to D0 are data fields.

25.6.1 Multiprocessor Transmission

Figure 25.19 shows a Sample Flowchart of Multiprocessor Data Transmission. Set the MPBT bit in the U2TB register to 1 for ID transmission cycles. Set the MPBT bit in the U2TB register to 0 for data transmission cycles. Other operations are the same as in universal asynchronous receiver/transmitter mode (UART mode).

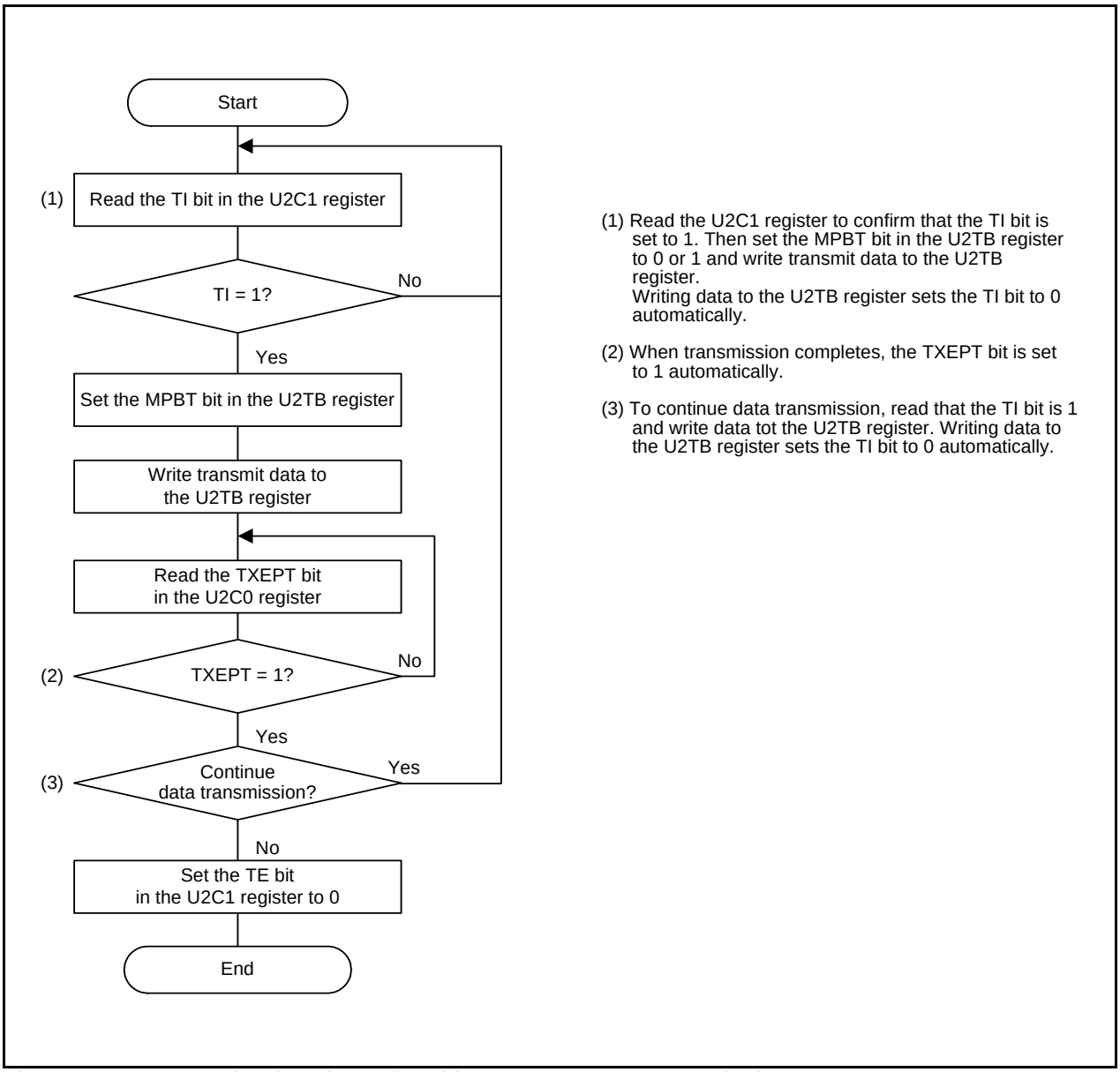


Figure 25.19 Sample Flowchart of Multiprocessor Data Transmission

25.6.2 Multiprocessor Reception

Figure 25.20 shows a Sample Flowchart of Multiprocessor Data Reception. When the MPIE bit in the U2SMR5 register is set to 1, communication data is ignored until data in which the multiprocessor bit is 1 is received. Communication data with a 1 multiprocessor bit added is transferred to the U2RB register as receive data. At this time, a reception complete interrupt request is generated. Other operations are the same as in universal asynchronous receiver/transmitter mode (UART mode). Figure 25.21 shows a Receive Operation Example during Multiprocessor Communication (with 8-Bit Data/Multiprocessor Bit/One Stop Bit).

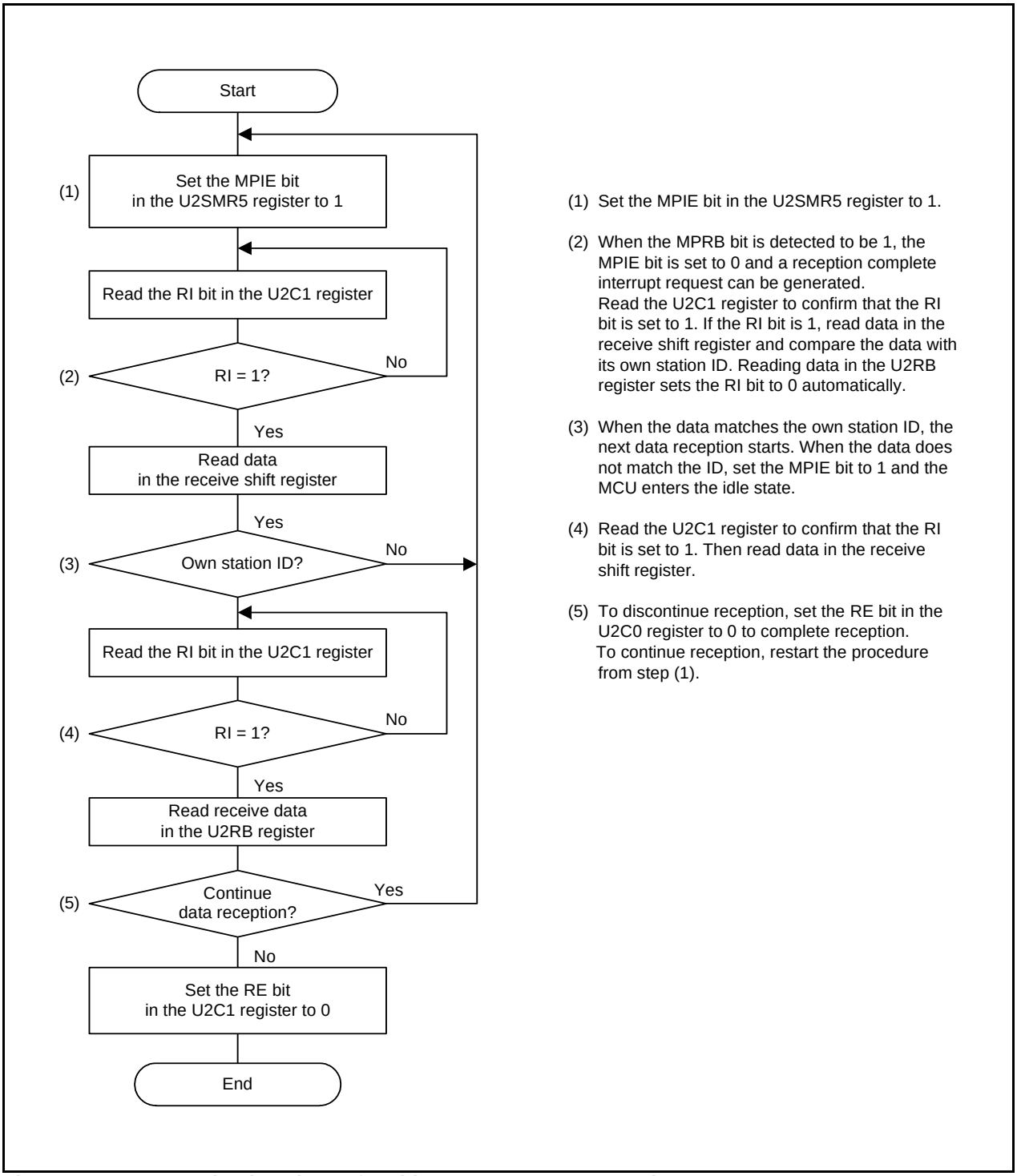


Figure 25.20 Sample Flowchart of Multiprocessor Data Reception

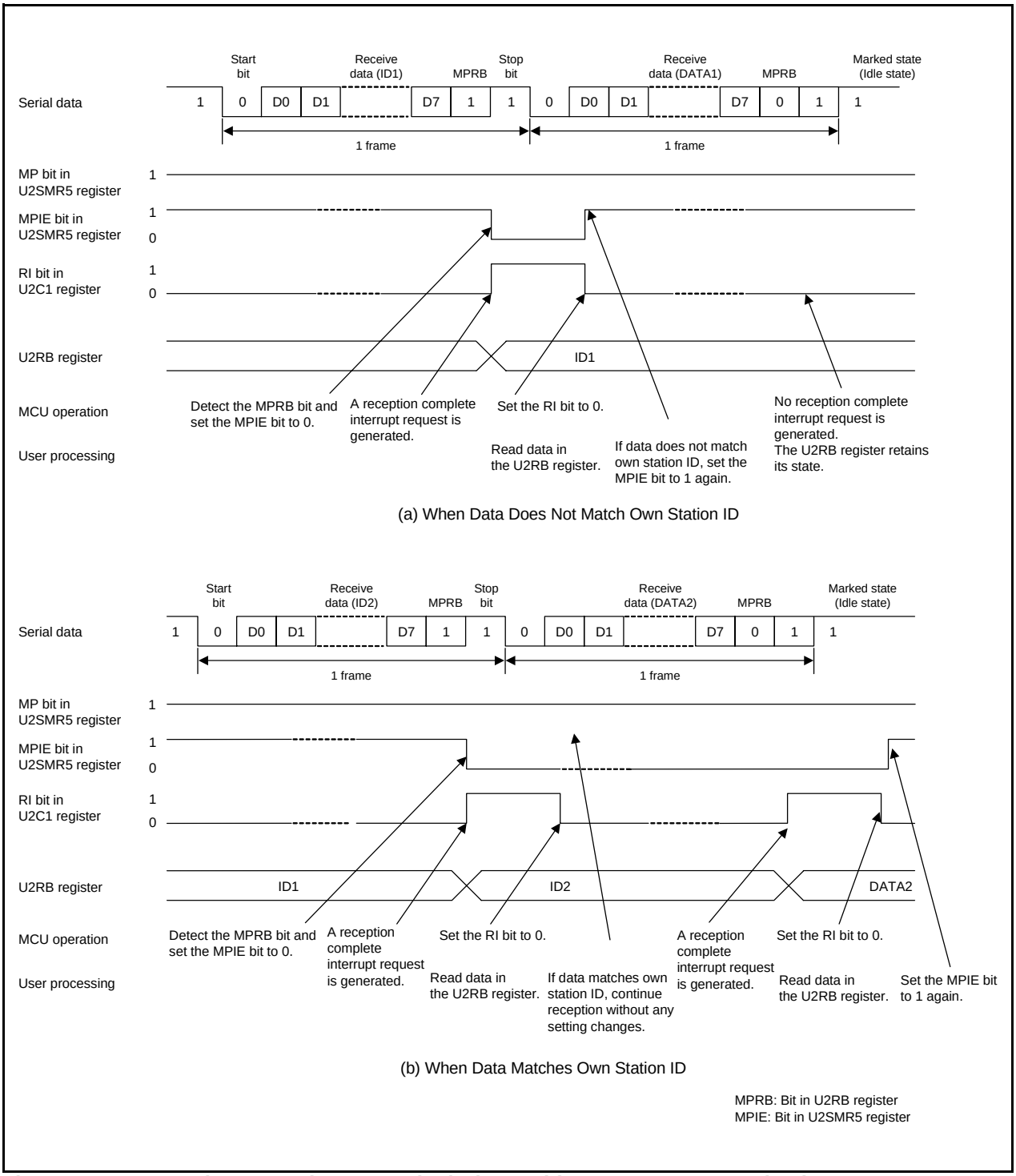
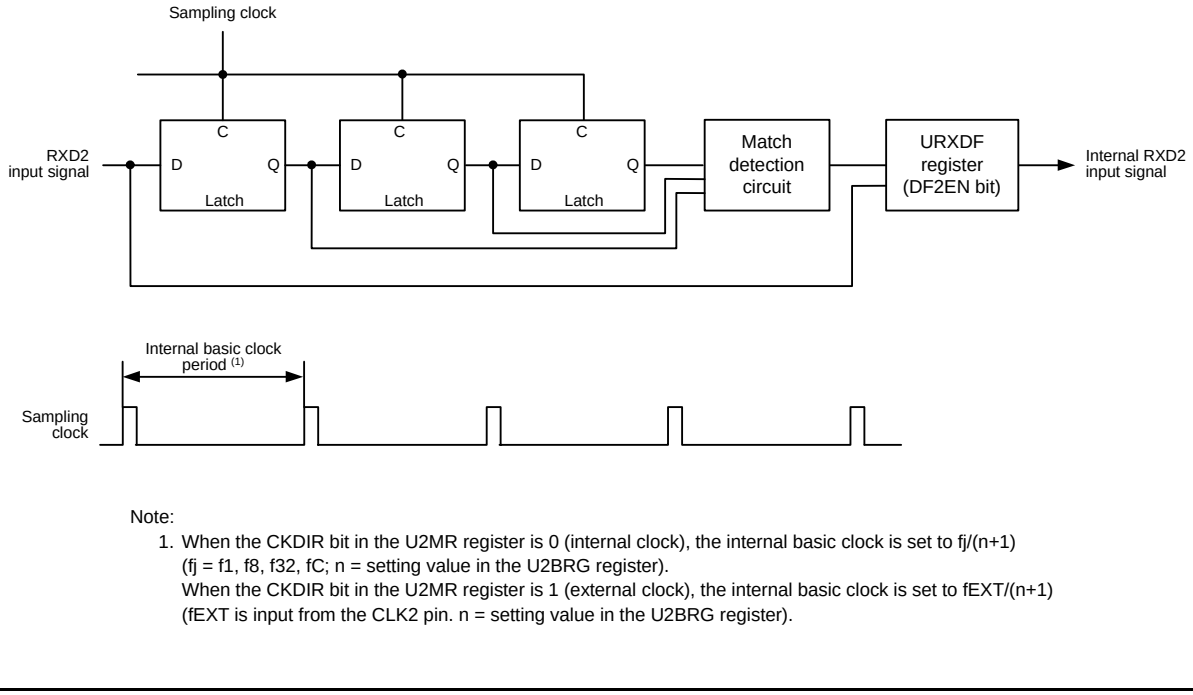


Figure 25.21 Receive Operation Example during Multiprocessor Communication (with 8-Bit Data/Multiprocessor Bit/One Stop Bit)

25.6.3 RXD2 Digital Filter Select Function

When the DF2EN bit in the URXDF register is set to 1 (RXD2 digital filer enabled), the RXD2 input signal is loaded internally via the digital filter circuit for noise reduction. The noise canceller consists of three cascaded latch circuits and a match detection circuit. The RXD2 input signal is sampled on the internal basic clock with a frequency 16 times the bit rate. It is recognized as a signal and the level is passed forward to the next circuit when three latch outputs match. When the outputs do not match, the previous value is retained.
In other words, when the level is changed within three clocks, the change is recognized as not a signal but noise.
Figure 25.12 shows a Block Diagram of RXD2 Digital Filter Circuit.



Note:
1. When the CKDIR bit in the U2MR register is 0 (internal clock), the internal basic clock is set to fj/(n+1) (fj = f1, f8, f32, fC; n = setting value in the U2BRG register).
When the CKDIR bit in the U2MR register is 1 (external clock), the internal basic clock is set to fEXT/(n+1) (fEXT is input from the CLK2 pin. n = setting value in the U2BRG register).

Figure 25.22 Block Diagram of RXD2 Digital Filter Circuit

25.7 Notes on Serial Interface (UART2)

25.7.1 Clock Synchronous Serial I/O Mode

25.7.1.1 Transmission/Reception

When the $\overline{\text{RTS}}$ function is used with an external clock, the $\overline{\text{RTS2}}$ pin outputs a low-level signal, which informs the transmitting side that the MCU is ready for a receive operation. The $\overline{\text{RTS2}}$ pin outputs a high-level signal when a receive operation starts. Therefore, the transmit timing and receive timing can be synchronized by connecting the $\overline{\text{RTS2}}$ pin to the $\overline{\text{CTS2}}$ pin of the transmitting side. The $\overline{\text{RTS}}$ function is disabled when an internal clock is selected.

25.7.1.2 Transmission

If an external clock is selected, the following conditions must be met while the external clock is held high when the CKPOL bit in the U2C0 register is set to 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock), or while the external clock is held low when the CKPOL bit is set to 1 (transmit data output at the rising edge and receive data input at the falling edge of the transfer clock).

- The TE bit in the U2C1 register is set to 1 (transmission enabled).
- The TI bit in the U2C1 register is set to 0 (data in the U2TB register).
- If the $\overline{\text{CTS}}$ function is selected, input to the $\overline{\text{CTS2}}$ pin is low.

25.7.1.3 Reception

In clock synchronous serial I/O mode, the shift clock is generated by activating the transmitter. Set the UART2-associated registers for transmission even if the MCU is used for reception only. Dummy data is output from the TXD2 pin during reception.

When an internal clock is selected, the shift clock is generated by setting the TE bit in the U2C1 register to 1 (transmission enabled) and setting dummy data in the U2TB register. When an external clock is selected, the shift clock is generated by setting the TE bit to 1 (transmission enabled), setting dummy data in the U2TB register, and inputting an external clock.

If data is received consecutively, an overrun error occurs when the RE bit in the U2C1 register is set to 1 (data in the U2RB register) and the next receive data is received in the UART2 receive register. Then, the OER bit in the U2RB register is set to 1 (overrun error). At this time, the U2RB register value is undefined. If an overrun error occurs, the IR bit in the S2RIC register remains unchanged.

To receive data consecutively, set dummy data in the low-order byte in the U2TB register per each receive operation.

If an external clock is selected, the following conditions must be met while the external clock is held high when the CKPOL bit is set to 0, or while the external clock is held low when the CKPOL bit is set to 1.

- The RE bit in the U2C1 register is set to 1 (reception enabled).
- The TE bit in the U2C1 register is set to 1 (transmission enabled).
- The TI bit in the U2C1 register is set to 0 (data in the U2TB register).

25.7.2 Clock Asynchronous Serial I/O (UART) Mode

25.7.2.1 Transmission/Reception

When the $\overline{\text{RTS}}$ function is used with an external clock, the $\overline{\text{RTS2}}$ pin outputs a low-level signal, which informs the transmitting side that the MCU is ready for a receive operation. The $\overline{\text{RTS2}}$ pin outputs a high-level signal when a receive operation starts. Therefore, the transmit timing and receive timing can be synchronized by connecting the $\overline{\text{RTS2}}$ pin to the $\overline{\text{CTS2}}$ pin of the transmitting side. The $\overline{\text{RTS}}$ function is disabled when an internal clock is selected.

25.7.2.2 Transmission

If an external clock is selected, the following conditions must be met while the external clock is held high when the CKPOL bit in the U2C0 register is set to 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock), or while the external clock is held low when the CKPOL bit is set to 1 (transmit data output at the rising edge and receive data input at the falling edge of the transfer clock).

- The TE bit in the U2C1 register is set to 1 (transmission enabled)
- The TI bit in the U2C1 register is set to 0 (data in the U2TB register)
- If the $\overline{\text{CTS}}$ function is selected, input on the $\overline{\text{CTS2}}$ pin is low.

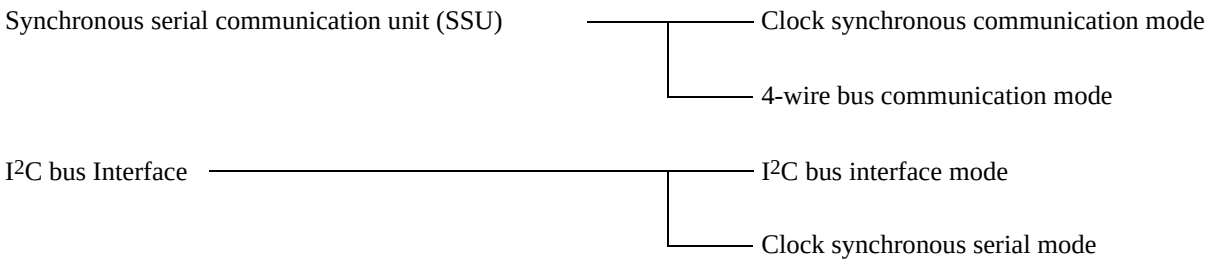
25.7.3 Special Mode 1 (I^2C Mode)

To generate start, stop, and restart conditions, set the STSPSEL bit in the U2SMR4 register to 0 and wait for more than half cycle of the transfer clock before changing each condition generation bit (STAREQ, RSTAREQ, and STPREQ) from 0 to 1.

26. Clock Synchronous Serial Interface

The clock synchronous serial interface is configured as follows.

Clock synchronous serial interface



The clock synchronous serial interface uses the registers at addresses 0193h to 019Dh. Registers, bits, symbols, and functions vary even for the same addresses depending on the mode. Refer to the registers of each function for details. Also, the differences between clock synchronous communication mode and clock synchronous serial mode are the options of the transfer clock, clock output format, and data output format.

26.1 Mode Selection

The clock synchronous serial interface supports four modes.

Table 26.1 lists the Mode Selections. Refer to **27. Synchronous Serial Communication Unit (SSU)**, **28. I2C bus Interface** and the sections that follow for details of each mode.

Table 26.1 Mode Selections

IICSEL Bit in SSUIICSR Register	Bit 7 in 0198h (ICE Bit in ICCR1 Register)	Bit 0 in 019Dh (SSUMS Bit in SSMR2 Register, FS Bit in SAR Register)	Function	Mode
0	0	0	Synchronous serial communication unit	Clock synchronous communication mode
0	0	1		4-wire bus communication mode
1	1	0	I2C bus interface	I2C bus interface mode
1	1	1		Clock synchronous serial mode

27. Synchronous Serial Communication Unit (SSU)

The synchronous serial communication unit (SSU) supports clock synchronous serial data communication.

27.1 Introduction

Table 27.1 shows the Synchronous Serial Communication Unit Specifications. Figure 27.1 shows a Block Diagram of Synchronous Serial Communication Unit.

Table 27.1 Synchronous Serial Communication Unit Specifications

Item	Specification
Transfer data format	• Transfer data length: 8 to 16 bits Continuous transmission and reception of serial data are enabled since both transmitter and receiver have buffer structures.
Operating modes	• Clock synchronous communication mode • 4-wire bus communication mode (including bidirectional communication)
Master/slave device	Selectable
I/O pins	SSCK (I/O): Clock I/O pin SSI (I/O): Data I/O pin SSO (I/O): Data I/O pin $\overline{\text{SCS}}$ (I/O): Chip-select I/O pin
Transfer clocks	• When the MSS bit in the SSCRH register is set to 0 (operation as a slave device), an external clock is selected (input from the SSCK pin). • When the MSS bit in the SSCRH register is set to 1 (operation as the master device), an internal clock (selectable among f1/256, f1/128, f1/64, f1/32, f1/16, f1/8 and f1/4, output from the SSCK pin) is selected. • The clock polarity and the phase of SSCK can be selected.
Receive error detection	• Overrun error An overrun error occurs during reception and completes in error. While the RDRF bit in the SSSR register is set to 1 (data in the SSRDR register) and when the next serial data reception is completed, the ORER bit is set to 1.
Multimaster error detection	• Conflict error When the SSUMS bit in the SSMR2 register is set to 1 (4-wire bus communication mode) and the MSS bit in the SSCRH register is set to 1 (operation as the master device) and when starting a serial communication, the CE bit in the SSSR register is set to 1 if a low-level signal applies to the $\overline{\text{SCS}}$ pin input. When the SSUMS bit in the SSMR2 register is set to 1 (4-wire bus communication mode), the MSS bit in the SSCRH register is set to 0 (operation as a slave device) and the $\overline{\text{SCS}}$ pin input changes state from low to high, the CE bit in the SSSR register is set to 1.
Interrupt requests	5 interrupt requests (transmit end, transmit data empty, receive data full, overrun error, and conflict error) (1).
Selectable functions	• Data transfer direction Selectable MSB first or LSB first • SSCK clock polarity Selectable a low or high level when the clock stops • SSCK clock phase Selectable edges for data change and data download

Note:
1. All sources use a single interrupt vector table for the synchronous serial communication unit.

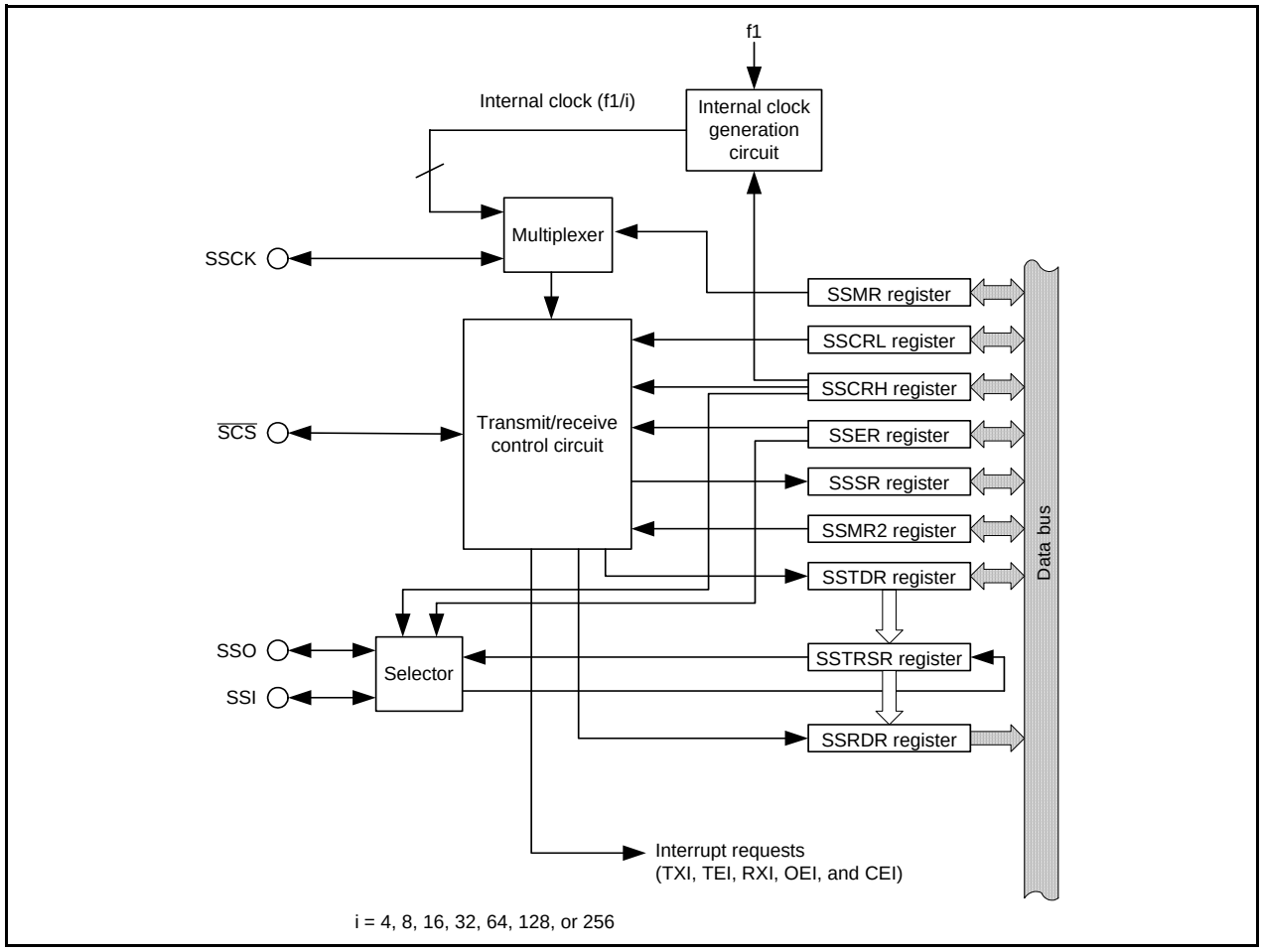


Figure 27.1 Block Diagram of Synchronous Serial Communication Unit

Table 27.2 Pin Configuration of Synchronous Serial Communication Unit

Pin Name	Assigned Pin	I/O	Function
SSI	P11_1	I/O	Data I/O
$\overline{\text{SCS}}$	P11_3	I/O	Chip-select signal I/O
SSCK	P11_0	I/O	Clock I/O
SSO	P11_2	I/O	Data I/O

27.2 Registers

27.2.1 Module Standby Control Register (MSTCR)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	MSTTRG	MSTTRC	MSTTRD	MSTIIC	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	MSTIIC	SSU, I^2C bus standby bit	0: Active 1: Standby (1)	R/W
b4	MSTTRD	Timer RD standby bit	0: Active 1: Standby (2)	R/W
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (3)	R/W
b6	MSTTRG	Timer RG standby bit	0: Active 1: Standby (4)	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. When the MSTIIC bit is set to 1 (standby), any access to the SSU or the I^2C bus associated registers (addresses 0193h to 019Dh) is disabled.
2. When the MSTTRD bit is set to 1 (standby), any access to the timer RD associated registers (addresses 0135h to 015Fh) is disabled.
3. When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0133h) is disabled.
4. When the MSTTRG bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0170h to 017Fh) is disabled.

27.2.2 SSU/IIC Pin Select Register (SSUIICSR)

Address 018Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	IICSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IICSEL	SSU/I^{2}C bus switch bit	0: SSU function selected 1: I^{2}C bus function selected	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

27.2.3 SS Bit Counter Register (SSBR)

Address 0193h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	BS3	BS2	BS1	BS0
After Reset	1	1	1	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	BS0	SSU data transfer length set bit (1)	b3 b2 b1 b0 0 0 0 0: 16 bits 1 0 0 0: 8 bits 1 0 0 1: 9 bits 1 0 1 0: 10 bits 1 0 1 1: 11 bits 1 1 0 0: 12 bits 1 1 0 1: 13 bits 1 1 1 0: 14 bits 1 1 1 1: 15 bits	R/W
b1	BS1			R/W
b2	BS2			R/W
b3	BS3			R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			—
b6	—			—
b7	—			—

Note:
1. Do not write to bits BS0 to BS3 during the SSU operation. Write to these bits when the RE bit in the SSER register is set to 0 (reception disabled) and the TE bit is set to 0 (transmission disabled).
   To set the SSBR register, set the RE bit in the SSER register to 0 and the TE bit to 0.

Bits BS0 to BS3 (SSU Data Transfer Length Set Bit)

From 8 to 16 bits can be used as the SSU data transfer length.

27.2.4 SS Transmit Data Register (SSTDR)

Address 0195h to 0194h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
b15 to b0	—	This register stores transmit data. When the SSTRSR register is detected as empty, the stored transmit data is transferred to the SSTRSR register and transmission starts. When the next transmit data is written to the SSTDR register during the data transmission from the SSTRSR register, continuous transmission is enabled. When the MLS bit in the SSMR register is set to 1 (transfer data with LSB first), the MSB-LSB inverted data is read after writing to the SSTDR register.	R/W

27.2.5 SS Receive Data Register (SSRDR)

Address 0197h to 0196h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
b15 to b0	—	This register stores receive data. (1) The receive data is transferred to the SSRDR register and the receive operation is completed when 1 byte of data has been received by the SSTRSR register. At this time, the next reception is enabled. Continuous reception is enabled using registers SSTRSR and SSRDR.	R

Note:
1. When the ORER bit in the SSSR register is set to 1 (overrun error), the SSRDR register retains the data received before an overrun error occurs. When an overrun error occurs, the receive data is discarded.

27.2.6 SS Control Register H (SSCRH)

Address 0198h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	RSSTP	MSS	—	—	CKS2	CKS1	CKS0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CKS0	Transfer clock select bit (1)	b2 b1 b0 0 0 0: f1/256 0 0 1: f1/128 0 1 0: f1/64 0 1 1: f1/32 1 0 0: f1/16 1 0 1: f1/8 1 1 0: f1/4 1 1 1: Do not set.	R/W
b1	CKS1			R/W
b2	CKS2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	MSS	Master/slave device select bit (2)	0: Operation as a slave device 1: Operation as the master device	R/W
b6	RSSTP	Receive single stop bit (3)	0: Receive operation is continued after receiving 1 byte of data 1: Receive operation is completed after receiving 1 byte of data	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. The set clock is used when an internal clock is selected.
2. The SSCK pin functions as the transfer clock output pin when the MSS bit is set to 1 (operation as the master device). The MSS bit is set to 0 (operation as a slave device) when the CE bit in the SSSR register is set to 1 (conflict error occurs).
3. The RSSTP bit is disabled when the MSS bit is set to 0 (operation as a slave device).

27.2.7 SS Control Register L (SSCRL)

Address 0199h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	SOL	SOLP	—	—	SRES	—
After Reset	0	1	1	1	1	1	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b1	SRES	SSU control unit reset bit	When 1 is written to this bit, the SSU control unit and the SSTRSR register are reset. The value of the SSU internal register (1) is retained.	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b3	—			
b4	SOLP	SOL write protect bit (2)	When 0 is written to this bit, the output level can be changed by the SOL bit. The SOLP bit remains unchanged even if 1 is written to it. When read, the content is 1.	R/W
b5	SOL	Serial data output value setting bit	When read 0: Serial data output is low 1: Serial data output is high When written (2, 3) 0: Data output is low after serial data output 1: Data output is high after serial data output	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. Registers SSBR, SSCRH, SSCRL, SSMR, SSER, SSSR, SSMR2, SSTDR, and SSRDR.
2. The data output after serial data output can be changed by writing to the SOL bit before or after transfer. When writing to the SOL bit, set the SOLP bit to 0 and the SOL bit to 0 or 1 simultaneously by the MOV instruction.
3. Do not write to the SOL bit during data transfer.

27.2.8 SS Mode Register (SSMR)

Address 019Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	MLS	CPOS	CPHS	—	BC3	BC2	BC1	BC0
After Reset	0	0	0	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	BC0	Bit counter 3 to 0	b3 b2 b1 b0 0 0 0 0: 16 bits left 0 0 0 1: 1 bit left 0 0 1 0: 2 bits left 0 0 1 1: 3 bits left 0 1 0 0: 4 bits left 0 1 0 1: 5 bits left 0 1 1 0: 6 bits left 0 1 1 1: 7 bits left 1 0 0 0: 8 bits left 1 0 0 1: 9 bits left 1 0 1 0: 10 bits left 1 0 1 1: 11 bits left 1 1 0 0: 12 bits left 1 1 0 1: 13 bits left 1 1 1 0: 14 bits left 1 1 1 1: 15 bits left	R
b1	BC1			R
b2	BC2			R
b3	BC3			R
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	CPHS	SSCK clock phase select bit (1)	0: Data change at odd edges (Data download at even edges) 1: Data change at even edges (Data download at odd edges)	R/W
b6	CPOS	SSCK clock polarity select bit (1)	0: High when clock stops 1: Low when clock stops	R/W
b7	MLS	MSB first/LSB first select bit	0: Transfer data with MSB first 1: Transfer data with LSB first	R/W

Note:
1. Refer to **27.3.1.1 Association between Transfer Clock Polarity, Phase, and Data** for the settings of bits CPHS and CPOS.

27.2.9 SS Enable Register (SSER)

Address 019Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIE	TEIE	RIE	TE	RE	—	—	CEIE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CEIE	Conflict error interrupt enable bit	0: Conflict error interrupt request disabled 1: Conflict error interrupt request enabled	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	RE	Reception enable bit	0: Reception disabled 1: Reception enabled	R/W
b4	TE	Transmission enable bit	0: Transmission disabled 1: Transmission enabled	R/W
b5	RIE	Receive interrupt enable bit	0: Receive data full and overrun error interrupt requests disabled 1: Receive data full and overrun error interrupt requests enabled	R/W
b6	TEIE	Transmit end interrupt enable bit	0: Transmit end interrupt request disabled 1: Transmit end interrupt request enabled	R/W
b7	TIE	Transmit interrupt enable bit	0: Transmit data empty interrupt request disabled 1: Transmit data empty interrupt request enabled	R/W

27.2.10 SS Status Register (SSSR)

Address 019Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TDRE	TEND	RDRF	—	—	ORER	—	CE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CE	Conflict error flag (1)	0: No conflict error 1: Conflict error (2)	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	ORER	Overrun error flag (1)	0: No overrun error 1: Overrun error (3)	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	RDRF	Receive data register full flag (1, 4)	0: No data in the SSRDR register 1: Data in the SSRDR register	R/W
b6	TEND	Transmit end flag (1, 5)	0: TDRE bit is set to 0 when transmitting the last bit of transmit data 1: TDRE bit is set to 1 when transmitting the last bit of transmit data	R/W
b7	TDRE	Transmit data empty flag (1, 5, 6)	0: No data transferred from registers SSTDR to SSTRSR 1: Data transferred from registers SSTDR to SSTRSR	R/W

Notes:

1. Writing 1 to the CE, ORER, RDRF, TEND, or TDRE bit is disabled. To set any of these bits to 0, first read 1 then write 0.
2. When the serial communication is started while the SSUMS bit in the SSMR2 register is set to 1 (4-wire bus communication mode) and the MSS bit in the SSCRH register is set to 1 (operation as the master device), the CE bit is set to 1 if a low-level signal is applied to the $\overline{SCS}$ pin input. Refer to **27.5.4 SCS Pin Control and Arbitration** for more information.
   When the SSUMS bit in the SSMR2 register is set to 1 (4-wire bus communication mode), the MSS bit in the SSCRH register is set to 0 (operation as a slave device) and the $\overline{SCS}$ pin input changes the level from low to high during transfer, the CE bit is set to 1.
3. Indicates when an overrun error occurs during reception and completes in error. If the next serial data receive operation is completed while the RDRF bit is set to 1 (data in the SSRDR register), the ORER bit is set to 1.
   After the ORER bit is set to 1 (overrun error), receive operation is disabled while the bit remains 1. Transmit operation is also disabled while the MSS bit is set to 1 (operation as the master device).
4. The RDRF bit is set to 0 when reading the data from the SSRDR register.
5. Bits TEND and TDRE are set to 0 when writing data to the SSTDR register.
6. The TDRE bit is set to 1 when the TE bit in the SSER register is set to 1 (transmission enabled).

To access the SSSR register successively, insert one or more NOP instructions between the instructions used for access.

27.2.11 SS Mode Register 2 (SSMR2)

Address 019Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BIDE	SCKS	CSS1	CSS0	SCKOS	SOOS	CSOS	SSUMS
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SSUMS	SSU mode select bit (1)	0: Clock synchronous communication mode 1: 4-wire bus communication mode	R/W
b1	CSOS	$\overline{SCS}$ pin open-drain output select bit	0: CMOS output 1: N-channel open-drain output	R/W
b2	SOOS	Serial data open-drain output select bit (1)	0: CMOS output (5) 1: N-channel open-drain output	R/W
b3	SCKOS	SSCK pin open-drain output select bit	0: CMOS output 1: N-channel open-drain output	R/W
b4	CSS0	$\overline{SCS}$ pin select bit (2)	b5 b4 0 0: Function as a port 0 1: Function as the $\overline{SCS}$ input pin 1 0: Function as the $\overline{SCS}$ output pin (3) 1 1: Function as the $\overline{SCS}$ output pin (3)	R/W
b5	CSS1			R/W
b6	SCKS	SSCK pin select bit	0: Function as a port 1: Function as the serial clock pin	R/W
b7	BIDE	Bidirectional mode enable bit (1, 4)	0: Standard mode (communication using 2 pins of data input and data output) 1: Bidirectional mode (communication using 1 pin of data input and data output)	R/W

Notes:
1. Refer to **27.3.2.1 Association between Data I/O Pins and SS Shift Register** for information on the combinations of data I/O pins.
2. The $\overline{SCS}$ pin functions as a port, regardless of the values of bits CSS0 and CSS1 when the SSUMS bit is set to 0 (clock synchronous communication mode).
3. This bit functions as the $\overline{SCS}$ input pin before starting transfer.
4. The BIDE bit is disabled when the SSUMS bit is set to 0 (clock synchronous communication mode).
5. When the SOOS bit is set to 0 (CMOS output), set the port direction register bits corresponding to pins SSI and SSO to 0 (input mode).

27.3 Common Items for Multiple Modes

27.3.1 Transfer Clock

The transfer clock can be selected from among seven internal clocks (f1/256, f1/128, f1/64, f1/32, f1/16, f1/8, and f1/4) and an external clock.

To use the synchronous serial communication unit, set the SCKS bit in the SSMR2 register to 1 and select the SSCK pin as the serial clock pin.

When the MSS bit in the SSCRH register is set to 1 (operation as the master device), an internal clock can be selected and the SSCK pin functions as output. When transfer is started, the SSCK pin outputs a clock at the transfer rate selected by bits CKS0 to CKS2 in the SSCRH register.

When the MSS bit in the SSCRH register is set to 0 (operation as a slave device), an external clock can be selected and the SSCK pin functions as input.

27.3.1.1 Association between Transfer Clock Polarity, Phase, and Data

The association between the transfer clock polarity, phase, and data changes according to the combination of the SSUMS bit in the SSMR2 register and bits CPHS and CPOS in the SSMR register.

Figure 27.2 shows the Association between Transfer Clock Polarity, Phase, and Transfer Data.

Also, the MSB-first transfer or LSB-first transfer can be selected by setting the MLS bit in the SSMR register. When the MLS bit is set to 1, transfer is started from the LSB and proceeds to the MSB. When the MLS bit is set to 0, transfer is started from the MSB and proceeds to the LSB.

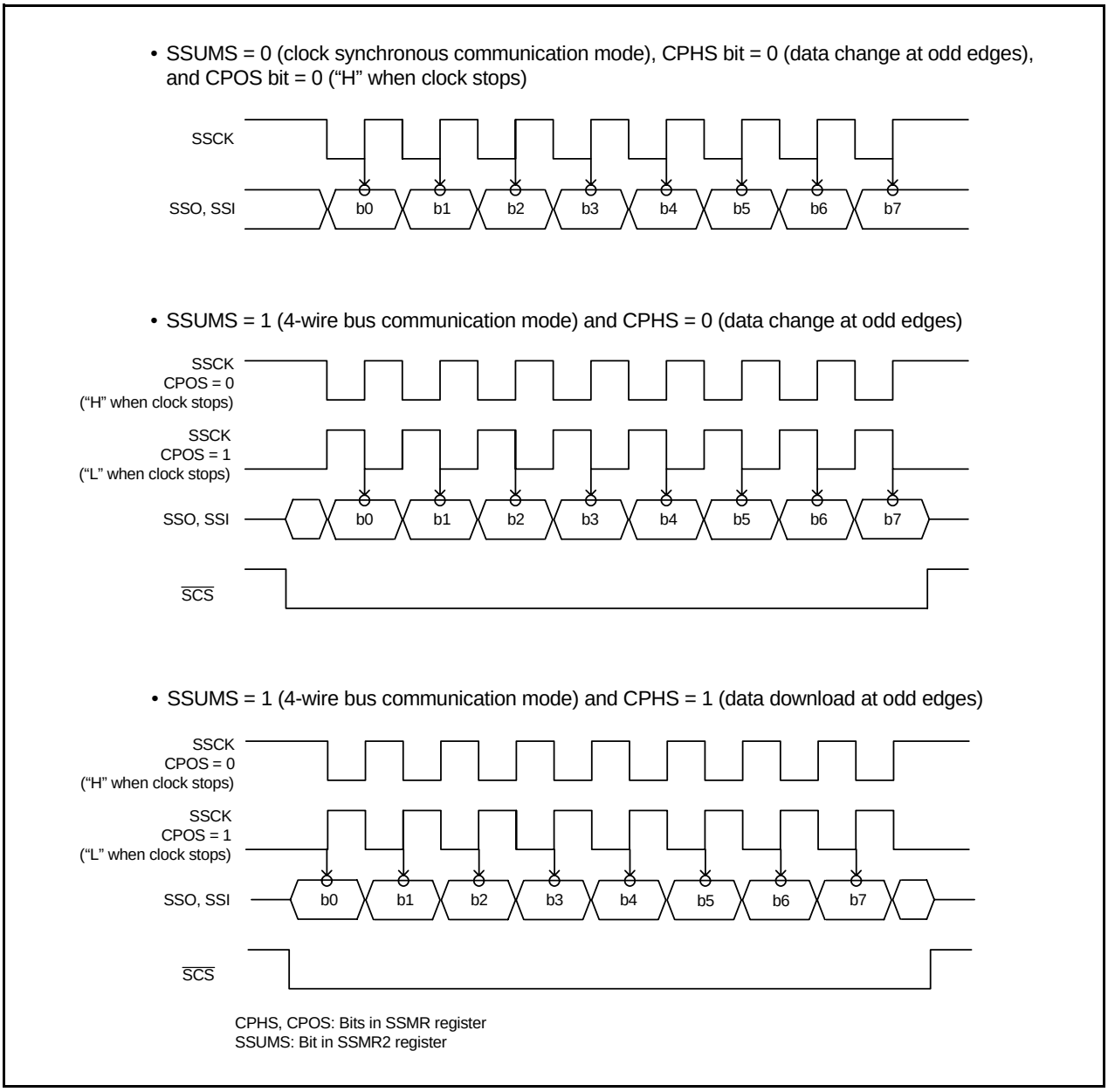


Figure 27.2 Association between Transfer Clock Polarity, Phase, and Transfer Data

27.3.2 SS Shift Register (SSTRSR)

The SSTRSR register is a shift register for transmitting and receiving serial data.
When transmit data is transferred from the SSTDR register to the SSTRSR register and the MLS bit in the SSMR register is set to 0 (MSB first), bit 0 in the SSTDR register is transferred to bit 0 in the SSTRSR register. When the MLS bit is set to 1 (LSB first), bit 7 in the SSTDR register is transferred to bit 0 in the SSTRSR register.

27.3.2.1 Association between Data I/O Pins and SS Shift Register

The connection between the data I/O pins and the SSTRSR register (SS shift register) changes according to a combination of the MSS bit in the SSCRH register and the SSUMS bit in the SSMR2 register. The connection also changes according to the BIDE bit in the SSMR2 register.
Figure 27.3 shows the Association between Data I/O Pins and SSTRSR Register.

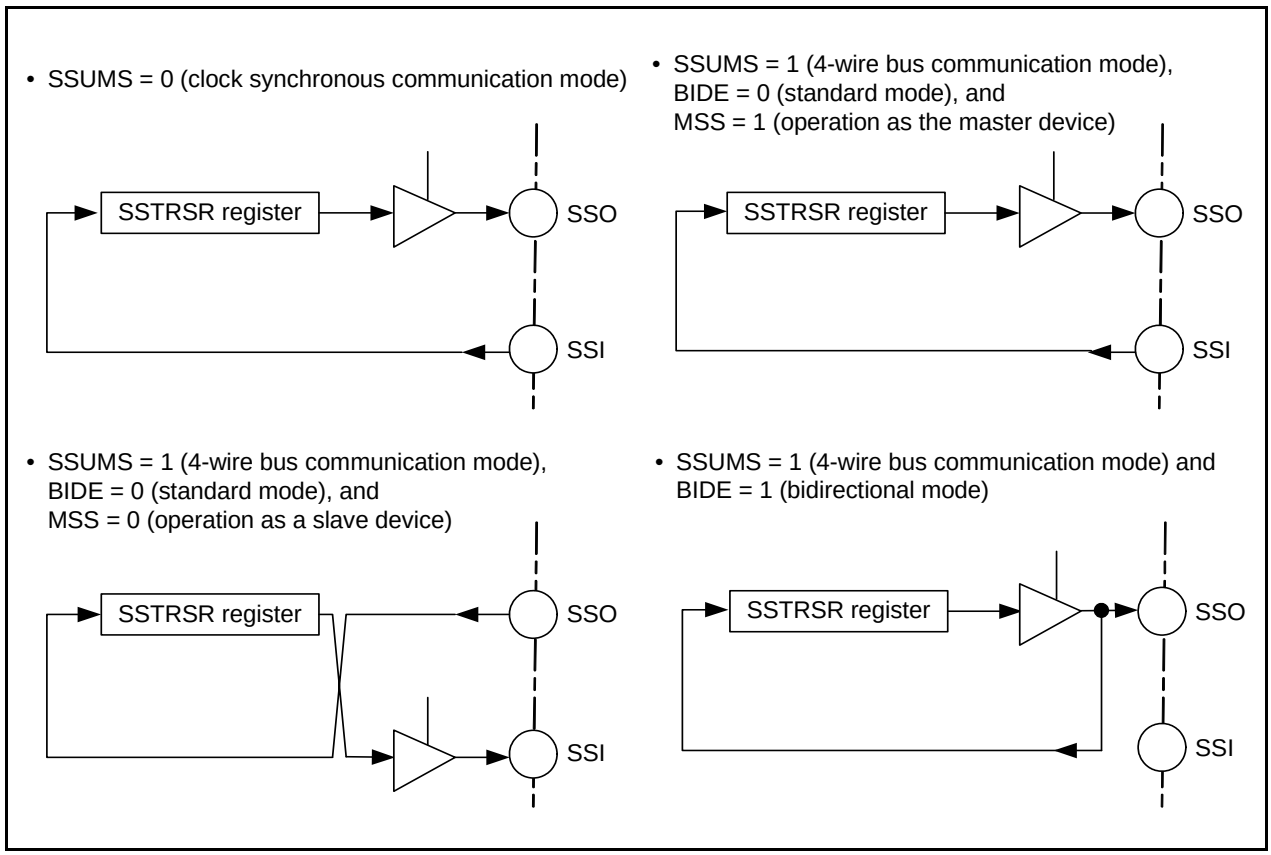


Figure 27.3 Association between Data I/O Pins and SSTRSR Register

27.3.3 Interrupt Requests

The synchronous serial communication unit has five interrupt requests: transmit data empty, transmit end, receive data full, overrun error, and conflict error. Since these interrupt requests are assigned to the synchronous serial communication unit interrupt vector table, determining interrupt sources by flags is required.
Table 27.3 shows the Interrupt Requests of Synchronous Serial Communication Unit.

Table 27.3 Interrupt Requests of Synchronous Serial Communication Unit

Interrupt Request	Abbreviation	Generation Condition
Transmit data empty	TXI	TIE = 1 and TDRE = 1
Transmit end	TEI	TEIE = 1 and TEND = 1
Receive data full	RXI	RIE = 1 and RDRF = 1
Overrun error	OEI	RIE = 1 and ORER = 1
Conflict error	CEI	CEIE = 1 and CE = 1

CEIE, RIE, TEIE, TIE: Bits in SSER register
ORER, RDRF, TEND, TDRE: Bits in SSSR register

If the generation conditions in Table 27.3 are met, an interrupt request of the synchronous serial communication unit is generated. Set each interrupt source to 0 by the synchronous serial communication unit interrupt routine.

However, bits TDRE and TEND are automatically set to 0 by writing transmit data to the SSTDR register and the RDRF bit is automatically set to 0 by reading the SSRDR register. In particular, the TDRE bit is set to 1 (data transferred from registers SSTDR to SSTRSR) at the same time transmit data is written to the SSTDR register. If the TDRE bit is further set to 0 (data not transferred from registers SSTDR to SSTRSR), additional 1 byte may be transmitted.

27.3.4 Communication Modes and Pin Functions

The synchronous serial communication unit switches the functions of the I/O pins in each communication mode according to the setting of the MSS bit in the SSCRH register and bits RE and TE in the SSER register. Table 27.4 shows the Association between Communication Modes and I/O Pins.

Table 27.4 Association between Communication Modes and I/O Pins

Communication Mode	Bit Setting					Pin State		
	SSUMS	BIDE	MSS	TE	RE	SSI	SSO	SSCK
Clock synchronous communication mode	0	Disabled	0	0	1	Input	– (1)	Input
				1	0	– (1)	Output	Input
					1	Input	Output	Input
			1	0	1	Input	– (1)	Output
				1	0	– (1)	Output	Output
					1	Input	Output	Output
4-wire bus communication mode	1	0	0	0	1	– (1)	Input	Input
				1	0	Output	– (1)	Input
					1	Output	Input	Input
			1	0	1	Input	– (1)	Output
				1	0	– (1)	Output	Output
					1	Input	Output	Output
4-wire bus (bidirectional) communication mode (2)	1	1	0	0	1	– (1)	Input	Input
				1	0	– (1)	Output	Input
			1	0	1	– (1)	Input	Output
				1	0	– (1)	Output	Output

Notes:
1. This pin can be used as a programmable I/O port.
2. Do not set both bits TE and RE to 1 in 4-wire bus (bidirectional) communication mode.

SSUMS, BIDE: Bits in SSMR2 register
MSS: Bit in SSCRH register
TE, RE: Bits in SSER register

27.4 Clock Synchronous Communication Mode

27.4.1 Initialization in Clock Synchronous Communication Mode

Figure 27.4 shows Initialization in Clock Synchronous Communication Mode. Before data transmission or reception, set the TE bit in the SSER register to 0 (transmission disabled) and the RE bit to 0 (reception disabled), and initialize the synchronous serial communication unit.
Set the TE bit to 0 and the RE bit to 0 before changing the communication mode or format.
Setting the RE bit to 0 does not change the contents of flags RDRF and ORER or the contents of the SSRDR register.

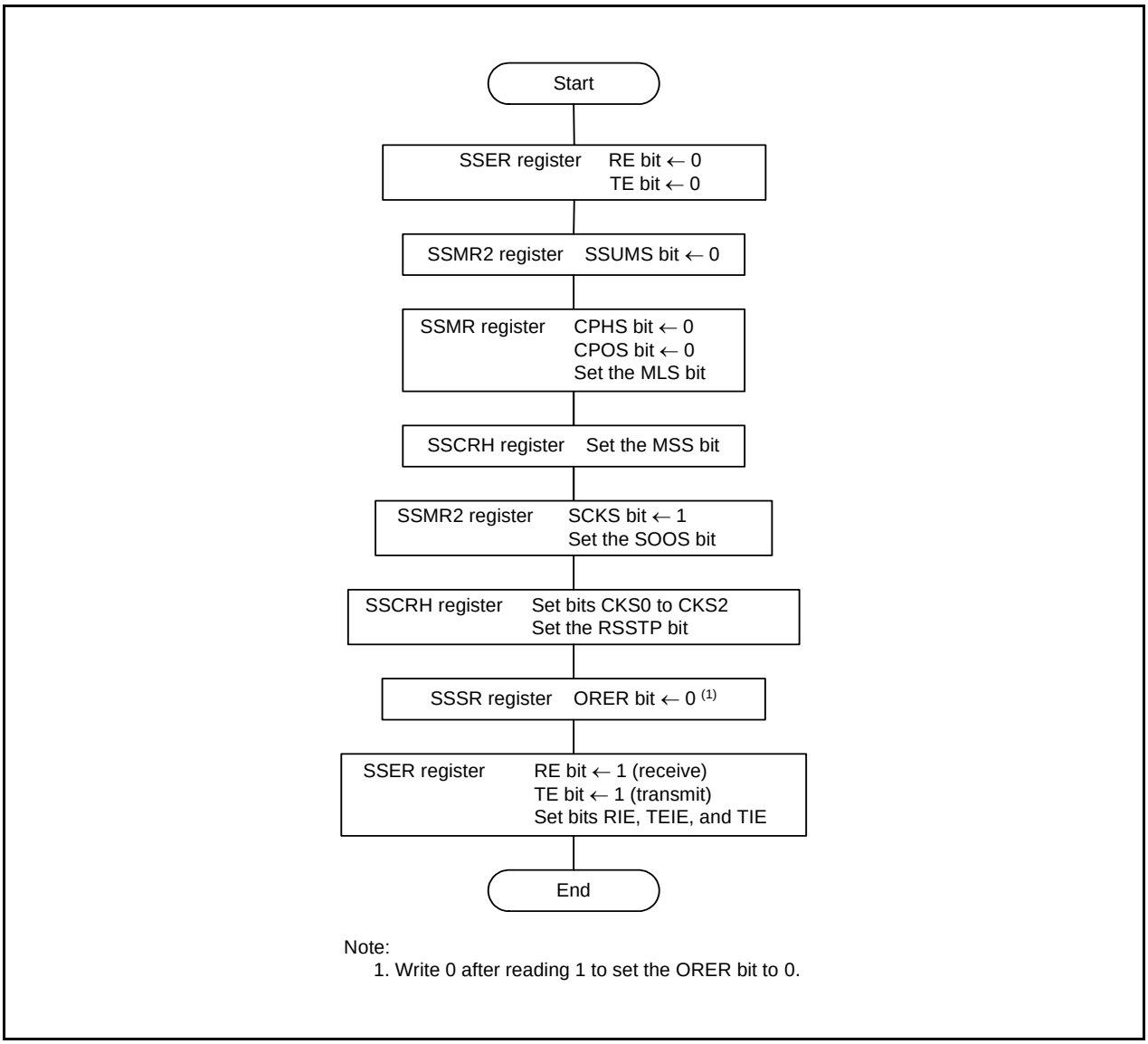


Figure 27.4 Initialization in Clock Synchronous Communication Mode

27.4.2 Data Transmission

Figure 27.5 shows an Example of Synchronous Serial Communication Unit Operation during Data Transmission (Clock Synchronous Communication Mode). During data transmission, the synchronous serial communication unit operates as described below.

When the synchronous serial communication unit is set as the master device, it outputs a synchronous clock and data. When the synchronous serial communication unit is set as a slave device, it outputs data synchronized with the input clock.

When the TE bit is set to 1 (transmission enabled) before writing the transmit data to the SSTDR register, the TDRE bit is automatically set to 0 (data not transferred from registers SSTDR to SSTRSR) and the data is transferred from registers SSTDR to SSTRSR. After the TDRE bit is set to 1 (data transferred from registers SSTDR to SSTRSR), transmission starts. When the TIE bit in the SSER register is set to 1 at this time, a TXI interrupt request is generated.

When one frame of data is transferred while the TDRE bit is set to 0, data is transferred from registers SSTDR to SSTRSR and transmission of the next frame is started. If the 8th bit is transmitted while the TDRE bit is set to 1, the TEND bit in the SSSR register is set to 1 (TDRE bit is set to 1 when the last bit of the transmit data is transmitted) and the state is retained. When the TEIE bit in the SSER register is set to 1 (transmit-end interrupt request enabled) at this time, a TEI interrupt request is generated. The SSCK pin is fixed high after transmit-end.

Transmission cannot be performed while the ORER bit in the SSSR register is set to 1 (overrun error). Confirm that the ORER bit is set to 0 before transmission.

Figure 27.6 shows a Sample Flowchart of Data Transmission (Clock Synchronous Communication Mode).

The data transfer length can be set from 8 to 16 bits using the SSBR register.

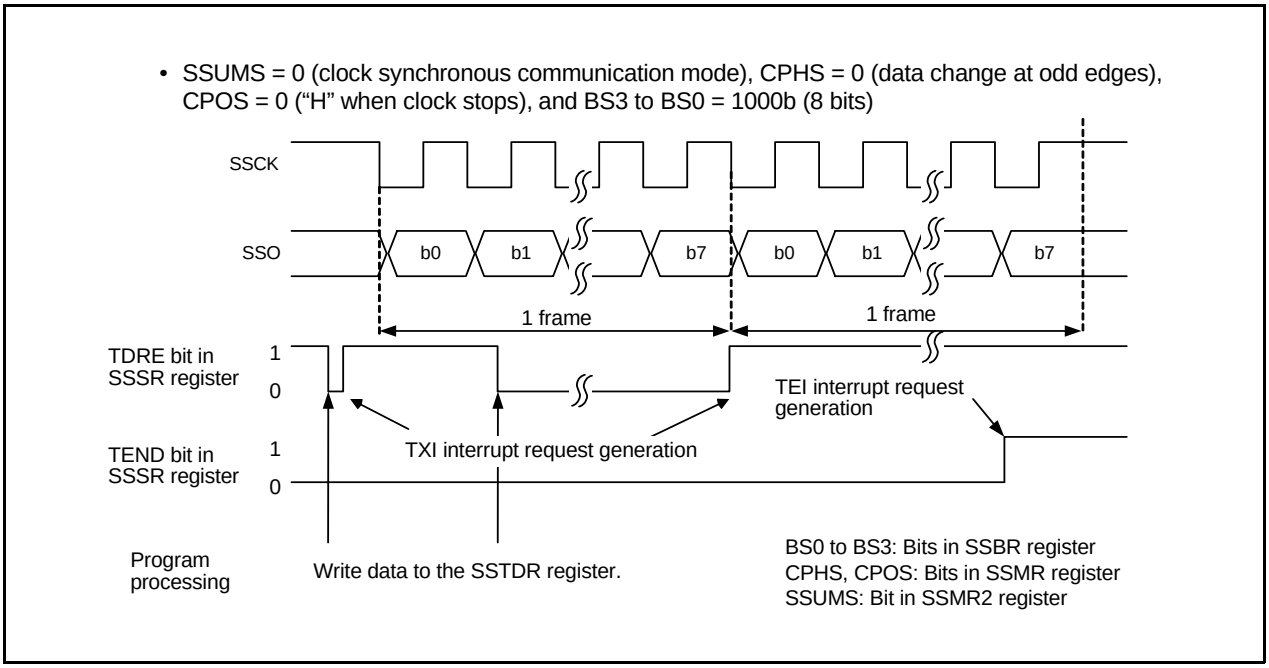
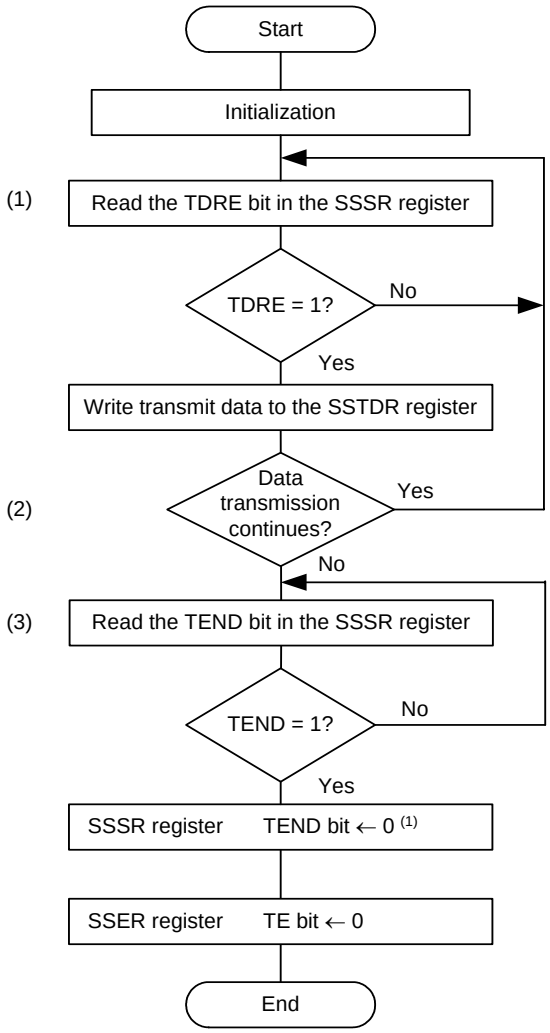


Figure 27.5 Example of Synchronous Serial Communication Unit Operation during Data Transmission (Clock Synchronous Communication Mode)



(1) After reading the SSSR register and confirming that the TDRE bit is set to 1, write the transmit data to the SSTDR register. When the transmit data is written to the SSTDR register, the TDRE bit is automatically set to 0.

(2) Determine whether data transmission continues.

(3) When data transmission is completed, the TEND bit is set to 1. Set the TEND bit to 0 and the TE bit to 0 and end transmit mode.

Note:
1. Write 0 after reading 1 to set the TEND bit to 0.

Figure 27.6 Sample Flowchart of Data Transmission (Clock Synchronous Communication Mode)

27.4.3 Data Reception

Figure 27.7 shows an Example of Synchronous Serial Communication Unit Operation during Data Reception (Clock Synchronous Communication Mode). During data reception, the synchronous serial communication unit operates as described below.

When the synchronous serial communication unit is set as the master device, it outputs a synchronous clock and inputs data. When the synchronous serial communication unit is set as a slave device, it inputs data synchronized with the input clock.

When the synchronous serial communication unit is set as the master device, it outputs a receive clock and starts receiving by performing dummy read from the SSRDR register.

After 8 bits of data are received, the RDRF bit in the SSSR register is set to 1 (data in the SSRDR register) and receive data is stored in the SSRDR register. When the RIE bit in the SSER register is set to 1 (RXI and OEI interrupt requests enabled) at this time, an RXI interrupt request is generated. If the SSDR register is read, the RDRF bit is automatically set to 0 (no data in the SSRDR register).

Read the receive data after setting the RSSTP bit in the SSCRH register to 1 (receive operation is completed after receiving 1 byte of data). The synchronous serial communication unit outputs a clock for receiving 8 bits of data and stops. After that, set the RE bit in the SSER register to 0 (reception disabled) and the RSSTP bit to 0 (receive operation is continued after receiving the 1 byte of data) and read the receive data. If the SSRDR register is read while the RE bit is set to 1 (reception enabled), a receive clock is output again.

When the 8th clock rises while the RDRF bit is set to 1, the ORER bit in the SSSR register is set to 1 (overrun error: OEI) and the operation is stopped. When the ORER bit is set to 1, reception cannot be performed. Confirm that the ORER bit is set to 0 before restarting reception.

Figure 27.8 shows a Sample Flowchart of Data Reception (MSS = 1) (Clock Synchronous Communication Mode).

The data transfer length can be set from 8 to 16 bits using the SSBR register.

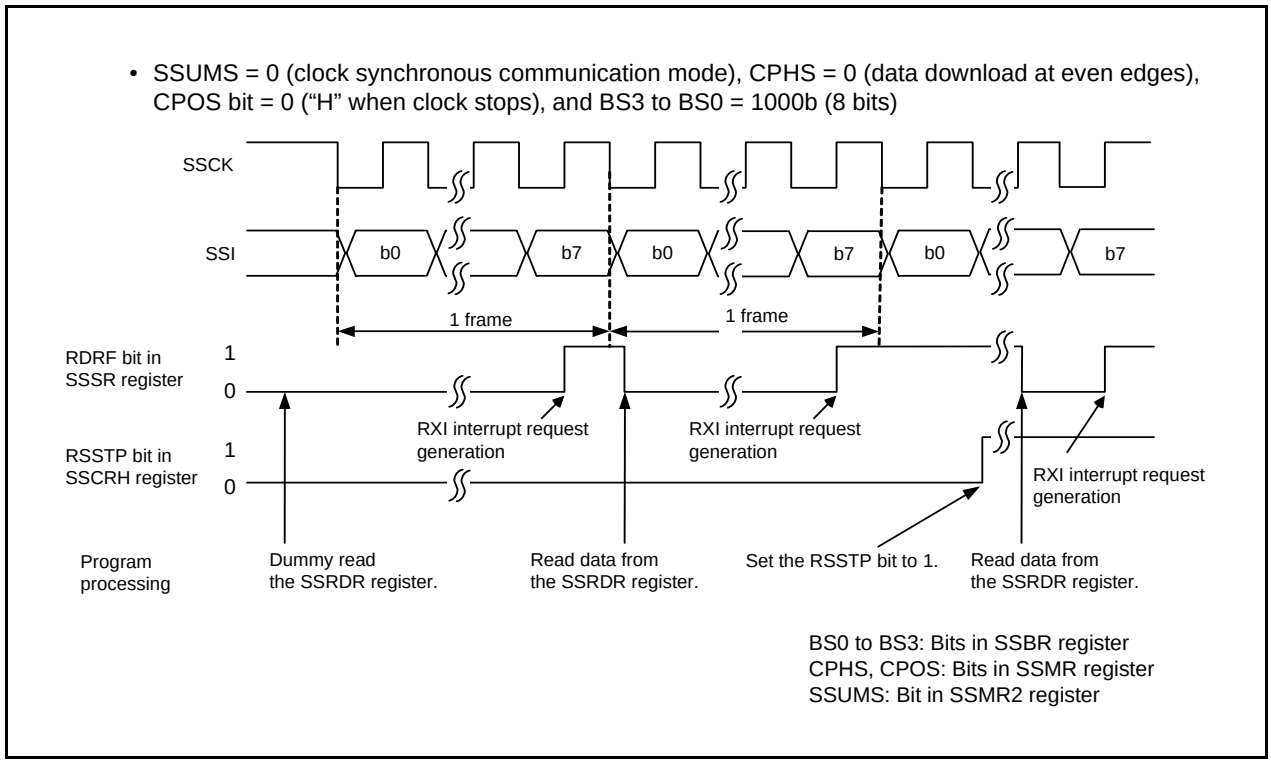


Figure 27.7 Example of Synchronous Serial Communication Unit Operation during Data Reception (Clock Synchronous Communication Mode)

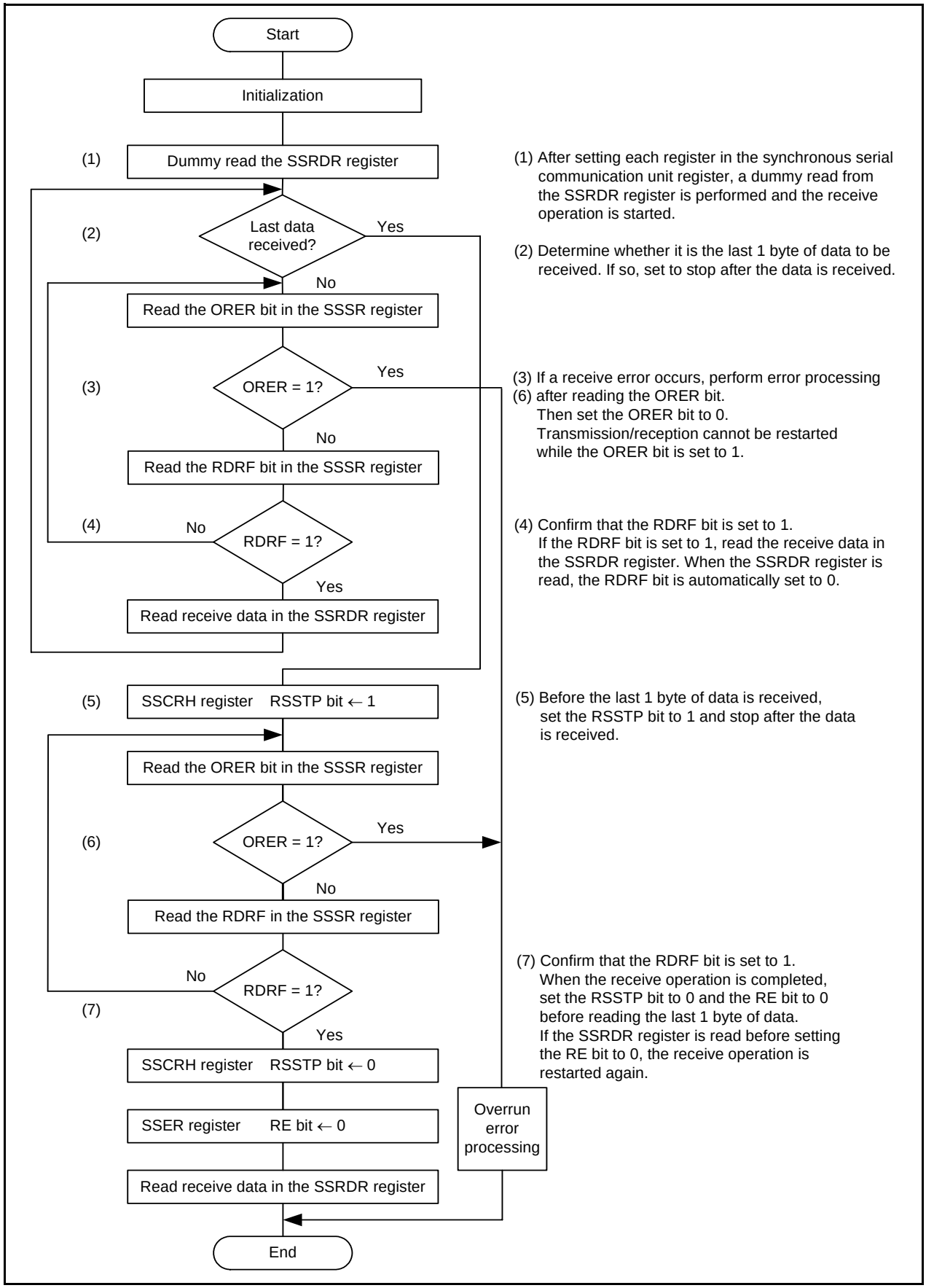


Figure 27.8 Sample Flowchart of Data Reception (MSS = 1) (Clock Synchronous Communication Mode)

27.4.3.1 Data Transmission/Reception

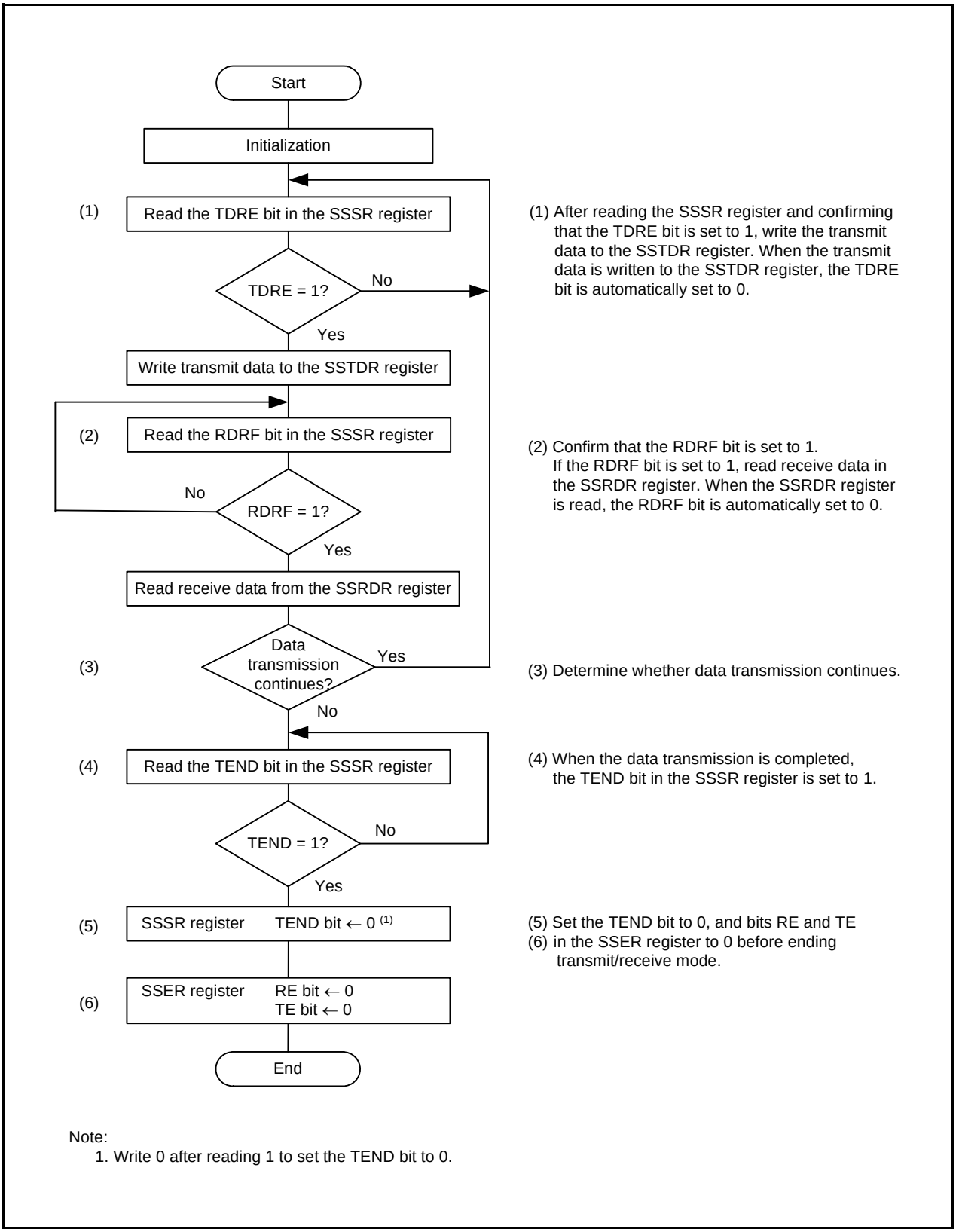
Data transmission/reception is an operation combining data transmission and reception which were described earlier.

Transmission/reception is started by writing data to the SSTDR register. When the 8th clock rises or the ORER bit is set to 1 (overrun error) while the TDRE bit is set to 1 (data transferred from registers SSTDR to SSTRSR), the transmit/receive operation is stopped.

Before switching from transmit mode (TE = 1) or receive mode (RE = 1) to transmit/receive mode (TE = RE = 1), set the TE bit to 0 and RE bit to 0 once. After confirming that the TEND bit is set to 0 (TDRE bit is set to 0 when the last bit of the transmit data is transmitted), the RDRF bit is set to 0 (no data in the SSRDR register), and the ORER bit is set to 0 (no overrun error), set bits TE and RE to 1.

Figure 27.9 shows a Sample Flowchart of Data Transmission/Reception (Clock Synchronous Communication Mode).

The data transfer length can be set from 8 to 16 bits using the SSBR register.



Note:
1. Write 0 after reading 1 to set the TEND bit to 0.

Figure 27.9 Sample Flowchart of Data Transmission/Reception (Clock Synchronous Communication Mode)

27.5 Operation in 4-Wire Bus Communication Mode

In 4-wire bus communication mode, a 4-wire bus consisting of a clock line, a data input line, a data output line, and a chip select line is used for communication. This mode includes bidirectional mode in which the data input line and data output line function as a single pin.

The data input line and output line change according to the settings of the MSS bit in the SSCRH register and the BIDE bit in the SSMR2 register. For details, refer to **27.3.2.1 Association between Data I/O Pins and SS Shift Register**. In this mode, the clock polarity, phase, and data settings are performed by using bits CPOS and CPHS in the SSMR register. For details, refer to **27.3.1.1 Association between Transfer Clock Polarity, Phase, and Data**.

When this MCU is set as the master device, the chip select line controls output. When the synchronous serial communication unit is set as a slave device, the chip select line controls input. When it is set as the master device, the chip select line controls output of the $\overline{\text{SCS}}$ pin or controls output of a general port according to the setting of the CSS1 bit in the SSMR2 register. When the MCU is set as a slave device, the chip select line sets the $\overline{\text{SCS}}$ pin as input by setting bits CSS1 and CSS0 in the SSMR2 register to 01b.

In 4-wire bus communication mode, the MLS bit in the SSMR register is set to 0 and communication is performed MSB first.

27.5.1 Initialization in 4-Wire Bus Communication Mode

Figure 27.10 shows Initialization in 4-Wire Bus Communication Mode. Before the data transit/receive operation, set the TE bit in the SSER register to 0 (transmission disabled), the RE bit in the SSER register to 0 (reception disabled), and initialize the synchronous serial communication unit.
Set the TE bit to 0 and the RE bit to 0 before changing the communication mode or format.
Setting the RE bit to 0 does not change the settings of flags RDRF and ORER or the contents of the SSRDR register.

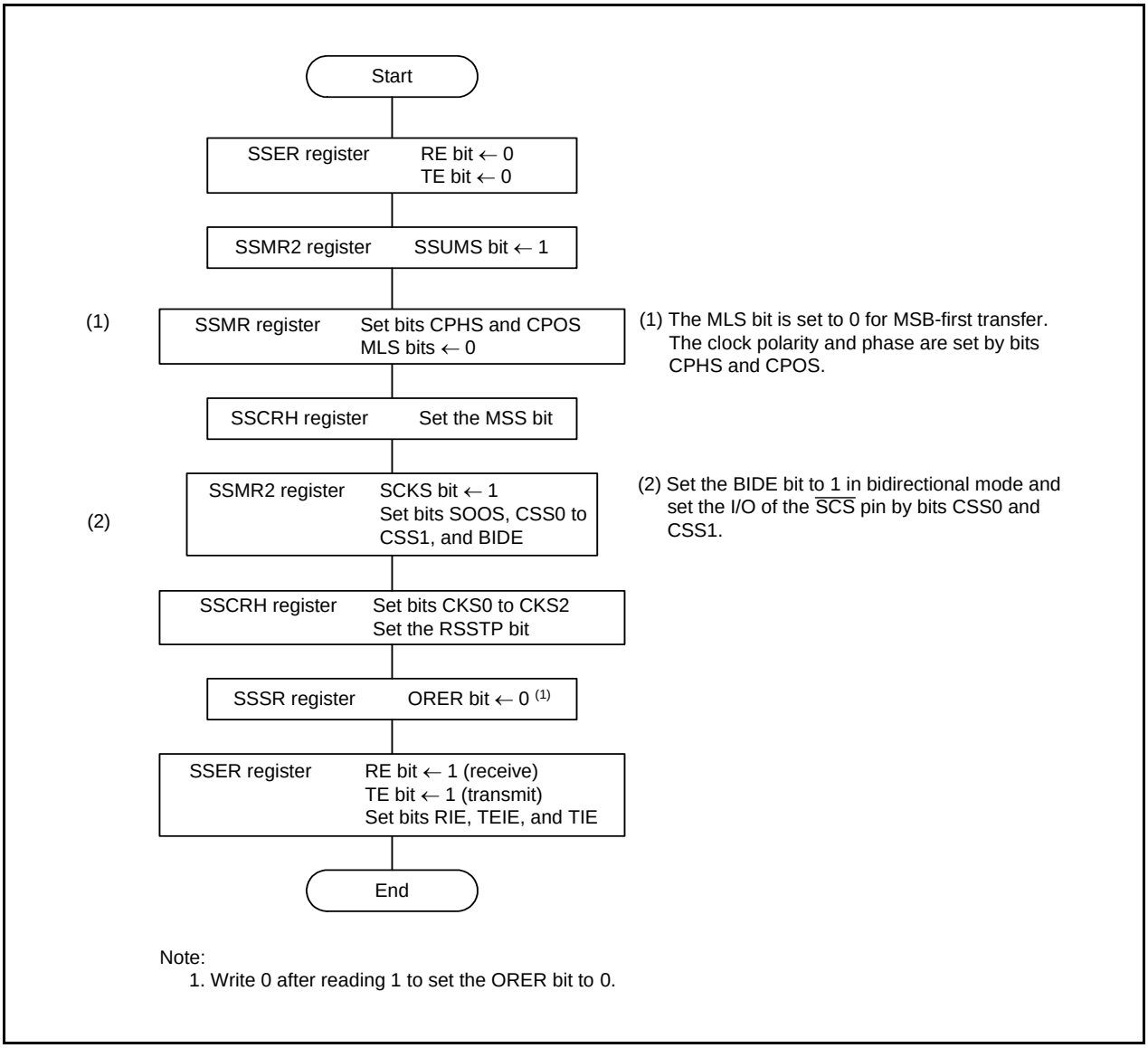


Figure 27.10 Initialization in 4-Wire Bus Communication Mode

27.5.2 Data Transmission

Figure 27.11 shows an Example of Synchronous Serial Communication Unit Operation during Data Transmission (4-Wire Bus Communication Mode). During the data transmit operation, the synchronous serial communication unit operates as described below.

When the MCU is set as the master device, it outputs a synchronous clock and data. When the MCU is set as a slave device, it outputs data in synchronization with the input clock while the $\overline{SCS}$ pin is low-input state.

When the transmit data is written to the SSTDR register after setting the TE bit to 1 (transmission enabled), the TDRE bit is automatically set to 0 (data not transferred from registers SSTDR to SSTRSR) and the data is transferred from registers SSTDR to SSTRSR. After the TDRE bit is set to 1 (data transferred from registers SSTDR to SSTRSR), transmission starts. When the TIE bit in the SSER register is set to 1 at this time, the TXI interrupt request is generated.

After one frame of data is transferred while the TDRE bit is set to 0, the data is transferred from registers SSTDR to SSTRSR and transmission of the next frame is started. If the 8th bit is transmitted while TDRE is set to 1, TEND in the SSSR register is set to 1 (when the last bit of the transmit data is transmitted, the TDRE bit is set to 1) and the state is retained. When the TEIE bit in the SSER register is set to 1 (transmit-end interrupt request enabled) at this time, the TEI interrupt request is generated. The SSCK pin remains high after transmit-end and the $\overline{SCS}$ pin is held high. When transmitting continuously while the $\overline{SCS}$ pin is held low, write the next transmit data to the SSTDR register before transmitting the 8th bit.

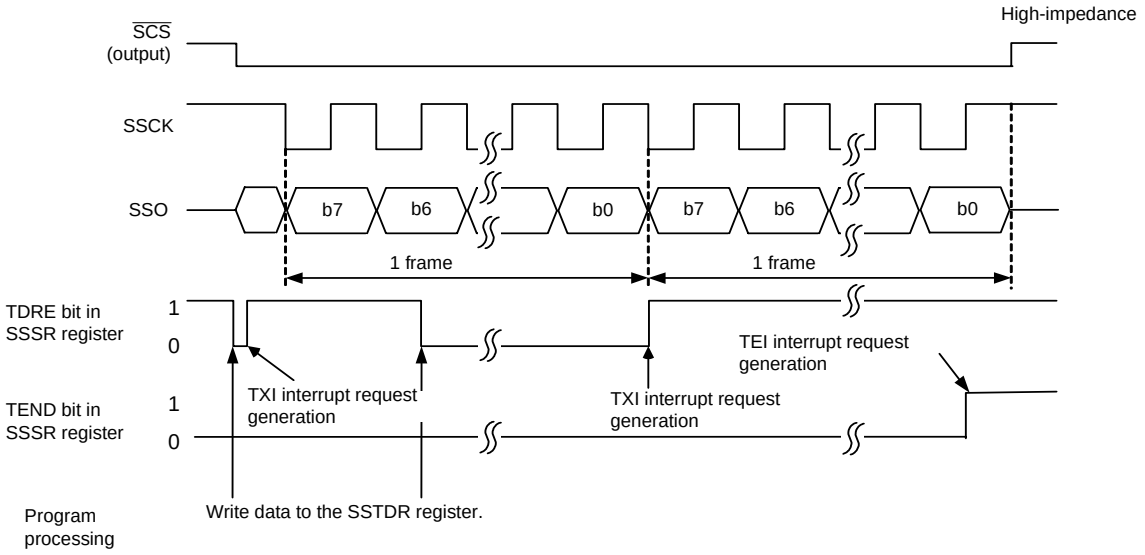
Transmission cannot be performed while the ORER bit in the SSSR register is set to 1 (overrun error). Confirm that the ORER bit is set to 0 before transmission.

In contrast to the clock synchronous communication mode, the SSO pin is placed in high-impedance state while the $\overline{SCS}$ pin is placed in high-impedance state when operating as the master device. The SSI pin is placed in high-impedance state while the $\overline{SCS}$ pin is high-input state when operating as a slave device.

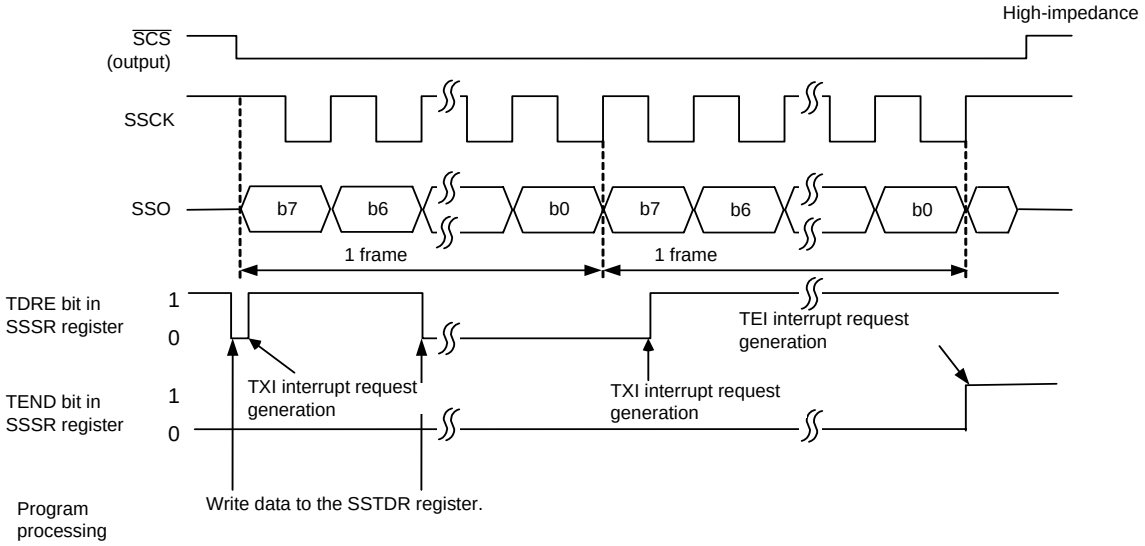
The sample flowchart is the same as that for the clock synchronous communication mode (refer to **Figure 27.6 Sample Flowchart of Data Transmission (Clock Synchronous Communication Mode)**).

The data transfer length can be set from 8 to 16 bits using the SSBR register.

• CPHS bit = 0 (data change at odd edges), CPOS bit = 0 (“H” when clock stops), and BS3 to BS0 = 1000b (8 bits)



• CPHS bit = 1 (data change at even edges). CPOS bit = 0 (“H” when clock stops), and BS3 to BS0 = 1000b (8 bits)



BS0 to BS3: Bits in SSBR register
CPHS, CPOS: Bits in SSMR register

Figure 27.11 Example of Synchronous Serial Communication Unit Operation during Data Transmission (4-Wire Bus Communication Mode)

27.5.3 Data Reception

Figure 27.12 shows an Example of Synchronous Serial Communication Unit Operation during Data Reception (4-Wire Bus Communication Mode). During data reception, the synchronous serial communication unit operates as described below.

When the MCU is set as the master device, it outputs a synchronous clock and inputs data. When the MCU is set as a slave device, it outputs data synchronized with the input clock while the $\overline{SCS}$ pin is low-input state.

When the MCU is set as the master device, it outputs a receive clock and starts receiving by performing a dummy read from the SSRDR register.

After 8 bits of data are received, the RDRF bit in the SSSR register is set to 1 (data in the SSRDR register) and receive data is stored in the SSRDR register. When the RIE bit in the SSER register is set to 1 (RXI and OEI interrupt requests enabled) at this time, an RXI interrupt request is generated. When the SSRDR register is read, the RDRF bit is automatically set to 0 (no data in the SSRDR register).

Read the receive data after setting the RSSTP bit in the SSCRH register to 1 (receive operation is completed after receiving 1-byte data). The synchronous serial communication unit outputs a clock for receiving 8 bits of data and stops. After that, set the RE bit in the SSER register to 0 (reception disabled) and the RSSTP bit to 0 (receive operation is continued after receiving 1-byte data) and read the receive data. When the SSRDR register is read while the RE bit is set to 1 (reception enabled), a receive clock is output again.

When the 8th clock rises while the RDRF bit is set to 1, the ORER bit in the SSSR register is set to 1 (overrun error: OEI) and the operation is stopped. When the ORER bit is set to 1, reception cannot be performed. Confirm that the ORER bit is set to 0 before restarting reception.

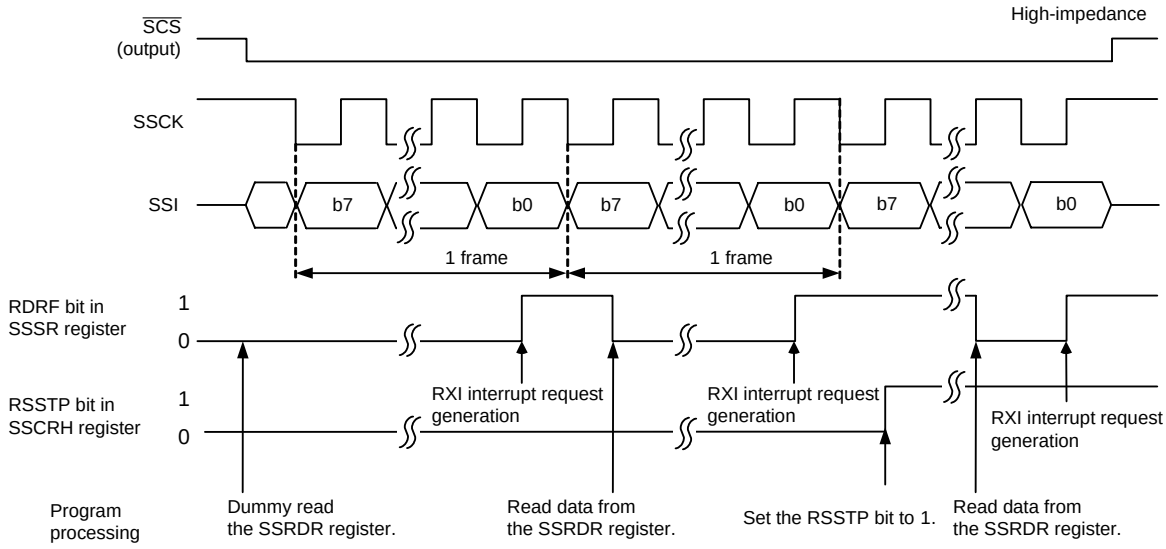
The timing at which bits RDRF and ORER are set to 1 varies depending on the setting of the CPHS bit in the SSMR register. Figure 27.12 shows when bits RDRF and ORER are set to 1.

When the CPHS bit is set to 1 (data download at odd edges), bits RDRF and ORER are set to 1 at some point during the frame.

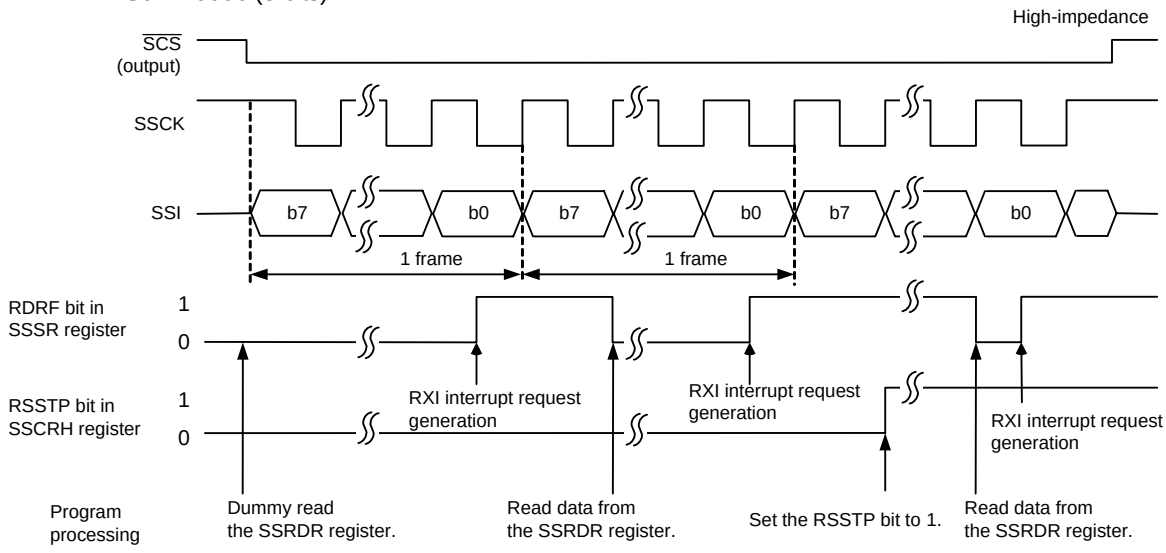
The sample flowchart is the same as that for the clock synchronous communication mode (refer to **Figure 27.8 Sample Flowchart of Data Reception (MSS = 1) (Clock Synchronous Communication Mode)**).

The data transfer length can be set from 8 to 16 bits using the SSBR register.

• CPHS bit = 0 (data download at even edges), CPOS bit = 0 (“H” when clock stops), and BS3 to BS0 = 1000b (8 bits)



• CPHS bit = 1 (data download at odd edges), CPOS bit = 0 (“H” when clock stops), and BS3 to BS0 = 1000b (8 bits)



BS0 to BS3: Bits in SSBR register
CPHS, CPOS: Bits in SSMR register

Figure 27.12 Example of Synchronous Serial Communication Unit Operation during Data Reception (4-Wire Bus Communication Mode)

27.5.4 $\overline{\text{SCS}}$ Pin Control and Arbitration

When the SSUMS bit in the SSMR2 register is set to 1 (4-wire bus communication mode) and the CSS1 bit is set to 1 (function as the $\overline{\text{SCS}}$ output pin), set the MSS bit in the SSCRH register to 1 (operation as the master device) and check the arbitration of the $\overline{\text{SCS}}$ pin before starting serial transfer. If the synchronous serial communication unit detects that the synchronized internal $\overline{\text{SCS}}$ signal is held low in this period, the CE bit in the SSSR register is set to 1 (conflict error) and the MSS bit is automatically set to 0 (operation as a slave device).
Figure 27.13 shows the Arbitration Check Timing.

Future transmit operations are not performed while the CE bit is set to 1. Set the CE bit to 0 (no conflict error) before starting transmission.

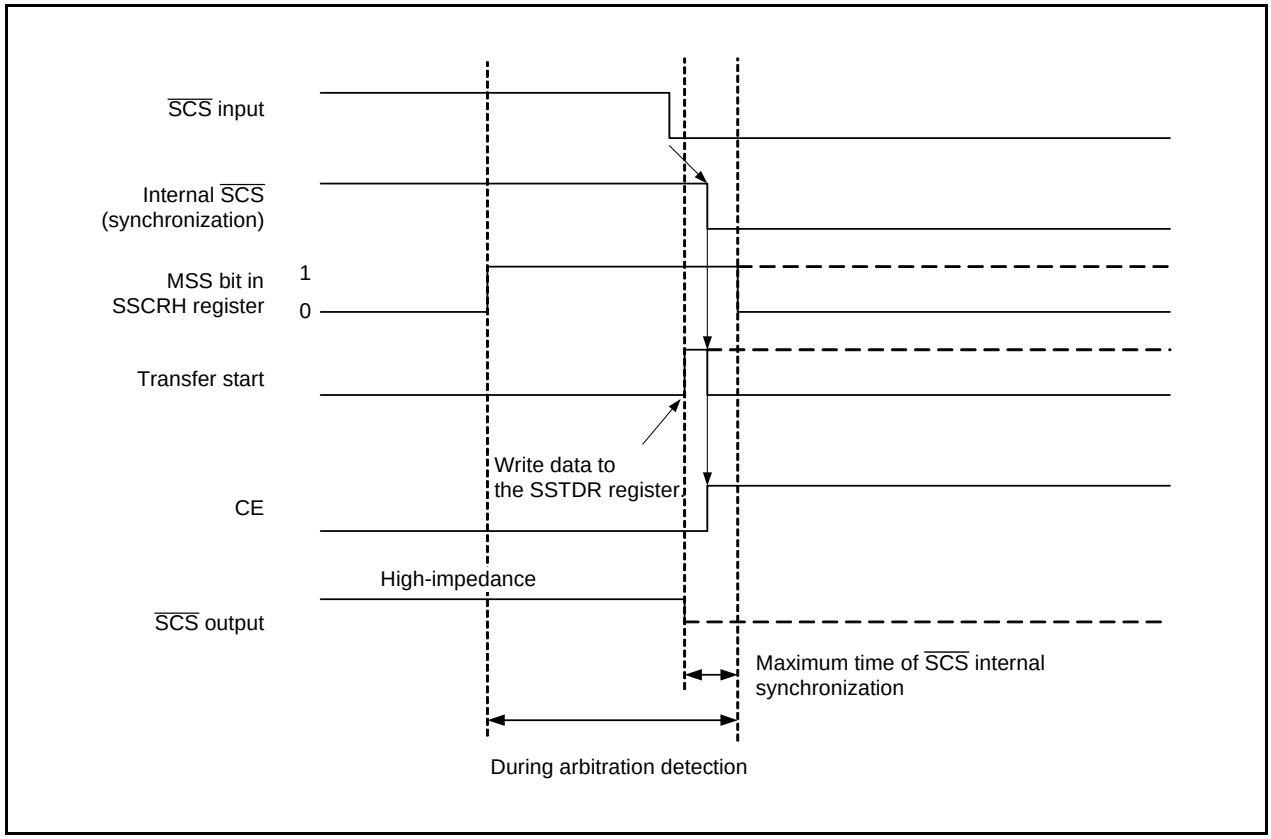


Figure 27.13 Arbitration Check Timing

27.6 Notes on Synchronous Serial Communication Unit

To use the synchronous serial communication unit, set the IICSEL bit in the SSUIICSR register to 0 (SSU function selected).

28. I2C bus Interface

The I2C bus interface is the circuit that performs serial communication based on the data transfer format of the Philips I2C bus.

28.1 Introduction

Table 28.1 lists the I2C bus Interface Specifications. Figure 28.1 shows a Block Diagram of I2C bus interface, and Figure 28.2 shows the External Circuit Connection Example of Pins SCL and SDA. Table 28.2 lists the I2C bus Interface Pin Configuration.

* I2C bus is a trademark of Koninklijke Philips Electronics N. V.

Table 28.1 I2C bus Interface Specifications

Item	Specification
Communication formats	• I2C bus format - Selectable as master/slave device - Continuous transmit/receive operation (because the shift register, transmit data register, and receive data register are independent) - Start/stop conditions are automatically generated in master mode. - Automatic loading of the acknowledge bit during transmission - Bit synchronization/wait function (In master mode, the state of the SCL signal is monitored per bit and the timing is synchronized automatically. If the transfer is not possible yet, the SCL signal goes low and the interface stands by.) - Support for direct drive of pins SCL and SDA (N-channel open-drain output) • Clock synchronous serial format - Continuous transmit/receive operation (because the shift register, transmit data register, and receive data register are independent)
I/O pins	SCL (I/O): Serial clock I/O pin SDA (I/O): Serial data I/O pin
Transfer clocks	• When the MST bit in the ICCR1 register is set to 0 External clock (input from the SCL pin) • When the MST bit in the ICCR1 register is set to 1 Internal clock selected by bits CKS0 to CKS3 in the ICCR1 register (output from the SCL pin)
Receive error detection	• Overrun error detection (clock synchronous serial format) Indicates an overrun error during reception. When the last bit of the next unit of data is received while the RDRF bit in the ICSR register is set to 1 (data in the ICDRR register), the AL bit is set to 1.
Interrupt sources	• I2C bus format ..... 6 sources (1) Transmit data empty (including when slave address matches), transmit end, receive data full (including when slave address matches), arbitration lost, NACK detection, and stop condition detection • Clock synchronous serial format ..... 4 sources (1) Transmit data empty, transmit end, receive data full, and overrun error
Selectable functions	• I2C bus format - Selectable output level for the acknowledge signal during reception • Clock synchronous serial format - Selectable MSB first or LSB first as the data transfer direction

Note:
1. All sources use a single interrupt vector table for the I2C bus interface.

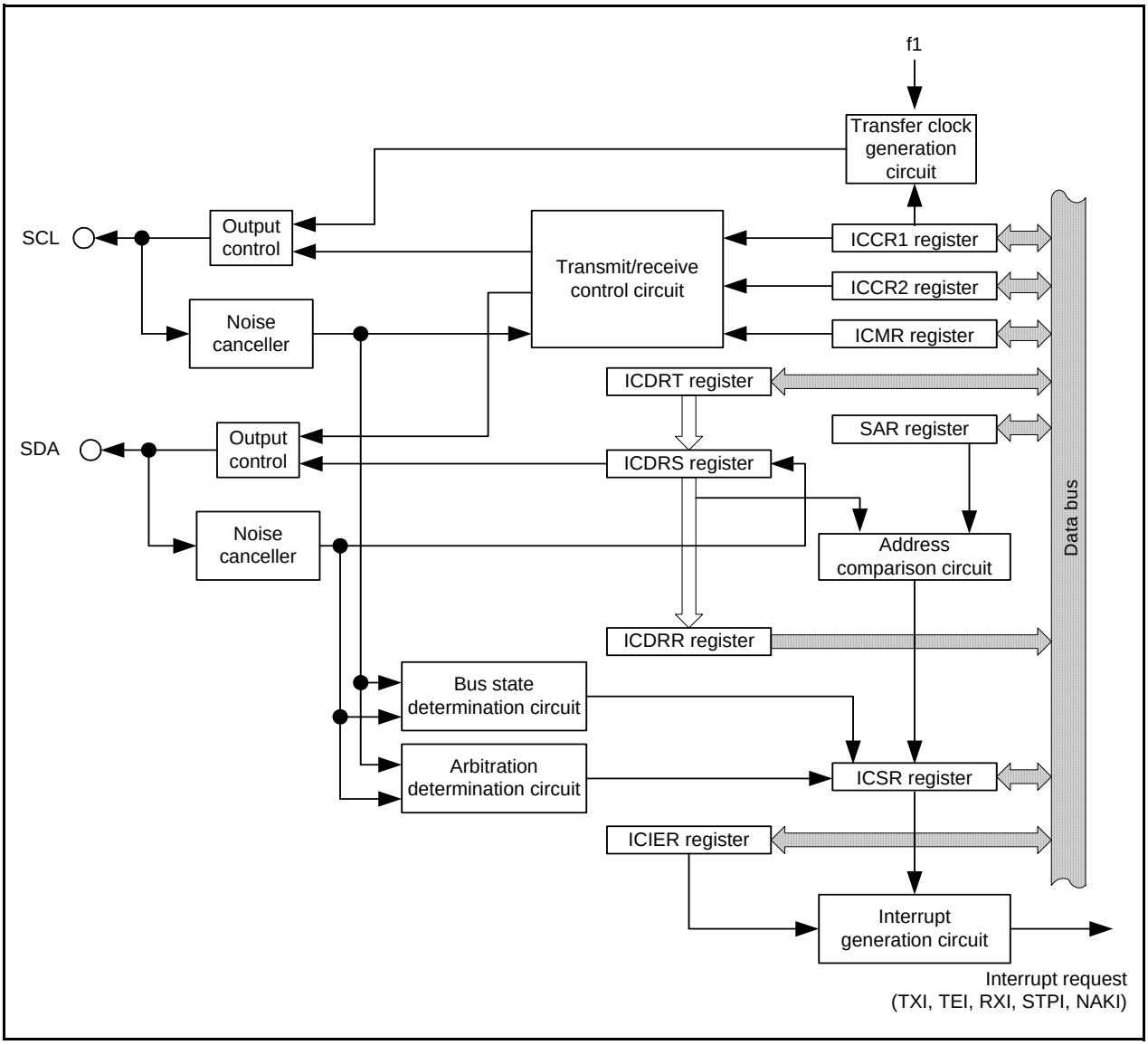


Figure 28.1 Block Diagram of I²C bus interface

Table 28.2 I²C bus Interface Pin Configuration

Pin Name	Assigned Pin	Function
SCL	P11_0	Clock I/O
SDA	P11_2	Data I/O

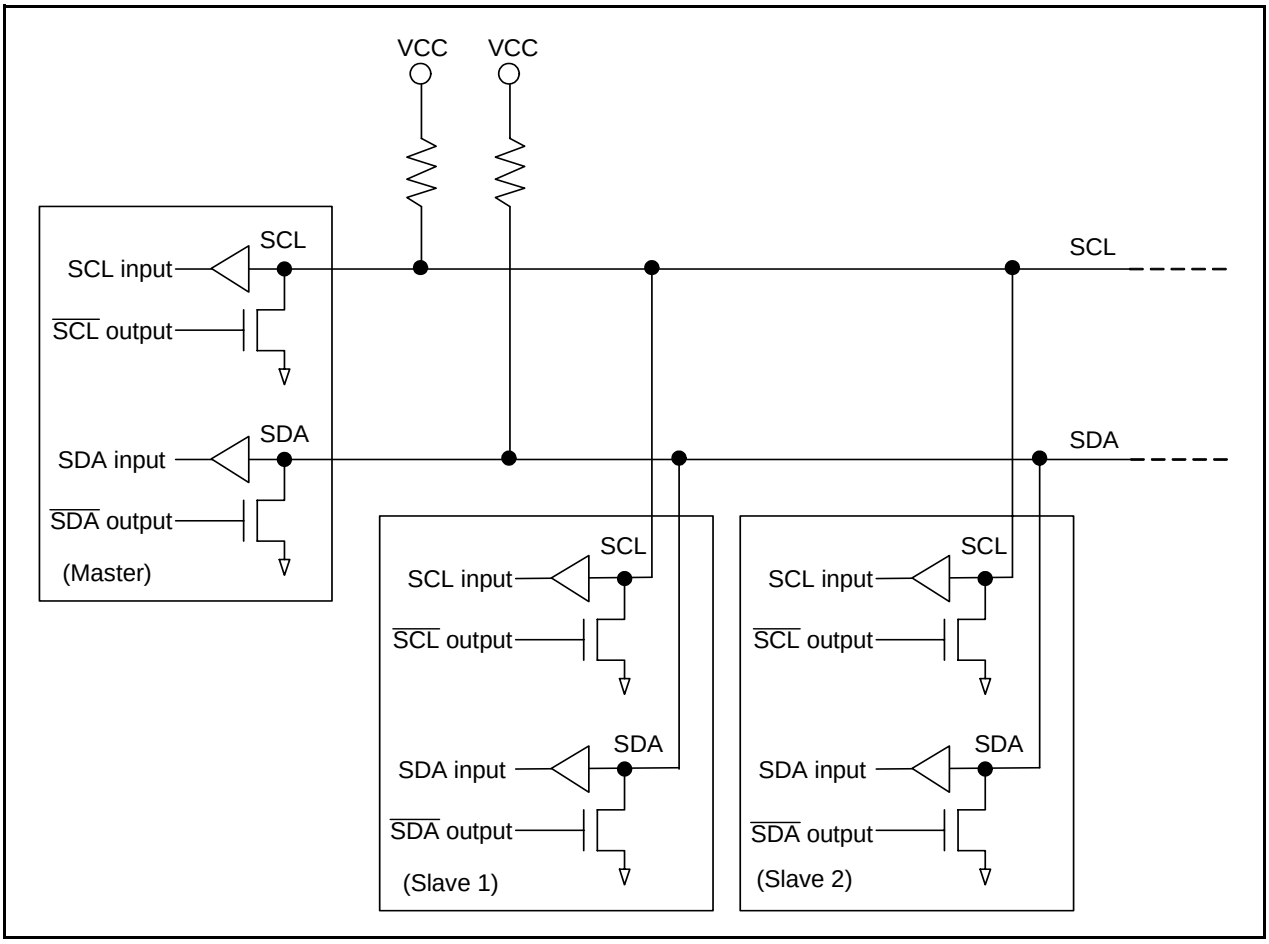


Figure 28.2 External Circuit Connection Example of Pins SCL and SDA

28.2 Registers

28.2.1 Module Standby Control Register (MSTCR)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	MSTTRG	MSTTRC	MSTTRD	MSTIIC	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	MSTIIC	SSU, I2C bus standby bit	0: Active 1: Standby (1)	R/W
b4	MSTTRD	Timer RD standby bit	0: Active 1: Standby (2)	R/W
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (3)	R/W
b6	MSTTRG	Timer RG standby bit	0: Active 1: Standby (4)	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. When the MSTIIC bit is set to 1 (standby), any access to the SSU or the I2C bus associated registers (addresses 0193h to 019Dh) is disabled.
2. When the MSTTRD bit is set to 1 (standby), any access to the timer RD associated registers (addresses 0135h to 015Fh) is disabled.
3. When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0133h) is disabled.
4. When the MSTTRG bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0170h to 017Fh) is disabled.

28.2.2 SSU/IIC Pin Select Register (SSUIICSR)

Address 018Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	IICSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IICSEL	SSU/I2C bus switch bit	0: SSU function selected 1: I2C bus function selected	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

28.2.3 IIC bus Transmit Data Register (ICDRT)

Address 0194h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b7 to b0	This register stores transmit data. When the ICDRS register is detected as empty, the stored transmit data is transferred to the ICDRS register and transmission starts. When the next transmit data is written to the ICDRT register during the data transmission from the ICDRS register, continuous transmission is enabled. When the MLS bit in the ICMR register is set to 1 (data transfer with LSB first), the MSB-LSB inverted data is read after writing to the ICDRT register.	R/W

28.2.4 IIC bus Receive Data Register (ICDRR)

Address 0196h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b7 to b0	This register stores receive data. When the ICDRS register receives 1 byte of data, the receive data is transferred to the ICDRR register and the next receive operation is enabled.	R

28.2.5 IIC bus Control Register 1 (ICCR1)

Address 0198h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ICE	RCVD	MST	TRS	CKS3	CKS2	CKS1	CKS0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CKS0	Transmit clock select bit 3 to 0 (1)	b3 b2 b1 b0 0 0 0 0: f1/28 0 0 0 1: f1/40 0 0 1 0: f1/48 0 0 1 1: f1/64 0 1 0 0: f1/80 0 1 0 1: f1/100 0 1 1 0: f1/112 0 1 1 1: f1/128 1 0 0 0: f1/56 1 0 0 1: f1/80 1 0 1 0: f1/96 1 0 1 1: f1/128 1 1 0 0: f1/160 1 1 0 1: f1/200 1 1 1 0: f1/224 1 1 1 1: f1/256	R/W
b1	CKS1			R/W
b2	CKS2			R/W
b3	CKS3			R/W
b4	TRS	Transmission/reception select bit (2, 3, 6)	b5 b4 0 0: Slave Receive Mode (4) 0 1: Slave Transmit Mode 1 0: Master Receive Mode 1 1: Master Transmit Mode	R/W
b5	MST	Master/slave select bit (5, 6)		R/W
b6	RCVD	Reception disable bit	After reading the ICDRR register while the TRS bit is set to 0, 0: Next receive operation continues 1: Next receive operation disabled	R/W
b7	ICE	I²C bus interface enable bit	0: This module is halted (Pins SCL and SDA are set to the port function) 1: This module is enabled for transfer operations (Pins SCL and SDA are in the bus drive state)	R/W

Notes:
1. Set according to the necessary transfer rate in master mode. Refer to **Table 28.3 Transfer Rate Examples** for the transfer rate. This bit is used for maintaining the setup time in transmit mode of slave mode. The time is 10Tcyc when the CKS3 bit is set to 0 and 20Tcyc when the CKS3 bit is set to 1. (1Tcyc = 1/f1(s))
2. Rewrite the TRS bit between transfer frames.
3. When the first 7 bits after the start condition in slave receive mode match the slave address set in the SAR register and the 8th bit is set to 1, the TRS bit is set to 1.
4. In master mode with the I²C bus format, if arbitration is lost, bits MST and TRS are set to 0 and the IIC enters slave receive mode.
5. When an overrun error occurs in master receive mode with the clock synchronous serial format, the MST bit is set to 0 and the I²C bus enters slave receive mode.
6. In multimaster operation, use the MOV instruction to set bits TRS and MST.

28.2.6 IIC bus Control Register 2 (ICCR2)

Address 0199h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BBSY	SCP	SDAO	SDAOP	SCLO	—	IICRST	—
After Reset	0	1	1	1	1	1	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b1	IICRST	I²C bus control block reset bit	When hang-up occurs due to communication failure during the I²C bus interface operation, writing 1 resets the control block of the I²C bus interface without setting ports or initializing registers.	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b3	SCLO	SCL monitor flag	0: SCL pin is set to low 1: SCL pin is set to high	R
b4	SDAOP	SDAO write protect bit	When rewriting the SDAO bit, write 0 simultaneously (1). When read, the content is 1.	R/W
b5	SDAO	SDA output value control bit	When read 0: SDA pin output is held low 1: SDA pin output is held high When written (1, 2) 0: SDA pin output is changed to low 1: SDA pin output is changed to high-impedance (High-level output via an external pull-up resistor)	R/W
b6	SCP	Start/stop condition generation disable bit	When writing to the to BBSY bit, write 0 simultaneously (3). When read, the content is 1. Writing 1 is invalid.	R/W
b7	BBSY	Bus busy bit (4)	When read: 0: Bus is released (SDA signal changes from low to high while SCL signal is held high) 1: Bus is occupied (SDA signal changes from high to low while SCL signal is held high) When written (3): 0: Stop condition generated 1: Start condition generated	R/W

Notes:
1. When rewriting the SDAO bit, write 0 to the SDAOP bit simultaneously using the MOV instruction.
2. Do not write to the SDAO bit during a transfer operation.
3. Enabled in master mode. When writing to the BBSY bit, write 0 to the SCP bit simultaneously using the MOV instruction. Execute the same way when a start condition is regenerated.
4. Disabled when the clock synchronous serial format is used.

28.2.7 IIC bus Mode Register (ICMR)

Address 019Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	MLS	WAIT	—	—	BCWP	BC2	BC1	BC0
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	BC0	Bit counter 2 to 0	I²C bus format	R/W
b1	BC1		(Read: Number of remaining transfer bits;	R/W
b2	BC2		Write: Number of next transfer data bits). (1, 2) b2 b1 b0 0 0 0: 9 bits (3) 0 0 1: 2 bits 0 1 0: 3 bits 0 1 1: 4 bits 1 0 0: 5 bits 1 0 1: 6 bits 1 1 0: 7 bits 1 1 1: 8 bits Clock synchronous serial format (Read: Number of remaining transfer bits; Write: Always 000b). b2 b1 b0 0 0 0: 8 bits 0 0 1: 1 bit 0 1 0: 2 bits 0 1 1: 3 bits 1 0 0: 4 bits 1 0 1: 5 bits 1 1 0: 6 bits 1 1 1: 7 bits	R/W
b3	BCWP	BC write protect bit	When rewriting bits BC0 to BC2, write 0 simultaneously. (2, 4) When read, the content is 1.	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—	Reserved bit	Set to 0.	R/W
b6	WAIT	Wait insertion bit (5)	0: No wait states (Data and the acknowledge bit are transferred successively) 1: Wait state (After the clock of the last data bit falls, a low-level period is extended for two transfer clocks)	R/W
b7	MLS	MSB first/LSB first select bit	0: Data transfer with MSB first (6) 1: Data transfer with LSB first	R/W

Notes:
1. Rewrite between transfer frames. When writing values other than 000b, write when the SCL signal is low.
2. When writing to bits BC0 to BC2, write 0 to the BCWP bit simultaneously using the MOV instruction.
3. After data including the acknowledge bit is transferred, these bits are automatically set to 000b. When a start condition is detected, these bits are automatically set to 000b.
4. Do not rewrite when the clock synchronous serial format is used.
5. The setting value is valid in master mode with the I²C bus format. It is invalid in slave mode with the I²C bus format or when the clock synchronous serial format is used.
6. Set to 0 when the I²C bus format is used.

28.2.8 IIC bus Interrupt Enable Register (ICIER)

Address 019Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIE	TEIE	RIE	NAKIE	STIE	ACKE	ACKBR	ACKBT
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ACKBT	Transmit acknowledge select bit	0: In receive mode, 0 is transmitted as the acknowledge bit. 1: In receive mode, 1 is transmitted as the acknowledge bit.	R/W
b1	ACKBR	Receive acknowledge bit	0: In transmit mode, the acknowledge bit received from the receive device is set to 0. 1: In transmit mode, the acknowledge bit received from the receive device is set to 1.	R
b2	ACKE	Acknowledge bit detection select bit	0: Content of the receive acknowledge bit is ignored and continuous transfer is performed. 1: When the receive acknowledge bit is set to 1, continuous transfer is halted.	R/W
b3	STIE	Stop condition detection interrupt enable bit	0: Stop condition detection interrupt request disabled 1: Stop condition detection interrupt request enabled (2)	R/W
b4	NAKIE	NACK receive interrupt enable bit	0: NACK receive interrupt request and arbitration lost/ overrun error interrupt request disabled 1: NACK receive interrupt request and arbitration lost/ overrun error interrupt request (1)	R/W
b5	RIE	Receive interrupt enable bit	0: Receive data full and overrun error interrupt request disabled 1: Receive data full and overrun error interrupt request enabled (1)	R/W
b6	TEIE	Transmit end interrupt enable bit	0: Transmit end interrupt request disabled 1: Transmit end interrupt request enabled	R/W
b7	TIE	Transmit interrupt enable bit	0: Transmit data empty interrupt request disabled 1: Transmit data empty interrupt request enabled	R/W

Notes:
1. An overrun error interrupt request is generated when the clock synchronous format is used.
2. Set the STIE bit to 1 (stop condition detection interrupt request enabled) when the STOP bit in the ICSR register is set to 0.

28.2.9 IIC bus Status Register (ICSR)

Address 019Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TDRE	TEND	RDRF	NACKF	STOP	AL	AAS	ADZ
After Reset	0	0	0	0	X	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADZ	General call address recognition flag (1, 2)	This flag is set to 1 when a general call address is detected.	R/W
b1	AAS	Slave address recognition flag (1)	This flag is set to 1 when the first frame immediately after the start condition matches bits SVA0 to SVA6 in the SAR register in slave receive mode (slave address detection and general call address detection).	R/W
b2	AL	Arbitration lost flag/ overrun error flag (1)	I2C bus format: This flag indicates that arbitration has been lost in master mode. This flag is set to 1 (3) when: • The internal SDA signal and SDA pin level do not match at the rising edge of the SCL signal in master transmit mode • The SDA pin is held high at start condition detection in master transmit/receive mode Clock synchronous format: This flag indicates an overrun error. This flag is set to 1 when: • The last bit of the next unit of data is received while the RDRF bit is set to 1	R/W
b3	STOP	Stop condition detection flag (1)	This flag is set to 1 when a stop condition is detected after the frame is transferred.	R/W
b4	NACKF	No acknowledge detection flag (1, 4)	This flag is set to 1 when no ACKnowledge is detected from the receive device after transmission.	R/W
b5	RDRF	Receive data register full flag (1, 5)	This flag is set to 1 when receive data is transferred from registers ICDRS to ICDRR.	R/W
b6	TEND	Transmit end flag (1, 6)	I2C bus format: This flag is set to 1 at the rising edge of the 9th clock cycle of the SCL signal while the TDRE bit is set to 1. Clock synchronous format: This flag is set to 1 when the last bit of the transmit frame is transmitted.	R/W
b7	TDRE	Transmit data empty flag (1, 6)	This flag is set to 1 when: • Data is transferred from registers ICDRT to ICDRS and the CDRT register is empty • The TRS bit in the ICCR1 register is set to 1 (transmit mode) • A start condition is generated (including retransmission) • Slave receive mode is changed to slave transmit mode	R/W

Notes:
1. Each bit is set to 0 by reading 1 before writing 0.
2. This flag is enabled in slave receive mode with the I2C bus format.
3. When two or more master devices attempt to occupy the bus at nearly the same time, if the I2C bus Interface monitors the SDA pin and the data which the I2C bus Interface transmits is different, the AL flag is set to 1 and the bus is occupied by another master.
4. The NACKF bit is enabled when the ACKE bit in the ICIER register is set to 1 (when the receive acknowledge bit is set to 1, transfer is halted).
5. The RDRF bit is set to 0 when data is read from the ICDRR register.
6. Bits TEND and TDRE are set to 0 when data is written to the ICDRT register.

When accessing the ICSR register successively, insert one or more NOP instructions between the instructions used for access.

28.2.10 Slave Address Register (SAR)

Address 019Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SVA6	SVA5	SVA4	SVA3	SVA2	SVA1	SVA0	FS
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FS	Format select bit	0: I²C bus format 1: Clock synchronous serial format	R/W
b1	SVA0	Slave address 6 to 0	Set an address different from that of the other slave devices connected to the I²C bus. When the 7 high-order bits of the first frame transmitted after the start condition match bits SVA0 to SVA6 in slave mode of the I²C bus format, the MCU operates as a slave device.	R/W
b2	SVA1			R/W
b3	SVA2			R/W
b4	SVA3			R/W
b5	SVA4			R/W
b6	SVA5			R/W
b7	SVA6			R/W

28.2.11 IIC bus Shift Register (ICDRS)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—

Bit	Function	R/W
b7 to b0	This register transmits and receives data. During transmission, data is transferred from registers ICRDT to ICDRS and transmitted from the SDA pin. During reception, data is transferred from registers ICDRS to the ICDRR after 1 byte of data is received.	—

28.3 Common Items for Multiple Modes

28.3.1 Transfer Clock

When the MST bit in the ICCR1 register is set to 0, the transfer clock is the external clock input from the SCL pin.
When the MST bit in the ICCR1 register is set to 1, the transfer clock is the internal clock selected by bits CKS0 to CKS3 in the ICCR1 register and the transfer clock is output from the SCL pin.
Table 28.3 lists Transfer Rate Examples.

Table 28.3 Transfer Rate Examples

ICCR1 Register				Transfer Clock	Transfer Rate				
CKS3	CKS2	CKS1	CKS0		f1 = 5 MHz	f1 = 8 MHz	f1 = 10 MHz	f1 = 16 MHz	f1 = 20 MHz
0	0	0	0	f1/28	179 kHz	286 kHz	357 kHz	571 kHz	714 kHz
			1	f1/40	125 kHz	200 kHz	250 kHz	400 kHz	500 kHz
		1	0	f1/48	104 kHz	167 kHz	208 kHz	333 kHz	417 kHz
			1	f1/64	78.1 kHz	125 kHz	156 kHz	250 kHz	313 kHz
	1	0	0	f1/80	62.5 kHz	100 kHz	125 kHz	200 kHz	250 kHz
			1	f1/100	50.0 kHz	80.0 kHz	100 kHz	160 kHz	200 kHz
		1	0	f1/112	44.6 kHz	71.4 kHz	89.3 kHz	143 kHz	179 kHz
			1	f1/128	39.1 kHz	62.5 kHz	78.1 kHz	125 kHz	156 kHz
1	0	0	0	f1/56	89.3 kHz	143 kHz	179 kHz	286 kHz	357 kHz
			1	f1/80	62.5 kHz	100 kHz	125 kHz	200 kHz	250 kHz
		1	0	f1/96	52.1 kHz	83.3 kHz	104 kHz	167 kHz	208 kHz
			1	f1/128	39.1 kHz	62.5 kHz	78.1 kHz	125 kHz	156 kHz
	1	0	0	f1/160	31.3 kHz	50.0 kHz	62.5 kHz	100 kHz	125 kHz
			1	f1/200	25.0 kHz	40.0 kHz	50.0 kHz	80.0 kHz	100 kHz
		1	0	f1/224	22.3 kHz	35.7 kHz	44.6 kHz	71.4 kHz	89.3 kHz
			1	f1/256	19.5 kHz	31.3 kHz	39.1 kHz	62.5 kHz	78.1 kHz

28.3.2 Interrupt Requests

The I²C bus interface has six interrupt requests when the I²C bus format is used and four interrupt requests when the clock synchronous serial format is used.

Table 28.4 lists the Interrupt Requests of I²C bus Interface.

Because these interrupt requests are allocated at the I²C bus interface interrupt vector table, the source must be determined bit by bit.

Table 28.4 Interrupt Requests of I²C bus Interface

Interrupt Request		Generation Condition	Format	
			I²C bus	Clock Synchronous Serial
Transmit data empty	TXI	TIE = 1 and TDRE = 1	Enabled	Enabled
Transmit end	TEI	TEIE = 1 and TEND = 1	Enabled	Enabled
Receive data full	RXI	RIE = 1 and RDRF = 1	Enabled	Enabled
Stop condition detection	STPI	STIE = 1 and STOP = 1	Enabled	Disabled
NACK detection	NAKI	NAKIE = 1 and AL = 1	Enabled	Disabled
Arbitration lost/overrun error		(or NAKIE = 1 and NACKF = 1)	Enabled	Enabled

STIE, NAKIE, RIE, TEIE, TIE: Bits in ICIER register
AL, STOP, NACKF, RDRF, TEND, TDRE: Bits in ICSR register

When generation conditions listed in Table 28.4 are met, an interrupt request of the I²C bus interface is generated. Set the interrupt generation conditions to 0 by the I²C bus interface interrupt routine.

However, bits TDRE and TEND are automatically set to 0 by writing transmit data to the ICDRT register and the RDRF bit is automatically set to 0 by reading the ICDRR register. In particular, the TDRE bit is set to 0 when transmit data is written to the ICDRT register and set to 1 when data is transferred from the ICDRT register to the ICDRS register. If the TDRE bit is further set to 0, additional 1 byte may be transmitted.
Also, set the STIE bit to 1 (stop condition detection interrupt request enabled) when the STOP bit is set to 0.

28.4 I²C bus Interface Mode

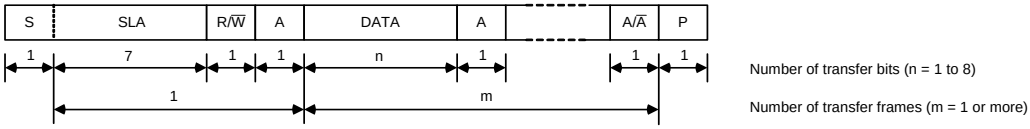
28.4.1 I²C bus Format

When the FS bit in the SAR register is set to 0, the I²C bus format is used for communication.

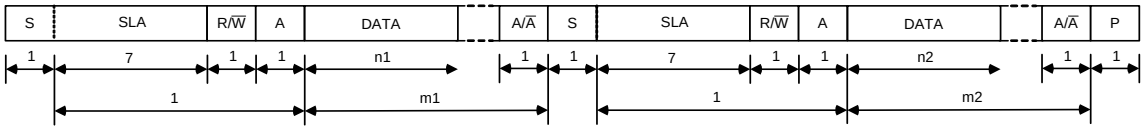
Figure 28.3 shows the I²C bus Format and Bus Timing. The first frame following the start condition consists of 8 bits.

(1) I²C bus format

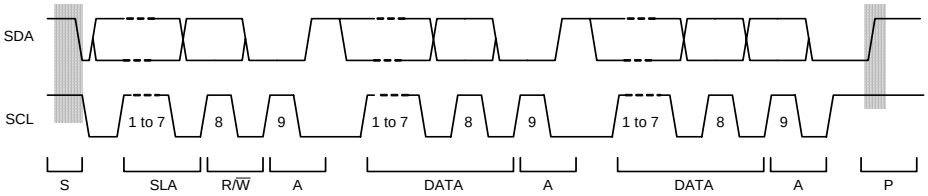
(a) I²C bus format (FS = 0)



(b) I²C bus format When Start Condition is Retransmitted (FS = 0)



(2) I²C bus timing



Legend:
S : Start condition
The master device changes the SDA signal from high to low while the SCL signal is held high.
SLA : Slave address
R/W : Indicates the direction of data transmission/reception
Data is transmitted when:
R/W value is 1: From the slave device to the master device
R/W value is 0: From the master device to the slave device
A : Acknowledge
The receive device sets the SDA signal to low.
DATA : Transmit/receive data
P : Stop condition
The master device changes the SDA signal from low to high while the SCL signal is held high.

Figure 28.3 I²C bus Format and Bus Timing

28.4.2 Master Transmit Operation

In master transmit mode, the master device outputs the transmit clock and data, and the slave device returns an acknowledge signal.

Figures 28.4 and 28.5 show the Operating Timing in Master Transmit Mode (I²C bus Interface Mode).

The transmit procedure and operation in master transmit mode are as follows:

(1) Set the STOP bit in the ICSR register to 0 for initialization, and set the ICE bit in the ICCR1 register to 1 (transfer operation enabled). Then, set bits WAIT and MLS in the ICMR register and bits CKS0 to CKS3 in the ICCR1 register (initial setting).

(2) After confirming that the bus is released by reading the BBSY bit in the ICCR2 register, set bits TRS and MST in the ICCR1 register to master transmit mode. Then, write 1 to the BBSY bit and 0 to the SCP bit with the MOV instruction (start condition generated). This will generate a start condition.

(3) After confirming that the TDRE bit in the ICSR register is set to 1 (data is transferred from registers ICDRT to ICDRS), write transmit data to the ICDRT register (data in which a slave address and R/$\overline{W}$ are indicated in the 1st byte). At this time, the TDRE bit is automatically set to 0. When data is transferred from registers ICDRT to ICDRS, the TDRE bit is set to 1 again.

(4) When 1 byte of data transmission is completed while the TDRE bit is set to 1, the TEND bit in the ICSR register is set to 1 at the rising edge of the 9th clock cycle of the transmit clock. After confirming that the slave device is selected by reading the ACKBR bit in the ICIER register, write the 2nd byte of data to the ICDRT register. Since the slave device is not acknowledged when the ACKBR bit is set to 1, generate a stop condition. Stop condition generation is enabled by writing 0 to the BBSY bit and 0 to the SCP bit with the MOV instruction. The SCL signal is fixed low until data is ready or a stop condition is generated.

(5) Write the transmit data after the 2nd byte to the ICDRT register every time the TDRE bit is set to 1.

(6) When the number of bytes to be transmitted is written to the ICDRT register, wait until the TEND bit is set to 1 while the TDRE bit is set to 1. Or wait for NACK (NACKF bit in ICSR register = 1) from the receive device while the ACKE bit in the ICIER register is set to 1 (when the receive acknowledge bit is set to 1, transfer is halted). Then, generate a stop condition before setting the TEND bit or the NACKF bit to 0.

(7) When the STOP bit in the ICSR register is set to 1, return to slave receive mode.

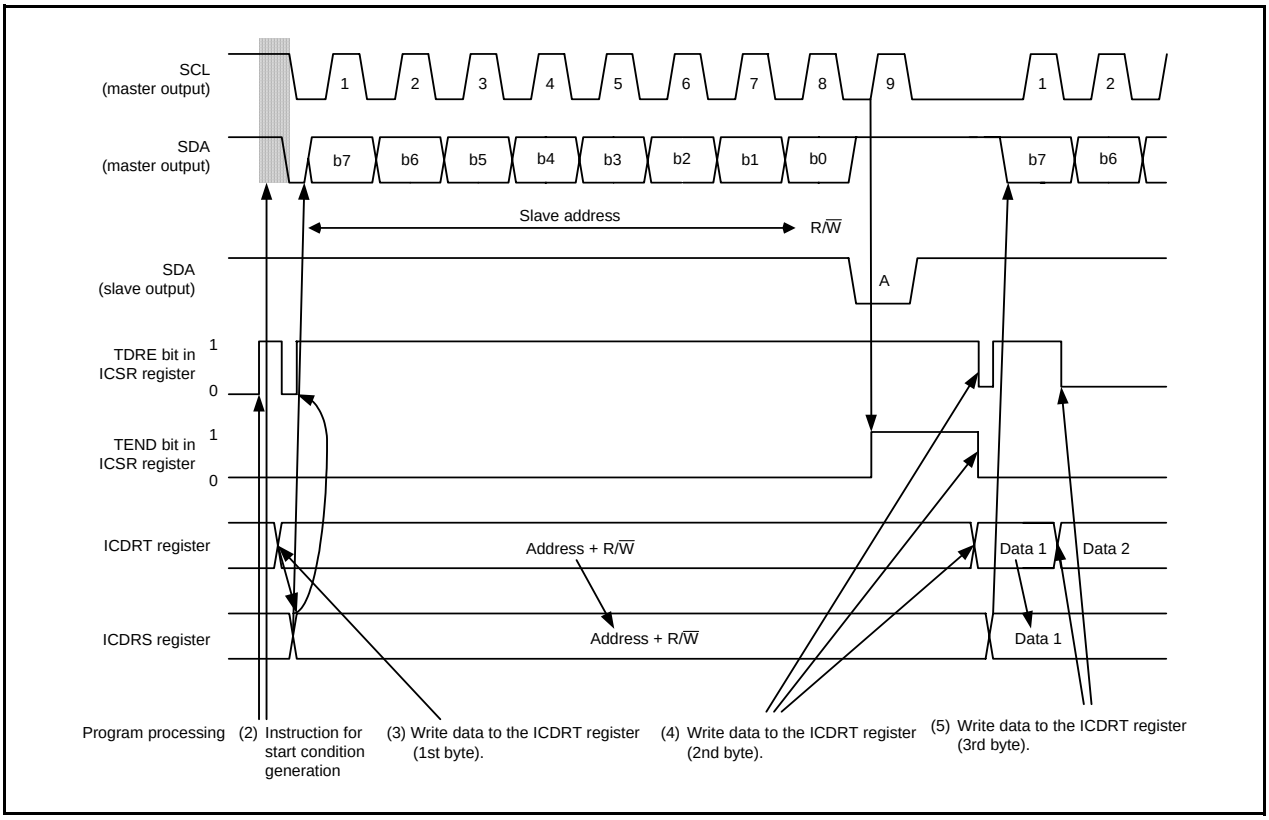


Figure 28.4 Operating Timing in Master Transmit Mode (I²C bus Interface Mode) (1)

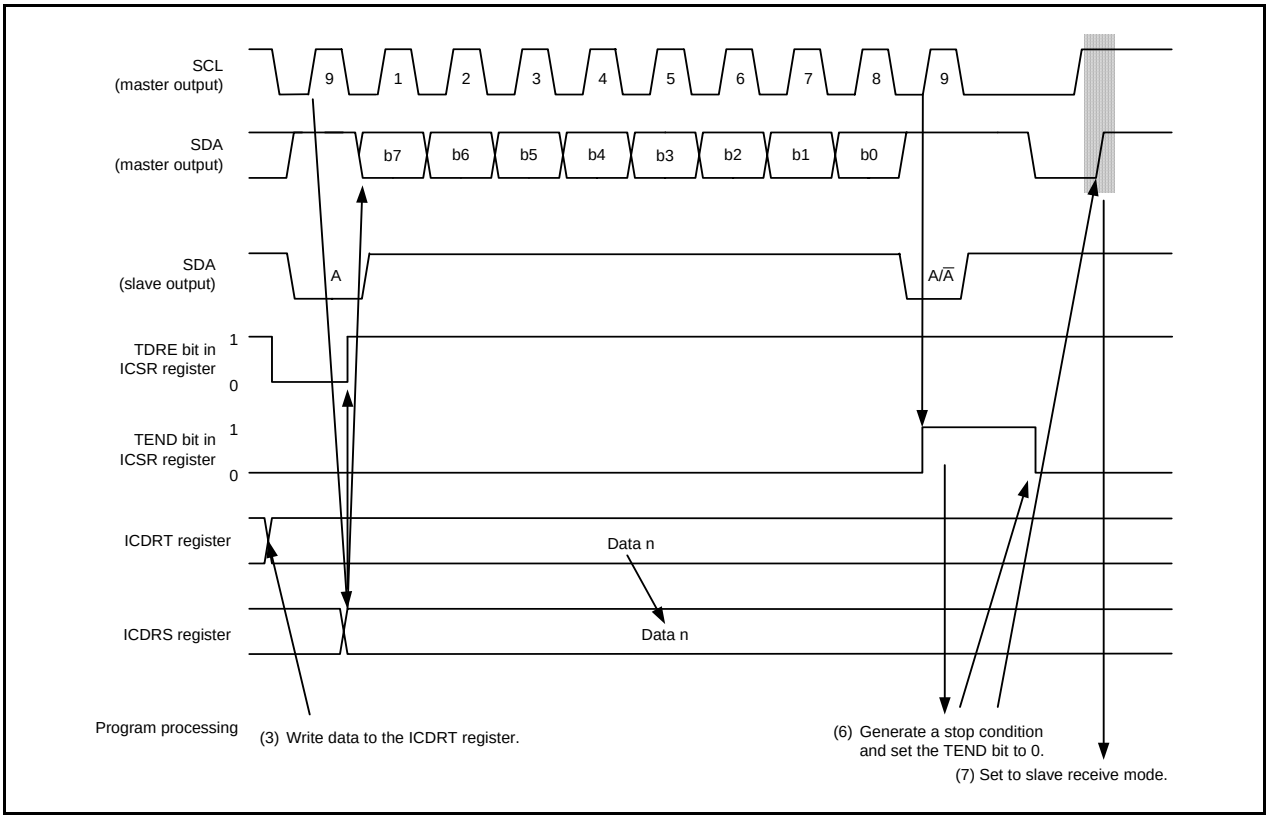


Figure 28.5 Operating Timing in Master Transmit Mode (I²C bus Interface Mode) (2)

28.4.3 Master Receive Operation

In master receive mode, the master device outputs the receive clock, receives data from the slave device, and returns an acknowledge signal.

Figures 28.6 and 28.7 show the Operating Timing in Master Receive Mode (I2C bus Interface Mode).

The receive procedure and operation in master receive mode are as follows:

(1) After setting the TEND bit in the ICSR register to 0, set the TRS bit in the ICCR1 register to 0 to switch from master transmit mode to master receive mode. Then set the TDRE bit in the ICSR register to 0.
(2) Dummy reading the ICDRR register starts receive operation. The receive clock is output in synchronization with the internal clock and data is received. The master device outputs the level set by the ACKBT bit in the ICIER register to the SDA pin at the rising edge of the 9th clock cycle of the receive clock.
(3) When one frame of data reception is completed, the RDRF bit in the ICSR register is set to 1 at the rising edge of the 9th clock cycle of the receive clock. If the ICDRR register is read at this time, the received data can be read and the RDRF bit is set to 0 simultaneously.
(4) Continuous receive operation is enabled by reading the ICDRR register every time the RDRF bit is set to 1. If reading the ICDRR register is delayed by another process and the 8th clock cycle falls while the RDRF bit is set to 1, the SCL signal is fixed low until the ICDRR register is read.
(5) If the next frame is the last receive frame and the RCVD bit in the ICCR1 register is set to 1 (next receive operation disabled) before reading the ICDRR register, stop condition generation is enabled after the next receive operation.
(6) When the RDRF bit is set to 1 at the rising edge of the 9th clock cycle of the receive clock, generate a stop condition.
(7) When the STOP bit in the ICSR register is set to 1, read the ICDRR register and set the RCVD bit to 0 (next receive operation continues).
(8) Return to slave receive mode.

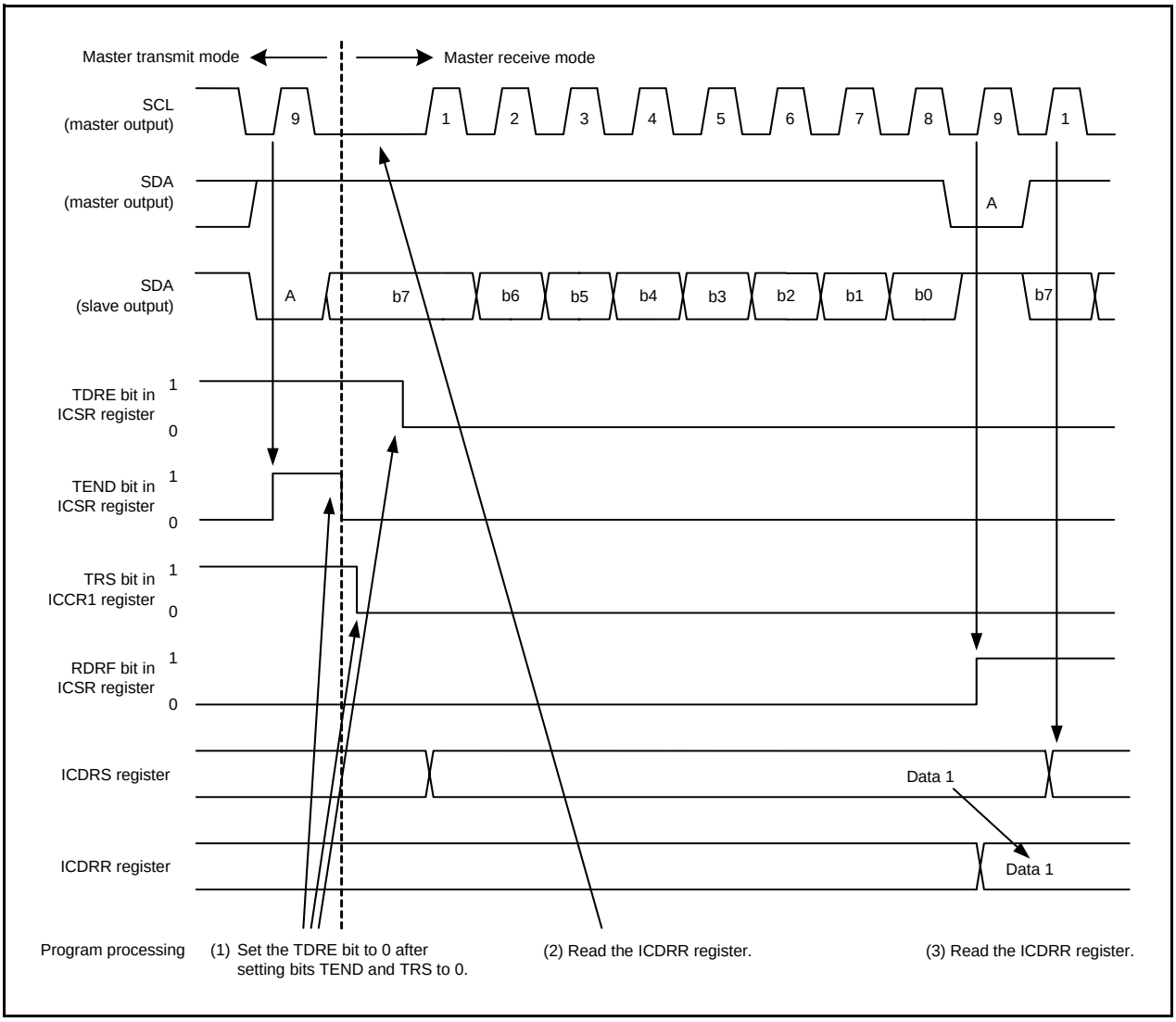


Figure 28.6 Operating Timing in Master Receive Mode (I²C bus Interface Mode) (1)

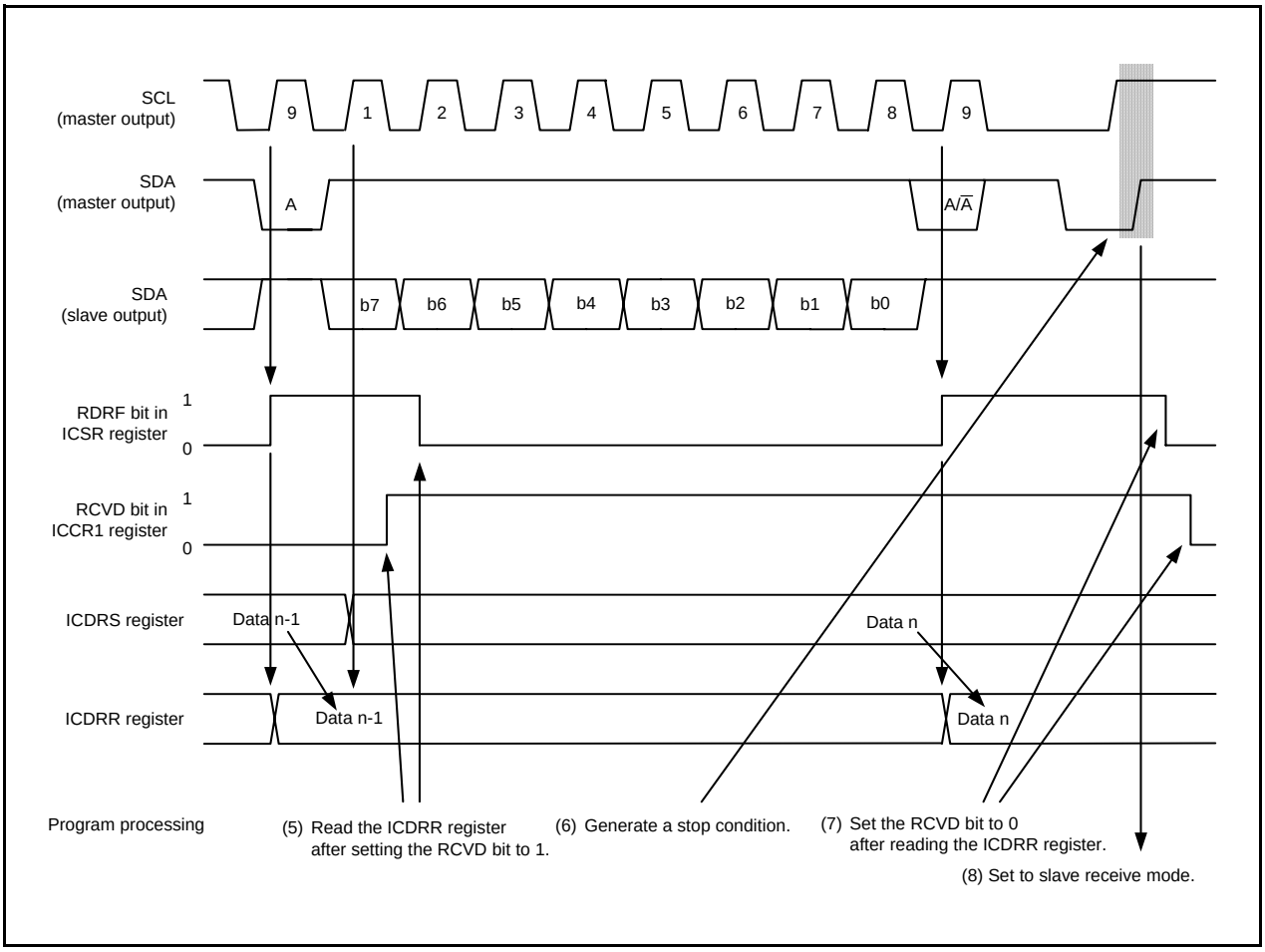


Figure 28.7 Operating Timing in Master Receive Mode (I²C bus Interface Mode) (2)

28.4.4 Slave Transmit Operation

In slave transmit mode, the slave device outputs the transmit data while the master device outputs the receive clock and returns an acknowledge signal.

Figures 28.8 and 28.9 show the Operating Timing in Slave Transmit Mode (I2C bus Interface Mode).

The transmit procedure and operation in slave transmit mode are as follows.

(1) Set the ICE bit in the ICCR1 register to 1 (transfer operation enabled), and set bits WAIT and MLS in the ICMR register and bits CKS0 to CKS3 in the ICCR1 register (initial setting). Then, set bits TRS and MST in the ICCR1 register to 0 and wait until the slave address matches in slave receive mode.

(2) When the slave address matches at the first frame after detecting the start condition, the slave device outputs the level set by the ACKBT bit in the ICIER register to the SDA pin at the rising edge of the 9th clock cycle. If the 8th bit of data (R/$\overline{W}$) is 1 at this time, bits TRS and TDRE in the ICSR register are set to 1, and the mode is switched to slave transmit mode automatically. Continuous transmission is enabled by writing transmit data to the ICDRT register every time the TDRE bit is set to 1.

(3) When the TDRE bit in the ICDRT register is set to 1 after the last transmit data is written to the ICDRT register, wait until the TEND bit in the ICSR register is set to 1 while the TDRE bit is set to 1. When the TEND bit is set to 1, set the TEND bit to 0.

(4) Set the TRS bit to 0 and dummy read the ICDRR register to end the process. This will release the SCL signal.

(5) Set the TDRE bit to 0.

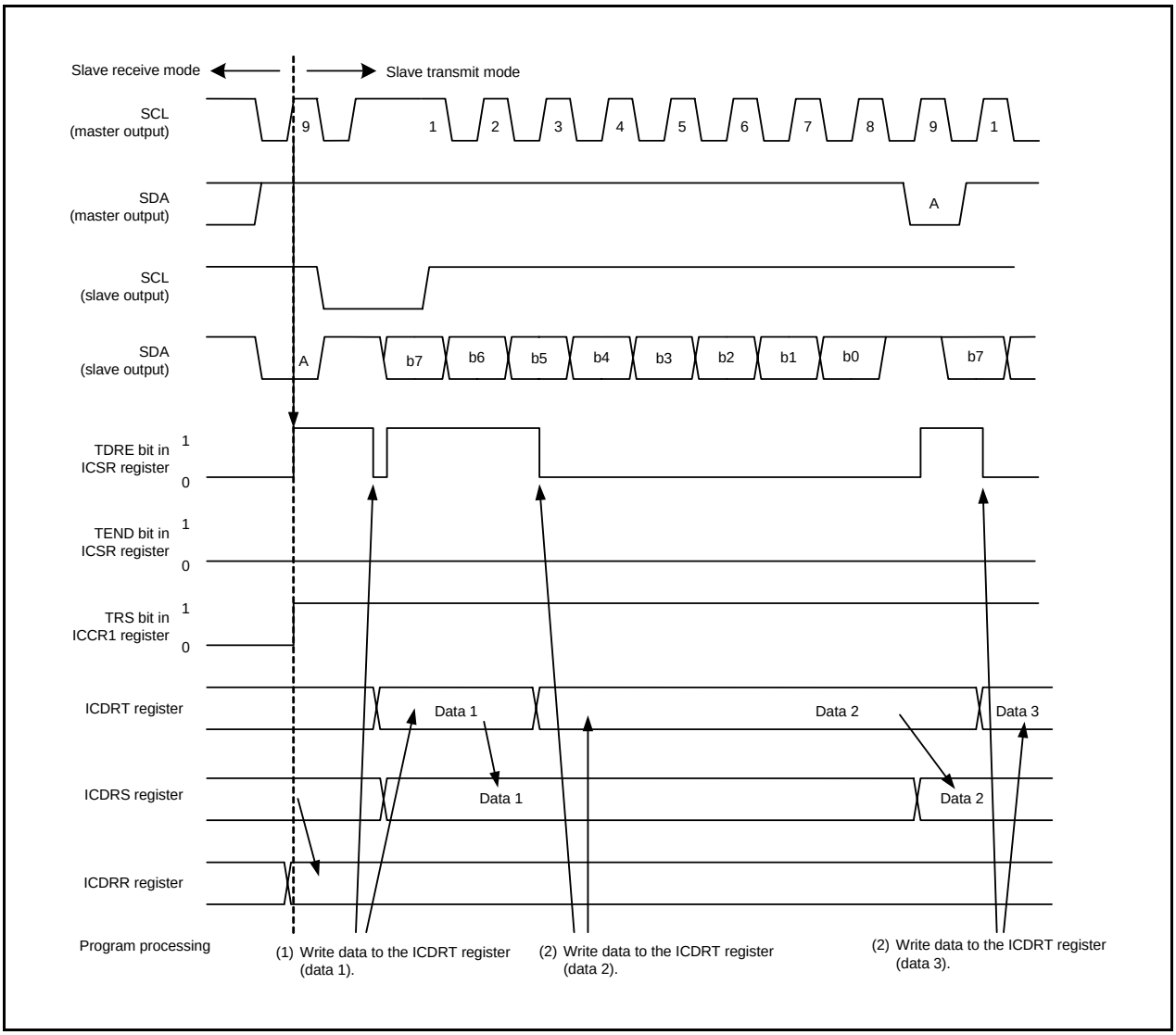


Figure 28.8 Operating Timing in Slave Transmit Mode (I²C bus Interface Mode) (1)

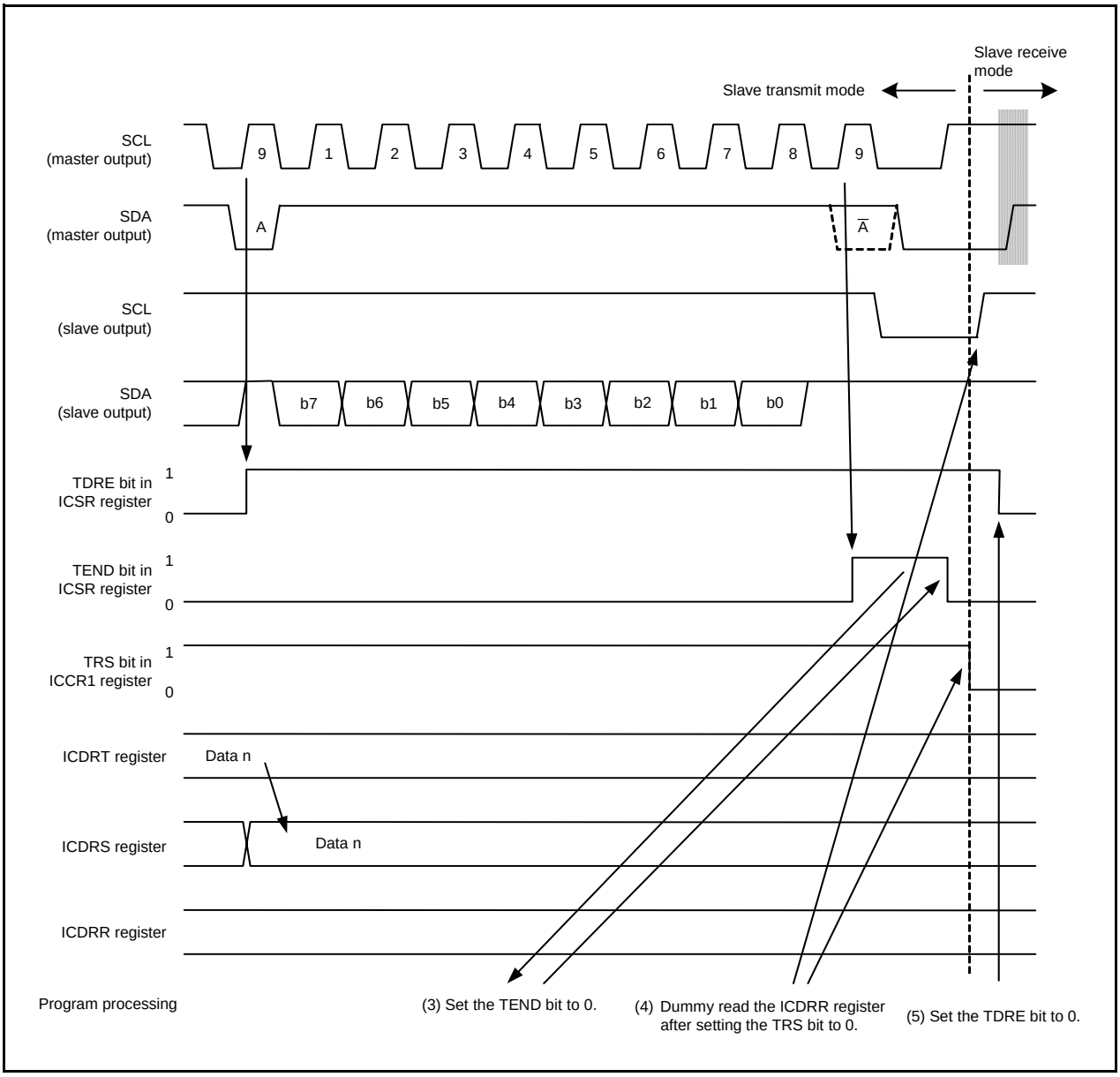


Figure 28.9 Operating Timing in Slave Transmit Mode (I²C bus Interface Mode) (2)

28.4.5 Slave Receive Operation

In slave receive mode, the master device outputs the transmit clock and data, and the slave device returns an acknowledge signal.

Figures 28.10 and 28.11 show the Operating Timing in Slave Receive Mode (I²C bus Interface Mode).

The receive procedure and operation in slave receive mode are as follows:

(1) Set the ICE bit in the ICCR1 register to 1 (transfer operation enabled), and set bits WAIT and MLS in the ICMR register and bits CKS0 to CKS3 in the ICCR1 register (initial setting). Then, set bits TRS and MST in the ICCR1 register to 0 and wait until the slave address matches in slave receive mode.

(2) When the slave address matches at the first frame after detecting the start condition, the slave device outputs the level set by the ACKBT bit in the ICIER register to the SDA pin at the rising edge of the 9th clock cycle. Since the RDRF bit in the ICSR register is set to 1 simultaneously, dummy read the ICDRR register (the read data is unnecessary because it indicates the slave address and R/$\overline{W}$).

(3) Read the ICDRR register every time the RDRF bit is set to 1. If the 8th clock cycle falls while the RDRF bit is set to 1, the SCL signal is fixed low until the ICDRR register is read. The setting change of the acknowledge signal returned to the master device before reading the ICDRR register takes affect from the following transfer frame.

(4) Reading the last byte is also performed by reading the ICDRR register.

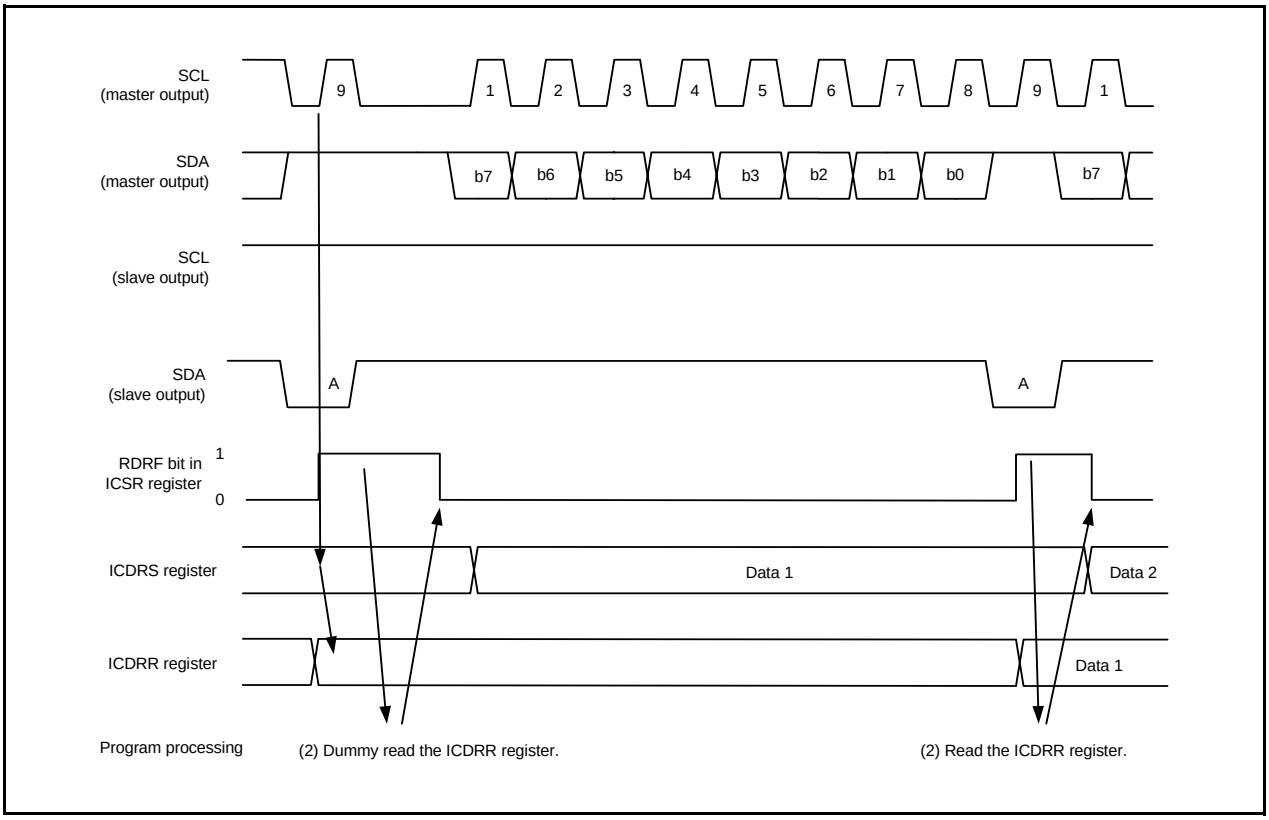


Figure 28.10 Operating Timing in Slave Receive Mode (I²C bus Interface Mode) (1)

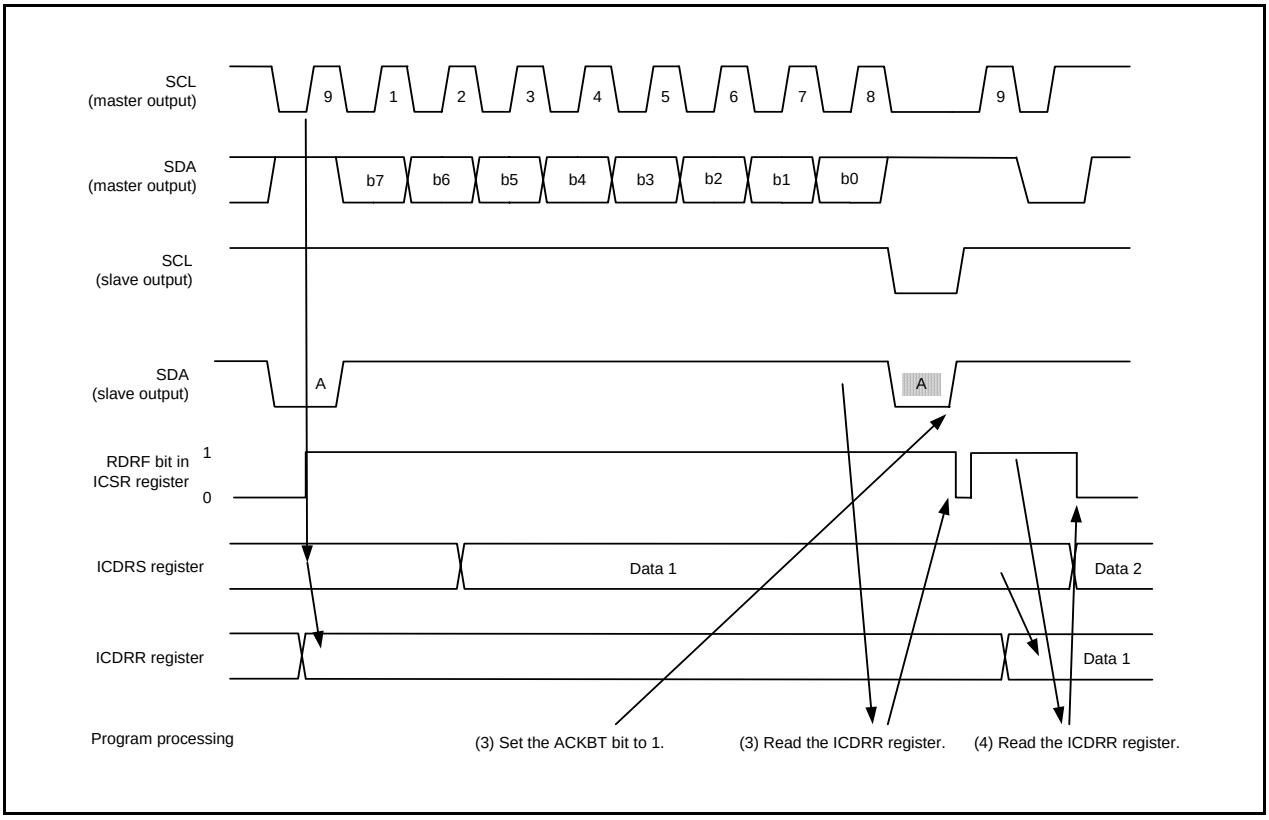


Figure 28.11 Operating Timing in Slave Receive Mode (I²C bus Interface Mode) (2)

28.5 Clock Synchronous Serial Mode

28.5.1 Clock Synchronous Serial Format

When the FS bit in the SAR register is set to 1, the clock synchronous serial format is used for communication. Figure 28.12 shows the Transfer Format of Clock Synchronous Serial Format.

When the MST bit in the ICCR1 register is set to 1, the transfer clock is output from the SCL pin. When the MST bit is set to 0, the external clock is input.

The transfer data is output between successive falling edges of the SCL clock, and data is determined at the rising edge of the SCL clock. MSB first or LSB first can be selected as the order of the data transfer by setting the MLS bit in the ICMR register. The SDA output level can be changed by the SDAO bit in the ICCR2 register during transfer standby.

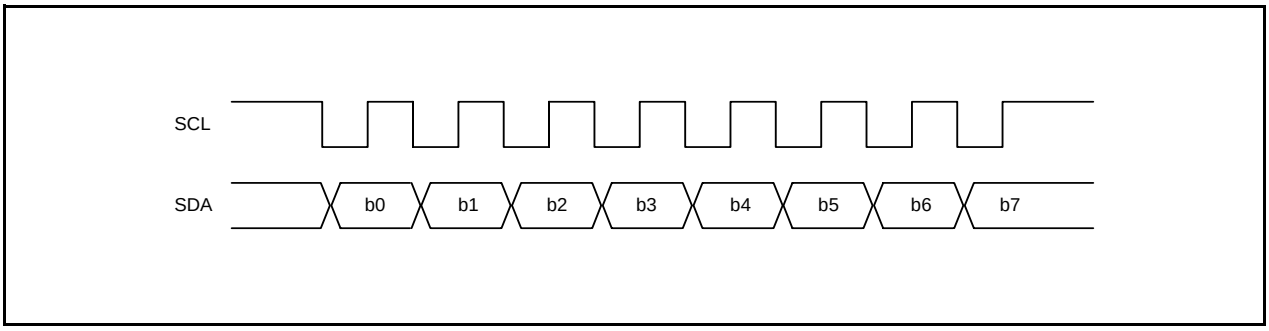


Figure 28.12 Transfer Format of Clock Synchronous Serial Format

28.5.2 Transmit Operation

In transmit mode, transmit data is output from the SDA pin in synchronization with the falling edge of the transfer clock. The transfer clock is output when the MST bit in the ICCR1 register is set to 1 and input when the MST bit is set to 0.
Figure 28.13 shows the Operating Timing in Transmit Mode (Clock Synchronous Serial Mode).

The transmit procedure and operation in transmit mode are as follows:

(1) Set the ICE bit in the ICCR1 register to 1 (transfer operation enabled). Then set bits CKS0 to CKS3 in the ICCR1 register and the MST bit (initial setting).
(2) Set the TRS bit in the ICCR1 register to 1 to select transmit mode. This will set the TDRE bit in the ICSR register is to 1.
(3) After confirming that the TDRE bit is set to 1, write transmit data to the ICDRT register. Data is transferred from registers ICDRT to ICDRS and the TDRE bit is automatically set to 1. Continuous transmission is enabled by writing data to the ICDRT register every time the TDRE bit is set to 1. To switch from transmit to receive mode, set the TRS bit to 0 while the TDRE bit is set to 1.

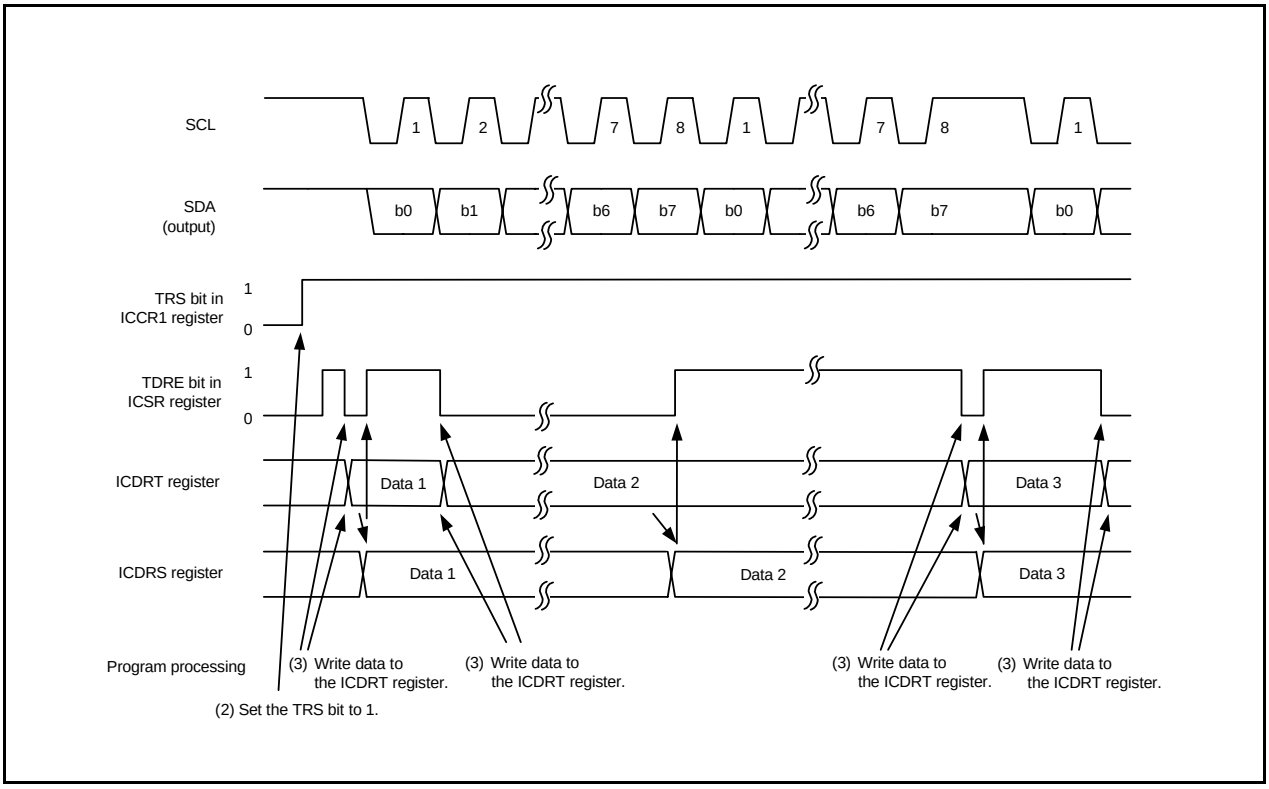


Figure 28.13 Operating Timing in Transmit Mode (Clock Synchronous Serial Mode)

28.5.3 Receive Operation

In receive mode, data is latched at the rising edge of the transfer clock. The transfer clock is output when the MST bit in the ICCR1 register is set to 1 and input when the MST bit is set to 0.
Figure 28.14 shows the Operating Timing in Receive Mode (Clock Synchronous Serial Mode).

The receive procedure and operation in receive mode are as follows:

(1) Set the ICE bit in the ICCR1 register to 1 (transfer operation enabled). Then set bits CKS0 to CKS3 in the ICCR1 register and the MST bit (initial setting).
(2) Set the MST bit to 1 while the transfer clock is being output. This will start the output of the receive clock.
(3) When the receive operation is completed, data is transferred from registers ICDRS to ICDRR and the RDRF bit in the ICSR register is set to 1. When the MST bit is set to 1, the clock is output continuously since the next byte of data is enabled for reception. Continuous receive operation is enabled by reading the ICDRR register every time the RDRF bit is set to 1. If the 8th clock cycle falls while the RDRF bit is set to 1, an overrun is detected and the AL bit in the ICSR register is set to 1. At this time, the last receive data is retained in the ICDRR register.
(4) When the MST bit is set to 1, set the RCVD bit in the ICCR1 register to 1 (next receive operation disabled) and read the ICDRR register. The SCL signal is fixed high after the following byte of data reception is completed.

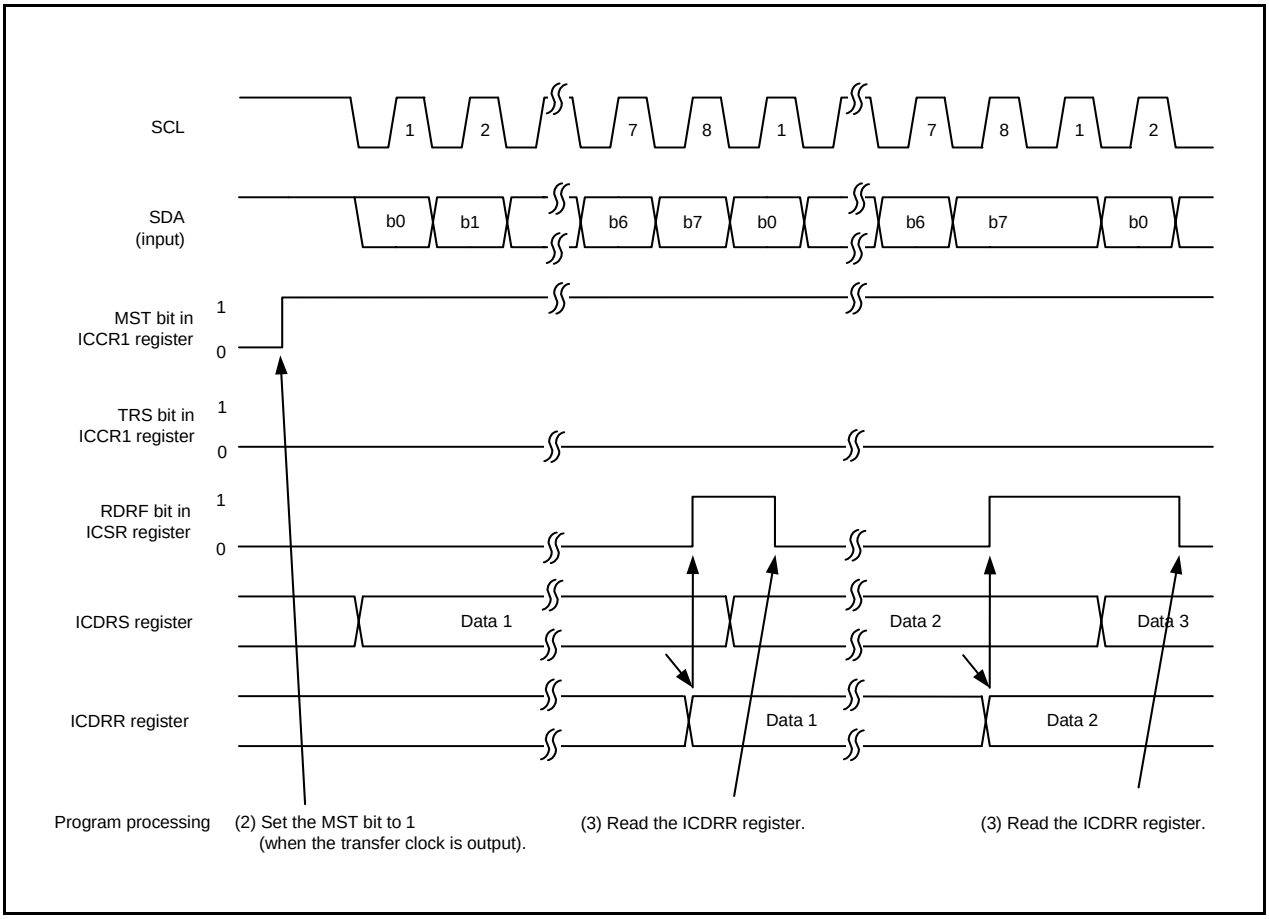


Figure 28.14 Operating Timing in Receive Mode (Clock Synchronous Serial Mode)

28.6 Register Setting Examples

Figures 28.15 to 28.18 show Register Setting Examples When Using I²C bus interface.

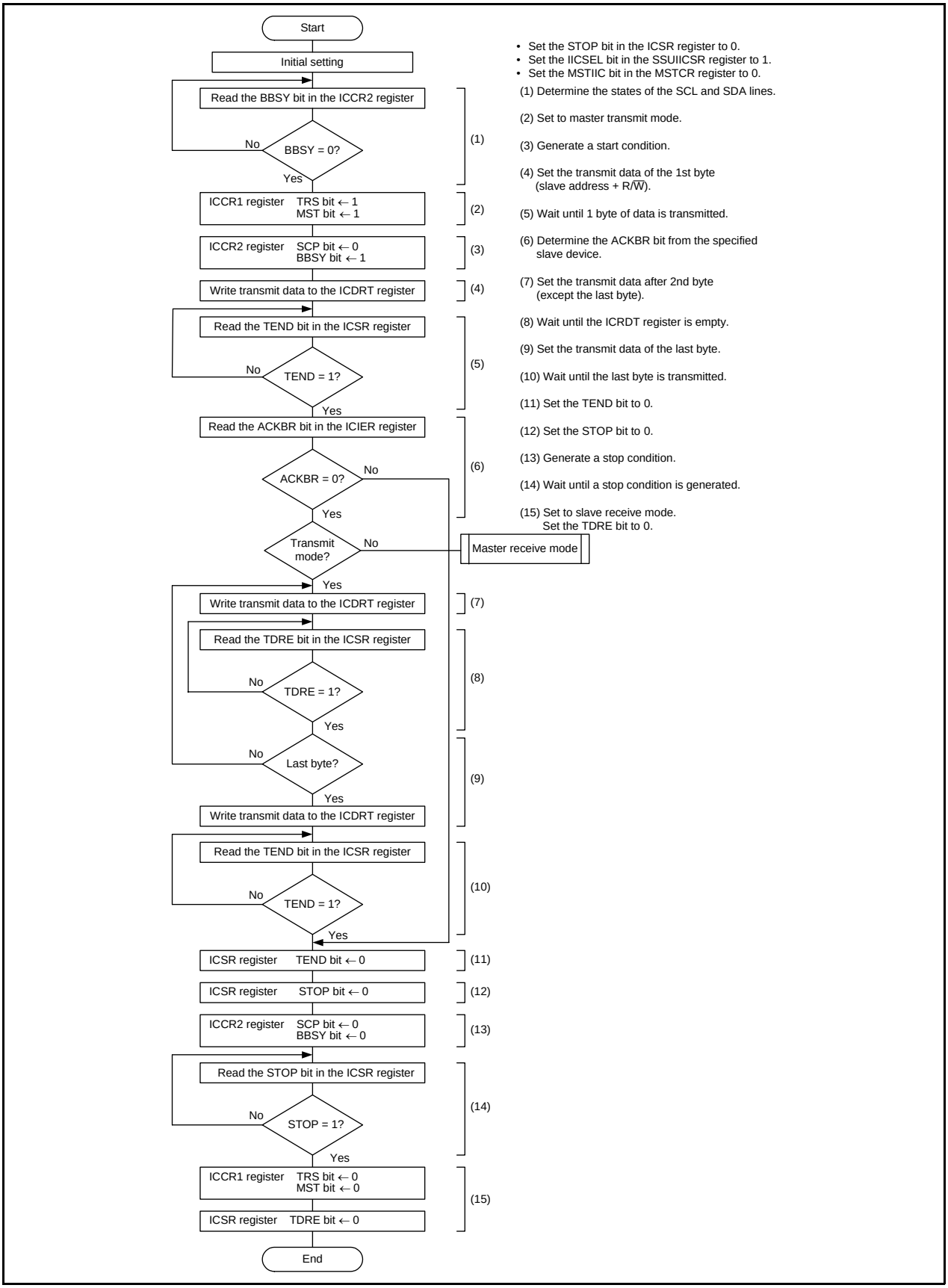
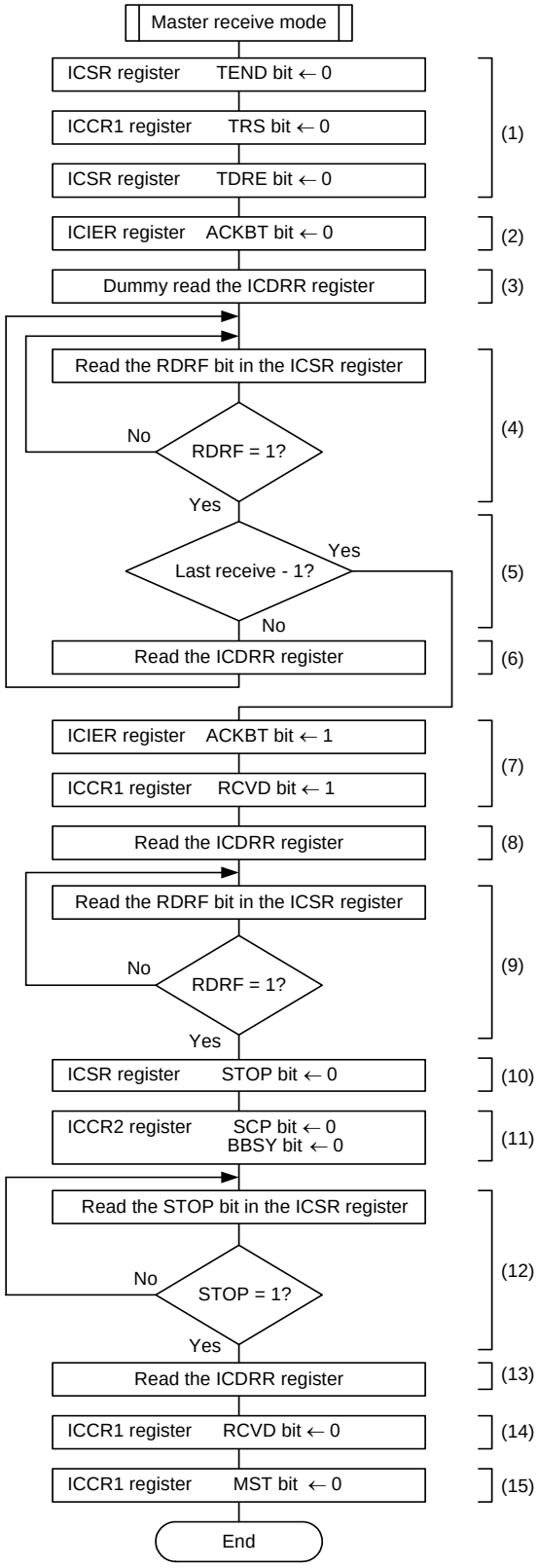


Figure 28.15 Register Setting Example in Master Transmit Mode (I²C bus Interface Mode)



(1) Set the TEND bit to 0 and set to master receive mode. Set the TDRE bit to 0. (1,2)

(2) Set the ACKBT bit to the transmit device. (1)

(3) Dummy read the ICDRR register. (1)

(4) Wait until 1 byte is received.

(5) Determine (last receive - 1).

(6) Read the receive data.

(7) Set the ACKBT bit of the last byte and set continuous receive operation to disable (RCVD = 1). (2)

(8) Read the receive data of (last byte - 1).

(9) Wait until the last byte is received.

(10) Set the STOP bit to 0.

(11) Generate a stop condition.

(12) Wait until a stop condition is generated.

(13) Read the receive data of the last byte.

(14) Set the RCVD bit to 0.

(15) Set to slave receive mode.

Notes:
1. Do not generate interrupts while processing steps (1) to (3).
2. For 1 byte of data reception, skip steps (2) to (6) after step (1) and jump to process step (7). Process step (8) is a dummy read from the ICDRR register.

Figure 28.16 Register Setting Example in Master Receive Mode (I²C bus Interface Mode)

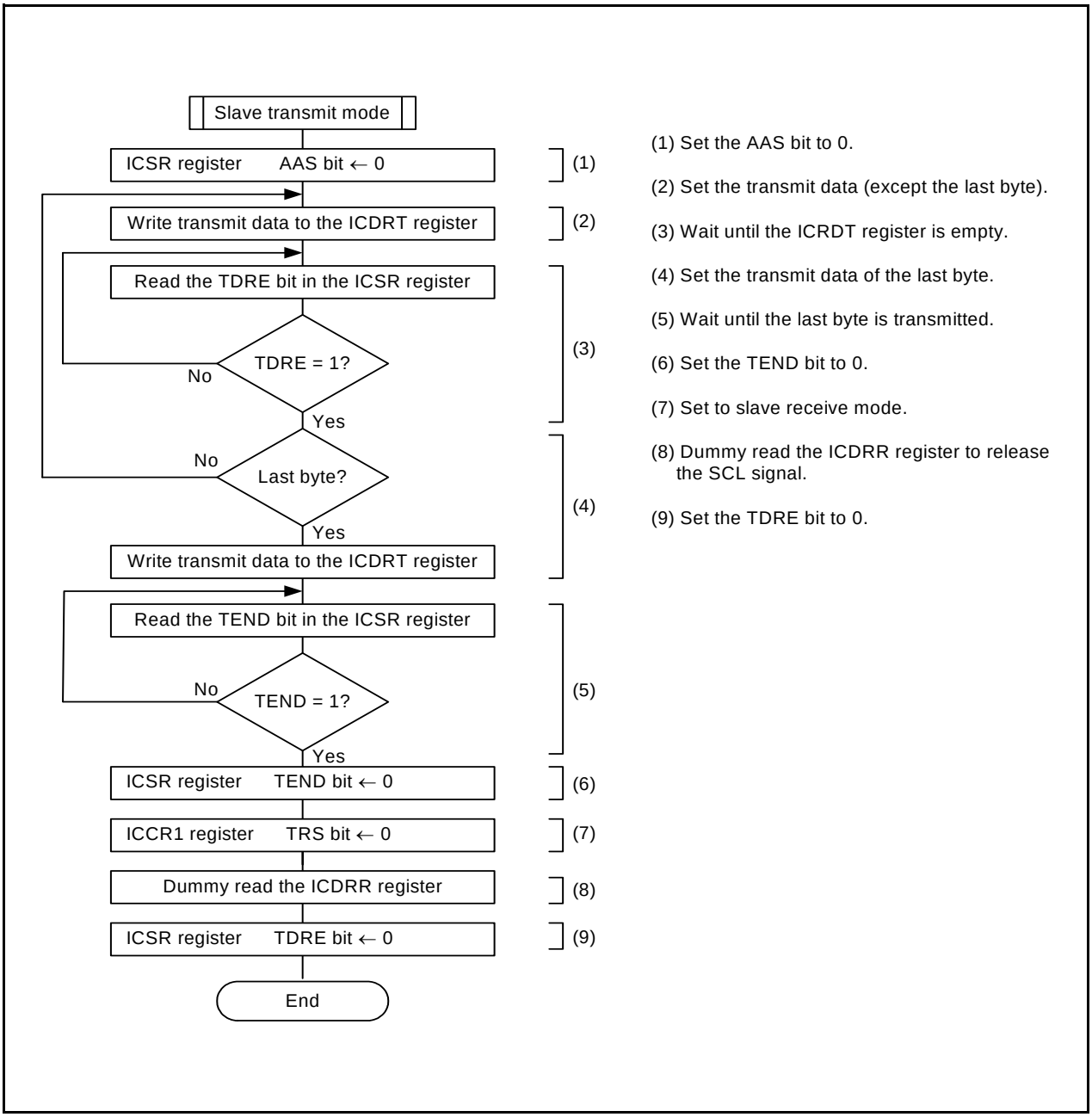
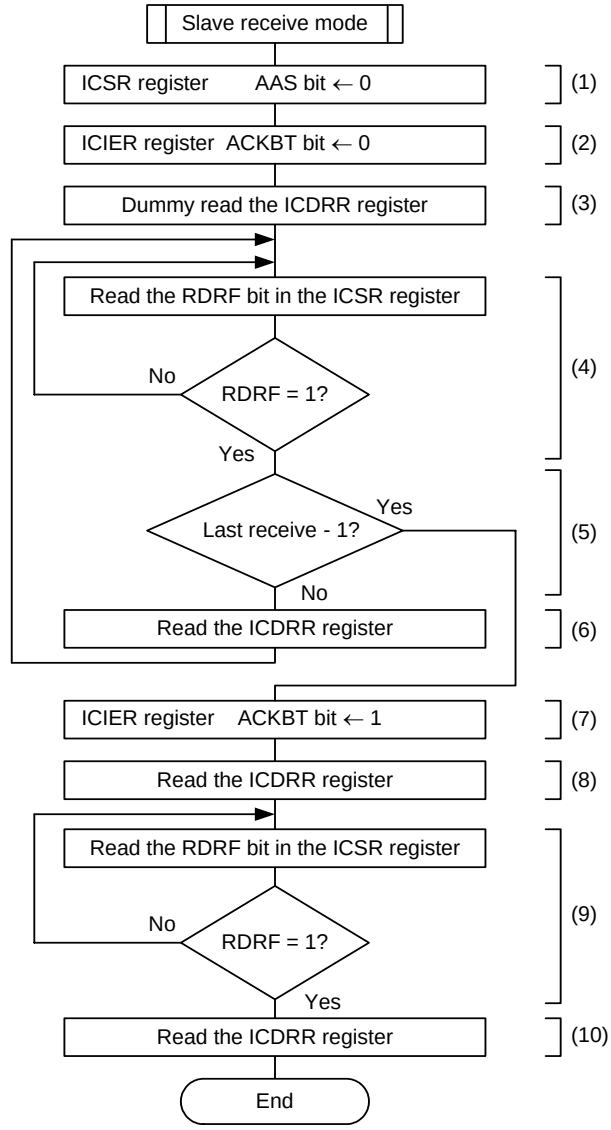


Figure 28.17 Register Setting Example in Slave Transmit Mode (I²C bus Interface Mode)



(1) Set the AAS bit to 0. (1)

(2) Set the ACKBT bit to the transmit device.

(3) Dummy read the ICDRR register.

(4) Wait until 1 byte is received.

(5) Determine (last receive - 1).

(6) Read the receive data.

(7) Set the ACKBT bit of the last byte. (1)

(8) Read the receive data of (last byte - 1).

(9) Wait until the last byte is received.

(10) Read the receive data of the last byte.

Note:
1. For 1 byte of data reception, skip steps (2) to (6) after (1) and jump to process step (7).
Process step (8) is a dummy read from the ICDRR register.

Figure 28.18 Register Setting Example in Slave Receive Mode (I²C bus Interface Mode)

28.7 Noise Canceller

The states of pins SCL and SDA are routed through the noise canceller before being latched internally.
Figure 28.19 shows a Block Diagram of Noise Canceller.
The noise canceller consists of two cascaded latch and match detector circuits. When the SCL pin input signal (or SDA pin input signal) is sampled on f1 and two latch outputs match, the level is passed forward to the next circuit. When they do not match, the former value is retained.

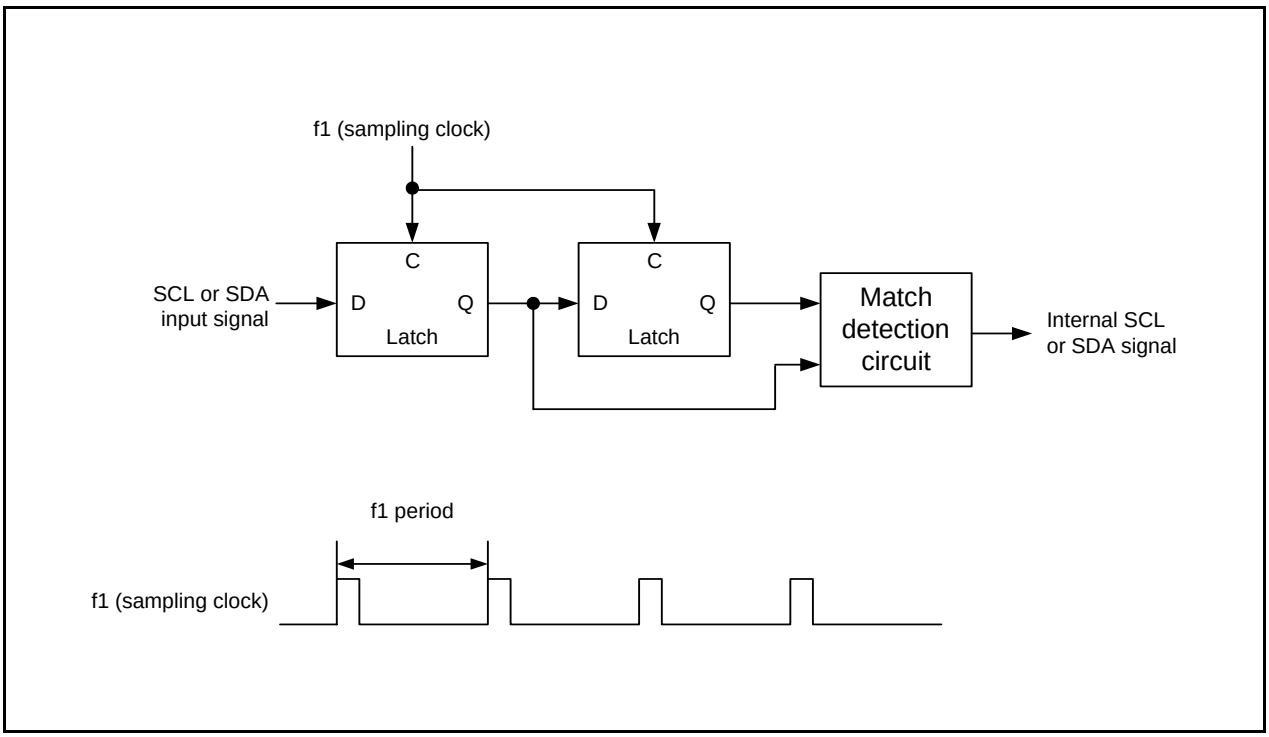


Figure 28.19 Block Diagram of Noise Canceller

28.8 Bit Synchronization Circuit

When the I2C bus interface is set to master mode, the high-level period may become shorter if:

- The SCL signal is held low by a slave device.
- The rise speed of the SCL signal is reduced by a load (load capacity or pull-up resistor) on the SCL line.

Therefore, the SCL signal is monitored and communication is synchronized bit by bit.
Figure 28.20 shows the Bit Synchronization Circuit Timing and Table 28.5 lists the Time between Changing SCL Signal from Low-Level Output to High-Impedance and Monitoring SCL Signal.

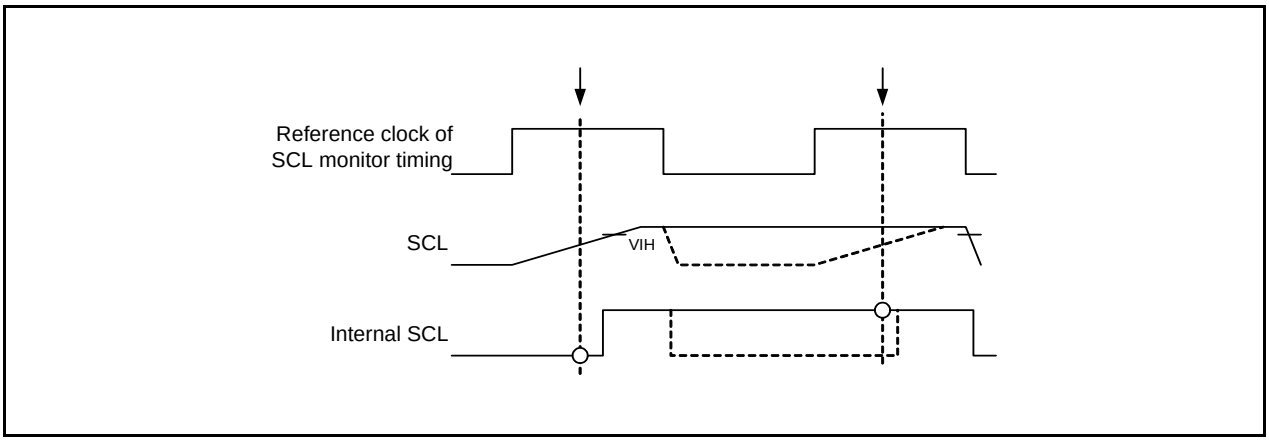


Figure 28.20 Bit Synchronization Circuit Timing

Table 28.5 Time between Changing SCL Signal from Low-Level Output to High-Impedance and Monitoring SCL Signal

ICCR1 Register		SCL Monitoring Time
CKS3	CKS2	
0	0	7.5Tcyc
	1	19.5Tcyc
1	0	17.5Tcyc
	1	41.5Tcyc

1Tcyc = 1/f1(s)

28.9 Notes on I²C bus Interface

To use the I²C bus interface, set the IICSEL bit in the SSUIICSR register to 1 (I²C bus interface function selected).

29. Hardware LIN

The hardware LIN performs LIN communication in cooperation with timer RA and UART0.

29.1 Introduction

The hardware LIN has the features listed below.
Figure 29.1 shows the Hardware LIN Block Diagram.

Master mode
- Synch Break generation
- Bus collision detection

Slave mode
- Synch Break detection
- Synch Field measurement
- Control function for Synch Break and Synch Field signal inputs to UART0
- Bus collision detection

Note:
1. The wake-up function is detected using $\overline{\text{INT1}}$.

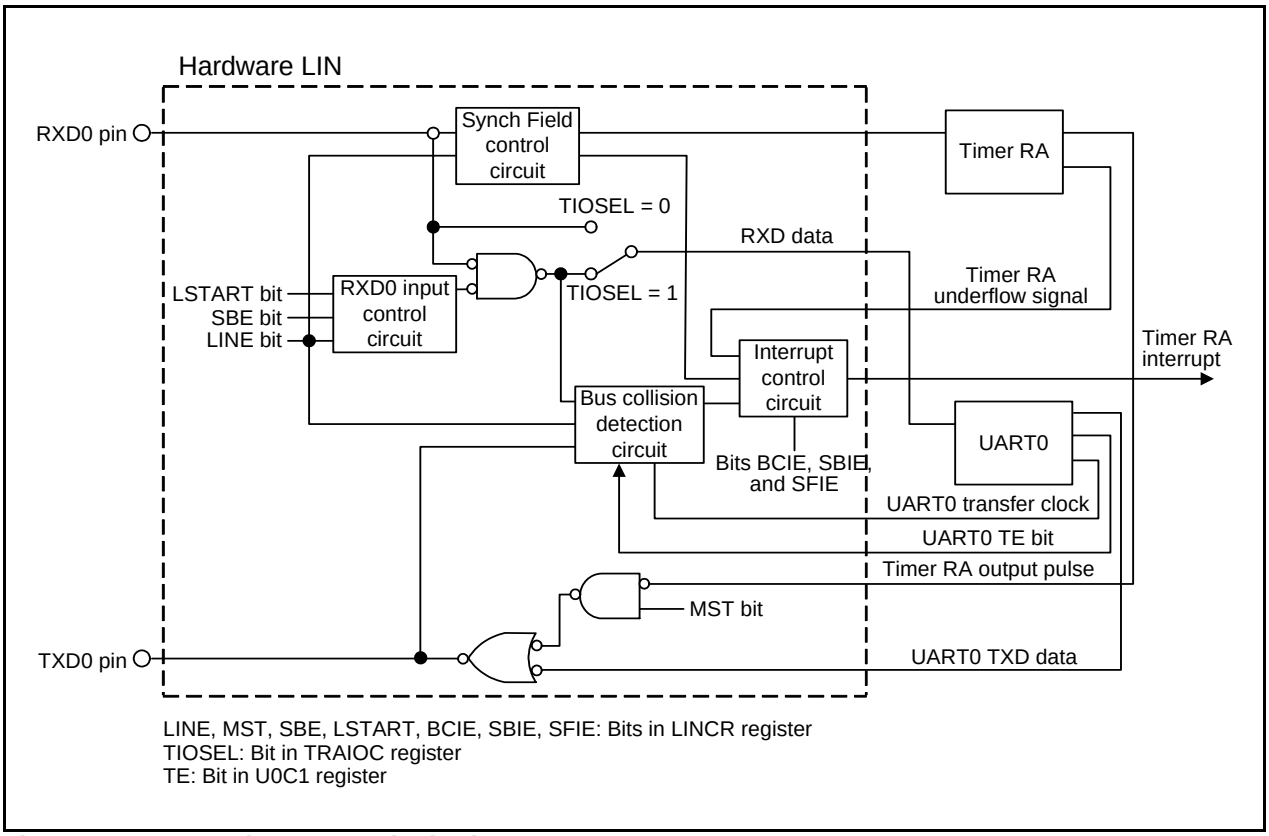


Figure 29.1 Hardware LIN Block Diagram

29.2 Input/Output Pins

Table 29.1 lists the Hardware LIN Pin Configuration.

Table 29.1 Hardware LIN Pin Configuration

Name	Pin Name	Assigned Pin	I/O	Function
Receive data input	RXD0	P11_4	Input	Receive data input for the hardware LIN
Transmit data output	TXD0	P13_1	Output	Transmit data output for the hardware LIN

Note:
1. To use the hardware LIN, set the TXD0SEL0 bit in the U0SR register to 1 and bits RXD0SEL1 to RXD0SEL0 to 10b.

29.3 Registers

The hardware LIN contains the following registers:
- LIN Control Register 2 (LINCR2)
- LIN Control Register (LINCR)
- LIN Status Register (LINST)

29.3.1 LIN Control Register 2 (LINCR2)

Address 0105h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	BCE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	BCE	Bus collision detection enable bit during Sync Break transmission	0: Bus collision detection disabled 1: Bus collision detection enabled	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

29.3.2 LIN Control Register (LINCR)

Address 0106h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	LINE	MST	SBE	LSTART	RXDSF	BCIE	SBIE	SFIE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SFIE	Synch Field measurement-complete interrupt enable bit	0: Synch Field measurement-complete interrupt disabled 1: Synch Field measurement-complete interrupt enabled	R/W
b1	SBIE	Synch Break detection interrupt enable bit	0: Synch Break detection interrupt disabled 1: Synch Break detection interrupt enabled	R/W
b2	BCIE	Bus collision detection interrupt enable bit	0: Bus collision detection interrupt disabled 1: Bus collision detection interrupt enabled	R/W
b3	RXDSF	RXD0 input status flag	0: RXD0 input enabled 1: RXD0 input disabled	R
b4	LSTART	Synch Break detection start bit (1)	When 1 is written, timer RA input is enabled and RXD0 input is disabled. When read, the content is 0.	R/W
b5	SBE	RXD0 input unmasking timing select bit (enabled only in slave mode)	0: Unmasked after Synch Break detection 1: Unmasked after Synch Field measurement is completed	R/W
b6	MST	LIN operation mode setting bit (2)	0: Slave mode (Synch Break detection circuit operation) 1: Master mode (timer RA output OR'ed with TXD0)	R/W
b7	LINE	LIN operation start bit	0: LIN operation stops 1: LIN operation starts (3)	R/W

Notes:
1. After setting the LSTART bit, confirm that the RXDSF flag is set to 1 before Synch Break input starts.
2. Before switching LIN operation modes, stop the LIN operation (LINE bit = 0) once.
3. Inputs to timer RA and UART0 are disabled immediately after the LINE bit is set to 1 (LIN operation starts). (Refer to **Figure 29.3 Header Field Transmission Flowchart Example (1)** and **Figure 29.7 Header Field Reception Flowchart Example (2)**.)

29.3.3 LIN Status Register (LINST)

Address 0107h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	B2CLR	B1CLR	B0CLR	BCDCT	SBDCT	SFDCT
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SFDCT	Synch Field measurement-complete flag	When this bit is set to 1, Synch Field measurement is completed.	R
b1	SBDCT	Synch Break detection flag	when this bit is set to 1, Synch Break is detected or Synch Break generation is completed.	R
b2	BCDCT	Bus collision detection flag	When this bit is set to 1, bus collision is detected.	R
b3	B0CLR	SFDCT flag clear bit	When 1 is written, the SFDCT bit is set to 0. When read, the content is 0.	R/W
b4	B1CLR	SBDCT flag clear bit	When 1 is written, the SBDCT bit is set to 0. When read, the content is 0.	R/W
b5	B2CLR	BCDCT flag clear bit	When 1 is written, the BCDCT bit is set to 0. When read, the content is 0.	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

29.4 Functional Description

29.4.1 Master Mode

Figure 29.2 shows an Operating Example during Header Field Transmission in master mode. Figures 29.3 and 29.4 show Examples of Header Field Transmission Flowchart.
During header field transmission, the hardware LIN operates as follows:

(1) When 1 is written to the TSTART bit in the TRACR register for timer RA, a low-level signal is output from the TXD0 pin for the period set in registers TRAPRE and TRA for timer RA.
(2) When timer RA underflows, the TXD0 pin output is inverted and the SBDCT flag in the LINST register is set to 1. If the SBIE bit in the LINCR register is set to 1, a timer RA interrupt is generated.
(3) The hardware LIN transmits 55h via UART0.
(4) After the hardware LIN completes transmitting 55h, it transmits an ID field via UART0.
(5) After the hardware LIN completes transmitting the ID field, it performs communication for a response field.

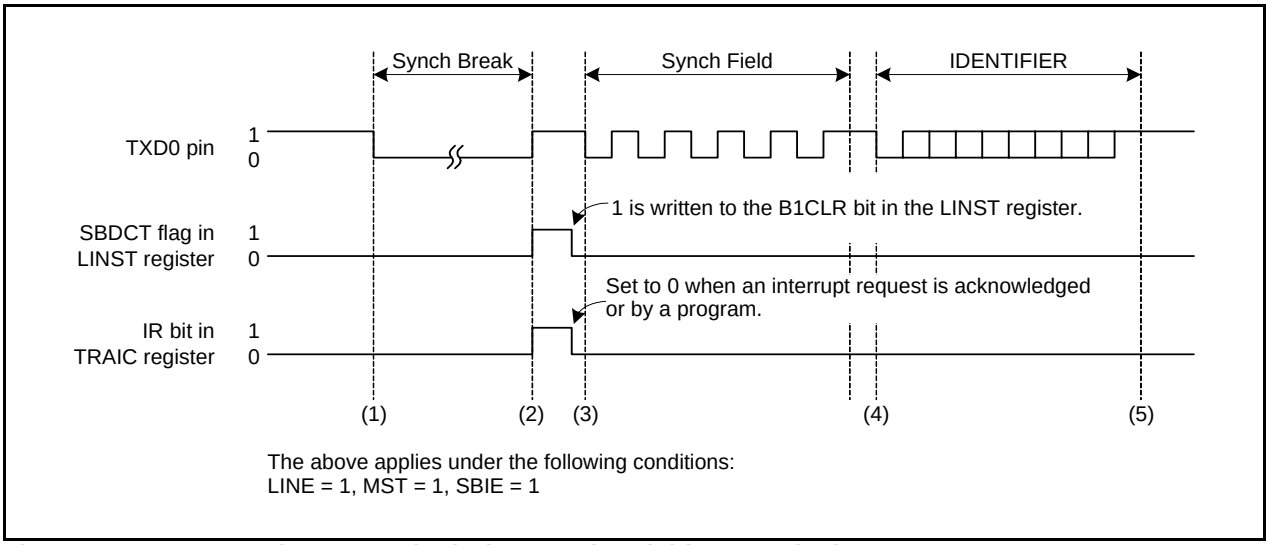
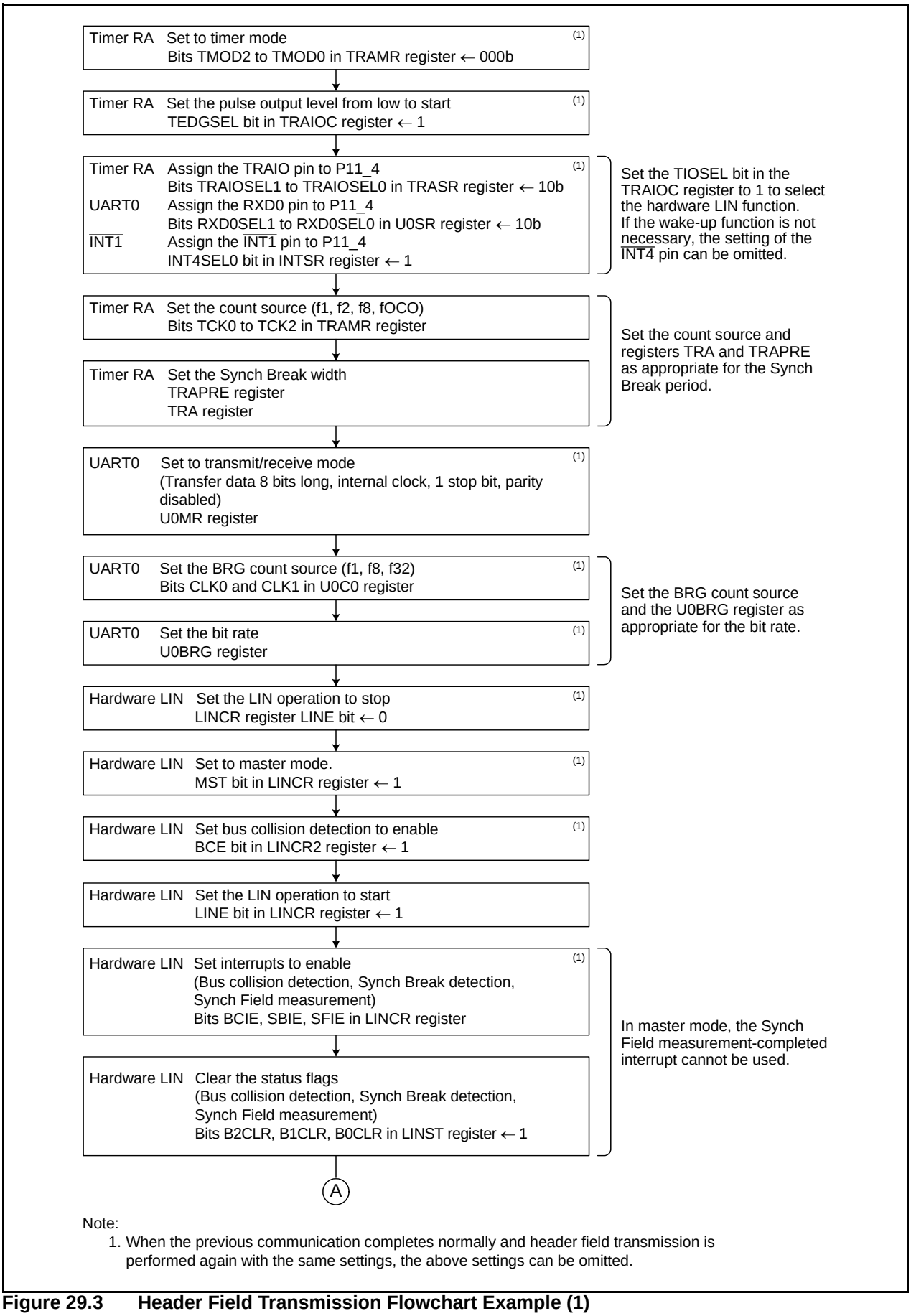


Figure 29.2 Operating Example during Header Field Transmission



Note:
1. When the previous communication completes normally and header field transmission is performed again with the same settings, the above settings can be omitted.

Figure 29.3 Header Field Transmission Flowchart Example (1)

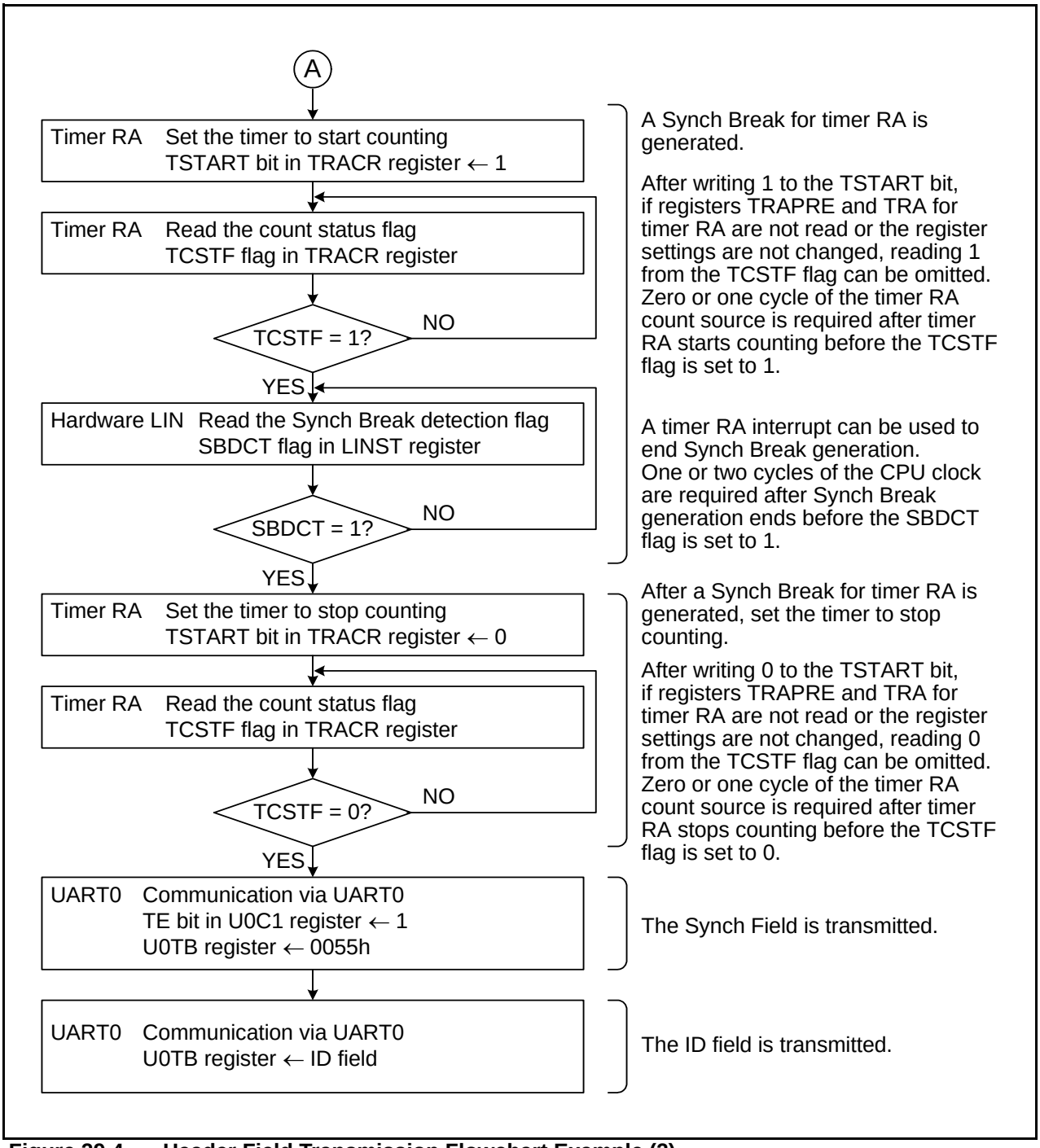


Figure 29.4 Header Field Transmission Flowchart Example (2)

29.4.2 Slave Mode

Figure 29.5 shows an Operating Example during Header Field Reception in slave mode. Figures 29.6 through 29.8 show examples of Header Field Reception Flowchart.
During header field reception, the hardware LIN operates as follows:

(1) When 1 is written to the LSTART bit in the LINCR register for the hardware LIN, Synch Break detection is enabled.
(2) When a low-level signal is input for a duration equal to or longer than the period set in timer RA, the hardware LIN detected it as a Synch Break. At this time, the SBDCT flag in the LINST register is set to 1. If the SBIE bit in the LINCR register is set to 1, a timer RA interrupt is generated. Then the hardware LIN transits to the Synch Field measurement.
(3) The hardware LINA receives a Synch Field (55h) and measures the period of the start bit and bits 0 to 6 is using timer RA. At this time, whether to input the Synch Field signal to RXD0 of UART0 can be selected by the SBE bit in the LINCR register.
(4) When the Synch Field measurement is completed, the SFDCT flag in the LINST register is set to 1. If the SFIE bit in the LINCR register is set to 1, a timer RA interrupt is generated.
(5) After the Synch Field measurement is completed, a transfer rate is calculated from the timer RA count value. The rate is set in UART0 and registers TRAPRE and TRA for timer RA are set again. Then the hardware LIN receives an ID field via UART0.
(6) After the hardware LIN completes receiving the ID field, it performs communication for a response field.

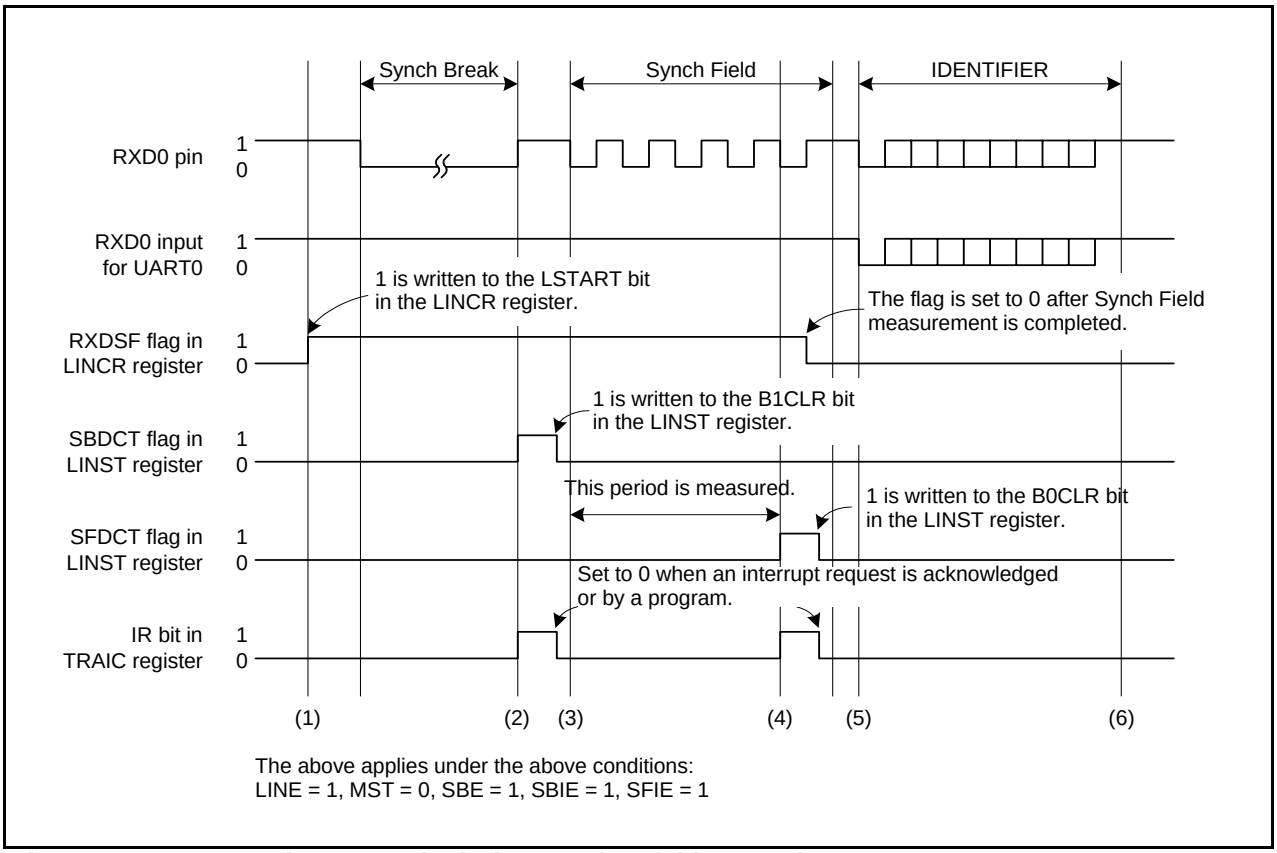
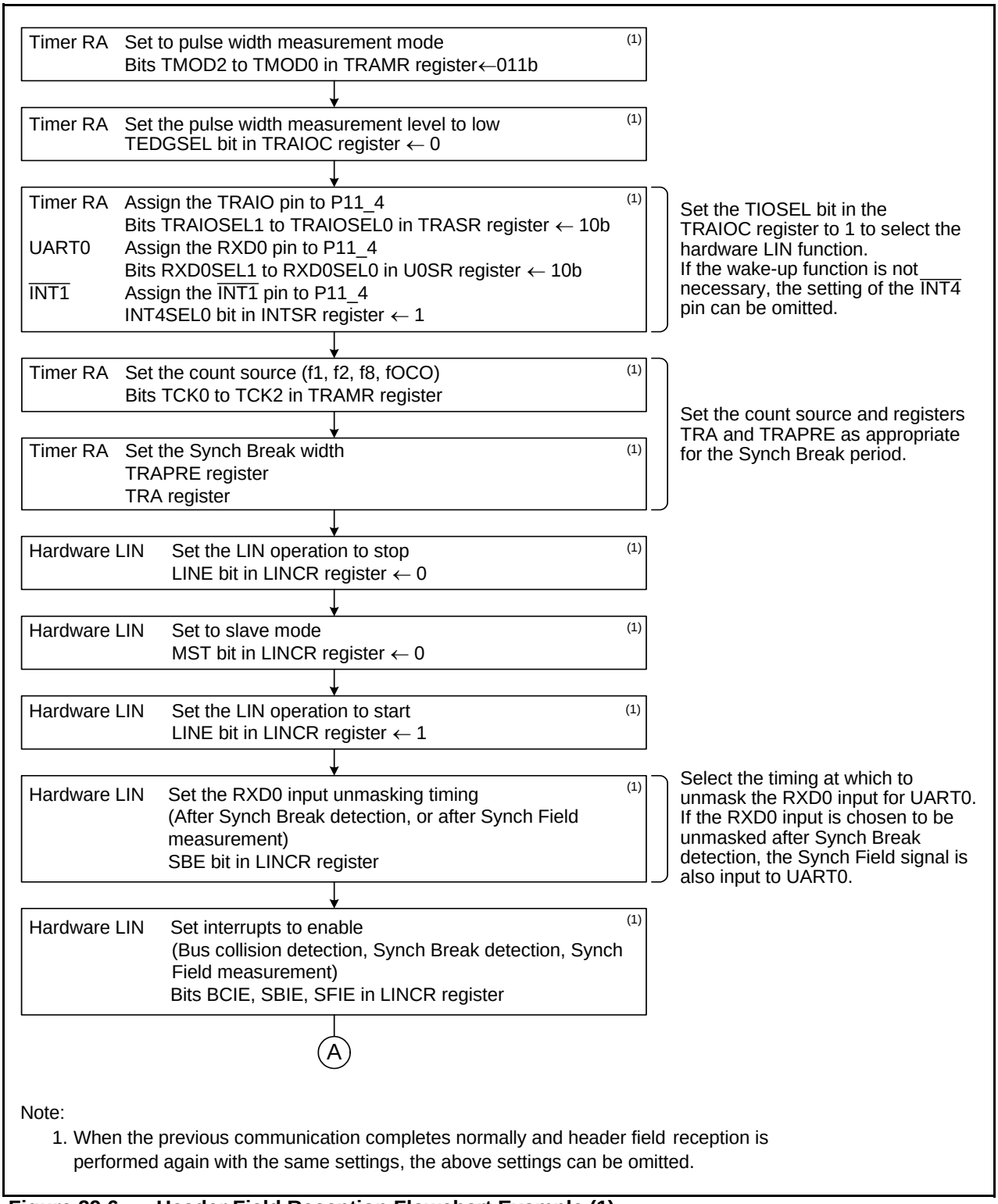


Figure 29.5 Operating Example during Header Field Reception



Note:
1. When the previous communication completes normally and header field reception is performed again with the same settings, the above settings can be omitted.

Figure 29.6 Header Field Reception Flowchart Example (1)

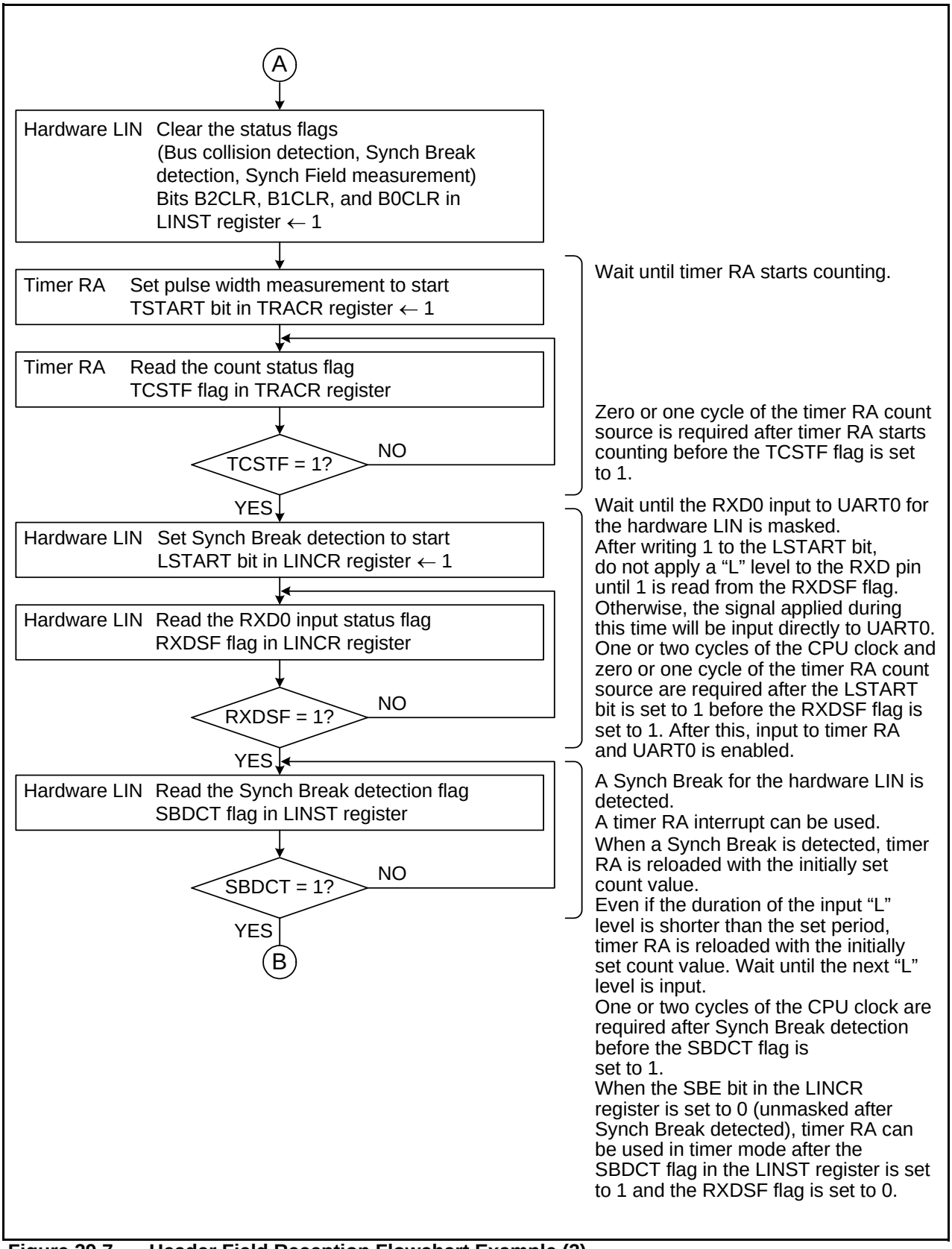


Figure 29.7 Header Field Reception Flowchart Example (2)

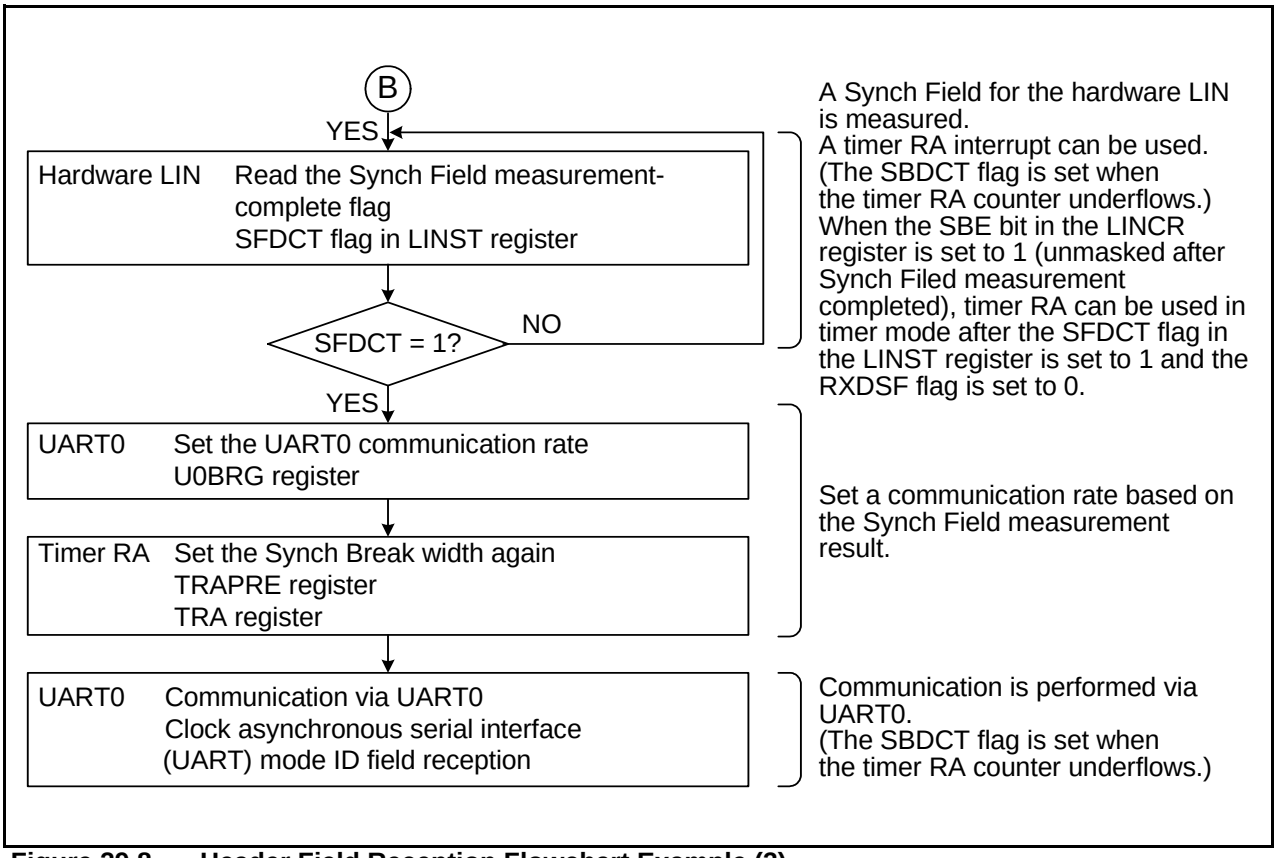


Figure 29.8 Header Field Reception Flowchart Example (3)

29.4.3 Bus Collision Detection Function

The bus collision detection function can be used when UART0 is enabled for transmission (TE bit in U0C1 register = 1). To detect a bus collision during Synch Break transmission, set the BCE bit in the LINCR2 register to 1 (bus collision detection enabled).
Figure 29.9 shows an Operating Example When Bus Collision is Detected.

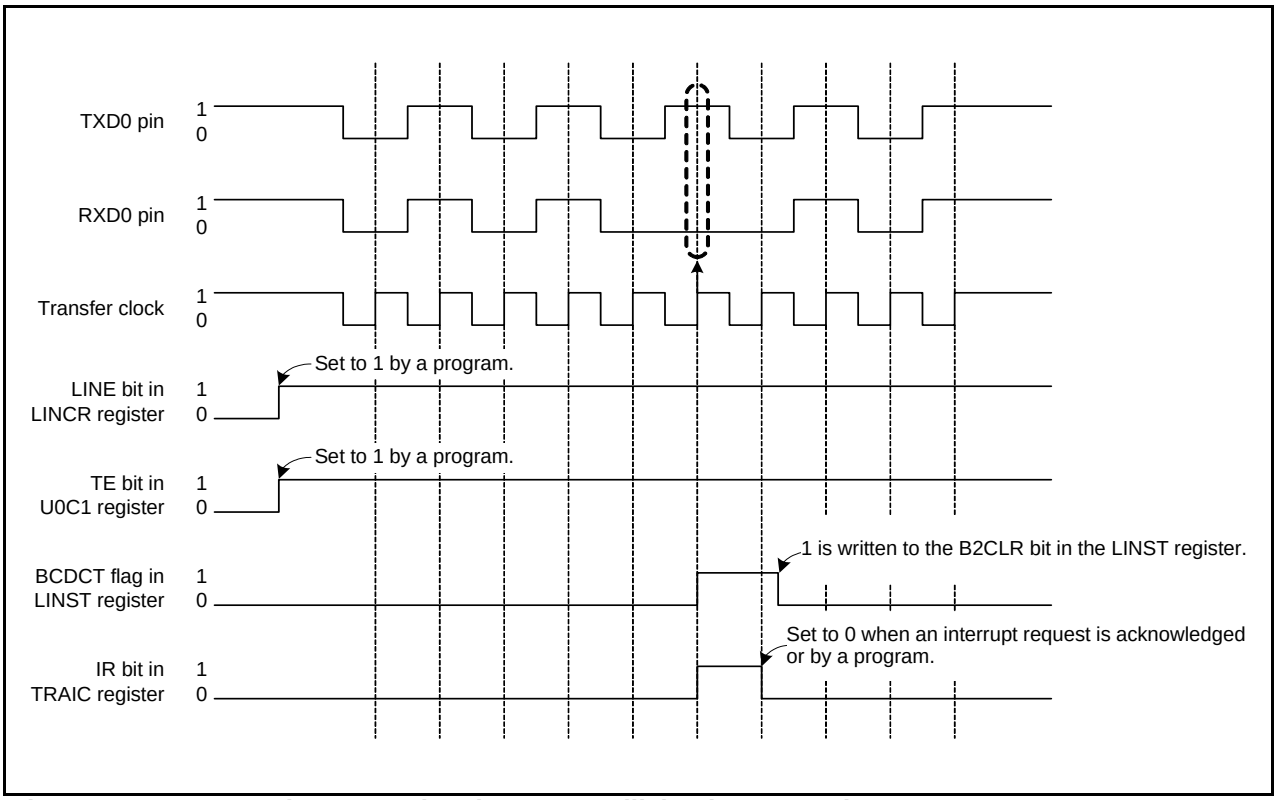


Figure 29.9 Operating Example When Bus Collision is Detected

29.4.4 Hardware LIN End Processing

Figure 29.10 shows an Example of Hardware LIN Communication Completion Flowchart.
Use the following timing for hardware LIN end processing:

- When the hardware bus collision detection function is used
  Perform hardware LIN end processing after checksum transmission completes.
- When the bus collision detection function is not used
  Perform hardware LIN end processing after header field transmission and reception complete.

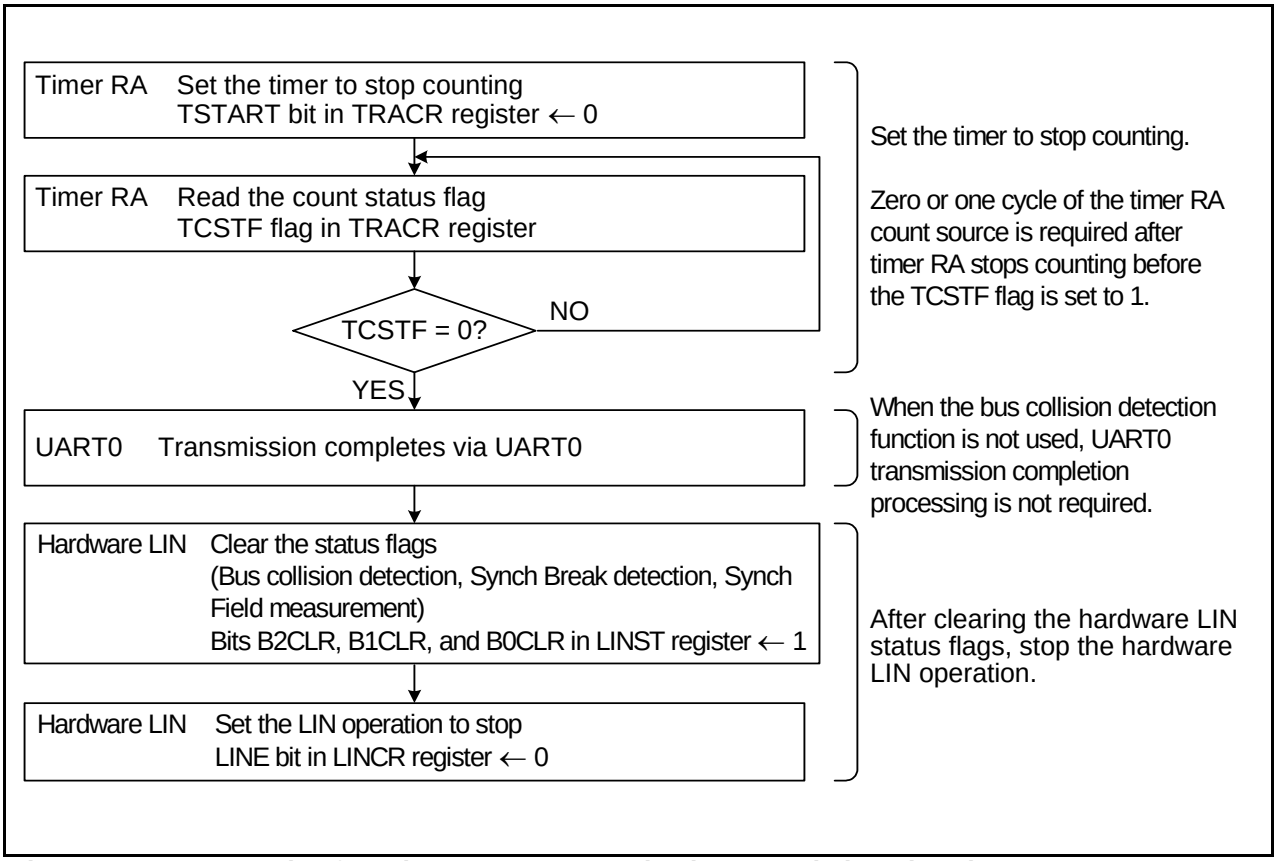


Figure 29.10 Example of Hardware LIN Communication Completion Flowchart

29.5 Interrupt Requests

There are four interrupt requests generated by the hardware LIN: Synch Break detection, completion of Synch Break generation, completion of Synch Field measurement, and bus collision detection. These interrupts are shared with timer RA.
Table 29.2 lists the Hardware LIN Interrupt Requests.

Table 29.2 Hardware LIN Interrupt Requests

Interrupt Request	Status Flag	Interrupt Source
Synch Break detection	SBDCT	Generated when timer RA underflows after the low-level duration for the RXD0 input is measured. Or when a low-level signal is input for a duration longer than the Synch Break period during communication.
Completion of Synch Break generation		Generated when the low-level output to TXD0 for the duration set by timer RA is completed.
Completion of Synch Field measurement	SFDCT	Generated when measurement for 6 bits of the Lynch Field by timer RA is completed.
Bus collision detection	BCDCT	Generated when the RXD0 input and TXD0 output values are different at the data latch timing while UART0 is enabled for transmission.

29.6 Notes on Hardware LIN

For the time-out processing of the header and response fields, use another timer to measure the duration of time with a Synch Break detection interrupt as the starting point.

30. A/D Converter

The A/D converter consists of one 10-bit successive approximation A/D converter circuit with a capacitive coupling amplifier. The analog input shares pins P0_0 to P0_7, P1_0 to P1_3, and P13_0 to P13_7.

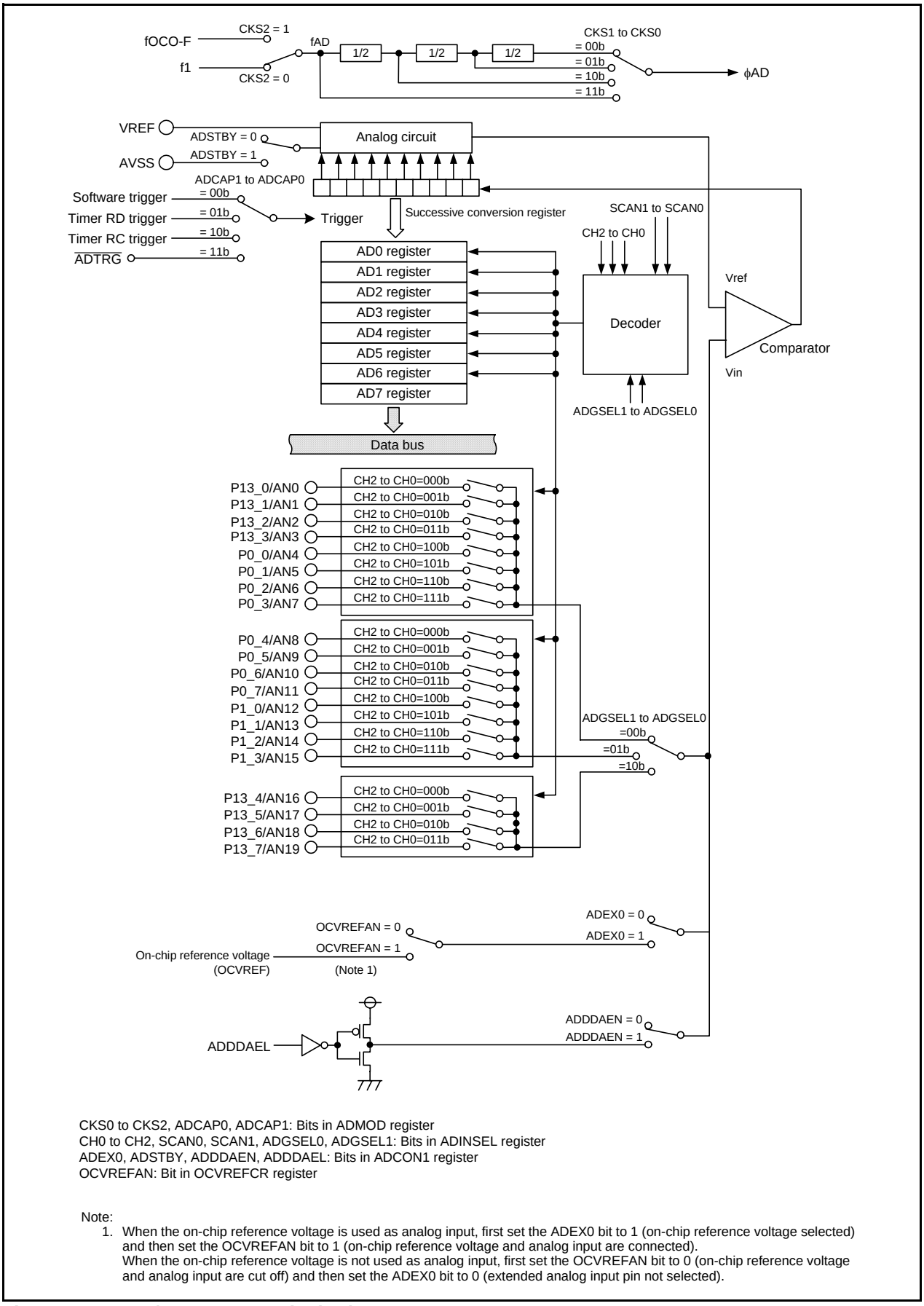
30.1 Introduction

Table 30.1 lists the A/D Converter Performance. Figure 30.1 shows the A/D Converter Block Diagram.

Table 30.1 A/D Converter Performance

Item	Performance
A/D conversion method	Successive approximation (with capacitive coupling amplifier)
Analog input voltage (1)	0 V to AVCC
Operating clock ϕAD (2)	fAD, fAD divided by 2, fAD divided by 4, fAD divided by 8 (fAD = f1 or fOCO-F)
Resolution	8 bits or 10 bits selectable
Absolute accuracy	AVCC = Vref = 5 V, ϕAD = 20 MHz • 8-bit resolution ±2 LSB • 10-bit resolution ±3 LSB AVCC = Vref = 3.3 V, ϕAD = 16 MHz • 8-bit resolution ±2 LSB • 10-bit resolution ±5 LSB AVCC = Vref = 3.0 V, ϕAD = 10 MHz • 8-bit resolution ±2 LSB • 10-bit resolution ±5 LSB AVCC = Vref = 2.2 V, ϕAD = 5 MHz • 8-bit resolution ±2 LSB • 10-bit resolution ±5 LSB
Operating modes	One-shot mode, repeat mode 0, repeat mode 1, single sweep mode, and repeat sweep mode
Analog input pins	20 pins (AN0 to AN19)
A/D conversion start conditions	• Software trigger • Timer RD • Timer RC • External trigger (Refer to **30.3.3 A/D Conversion Start Conditions**.)
Conversion rate per pin (3) (ϕAD = fAD)	Minimum 43 ϕAD cycles

Notes:
1. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.
2. When 4.0 V ≤ AVCC ≤ 5.5 V, the frequency of ϕAD must be 20 MHz or below.
   When 3.2 V ≤ AVCC < 4.0 V, the frequency of ϕAD must be 16 MHz or below.
   When 3.0 V ≤ AVCC < 3.2 V, the frequency of ϕAD must be 10 MHz or below.
   When 2.2 V ≤ AVCC < 3.0 V, the frequency of ϕAD must be 5 MHz or below.
   The frequency of ϕAD must be 2 MHz or above.
3. The conversion rate per pin is minimum 43 ϕAD cycles for 8-bit and 10-bit resolution.



CKS0 to CKS2, ADCAP0, ADCAP1: Bits in ADMOD register
CH0 to CH2, SCAN0, SCAN1, ADGSEL0, ADGSEL1: Bits in ADINSEL register
ADEX0, ADSTBY, ADDDAEN, ADDDAEL: Bits in ADCON1 register
OCVREFAN: Bit in OCVREFCR register

Note:
1. When the on-chip reference voltage is used as analog input, first set the ADEX0 bit to 1 (on-chip reference voltage selected) and then set the OCVREFAN bit to 1 (on-chip reference voltage and analog input are connected).
When the on-chip reference voltage is not used as analog input, first set the OCVREFAN bit to 0 (on-chip reference voltage and analog input are cut off) and then set the ADEX0 bit to 0 (extended analog input pin not selected).

Figure 30.1 A/D Converter Block Diagram

30.2 Registers

30.2.1 On-Chip Reference Voltage Control Register (OCVREFCR)

Address 0026h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	OCVREFAN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	OCVREFAN	On-chip reference voltage to analog input connect bit (1)	0: On-chip reference voltage and analog input are cut off 1: On-chip reference voltage and analog input are connected	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. When the on-chip reference voltage is used as analog input, first set the ADEX0 bit in the ADCON1 register to 1 (on-chip reference voltage selected) and then set the OCVREFAN bit to 1 (on-chip reference voltage and analog input are connected).
   When the on-chip reference voltage is not used as analog input, first set the OCVREFAN bit to 0 (on-chip reference voltage and analog input are cut off) and then set the ADEX0 bit to 0 (extended analog input pin not selected).

   Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the OCVREFCR register.
   If the content of the OCVREFCR register is rewritten during A/D conversion, the conversion result is undefined.

30.2.2 A/D Register i (ADi) (i = 0 to 7)

Address 00C1h to 00C0h (AD0), 00C3h to 00C2h (AD1), 00C5h to 00C4h (AD2),
00C7h to 00C6h (AD3), 00C9h to 00C8h (AD4), 00CBh to 00CAh (AD5),
00CDh to 00CCh (AD6), 00CFh to 00CEh (AD7)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	X	X

Bit	Function		R/W
	10-bit mode (BITS bit in ADCON1 register = 1)	8-bit mode (BITS bit in ADCON1 register = 0)	
b0	8 low-order bits in A/D conversion result	A/D conversion result	R
b1			
b2			
b3			
b4			
b5			
b6			
b7			
b8	2 high-order bits in A/D conversion result	When read, the content is 0.	R
b9			
b10	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b11			
b12			
b13			
b14			
b15	Reserved bit	When read, the content is undefined.	R

If the contents of the ADCON1, ADMOD, ADINSEL, or OCVREFCR register are written during A/D conversion, the conversion result is undefined.
When using the A/D converter in 10-bit mode, repeat mode 0, repeat mode 1, or repeat sweep mode, access the ADi register in 16-bit units. Do not access it in 8-bit units.

30.2.3 A/D Mode Register (ADMOD)

Address 00D4h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADCAP1	ADCAP0	MD2	MD1	MD0	CKS2	CKS1	CKS0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CKS0	Division select bit	b1 b0 0 0: fAD divided by 8 0 1: fAD divided by 4 1 0: fAD divided by 2 1 1: fAD divided by 1 (no division)	R/W
b1	CKS1			R/W
b2	CKS2	Clock source select bit (1)	0: f1 selected 1: fOCO-F selected	R/W
b3	MD0	A/D operating mode select bit	b5 b4 b3 0 0 0: One-shot mode 0 0 1: Do not set. 0 1 0: Repeat mode 0 0 1 1: Repeat mode 1 1 0 0: Single sweep mode 1 0 1: Do not set. 1 1 0: Repeat sweep mode 1 1 1: Do not set.	R/W
b4	MD1			R/W
b5	MD2			R/W
b6	ADCAP0	A/D conversion trigger select bit	b7 b6 0 0: A/D conversion starts by software trigger (ADST bit in ADCON0 register) 0 1: A/D conversion starts by conversion trigger from timer RD 1 0: A/D conversion starts by conversion trigger from timer RC 1 1: A/D conversion starts by external trigger ($\overline{\text{ADTRG}}$)	R/W
b7	ADCAP1			R/W

Note:
1. When the CKS2 bit is changed, wait for three ϕAD cycles or more before starting A/D conversion.

If the content of the ADMOD register is rewritten during A/D conversion, the conversion result is undefined.

30.2.4 A/D Input Select Register (ADINSEL)

Address 00D5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADGSEL1	ADGSEL0	SCAN1	SCAN0	—	CH2	CH1	CH0
After Reset	1	1	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CH0	Analog input pin select bit	Refer to **Table 30.2 Analog Input Pin Selection**	R/W
b1	CH1			R/W
b2	CH2			R/W
b3	—	Reserved bit	Set to 0.	R/W
b4	SCAN0	A/D sweep pin count select bit	b5 b4 0 0: 2 pins 0 1: 4 pins 1 0: 6 pins 1 1: 8 pins	R/W
b5	SCAN1			R/W
b6	ADGSEL0	A/D input group select bit	b7 b6 0 0: Port P13_0 to P13_3 and port P0_0 to P0_3 groups selected 0 1: Port P0_4 to P0_7 and port P1_0 to P1_3 groups selected 1 0: Port P13_4 to P13_7 group selected 1 1: Port group not selected	R/W
b7	ADGSEL1			R/W

If the content of the ADINSEL register is rewritten during A/D conversion, the conversion result is undefined.

Table 30.2 Analog Input Pin Selection

Bits CH2 to CH0	Bits ADGSEL1 to ADGSEL0 = 00b	Bits ADGSEL1 to ADGSEL0 = 01b	Bits ADGSEL1 to ADGSEL0 = 10b
000b	AN0	AN8	AN16
001b	AN1	AN9	AN17
010b	AN2	AN10	AN18
011b	AN3	AN11	AN19
100b	AN4	AN12	Do not set.
101b	AN5	AN13	
110b	AN6	AN14	
111b	AN7	AN15	

30.2.5 A/D Control Register 0 (ADCON0)

Address 00D6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	ADST
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADST	A/D conversion start flag	0: A/D conversion stops 1: A/D conversion starts	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

ADST Bit (A/D Conversion Start Flag)

[Conditions for setting to 1] When A/D conversion starts and while A/D conversion is in progress.
[Condition for setting to 0] When A/D conversion stops.

30.2.6 A/D Control Register 1 (ADCON1)

Address 00D7h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADDDAEL	ADDDAEN	ADSTBY	BITS	—	—	—	ADEX0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADEX0	Extended analog input pin select bit (1)	0: Extended analog input pin not selected 1: On-chip reference voltage selected (2)	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	BITS	8-/10-bit mode select bit	0: 8-bit mode 1: 10-bit mode	R/W
b5	ADSTBY	A/D standby bit (3)	0: A/D operation stops (standby) 1: A/D operation enabled	R/W
b6	ADDDAEN	A/D open-circuit detection assist function enable bit (4)	0: Disabled 1: Enabled	R/W
b7	ADDDAEL	A/D open-circuit detection assist method select bit (4)	0: Discharge before conversion 1: Precharge before conversion	R/W

Notes:
1. When the on-chip reference voltage is used as analog input, first set the ADEX0 bit to 1 (on-chip reference voltage selected) and then set the OCVREFAN bit in the OCVREFCR register to 1 (on-chip reference voltage and analog input are connected).
   When the on-chip reference voltage is not used as analog input, first set the OCVREFAN bit to 0 (on-chip reference voltage and analog input are cut off) and then set the ADEX0 bit to 0 (extended analog input pin not selected).
2. Do not set in single sweep mode or repeat sweep mode.
3. When the ADSTBY bit is changed from 0 (A/D operation stops) to 1 (A/D operation enabled), wait for one ϕAD cycle or more before starting A/D conversion.
4. To enable the A/D open-circuit detection assist function, select the conversion start state with the ADDDAEL bit after setting the ADDDAEN bit to 1 (enabled).
   The conversion result for an open circuit varies with external circuits. Careful evaluation should be performed according to the system before using this function.
   If the content of the ADCON1 register is rewritten during A/D conversion, the conversion result is undefined.

30.3 Common Items for Multiple Modes

30.3.1 Input/Output Pins

The analog input shares pins P0_0 to P0_7, P1_0 to P1_3, and P13_0 to P13_7 in AN0 to AN19.
To use the ANi (i = 0 to 19) pin as input, set the corresponding port direction bit to 0 (input mode).
After changing the A/D operating mode, select an analog input pin again.

30.3.2 A/D Conversion Cycles

Figure 30.2 shows the Timing Diagram of A/D Conversion. Figure 30.3 shows the A/D Conversion Cycles (ϕAD = fAD).

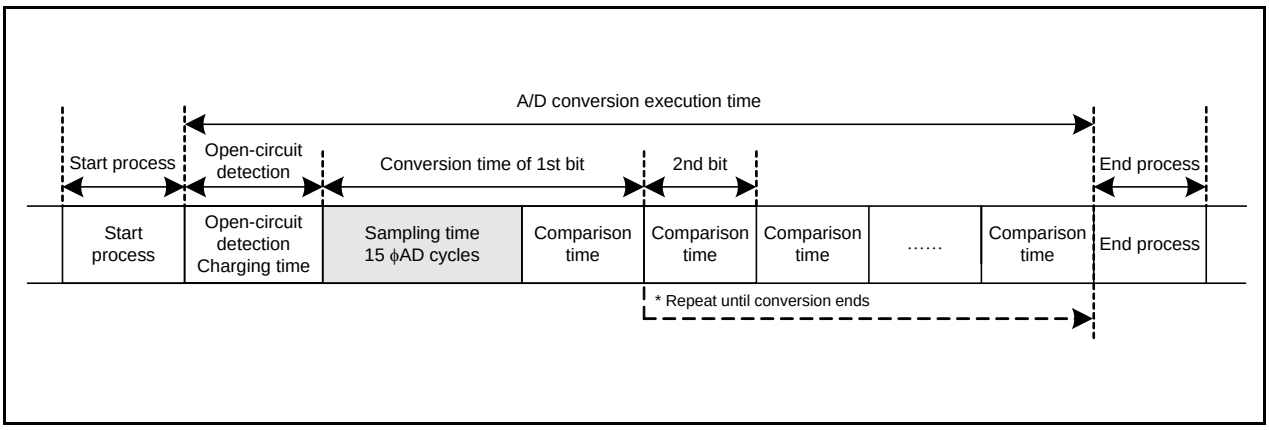
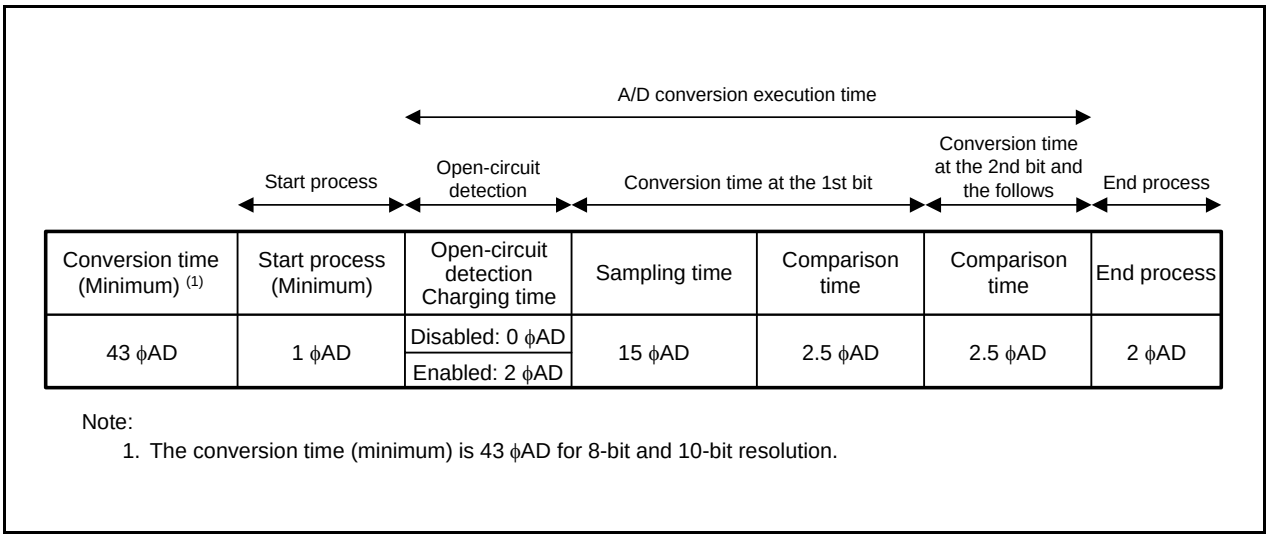


Figure 30.2 Timing Diagram of A/D Conversion



Conversion time (Minimum) (1)	Start process (Minimum)	Open-circuit detection Charging time	Sampling time	Comparison time	Comparison time	End process
43 ϕAD	1 ϕAD	Disabled: 0 ϕAD Enabled: 2 ϕAD	15 ϕAD	2.5 ϕAD	2.5 ϕAD	2 ϕAD

Note:
1. The conversion time (minimum) is 43 ϕAD for 8-bit and 10-bit resolution.

Figure 30.3 A/D Conversion Cycles (ϕAD = fAD)

Table 30.3 shows the Number of Cycles for A/D Conversion Items. The A/D conversion time is defined as follows:
The start process time varies depending on which ϕAD is selected.
When 1 (A/D conversion starts) is written to the ADST bit in the ADCON0 register, an A/D conversion starts after the start process time has elapsed. Reading the ADST bit before the A/D conversion returns 0 (A/D conversion stops).
In the modes where an A/D conversion is performed on multiple pins or multiple times, the between-execution process time is inserted between the A/D conversion execution time for one pin and the next A/D conversion time.
In one-shot mode and single sweep mode, the ADST bit is set to 0 during the end process time and the last A/D conversion result is stored in the ADi register.

- In on-shot mode
  Start process time + A/D conversion execution time + end process time

- When two pins are selected in single sweep mode
  Start process time + (A/D conversion execution time + between-execution process time + A/D conversion execution time) + end process time

Table 30.3 Number of Cycles for A/D Conversion Items

A/D Conversion Item		Number of Cycles
Start process time	ϕAD = fAD	1 or 2 fAD cycles
	ϕAD = fAD divided by 2	2 or 3 fAD cycles
	ϕAD = fAD divided by 4	3 or 4 fAD cycles
	ϕAD = fAD divided by 8	5 or 6 fAD cycles
A/D conversion execution time	Open-circuit detection disabled	40 ϕAD cycles
	Open-circuit detection enabled	42 ϕAD cycles
Between-execution process time		1 ϕAD cycle
End process time		2 or 3 fAD cycles

30.3.3 A/D Conversion Start Conditions

A software trigger, trigger from timer RD or timer RC, and external trigger are used as A/D conversion start triggers.
Figure 30.4 shows the Block Diagram of A/D Conversion Start Control Unit.

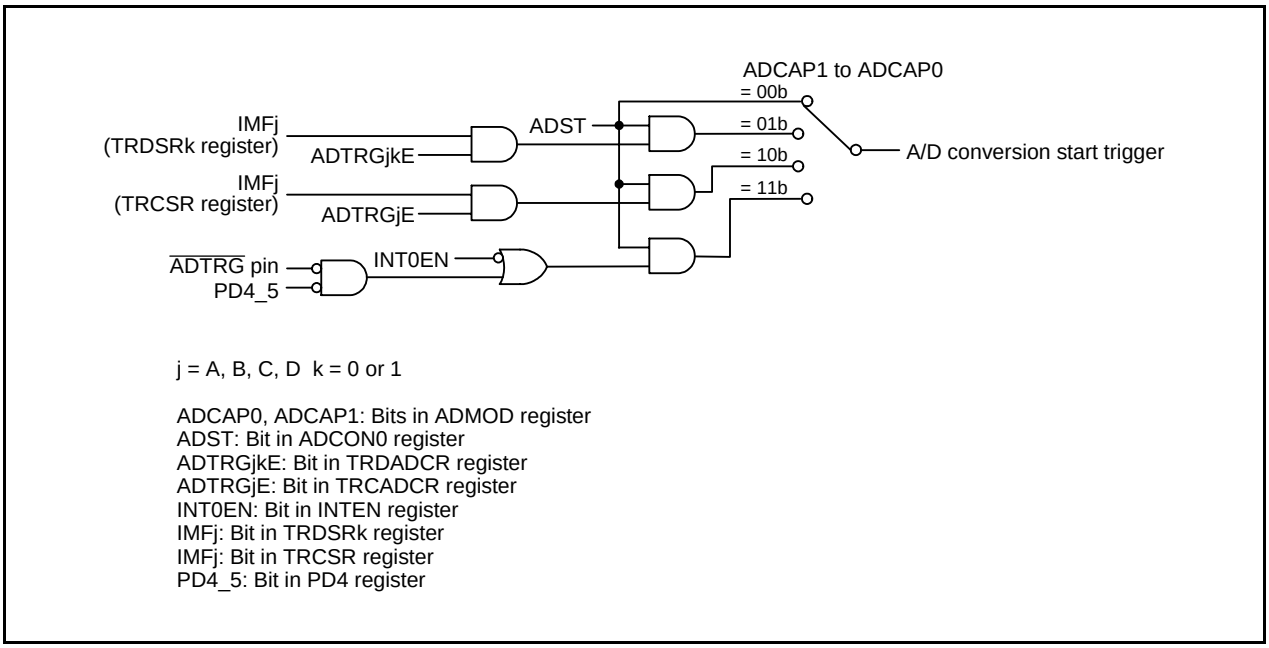


Figure 30.4 Block Diagram of A/D Conversion Start Control Unit

30.3.3.1 Software Trigger

A software trigger is selected when bits ADCAP1 to ADCAP0 in the ADMOD register are set to 00b (software trigger).
The A/D conversion starts when the ADST bit in the ADCON0 register is set to 1 (A/D conversion starts).

30.3.3.2 Trigger from Timer RD

This trigger is selected when bits ADCAP1 to ADCAP0 in the ADMOD register are set to 01b (timer RD).
To use this function, make sure the following conditions are met:

- Bits ADCAP1 to ADCAP0 in the ADMOD register are set to 01b (timer RD).
- Timer RD is used in the output compare function (timer mode, PWM mode, reset synchronous PWM mode, complementary PWM mode, and PWM3 mode).
- The ADTRGjkE bit (j = A, B, C, D, k = 0 or 1) in the TRDADCR register is set to 1 (A/D trigger occurs at compare match with TRDGRjk register).
- The ADST bit in the ADCON0 register is set to 1 (A/D conversion starts).

When the IMFj bit in the TRDSRk register is changed from 0 to 1 under the above conditions, A/D conversion starts.
Refer to **21. Timer RD**, **21.4 Output Compare Function**, **21.5 PWM Mode**, **21.6 Reset Synchronous PWM Mode**, **21.7 Complementary PWM Mode**, **21.8 PWM3 Mode** for the details of timer RD and the output compare function (timer mode, PWM mode, reset synchronous PWM mode, complementary PWM mode, and PWM3 mode).

30.3.3.3 Trigger from Timer RC

This trigger is selected when bits ADCAP1 to ADCAP0 in the ADMOD register are set to 10b (timer RC).
To use this function, make sure the following conditions are met:

- Bits ADCAP1 to ADCAP0 in the ADMOD register are set to 10b (timer RC).
- Timer RC is used in the output compare function (timer mode, PWM mode, and PWM2 mode).
- The ADTRGjE bit (j = A, B, C, D) in the TRCADCR register is set to 1 (A/D trigger occurs at compare match with TRCGRj register).
- The ADST bit in the ADCON0 register is set to 1 (A/D conversion starts).

When the IMFj bit in the TRCSR register is changed from 0 to 1 under the above conditions, A/D conversion starts.
Refer to **20. Timer RC**, **20.5 Timer Mode (Output Compare Function)**, **20.6 PWM Mode**, **20.7 PWM2 Mode** for the details of timer RC and the output compare function (timer mode, PWM mode, and PWM2 mode).

30.3.3.4 External Trigger

This trigger is selected when bits ADCAP1 to ADCAP0 in the ADMOD register are set to 11b (external trigger ($\overline{\text{ADTRG}}$)).
To use this function, make sure the following conditions are met:

- Bits ADCAP1 to ADCAP0 in the ADMOD register are set to 11b (external trigger ($\overline{\text{ADTRG}}$)).
- The INT7EN bit in the INTEN register is set to 1 (($\overline{\text{INT7}}$ input enabled)).
- The port direction register is set to input:
  When the INT7SEL0 bit in the INTSR register is 0, the PD3_7 bit in the PD3 register is set to 0 (input mode).
  When the INT7SEL0 bit in the INTSR register is 1, the PD11_7 bit in the PD11 register is set to 0 (input mode)
- The ADST bit in the ADCON0 register is set to 1 (A/D conversion starts).

When the $\overline{\text{ADTRG}}$ pin input is changed from high to low under the above conditions, A/D conversion starts.

30.3.4 A/D Conversion Result

The A/D conversion result is stored in the ADi register (i = 0 to 7). The register where the result is stored varies depending on the A/D operating mode used. The contents of the ADi register are undefined after reset. Values cannot be written to the ADi register.

In repeat mode 0, no interrupt request is generated. After the first AD conversion is completed, determine if the A/D conversion time has elapsed by a program.
In one-shot mode, repeat mode 1, single sweep mode, and repeat sweep mode, an interrupt request is generated at certain times, such as when an A/D conversion completes (the IR bit in the ADIC register is set to 1).
However, in repeat mode 1 and repeat sweep mode, A/D conversion continues after an interrupt request is generated. Read the ADi register before the next A/D conversion is completed, since at completion the ADi register is rewritten with the new value.

In one-shot mode and single sweep mode, when bits ADCAP1 to ADCAP0 in the ADMOD register is set to 00b (software trigger), the ADST bit in the ADCON0 register is used to determine whether the A/D conversion or sweep has completed.

During an A/D conversion operation, if the ADST bit in the ADCON0 register is set to 0 (A/D conversion stops) by a program to forcibly terminate A/D conversion, the conversion result of the A/D converter is undefined and no interrupt is generated. If the ADST bit is set to 0 by a program, do not use the value of the ADi register.

30.3.5 Low-Current-Consumption Function

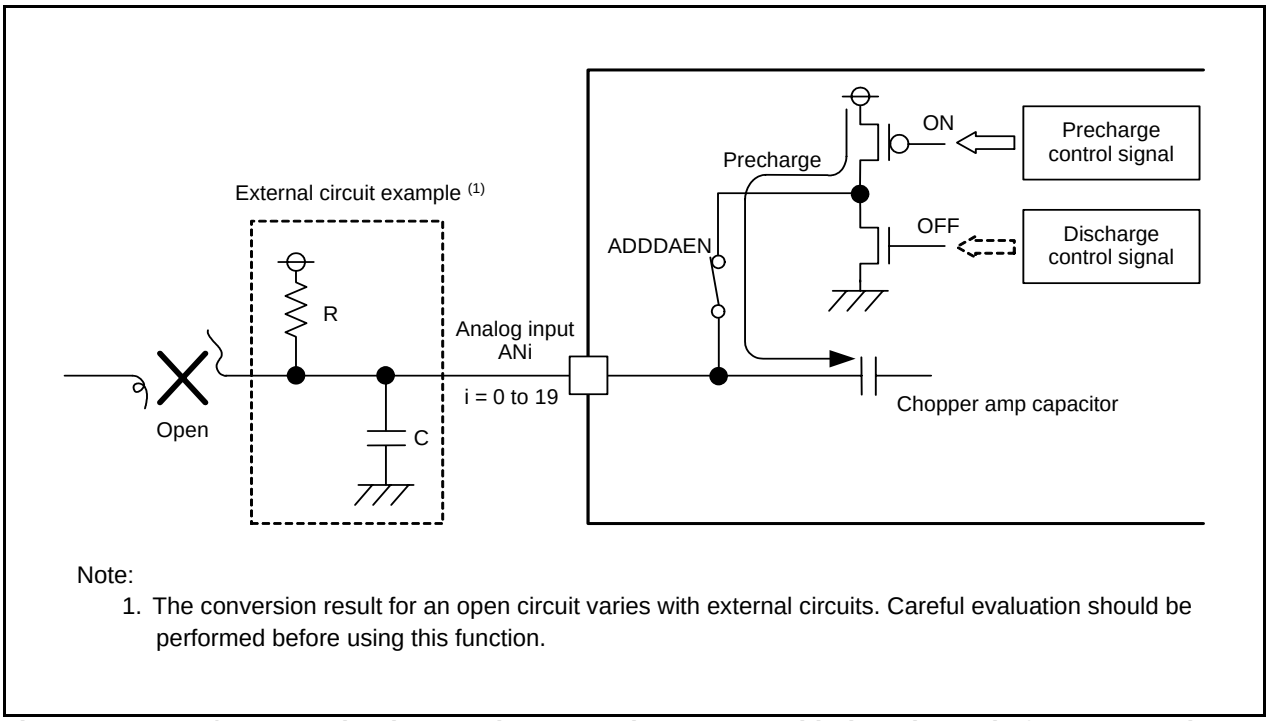
When the A/D converter is not used, power consumption can be reduced by setting the ADSTBY bit in the ADCON1 register to 0 (A/D operation stops (standby)) to shut off any analog circuit current flow.
To use the A/D converter, set the ADSTBY bit to 1 (A/D operation enabled) and wait for one ϕAD cycle or more before setting the ADST bit in the ADCON0 register to 1 (A/D conversion starts). Do not write 1 to bits ADST and ADSTBY at the same time.
Also, do not set the ADSTBY bit to 0 (A/D operation stops (standby)) during the A/D conversion.

30.3.6 Extended Analog Input Pins

In one-shot mode, repeat mode 0, and repeat mode 1, the on-chip reference voltage (OCVREF) can be used as analog input.
Any variation in VREF can be confirmed using the on-chip reference voltage. Use the ADEX0 bit in the ADCON1 register and the OCVREFAN bit in the OCVREFCR register to select the on-chip reference voltage.
The A/D conversion result of the on-chip reference voltage in one-shot mode or in repeat mode 0 is stored in the AD0 register.

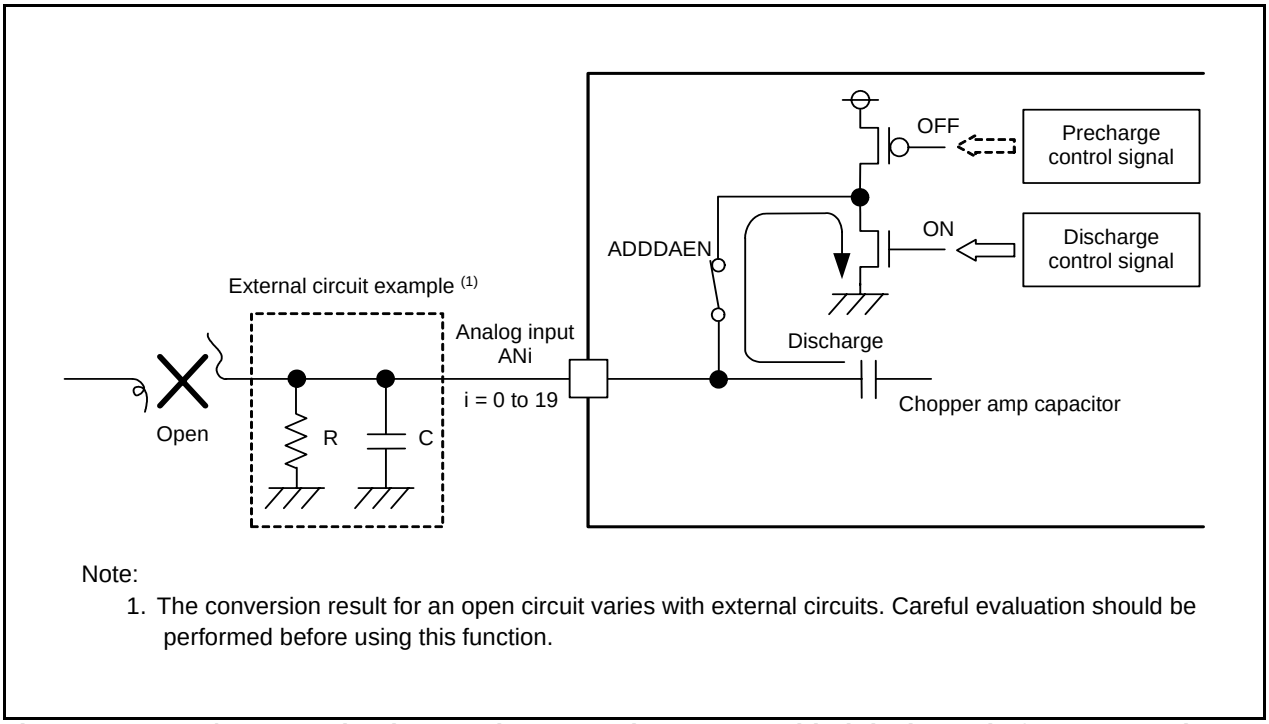
30.3.7 A/D Open-Circuit Detection Assist Function

To suppress influences of the analog input voltage leakage from the previously converted channel during A/D conversion operation, a function is incorporated to fix the electric charge on the chopper amp capacitor to the predetermined state (AVCC or GND) before starting conversion.
This function enables more reliable detection of an open circuit in the wiring connected to the analog input pins.
Figure 30.5 shows the A/D Open-Circuit Detection Example on AVCC Side (Precharge before Conversion Selected) and Figure 30.6 shows the A/D Open-Circuit Detection Example on AVSS Side (Discharge before Conversion Selected).



Note:
1. The conversion result for an open circuit varies with external circuits. Careful evaluation should be performed before using this function.

Figure 30.5 A/D Open-Circuit Detection Example on AVCC Side (Precharge before Conversion Selected)



Note:
1. The conversion result for an open circuit varies with external circuits. Careful evaluation should be performed before using this function.

Figure 30.6 A/D Open-Circuit Detection Example on AVSS Side (Discharge before Conversion Selected)

30.4 One-Shot Mode

In one-shot mode, the input voltage to one pin selected from among AN0 to AN19 or OCVREF is A/D converted once.
Table 30.4 lists the One-Shot Mode Specifications.

Table 30.4 One-Shot Mode Specifications

Item	Specification
Function	The input voltage to the pin selected by bits CH2 to CH0 and bits ADGSEL1 to ADGSEL0 in the ADINSEL register or the ADEX0 bit in the ADCON1 register is A/D converted once.
Resolution	8 bits or 10 bits selectable
A/D conversion start conditions	• Software trigger • Timer RD • Timer RC • External trigger (Refer to **30.3.3 A/D Conversion Start Conditions)**
A/D conversion stop conditions	• A/D conversion completes (when bits ADCAP1 to ADCAP0 in the ADMOD register are set to 00b (software trigger), the ADST bit in the ADCON0 register is set to 0.) • Set the ADST bit to 0.
Interrupt request generation timing	When A/D conversion completes.
Analog input pin	One pin is selectable from among AN0 to AN19 or OCVREF.
Storage resisters for A/D conversion result	AD0 register: AN0, AN8, AN16, OCVREF AD1 register: AN1, AN9, AN17 AD2 register: AN2, AN10, AN18 AD3 register: AN3, AN11, AN19 AD4 register: AN4, AN12 AD5 register: AN5, AN13 AD6 register: AN6, AN14 AD7 register: AN7, AN15
Reading of A/D conversion result	Read the register among AD0 to AD7 corresponding to the selected pin.

30.5 Repeat Mode 0

In repeat mode 0, the input voltage to one pin selected from among AN0 to AN19 or OCVREF is A/D converted repeatedly.
Table 30.5 lists the Repeat Mode 0 Specifications.

Table 30.5 Repeat Mode 0 Specifications

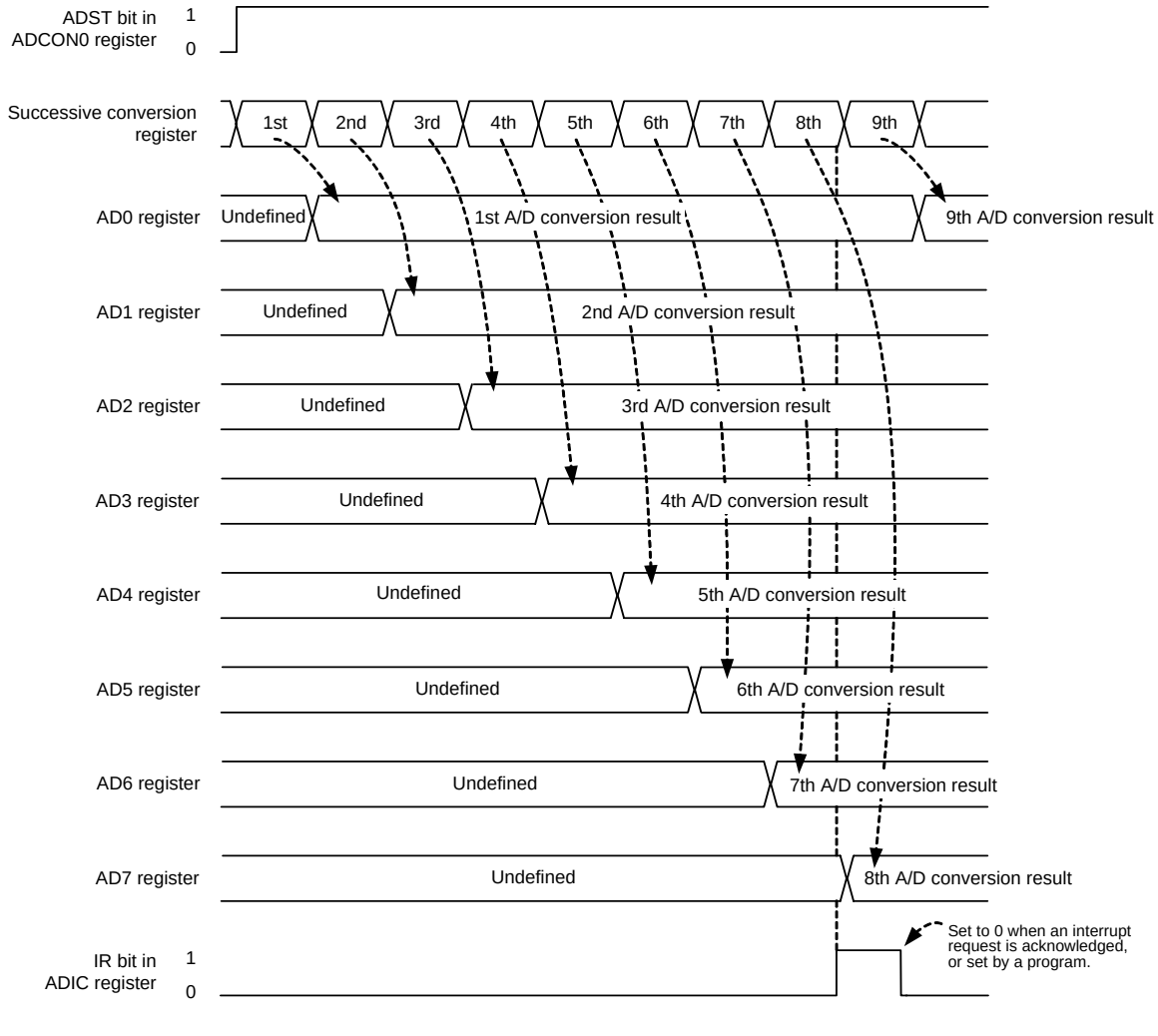
Item	Specification
Function	The input voltage to the pin selected by bits CH2 to CH0 and bits ADGSEL1 to ADGSEL0 in the ADINSEL register or the ADEX0 bit in the ADCON1 register is A/D converted repeatedly.
Resolution	8 bits or 10 bits selectable
A/D conversion start conditions	• Software trigger • Timer RD • Timer RC • External trigger (Refer to **30.3.3 A/D Conversion Start Conditions)**
A/D conversion stop conditions	Set the ADST bit in the ADCON0 register to 0
Interrupt request generation timing	Not generated
Analog input pin	One pin is selectable from among AN0 to AN19 or OCVREF.
Storage resisters for A/D conversion result	AD0 register: AN0, AN8, AN16, OCVREF AD1 register: AN1, AN9, AN17 AD2 register: AN2, AN10, AN18 AD3 register: AN3, AN11, AN19 AD4 register: AN4, AN12 AD5 register: AN5, AN13 AD6 register: AN6, AN14 AD7 register: AN7, AN15
Reading of A/D conversion result	Read the register among AD0 to AD7 corresponding to the selected pin.

30.6 Repeat Mode 1

In repeat mode 1, the input voltage to one pin selected from among AN0 to AN19 or OCVREF is A/D converted repeatedly.
Table 30.6 lists the Repeat Mode 1 Specifications. Figure 30.7 shows an Operating Example in Repeat Mode 1.

Table 30.6 Repeat Mode 1 Specifications

Item	Specification
Function	The input voltage to the pin selected by bits CH2 to CH0 and bits ADGSEL1 to ADGSEL0 in the ADINSEL register or the ADEX0 bit in the ADCON1 register is A/D converted repeatedly.
Resolution	8 bits or 10 bits selectable
A/D conversion start conditions	• Software trigger • Timer RD • Timer RC • External trigger (Refer to **30.3.3 A/D Conversion Start Conditions)**
A/D conversion stop condition	Set the ADST bit in the ADCON0 register to 0.
Interrupt request generation timing	When the A/D conversion result is stored in the AD7 register.
Analog input pin	One pin is selectable from among AN0 to AN19 or OCVREF.
Storage resisters for A/D conversion result	AD0 register: 1st A/D conversion result, 9th A/D conversion result... AD1 register: 2nd A/D conversion result, 10th A/D conversion result... AD2 register: 3rd A/D conversion result, 11th A/D conversion result... AD3 register: 4th A/D conversion result, 12th A/D conversion result... AD4 register: 5th A/D conversion result, 13th A/D conversion result... AD5 register: 6th A/D conversion result, 14th A/D conversion result... AD6 register: 7th A/D conversion result, 15th A/D conversion result... AD7 register: 8th A/D conversion result, 16th A/D conversion result...
Reading of A/D conversion result	Read registers AD0 to AD7.



The above applies under the following condition:
Bits ADCAP1 to ADCAP0 in the ADMOD register are set to 00b (A/D conversion starts by software trigger).

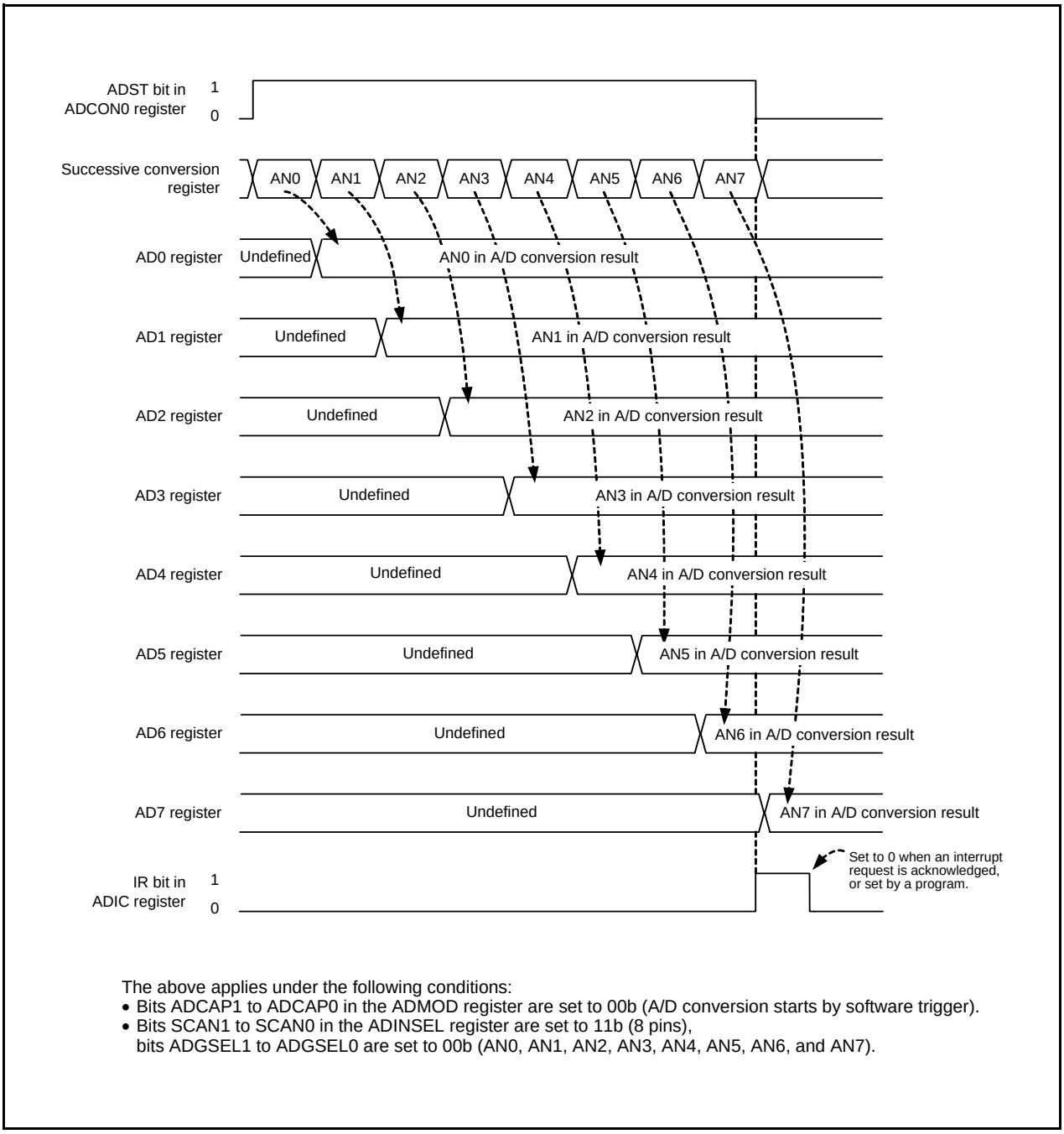
Figure 30.7 Operating Example in Repeat Mode 1

30.7 Single Sweep Mode

In single sweep mode, the input voltage to two, four, six, or eight pins selected from among AN0 to AN19 are A/D converted one-by-one.
Table 30.7 lists the Single Sweep Mode Specifications. Figure 30.8 shows an Operating Example in Single Sweep Mode.

Table 30.7 Single Sweep Mode Specifications

Item	Specification
Function	The input voltage to the pin selected by bits CH2 to CH0 and bits ADGSEL1 to ADGSEL0 in the ADINSEL register or the ADEX0 bit in the ADCON1 register is A/D converted one-by-one.
Resolution	8 bits or 10 bits selectable
A/D conversion start conditions	• Software trigger • Timer RD • Timer RC • External trigger (Refer to **30.3.3 A/D Conversion Start Conditions)**
A/D conversion stop conditions	• If 2 pins are selected, when A/D conversion of the 2 selected pins completes. (The ADST bit in the ADCON0 register is set to 0.) • If 4 pins are selected, when A/D conversion of the 4 selected pins completes. (The ADST bit is set to 0.) • If 6 pins are selected, when A/D conversion of the 6 selected pins completes. (The ADST bit is set to 0.) • If 8 pins are selected, when A/D conversion of the 8 selected pins completes. (The ADST bit is set to 0.) • Set the ADST bit to 0.
Interrupt request generation timing	• If 2 pins are selected, when A/D conversion of the 2 selected pins completes. • If 4 pins are selected, when A/D conversion of the 4 selected pins completes. • If 6 pins are selected, when A/D conversion of the 6 selected pins completes. • If 8 pins are selected, when A/D conversion of the 8 selected pins completes.
Analog input pins	AN0 and AN1 (2 pins), AN8 and AN9 (2 pins), AN16 and AN17 (2 pins) AN0 to AN3 (4 pins), AN8 to AN11 (4 pins), AN16 to AN19 (4 pins), AN0 to AN5 (6 pins), AN8 to AN13 (6 pins), AN0 to AN7 (8 pins), AN8 to AN15 (8 pins), (Selectable by bits SCAN1 to SCAN0 and bits ADGSEL1 to ADGSEL0.)
Storage resisters for A/D conversion result	AD0 register: AN0, AN8, AN16, OCVREF AD1 register: AN1, AN9, AN17 AD2 register: AN2, AN10, AN18 AD3 register: AN3, AN11, AN19 AD4 register: AN4, AN12 AD5 register: AN5, AN13 AD6 register: AN6, AN14 AD7 register: AN7, AN15
Reading of A/D conversion result	Read the register among AD0 to AD7 corresponding to the selected pin.



The above applies under the following conditions:
- Bits ADCAP1 to ADCAP0 in the ADMOD register are set to 00b (A/D conversion starts by software trigger).
- Bits SCAN1 to SCAN0 in the ADINSEL register are set to 11b (8 pins), bits ADGSEL1 to ADGSEL0 are set to 00b (AN0, AN1, AN2, AN3, AN4, AN5, AN6, and AN7).

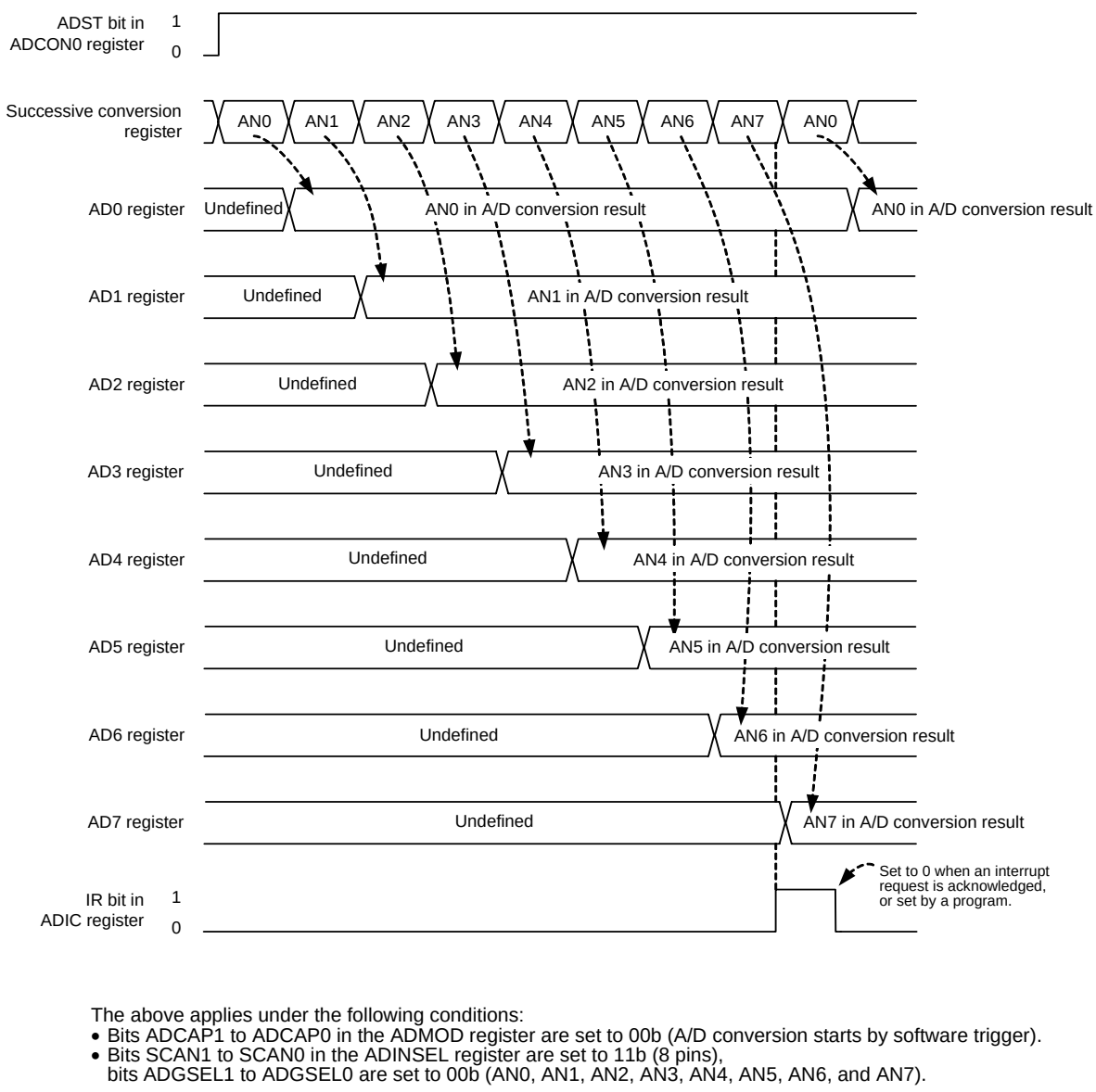
Figure 30.8 Operating Example in Single Sweep Mode

30.8 Repeat Sweep Mode

In repeat sweep mode, the input voltage to two, four, six, or eight pins selected from among AN0 to AN19 are A/D converted repeatedly.
Table 30.8 lists the Repeat Sweep Mode Specifications. Figure 30.9 shows an Operating Example in Repeat Sweep Mode.

Table 30.8 Repeat Sweep Mode Specifications

Item	Specification
Function	The input voltage to the pin selected by bits CH2 to CH0 and bits ADGSEL1 to ADGSEL0 in the ADINSEL register or the ADEX0 bit in the ADCON1 register is A/D converted repeatedly.
Resolution	8 bits or 10 bits selectable
A/D conversion start conditions	• Software trigger • Timer RD • Timer RC • External trigger (Refer to **30.3.3 A/D Conversion Start Conditions)**
A/D conversion stop condition	Set the ADST bit in the ADCON0 register to 0
Interrupt request generation timing	• If 2 pins are selected, when A/D conversion of the 2 selected pins completes. • If 4 pins are selected, when A/D conversion of the 4 selected pins completes. • If 6 pins are selected, when A/D conversion of the 6 selected pins completes. • If 8 pins are selected, when A/D conversion of the 8 selected pins completes.
Analog input pins	AN0 and AN1 (2 pins), AN8 and AN9 (2 pins), AN16 and AN17 (2 pins) AN0 to AN3 (4 pins), AN8 to AN11 (4 pins), AN16 to AN19 (4 pins), AN0 to AN5 (6 pins), AN8 to AN13 (6 pins), AN0 to AN7 (8 pins), AN8 to AN15 (8 pins), (Selectable by bits SCAN1 to SCAN0 and bits ADGSEL1 to ADGSEL0.)
Storage resisters for A/D conversion result	AD0 register: AN0, AN8, AN16, OCVREF AD1 register: AN1, AN9, AN17 AD2 register: AN2, AN10, AN18 AD3 register: AN3, AN11, AN19 AD4 register: AN4, AN12 AD5 register: AN5, AN13 AD6 register: AN6, AN14 AD7 register: AN7, AN15
Reading of A/D conversion result	Read the register among AD0 to AD7 corresponding to the selected pin.

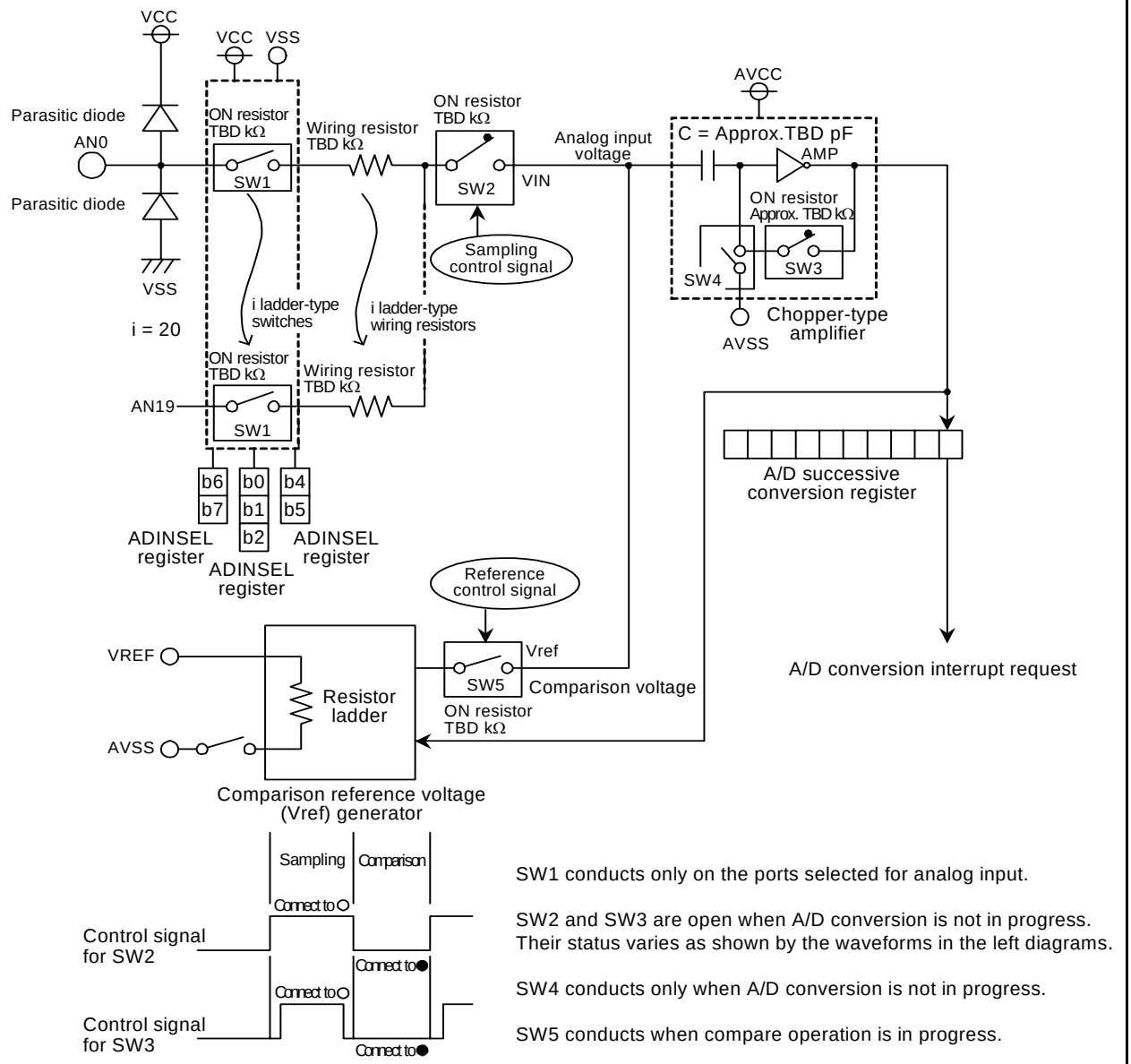


The above applies under the following conditions:
- Bits ADCAP1 to ADCAP0 in the ADMOD register are set to 00b (A/D conversion starts by software trigger).
- Bits SCAN1 to SCAN0 in the ADINSEL register are set to 11b (8 pins), bits ADGSEL1 to ADGSEL0 are set to 00b (AN0, AN1, AN2, AN3, AN4, AN5, AN6, and AN7).

Figure 30.9 Operating Example in Repeat Sweep Mode

30.9 Internal Equivalent Circuit of Analog Input

Figure 30.10 shows the Internal Equivalent Circuit of Analog Input.



Note:
1. Use only as a standard for designing this data.
   Mass production may cause some changes in device characteristics.

Figure 30.10 Internal Equivalent Circuit of Analog Input

30.10 Output Impedance of Sensor during A/D Conversion

To carry out A/D conversion properly, charging the internal capacitor C in Figure 30.11 has to be completed within the period specified as the sampling time T. Let the output impedance of the sensor equivalent circuit be R0, the internal resistance of the MCU be R, the precision (error) of the A/D converter be X, and the resolution of the A/D converter be Y (Y is 1024 in 10-bit mode, and 256 in 8-bit mode).

VC is generally $VC = VIN\left\{1 - e^{-\frac{1}{C(R0+R)}t}\right\}$

And when t = T, $VC = VIN - \frac{X}{Y}VIN = VIN\left(1 - \frac{X}{Y}\right)$

$$e^{-\frac{1}{C(R0+R)}T} = \frac{X}{Y}$$

$$-\frac{1}{C(R0+R)}T = \ln\frac{X}{Y}$$

Hence, $$R0 = -\frac{T}{C \bullet \ln\frac{X}{Y}} - R$$

Figure 30.11 shows an example of Analog Input Pin and External Sensor Equivalent Circuit.
When the difference between VIN and VC becomes 0.1 LSB, the impedance R0 can be obtained if the voltage between pins VC changes from 0 to VIN-(0.1/1024) VIN in the time T. (0.1/1024) means that the drop in A/D precision, due to insufficient capacitor charge, is limited to 0.1 LSB during A/D conversion in 10-bit mode. Actual error, however, is the value of absolute precision added to 0.1 LSB.
T = TBD µs when f(ϕAD) = TBD MHz. The output impedance R0 allowing sufficient charging of the capacitor C within the time T is determined as follows:

T = TBD µs, R = TBD kΩ, C = TBD pF, X = 0.1, and Y = 1024. Hence,

$$R0 = -\frac{TBD}{TBD \bullet \ln\frac{0.1}{1024}} - TBD \approx TBD$$

Thus, the allowable output impedance R0 of the sensor equivalent circuit, resulting in a precision (error) of 0.1 LSB or less, is approximately TBD kΩ maximum.

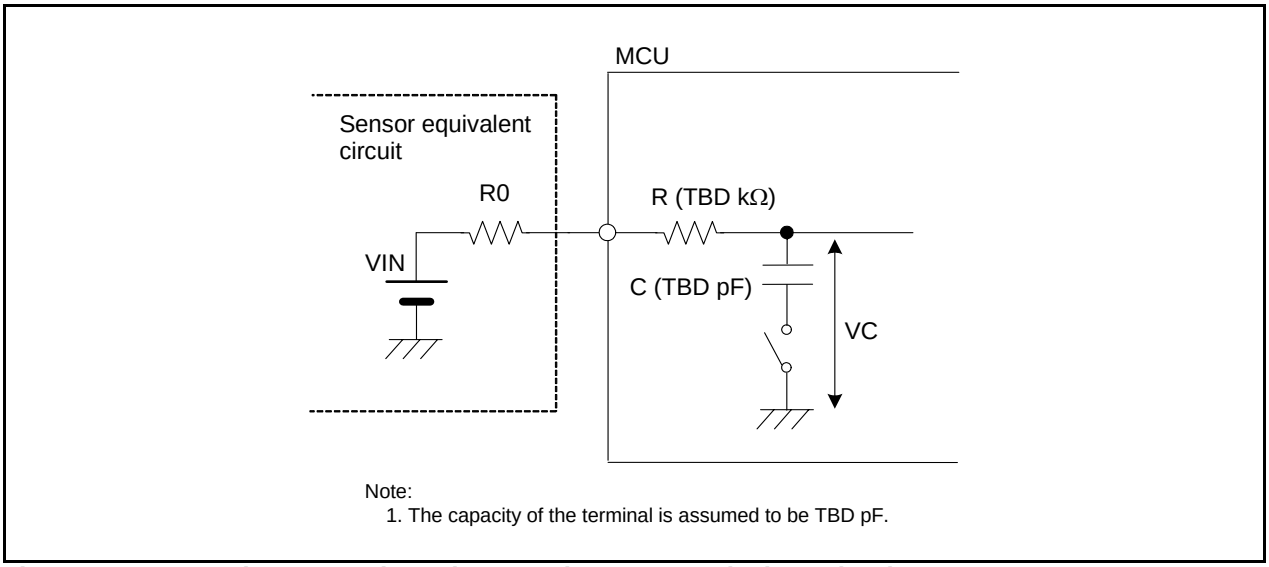


Figure 30.11 Analog Input Pin and External Sensor Equivalent Circuit

30.11 Notes on A/D Converter

- Write to the ADMOD, ADINSEL, ADCON0 (other than the ADST bit), ADCON1, or OCVREFCR register must be performed while A/D conversion is stopped (before a trigger occurs).
- To use the A/D converter in repeat mode 0, repeat mode 1, or repeat sweep mode, select the frequency of the A/D converter operating clock ϕAD or more for the CPU clock during A/D conversion.
  Do not select fOCO-F as ϕAD.
- Connect 0.1 µF capacitor between pins VREF and AVSS.
- Do not enter stop mode during A/D conversion.
- Do not enter wait mode during A/D conversion regardless of the state of the CM02 bit in the CM0 register (1: Peripheral function clock stops in wait mode or 0: Peripheral function clock does not stop in wait mode).
- Do not set the FMSTP bit in the FMR0 register to 1 (flash memory stops) during A/D conversion.

31. D/A Converter

The D/A converters are 8-bit R-2R type units. There are two independent D/A converters.

31.1 Introduction

D/A conversion is performed by writing a value to the DAi register (i = 0 or 1). To output the conversion result, set the DAiE bit in the DACON register to 1 (output enabled). Before using D/A conversion, set the corresponding bits PD13_0 and PD13_1 in the PD13 register to 0 (input mode).
The output analog voltage (V) is determined by the setting value n (n: decimal) of the DAi register.

$$V = Vref \times n / 256 \quad (n = 0 \text{ to } 255)$$

Vref: Reference voltage

Table 31.1 lists the D/A Converter Specifications. Figure 31.1 shows the D/A Converter Block Diagram and Figure 31.2 shows the D/A Converter Equivalent Circuit.

Table 31.1 D/A Converter Specifications

Item	Performance
D/A conversion method	R-2R method
Resolution	8 bits
Analog output pins	2 (DA0 and DA1)

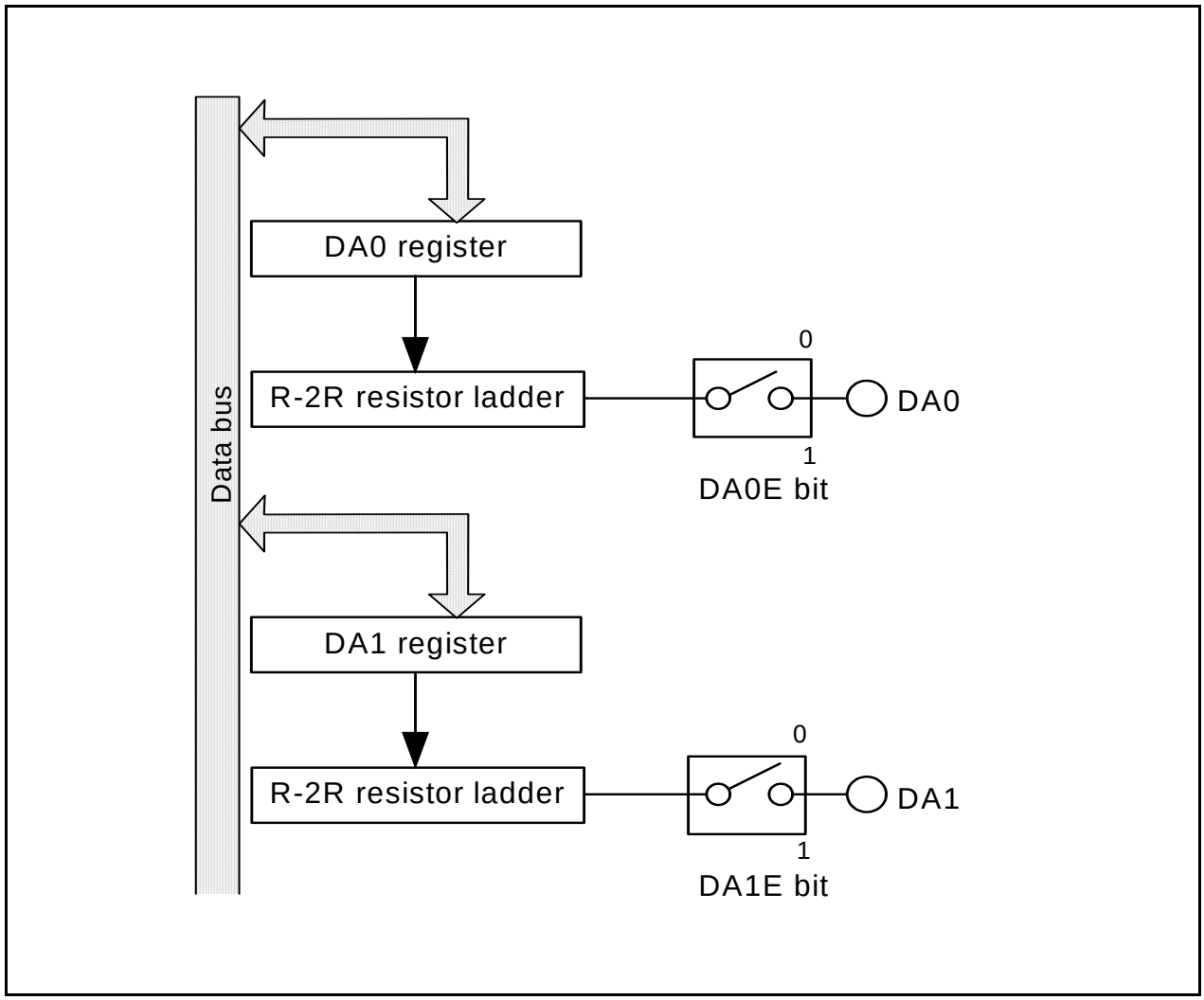


Figure 31.1 D/A Converter Block Diagram

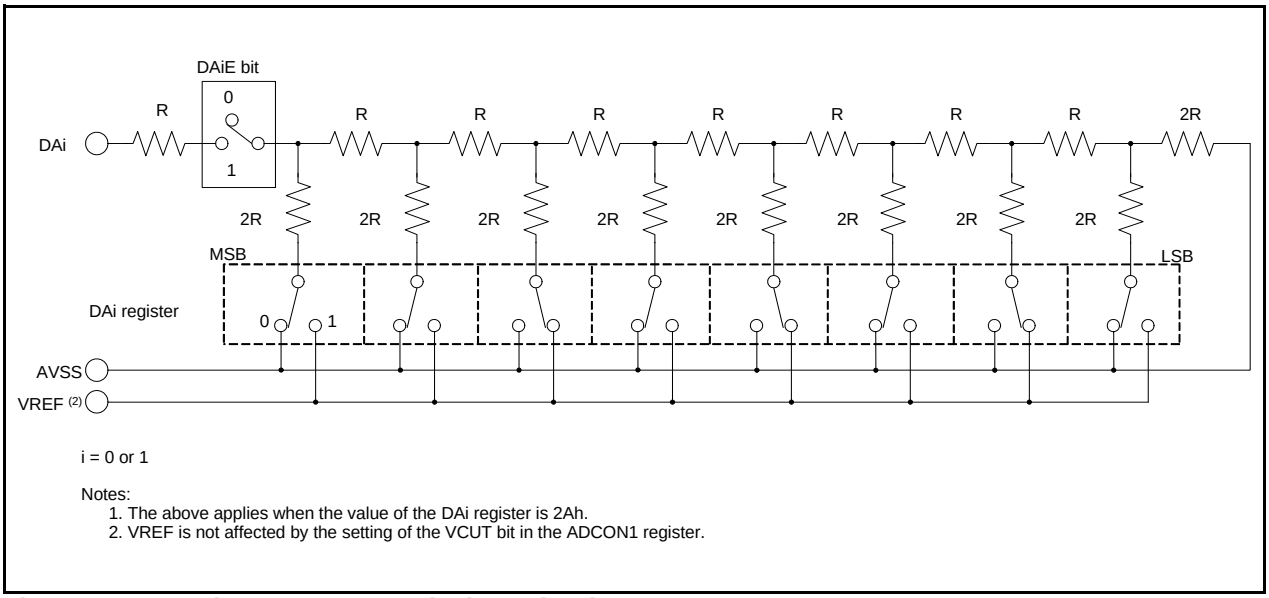


Figure 31.2 D/A Converter Equivalent Circuit

31.2 Registers

31.2.1 D/Ai Register (DAi) (i = 0 or 1)

Address 00D8h (DA0), 00D9h (DA1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b7-b0	Output value of D/A conversion	00h to FFh	R/W

When the D/A converter is not used, set the DAiE bit (i = 0 or 1) to 0 (output disabled) and set the DAi register to 00h to prevent current from flowing into the R-2R resistor ladder to reduce unnecessary current consumption.

31.2.2 D/A Control Register (DACON)

Address 00DCh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	DA1E	DA0E
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DA0E	D/A0 output enable bit	0: Output disabled 1: Output enabled	R/W
b1	DA1E	D/A1 output enable bit	0: Output disabled 1: Output enabled	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

When the D/A converter is not used, set the DAiE bit (i = 0 or 1) to 0 (output disabled) and set the DAi register to 00h to prevent current from flowing into the R-2R resistor ladder to reduce unnecessary current consumption.

32. Comparator A

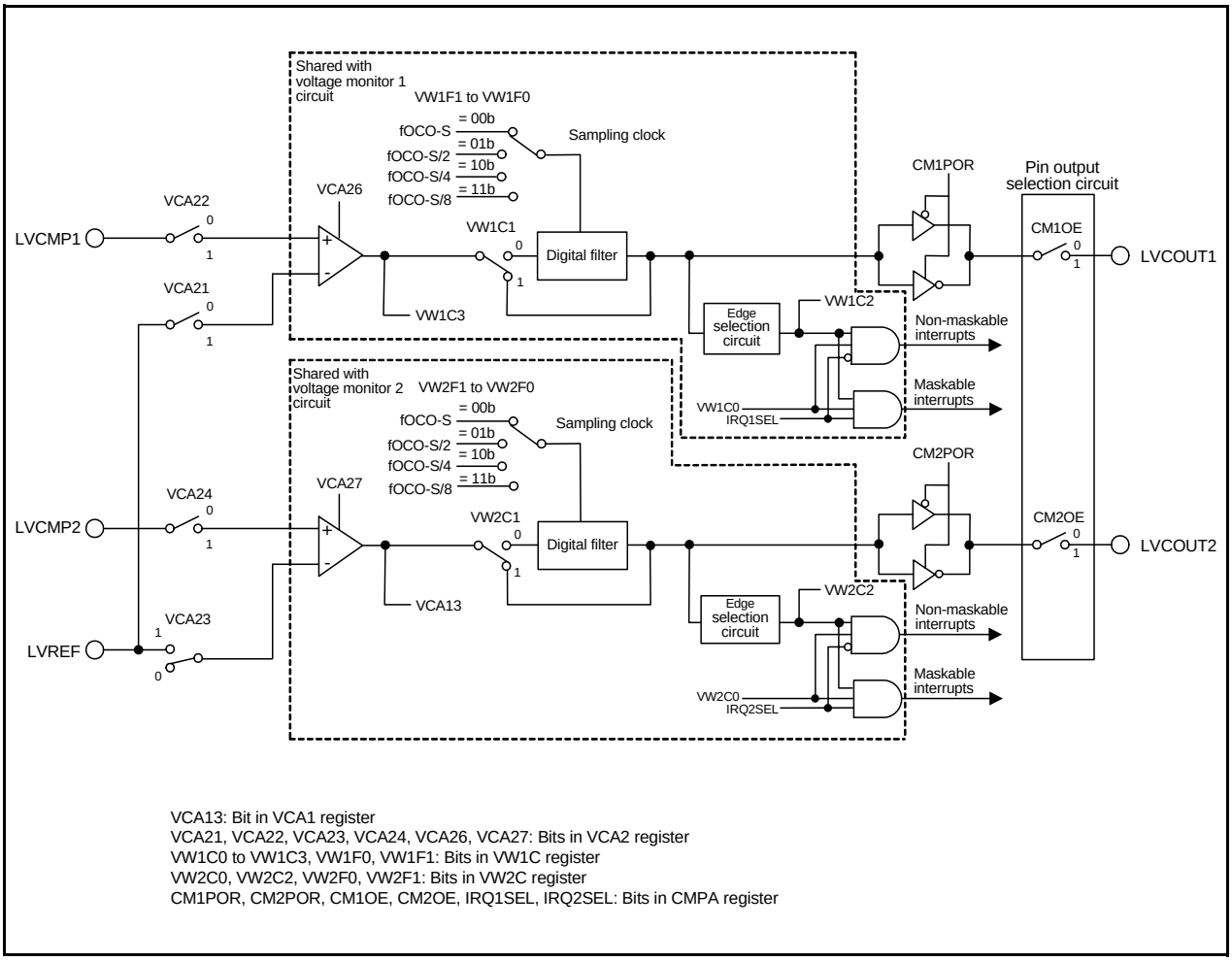
Comparator A compares a reference input voltage and an analog input voltage. Comparator A1 and comparator A2 are independent of each other. Note that these comparators share the voltage detection circuit with voltage monitor 1 and voltage monitor 2. Either comparator A1 and comparator A2 or voltage monitor 1 and voltage monitor 2 can be selected to use the voltage detection circuit.

32.1 Introduction

The comparison result of the reference input voltage and analog input voltage can be read by software. The result also can be output from the VCOUTi (i = 1 or 2) pin. An input voltage to the LVREF pin can be selected as the reference input voltage. Also, the comparator A1 interrupt and comparator A2 interrupt can be used.
Table 32.1 lists the Comparator A Specifications, Figure 32.1 shows the Comparator A Block Diagram, and Table 32.2 lists the Comparator A Pin Configuration.

Table 32.1 Comparator A Specifications

Item		Comparator A1	Comparator A2
Analog input voltage		Input voltage to the LVCMP1 pin	Input voltage to the LVCMP2 pin
Reference input voltage		Input voltage to the LVREF pin	
Comparison target		Whether passing thorough the reference input voltage by rising or falling.	
Comparison result monitor		The VW1C3 bit in the VW1C register	The VCA13 bit in the VCA1 register
		Whether higher or lower than the reference input voltage.	
Interrupt		Comparator A1 interrupt (non-makable or maskable selectable)	Comparator A2 interrupt (non-makable or maskable selectable)
		Interrupt request at: Reference input voltage > input voltage to the LVCMP1 pin and/or Input voltage to the LVCMP1 pin > reference input voltage	Interrupt request at: Reference input voltage > input voltage to the LVCMP2 pin and/or Input voltage to the LVCMP2 pin > reference input voltage
Digital Filter	Switching enable/disable	Supported	
	Sampling time	(fOCO-S divided by n) × 2 n: 1, 2, 4, and 8	
Comparison result output		Output from the LVCOUT1 pin (Whether the comparison result output is inverted or not can be selected.)	Output from the LVCOUT2 pin (Whether the comparison result output is inverted or not can be selected.)



VCA13: Bit in VCA1 register
VCA21, VCA22, VCA23, VCA24, VCA26, VCA27: Bits in VCA2 register
VW1C0 to VW1C3, VW1F0, VW1F1: Bits in VW1C register
VW2C0, VW2C2, VW2F0, VW2F1: Bits in VW2C register
CM1POR, CM2POR, CM1OE, CM2OE, IRQ1SEL, IRQ2SEL: Bits in CMPA register

Figure 32.1 Comparator A Block Diagram

Table 32.2 Comparator A Pin Configuration

Pin Name	I/O	Function
LVCMP1	Input	Comparator A1 analog pin
LVCOUT1	Output	Comparator A1 comparison result output pin
LVCMP2	Input	Comparator A2 analog pin
LVCOUT2	Output	Comparator A2 comparison result output pin
LVREF	Input	Comparator reference voltage pin

32.2 Registers

32.2.1 Voltage Monitor Circuit/Comparator A Control Register (CMPA)

Address 0030h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	COMPSEL	—	IRQ2SEL	IRQ1SEL	CM2OE	CM1OE	CM2POR	CM1POR
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CM1POR	LVCOUT1 output polarity select bit	0: Non-inverted comparator A1 comparison result is output to LVCOUT1. 1: Inverted comparator A1 comparison result is output to LVCOUT1.	R/W
b1	CM2POR	LVCOUT2 output polarity select bit	0: Non-inverted Comparator A2 comparison result is output to LVCOUT2. 1: Inverted comparator A2 comparison result is output to LVCOUT2.	R/W
b2	CM1OE	LVCOUT1 output enable bit	0: Output disabled 1: Output enabled	R/W
b3	CM2OE	LVCOUT2 output enable bit	0: Output disabled 1: Output enabled	R/W
b4	IRQ1SEL	Voltage monitor 1/comparator A1 interrupt type select bit	0: Non-maskable interrupt 1: Maskable interrupt	R/W
b5	IRQ2SEL	Voltage monitor 2/comparator A2 interrupt type select bit	0: Non-maskable interrupt 1: Maskable interrupt	R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	COMPSEL	Voltage monitor/comparator A interrupt type selection enable bit	0: Bits IRQ1SEL and IRQ2SEL disabled 1: Bits IRQ1SEL and IRQ2SEL enabled	R/W

32.2.2 Voltage Monitor Circuit Edge Select Register (VCAC)

Address 0031h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	VCAC2	VCAC1	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	VCAC1	Comparator A1 circuit edge select bit (1)	0: One edge 1: Both edges	R/W
b2	VCAC2	Comparator A2 circuit edge select bit (2)	0: One edge 1: Both edges	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Notes:
1. When the VCA1 bit is set to 0 (one edge), the VW1C7 bit in the VW1C register is enabled. Set the VW1C7 bit after setting the VCAC1 bit to 0.
2. When the VCA2 bit is set to 0 (one edge), the VW2C7 bit in the VW2C register is enabled. Set the VW2C7 bit after setting the VCAC2 bit to 0.

32.2.3 Voltage Detect Register 1 (VCA1)

Address 0033h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	VCA13	—	—	—
After Reset	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	VCA13	Comparator A2 signal monitor flag (1)	0: LVCMP2 < reference voltage 1: LVCMP2 ≥ reference voltage or comparator A2 circuit disabled	R
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

Note:
1. When the VCA27 bit in the VCA2 register is set to 1 (comparator A2 circuit enabled), the VCA13 bit is enabled. When the VCA27 bit in the VCA2 register is set to 0 (comparator A2 circuit disabled), the VCA13 bit is set to 1 (VCMP2 ≥ reference voltage).

32.2.4 Voltage Detect Register 2 (VCA2)

Address 0034h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VCA27	VCA26	VCA25	VCA24	VCA23	VCA22	VCA21	VCA20
After Reset	The LVDAS bit in the OFS register is set to 1.							
	0	0	0	0	0	0	0	0
After Reset	The LVDAS bit in the OFS register is set to 0.							
	0	0	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	VCA20	Internal power low consumption enable bit (1)	0: Low consumption disabled 1: Low consumption enabled (2)	R/W
b1	VCA21	Comparator A1 reference voltage input select bit	0: Internal reference voltage 1: LVREF pin input voltage	R/W
b2	VCA22	LVCMP1 comparison voltage external input select bit	0: Supply voltage (VCC) 1: LVCMP1 pin input voltage	R/W
b3	VCA23	Comparator A2 reference voltage input select bit	0: Internal reference voltage 1: LVREF pin input voltage	R/W
b4	VCA24	LVCMP2 comparison voltage external input select bit	0: Supply voltage (VCC) (Vdet2_0) 1: LVCMP2 pin input voltage (Vdet2_EXT)	R/W
b5	VCA25	Voltage detection 0 enable bit (3)	0: Voltage detection 0 circuit disabled 1: Voltage detection 0 circuit enabled	R/W
b6	VCA26	Voltage detection 1/comparator A1 enable bit (4)	0: Voltage detection 1/comparator A1 circuit disabled 1: Voltage detection 1/comparator A1 circuit enabled	R/W
b7	VCA27	Voltage detection 2/comparator A2 enable bit (5)	0: Voltage detection 2/comparator A2 circuit disabled 1: Voltage detection 2/comparator A2 circuit enabled	R/W

Notes:
1. Use the VCA20 bit only when the MCU enters wait mode. To set the VCA20 bit, follow the procedure shown in **Figure 10.7 Handling Procedure for Reducing Internal Power Consumption Using VCA20 Bit**.
2. When the VCA20 bit is set to 1 (low consumption enabled), do not set the CM10 bit in the CM1 register to 1 (stop mode).
3. To use voltage monitor 0 reset, set the VCA25 bit to 1.
   After the VCA25 bit is set to 1 from 0, allow td(E-A) to elapse before the voltage detection circuit starts operation.
4. To use the voltage detection 1/comparator A1 interrupt or the VW1C3 bit in the VW1C register, set the VCA26 bit to 1.
   After the VCA26 bit is set to 1 from 0, allow td(E-A) to elapse before the voltage detection 1/comparator A1 circuit starts operation.
5. To use the voltage detection 2/comparator A2 interrupt or the VCAC13 bit in the VCA1 register, set the VCA27 bit to 1.
   After the VCA27 bit is set to 1 from 0, allow td(E-A) to elapse before the voltage detection 2/comparator A2 circuit starts operation.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VCA2 register.

32.2.5 Voltage Monitor 1 Circuit Control Register (VW1C)

Address 0039h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VW1C7	—	VW1F1	VW1F0	VW1C3	VW1C2	VW1C1	VW1C0
After Reset	1	0	0	0	1	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	VW1C0	Comparator A1 interrupt enable bit (1)	0: Disabled 1: Enabled	R/W
b1	VW1C1	Comparator A1 digital filter disable mode select bit (2)	0: Digital filter enable mode (digital filter circuit enabled) 1: Digital filter disable mode (digital filter circuit disabled)	R/W
b2	VW1C2	Comparator A1 interrupt flag (3, 4)	[Condition for setting to 0] 0 is written. [Condition for setting to 1] When an interrupt request is generated.	R/W
b3	VW1C3	Comparator A1 signal monitor flag (3)	0: LVCMP1 < reference voltage 1: LVCMP1 ≥ reference voltage or comparator A1 circuit disabled	R
b4	VW1F0	Sampling clock select bit	b5 b4 0 0: fOCO-S divided by 1 0 1: fOCO-S divided by 2 1 0: fOCO-S divided by 4 1 1: fOCO-S divided by 8	R/W
b5	VW1F1			R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	VW1C7	Comparator A1 interrupt generation condition select bit (5)	0: When LVCMP1 reaches reference voltage or above. 1: When LVCMP1 reaches reference voltage or below.	R/W

Notes:
1. The VW1C0 is enabled when the VCA26 bit in the VCA2 register is set to 1 (comparator A1 circuit enabled). Set the VW1C0 bit to 0 (disabled) when the VCA26 bit is set to 0 (comparator A1 circuit disabled). To set the VW1C0 bit to 1 (enabled), follow the procedure shown in **Table 32.3 Procedure for Setting Bits Associated with Comparator A1 Interrupt**.
2. To use the comparator A1 interrupt to exit stop mode and to return again, write 0 and then 1 to the VW1C1 bit.
3. Bits VW1C2 and VW1C3 are enabled when the VCA26 bit in the VCA2 register is set to 1 (comparator A1 circuit enabled).
4. Set the VW1C2 bit to 0 by a program. When 0 is written by a program, this bit is set to 0 (and remains unchanged even if 1 is written to it).
5. The VW1C7 bit is enabled when the VCAC1 bit in the VCAC register is set to 0 (one edge). After setting the VCAC1 bit to 0, set the VW1C7 bit.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VW1C register.
Rewriting the VW1C register may set the VW1C2 bit to 1. After rewriting this register, set the VW1C2 bit to 0.

32.2.6 Voltage Monitor 2 Circuit Control Register (VW2C)

Address 003Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VW2C7	VW2C6	VW2F1	VW2F0	VW2C3	VW2C2	VW2C1	VW2C0
After Reset	1	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	VW2C0	Comparator A2 interrupt enable bit (1)	0: Disabled 1: Enabled	R/W
b1	VW2C1	Comparator A2 digital filter disable mode select bit (2)	0: Digital filter enable mode (digital filter circuit enabled) 1: Digital filter disable mode (digital filter circuit disabled)	R/W
b2	VW2C2	Comparator A2 interrupt flag (3, 4)	[Condition for setting to 0] 0 is written. [Condition for setting to 1] When an interrupt request is generated.	R/W
b3	VW2C3	WDT detection monitor flag (4)	0: Not detected 1: Detected	R/W
b4	VW2F0	Sampling clock select bit	b5 b4 0 0: fOCO-S divided by 1 0 1: fOCO-S divided by 2 1 0: fOCO-S divided by 4 1 1: fOCO-S divided by 8	R/W
b5	VW2F1			R/W
b6	VW2C6	Reserved bit	Set to 0.	R/W
b7	VW2C7	Comparator A2 interrupt generation condition select bit (5)	0: When LVCMP2 reaches reference voltage or above. 1: When LVCMP2 reaches reference voltage or below.	R/W

Notes:
1. The VW2C0 is enabled when the VCA27 bit in the VCA2 register is set to 1 (comparator A2 circuit enabled). Set the VW2C0 bit to 0 (disabled) when the VCA27 bit is set to 0 (comparator A2 circuit disabled). To set the VW1C0 bit to 1 (enabled), follow the procedure shown in **Table 32.4 Procedure for Setting Bits Associated Comparator A2 Interrupt**.
2. To use the comparator A2 interrupt to exit stop mode and to return again, write 0 and then 1 to the VW2C1 bit.
3. The VW2C2 bit is enabled when the VCA27 bit in the VCA2 register is set to 1 (comparator A2 circuit enabled).
4. Set this bit to 0 by a program. When 0 is written by a program, this bit is set to 0 (and remains unchanged even if 1 is written to it).
5. The VW2C7 bit is enabled when the VCAC2 bit in the VCAC register is set to 0 (one edge). After setting the VCAC2 bit to 0, set the VW2C7 bit.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VW2C register.
Rewriting the VW2C register may set the VW2C2 bit to 1. After rewriting this register, set the VW2C2 bit to 0.

32.3 Monitoring Comparison Results

32.3.1 Monitoring Comparator A1

Once the following settings are made, the comparison result of comparator A1 can be monitored by the VW1C3 bit in the VW1C register after td(E-A) has elapsed (refer to **36. Electrical Characteristics**).

(1) Set the VCA21 bit in the VCA2 register to 1 (LVREF pin input voltage).
(2) Set the VCA22 bit in the VCA2 register to 1 (LVCMP1 pin input voltage).
(3) Set the VCA26 bit in the VCA2 register to 1 (comparator A1 circuit enabled).

32.3.2 Monitoring Comparator A2

Once the following settings are made, the comparison result of comparator A2 can be monitored by the VCA13 bit in the VCA1 register after td(E-A) has elapsed (refer to **36. Electrical Characteristics**).

(1) Set the VCA23 bit in the VCA2 register to 1 (LVREF pin input voltage).
(2) Set the VCA24 bit in the VCA2 register to 1 (LVCMP2 pin input voltage).
(3) Set the VCA27 bit in the VCA2 register to 1 (comparator A2 circuit enabled).

32.4 Functional Description

Comparator A1 and comparator A2 operate independently.
The comparison result of the reference input voltage and analog input voltage can be read by software. The result can also be output from the LVCOUTi (i = 1 or 2) pin. An input voltage to the LVREF pin can be used as the reference input voltage. The comparator A1 interrupt or the comparator A2 interrupt can be used by selecting non-maskable or maskable for each interrupt type.

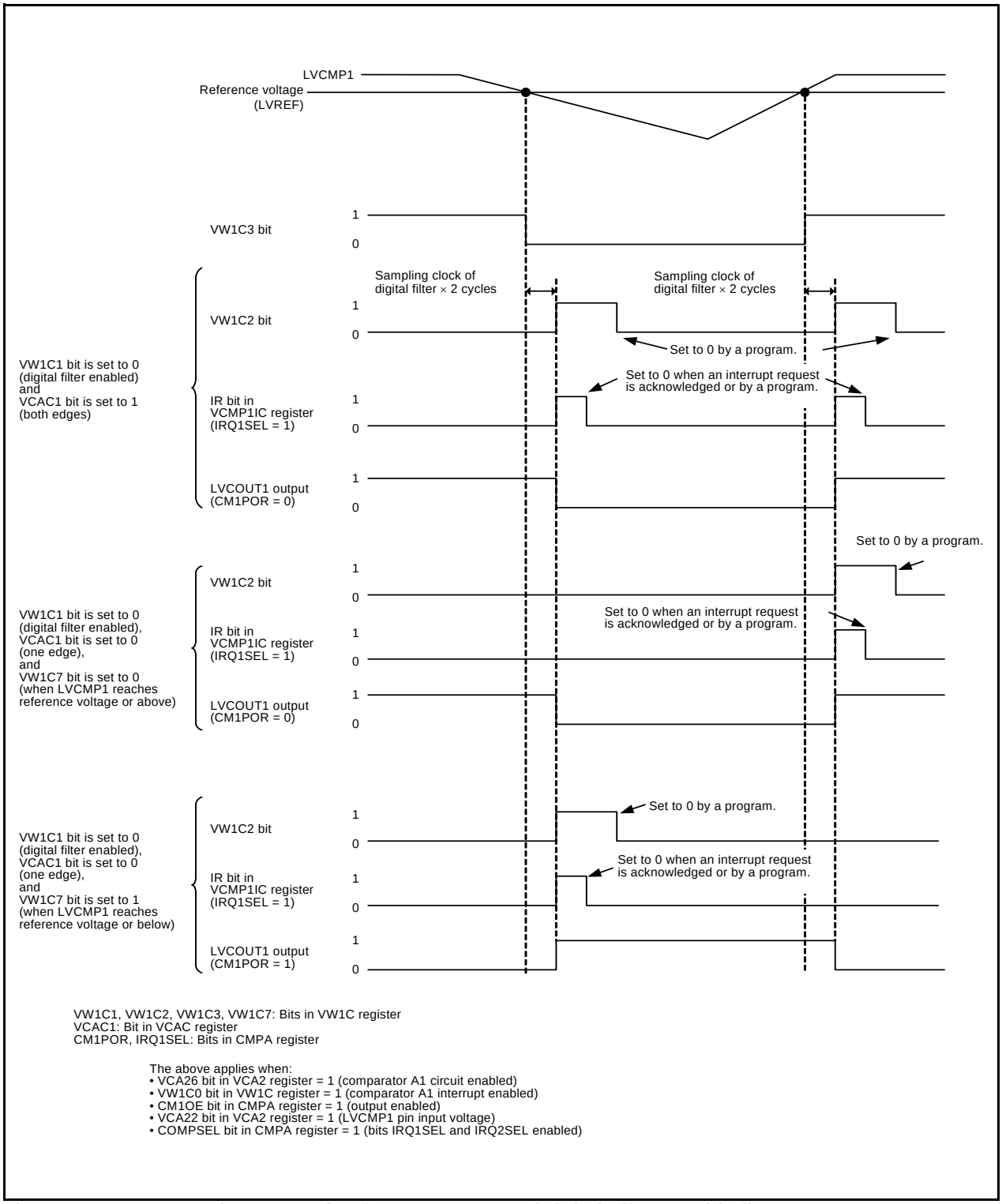
32.4.1 Comparator A1

Table 32.3 lists the Procedure for Setting Bits Associated with Comparator A1 Interrupt, Figure 32.2 shows an Operating Example of Comparator A1 (Digital Filter Enabled), and Figure 32.3 shows an Operating Example of Comparator A1 (Digital Filter Disabled).

Table 32.3 Procedure for Setting Bits Associated with Comparator A1 Interrupt

Step	When Using Digital Filter	When Using No Digital Filter
1	Set the COMPSEL bit in the CMPA register to 1 (bits IRQ1SEL and IRQ2SEL enabled).	
2	Set the VCA21 bit in the VCA2 register to 1 (LVREF pin input voltage) and the VCA22 bit to 1 (LVCMP1 pin input voltage).	
3	Set the VCA26 bit in the VCA2 register to 1 (comparator A1 circuit enabled).	
4	Wait for td(E-A).	
5	Select the interrupt type by the IRQ1SEL bit in the CMPA register.	
6	Select the sampling clock of the digital filter by bits VW1F0 and VW1F1 in the VW1C register.	Set the VW1C1 bit in the VW1C register to 1 (digital filter disabled).
7 (1)	Set the VW1C1 bit in the VW1C register to 0 (digital filter enabled).	–
8	Select the interrupt request timing by the VCAC1 bit in the VCAC register and the VW1C7 bit in the VW1C register.	
9	Set the VW1C2 bit in the VW1C register to 0.	
10	Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on).	–
11	Wait for 2 cycles of the sampling clock of the digital filter.	– (No wait time required)
12	Set the VW1C0 bit in the VW1C register to 1 (comparator A1 interrupt enabled).	

Note:
1. When the VW1C0 bit is set to 0, steps 6 and 7 can be executed at the same time (with one instruction).



VW1C1, VW1C2, VW1C3, VW1C7: Bits in VW1C register
VCAC1: Bit in VCAC register
CM1POR, IRQ1SEL: Bits in CMPA register

The above applies when:
- VCA26 bit in VCA2 register = 1 (comparator A1 circuit enabled)
- VW1C0 bit in VW1C register = 1 (comparator A1 interrupt enabled)
- CM1OE bit in CMPA register = 1 (output enabled)
- VCA22 bit in VCA2 register = 1 (LVCMP1 pin input voltage)
- COMPSEL bit in CMPA register = 1 (bits IRQ1SEL and IRQ2SEL enabled)

Figure 32.2 Operating Example of Comparator A1 (Digital Filter Enabled)

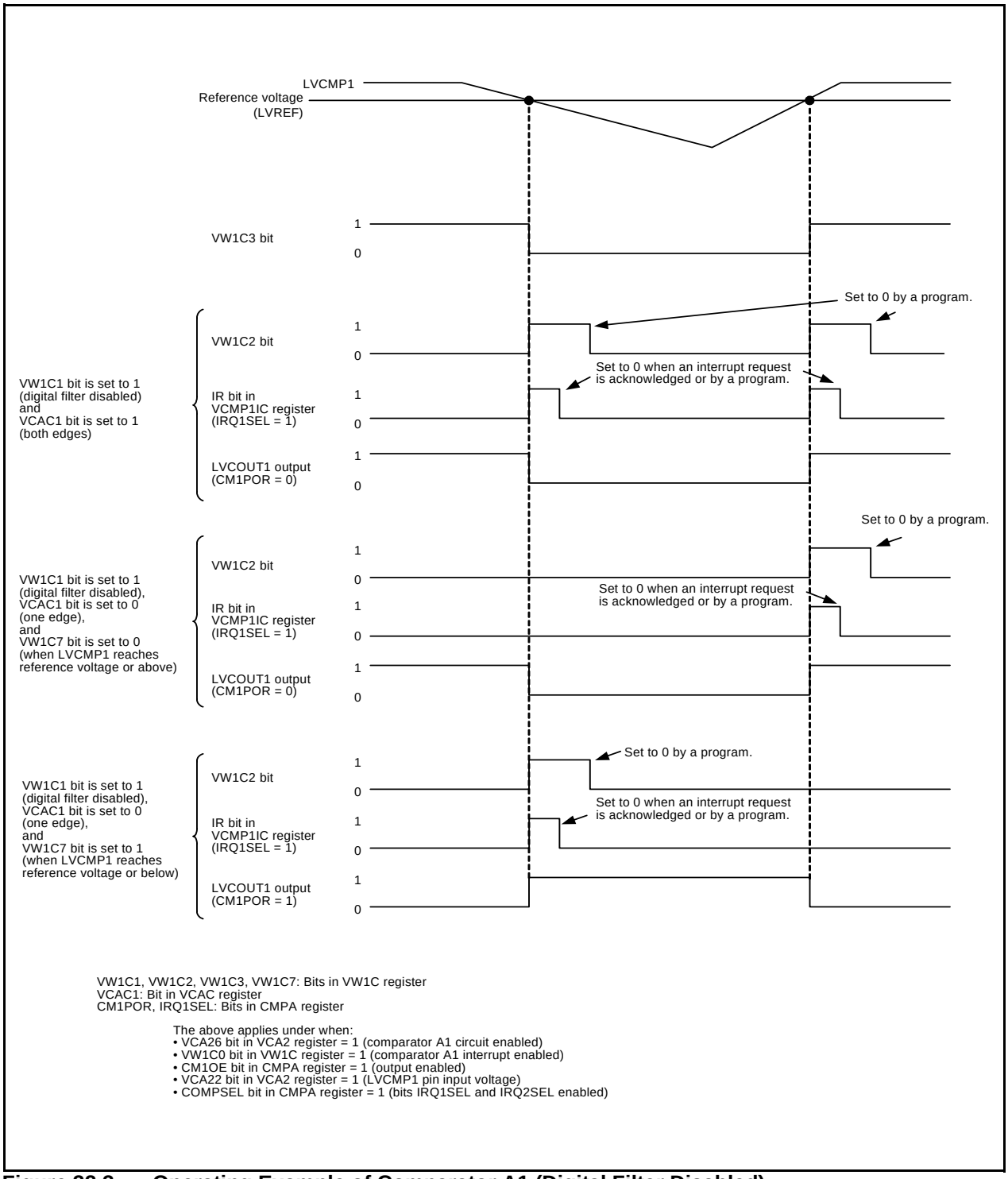


Figure 32.3 Operating Example of Comparator A1 (Digital Filter Disabled)

32.4.2 Comparator A2

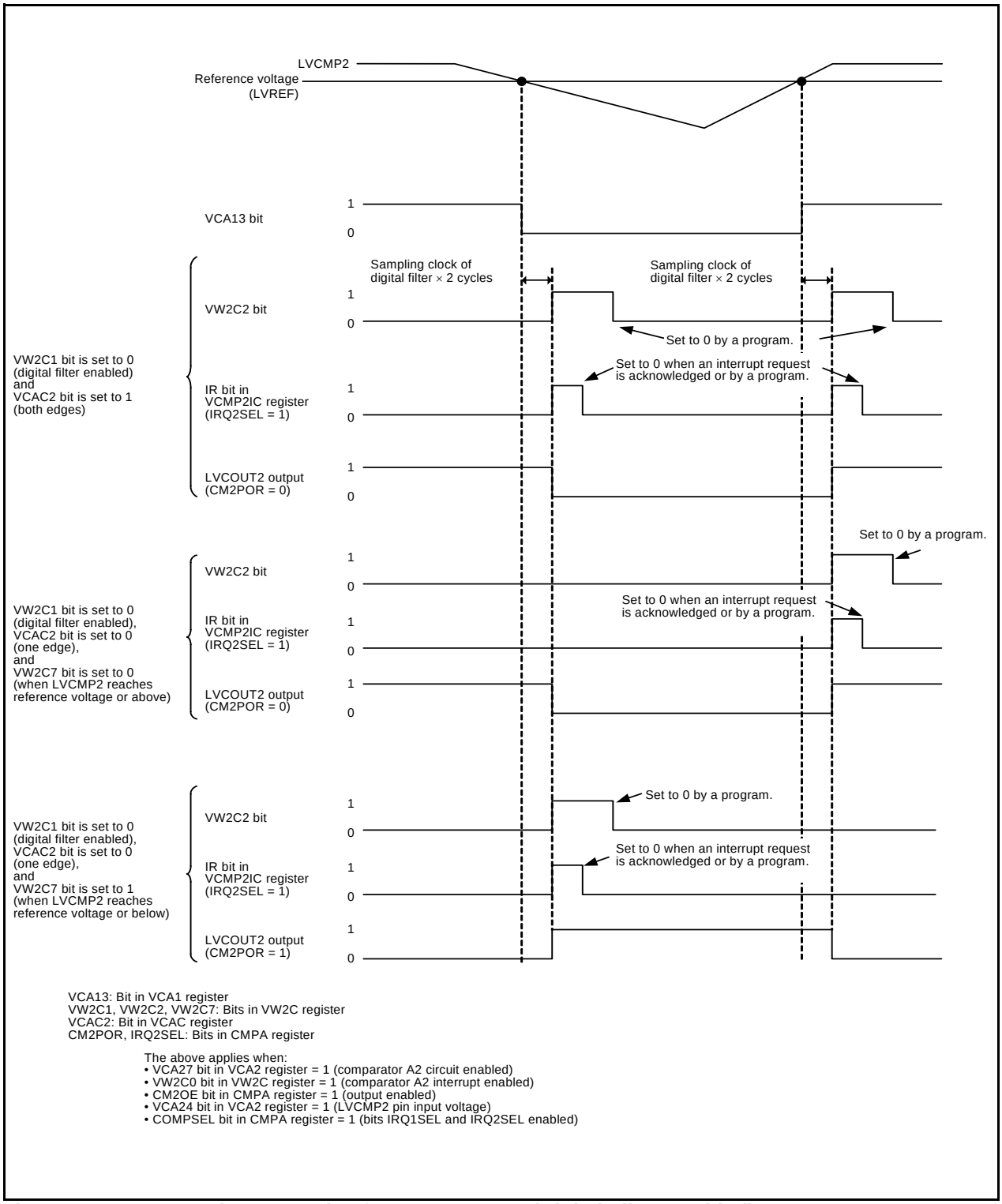
Table 32.4 lists the Procedure for Setting Bits Associated Comparator A2 Interrupt, Figure 32.4 shows an Operating Example of Comparator A2 (Digital Filter Enabled), and Figure 32.5 shows an Operating Example of Comparator A2 (Digital Filter Disabled).

Table 32.4 Procedure for Setting Bits Associated Comparator A2 Interrupt

Step	When Using Digital Filter	When Using No Digital Filter
1	Set the COMPSEL bit in the CMPA register to 1 (bits IRQ1SEL and IRQ2SEL enabled).	
2	Set the VCA23 bit in the VCA2 register to 1 (LVREF pin input voltage) and the VCA24 bit to 1 (LVCMP2 pin input voltage).	
3	Set the VCA27 bit in the VCA2 register to 1 (comparator A2 circuit enabled).	
4	Wait for td(E-A).	
5	Select the interrupt type by the IRQ2SEL bit in the CMPA register.	
6	Select the sampling clock of the digital filter by bits VW2F0 and VW2F1 in the VW2C register.	Set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).
7 (1)	Set the VW2C1 bit in the VW2C register to 0 (digital filter enabled).	–
8	Select the interrupt request timing by the VCAC2 bit in the VCAC register and the VW2C7 bit in the VW2C register.	
9	Set the VW2C2 bit in the VW2C register to 0.	
10	Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on).	–
11	Wait for 2 cycles of the sampling clock of the digital filter.	– (No wait time required)
12	Set the VW2C0 bit in the VW2C register to 1 (comparator A2 interrupt enabled).	

Note:

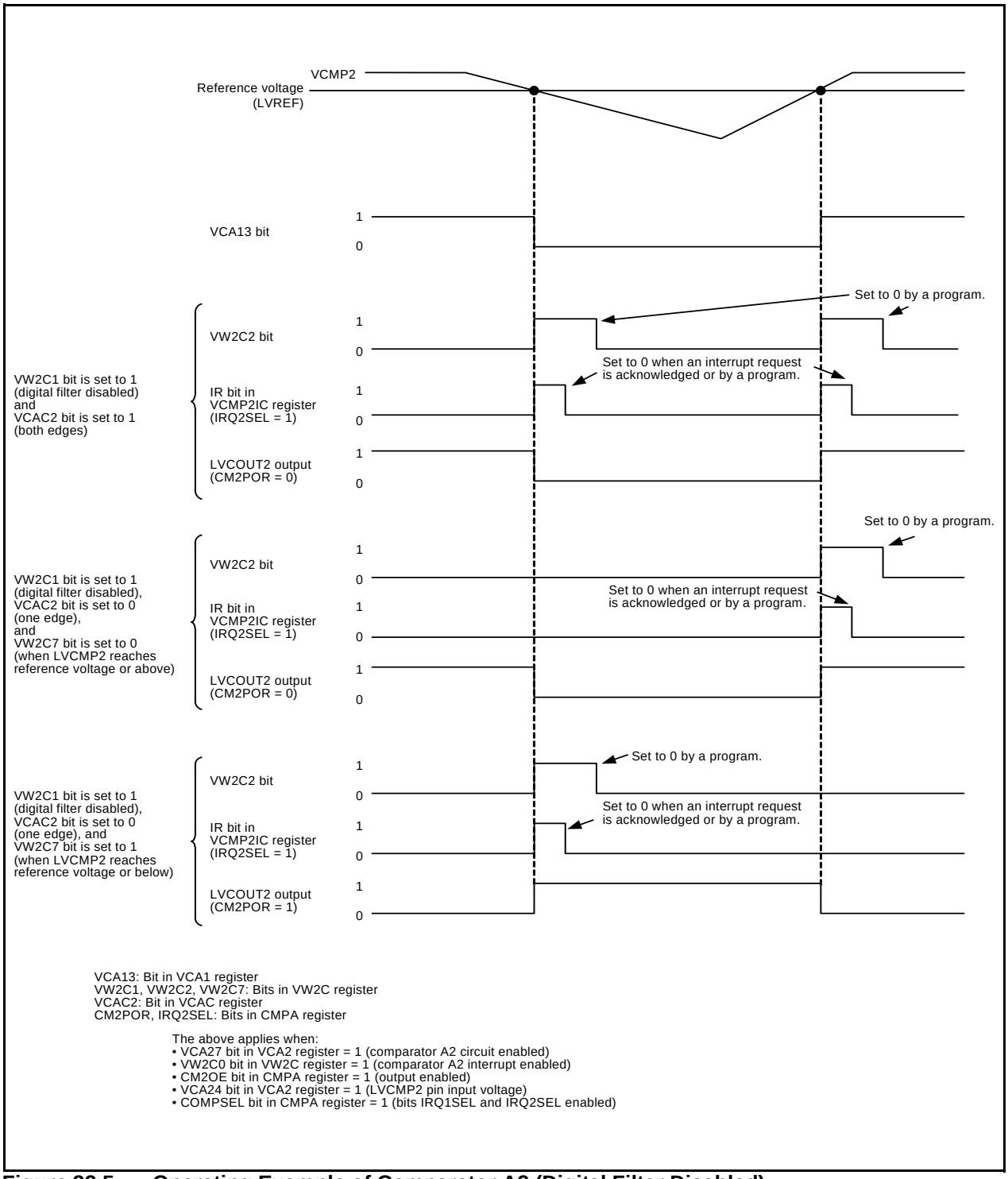
1. When the VW2C0 bit is set to 0, steps 6 and 7 can be executed at the same time (with one instruction).



VCA13: Bit in VCA1 register
VW2C1, VW2C2, VW2C7: Bits in VW2C register
VCAC2: Bit in VCAC register
CM2POR, IRQ2SEL: Bits in CMPA register

The above applies when:
- VCA27 bit in VCA2 register = 1 (comparator A2 circuit enabled)
- VW2C0 bit in VW2C register = 1 (comparator A2 interrupt enabled)
- CM2OE bit in CMPA register = 1 (output enabled)
- VCA24 bit in VCA2 register = 1 (LVCMP2 pin input voltage)
- COMPSEL bit in CMPA register = 1 (bits IRQ1SEL and IRQ2SEL enabled)

Figure 32.4 Operating Example of Comparator A2 (Digital Filter Enabled)



VCA13: Bit in VCA1 register
VW2C1, VW2C2, VW2C7: Bits in VW2C register
VCAC2: Bit in VCAC register
CM2POR, IRQ2SEL: Bits in CMPA register

The above applies when:
- VCA27 bit in VCA2 register = 1 (comparator A2 circuit enabled)
- VW2C0 bit in VW2C register = 1 (comparator A2 interrupt enabled)
- CM2OE bit in CMPA register = 1 (output enabled)
- VCA24 bit in VCA2 register = 1 (LVCMP2 pin input voltage)
- COMPSEL bit in CMPA register = 1 (bits IRQ1SEL and IRQ2SEL enabled)

Figure 32.5 Operating Example of Comparator A2 (Digital Filter Disabled)

32.5 Comparator A1 and Comparator A2 Interrupts

Comparator A generates an interrupt request from two sources, comparator A1 and comparator A2. Non-maskable or maskable can be selected for each interrupt type.
Refer to **12. Interrupts** for details of interrupts.

32.5.1 Non-Maskable Interrupts

When the COMPSEL bit in the CMPA register is set to 1 (bits IRQ1SEL and IRQ2SEL enabled) and the IRQiSEL (i = 1 or 2) is set to 0, the comparator Ai interrupt functions as a non-maskable interrupt.
When the selected interrupt request timing occurs, the VWiC2 bit in the VWiC register is set to 1. At this time, a non-maskable interrupt request for comparator Ai is generated.

32.5.2 Maskable Interrupts

When the COMPSEL bit in the CMPA register is set to 1 (bits IRQ1SEL and IRQ2SEL enabled) and the IRQiSEL (i = 1 or 2) is set to 1, the comparator Ai interrupt functions as a maskable interrupt.
The comparator Ai interrupt uses the corresponding VCMPiIC register (bits IR and ILVL0 to ILVL2) and a single vector. When the selected interrupt request timing occurs, the VWiC2 bit in the VWiC register is set to 1. At this time, the IR bit in the VCMPiIC register is set to 1 (interrupt requested).
Refer to **12.3 Interrupt Control** for the VCMPiIC register and **12.1.5.2 Relocatable Vector Tables** for interrupt vectors.

33. Comparator B

Comparator B compares a reference input voltage and an analog input voltage. Comparator B1 and comparator B3 are independent of each other.

33.1 Introduction

The comparison result of the reference input voltage and analog input voltage can be read by software. An input to the IVREFi (i = 1 or 3) pin can be used as the reference input voltage.
Table 33.1 lists the Comparator B Specifications, Figure 33.1 shows the Comparator B Block Diagram, and Table 33.2 lists the I/O Pins.

Table 33.1 Comparator B Specifications

Item	Specification
Analog input voltage	Input voltage to the IVCMPi pin
Reference input voltage	Input voltage to the IVREFi pin
Comparison result	Read from the INTiCOUT bit in the INTCMP register
Interrupt request generation timing	When the comparison result changes.
Selectable function	• Digital filter function Whether the digital filter is applied or not and the sampling frequency can be selected.

i = 1 or 3

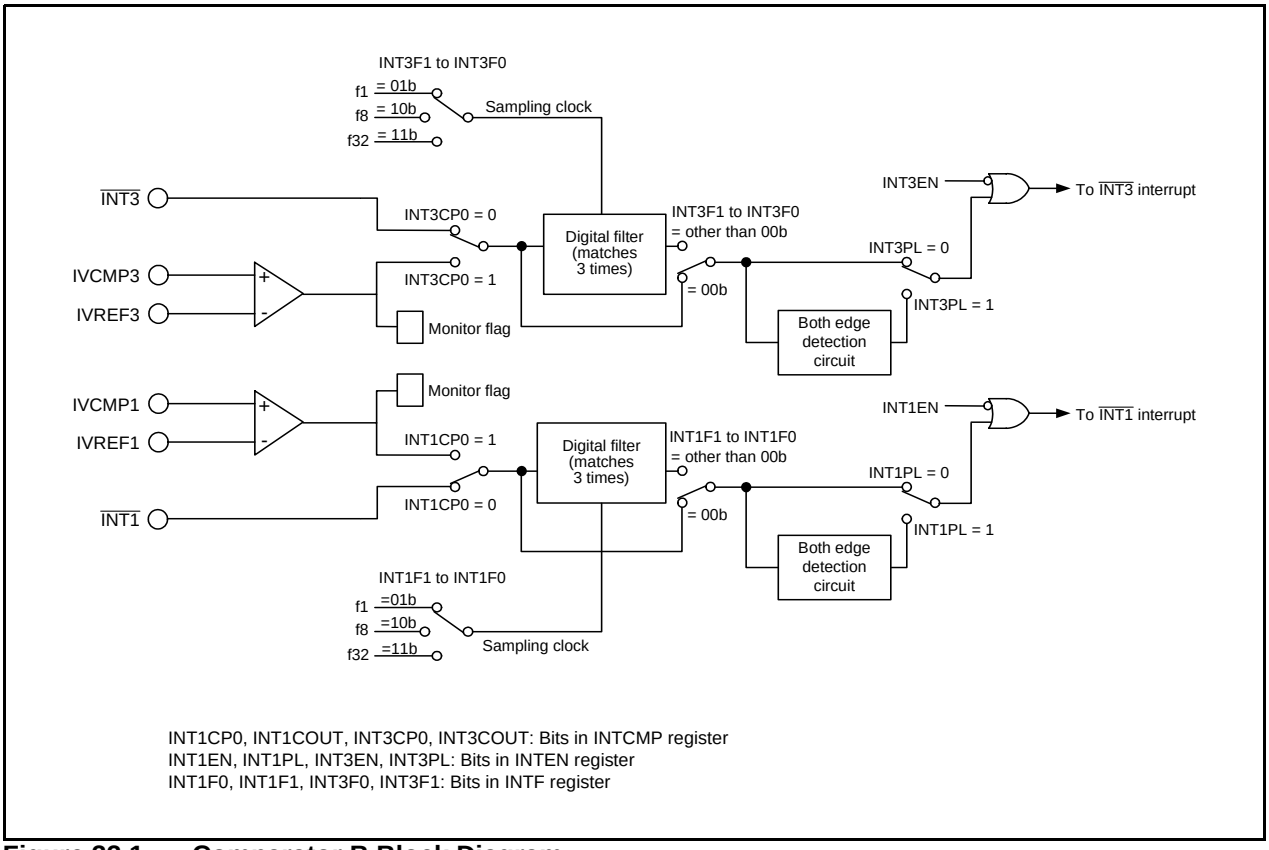


Figure 33.1 Comparator B Block Diagram

Table 33.2 I/O Pins

Pin Name	I/O	Function
IVCMP1	Input	Comparator B1 analog pin
IVREF1	Input	Comparator B1 reference voltage pin
IVCMP3	Input	Comparator B3 analog pin
IVREF3	Input	Comparator B3 reference voltage pin

33.2 Registers

33.2.1 Comparator B Control Register 0 (INTCMP)

Address 01F8h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3COUT	—	—	INT3CP0	INT1COUT	—	—	INT1CP0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT1CP0	Comparator B1 operation enable bit	0: Comparator B1 operation disabled 1: Comparator B1 operation enabled	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	INT1COUT	Comparator B1 monitor flag	0: IVCMP1 < IVREF1 or comparator B1 operation disabled 1: IVCMP1 > IVREF1	R
b4	INT3CP0	Comparator B3 operation enable bit	0: Comparator B3 operation disabled 1: Comparator B3 operation enabled	R/W
b5	—	Reserved bits	Set to 0.	R/W
b6	—			
b7	INT3COUT	Comparator B3 monitor flag	0: IVCMP3 < IVREF3 or comparator B3 operation disabled 1: IVCMP3 > IVREF3	R

33.2.2 External Input Enable Register 0 (INTEN)

Address 01FAh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3PL	INT3EN	INT2PL	INT2EN	INT1PL	INT1EN	INT0PL	INT0EN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0EN	$\overline{\text{INT0}}$ input enable bit	0: Disabled 1: Enabled	R/W
b1	INT0PL	$\overline{\text{INT0}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b2	INT1EN	$\overline{\text{INT1}}$ input enable bit	0: Disabled 1: Enabled	R/W
b3	INT1PL	$\overline{\text{INT1}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b4	INT2EN	$\overline{\text{INT2}}$ input enable bit	0: Disabled 1: Enabled	R/W
b5	INT2PL	$\overline{\text{INT2}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b6	INT3EN	$\overline{\text{INT3}}$ input enable bit	0: Disabled 1: Enabled	R/W
b7	INT3PL	$\overline{\text{INT3}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W

Notes:
1. To set the INTiPL bit (i = 0 to 3) to 1 (both edges), set the POL bit in the INTiIC register to 0 (falling edge selected).
2. The IR bit in the INTiIC register may be set to 1 (interrupt requested) if the INTiPL bit is rewritten. Refer to **12.8.4 Changing Interrupt Sources**.

33.2.3 INT Input Filter Select Register 0 (INTF)

Address 01FCh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3F1	INT3F0	INT2F1	INT2F0	INT1F1	INT1F0	INT0F1	INT0F0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0F0	$\overline{\text{INT0}}$ input filter select bit	b1 b0 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b1	INT0F1			R/W
b2	INT1F0	$\overline{\text{INT1}}$ input filter select bit	b3 b2 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b3	INT1F1			R/W
b4	INT2F0	$\overline{\text{INT2}}$ input filter select bit	b5 b4 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b5	INT2F1			R/W
b6	INT3F0	$\overline{\text{INT3}}$ input filter select bit	b7 b6 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b7	INT3F1			R/W

33.3 Functional Description

Comparator B1 and comparator B3 operate independently. Their operations are the same.
Table 33.3 lists the Procedure for Setting Registers Associated with Comparator B.

Table 33.3 Procedure for Setting Registers Associated with Comparator B

Step	Register	Bit	Setting Value
1	Select the function of pins IVCMPi and IVREFi. Refer to **7.5 Port Settings**. However, set registers and bits other than listed in step 2 and the following steps.		
2	INTF	Select whether to enable or disable the filter. Select the sampling clock.	
3	INTCMP	INTiCP0	1 (operation enabled)
4	Wait for comparator stability time (TBD μs max.)		
5	INTEN	INTiEN	When using an interrupt: 1 (interrupt enabled)
		INTiPL	When using an interrupt: Select the input polarity.
6	INTiIC	ILVL0 to ILVL2	When using an interrupt: Select the interrupt priority level.
		IR	When using an interrupt: 0 (no interrupt requested: initialization)

i = 1 or 3

Figure 33.2 shows an Operating Example of Comparator Bi (i = 1 or 3).
If the analog input voltage is higher than the reference input voltage, the INTiCOUT bit in the INTCMP register is set to 1. If the analog input voltage is lower than the reference input voltage, the INTiCOUT bit is set to 0. To use the comparator Bi interrupt, set the INTiEN bit in the INTEN register to 1 (interrupt enabled). If the comparison result changes at this time, a comparator Bi interrupt request is generated. Refer to **33.4 Comparator B1 and Comparator B3 Interrupts** for details of interrupts.

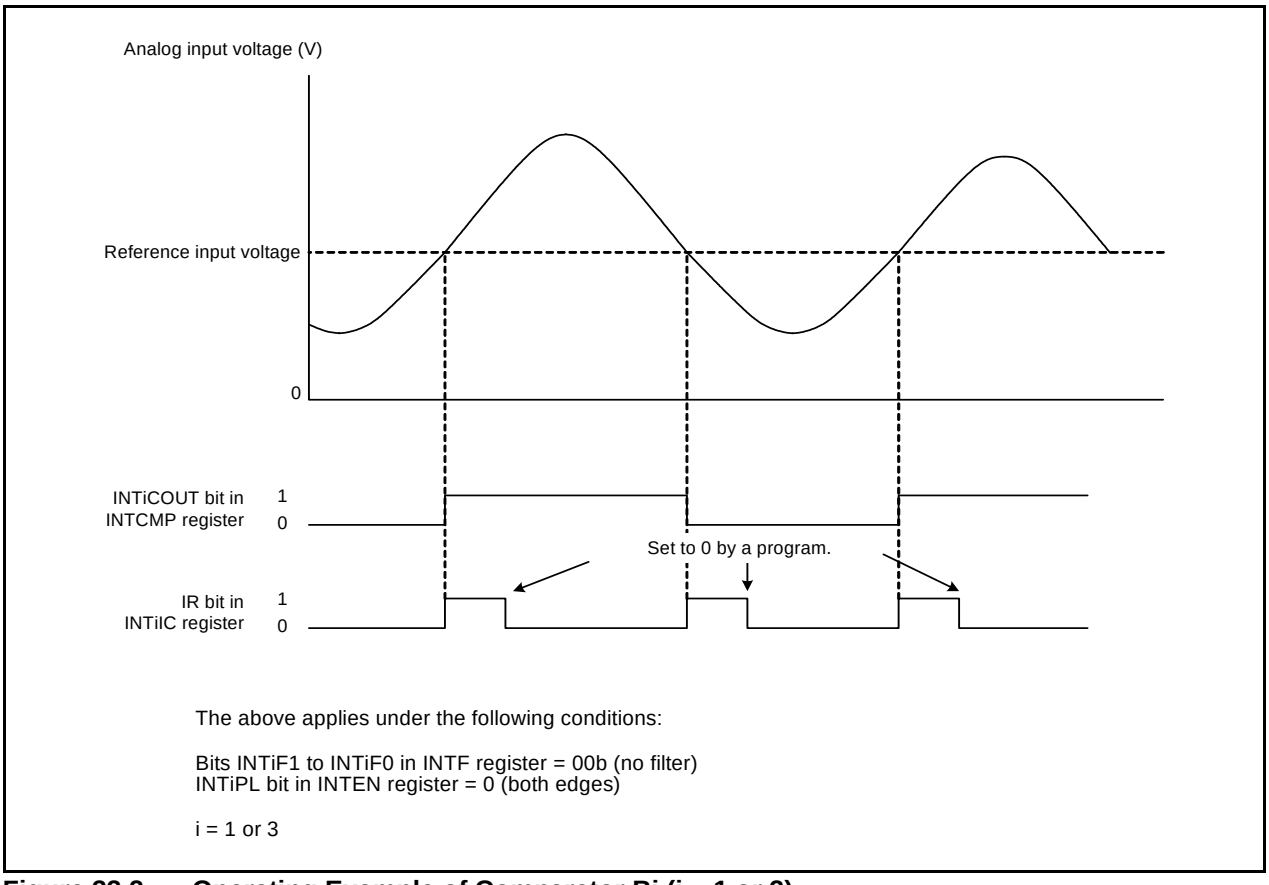


Figure 33.2 Operating Example of Comparator Bi (i = 1 or 3)

33.3.1 Comparator Bi Digital Filter (i = 1 or 3)

Comparator Bi can use the same digital filter as the INTi input. The sampling clock can be selected by bits INTiF0 and INTiF1 in the INTF register. The INTiCOUT signal output from comparator Bi is sampled every sampling clock. When the level matches three times, the IR bit in the INTiIC register is set to 1 (interrupt requested).

Figure 33.3 shows the Configuration of Comparator Bi Digital Filter, and Figure 33.4 shows an Operating Example of Comparator Bi Digital Filter.

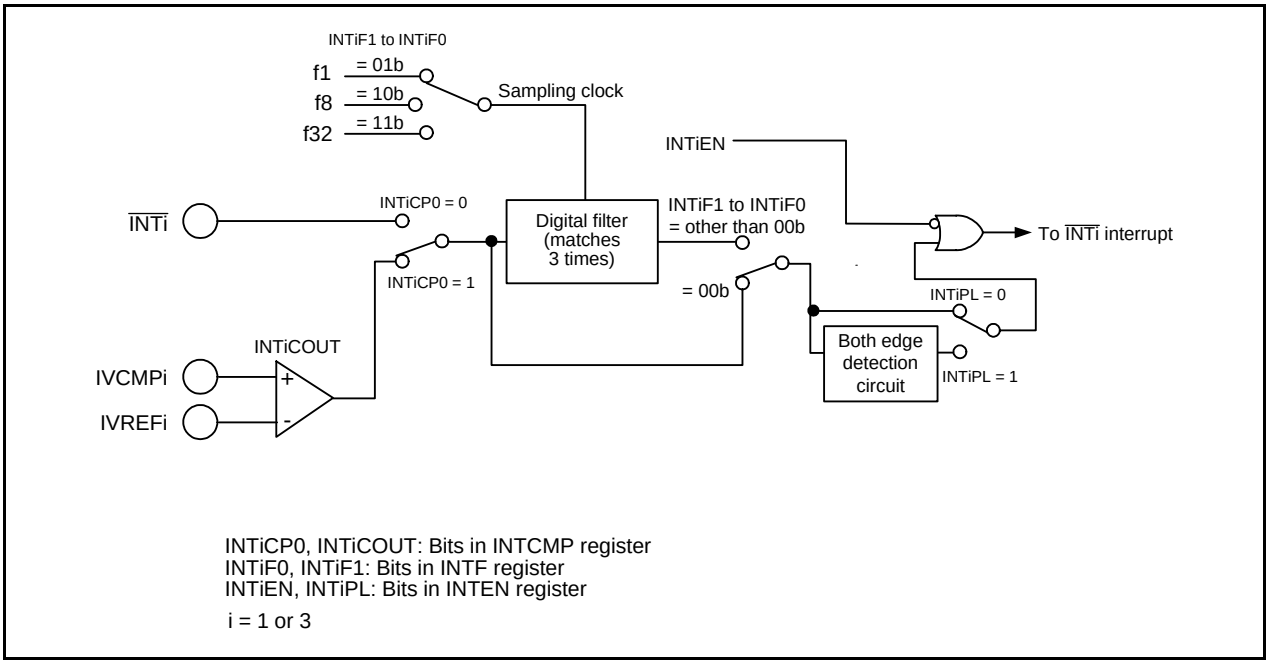


Figure 33.3 Configuration of Comparator Bi Digital Filter

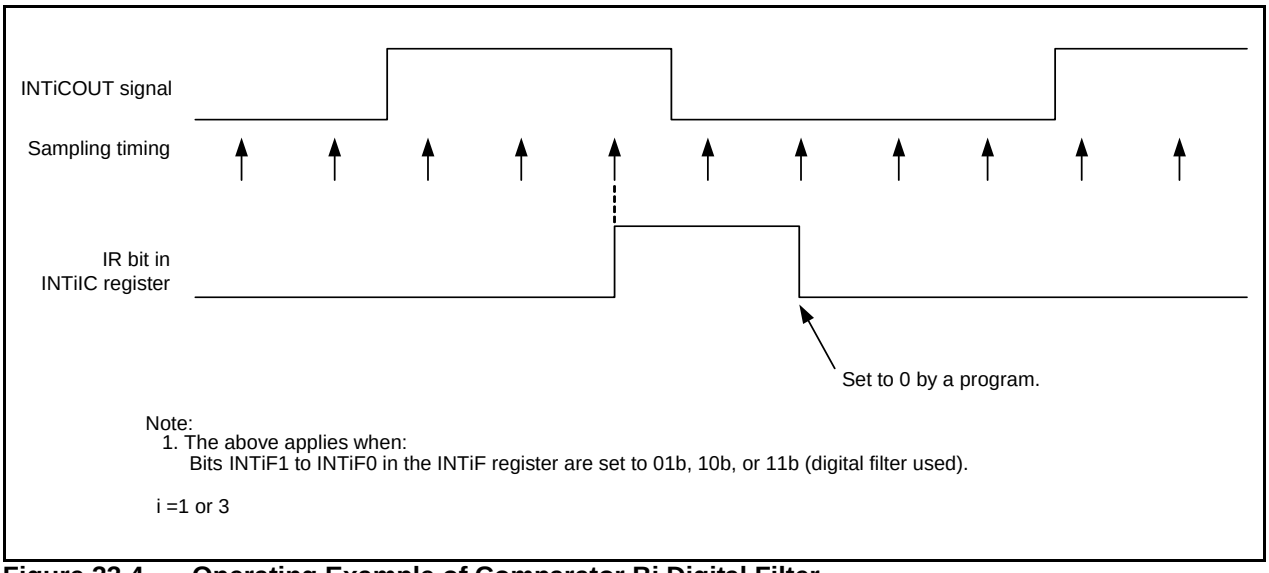


Figure 33.4 Operating Example of Comparator Bi Digital Filter

33.4 Comparator B1 and Comparator B3 Interrupts

Comparator B generates an interrupt request from two sources, comparator B1 and comparator B3. The comparator Bi (i = 1 or 3) interrupt uses the same INTiIC register (bits IR and ILVL0 to ILVL2) as the INTi (i = 1 or 3) and a single vector.

To use the comparator Bi interrupt, set the INTiEN bit in the INTEN register to 1 (interrupt enabled). In addition, the polarity can be selected by the INTiPL bit in the INTEN register and the POL bit in the INTiIC register.

Inputs can also be passed through the digital filter with three different sampling clocks.

34. LCD Drive Control Circuit

A liquid crystal display (LCD) drive control circuit is integrated on chip.
A maximum of 56 pins can be used for segment output and 8 pins for common output. Up to 416 pixels of an LCD display can be controlled.
Segment output pins, common output pins, and the capacity connect pins CL1 and CL2 for the voltage multiplier are shared with the I/O port functions. When the LCD display function is not used, these pins are used as I/O ports. Pins VL1 to VL4 are used as the power supply pins for the LCD drive control circuit.
The number of these LCD display function pins varies for each group. Table 34.1 lists the LCD Display Function Pins Provided for Each Group.
This chapter applies to the R8C/L3AA Group and R8C/L3AB Group, which have the maximum number of LCD display function pins. For other groups, note that only the pins listed in Table 34.1 are provided.

Table 34.1 LCD Display Function Pins Provided for Each Group

Shared I/O Port	L35A, L35B Group Common output: Max. 4 Segment output: Max. 24								L36A, L36B Group Common output: Max. 8 Segment output: Max. 32								L38A, L38B Group Common output: Max. 8 Segment output: Max. 48								L3AA, L3AB Group Common output: Max. 8 Segment output: Max. 56							
P0	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0
P1	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	SEG 11	SEG 10	SEG 9	SEG 8	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8
P2	SEG 23	SEG 22	SEG 21	SEG 20	–	–	–	–	SEG 23	SEG 22	SEG 21	SEG 20	–	–	–	–	SEG 23	SEG 22	SEG 21	SEG 20	SEG 19	SEG 18	SEG 17	SEG 16	SEG 23	SEG 22	SEG 21	SEG 20	SEG 19	SEG 18	SEG 17	SEG 16
P3	-	-	-	-	SEG 27	SEG 26	SEG 25	SEG 24	SEG 31	SEG 30	SEG 29	SEG 28	SEG 27	SEG 26	SEG 25	SEG 24	SEG 31	SEG 30	SEG 29	SEG 28	SEG 27	SEG 26	SEG 25	SEG 24	SEG 31	SEG 30	SEG 29	SEG 28	SEG 27	SEG 26	SEG 25	SEG 24
P4	SEG 39	SEG 38	SEG 37	SEG 36	SEG 35	SEG 34	SEG 33	SEG 32	SEG 39	SEG 38	SEG 37	SEG 36	SEG 35	SEG 34	SEG 33	SEG 32	SEG 39	SEG 38	SEG 37	SEG 36	SEG 35	SEG 34	SEG 33	SEG 32	SEG 39	SEG 38	SEG 37	SEG 36	SEG 35	SEG 34	SEG 33	SEG 32
P5	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	SEG 43	SEG 42	SEG 41	SEG 40
P6	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	SEG 51	SEG 50	SEG 49	SEG 48	SEG 47	SEG 46	SEG 45	SEG 44	SEG 51	SEG 50	SEG 49	SEG 48	SEG 47	SEG 46	SEG 45	SEG 44
P7	COM 0	COM 1	COM 2	COM 3	–	–	–	–	COM 0	COM 1	COM 2	COM 3	SEG 55	SEG 54	SEG 53	SEG 52	COM 0	COM 1	COM 2	COM 3	SEG 55	SEG 54	SEG 53	SEG 52	COM 0	COM 1	COM 2	COM 3	SEG 55	SEG 54	SEG 53	SEG 52
P12	–	–	–	–	CL2	CL1	–	–	–	–	–	–	CL2	CL1	–	–	–	–	–	–	CL2	CL1	–	–	–	–	–	–	CL2	CL1	–	–
–	VL1								VL1								VL1								VL1							
–	VL2								VL2								VL2								VL2							
–	–								VL3								VL3								VL3							
–	VL4								VL4								VL4								VL4							

Notes:
1. The symbol “-” indicates there is no LCD display function.
2. SEG52 to SEG55 can be used as COM7 to COM4.
3. The R8C/L35A Group and R8C/L35B Group do not have the VL3 pin.
   The available bias settings are 1/3 bias, 1/2 bias, or static.

34.1 Introduction

Table 34.2 lists the Specification Overview of LCD Drive Control Circuit (1) and Table 34.3 lists the Specification Overview of LCD Drive Control Circuit (2). Figure 34.1 shows a Block Diagram of LCD Drive Control Circuit.

Table 34.2 Specification Overview of LCD Drive Control Circuit (1)

<table>
<tr><th>Item</th><th>Specification</th></tr>
<tr><td>Segment output</td><td>Max. 56 pins (SEG0 to SEG55)
• Pins SEG0 to SEG51 can be individually controlled for use as an I/O port or a segment output pin.
• Pins SEG52 to SEG55 can be individually controlled for use as an I/O port or a common output/segment output pin.</td></tr>
<tr><td>Common output</td><td>Max. 8 pins (COM0 to COM7)
• The common output pins can be selected.
• Pins COM0 to COM3 can be used I/O ports when not in use as common output pins.
• Pins COM4 to COM7 can be individually controlled for use as an I/O port or a segment output pin when not in use as a common output pin.
<table>
<tr><th>Duty</th><th>Common Pin</th><th>Maximum Number of Display Pixels</th></tr>
<tr><td>Static</td><td>COM0</td><td>56 dots or 8-segment LCD 7 digits</td></tr>
<tr><td>1/2</td><td>COM0, COM1</td><td>112 dots or 8-segment LCD 14 digits</td></tr>
<tr><td>1/3</td><td>COM0 to COM2</td><td>168 dots or 8-segment LCD 21 digits</td></tr>
<tr><td>1/4</td><td>COM0 to COM3</td><td>224 dots or 8-segment LCD 28 digits</td></tr>
<tr><td>1/8</td><td>COM0 to COM7</td><td>416 dots or 8-segment LCD 52 digits</td></tr>
</table></td></tr>
<tr><td>Frame frequency</td><td>Frame frequency
$f(FR) = \frac{\text{Frequency of LCD clock}}{n \times \text{division ratio}}$
Notes:
n = 32 when f32 is selected
n = 4 when fC–LCD is selected
LCD clock source: bits LCKS0 to LCKS1
Division ratio: bits LPSC0 to LPSC2</td></tr>
<tr><td>Bias control
Note:
The R8C/L35A Group and R8C/L35B Group do not have the VL3 pin. The 1/4 bias value cannot be used.</td><td>External division resistors or the internal voltage multiplier can be used
(1) When external division resistors are used
• The LCD drive voltage is applied to LCD power supply pins VL1 to VL4 using external division resistors.
• The following voltage values are applied to LCD power supply pins VL1 to VL4 based on the bias values set by the LCR0 register.
<table>
<tr><th>Bias Value</th><th>Voltage Value</th></tr>
<tr><td>1/4 bias</td><td>VL4 = VLCD
VL3 = 3/4 VLCD
VL2 = 2/4 VLCD
VL1 = 1/4 VLCD</td></tr>
<tr><td>1/3 bias</td><td>VL4 = VLCD
VL3 = VL2 = 2/3 VLCD
VL1 = 1/3 VLCD</td></tr>
<tr><td>1/2 bias</td><td>VL4 = VLCD
VL1 = VL2 = VL3 = 1/2 VLCD</td></tr>
</table>
VLCD: Maximum value of supply voltage for LCD panel
(2) When the internal voltage multiplier is used
1/4 or 1/2 bias selected:
Based on the VL1 voltage, two times the voltage is generated at the VL2 pin, three times the voltage at the VL3 pin, and four times the voltage at the VL4 pin.
1/3 bias selected:
Based on the VL1 voltage, two times the voltage is generated at pins VL2 and VL3, and three time the voltage at the VL4 pin.
The VL1 voltage can be generated internally or input externally.</td></tr>
<tr><td>LCD display data register</td><td>LCD display data is set in the LCD display data register.
56 bytes
When a bit is set to 1, the corresponding segment is turned on.
When a bit is set to 0, the corresponding segment is turned off.</td></tr>
<tr><td>LCD display control data register</td><td>56 bytes
When a bit is set to 1, the corresponding segment is turned off or inverted. Turning off or inversion is selected by setting the LRVRS bit.</td></tr>
</table>

Table 34.3 Specification Overview of LCD Drive Control Circuit (2)

Item	Specification
Pin status at after reset	• SEG0 to SEG55: High impedance • COM0 to COM7: High impedance • CL1 to CL2: High impedance • VL1 to VL4: High impedance

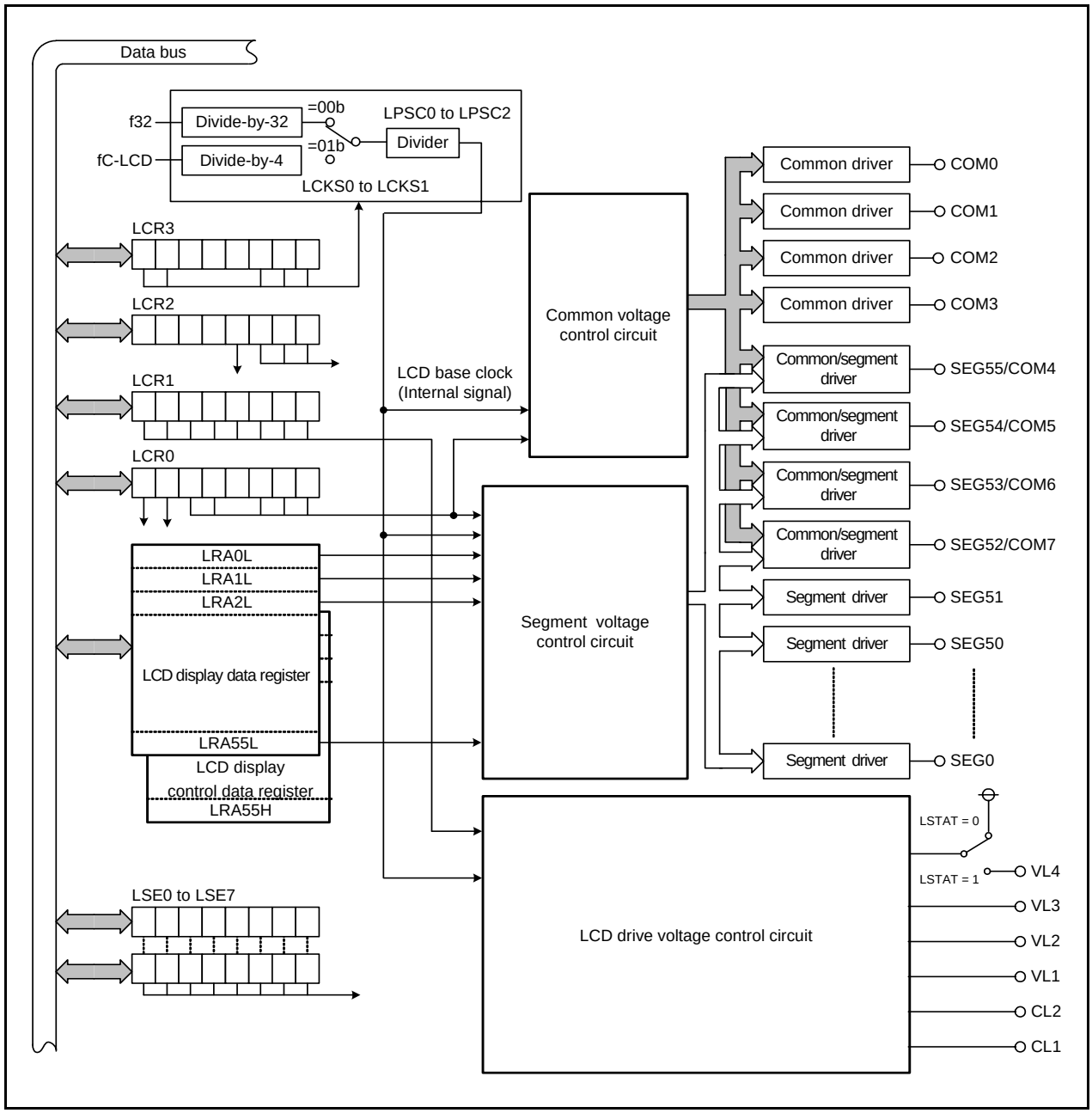


Figure 34.1 Block Diagram of LCD Drive Control Circuit

34.2 Registers

34.2.1 LCD Control Register (LCR0)

Address 0200h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	LSTAT	LDSPE	LBAS1	LBAS0	LWAV	LDTY2	LDTY1	LDTY0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	LDTY0	Duty Select Bit	b2 b1 b0 0 0 0: Static (COM0 used) 0 0 1: 1/2 duty (COM0 and COM1 used) 0 1 0: 1/3 duty (COM0 to COM2 used) 0 1 1: 1/4 duty (COM0 to COM3 used) 1 0 0: 1/8 duty (COM0 to COM7 used) 1 0 1: Do not set. 1 1 0: Do not set. 1 1 1: Do not set.	R/W
b1	LDTY1			R/W
b2	LDTY2			R/W
b3	LWAV	LCD waveform control select bit	0: Segment panel control waveform 1: Dot matrix panel control waveform	R/W
b4	LBAS0	Bias select bit	b5 b4 0 0: 1/2 bias 0 1: 1/3 bias 1 0: 1/4 bias 1 1: Do not set.	R/W
b5	LBAS1			R/W
b6	LDSPE	LCD display enable bit	0: LCD off 1: LCD on	R/W
b7	LSTAT	LCD drive start bit	0: Drive starts 1: Drive stops	R/W

34.2.2 LCD Bias Control Register (LCR1)

Address 0201h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	LVUPE	LVURS	LVWT1	LVWT0	LVLS3	LVLS2	LVLS1	LVLS0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function			R/W
b0	LVLS0	VL1 internally-generated voltage select bit		LBAS1 to LBAS0 = 00b/10b (1/2, 1/4 bias)	LBAS1 to LBAS0 = 01b (1/3 bias)	R/W
b1	LVLS1		b3 b2 b1 b0			R/W
b2	LVLS2		0 0 0 0 : VL1 =	1.120 V	1.120 V	R/W
b3	LVLS3		0 0 0 1 : VL1 =	1.159 V	1.159 V	R/W
			0 0 1 0 : VL1 =	1.200 V	1.200 V	
			0 0 1 1 : VL1 =	1.244 V	1.244 V	
			0 1 0 0 : VL1 =	1.292 V	1.292 V	
			0 1 0 1 : VL1 =	1.344 V	1.344 V	
			0 1 1 0 : VL1 =	1.120 V	1.400 V	
			0 1 1 1 : VL1 =	1.120 V	1.461 V	
			1 0 0 0 : VL1 =	1.120 V	1.527 V	
			1 0 0 1 : VL1 =	1.120 V	1.600 V	
			1 0 1 0 : VL1 =	1.120 V	1.680 V	
			1 0 1 1 : VL1 =	1.120 V	1.768 V	
			1 1 0 0 : VL1 =	1.120 V	1.120 V	
			1 1 0 1 : VL1 =	1.120 V	1.120 V	
			1 1 1 0 : VL1 =	1.120 V	1.120 V	
			1 1 1 1 : VL1 =	1.120 V	1.120 V	
b4	LVWT0	Voltage multiplier wait time select bit		Other than LDTY2 to LDTY0 = 010b (other than 1/3 duty)	LDTY2 to LDTY0 = 010b (1/3 duty)	R/W
b5	LVWT1		b5 b4			R/W
			0 0 : Wait time = f(FR)	× 64 counts	× 48 counts	
			0 1 : Wait time = f(FR)	× 32 counts	× 24 counts	
			1 0 : Wait time = f(FR)	× 16 counts	× 12 counts	
			1 1 : Wait time = f(FR)	× 8 counts	× 6 counts	
b6	LVURS	Voltage multiplier reference voltage source select bit	0: VL1 externally-input voltage 1: VL1 internally-generated voltage			R/W
b7	LVUPE	Voltage multiplier enable bit	0: Voltage multiplier disabled 1: Voltage multiplier enabled			R/W

34.2.3 LCD Display Control Register (LCR2)

Address 0202h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	LRVRS	LDSPC	LDFR2	LDFR1	LDFR0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function			R/W
b0	LDFR0	Data display control interval select bit		Other than LDTY2 to LDTY0 = 010b (other than 1/3 duty)	LDTY2 to LDTY0 = 010b (1/3 duty)	R/W
b1	LDFR1		b2 b1 b0			R/W
b2	LDFR2		0 0 0: Display control interval = f(FR)	× 16 counts	× 12 counts	R/W
			0 0 1: Display control interval = f(FR)	× 32 counts	× 24 counts	
			0 1 0: Display control interval = f(FR)	× 64 counts	× 48 counts	
			0 1 1: Display control interval = f(FR)	× 128 counts	× 96 counts	
			1 0 0: Display control interval = f(FR)	× 256 counts	× 192 counts	
			1 0 1: Do not set.			
			1 1 0: Do not set.			
			1 1 1: Display control interval =	Static	Static	
b3	LDSPC	LCD data display control enable bit	0: Data display control disabled 1: Data display control enabled			R/W
b4	LRVRS	LCD display control mode select bit	0: On/off display 1: Inverted display			R/W
b5	—	Reserved bits	Set to 0.			R/W
b6	—					R/W
b7	—					R/W

34.2.4 LCD Clock Control Register (LCR3)

Address 0203h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	LCKS1	LCKS0	—	—	—	LPSC2	LPSC1	LPSC0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	LPSC0	Division ratio select bit	b2 b1 b0	R/W
b1	LPSC1		0 0 0: Divide-by-2	R/W
b2	LPSC2		0 0 1: Divide-by-4 0 1 0: Divide-by-8 0 1 1: Divide-by-16 1 0 0: Divide-by-32 1 0 1: Divide-by-64 1 1 0: Divide-by-128 1 1 1: Do not set.	R/W
b3	—	Reserved bits	Set to 0.	—
b4	—			
b5	—			
b6	LCKS0	LCD clock source select bit	b7 b6	R/W
b7	LCKS1		0 0: f32 0 1: fC-LCD 1 0: Do not set. 1 1: Do not set.	R/W

34.2.5 LCD Port Select Register 0 (LSE0)

Address 0206h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	LSE07	LSE06	LSE05	LSE04	LSE03	LSE02	LSE01	LSE00
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	LSE00	LCD port select bit 0	0: Port P0_0 1: SEG0	R/W
b1	LSE01	LCD port select bit 1	0: Port P0_1 1: SEG1	R/W
b2	LSE02	LCD port select bit 2	0: Port P0_2 1: SEG2	R/W
b3	LSE03	LCD port select bit 3	0: Port P0_3 1: SEG3	R/W
b4	LSE04	LCD port select bit 4	0: Port P0_4 1: SEG4	R/W
b5	LSE05	LCD port select bit 5	0: Port P0_5 1: SEG5	R/W
b6	LSE06	LCD port select bit 6	0: Port P0_6 1: SEG6	R/W
b7	LSE07	LCD port select bit 7	0: Port P0_7 1: SEG7	R/W

34.2.6 LCD Port Select Register 1 (LSE1)

Address 0207h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	LSE15	LSE14	LSE13	LSE12	LSE11	LSE10	LSE09	LSE08
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	LSE08	LCD port select bit 8	0: Port P1_0 1: SEG8	R/W
b1	LSE09	LCD port select bit 9	0: Port P1_1 1: SEG9	R/W
b2	LSE10	LCD port select bit 10	0: Port P1_2 1: SEG10	R/W
b3	LSE11	LCD port select bit 11	0: Port P1_3 1: SEG11	R/W
b4	LSE12	LCD port select bit 12	0: Port P1_4 1: SEG12	R/W
b5	LSE13	LCD port select bit 13	0: Port P1_5 1: SEG13	R/W
b6	LSE14	LCD port select bit 14	0: Port P1_6 1: SEG14	R/W
b7	LSE15	LCD port select bit 15	0: Port P1_7 1: SEG15	R/W

34.2.7 LCD Port Select Register 2 (LSE2)

Address 0208h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	LSE23	LSE22	LSE21	LSE20	LSE19	LSE18	LSE17	LSE16
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	LSE16	LCD port select bit 16	0: Port P2_0 1: SEG16	R/W
b1	LSE17	LCD port select bit 17	0: Port P2_1 1: SEG17	R/W
b2	LSE18	LCD port select bit 18	0: Port P2_2 1: SEG18	R/W
b3	LSE19	LCD port select bit 19	0: Port P2_3 1: SEG19	R/W
b4	LSE20	LCD port select bit 20	0: Port P2_4 1: SEG20	R/W
b5	LSE21	LCD port select bit 21	0: Port P2_5 1: SEG21	R/W
b6	LSE22	LCD port select bit 22	0: Port P2_6 1: SEG22	R/W
b7	LSE23	LCD port select bit 23	0: Port P2_7 1: SEG23	R/W

34.2.8 LCD Port Select Register 3 (LSE3)

Address 0209h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	LSE31	LSE30	LSE29	LSE28	LSE27	LSE26	LSE25	LSE24
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	LSE24	LCD port select bit 24	0: Port P3_0 1: SEG24	R/W
b1	LSE25	LCD port select bit 25	0: Port P3_1 1: SEG25	R/W
b2	LSE26	LCD port select bit 26	0: Port P3_2 1: SEG26	R/W
b3	LSE27	LCD port select bit 27	0: Port P3_3 1: SEG27	R/W
b4	LSE28	LCD port select bit 28	0: Port P3_4 1: SEG28	R/W
b5	LSE29	LCD port select bit 29	0: Port P3_5 1: SEG29	R/W
b6	LSE30	LCD port select bit 30	0: Port P3_6 1: SEG30	R/W
b7	LSE31	LCD port select bit 31	0: Port P3_7 1: SEG31	R/W

34.2.9 LCD Port Select Register 4 (LSE4)

Address 020Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	LSE39	LSE38	LSE37	LSE36	LSE35	LSE34	LSE33	LSE32
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	LSE32	LCD port select bit 32	0: Port P4_0 1: SEG32	R/W
b1	LSE33	LCD port select bit 33	0: Port P4_1 1: SEG33	R/W
b2	LSE34	LCD port select bit 34	0: Port P4_2 1: SEG34	R/W
b3	LSE35	LCD port select bit 35	0: Port P4_3 1: SEG35	R/W
b4	LSE36	LCD port select bit 36	0: Port P4_4 1: SEG36	R/W
b5	LSE37	LCD port select bit 37	0: Port P4_5 1: SEG37	R/W
b6	LSE38	LCD port select bit 38	0: Port P4_6 1: SEG38	R/W
b7	LSE39	LCD port select bit 39	0: Port P4_7 1: SEG39	R/W

34.2.10 LCD Port Select Register 5 (LSE5)

Address 020Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	LSE47	LSE46	LSE45	LSE44	LSE43	LSE42	LSE41	LSE40
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	LSE40	LCD port select bit 40	0: Port P5_0 1: SEG40	R/W
b1	LSE41	LCD port select bit 41	0: Port P5_1 1: SEG41	R/W
b2	LSE42	LCD port select bit 42	0: Port P5_2 1: SEG42	R/W
b3	LSE43	LCD port select bit 43	0: Port P5_3 1: SEG43	R/W
b4	LSE44	LCD port select bit 44	0: Port P6_0 1: SEG44	R/W
b5	LSE45	LCD port select bit 45	0: Port P6_1 1: SEG45	R/W
b6	LSE46	LCD port select bit 46	0: Port P6_2 1: SEG46	R/W
b7	LSE47	LCD port select bit 47	0: Port P6_3 1: SEG47	R/W

34.2.11 LCD Port Select Register 6 (LSE6)

Address 020Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	LSE55	LSE54	LSE53	LSE52	LSE51	LSE50	LSE49	LSE48
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	LSE48	LCD port select bit 48	0: Port P6_4 1: SEG48	R/W
b1	LSE49	LCD port select bit 49	0: Port P6_5 1: SEG49	R/W
b2	LSE50	LCD port select bit 50	0: Port P6_6 1: SEG50	R/W
b3	LSE51	LCD port select bit 51	0: Port P6_7 1: SEG51	R/W
b4	LSE52	LCD port select bit 52	0: Port P7_0 1: SEG52 or COM7	R/W
b5	LSE53	LCD port select bit 53	0: Port P7_1 1: SEG53 or COM6	R/W
b6	LSE54	LCD port select bit 54	0: Port P7_2 1: SEG54 or COM5	R/W
b7	LSE55	LCD port select bit 55	0: Port P7_3 1: SEG55 or COM4	R/W

34.2.12 LCD Port Select Register 7 (LSE7)

Address 020Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	LSE60	LSE59	LSE58	LSE57	LSE56
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	LSE56	LCD port select bit 56	0: Port P7_4 1: COM3	R/W
b1	LSE57	LCD port select bit 57	0: Port P7_5 1: COM2	R/W
b2	LSE58	LCD port select bit 58	0: Port P7_6 1: COM1	R/W
b3	LSE59	LCD port select bit 59	0: Port P7_7 1: COM0	R/W
b4	LSE60	LCD port select bit 60	0: Ports P12_2 and P12_3 1: CL1 and CL2	R/W
b5	—	Reserved bits	Set to 0.	R/W
b6	—			R/W
b7	—			R/W

34.3 Data Registers

The LCD display data register (LRAL) and the LCD display control data register (LRAH) are available as data registers.

When 1 is written to a bit in the LCD display data register, the corresponded segment of the LCD panel is turned on, when a bit is set to 0, the corresponding segment is turned off.

When 1 is written to a bit in the LCD display control data register while the LDSPC bit in the LCR2 register is set to 1, the corresponding segment of the LCD panel is operated (turned on/off or inverted) as specified by the LRVRS bit, for the interval selected by bits LDFR0 to LDFR2.

Symbol	Address	bit 7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
		COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0
LRA0L	0210h	SEG0							
LRA1L	0211h	SEG1							
LRA2L	0212h	SEG2							
LRA3L	0213h	SEG3							
LRA4L	0214h	SEG4							
LRA5L	0215h	SEG5							
LRA6L	0216h	SEG6							
LRA7L	0217h	SEG7							
LRA8L	0218h	SEG8							
LRA9L	0219h	SEG9							
LRA10L	021Ah	SEG10							
LRA11L	021Bh	SEG11							
LRA12L	021Ch	SEG12							
LRA13L	021Dh	SEG13							
LRA14L	021Eh	SEG14							
LRA15L	021Fh	SEG15							
LRA16L	0220h	SEG16							
LRA17L	0221h	SEG17							
LRA18L	0222h	SEG18							
LRA19L	0223h	SEG19							
LRA20L	0224h	SEG20							
LRA21L	0225h	SEG21							
LRA22L	0226h	SEG22							
LRA23L	0227h	SEG23							
LRA24L	0228h	SEG24							
LRA25L	0229h	SEG25							
LRA26L	022Ah	SEG26							
LRA27L	022Bh	SEG27							
LRA28L	022Ch	SEG28							
LRA29L	022Dh	SEG29							
LRA30L	022Eh	SEG30							
LRA31L	022Fh	SEG31							
LRA32L	0230h	SEG32							
LRA33L	0231h	SEG33							
LRA34L	0232h	SEG34							
LRA35L	0233h	SEG35							
LRA36L	0234h	SEG36							
LRA37L	0235h	SEG37							
LRA38L	0236h	SEG38							
LRA39L	0237h	SEG39							
LRA40L	0238h	SEG40							
LRA41L	0239h	SEG41							
LRA42L	023Ah	SEG42							
LRA43L	023Bh	SEG43							
LRA44L	023Ch	SEG44							
LRA45L	023Dh	SEG45							
LRA46L	023Eh	SEG46							
LRA47L	023Fh	SEG47							

Symbol	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
		COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0
LRA48L	0240h	SEG48							
LRA49L	0241h	SEG49							
LRA50L	0242h	SEG50							
LRA51L	0243h	SEG51							
LRA52L	0244h	SEG52							
LRA53L	0245h	SEG53							
LRA54L	0246h	SEG54							
LRA55L	0247h	SEG55							
LRA56L	0248h	Do not set.							
LRA57L	0249h								
LRA58L	024Ah								
LRA59L	024Bh								
LRA60L	024Ch								
LRA61L	024Dh								
LRA62L	024Eh								
LRA63L	024Fh								
LRA64L	0250h								
LRA65L	0251h								
LRA66L	0252h								
LRA67L	0253h								
LRA68L	0254h								
LRA69L	0255h								
LRA70L	0256h								
LRA71L	0257h								
LRA72L	0258h								
LRA73L	0259h								
LRA74L	025Ah								
LRA75L	025Bh								
LRA76L	025Ch								
LRA77L	025Dh								
LRA78L	025Eh								
LRA79L	025Fh								
LRA80L	0260h								
LRA81L	0261h								
LRA82L	0262h								
LRA83L	0263h								
LRA84L	0264h								
LRA85L	0265h								
LRA86L	0266h								
LRA87L	0267h								
LRA88L	0268h								
LRA89L	0269h								
LRA90L	026Ah								
LRA91L	026Bh								
LRA92L	026Ch								
LRA93L	026Dh								
LRA94L	026Eh								
LRA95L	026Fh								

Figure 34.2 LCD Display Data Register

Symbol	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
		COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0
LRA0H	0270h	SEG0							
LRA1H	0271h	SEG1							
LRA2H	0272h	SEG2							
LRA3H	0273h	SEG3							
LRA4H	0274h	SEG4							
LRA5H	0275h	SEG5							
LRA6H	0276h	SEG6							
LRA7H	0277h	SEG7							
LRA8H	0278h	SEG8							
LRA9H	0279h	SEG9							
LRA10H	027Ah	SEG10							
LRA11H	027Bh	SEG11							
LRA12H	027Ch	SEG12							
LRA13H	027Dh	SEG13							
LRA14H	027Eh	SEG14							
LRA15H	027Fh	SEG15							
LRA16H	0280h	SEG16							
LRA17H	0281h	SEG17							
LRA18H	0282h	SEG18							
LRA19H	0283h	SEG19							
LRA20H	0284h	SEG20							
LRA21H	0285h	SEG21							
LRA22H	0286h	SEG22							
LRA23H	0287h	SEG23							
LRA24H	0288h	SEG24							
LRA25H	0289h	SEG25							
LRA26H	028Ah	SEG26							
LRA27H	028Bh	SEG27							
LRA28H	028Ch	SEG28							
LRA29H	028Dh	SEG29							
LRA30H	028Eh	SEG30							
LRA31H	028Fh	SEG31							
LRA32H	0290h	SEG32							
LRA33H	0291h	SEG33							
LRA34H	0292h	SEG34							
LRA35H	0293h	SEG35							
LRA36H	0294h	SEG36							
LRA37H	0295h	SEG37							
LRA38H	0296h	SEG38							
LRA39H	0297h	SEG39							
LRA40H	0298h	SEG40							
LRA41H	0299h	SEG41							
LRA42H	029Ah	SEG42							
LRA43H	029Bh	SEG43							
LRA44H	029Ch	SEG44							
LRA45H	029Dh	SEG45							
LRA46H	029Eh	SEG46							
LRA47H	029Fh	SEG47							

Symbol	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
		COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0
LRA48H	02A0h	SEG48							
LRA49H	02A1h	SEG49							
LRA50H	02A2h	SEG50							
LRA51H	02A3h	SEG51							
LRA52H	02A4h	SEG52							
LRA53H	02A5h	SEG53							
LRA54H	02A6h	SEG54							
LRA55H	02A7h	SEG55							
LRA56H	02A8h	Do not set.							
LRA57H	02A9h								
LRA58H	02AAh								
LRA59H	02ABh								
LRA60H	02ACh								
LRA61H	02ADh								
LRA62H	02AEh								
LRA63H	02AFh								
LRA64H	02B0h								
LRA65H	02B1h								
LRA66H	02B2h								
LRA67H	02B3h								
LRA68H	02B4h								
LRA69H	02B5h								
LRA70H	02B6h								
LRA71H	02B7h								
LRA72H	02B8h								
LRA73H	02B9h								
LRA74H	02BAh								
LRA75H	02BBh								
LRA76H	02BCh								
LRA77H	02BDh								
LRA78H	02BEh								
LRA79H	02BFh								
LRA80H	02C0h								
LRA81H	02C1h								
LRA82H	02C2h								
LRA83H	02C3h								
LRA84H	02C4h								
LRA85H	02C5h								
LRA86H	02C6h								
LRA87H	02C7h								
LRA88H	02C8h								
LRA89H	02C9h								
LRA90H	02CAh								
LRA91H	02CBh								
LRA92H	02CCh								
LRA93H	02CDh								
LRA94H	02CEh								
LRA95H	02CFh								

Figure 34.3 LCD Display Control Data Register

34.4 LCD Drive Control

Table 34.4 shows an outline of the LCD drive control procedure.

Table 34.4 LCD Drive Control Procedure and Status of Segment and Common Pins

Procedure	Status of Segment and Common Pins
Reset	• I/O port (input) • High-impedance state (Depending on the pull-up control registers) • High-impedance
LSE0 to LSE7 register setting • Select segment output pins	
LCD display data register initial value setting • Set the initial value for the data output from the SEG pins LCD display control register initial value setting • Set the initial value for the SEG pin control	
LCR3 register setting • LCKS1 to LCKS0: Select the LCD clock source • LPSC2 to LPSC0: Select the division ratio	
LCR2 register setting • LDSPC: Enable LCD data display control • LDFR2 to LDFR0: Select the LCD data display control interval	
VL1 to VL4 Division resistor connected externally Voltage multiplier used	
LCR1 register setting • LVUPE: Enable the voltage multiplier • LVURS: Select the reference voltage for the voltage multiplier • LVWT1 to LVWT0: Select the wait time for the voltage multiplier • LVLS3 to LVLS0: Select the VL1 internally-generated reference voltage	
LCR0 register setting • LSTAT: Start LCD control • LDSPE: Enable LCD display • LBAS1 to LBAS0: Select the bias • LWAV: Select LCD waveform control • LDTY2 to LDTY0: Select the duty	At start of LCD control • When the LDSPE bit is set to 0, the segment and common pins output a low-level signal. • When the LDSPE bit is set to 1 and the LVUPE bit is set to 0, the segment and common pins output the content of the LCD display data register. • When the LDSPE bit is set to 1 and the LVUPE bit is set to 1, the segment and common pins output the content of the LCD display data register after the time specified by bits LVWT0 and LVWT1 has elapsed.
LCD display data register setting • Set the data output from the SEG pins	
LCR2 register setting • LDSPC: Enable LCD data display control • LDFR2 to LDFR0: Select the LCD data display control interval	

34.4.1 Segment Output Pin Selection

All of the segment output pins SEG0 to SEG55 and common output pins COM0 to COM7 are shared with I/O ports. Since all these pins function as I/O ports after a reset, set the corresponding LSEi bit (i = 00 to 59) bit to 1 for the pins to be used as segment output and common output for LCD displays. Set the corresponding LSEi bit to 0 (I/O port) for the pins not to be used as segment output and common output. If these pins are not used as I/O ports, perform unassigned pin handling for I/O ports (refer to **Table 7.24 Unassigned Pin Handling**).

34.4.2 LCD Clock Selection

Either f32 or fC-LCD is selected as the LCD clock source by setting bits LCKS0 and LCKS1. The division ratio is selected from a range of divide-by-1 to divide-by-64 by setting bits LPSC0 to LPSC2.

34.4.3 LCD Data Display Control

The LCD data display control function is used to turn on or off, or to invert an LCD display. This function is enabled by setting the LDSPC bit to 1. A display is turned on or off by setting the LRVRS bit to 0 and inverted by setting the bit to 1. The interval for turning on/off or inversion is selected by bits LDFR0 to LDFR2.

34.4.4 Bias Control

The bias is controlled by connecting external division resistors to LCD power supply pins VL1 to VL4 or by using the voltage multiplier. Figure 34.4 shows the Pin Connection and Voltage Levels when Division Resistors are Connected Externally. Figure 34.5 shows the Pin Connection and Voltage Levels when Voltage Multiplier is Used.

To connect division resistors externally, set the LVUPE bit to 0. Leave pins CL1 and CL2 open by setting the LSE60 bit to 1. These pins can also be used as I/O ports by setting the LSE60 bit to 0.

To use the voltage multiplier, set the LVUPE bit to 1. Select the reference voltage VL1 for the voltage multiplier to input externally or generate one internally by using the LVURS bit. Connect the voltage multiplier capacitor between pins CL1 and CL2. To generate the voltage internally, select the VL1 voltage value by setting bits LVLS0 to LVLS3. The wait time for the voltage multiplier is selected from the count source × 8 to count source × 64 using bits LVW0 and LVW1.

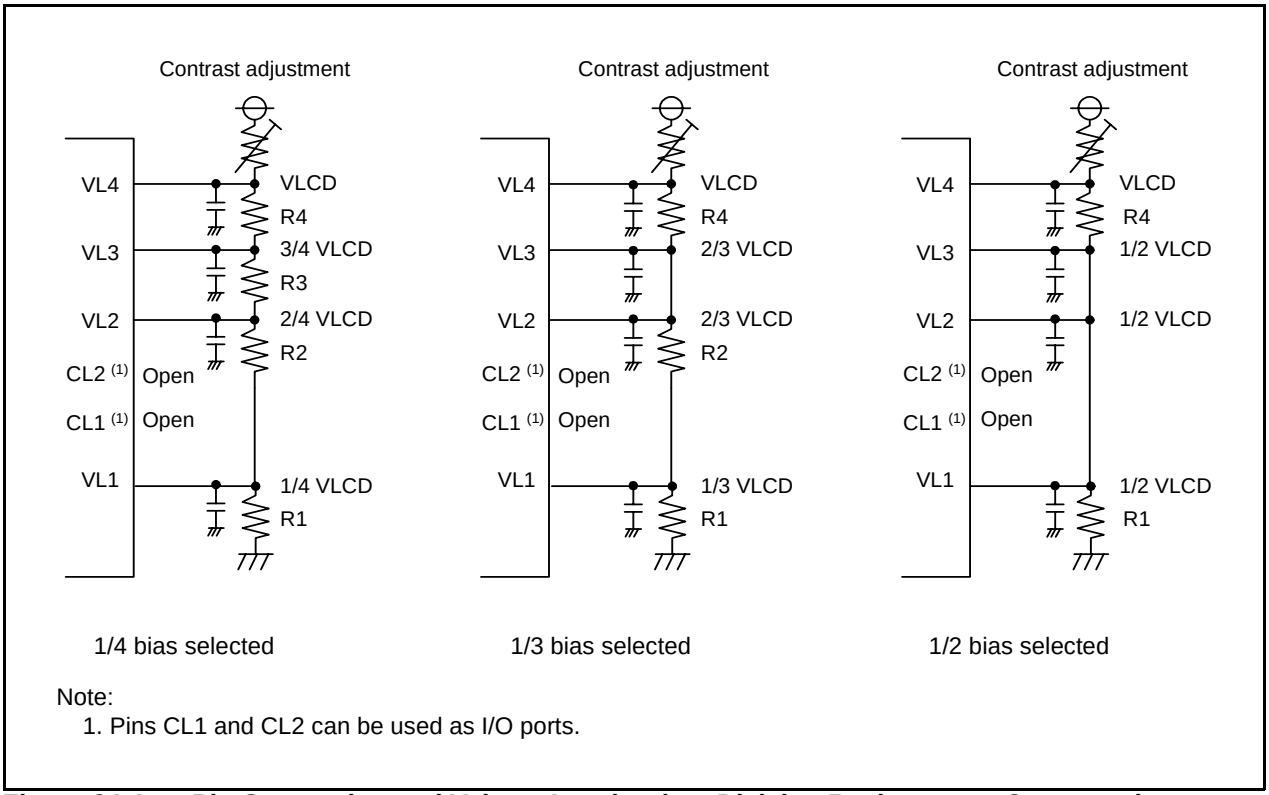
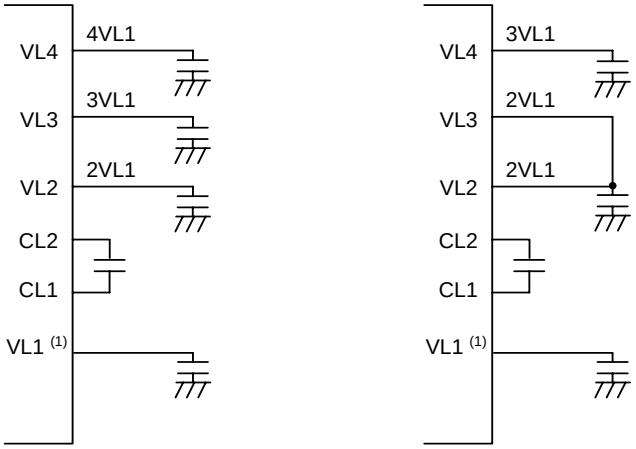


Figure 34.4 Pin Connection and Voltage Levels when Division Resistors are Connected Externally



Note:
1. When VL1 is generated internally (LVURS = 1).
When LVURS is 0, supply VL1 externally.

Figure 34.5 Pin Connection and Voltage Levels when Voltage Multiplier is Used

34.4.5 LCD Data Display

The bias is selected by setting bits LBAS0 and LBAS1, and the duty is selected by setting bits LDTY0 to LDTY2. Either a segment panel control waveform or a dot matrix panel control waveform is selected by setting the LWAV bit. An LCD display is enabled by setting the LDSPE bit to 1, and the display is started by setting LSTAT bit to 1.
The LCD display contents are changed by rewriting the contents of the LCD display data register and the LCR2 register.

34.4.6 Pin Status in Stop Mode

The status of the LCD display function pins selected by bits LSE00 to LSE60 in registers LSE0 to LSE7 are shown below. LCD control is restarted by means of the same operation as that used to make LCR0 register settings, as shown the LCD drive control procedure in Table 34.4.

Table 34.5 LCD Display Function Pin Status in Stop Mode

Pin Name	Pin Status
SEG0 to SEG55	Outputs a low-level signal.
COM0 to COM7	Outputs a low-level signal.
CL1 and CL2	Outputs a low-level signal.
VL1	• When external division resistors are used (the voltage multiplier is disabled by setting the LVUPE bit in the LCR1 register to 0) High-impedance state. • When the voltage multiplier is used with the VL1 externally-input voltage (the LVUPE bit is set to 1 and the LVURS bit is set to 0) High-impedance state. • When the voltage multiplier is used with the VL1 internally-generated voltage (the LVUPE bit is set to 1 and the LVURS bit is set to 1) Outputs the internally-generated voltage.
VL2 to VL4	High-impedance state

34.4.7 Pin Status in Power-Off Mode

The status of the LCD display function pins selected by bits LSE00 to LSE60 in registers LSE0 to LSE7 are shown in Table 34.6. The operation is started from a reset as shown in Table 34.4.

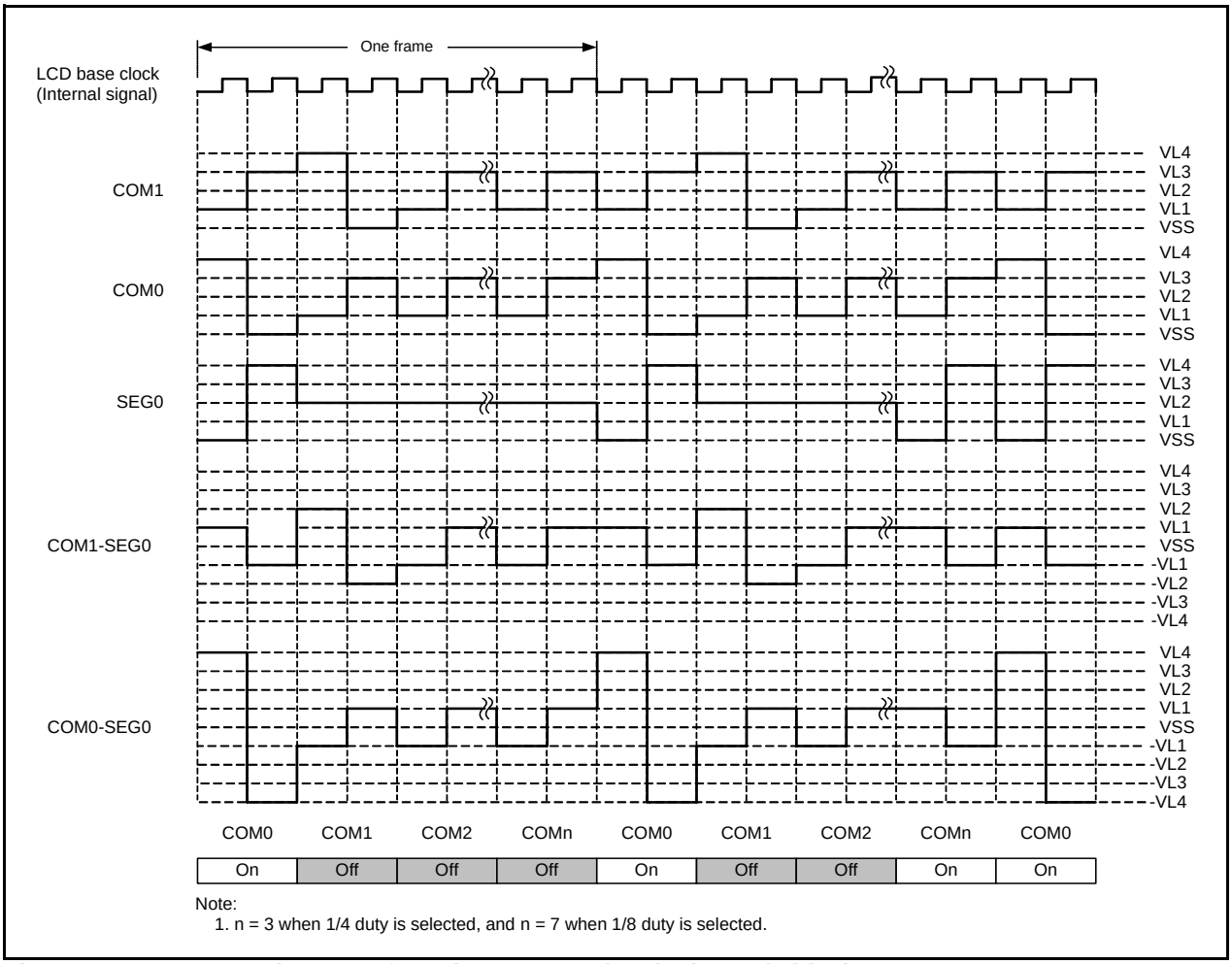
Table 34.6 LCD Display Function Pin Status in Power-Off Mode

Pin Name	Pin Status
SEG0 to SEG55	Outputs a low-level signal.
COM0 to COM7	
CL1 and CL2	High-impedance state
VL1 to VL4	High-impedance state

34.5 LCD Drive Waveform

34.5.1 Segment Panel Control Waveform

Figures 34.6 to 34.17 show the LCD drive waveform corresponding to each duty and bias for segment panel control (LWAV = 0).



Note:
1. n = 3 when 1/4 duty is selected, and n = 7 when 1/8 duty is selected.

Figure 34.6 LCD Drive Waveform (LWAV = 0, 1/4, 1/8 duty, 1/4 bias)

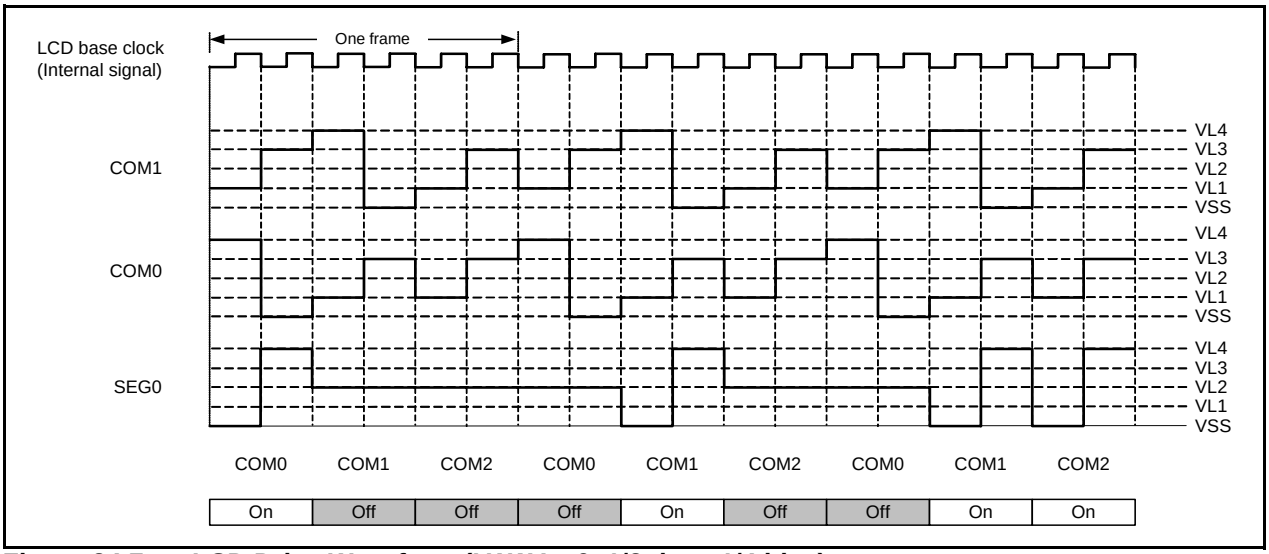


Figure 34.7 LCD Drive Waveform (LWAV = 0, 1/3 duty, 1/4 bias)

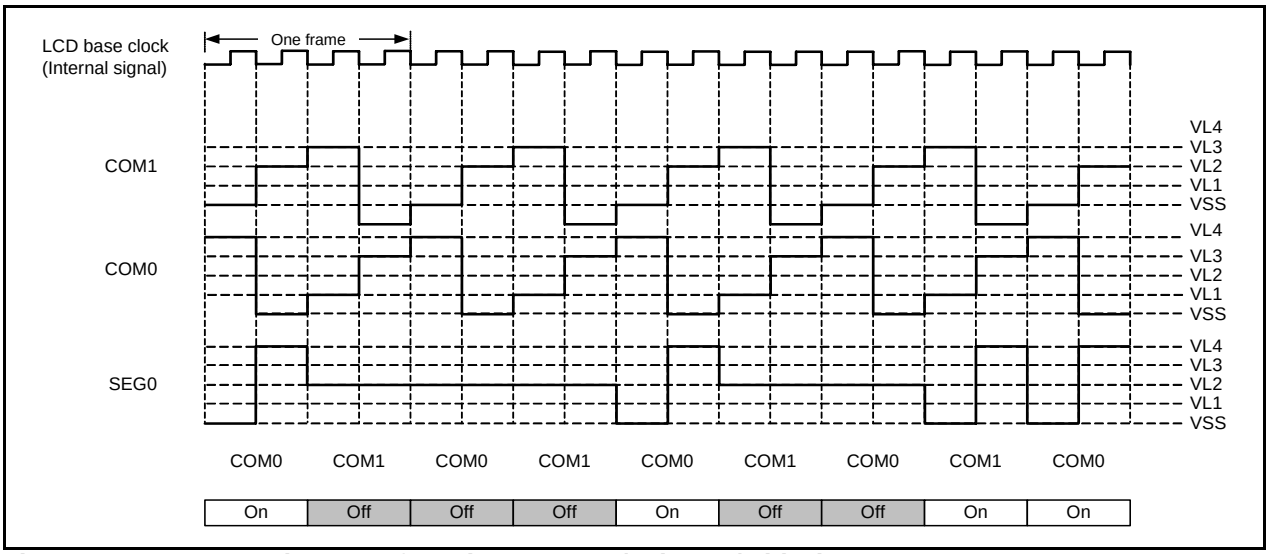


Figure 34.8 LCD Drive Waveform (LWAV = 0, 1/2 duty, 1/4 bias)

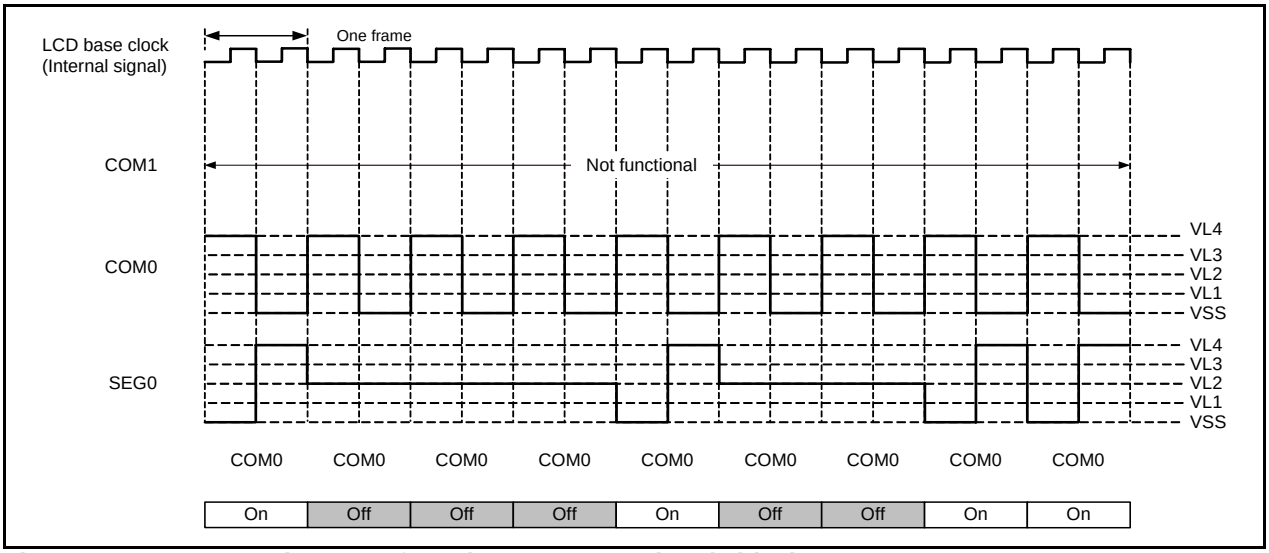
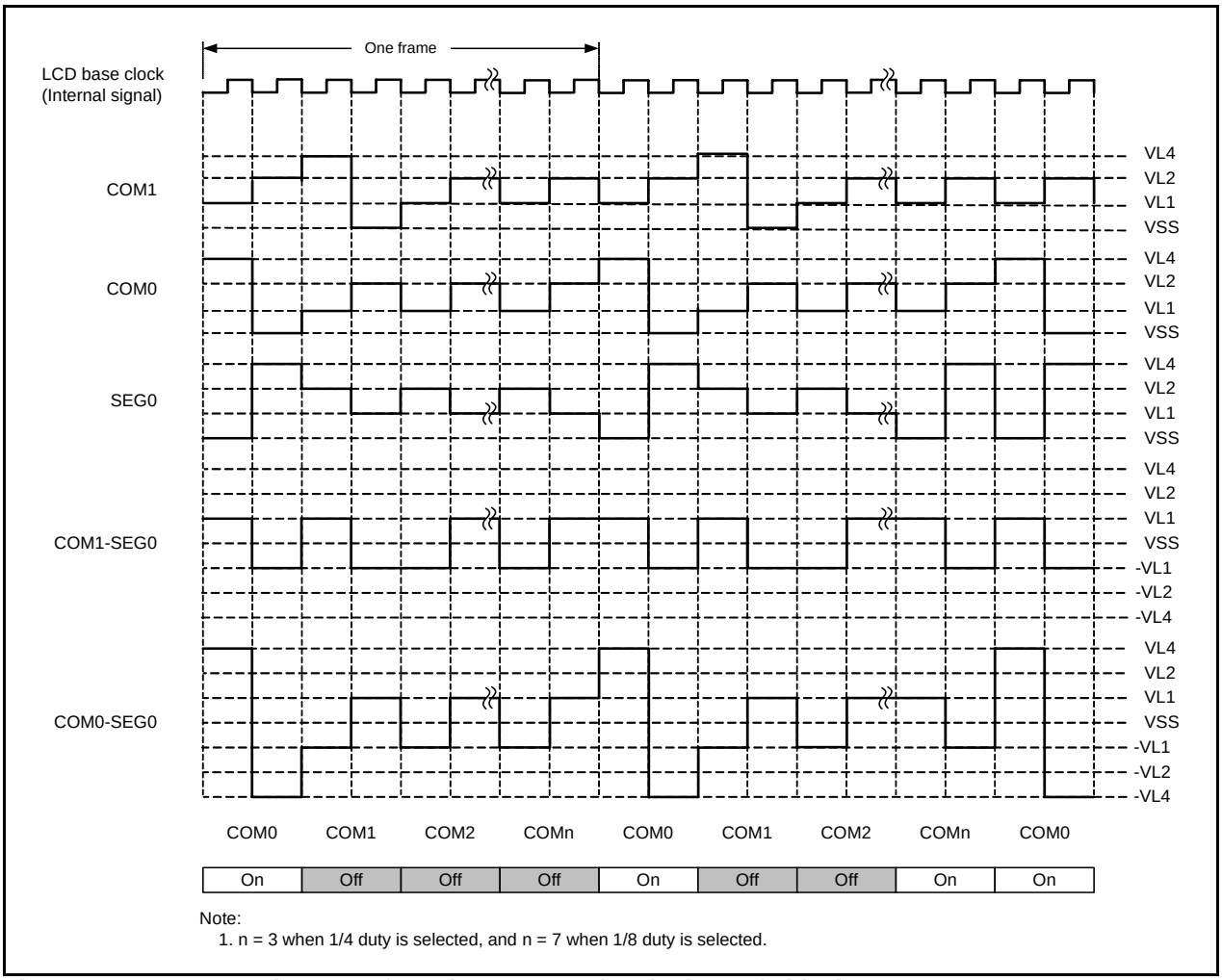


Figure 34.9 LCD Drive Waveform (LWAV = 0, Static, 1/4 bias)



Note:
1. n = 3 when 1/4 duty is selected, and n = 7 when 1/8 duty is selected.

Figure 34.10 LCD Drive Waveform (LWAV = 0, 1/4, 1/8 duty, 1/3 bias)

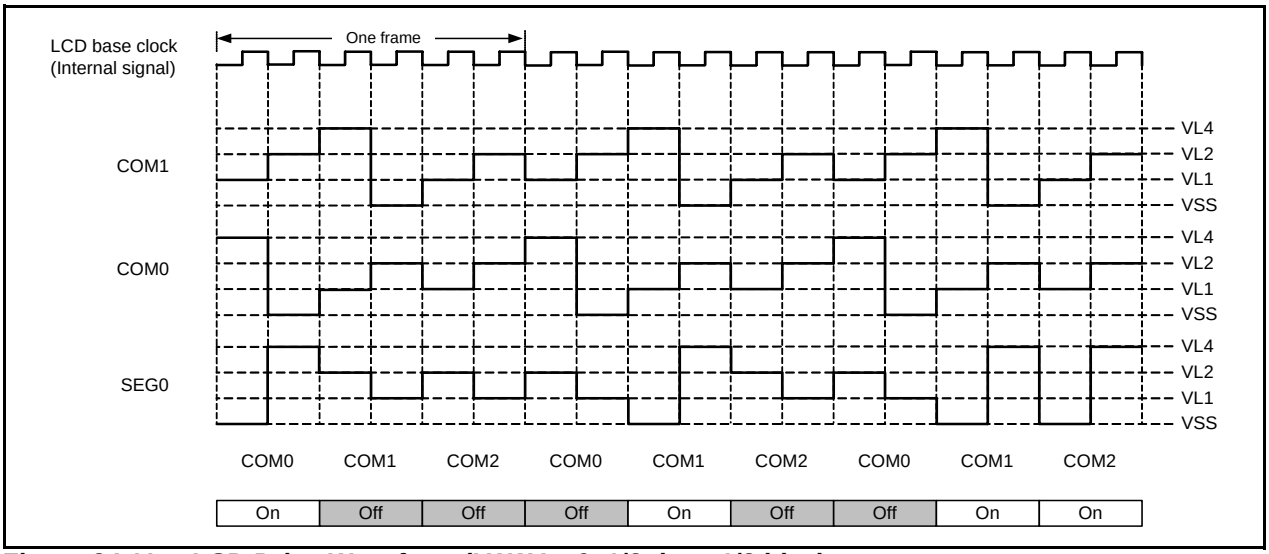


Figure 34.11 LCD Drive Waveform (LWAV = 0, 1/3 duty, 1/3 bias)

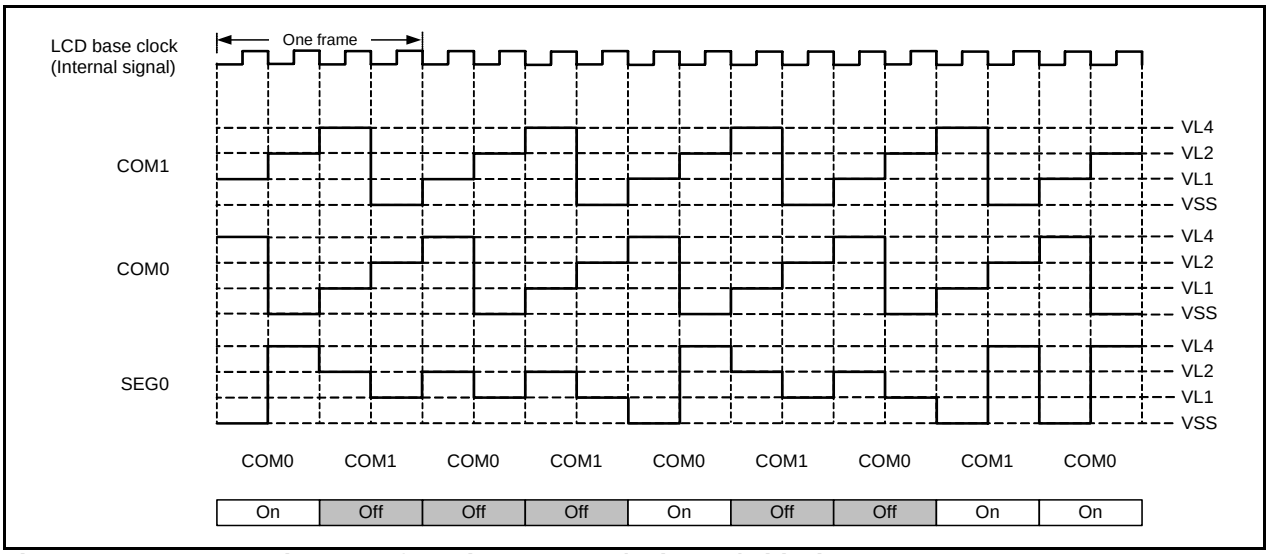


Figure 34.12 LCD Drive Waveform (LWAV = 0, 1/2 duty, 1/3 bias)

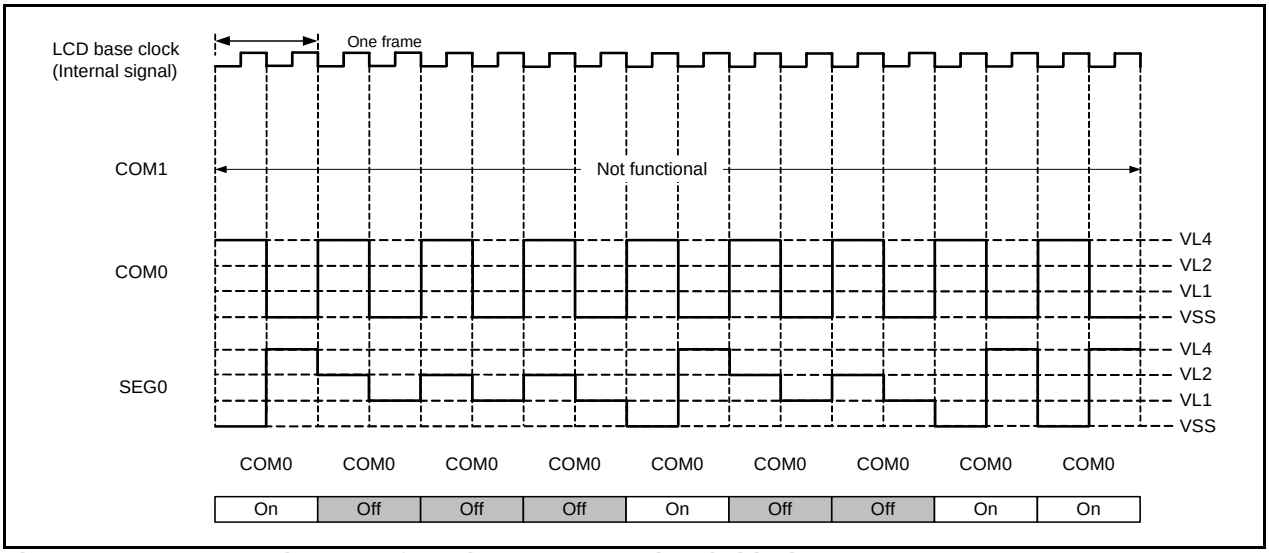
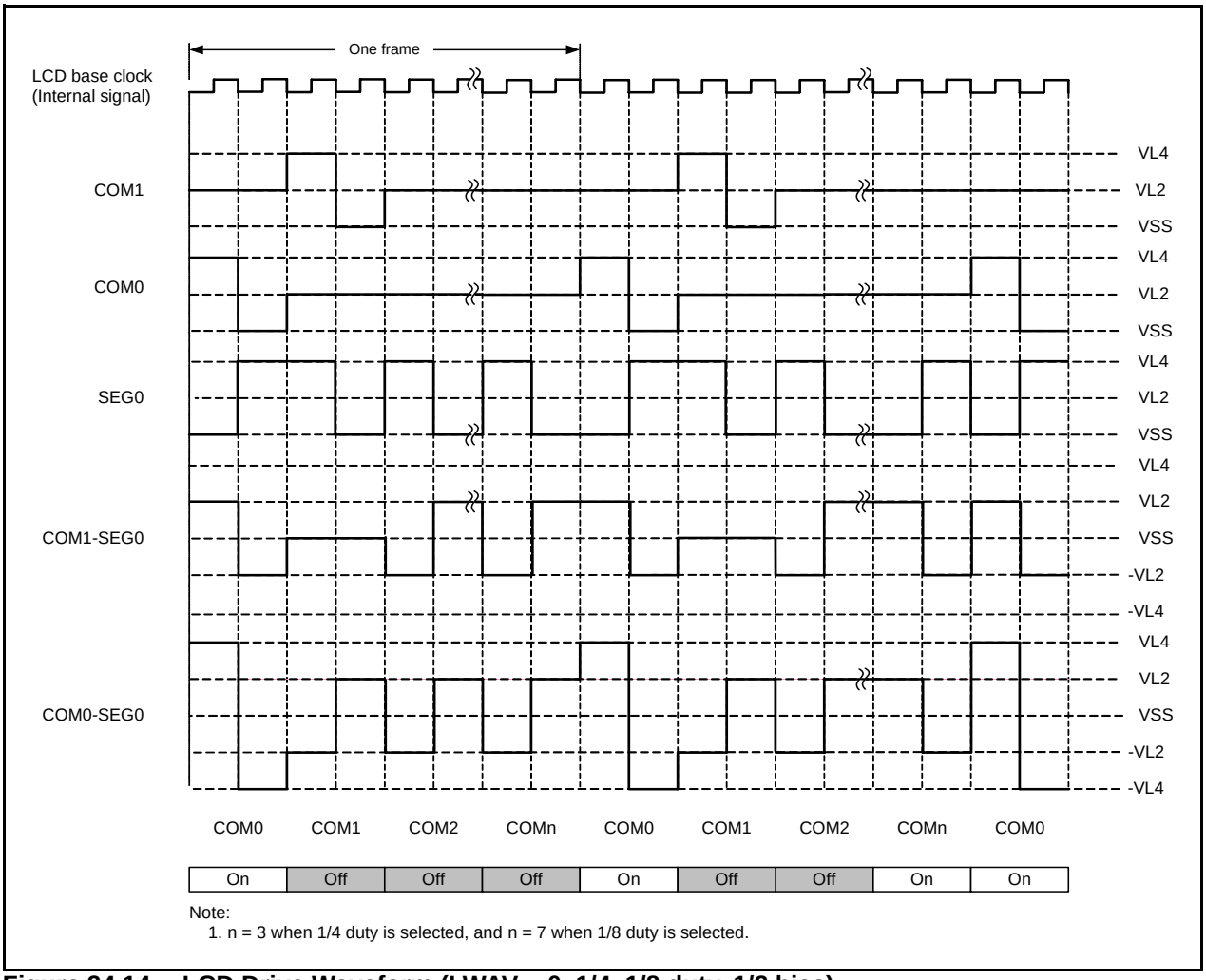


Figure 34.13 LCD Drive Waveform (LWAV = 0, Static, 1/3 bias)



Note:
1. n = 3 when 1/4 duty is selected, and n = 7 when 1/8 duty is selected.

Figure 34.14 LCD Drive Waveform (LWAV = 0, 1/4, 1/8 duty, 1/2 bias)

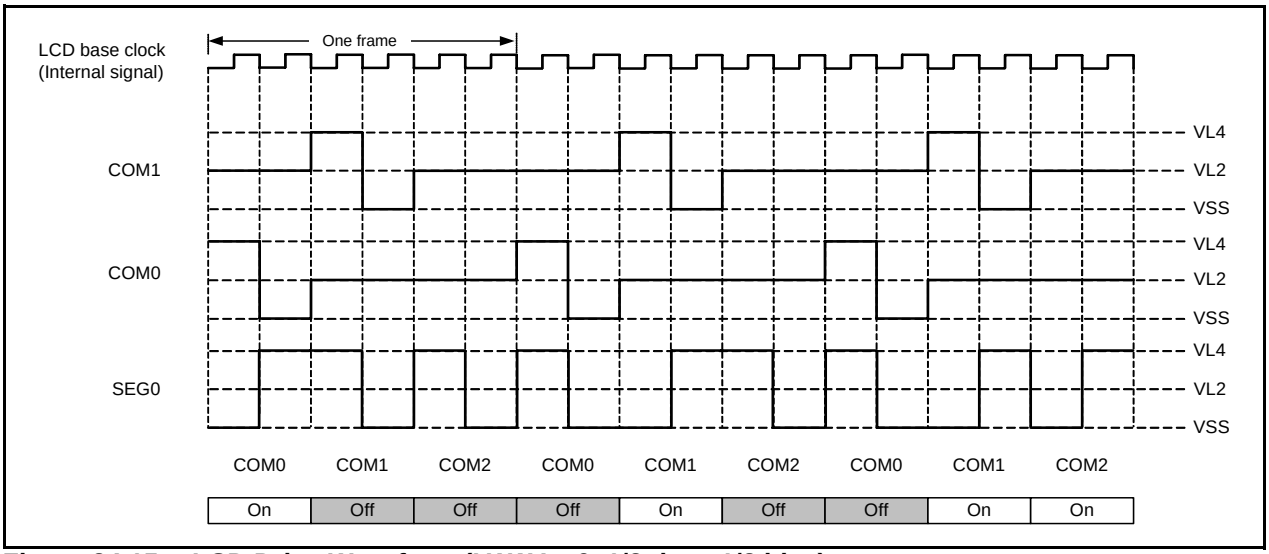


Figure 34.15 LCD Drive Waveform (LWAV = 0, 1/3 duty, 1/2 bias)

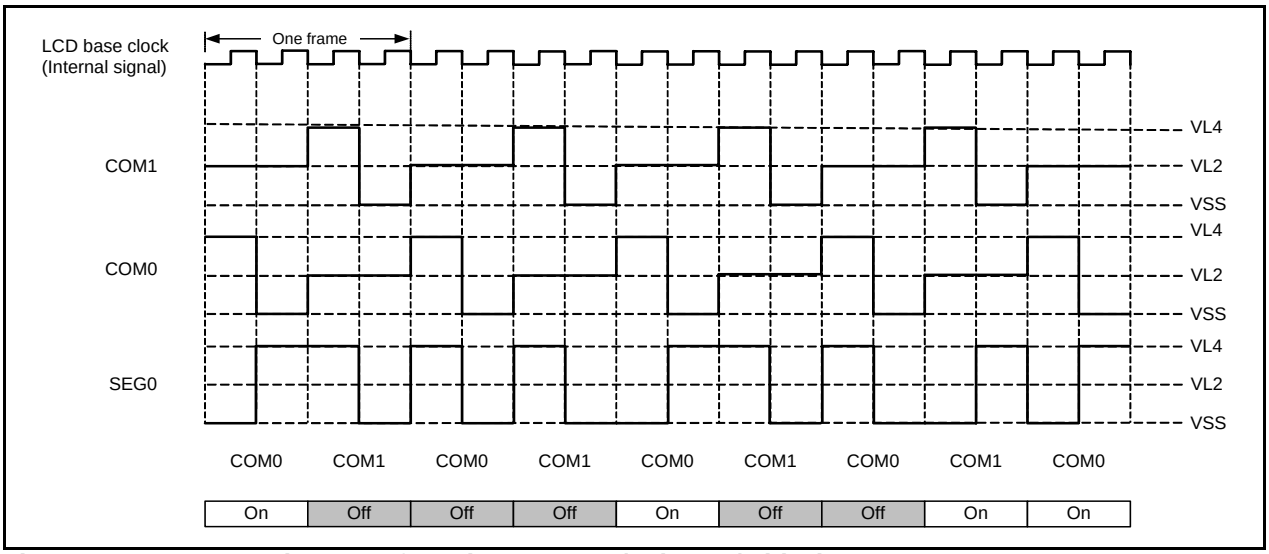


Figure 34.16 LCD Drive Waveform (LWAV = 0, 1/2 duty, 1/2 bias)

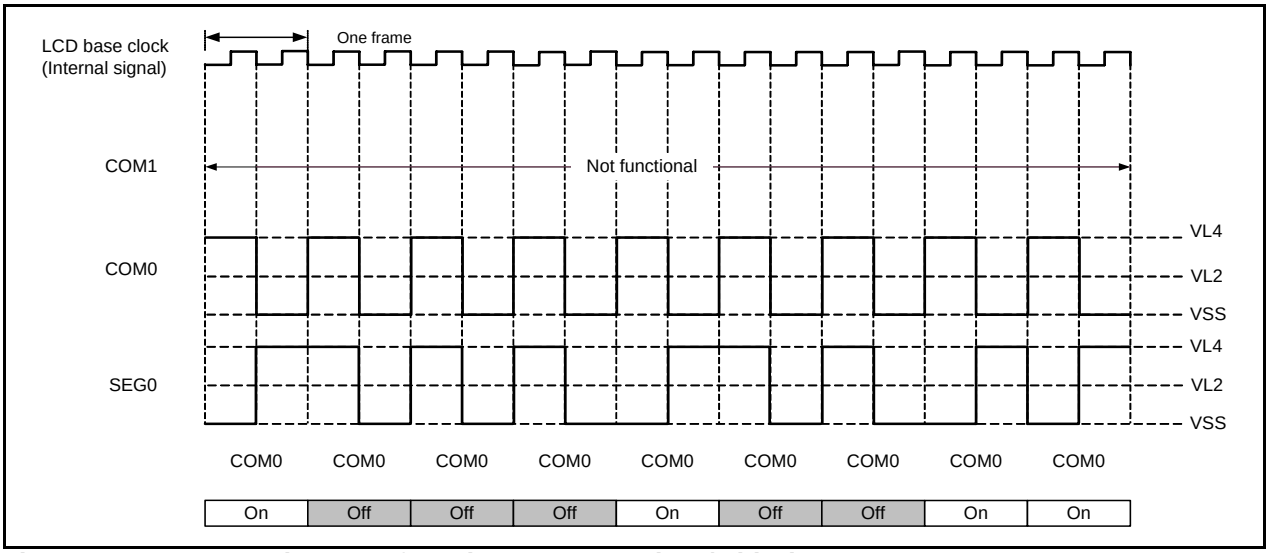
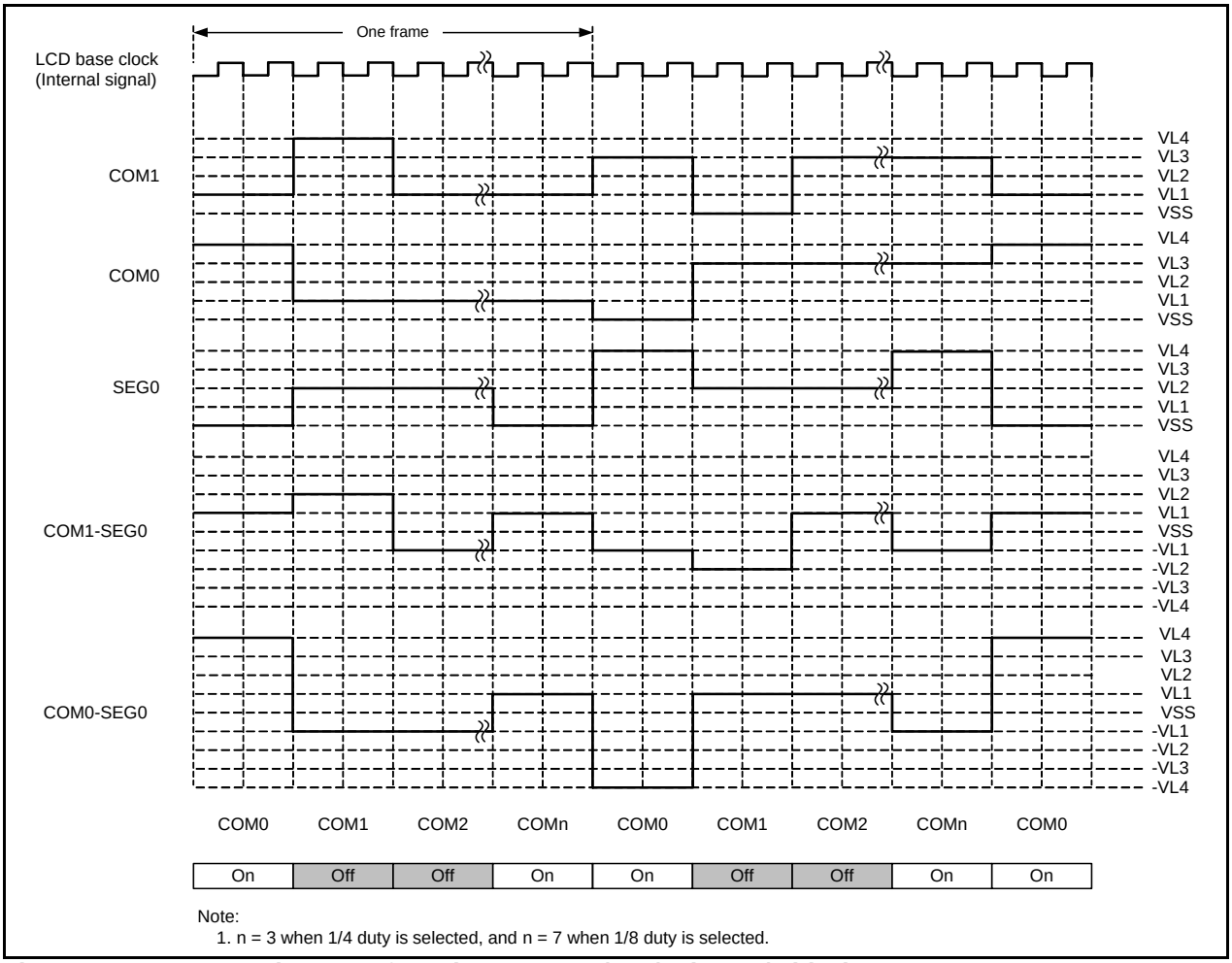


Figure 34.17 LCD Drive Waveform (LWAV = 0, Static, 1/2 bias)

34.5.2 Dot Matrix Panel Control Waveform

Figures 34.18 to 34.29 show the LCD drive waveform corresponding to each duty and bias for dot matrix panel control (LWAV = 1).



Note:
1. n = 3 when 1/4 duty is selected, and n = 7 when 1/8 duty is selected.

Figure 34.18 LCD Drive Waveform (LWAV = 1, 1/4, 1/8 duty, 1/4 bias)

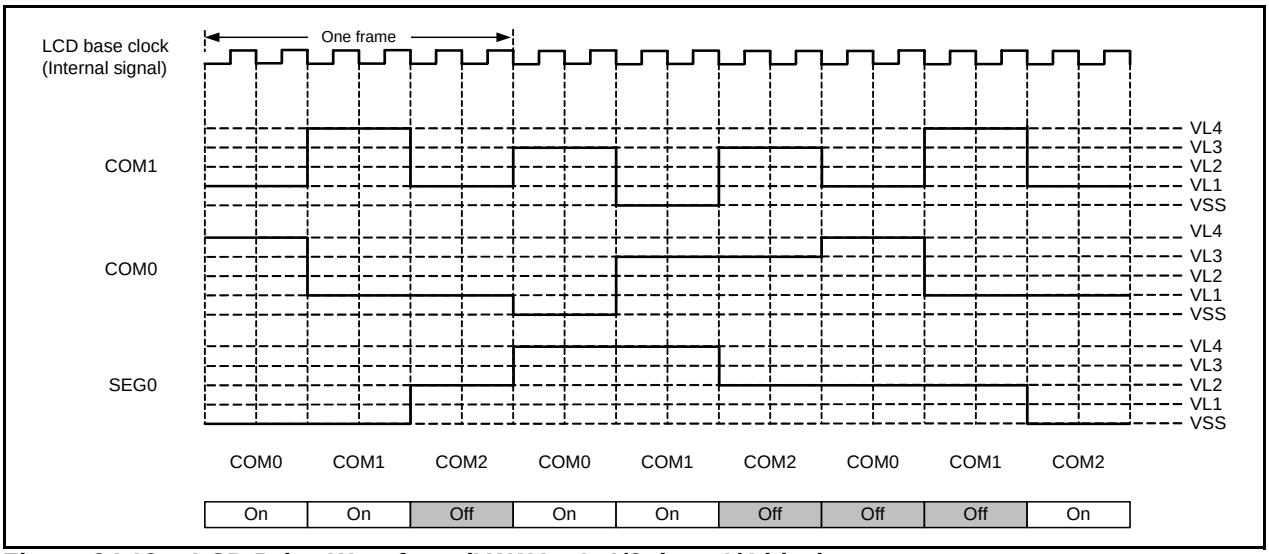


Figure 34.19 LCD Drive Waveform (LWAV = 1, 1/3 duty, 1/4 bias)

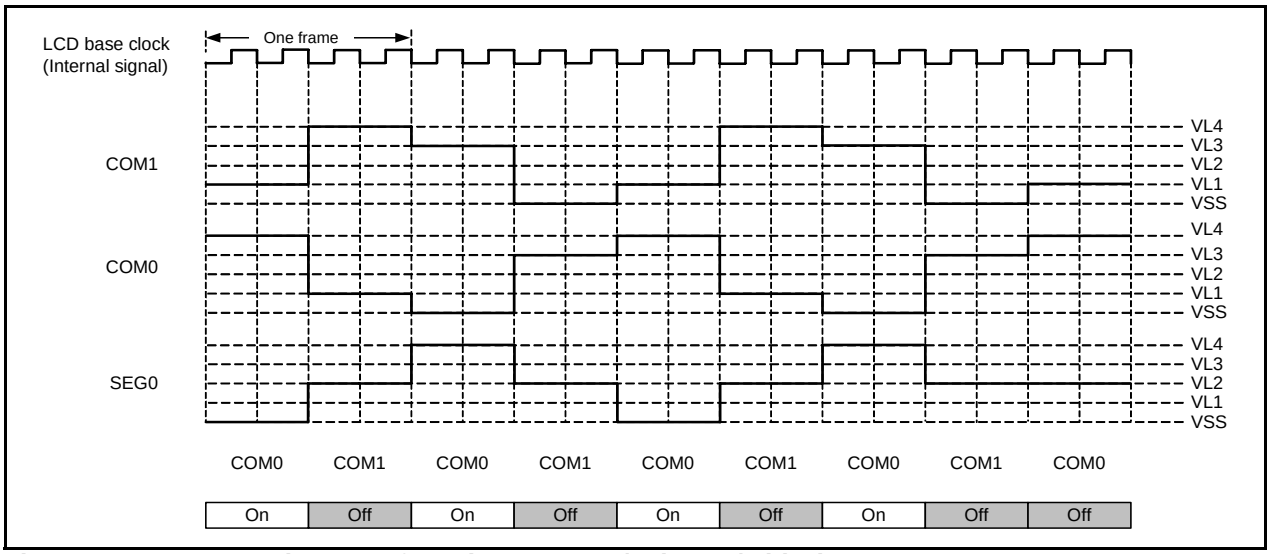


Figure 34.20 LCD Drive Waveform (LWAV = 1, 1/2 duty, 1/4 bias)

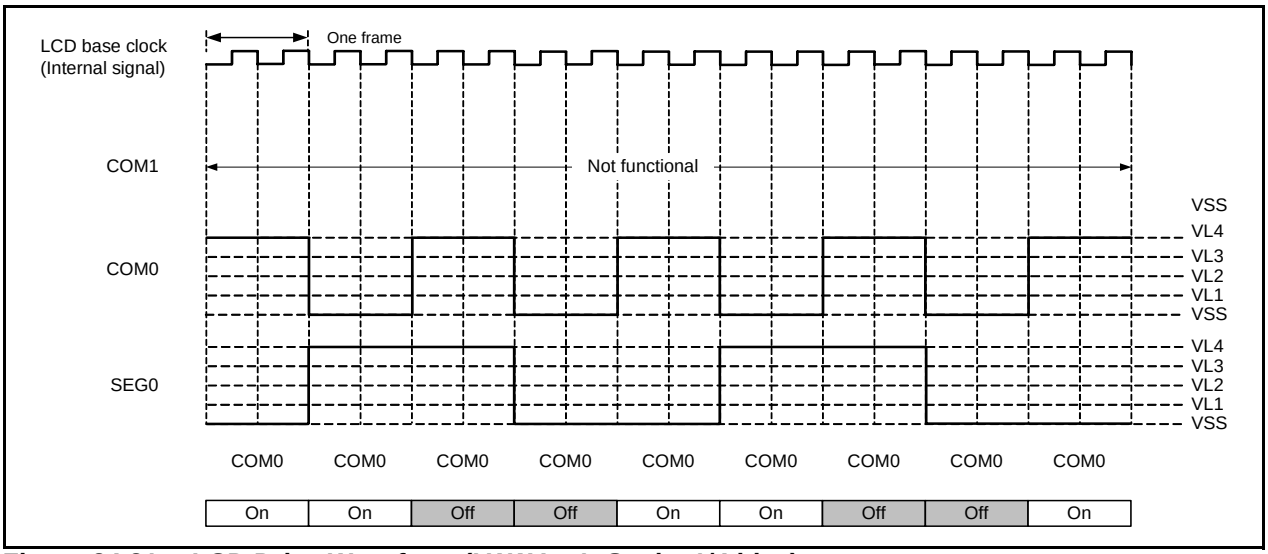
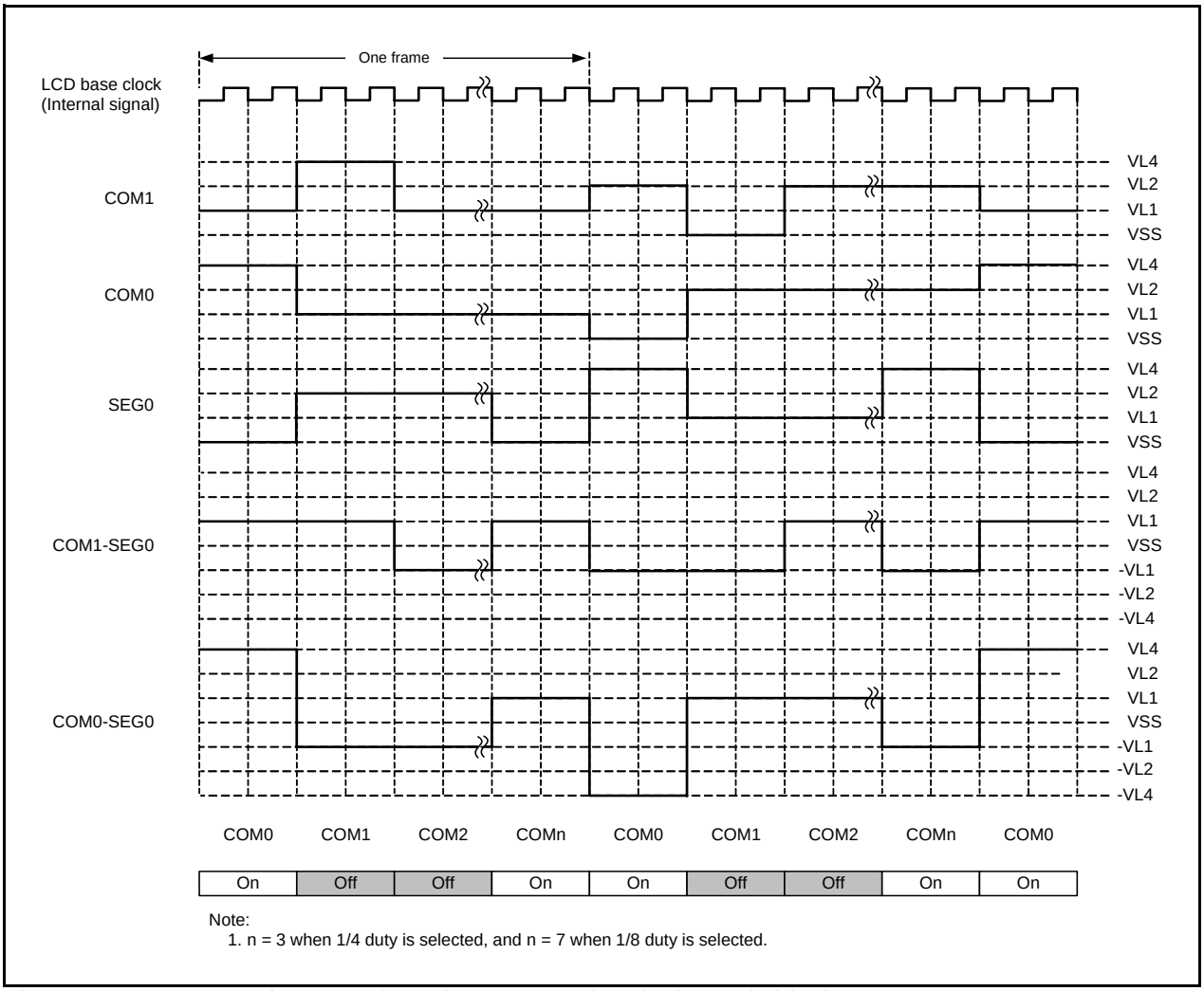


Figure 34.21 LCD Drive Waveform (LWAV = 1, Static, 1/4 bias)



Note:
1. n = 3 when 1/4 duty is selected, and n = 7 when 1/8 duty is selected.

Figure 34.22 LCD Drive Waveform (LWAV = 1, 1/4, 1/8 duty, 1/3 bias)

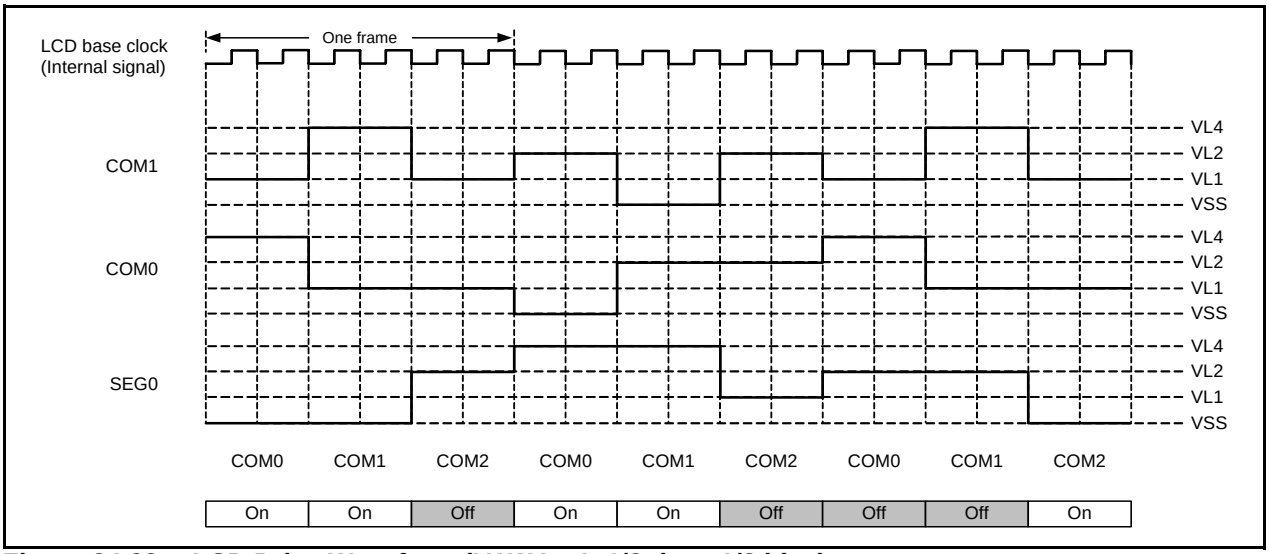


Figure 34.23 LCD Drive Waveform (LWAV = 1, 1/3 duty, 1/3 bias)

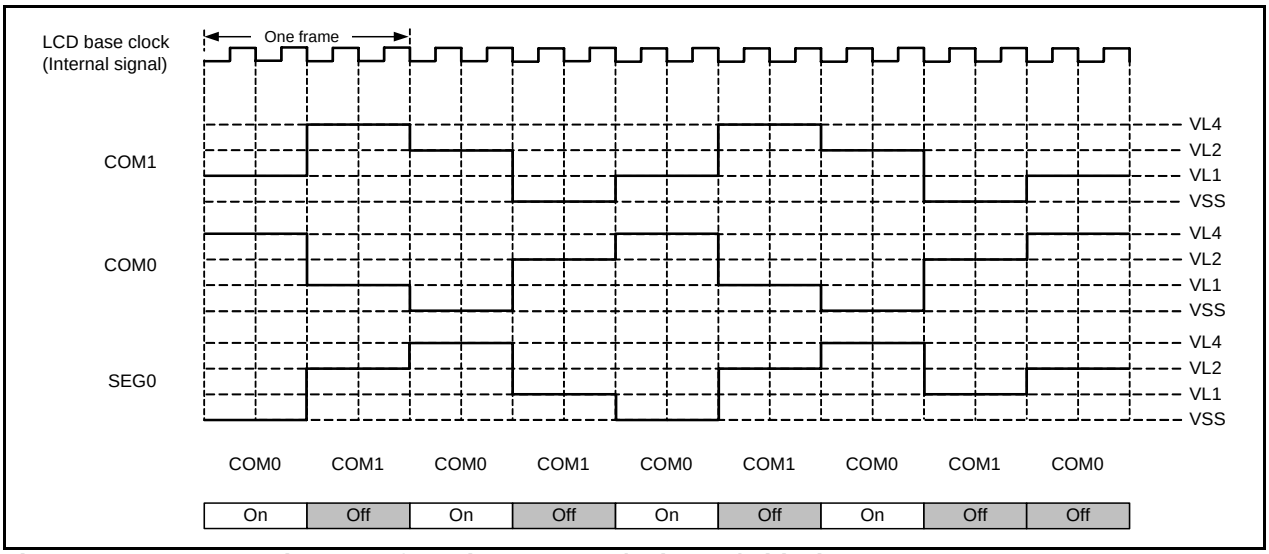


Figure 34.24 LCD Drive Waveform (LWAV = 1, 1/2 duty, 1/3 bias)

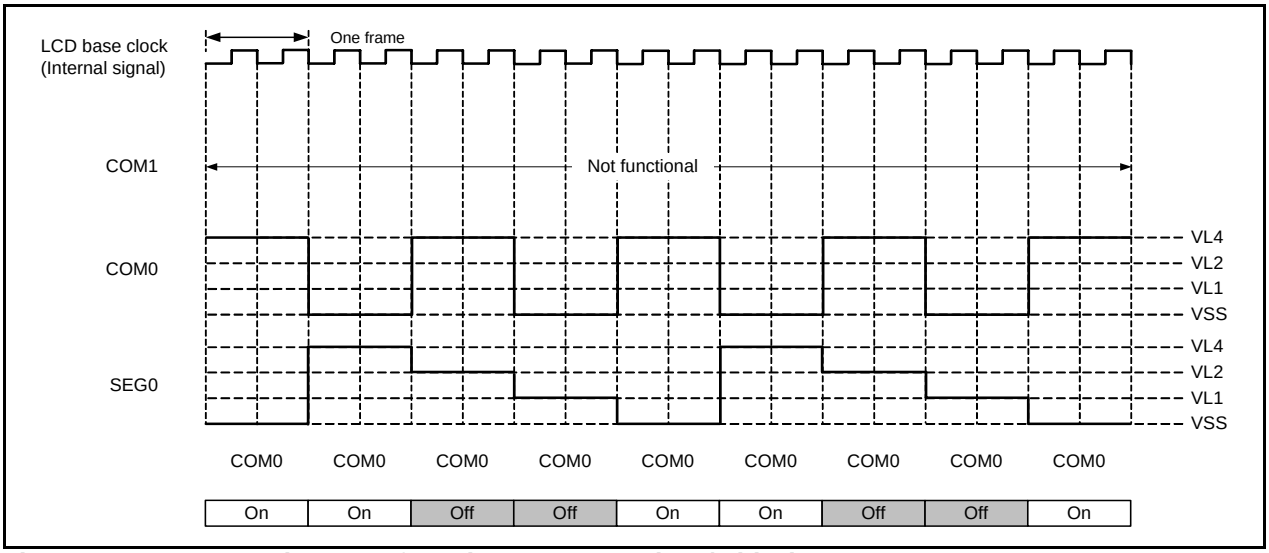
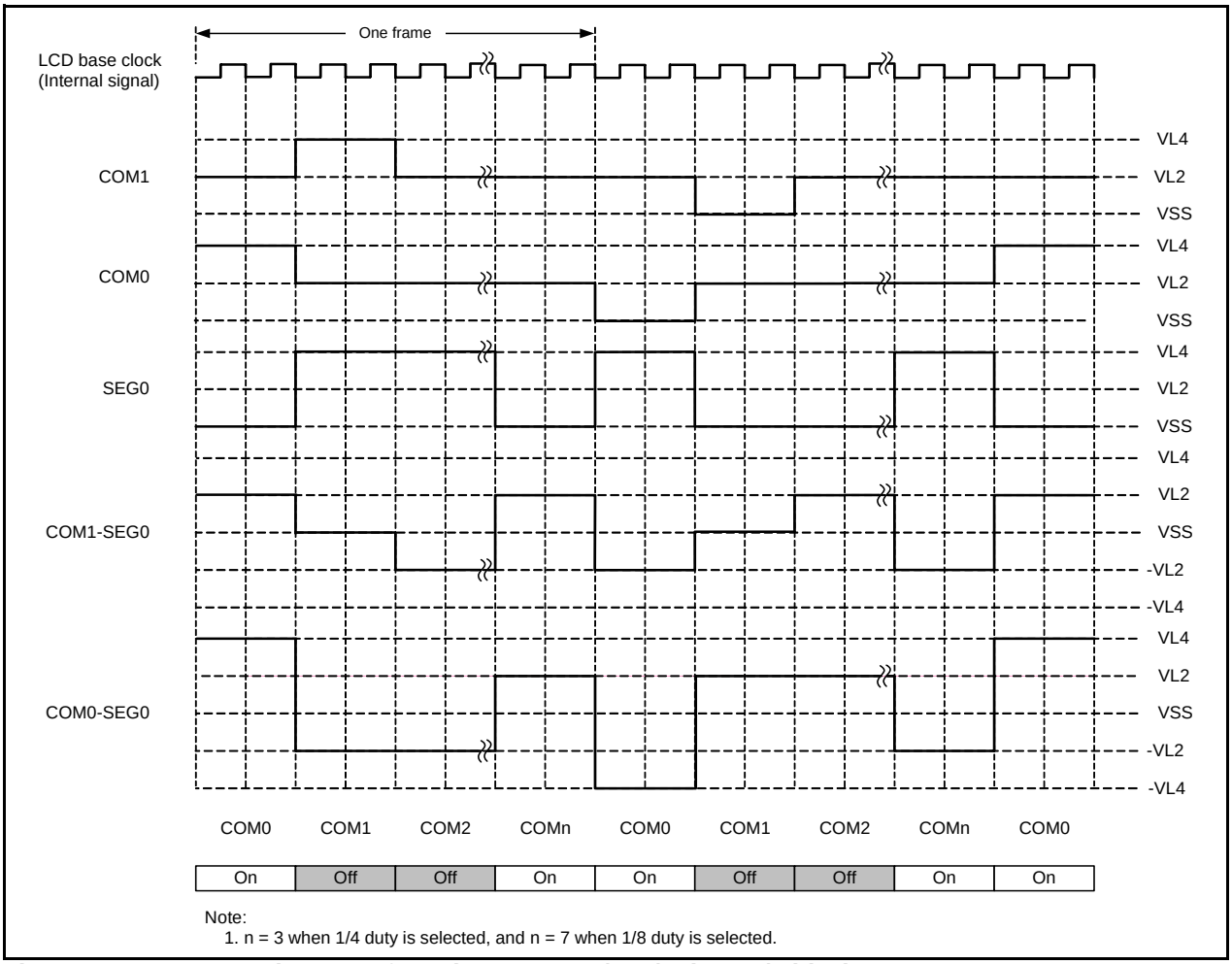


Figure 34.25 LCD Drive Waveform (LWAV = 1, Static, 1/3 bias)



Note:
1. n = 3 when 1/4 duty is selected, and n = 7 when 1/8 duty is selected.

Figure 34.26 LCD Drive Waveform (LWAV = 1, 1/4, 1/8 duty, 1/2 bias)

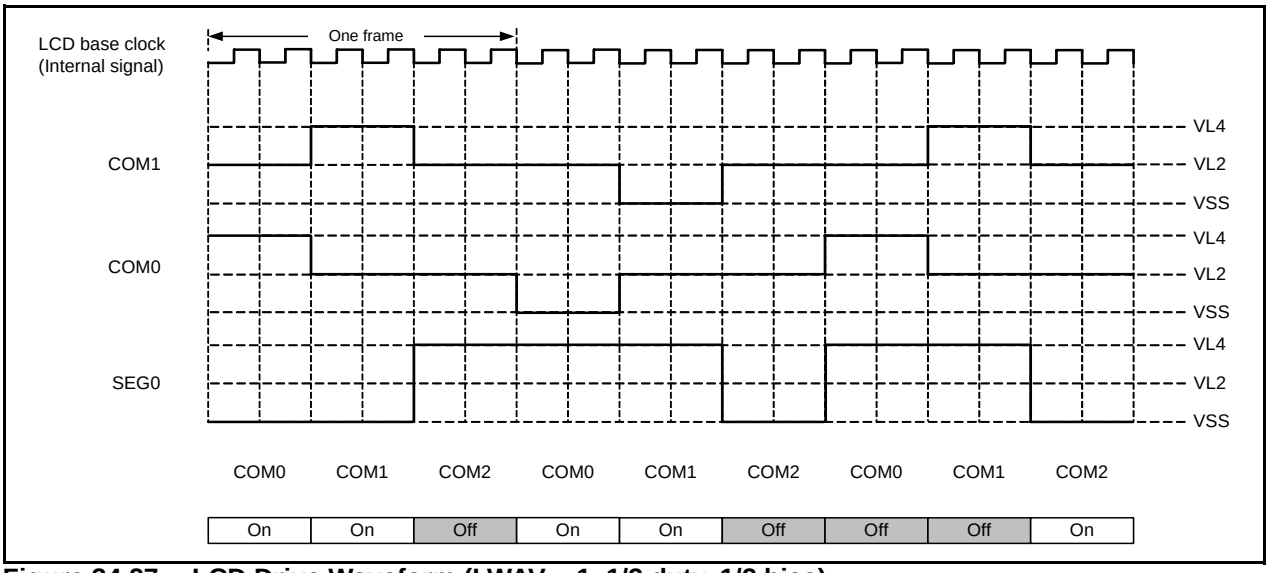


Figure 34.27 LCD Drive Waveform (LWAV = 1, 1/3 duty, 1/2 bias)

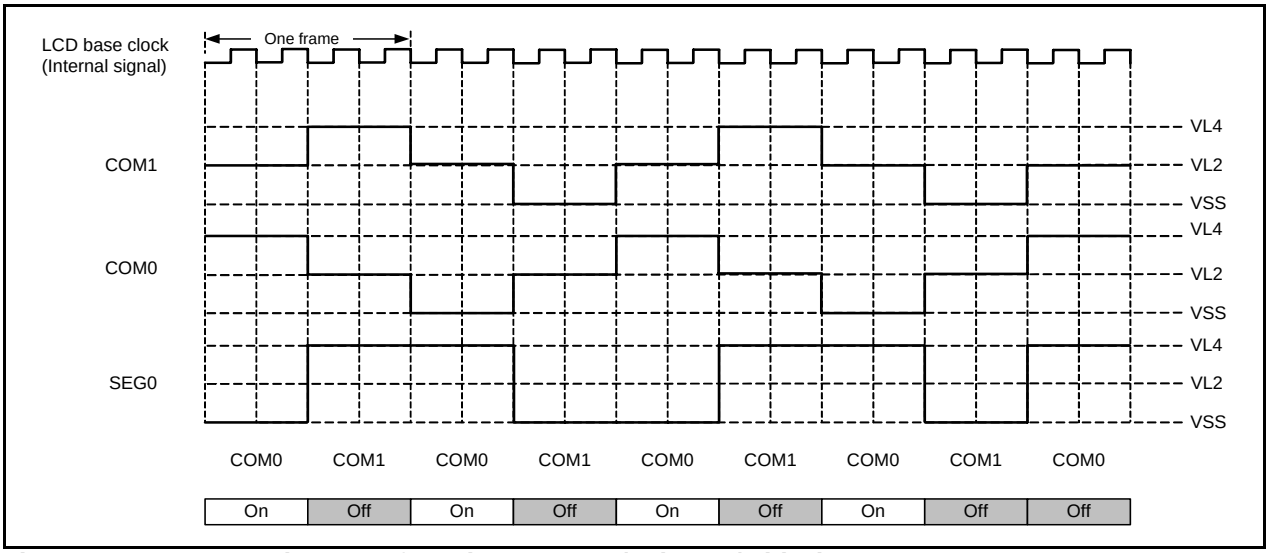


Figure 34.28 LCD Drive Waveform (LWAV = 1, 1/2 duty, 1/2 bias)

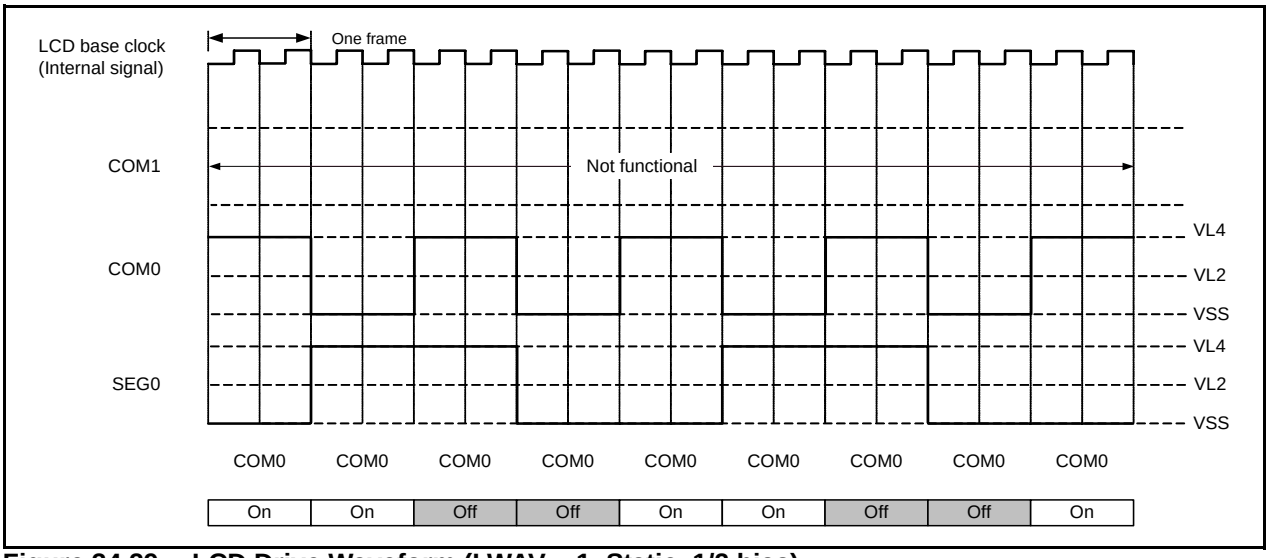


Figure 34.29 LCD Drive Waveform (LWAV = 1, Static, 1/2 bias)

34.6 Notes on LCD Drive Control Circuit

34.6.1 Voltage Multiplier

The voltage multiplier boosts the VL1 pin voltage by charging/discharging the capacitor connected between pins CL1 and CL2. As a result, the expected level from the VL4 pin may not achieved when driving a large LCD panel. An external power source is recommended to obtain a stable power supply in these cases.

34.6.2 When Division Resistors are Connected Externally

Set the resistor value between pins VL4 and VCC (the total of R1 to R4 as shown in Figure 34.4) to the highest value 100 kΩ or more.

35. Flash Memory

The flash memory can perform in the following three rewrite modes: CPU rewrite mode, standard serial I/O mode, and parallel I/O mode.

35.1 Introduction

Table 35.1 lists the Flash Memory Version Performance. (Refer to the specifications in **Table 1.1** and **Table 1.2** for items not listed in Table 35.1.)

Table 35.1 Flash Memory Version Performance

Item		Specification
Flash memory operating mode		3 modes (CPU rewrite, standard serial I/O, and parallel I/O)
Division of erase blocks		Refer to **Figure 35.1**.
Programming method		Byte units
Erasure method		Block erase
Programming and erasure control method (1)		Program and erase control by software commands
Rewrite control method	Blocks 0 to 6 (Program ROM)	Rewrite protect control in block units by the lock bit
	Blocks A, B, C, and D (Data flash)	Individual rewrite protect control on blocks A, B, C, and D by bits FMR14, FMR15, FMR16, and FMR17 in the FMR1 register
Number of commands		8 commands
Programming and erasure endurance (2)	Blocks 0 to 6 (Program ROM)	1,000 times
	Blocks A, B, C, and D (Data flash)	10,000 times
ID code check function		Standard serial I/O mode supported
ROM code protection		Parallel I/O mode supported

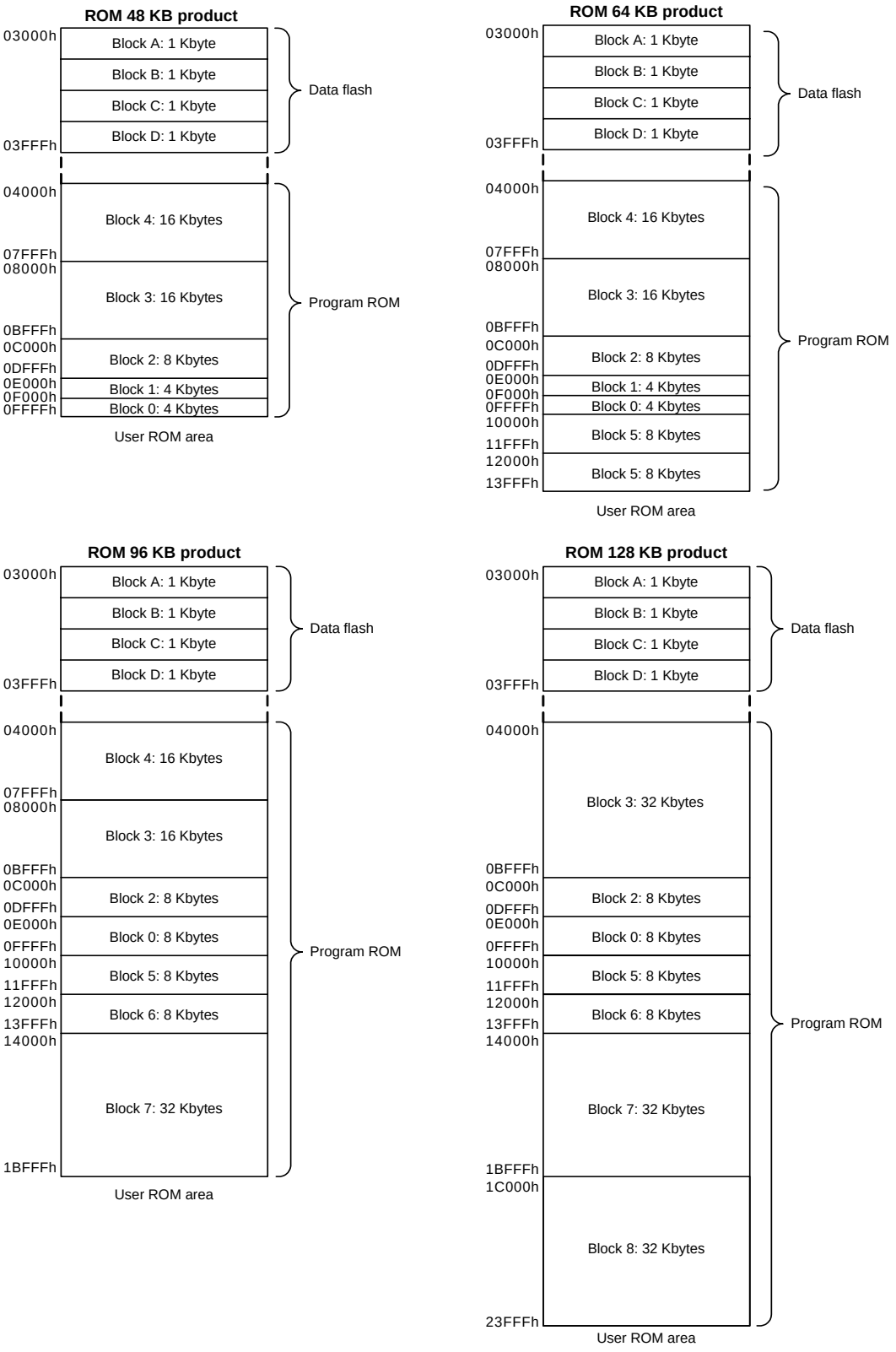
Notes:
1. To perform programming and erasure, use VCC = 2.7 V to 5.5 V as the supply voltage. Do not perform programming and erasure at less than 2.7 V.
2. Definition of programming and erasure endurance
   The programming and erasure endurance is defined on a per-block basis. If the programming and erasure endurance is n (n = 1,000 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1-Kbyte block, and then the block is erased, the programing/erasure endurance still stands at one. When performing 100 or more rewrites, the actual erase count can be reduced by executing program operations in such a way that all blank areas are used before performing an erase operation. Avoid rewriting only particular blocks and try to average out the programming and erasure endurance of the blocks. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.

Table 35.2 Flash Memory Rewrite Mode

Flash Memory Rewrite Mode	CPU Rewrite Mode	Standard Serial I/O Mode	Parallel I/O Mode
Function	User ROM area is rewritten by executing software commands from the CPU.	User ROM area is rewritten using a dedicated serial programmer.	User ROM area is rewritten using a dedicated parallel programmer.
Rewritable area	User ROM	User ROM	User ROM
Rewrite programs	User program	Standard boot program	–

35.2 Memory Map

The flash memory contains a user ROM area and a boot ROM area (reserved area).
Figures 35.1 shows the Flash Memory Block Diagrams of R8C/L35A, L36A, L38A, L3AA, R8C/L35B, L36B, L38B, and L3AB Groups.
The user ROM area contains program ROM and data flash.
Program ROM: Flash memory mainly used for storing programs
Data flash: Flash memory mainly used for storing data to be rewritten
(Data flash is not provided in the following groups: R8C/L35B, L36B, L38B, and L3AB.)
The user ROM area is divided into several blocks. The user ROM area can be rewritten in CPU rewrite mode, standard serial I/O mode, or parallel I/O mode.
The rewrite control program (standard boot program) for standard serial I/O mode is stored in the boot ROM area before shipment. The boot ROM area is allocated separately from the user ROM area.



Note:
1. Data flash is not provided in the following groups: R8C/L35B, L36B, L38B, and L3AB.

Figure 35.1 Flash Memory Block Diagrams of R8C/L35A, L36A, L38A, L3AA, R8C/L35B, L36B, L38B, and L3AB Groups

35.3 Functions to Prevent Flash Memory from being Rewritten

Standard serial I/O mode has an ID code check function, and parallel I/O mode has a ROM code protect function to prevent the flash memory from being read or rewritten easily.

35.3.1 ID Code Check Function

The ID code check function is used in standard serial I/O mode. Unless 3 bytes (addresses 0FFFCh to 0FFFEh) of the reset vector are set to FFFFFFh, the ID codes sent from the serial programmer or the on-chip debugging emulator and the 7-byte ID codes written in the flash memory are checked to see if they match. If the ID codes do not match, the commands sent from the serial programmer or the on-chip debugging emulator are not accepted. For details of the ID code check function, refer to **13. ID Code Areas**.

35.3.2 ROM Code Protect Function

The ROM protect function prevents the contents of the flash memory from being read, rewritten, or erased using the OFS register in parallel I/O mode.
Refer to **14. Option Function Select Area** for details of the OFS register.

The ROM code protect function is enabled by writing 1 to the ROMCR bit and writing 0 to the ROMCP1 bit. This prevents the content of the on-chip flash memory from being read or rewritten.
Once ROM code protection is enabled, the content of the internal flash memory cannot be rewritten in parallel I/O mode. To disable ROM code protection, erase the block including the OFS register using CPU rewrite mode or standard serial I/O mode.

35.3.3 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON	
When shipping	1	1	1	1	1	1	1	1	(Note 1)

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bit (2)	b5 b4	R/W
b5	VDSEL1		0 0: 3.80 V selected (Vdet0_3) 0 1: 2.85 V selected (Vdet0_2) 1 0: 2.35 V selected (Vdet0_1) 1 1: 1.90 V selected (Vdet0_0)	R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protection mode enabled after reset 1: Count source protection mode disabled after reset	R/W

Notes:
1. If the block including the OFS register is erased, the OFS register value is set to FFh.
2. The same level of the voltage detection 0 level selected by bits VDSEL0 and VDESL1 is set in both functions of voltage monitor 0 reset and power-on reset.
3. To use power-on reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

The OFS register is allocated in the flash memory. Write to this register with a program.
After writing, do not write additions to this register.

LVDAS Bit (Voltage Detection 0 Circuit Start Bit)

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

35.4 CPU Rewrite Mode

In CPU rewrite mode, the user ROM area can be rewritten by executing software commands from the CPU. Therefore, the user ROM area can be rewritten directly while the MCU is mounted on a board without using a ROM programmer. Execute the software command only to blocks in the user ROM area.
The flash module has an erase-suspend function which halts the erase operation temporarily during an erase operation in CPU rewrite mode. During erase-suspend, the user ROM area can be read by a program.
Erase-write 0 mode (EW0 mode) and erase-write 1 mode (EW1 mode) are available in CPU rewrite mode.
Table 35.3 lists the Differences between EW0 Mode and EW1 Mode.

Table 35.3 Differences between EW0 Mode and EW1 Mode

Item	EW0 Mode	EW1 Mode
Operating mode	Single-chip mode	Single-chip mode
Rewrite control program allocatable area	User ROM	User ROM
Rewrite control program executable areas	RAM (The rewrite control program must be transferred before being executed.) However, the program can be executed in the program ROM area when rewriting the data flash area.	User ROM or RAM
Rewritable area	User ROM	User ROM However, blocks which contain the rewrite control program are excluded.
Software command restrictions	Read status register command cannot be executed.	• Program and block erase commands cannot be executed to any block which contains the rewrite control program. • Read status register command cannot be executed.
Mode after program or block erase	Read array mode	Read array mode
CPU state during programming and block erasure	The CPU operates.	• The CPU operates while the data flash area is being programmed or block erased. • The CPU is put in a hold state while the program ROM area is being programmed or block erased. (I/O ports retain the states before the command execution).
Flash memory status detection	Read bits FST7, FMT5, and FMT4 in the FST register by a program.	Read bits FST7, FMT5, and FMT4 in the FST register by a program.
Conditions for entering program-suspend	• Set bits FMR20 and FMR21 in the FMR2 register to 1 by a program. • Set bits FMR20 and FMR22 in the FMR2 register to 1 and the enabled maskable interrupt is generated.	• Set bits FMR20 and FMR21 in the FMR2 register to 1 by a program (while rewriting the data flash area). • Set bits FMR20 and FMR22 in the FMR2 register to 1 and the enabled maskable interrupt is generated.
CPU clock	20 MHz	20 MHz

35.4.1 Flash Memory Status Register (FST)

Address 01B2h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	FST7	FST6	FST5	FST4	—	LBDATA	BSYAEI	RDYSTI
After Reset	1	0	0	0	0	X	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	RDYSTI	Flash ready status interrupt request flag (1)	0: No flash ready status interrupt request 1: Flash ready status interrupt request	R/W
b1	BSYAEI	Flash access error interrupt request flag (2)	0: No flash access error interrupt request 1: Flash access error interrupt request	R/W
b2	LBDATA	LBDATA monitor flag	0: Locked 1: Not locked	R
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	FST4	Program error status flag (3)	0: No program error 1: Program error	R
b5	FST5	Erase error status flag (3)	0: No erase error 1: Erase error	R
b6	FST6	Erase-suspend status flag	0: Other than erase-suspend 1: During erase-suspend	R
b7	FST7	Ready/busy status flag	0: Busy 1: Ready	R

Notes:
1. The RDYSTI bit cannot be set to 1 (flash ready status interrupt request) by a program. In parallel I/O mode, this bit is fixed to 0 (no flash ready status interrupt request).
2. The BSYAEI bit cannot be set to 1 (flash access error interrupt request) by a program. In parallel I/O mode, this bit is fixed to 0 (no flash access error interrupt request).
3. This bit is also set to 1 (error) when a command error occurs.

RDYSTI Bit (Flash Ready Status Flag Interrupt Request Flag)

When the RDYSTIE bit in the FMR0 register is set to 1 (flash ready status interrupt enabled) and auto-programming or auto-erasure completes, or erase-suspend mode is entered, the RDYSTI bit is set to 1 (flash ready status interrupt request).
During interrupt handling, set the RDYSTI bit to 0 (no flash ready status interrupt request).

[Condition for setting to 0]
Set to 0 by an interrupt handling program.
[Condition for setting to 1]
When the flash memory status changes from busy to ready while the RDYSTIE bit in the FRMR0 register is set to 1, the RDYSTI bit is set to 1.
The status is changed from busy to ready by the following operations: erasing/writing to the flash memory, suspend acknowledgement, forcible termination, completion of the lock bit program, and completion of the read lock bit status.

BYSAEI Bit (Flash Access Error Interrupt Request Flag)

The BYSAEI bit is set to 1 (flash access error interrupt request) when the BSYAEIE bit in the FMR0 register is set to 1 (flash access error interrupt enabled) and the block during auto-programming/auto-erasure is accessed. This bit is also set to 1 if an erase or program error occurs when the CMDERIE bit in the FMR0 register is set to 1 (erase/write error interrupt enabled).
During interrupt handling, set the BSYAEI bit to 0 (no flash access error interrupt request).

[Conditions for setting to 0]
(1) Set to 0 by an interrupt handling program.
(2) Execute the status clear instruction.
[Conditions for setting to 1]
(1) Read or write the area that is being erased/written when the BSYAEIE bit in the FRMR0 register is set to 1 and while the flash memory is busy.
Or, read the data flash area while erasing/writing to the program ROM area. (Note that the read value is undefined in both cases. Writing has no effect.)
(2) If an erase or program error occurs when the CMDERIE bit in the FMR0 register is set to 1 (erase/write error interrupt enabled).

LBDATA Bit (LBDATA Monitor Flag)

This is a read-only bit indicating the lock bit status. To confirm the lock bit status, execute the read lock bit status command and read the LBDATA bit after the FST7 bit is set to 1 (ready).
The condition for updating this bit is when the program, erase, read lock bit status commands are generated.
When the read lock bit status command is input, the FST7 bit is set to 0 (busy). At the time when the FST7 bit is set to 1 (ready), the lock bit status is stored in the LBDATA bit. The data in the LBDATA bit is retained until the next command is input.

FST4 Bit (Program Error Status Flag)

This is a read-only bit indicating the auto-programming status. The bit is set to 1 if a program error occurs; otherwise, it is set to 0. For details, refer to the description in **35.4.17 Full Status Check**.

FST5 Bit (Erase Error Status Flag)

This is a read-only bit indicating the status of auto-programming or the blank check command. The bit is set to 1 if an erase error or blank check error occurs; otherwise, it is set to 0. Refer to **35.4.17 Full Status Check** for details.

FST6 Bit (Erase Suspend Status Flag)

This is a read-only bit indicating the suspend status. The bit is set to 1 when an erase-suspend request is acknowledged and a suspend status is entered; otherwise, it is set to 0.

FST7 Bit (Ready/Busy Status Flag)

This is a read-only bit indicating the operating status of the flash memory. The bit is set to 0 during program and erase operations; otherwise, it is set to 1.

35.4.2 Flash Memory Control Register 0 (FMR0)

Address 01B4h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RDYSTIE	BSYAEIE	CMDERIE	CMDRST	FMSTP	FMR02	FMR01	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bit	Set to 0.	R/W
b1	FMR01	CPU rewrite mode select bit (1)	0: CPU rewrite mode disabled 1: CPU rewrite mode enabled	R/W
b2	FMR02	EW1 mode select bit (1)	0: EW0 mode 1: EW1 mode	R/W
b3	FMSTP	Flash memory stop bit (2)	0: Flash memory operates 1: Flash memory stops (Low-power consumption state, flash memory initialization)	R/W
b4	CMDRST	Erase/write sequence reset bit (3)	When the CMDRST bit is set to 1, the erase/write sequence is reset and erasure/writing can be forcibly stopped. When read, the content is 0.	R/W
b5	CMDERIE	Erase/write error interrupt enable bit	0: Erase/write error interrupt disabled 1: Erase/write error interrupt enabled	R/W
b6	BSYAEIE	Flash access error interrupt enable bit	0: Flash access error interrupt disabled 1: Flash access error interrupt enabled	R/W
b7	RDYSTIE	Flash ready status interrupt enable bit	0: Flash ready status interrupt disabled 1: Flash ready status interrupt enabled	R/W

Notes:
1. To set this bit to 1, first write 0 and then 1 immediately. Do not generate an interrupt between writing 0 and writing 1.
2. Write to the FMSTP bit by a program transferred to the RAM. The FMSTP bit is enabled when the FMR01 bit is set to 1 (CPU rewrite mode enabled). To set the FMSTP bit to 1 (flash memory stops), set it when the FST7 bit in the FST register is set to 1 (ready).
3. The CMDRST bit is enabled when the FMR01 bit is set to 1 (CPU rewrite mode enabled) and the FST7 bit in the FST register is set to 0 (busy).

FMR01 Bit (CPU Rewrite Mode Select Bit)

When the FMR01 bit is set to 1 (CPU rewrite mode enabled), the MCU is made ready to accept software commands.

FMR02 Bit (EW1 Mode Select Bit)

When the FMR02 bit is set to 1 (EW1 mode), EW1 mode is selected.

FMSTP Bit (Flash Memory Stop Bit)

This bit is used to initialize the flash memory control circuits, and also to reduce the amount of current consumed by the flash memory. Access to the flash memory is disabled by setting the FMSTP bit to 1.
Write to the FMSTP bit by a program transferred to the RAM.
To reduce the power consumption further in high-speed on-chip oscillator mode, low-speed on-chip oscillator mode (XIN clock stopped), and low-speed clock mode (XIN clock stopped), set the FMSTP bit to 1. Refer to **10.7.10 Stopping Flash Memory** for details.
When entering stop mode or wait mode while CPU rewrite mode is disabled, the FMR0 register does not need to be set because the power for the flash memory is automatically turned off and is turned back on when exiting stop or wait mode.

CMDRST Bit (Erase/Write Sequence Reset Bit)

This bit is used to initialize the flash memory sequence and forcibly stop a program or erase command. The user ROM area can be read while the flash memory sequence is being initialized.
For addresses and blocks which the program or erase command is forcibly stopped by the CMDRST bit, execute a block erasure again and ensure it completes normally.
The time from when the command is forcibly stopped and until reading is enabled is some hundreds μs where the suspend response time is 10 ms.

CMDERIE Bit (Erase/Write Interrupt Enable Bit)

This bit enables an flash command error interrupt to be generated if a program or block erase error occurs. When the CMDERIE bit is set to 1 (erase/write error interrupt enabled) and erasure/writing is performed, an interrupt is generated if an erase or program error occurs.
If a flash command error interrupt is generated, execute the clear status register command during interrupt handling.

BSYAEIE Bit (Flash Access Error Interrupt Enable Bit)

This bit enables a flash access error interrupt to be generated if the flash memory during rewriting is accessed.

RDYSTIE Bit (Flash Ready Status Interrupt Enable Bit)

This bit enables a flash ready status error interrupt to be generated when the status of the flash memory sequence changes from the busy to ready status.

35.4.3 Flash Memory Control Register 1 (FMR1)

Address 01B5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	FMR17	FMR16	FMR15	FMR14	FMR13	FMR12	FMR11	FMR10
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FMR10	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	FMR11			—
b2	FMR12			—
b3	FMR13	Lock bit disable select bit (1)	0: Lock bit enabled 1: Lock bit disabled	R/W
b4	FMR14	Data flash block A rewrite disable bit (2)	0: Rewrite enabled (software command acceptable) 1: Rewrite disabled (software command not acceptable, no error occurred)	R/W
b5	FMR15	Data flash block B rewrite disable bit (2)	0: Rewrite enabled (software command acceptable) 1: Rewrite disabled (software command not acceptable, no error occurred)	R/W
b6	FMR16	Data flash block C rewrite disable bit (2)	0: Rewrite enabled (software command acceptable) 1: Rewrite disabled (software command not acceptable, no error occurred)	R/W
b7	FMR17	Data flash block D rewrite disable bit (2)	0: Rewrite enabled (software command acceptable) 1: Rewrite disabled (software command not acceptable, no error occurred)	R/W

Notes:
1. To set the FMR13 bit to 1, first write 0 and then 1 immediately. Do not generate an interrupt between writing 0 and writing 1.
2. To set this bit to 0, first write 1 and then 0 immediately. Do not generate an interrupt between writing 1 and writing 0.

FMR13 Bit (Lock Bit Disable Select Bit)

When the FMR13 bit is set to 1 (lock bit disabled), the lock bit is disabled. When the FMR13 bit is set to 0, the lock bit is enabled. Refer to **35.4.10 Data Protect Function** for the details of the lock bit.
The FMR13 bit enables the lock bit function only and the lock bit data does not change. However, when a block erase command is executed while the FMR13 bit is set to 1, the lock bit data set to 0 (locked) changes to 1 (not locked) after erasure completes.

[Conditions for setting to 0]
The FMR13 bit is set to 0 when one of the following conditions is met:
- Completion of the program command
- Completion of the erase command
- Generation of a command error
- The FMR01 bit in the FMR0 register is set to 0 (CPU rewrite mode disabled).
- The FMSTP bit in the FMR0 register is set to 1 (flash memory stops).
- The CMDRST bit in the FMR0 register is set to 1 (erasure/writing stopped).

[Condition for setting to 1]
Set to 1 by a program.

FMR14 Bit (Data Flash Block A Rewrite Disable Bit)

When the FMR 14 bit is set to 0, data flash block A accepts program and block erase commands.

FMR15 Bit (Data Flash Block B Rewrite Disable Bit)

When the FMR 15 bit is set to 0, data flash block B accepts program and block erase commands.

FMR16 Bit (Data Flash Block C Rewrite Disable Bit)

When the FMR 16 bit is set to 0, data flash block C accepts program and block erase commands.

FMR17 Bit (Data Flash Block D Rewrite Disable Bit)

When the FMR 17 bit is set to 0, data flash block D accepts program and block erase commands.

35.4.4 Flash Memory Control Register 2 (FMR2)

Address 01B6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	FMR27	—	—	—	—	FMR22	FMR21	FMR20
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FMR20	Erase-suspend enable bit (1)	0: Erase-suspend disabled 1: Erase-suspend enabled	R/W
b1	FMR21	Erase-suspend request bit	0: Erase restart 1: Erase-suspend request	R/W
b2	FMR22	Interrupt request suspend request enable bit (1)	0: Erase-suspend request disabled by interrupt request 1: Erase-suspend request enabled by interrupt request	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—	Reserved bits	Set to 0.	R/W
b5	—			R/W
b6	—			R/W
b7	FMR27	Low-consumption-current read mode enable bit (1)	0: Low-consumption-current read mode disabled 0: Low-consumption-current read mode enabled	R/W

Note:
1. To set this bit to 1, first write 0 and then 1 immediately. Do not generate an interrupt between writing 0 and writing 1.

FMR20 Bit (Erase-Suspend Enable Bit)

When the FMR20 bit is set to 1 (enabled), the erase-suspend function is enabled.

FMR21 Bit (Erase-Suspend Request Bit)

When the FMR21 bit is set to 1, erase-suspend mode is entered. If the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request) when an interrupt request for the enabled interrupt is generated, and erase-suspend mode is entered. To restart auto-erasure, set the FMR21 bit to 0 (erase restart).

[Condition for setting to 0]
Set to 0 by a program.
[Conditions for setting to 1]
- The FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request) when an interrupt is generated.
- Set to 1 by a program.

FMR22 Bit (Interrupt Request Suspend-Request Enable Bit)

When the FMR 22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request) at the time an interrupt request is generated during auto-erasure. Set the FMR22 bit to 1 when using erase-suspend while rewriting the user ROM area in EW1 mode.

FMR27 Bit (Low-Power-Current Read Mode Enable Bit)

When the FMR 27 bit is set to 1 (low-consumption-current read mode enabled) in low-speed clock mode (XIN clock stopped) or low-speed on-chip oscillator mode (XIN clock stopped), power consumption when reading the flash memory can be reduced. Refer to **10.7.11 Low-Current-Consumption Read Mode** for details.

35.4.5 EW0 Mode

When the FMR01 bit in the FMR0 register is set to 1 (CPU rewrite mode enabled), the MCU enters CPU rewrite mode and software commands can be accepted. At this time, the FMR02 bit in the FMR0 register is set to 0 so that EW0 mode is selected.

Software commands are used to control program and erase operations. The FST register or the status register can be used to confirm whether programming or erasure has completed.

To enter erase-suspend during auto-erasure, set the FMR20 bit to 1 (erase-suspend enabled) and the FMR21 bit to 1 (erase-suspend request). Wait for td(SR-SUS) and ensure that the FST6 bit in the FST register is set to 1 (during erase-suspend) before accessing the flash memory. Auto-erasure can be restarted by setting the FMR21 bit in the FMR2 register to 0 (erase restart).

35.4.6 EW1 Mode

After the FMR01 bit in the FMR0 register is set to 1 (CPU rewrite mode enabled), EW1 mode is selected by setting the FMR02 bit is set to 1.

The FST register can be used to confirm whether programming and erasure has completed. Do not execute the read status register command in EW1 mode.

To enable the erase-suspend function during auto-erasure, execute the block erase command after setting the FMR20 bit in the FMR2 register to 1 (suspend enabled). To enter erase-suspend while auto-erasing the user ROM area, set the FMR22 bit in the FMR2 register to 1 (erase-suspend request enabled by interrupt request). Also, the interrupt to enter program-suspend must be enabled beforehand.

When an interrupt request is generated, the FMR21 bit in the FMR2 register is automatically set to 1 (erase-suspend request) and auto-erasure suspends after td(SR-SUS). After interrupt handling completes, set the FMR21 bit to 0 (erase restart) to restart auto-erasure.

35.4.7 Suspend Operation

Figure 35.2 shows the Suspend Operation Timing.

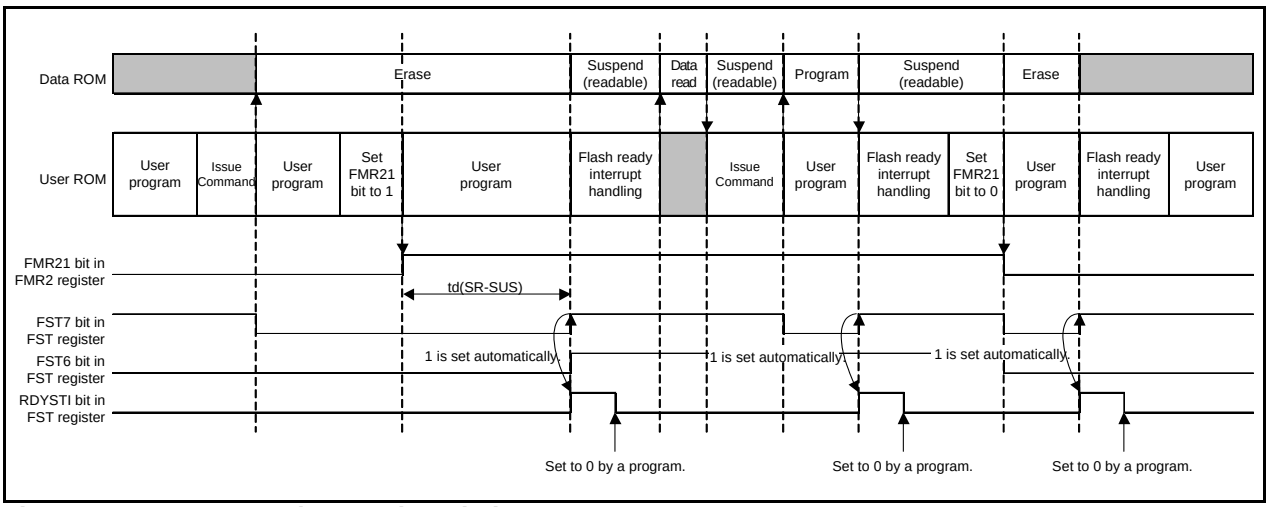


Figure 35.2 Suspend Operation Timing

35.4.8 How to Set and Exit Each Mode

Figure 35.3 shows How to Set and Exit EW0 Mode and Figure 35.4 shows How to Set and Exit EW0 Mode (When Rewriting Data Flash) and EW1 Mode.

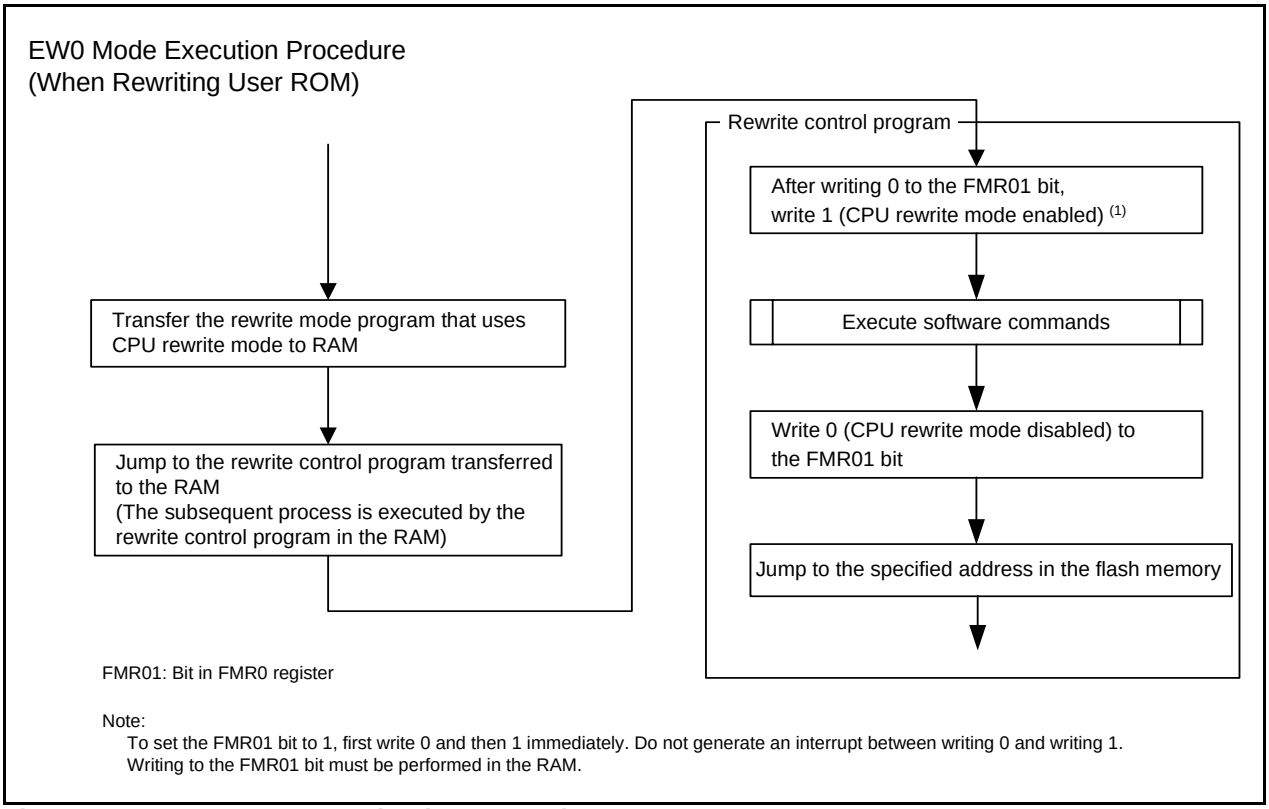


Figure 35.3 How to Set and Exit EW0 Mode

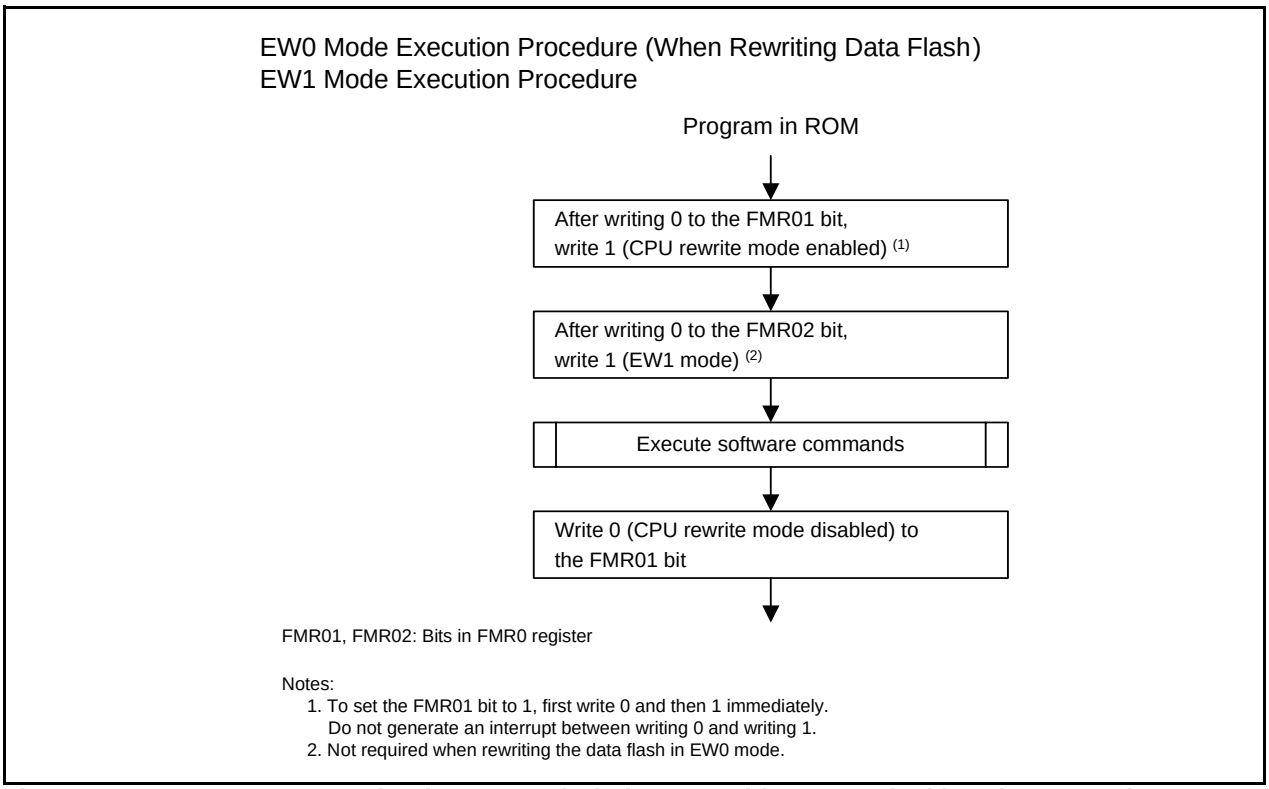


Figure 35.4 How to Set and Exit EW0 Mode (When Rewriting Data Flash) and EW1 Mode

35.4.9 BGO (BackGround Operation) Function

When the program ROM area is specified while a program or block erase operation to the data flash, array data can be read. This eliminates the need for writing software commands. Access time is the same as for normal read operations.
Figure 35.5 shows the BGO Function.

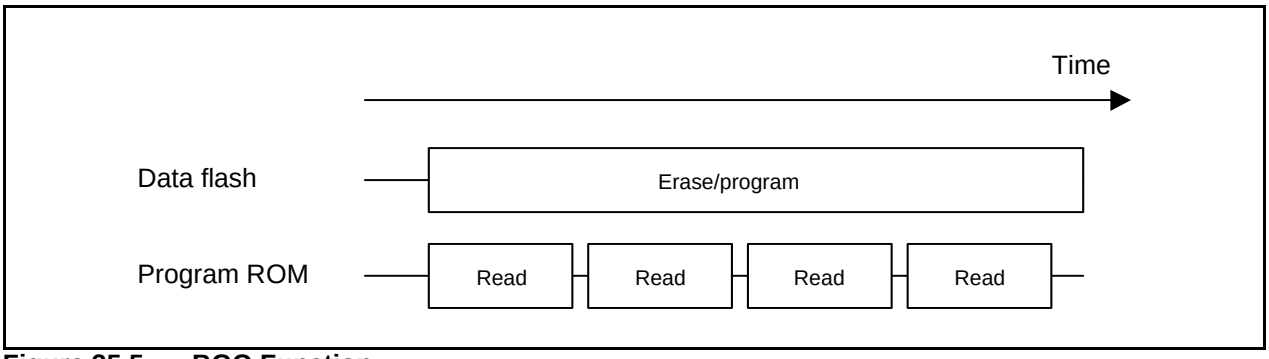


Figure 35.5 BGO Function

35.4.10 Data Protect Function

Each block in the flash memory has a nonvolatile lock bit. The lock bit is enabled by setting the FMR13 bit in the FMR1 register is set to 0 (lock bit enabled). The lock bit can be used to disable (lock) programming or erasing each block. This prevents data from being written or erased inadvertently. A block status changes according to the lock bit as follows:

- When the lock bit data is set to 0: locked (the block cannot be programmed or erased)
- When the lock bit data is set to 1: not locked (the block can be programmed and erased)

The lock bit data is set to 0 (locked) by executing the lock bit program command and to 1 (not locked) by erasing the block. No commands can be used to set only the lock bit data to 1.
The lock bit data can be read using the read lock bit status command.

When the FMR13 bit is set to 1 (lock bit disabled), the lock bit function is disabled and all blocks are not locked (each lock bit data remains unchanged). The lock bit function is enabled by setting the FMR13 bit to 0 (the lock bit data is retained).
When the block erase command is executed while the FMR13 bit is set to 1, the target block is erased regardless of the lock bit status. The lock bit of the erase target block is set to 1 after auto-erasure completes.
Refer to **35.4.11 Software Commands** for the details of individual commands.
The FMR13 bit is set to 0 after auto-erasure completes. This bit is also set to 0 if one of the following conditions is met. To erase or program a different locked block, set the FMR 13 bit to 1 again and execute the block erase or program command.

- The FST7 bit in the FST register changes from 0 (busy) to 1 (ready).
- An incorrect command is input.
- The FMR01 bit in the FMR0 register is set to 0 (CPU mode disabled).
- The FMSTP bit in the FM0 register is set to 1 (flash memory stops).

Figure 35.6 shows the FMR13 Bit Operation Timing.

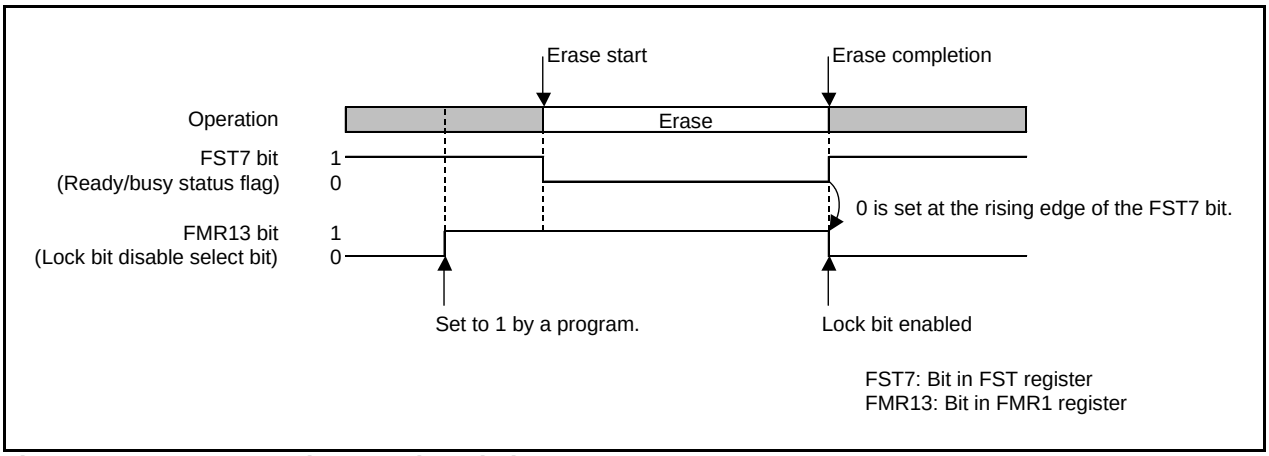


Figure 35.6 FMR13 Bit Operation Timing

35.4.11 Software Commands

The software commands are described below. Read or write commands and data in 8-bit units.

Table 35.4 Software Commands

Command	First Bus Cycle			Second Bus Cycle		
	Mode	Address	Data	Mode	Address	Data
Read array	Write	×	FFh			
Read status register	Write	×	70h	Read	×	SRD
Clear status register	Write	×	50h			
Program	Write	WA	40h	Write	WA	WD
Block erase	Write	×	20h	Write	BA	D0h
Lock bit program	Write	BT	77h	Write	BT	D0h
Read lock bit status	Write	×	71h	Write	BT	D0h
Block blank check	Write	×	25h	Write	BA	D0h

SRD: Status register data
WA: Write address
WD: Write data
BA: Any block address
BT: Starting block address
×: Any address in the user ROM area

35.4.11.1 Read Array Command

The read array command is used to read the flash memory.
When FFh is written in the first bus cycle, the MCU enters read array mode. When the read address is input in the following bus cycles, the content of the specified address can be read in 8-bit units.
Since read array mode remains until another command is written, the contents of multiple addresses can be read continuously.
In addition, the MCU enters read array mode after a reset.

35.4.11.2 Read Status Register Command

The read status register command is used to read the status register.
When 70h is written in the first bus cycle, the status register can be read in the second bus cycle. When reading the status register, read the same address as the address value in the first bus cycle.
In CPU rewrite mode, do not execute this command.
Read status register mode remains until the next read array command is written.

35.4.11.3 Clear Status Register Command

The clear status register command is used to set the status register to 0.
When 50h is written in the first bus cycle, bits FST4 and FST5 in the FST register and bits SR4 and SR5 in the status register are set to 0. If the clear status register is input in read array mode, the MCU enters read array mode after the status register is set to 0.

35.4.11.4 Program Command

The program command is used to write data to the flash memory in 1-byte units.
When 40h is written in the first bus cycle and data is written in the second bus cycle to the write address, auto-programming (data program and verify operation) starts. Make sure the address value specified in the first bus cycle is the same address as the write address specified in the second bus cycle.
The FST7 bit in the FST register can be used to confirm whether auto-programming has completed. The FST7 bit is set to 0 during auto-programming and is set to 1 when auto-programming completes.
After auto-programming has completed, the auto-program result can be confirmed by the FST4 bit in the FST register (refer to **35.4.17 Full Status Check**).
Do not write additions to the already programmed addresses.

The program command targeting each block in the program ROM can be disabled using the lock bit.
The following commands are not accepted under the following conditions:

- Block erase commands targeting data flash block A when the FMR14 bit in the FMR1 register is set to 1 (rewrite disabled).
- Block erase commands targeting data flash block B when the FMR15 bit is set to 1 (rewrite disabled).
- Block erase commands targeting data flash block C when the FMR16 bit is set to 1 (rewrite disabled).
- Block erase commands targeting data flash block D when the FMR17 bit is set to 1 (rewrite disabled).

Figure 35.7 shows a Program Flowchart (Flash Ready Status Interrupt Disabled) and Figure 35.8 shows a Program Flowchart (Flash Ready Status Interrupt Enabled).

In EW1 mode, do not execute this command to any address where a rewrite control program is allocated.

When RDYSTIE bit in the FMR0 register is set to 1 (flash ready status interrupt enabled), a flash ready status interrupt can be generated upon completion of auto-programming. The auto-program result can be confirmed by reading the FST register during the interrupt routine.

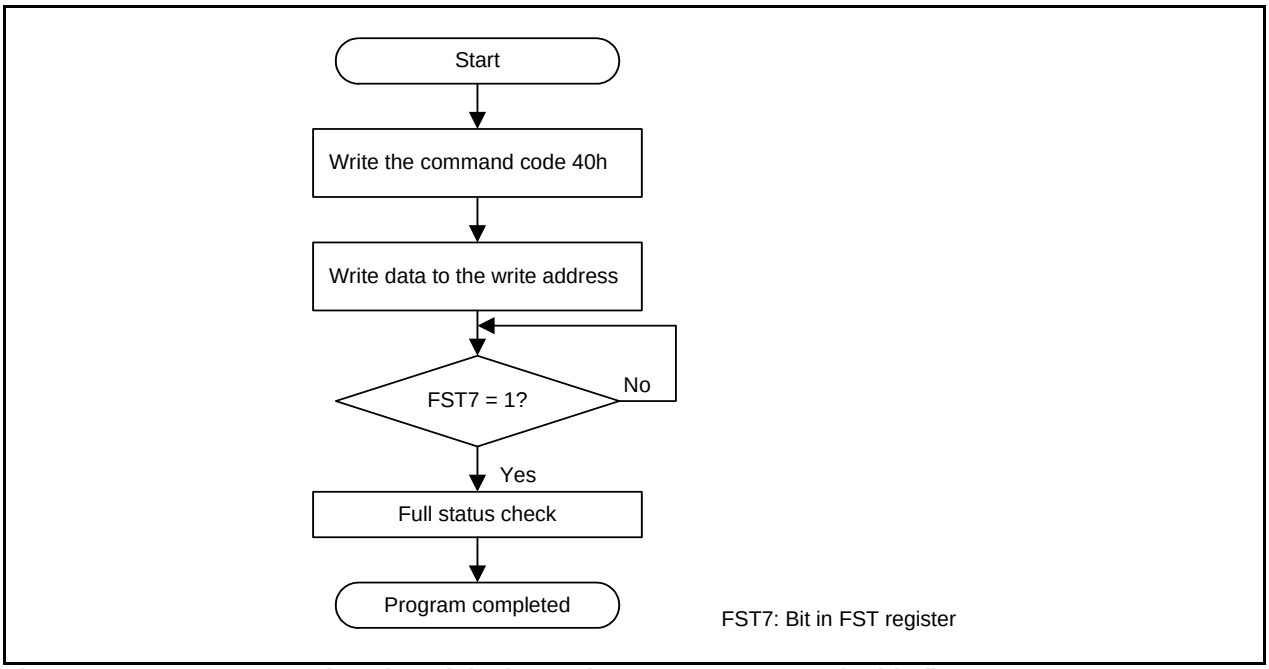


Figure 35.7 Program Flowchart (Flash Ready Status Interrupt Disabled)

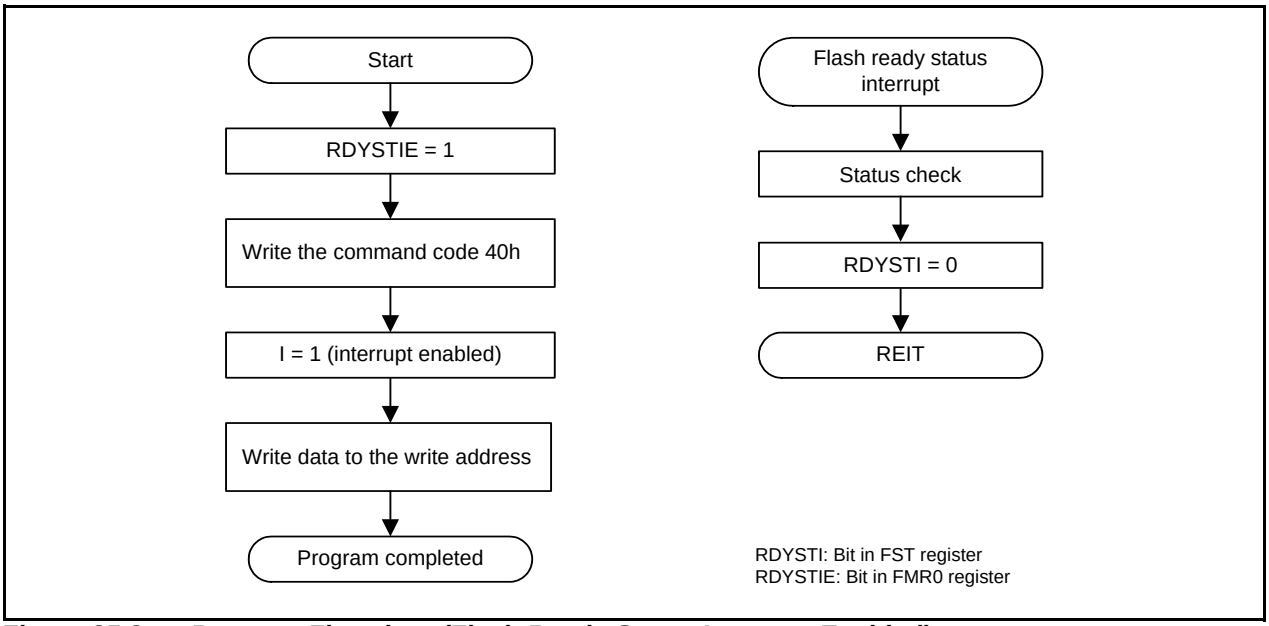


Figure 35.8 Program Flowchart (Flash Ready Status Interrupt Enabled)

35.4.11.5 Block Erase Command

When 20h is written in the first bus cycle and then D0h is written in the second bus cycle to any block address, auto-erasure (erase and erase verify operation) starts in the specified block.
The FST7 bit in the FST register can be used to confirm whether auto-erasure has completed. The FST7 bit is set to 0 during auto-erasure and is set to 1 when auto-erasure completes.
After auto-erasure has completed, the auto-erase result can be confirmed by the FST5 bit in the FST register. (Refer to **35.4.17 Full Status Check**).

The block erase command targeting each block in the program ROM can be disabled using the lock bit.
The following commands are not accepted under the following conditions:

- Block erase commands targeting data flash block A when the FMR14 bit in the FMR1 register is set to 1 (rewrite disabled).
- Block erase commands targeting data flash block B when the FMR15 bit is set to 1 (rewrite disabled).
- Block erase commands targeting data flash block C when the FMR16 bit is set to 1 (rewrite disabled).
- Block erase commands targeting data flash block D when the FMR17 bit is set to 1 (rewrite disabled).

Figure 35.9 shows the Block Erase Flowchart (Flash Ready Status Interrupt Disabled), Figure 35.10 shows the Block Erase Flowchart (Flash Ready Status Interrupt Disabled and Suspend Enabled), and Figure 35.11 shows the Block Erase Flowchart (Flash Ready Status Interrupt Enabled and Suspend Enabled).

In EW1 mode, do not execute this command to any block where a rewrite control program is allocated.

While the RDYSTIE bit in the FMR0 register is set to 1 (flash ready status interrupt enabled), a flash ready status interrupt can be generated upon completion of auto-erasure. While the RDYSTIE bit is set to 1 and the FMR20 bit in the FMR2 register is set to 1 (erase-suspend enabled), a flash ready status interrupt is generated when the FMR21 bit is set to 1 (erase-suspend request) and auto-erasure suspends. The auto-erase result can be confirmed by reading the FST register during the interrupt routine.

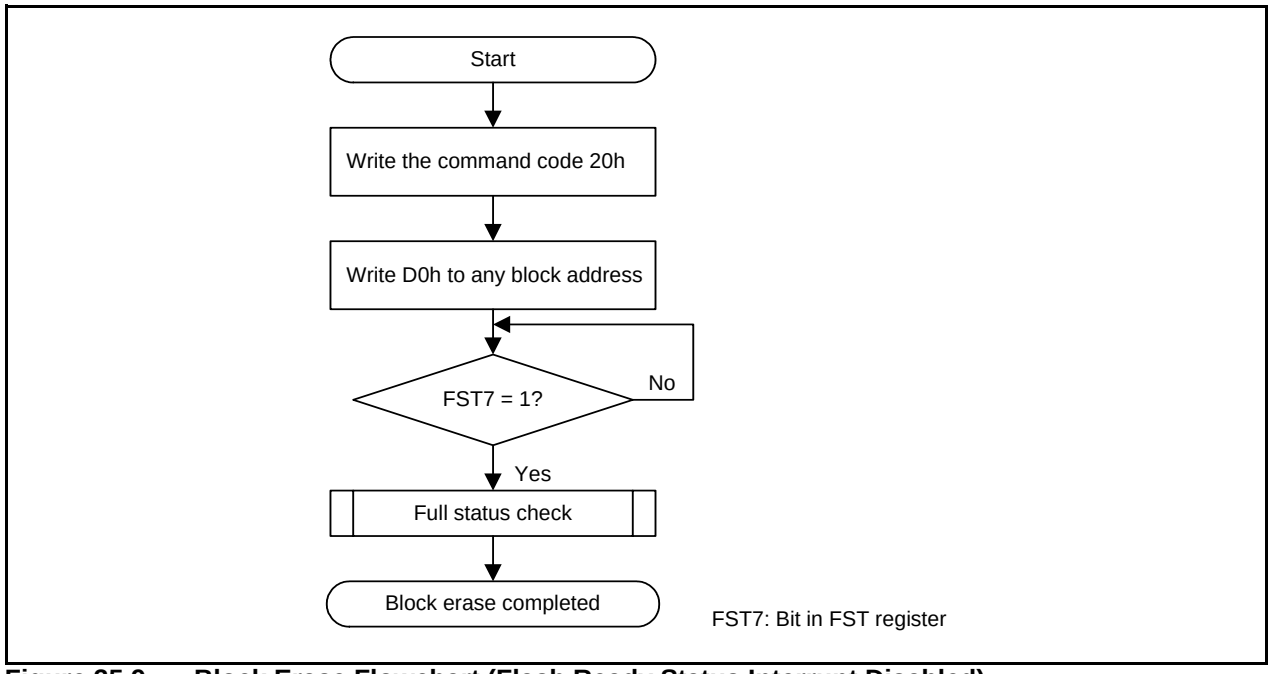
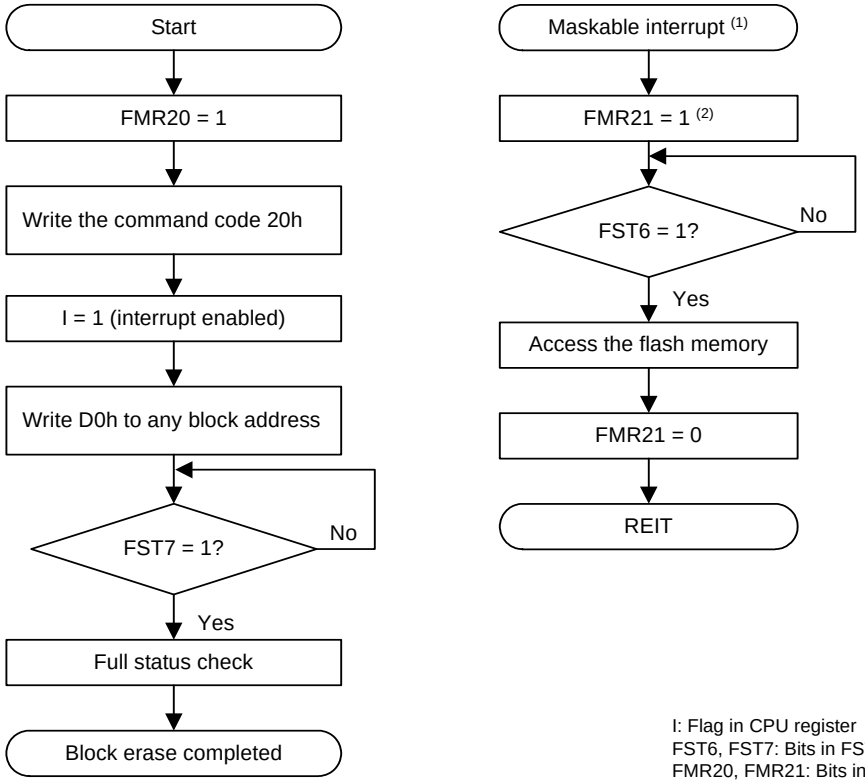
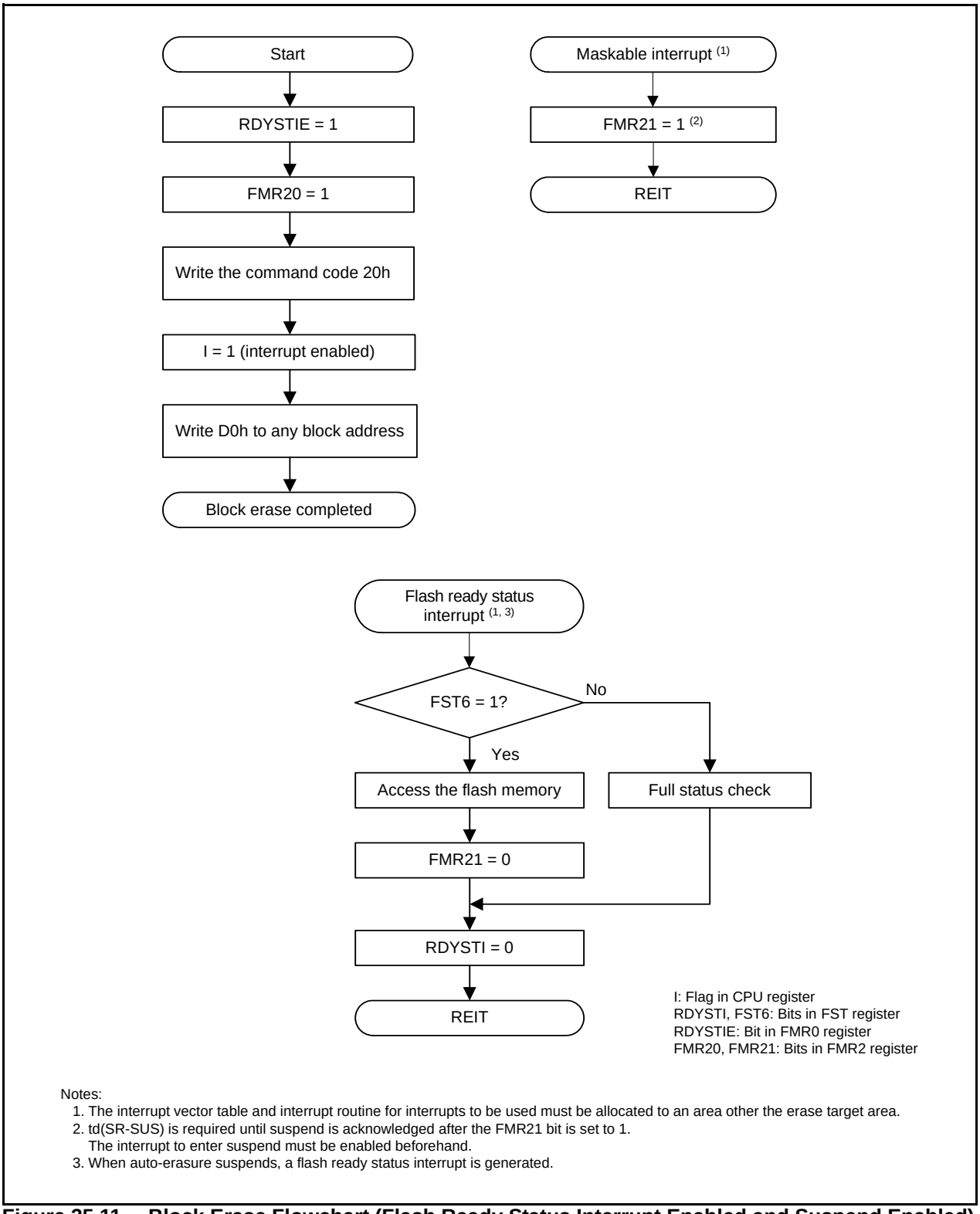


Figure 35.9 Block Erase Flowchart (Flash Ready Status Interrupt Disabled)



Notes:
1. The interrupt vector table and interrupt routine for interrupts to be used must be allocated to an area other the erase target area.
2. td(SR-SUS) is required until suspend is acknowledged after the FMR21 bit is set to 1.
   The interrupt to enter suspend must be enabled beforehand.

Figure 35.10 Block Erase Flowchart (Flash Ready Status Interrupt Disabled and Suspend Enabled)



Notes:
1. The interrupt vector table and interrupt routine for interrupts to be used must be allocated to an area other the erase target area.
2. td(SR-SUS) is required until suspend is acknowledged after the FMR21 bit is set to 1.
   The interrupt to enter suspend must be enabled beforehand.
3. When auto-erasure suspends, a flash ready status interrupt is generated.

Figure 35.11 Block Erase Flowchart (Flash Ready Status Interrupt Enabled and Suspend Enabled)

35.4.11.6 Lock Bit Program Command

This command is used to set the lock bit of any block in the program ROM area to 0 (locked).
When 77h is written in the first bus cycle and D0h is written in the second bus cycle to the starting block address, 0 is written to the lock bit of the specified block. Make sure the address value in the first bus cycle is the same address as the starting block address specified in the second bus cycle.
Figure 35.12 shows the Lock Bit Program Flowchart. The lock bit status (lock bit data) can be read using the read lock bit status command.
The FST7 bit in the FST register can be used to confirm whether writing to the lock bit has completed.
Refer to **35.4.10 Data Protect Function** for the lock bit function and how to set the lock bit to 1 (not locked).

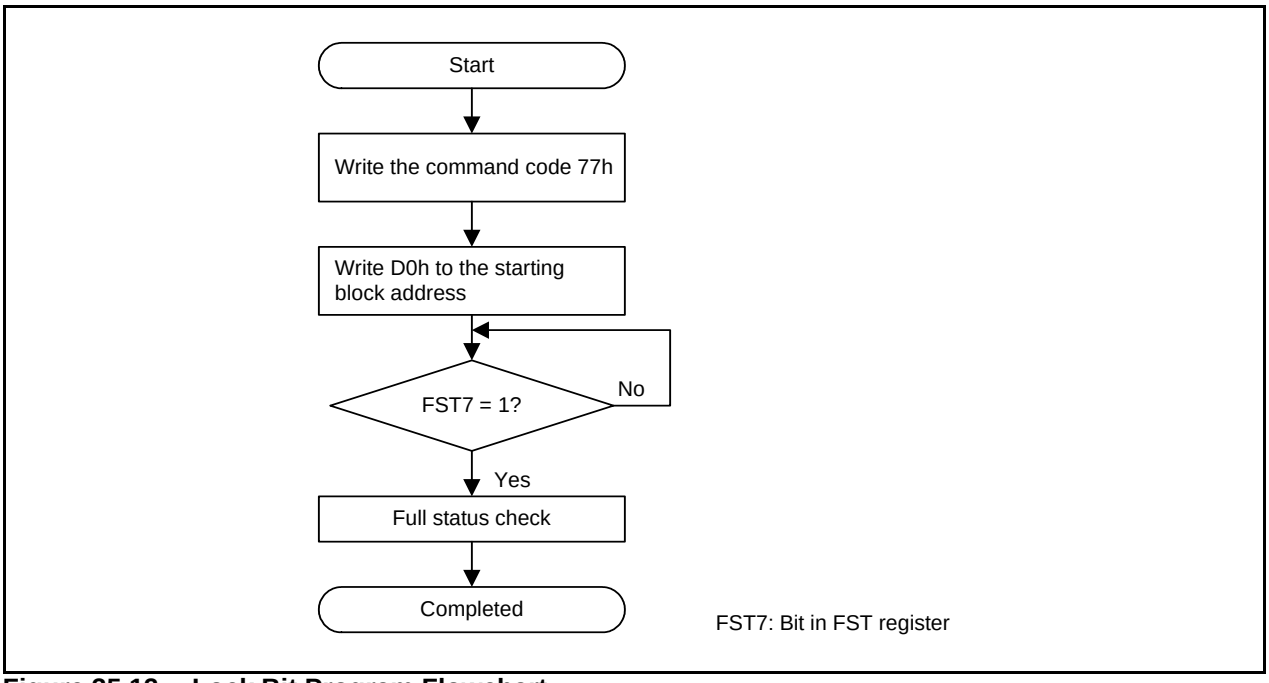


Figure 35.12 Lock Bit Program Flowchart

35.4.11.7 Read Lock Bit Status Command

This command is used to read the lock bit status of any address in the program ROM area.
When 71h written in the first bus cycle and D0h is written in the second cycle to the starting block address, the lock bit status of the specified block is stored in the LBDATA bit in the FST register. After the FST7 bit in the FST register has been set to 1 (ready), read the LBDATA bit.
Figure 35.13 shows the Read Lock Bit Status Flowchart.

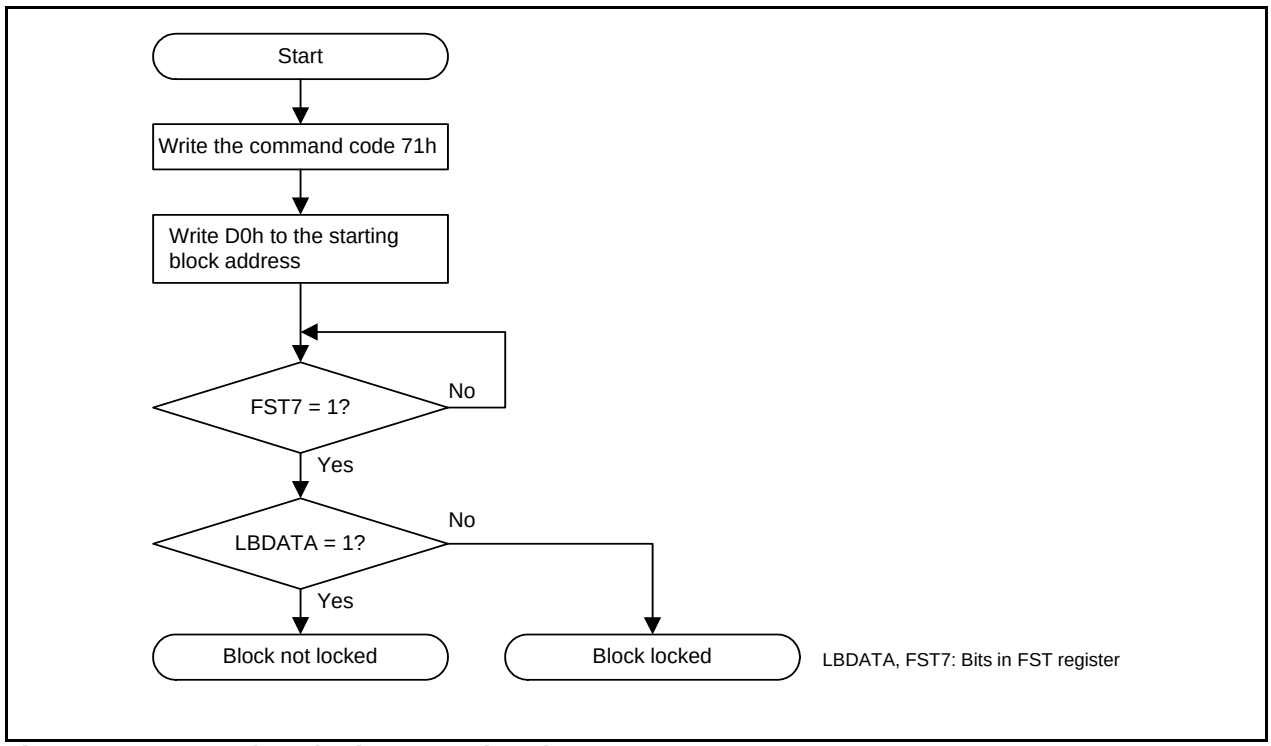


Figure 35.13 Read Lock Bit Status Flowchart

35.4.11.8 Block Blank Check Command

This command is used to confirm that all addresses in any block are blank data FFh.
When 25h is written in the first bus cycle and D0h is written in the second bus cycle to any block address, blank checking starts in the specified block. The FST7 bit in the FST register can be used to confirm whether blank checking has completed. The FST7 bit is set to 0 during the blank-check period and set to 1 when blank checking completes.
After blank checking has completed, the blank-check result can be confirmed by the FST5 bit in the FST register. (Refer to **35.4.17 Full Status Check**.).
Figure 35.14 shows the Block Blank Check Flowchart.

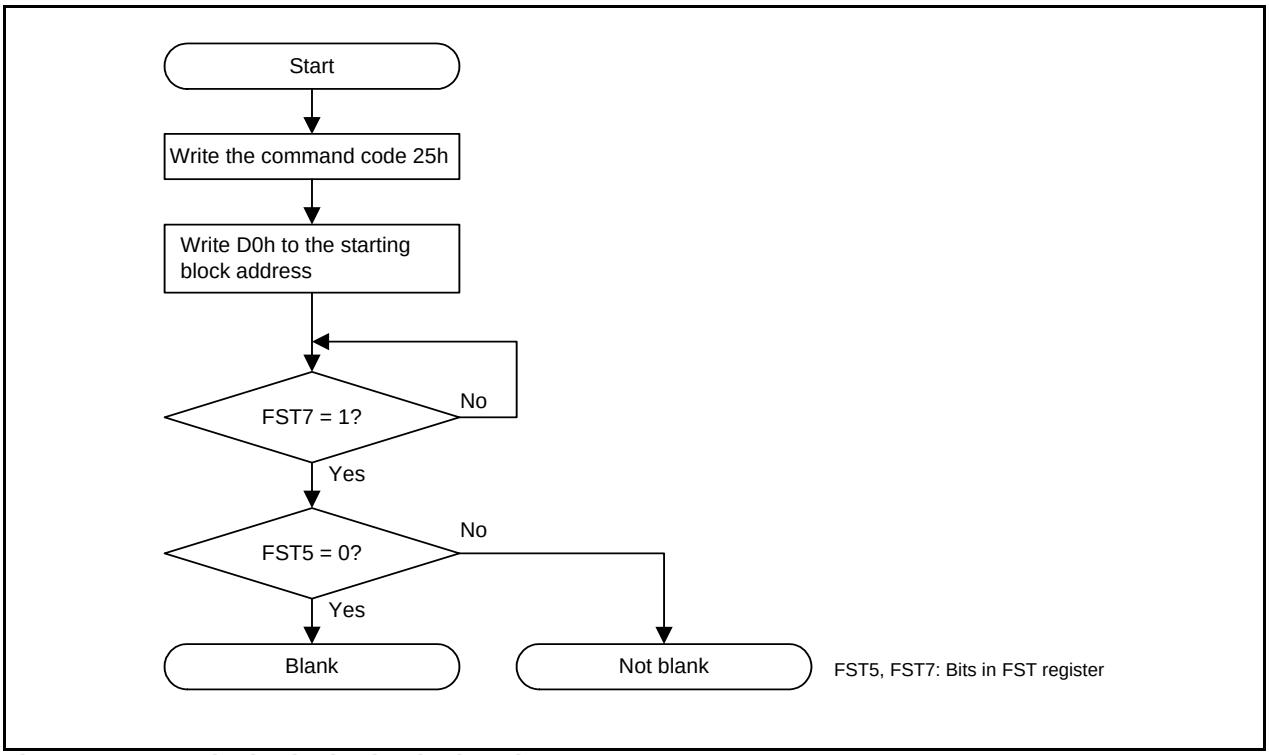


Figure 35.14 Block Blank Check Flowchart

35.4.12 Status Register

The status register indicates the operating status of the flash memory and whether erasure or programming has completed normally or terminated in error. The status of the status register can be read by using the FST register.

35.4.13 Sequence Status

The clear sequence status bit indicates the operating status of the flash memory. This bit is set to 0 (busy) during auto-programming and auto-erasure. It is set to 1 (ready) when these operations complete.

35.4.14 Erase Status

Refer to **35.4.17 Full Status Check**.

35.4.15 Program Status

Refer to **35.4.17 Full Status Check**.

35.4.16 Suspend Status

The suspend status bit indicates the suspend status of the flash memory commands. This bit is set to 1 (during erase-suspend) while auto-erasure suspends and set to 0 (other than erase-suspend) when auto-erasure restarts. Table 35.5 lists the Status Register.

Table 35.5 Status Register

Status Register Bit	FST Register Bit	Status Name	Content		Value After Reset
			0	1	
SR0 (D0)	–	Reserved	–	–	–
SR1 (D1)	–	Reserved	–	–	–
SR2 (D2)	–	Reserved	–	–	–
SR3 (D3)	–	Reserved	–	–	–
SR4 (D4)	FST4	Program status	Completed normally	Terminated in error	0
SR5 (D5)	FST5	Erase status/ blank check	Completed normally	Terminated in error	0
SR6 (D6)	FST6	Suspend status	Other than erase-suspend	During erase-suspend	0
SR7 (D7)	FST7	Sequencer status	Busy	Ready	1

D0 to D7: Indicate the data bus which is read when the read status register command is executed.
Bits FST4 (SR4) and FST5 (SR5) are set to 0 by executing the clear status command.
When the FST4 bit (SR4) or FST5 bit (SR5) is set to 1, the program and block erase commands cannot be accepted.

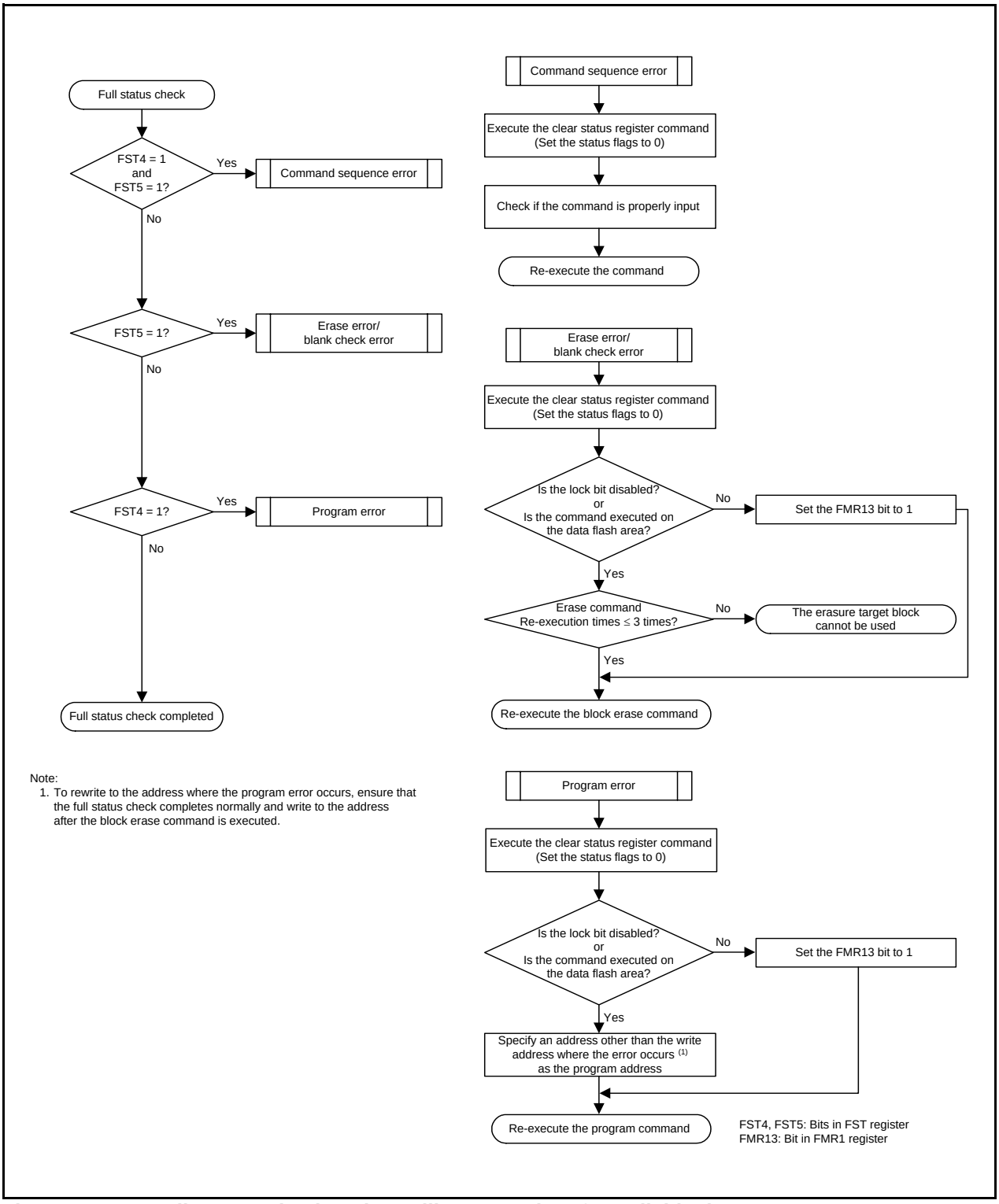
35.4.17 Full Status Check

If an error occurs, bits FST4 and FST5 in the FST register are set to 1, indicating the occurrence of an error. The execution result can be confirmed by checking these status bits (full status check).
Table 35.6 lists the Errors and FST Register Status. Figure 35.15 shows the Full Status Check and Handling Procedure for Individual Errors.

Table 35.6 Errors and FST Register Status

FST Register (Status Register) Status		Error	Error Occurrence Condition
FST5 (SR5)	FST4 (SR4)		
1	1	Command sequence error	• When a command is not written correctly. • When data other than valid data (i.e., D0h or FFh) is written in the second bus cycle of the block erase command. (1)
1	0	Erase error	When the block erase command is executed, but auto-erasure does not complete correctly.
		Blank check error	When the blank check command is executed and data other than blank data FFh is read.
0	1	Program error	When the program command is executed, but auto-programming does not complete correctly.

Note:
1. When FFh is written in the second bus cycle of these commands, the MCU enters read array mode. At the same time, the command code written in the first bus cycle is invalid.



Note:
1. To rewrite to the address where the program error occurs, ensure that the full status check completes normally and write to the address after the block erase command is executed.

Figure 35.15 Full Status Check and Handling Procedure for Individual Errors

35.5 Standard Serial I/O Mode

In standard serial I/O mode, a serial programmer which supports the MCU can be used to rewrite the user ROM area while the MCU is mounted on-board.
There are three types of standard serial I/O modes:

- Standard serial I/O mode 1 .....Clock synchronous serial I/O used to connect to a serial programmer
- Standard serial I/O mode 2 .....Clock asynchronous serial I/O used to connect to a serial programmer
- Standard serial I/O mode 3 .....Special clock asynchronous serial I/O used to connect to a serial programmer

Standard serial I/O mode 2 and standard serial I/O mode 3 can be used for the MCU.

Refer to **Appendix 2. Connection Examples with M16C Flash Starter** for examples of connecting to a serial programmer. Contact the serial programmer manufacturer for more information. Refer to the user's manual included with your serial programmer for instructions.

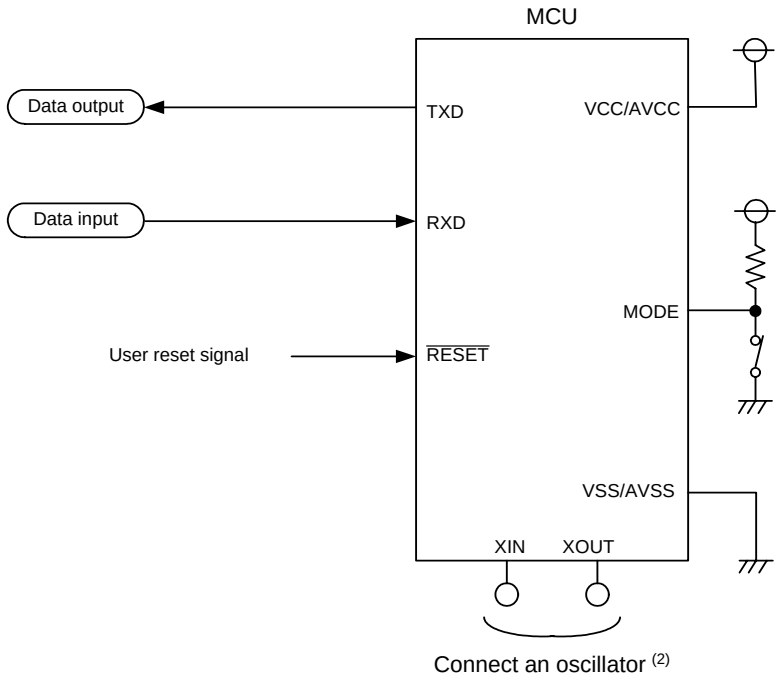
Table 35.7 lists the Pin Functions (Flash Memory Standard Serial I/O Mode 2) and Figure 35.16 shows Pin Handling in Standard Serial I/O Mode 2. Table 35.8 lists the Pin Functions (Flash Memory Standard Serial I/O Mode 3) and Figure 35.17 shows Pin Handling in Standard Serial I/O Mode 3.
After handling the pins shown in Table 35.8 and rewriting the flash memory using the programmer, apply a high-level signal to the MODE pin and reset the hardware to run a program in the flash memory in single-chip mode.

35.5.1 ID Code Check Function

The ID code check function determines whether the ID codes sent from the serial programmer and those written in the flash memory match.
Refer to **13. ID Code Areas** for details of the ID code check.

Table 35.7 Pin Functions (Flash Memory Standard Serial I/O Mode 2)

Pin	Name	I/O	Description
VCC, VSS	Power supply input		Apply the guaranteed programming and erasure voltage to the VCC pin and 0 V to the VSS pin.
$\overline{\text{RESET}}$	Reset input	I	Reset input pin
P12_0/XIN	P12_0 input/clock input	I	Connect a ceramic resonator or crystal oscillator between pins XIN and XOUT.
P12_1/XOUT	P12_1 input/clock output	I/O	
XCIN	Clock input	I	Connect a crystal oscillator between pins XCIN and XCOUT.
XCOUT	Clock output	I/O	
P0 to P7	Input ports P0 to P7	I	Input a high- or low-level signal or leave open.
P10, P11, P12_2 to P12_3	Input ports P10 to P12	I	Input a high- or low-level signal or leave open.
P13_0, P13_3 to P13_7	Input port P13	I	Input a high- or low-level signal or leave open.
VREF	Reference voltage	I	Input a high-level signal.
MODE	MODE	I/O	Input a low-level signal.
P13_2	TXD output	O	Serial data output pin
P13_1	RXD input	I	Serial data input pin

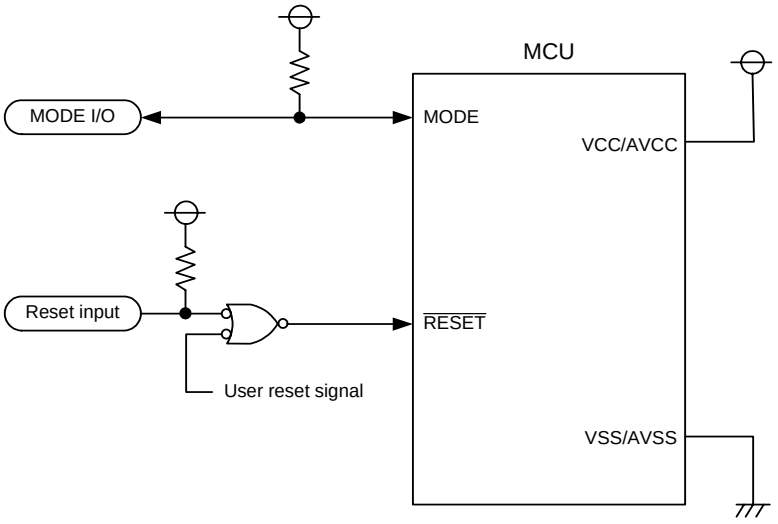


Notes:
1. In this example, modes are switched between single-chip mode and standard serial I/O mode by controlling the MODE input with a switch.
2. When operating with the on-chip oscillator clock, it is not necessary to connect an oscillation circuit. Refer to **Appendix 2 Connection Examples with M16C Flash Starter**.

Figure 35.16 Pin Handling in Standard Serial I/O Mode 2

Table 35.8 Pin Functions (Flash Memory Standard Serial I/O Mode 3)

Pin	Name	I/O	Description
VCC, VSS	Power supply input		Apply the guaranteed programming and erasure voltage to the VCC pin and 0 V to the VSS pin.
$\overline{\text{RESET}}$	Reset input	I	Reset input pin
P12_0/XIN	P12_0 input/clock input	I	If an external oscillator is connected, connect a ceramic resonator or crystal oscillator between pins XIN and XOUT.
P12_1/XOUT	P12_1 input/clock output	I/O	
XCIN	Clock input	I	If an external oscillator is connected, connect a crystal oscillator between pins XCIN and XCOUT.
XCOUT	Clock output	I/O	
P0 to P7	Input ports P0 to P7	I	Input a high- or low-level signal or leave open.
P10 to P13	Input ports P10 to P13	I	Input a high- or low-level signal or leave open.
VREF	Reference voltage	I	Input a high-level signal.
MODE	MODE	I/O	Serial data I/O pin. Connect the pin to a programmer.



Notes:
1. Controlled pins and external circuits vary depending on the programmer.
   Refer to the programmer manual for details.
2. In this example, modes are switched between single-chip mode and standard serial I/O mode by connecting a programmer.
3. When operating with the on-chip oscillator clock, it is not necessary to connect an oscillation circuit.

Figure 35.17 Pin Handling in Standard Serial I/O Mode 3

35.6 Parallel I/O Mode

Parallel I/O mode is used to input and output software commands, addresses and data necessary to control (read, program, and erase) the on-chip flash memory.
Use a parallel programmer which supports the MCU. Contact the parallel programmer manufacturer for more information. Refer to the user's manual included with your parallel programmer for instructions.
In parallel I/O mode, the user ROM areas shown in Figure 35.1 can be rewritten.

35.6.1 ROM Code Protect Function

The ROM code protect function prevents the flash memory from being read and rewritten. (Refer to the **35.3.2 ROM Code Protect Function**.)

35.7 Notes on Flash Memory

35.7.1 CPU Rewrite Mode

35.7.1.1 Prohibited Instructions

The following instructions cannot be used while the program ROM area is being rewritten in EW0 mode because they reference data in the flash memory: UND, INTO, and BRK.

35.7.1.2 Non-Maskable Interrupts

Tables 35.9 and 35.10 list CPU Rewrite Mode Interrupts (1) and (2), respectively.

Table 35.9 CPU Rewrite Mode Interrupts (1)

Mode	Erase/ Write Target	Status	Maskable Interrupt	• Address Match • Address Break (Note 1)
EW0	Data flash	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request). The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0 (erase-suspend request disabled by interrupt request), set the FMR 21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read. Auto-erasure can be restarted by setting the FMR21 bit to 0 (erase restart).	
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.	
		During auto-programming		
	Program ROM	During auto-erasure (suspend enabled)	Usable by allocating a vector in RAM.	Not usable during auto-erasure or auto-programming.
		During auto-erasure (suspend disabled)		
		During auto-programming		
EW1	Data flash	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1, the FMR21 bit is automatically set to 1. The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0, set the FMR 21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read. Auto-erasure can be restarted by setting the FMR21 bit to 0.	
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.	
		During auto-programming		
	Program ROM	During auto-erasure (suspend enabled)	Auto-erasure suspends after td(SR-SUS) and interrupt handling is executed. Auto-erasure can be restarted by setting the FMR21 bit to 0 after interrupt handling completes. While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read.	
		During auto-erasure (suspend disabled or FMR22 = 0)	Auto-erasure and auto-programming have priority and interrupt requests are put on standby. Interrupt handling is executed after auto-erase and auto-program complete.	
		During auto-programming		

FMR21, FMR22: Bits in FMR2 register

Note:

1. Do not use a non-maskable interrupt while block 0 is being auto-erased because the fixed vector is allocated in block 0.

Table 35.10 CPU Rewrite Mode Interrupts (2)

Mode	Erase/ Write Target	Status	• Watchdog Timer • Oscillation Stop Detection • Voltage Monitor 2 • Voltage Monitor 1 • NMI (Note 1)	• Undefined Instruction • INTO Instruction • BRK Instruction • Single Step (Note 1)
EW0	Data flash	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request). The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0 (erase-suspend request disabled by interrupt request), set the FMR 21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read. Auto-erasure can be restarted by setting the FMR21 bit is set to 0 (erase restart).	
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.	
		During auto-programming		
	Program ROM	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period. Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally. The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the erase-suspend function.	Not usable during auto-erasure or auto-programming.
		During auto-erasure (suspend disabled)		
		During auto-programming		
EW1	Data flash	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1, the FMR21 bit is automatically set to 1. The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0, set the FMR 21 bit to 1 during interrupt handling. The flash memory suspends auto-programming after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read. Auto-erasure can be restarted by setting the FMR21 bit is set to 0.	
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.	
		During auto-programming		
	Program ROM	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period. Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally. The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the erase-suspend function.	Not usable during auto-erasure or auto-programming.
		During auto-erasure (suspend disabled or FMR22 = 0)		
		During auto-programming		

FMR21, FMR22: Bits in FMR2 register

Note:

1. Do not use a non-maskable interrupt while block 0 is being auto-erased because the fixed vector is allocated in block 0.

35.7.1.3 How to Access

To set one of the following bits to 1, first write 0 and then 1 immediately. Do not generate an interrupt between writing 0 and writing 1.

- The FMR01 or FMR02 bit in the FMR0 register
- The FMR13 bit in the FMR1 register
- The FMR20, FMR22, or FMR 27 bit in the FMR2 register

To set one of the following bits to 0, first write 1 and then 0 immediately. Do not generate an interrupt between writing 1 and writing 0.

- The FMR14, FMR15, FMR16, or FMR17 bit in the FMR1 register

35.7.1.4 Rewriting User ROM Area

In EW0 Mode, if the supply voltage drops while rewriting any block in which a rewrite control program is stored, it may not be possible to rewrite the flash memory because the rewrite control program cannot be rewritten correctly. In this case, use standard serial I/O mode.

35.7.1.5 Programming

Do not write additions to the already programmed address.

35.7.1.6 Entering Stop Mode or Wait Mode

Do not enter stop mode or wait mode during erase-suspend.
When the FST7 in the FST register is set to 0 (busy (during programming or erasure execution), do not enter to stop mode or wait mode.

35.7.1.7 Programming and Erasure Voltage for Flash Memory

To perform programming and erasure, use VCC = 2.7 V to 5.5 V as the supply voltage. Do not perform programming and erasure at less than 2.7 V.

36. Electrical Characteristics

TBD

37. Usage Notes

37.1 Notes on Clock Generation Circuit

37.1.1 Oscillation Stop Detection Function

Since the oscillation stop detection function cannot be used when the XIN clock frequency is below 2 MHz, set bits OCD1 to OCD0 to 00b.

37.1.2 Oscillation Circuit Constants

Consult the oscillator manufacturer to determine the optimal oscillation circuit constants for the user system.
To use the MCU with supply voltage below VCC = 2.7 V, it is recommended to set the CM11 bit in the CM1 register to 1 (on-chip feedback resistor disabled) and connect the feedback resistor to the chip externally.

37.2 Notes on Power Control

37.2.1 Stop Mode

To enter stop mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and then the CM10 bit in the CM1 register to 1 (stop mode). An instruction queue pre-reads 4 bytes from the instruction which sets the CM10 bit to 1 (stop mode) and the program stops.
Insert at least four NOP instructions following the JMP.B instruction after the instruction which sets the CM10 bit to 1.

- Program example to enter stop mode
```
BCLR 1, FMR0; CPU rewrite mode disabled
BSET 0, PRCR; Protect disabled
FSET I; Enable interrupt
BSET 0, CM1; Stop mode
JMP.B LABEL_001
LABEL_001:
NOP
NOP
NOP
NOP
```

37.2.2 Wait Mode

To enter wait mode with the WAIT instruction, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and then execute the WAIT instruction. An instruction queue pre-reads 4 bytes from the WAIT instruction and the program stops. Insert at least four NOP instructions after the WAIT instruction.

- Program example to execute the WAIT instruction
```
BCLR 1, FMR0; CPU rewrite mode disabled
FSET I; Enable interrupt
WAIT; Wait mode
NOP
NOP
NOP
NOP
```

37.2.3 Power-Off Mode

To enter power-off mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and then access the POMCR0 register. A period of a few microseconds is required between accessing the POMCR0 register and entering power-off mode. As the CPU continues to operate during this period, insert the NOP and the WAIT instructions to stop the program.

- Program example to enter power-off mode (when timer RE and the low-speed clock is enabled)
```
BCLR 1, FMR0; CPU rewrite mode disabled
MOV. B #08H, POMCR0; Select power-off 0 and WKUP1 input enabled
MOV. B #88H, POMCR0; Fixed value
MOV. B #15H, POMCR0; Fixed value
MOV. B #92H, POMCR0; Fixed value
MOV. B #25H, POMCR0; Fixed value
NOP;
NOP;
NOP;
NOP; Enter power-off mode
WAIT; Wait mode
```

37.3 Notes on Interrupts

37.3.1 Reading Address 00000h

Do not read address 00000h by a program. When a maskable interrupt request is acknowledged, the CPU reads interrupt information (interrupt number and interrupt request level) from 00000h in the interrupt sequence. At this time, the IR bit for the acknowledged interrupt is set to 0.
If address 00000h is read by a program, the IR bit for the interrupt which has the highest priority among the enabled interrupts is set to 0. This may cause the interrupt to be canceled, or an unexpected interrupt to be generated.

37.3.2 SP Setting

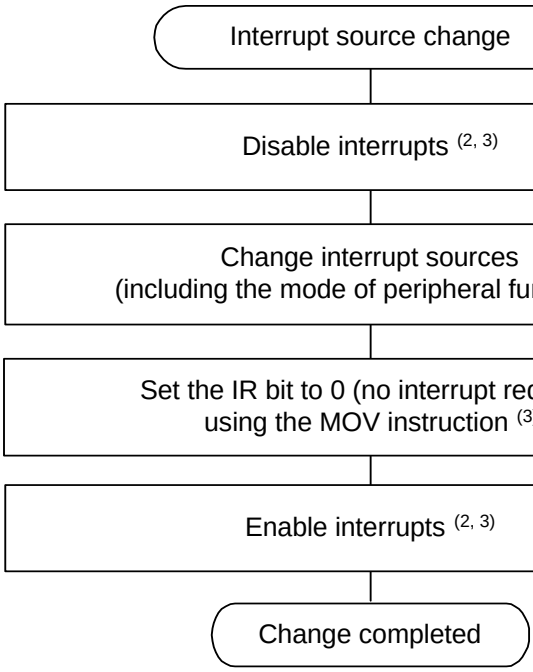
Set a value in the SP before an interrupt is acknowledged. The SP is set to 0000h after a reset. If an interrupt is acknowledged before setting a value in the SP, the program may run out of control.

37.3.3 External Interrupt, Key Input Interrupt

Either the low-level width or high-level width shown in the Electrical Characteristics is required for the signal input to pins $\overline{\text{INT0}}$ to $\overline{\text{INT7}}$ and pins $\overline{\text{KI0}}$ to $\overline{\text{KI7}}$, regardless of the CPU clock.
For details, refer to **Table 36.XX** (VCC = 5 V), **Table 36.XX** (VCC = 3 V), **Table 36.XX** (VCC = 1.8 V) **External Interrupt INTi (i = 0 to 7) Input**, **Key Input Interrupt KIi (i = 0 to 7)**.

37.3.4 Changing Interrupt Sources

The IR bit in the interrupt control register may be set to 1 (interrupt requested) when the interrupt source changes. To use an interrupt, set the IR bit to 0 (no interrupt requested) after changing interrupt sources.
Changing interrupt sources as referred to here includes all factors that change the source, polarity, or timing of the interrupt assigned to a software interrupt number. Therefore, if a mode change of a peripheral function involves the source, polarity, or timing of an interrupt, set the IR bit to 0 (no interrupt requested) after making these changes. Refer to the descriptions of the individual peripheral functions for related interrupts.
Figure 37.1 shows a Procedure Example for Changing Interrupt Sources.



IR bit: Bit in the interrupt control register bit for the interrupt whose source is to be changed

Notes:
1. The above settings must be executed individually. Do not execute two or more settings simultaneously (using one instruction).
2. To prevent interrupt requests from being generated, disable the peripheral function before changing the interrupt source. In this case, use the I flag if all maskable interrupts can be disabled.
   If all maskable interrupts cannot be disabled, use bits ILVL0 to ILVL2 for the interrupt whose source is to be changed.
3. Refer to **12.8.5 Rewriting Interrupt Control Register** for the instructions to use and related notes.

Figure 37.1 Procedure Example for Changing Interrupt Sources

37.3.5 Rewriting Interrupt Control Register

(a) The contents of the interrupt control register can be rewritten only while no interrupt requests corresponding to that register are generated. If an interrupt request may be generated, disable the interrupt before rewriting the contents of the interrupt control register.

(b) When rewriting the contents of the interrupt control register after disabling the interrupt, be careful to choose appropriate instructions.
Changing any bit other than the IR bit
If an interrupt request corresponding to the register is generated while executing the instruction, the IR bit may not be set to 1 (interrupt requested), and the interrupt may be ignored. If this causes a problem, use one of the following instructions to rewrite the contents of the register:
AND, OR, BCLR, and BSET.

Changing the IR bit
Depending on the instruction used, the IR bit may not be set to 0 (no interrupt requested).
Use the MOV instruction to set the IR bit to 0.

(c) When using the I flag to disable an interrupt, set the I flag as shown in the sample programs below.
Refer to (b) regarding rewriting the contents of interrupt control registers using the sample programs.

Examples 1 to 3 shows how to prevent the I flag from being set to 1 (interrupts enabled) before the contents of the interrupt control register are rewritten for the effects of the internal bus and the instruction queue buffer.

Example 1: Use the NOP instructions to pause program until the interrupt control register is rewritten

```
INT_SWITCH1:
    FCLR    I               ; Disable interrupts
    AND.B   #00H,0056H      ; Set the TRAIC register to 00h
    NOP                     ;
    NOP
    FSET    I               ; Enable interrupts
```

Example 2: Use a dummy read to delay the FSET instruction

```
INT_SWITCH2:
    FCLR    I               ; Disable interrupts
    AND.B   #00H,0056H      ; Set the TRAIC register to 00h
    MOV.W   MEM,R0          ; Dummy read
    FSET    I               ; Enable interrupts
```

Example 3: Use the POPC instruction to change the I flag

```
INT_SWITCH3:
    PUSHC   FLG
    FCLR    I               ; Disable interrupts
    AND.B   #00H,0056H      ; Set the TRAIC register to 00h
    POPC    FLG             ; Enable interrupts
```

37.4 Notes on ID Code Areas

37.4.1 Setting Example of ID Code Areas

As the ID code areas are allocated in the flash memory (not in the SFRs), they cannot be rewritten by executing an instruction. Write appropriate values when creating a program. The following shows a setting example.

- To set 55h in all of the ID code areas

```
.org 00FFDCH
.lword dummy | (55000000h)    ; UND
.lword dummy | (55000000h)    ; INTO
.lword dummy ; BREAK
.lword dummy | (55000000h)    ; ADDRESS MATCH
.lword dummy | (55000000h)    ; SET SINGLE STEP
.lword dummy | (55000000h)    ; WDT
.lword dummy | (55000000h)    ; ADDRESS BREAK
.lword dummy | (55000000h)    ; RESERVE
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

37.5 Notes on Option Function Select Area

37.5.1 Setting Example of Option Function Select Area

As the option function select area is allocated in the flash memory (not in the SFRs), they cannot be rewritten by executing an instruction. Write appropriate values when creating a program. The following shows a setting example.

- To set FFh in the OFS register

```
.org 00FFFCH
.lword reset | (0FF000000h)     ; RESET
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

37.6 Notes on DTC

37.6.1 DTC activation source

- Do not generate any DTC activation sources before entering wait mode or during wait mode.
- Do not generate any DTC activation sources before entering stop mode or during stop mode.

37.6.2 DTCENi (i = 0 to 6) Registers

- Modify bits DTCENi0 to DTCENi7 only while an interrupt request corresponding to the bit is not generated.
- When the interrupt source flag in the status register for the peripheral function is 1, do not modify the corresponding activation source bit among bits DTCENi0 to DTCENi7.
- Do not access the DTCENi register using a DTC transfer.

37.6.3 Peripheral Modules

- Do not set the status register bit for the peripheral function to 0 using a DTC transfer.
- When the DTC activation source is SSU/I^{2}C bus receive data full, read the SSRDR register/the ICDRR register using a DTC transfer.
  The RDRF bit in the SSSR register/the ICSR register is set to 0 (no data in SSRDR/ICDRR register) by reading the SSRDR register/the ICDRR register.
  However, the RDRF bit is not set to 0 by reading the SSRDR register/the ICDRR register when the DTC data transfer setting is either of the following:
  - Transfer causing the DTCCTj (j = 0 to 23) register value to change from 1 to 0 in normal mode
  - Transfer causing the DTCCRj register value to change from 1 to 0 while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled) in repeat mode.
- When the DTC activation source is SSU/I^{2}C bus transmit data empty, write to the SSTDR register/the ICDRT register using a DTC transfer. The TDRE bit in the SSSR register/the ICSR register is set to 0 (data is not transferred from registers SSTDR/ICDRT to SSTRSR/ICDRS) by writing to the SSTDR register/the ICDRT register.

37.7 Notes on Timer RA

- Timer RA stops counting after a reset. Set the values in the timer RA and timer RA prescalers before the count starts.
- Even if the prescaler and timer RA are read out in 16-bit units, these registers are read 1 byte at a time in the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In pulse period measurement mode, bits TEDGF and TUNDF in the TRACR register can be set to 0 by writing 0 to these bits by a program. However, these bits remain unchanged if 1 is written. When using the READ-MODIFY-WRITE instruction for the TRACR register, the TEDGF or TUNDF bit may be set to 0 although these bits are set to 1 while the instruction is being executed. In this case, write 1 to the TEDGF or TUNDF bit which is not supposed to be set to 0 with the MOV instruction.
- When changing to pulse period measurement mode from another mode, the contents of bits TEDGF and TUNDF are undefined. Write 0 to bits TEDGF and TUNDF before the count starts.
- The TEDGF bit may be set to 1 by the first timer RA prescaler underflow generated after the count starts.
- When using the pulse period measurement mode, leave two or more periods of the timer RA prescaler immediately after the count starts, then set the TEDGF bit to 0.
- The TCSTF bit remains 0 (count stops) for zero or one cycle of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.
  During this time, do not access registers associated with timer RA (1) other than the TCSTF bit. Timer RA starts counting at the first active edge of the count source after The TCSTF bit is set to 1 (during count operation).
  The TCSTF bit remains 1 for zero or one cycle of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RA counting is stopped when the TCSTF bit is set to 0.
  During this time, do not access registers associated with timer RA (1) other than the TCSTF bit.

  Note:
  1. Registers associated with timer RA:
     TRACR, TRAIOC, TRAMR, TRAPRE, and TRA

- When the TRAPRE register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source clock for each write interval.
- When the TRA register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the prescaler underflow for each write interval.

37.8 Notes on Timer RB

- Timer RB stops counting after a reset. Set the values in the timer RB and timer RB prescalers before the count starts.
- Even if the prescaler and timer RB is read out in 16-bit units, these registers are read 1 byte at a time in the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In programmable one-shot generation mode and programmable wait one-shot generation mode, when setting the TSTART bit in the TRBCR register to 0 (count stops) or setting the TOSSP bit in the TRBOCR register to 1 (one-shot stops), the timer reloads the value of reload register and stops. Therefore, in programmable one-shot generation mode and programmable wait one-shot generation mode, read the timer count value before the timer stops.
- The TCSTF bit remains 0 (count stops) for one or two cycles of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.
  During this time, do not access registers associated with timer RB (1) other than the TCSTF bit. Timer RB starts counting at the first active edge of the count source after the TCSTF bit is set to 1 (during count operation).
  The TCSTF bit remains 1 for one or two cycles of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RB counting is stopped when the TCSTF bit is set to 0.
  During this time, do not access registers associated with timer RB (1) other than the TCSTF bit.

  Note:
  1. Registers associated with timer RB:
     TRBCR, TRBOCR, TRBIOC, TRBMR, TRBPRE, TRBSC, and TRBPR

- When the TSTOP bit in the TRBCR register is set to 1 during timer operation, timer RB stops immediately.
- When 1 is written to the TOSST or TOSSP bit in the TRBOCR register, the value of the TOSSTF bit changes after one or two cycles of the count source have elapsed. When 1 is written to the TOSSP bit during the period between when 1 is written to the TOSST bit and when the TOSSTF bit is set to 1, the TOSSTF bit may be set to either 0 or 1 depending on the content state. Likewise, when 1 is written to the TOSST bit during the period between when 1 is written to the TOSSP bit and when the TOSSTF bit is set to 0, the TOSSTF bit may be set to either 0 or 1.

37.8.1 Timer Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

37.8.2 Programmable Waveform Generation Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

37.8.3 Programmable One-Shot Generation Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following:

- When the TRBPRE register is written continuously during count operation, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously during count operation, allow three or more cycles of the prescaler underflow for each write interval.

37.8.4 Programmable Wait One-shot Generation Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

37.9 Notes on Timer RC

37.9.1 TRC Register

- The following note applies when the CCLR bit in the TRCCR1 register is set to 1 (TRC register cleared by compare match with TRCGRA register).
  When using a program to write a value to the TRC register while the TSTART bit in the TRCMR register is set to 1 (count starts), ensure that the write does not overlap with the timing with which the TRC register is set to 0000h.
  If the timing of the write to the TRC register and the setting of the TRC register to 0000h coincide, the write value will not be written to the TRC register and the TRC register will be set to 0000h.

- Reading from the TRC register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```
Program Example     MOV.W   #XXXXh, TRC    ;Write
                    JMP.B   L1             ;JMP.B instruction
                L1: MOV.W   TRC,DATA       ;Read
```

37.9.2 TRCSR Register

Reading from the TRCSR register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```
Program Example     MOV.B   #XXh, TRCSR    ;Write
                    JMP.B   L1             ;JMP.B instruction
                L1: MOV.B   TRCSR,DATA     ;Read
```

37.9.3 TRCCR1 Register

To set bits TCK2 to TCK0 in the TRCCR1 register to 111b (fOCO-F), set fOCO-F to the clock frequency higher than the CPU clock frequency.

37.9.4 Count Source Switching

- Stop the count before switching the count source.

Switching procedure
(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.

- After switching the count source from fOCO40M to another clock, allow two or more cycles of f1 to elapse after changing the clock setting before stopping fOCO40M.

Switching procedure
(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.
(3) Wait for two or more cycles of f1.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

37.9.5 Input Capture Function

- The pulse width of the input capture signal should be set to three cycles or more of the timer RC operation clock (refer to **Table 20.1 Timer RC Operating Clocks**).
- The value of the TRC register is transferred to the TRCGRj register one or two cycles of the timer RC operation clock after the input capture signal is input to the TRCIOj (j = A, B, C, or D) pin (when the digital filter function is not used).

37.9.6 TRCMR Register in PWM2 Mode

When the CSEL bit in the TRCCR2 register is set to 1 (count stops at compare match with the TRCGRA register), do not set the TRCMR register at compare match timing of registers TRC and TRCGRA.

37.10 Notes on Timer RD

37.10.1 TRDSTR Register

- Set the TRDSTR register using the MOV instruction.

- When the CSELi (i = 0 or 1) is set to 0 (count stops at compare match between registers TRDi and TRDGRAi), the count does not stop and the TSTARTi bit remains unchanged even if 0 (count stops) is written to the TSTARTi bit.
  When the CSELi bit is set to 0, write 0 to the TSTARTi bit to change other bits without changing the TSTARTi bit.
  To stop counting by a program, write 0 to the TSTARTi bit after setting the CSELi bit to 1. If 1 is written to the CSELi bit and 0 is written to the TSTARTi bit is set to 0 at the same time (with one instruction), the count cannot be stopped.

- Table 37.1 lists the TRDIOji (j = A, B, C, or D) Pin Output Level when Count Stops while the TRDIOji (j = A, B, C, or D) pin is used for the timer RD output.

Table 37.1 TRDIOji (j = A, B, C, or D) Pin Output Level when Count Stops

Stopping Count	TRDIOji Pin Output when Count Stops
When the CSELi bit is set to 1, write 0 to the TSTARTi bit and the count stops.	Holds the output level immediately before the count stops.
When the CSELi bit is set to 0, the count stops at compare match between registers TRDi and TRDGRAi.	Holds the output level after the output changes by the compare match.

37.10.2 TRDi Register (i = 0 or 1)

- When writing the value to the TRDi register by a program while the TSTARTi bit in the TRDSTR register is set to 1 (count starts), avoid overlapping with the timing for setting the TRDi register to 0000h, and then write. If the timing for setting the TRDi register to 0000h overlaps with the timing for writing the value to the TRDi register, the value is not written and the TRDi register is set to 0000h.
  These notes apply when selecting the following by bits CCLR2 to CCLR0 in the TRDCRi register.
  - 001b (Clear by the TRDi register at compare match with the TRDGRAi register.)
  - 010b (Clear by the TRDi register at compare match with the TRDGRBi register.)
  - 011b (Synchronous clear)
  - 101b (Clear by the TRDi register at compare match with the TRDGRCi register.)
  - 110b (Clear by the TRDi register at compare match with the TRDGRDi register.)

- When writing the value to the TRDi register and continuously reading the same register, the value before writing may be read. In this case, execute the JMP.B instruction between the writing and reading.

```
Program example     MOV.W   #XXXXh, TRD0     ;Write
                    JMP.B   L1               ;JMP.B
                L1: MOV.W   TRD0,DATA        ;Read
```

37.10.3 TRDSRi Register (i = 0 or 1)

When writing the value to the TRDSRi register and continuously reading the same register, the value before writing may be read. In this case, execute the JMP.B instruction between the writing and reading.

```
Program example     MOV.B   #XXh, TRDSR0     ;Write
                    JMP.B   L1               ;JMP.B
                L1: MOV.B   TRDSR0,DATA      ;Read
```

37.10.4 Count Source Switching

• Switch the count source after the count stops.

Switching procedure

(1) Set the TSTARTi (i = 0 or 1) bit in the TRDSTR register to 0 (count stops).
(2) Change bits TCK2 to TCK0 in the TRDCRi register.

• When changing the count source from fOCO40M to another source and stopping fOCO40M, wait two or more cycles of f1 after setting the clock switch, and then stop fOCO40M.

Switching procedure

(1) Set the TSTARTi (i = 0 or 1) bit in the TRDSTR register to 0 (count stops).
(2) Change bits TCK2 to TCK0 in the TRDCRi register.
(3) Wait for two or more cycles of f1.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

37.10.5 Input Capture Function

• The pulse width of the input capture signal should be set to three or more cycles of the timer RD operating clock (refer to **Table 21.1 Timer RD Operating Clocks**).
• The value of the TRDi register is transferred to the TRDGRji register two or three cycles of the timer RD operating clock after the input capture signal is applied to the TRDIOji pin (i = 0 or 1, j = either A, B, C, or D) (when the digital filter is not used).

37.10.6 Reset Synchronous PWM Mode

• When reset synchronous PWM mode is used for motor control, make sure OLS0 = OLS1.
• Set to reset synchronous PWM mode by the following procedure:

Switching procedure

(1) Set the TSTART0 bit in the TRDSTR register to 0 (count stops).
(2) Set bits CMD1 to CMD0 in the TRDFCR register to 00b (timer mode, PWM mode, and PWM3 mode).
(3) Set bits CMD1 to CMD0 to 01b (reset synchronous PWM mode).
(4) Set the other registers associated with timer RD again.

37.10.7 Complementary PWM Mode

- When complementary PWM mode is used for motor control, make sure OLS0 = OLS1.
- Change bits CMD1 to CMD0 in the TRDFCR register in the following procedure.

Switching procedure: When setting to complementary PWM mode (including re-set), or changing the transfer timing from the buffer register to the general register in complementary PWM mode.

(1) Set both the TSTART0 and TSTART1 bits in the TRDSTR register to 0 (count stops).
(2) Set bits CMD1 to CMD0 in the TRDFCR register to 00b (timer mode, PWM mode, and PWM3 mode).
(3) Set bits CMD1 to CMD0 to 10b or 11b (complementary PWM mode).
(4) Set the registers associated with other timer RD again.

Switching procedure: When stopping complementary PWM mode

(1) Set both the TSTART0 and TSTART1 bits in the TRDSTR register to 0 (count stops).
(2) Set bits CMD1 to CMD to 00b (timer mode, PWM mode, and PWM3 mode).

- Do not write to TRDGRA0, TRDGRB0, TRDGRA1, or TRDGRB1 register during operation.
  When changing the PWM waveform, transfer the values written to registers TRDGRD0, TRDGRC1, and TRDGRD1 to registers TRDGRB0, TRDGRA1, and TRDGRB1 using the buffer operation.
  However, to write data to the TRDGRD0, TRDGRC1, or TRDGRD1 register, set bits BFD0, BFC1, and BFD1 to 0 (general register). After this, bits BFD0, BFC1, and BFD1 may be set to 1 (buffer register).
  The PWM period cannot be changed.

- If the value set in the TRDGRA0 register is assumed to be m, the TRD0 register counts m-1, m, m+1, m, m-1, in that order, when changing from increment to decrement operation.
  When changing from m to m+1, the IMFA bit is set to 1. Also, bits CMD1 to CMD0 in the TRDFCR register are set to 11b (complementary PWM mode, buffer data transferred at compare match between registers TRD0 and TRDGRA0), the content of the buffer registers (TRDGRD0, TRDGRC1, and TRDGRD1) is transferred to the general registers (TRDGRB0, TRDGRA1, and TRDGRB1).
  During m+1, m, and m-1 operation, the IMFA bit remains unchanged and data are not transferred to registers such as the TRDGRA0 register.

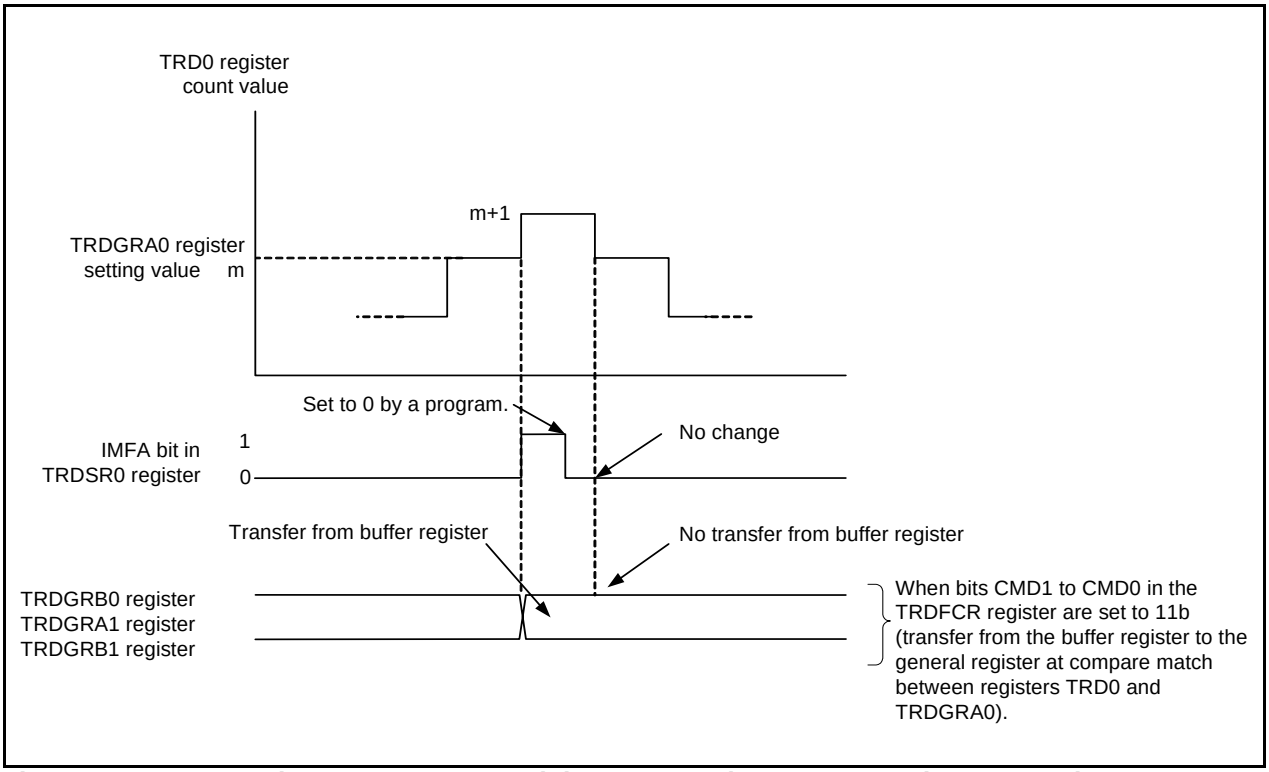


Figure 37.2 Operation at Compare Match between Registers TRD0 and TRDGRA0 in Complementary PWM Mode

- The TRD1 register counts 1, 0, FFFFh, 0, 1, in that order, when changing from decrement to increment operation.

  The UDF bit is set to 1 when changing between 1, 0, and FFFFh operation. Also, when bits CMD1 to CMD0 in the TRDFCR register are set to 10b (complementary PWM mode, buffer data transferred at underflow in the TRD1 register), the content of the buffer registers (TRDGRD0, TRDGRC1, and TRDGRD1) is transferred to the general registers (TRDGRB0, TRDGRA1, and TRDGRB1). During FFFFh, 0, 1 operation, data are not transferred to registers such as the TRDGRB0 register. Also, at this time, the OVF bit remains unchanged.

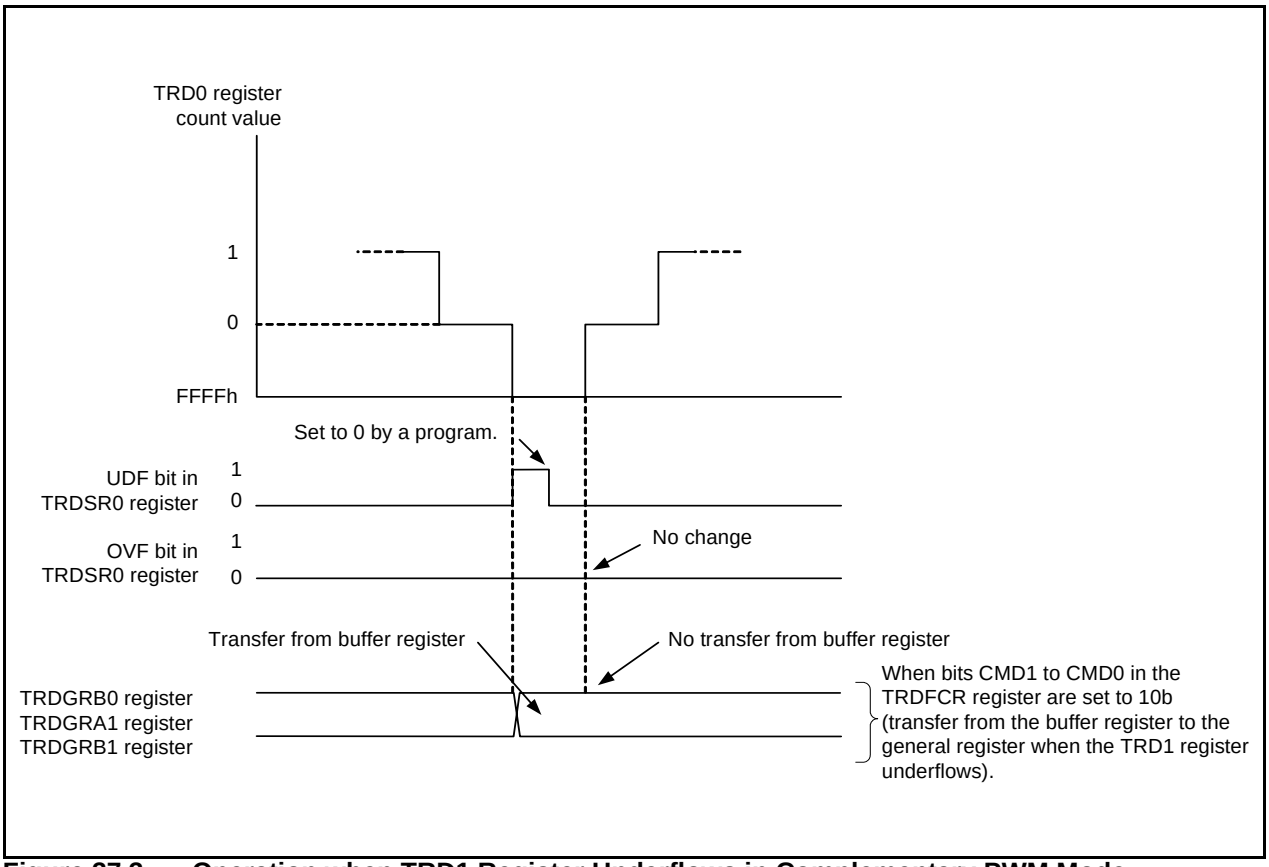


Figure 37.3 Operation when TRD1 Register Underflows in Complementary PWM Mode

- Using bits CMD1 to CMD0, select the timing of data transfer from the buffer register to the general register. However, transfer takes place with the following timing in spite of the values of bits CMD1 to CMD0 in the following cases:

  Buffer register value ≥ TRDGRA0 register value:
  Transfer takes place at underflow of the TRD1 register.
  After this, when the buffer register is set to 0001h or above and a value smaller than the value of the TRDGRA0 register, and the TRD1 register underflows for the first time after setting, the value is transferred to the general register. After that, the value is transferred with the timing selected by bits CMD1 to CMD0.

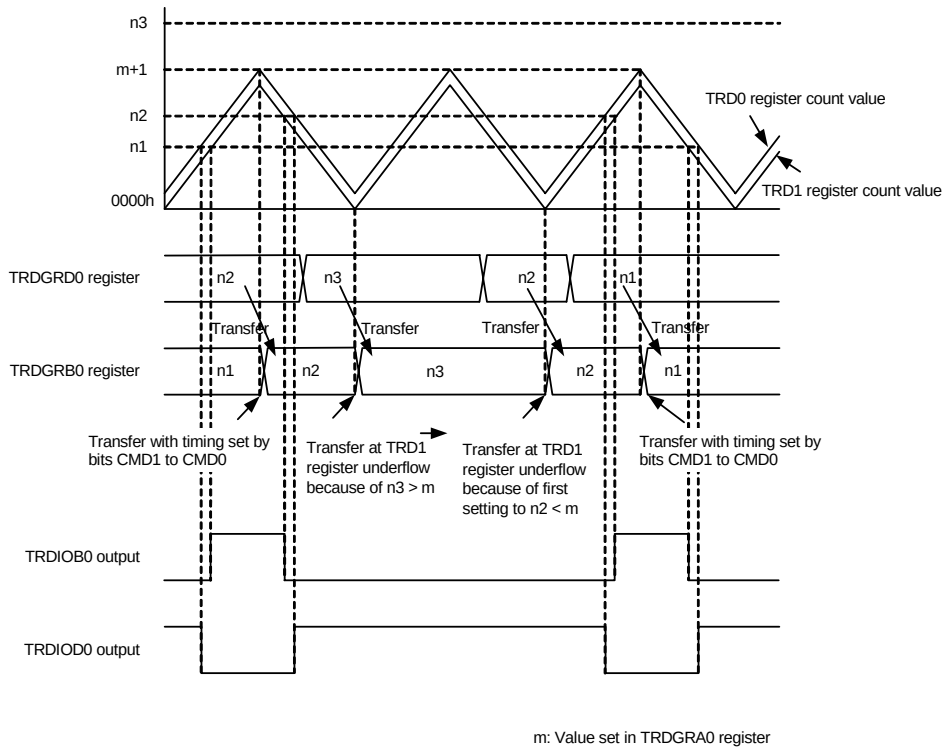


Figure 37.4 Operation when Buffer Register Value ≥ TRDGRA0 Register Value in Complementary PWM Mode

When the value of the buffer register is set to 0000h:
Transfer takes place at compare match between registers TRD0 and TRDGRA0.
After this, when the buffer register is set to 0001h or above and a value than smaller the value of the TRDGRA0 register, and a compare match occurs between registers TRD0 and TRDGRA0 for the first time after setting, the value is transferred to the general register. After that, the value is transferred with the timing selected by bits CMD0 and CMD1.

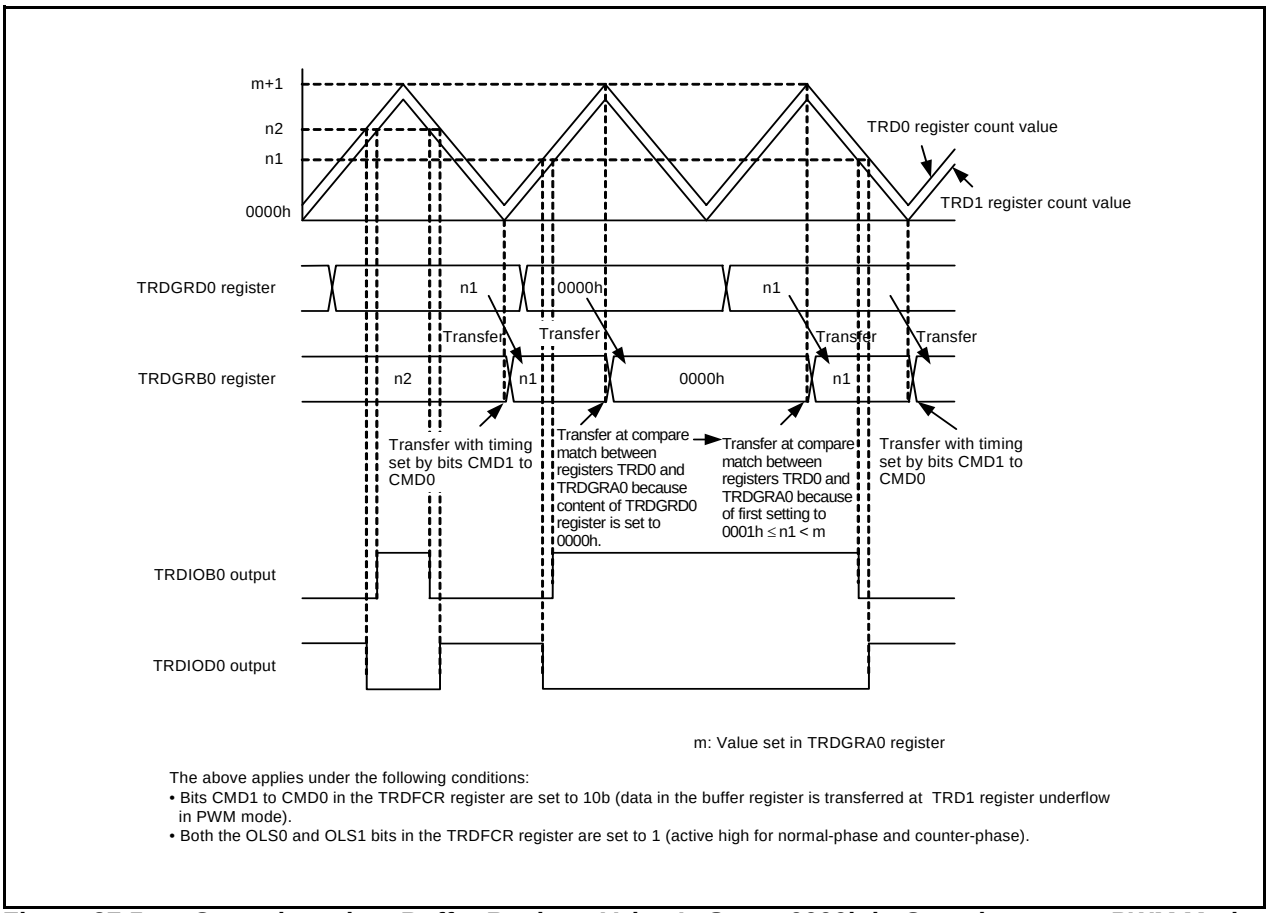


Figure 37.5 Operation when Buffer Register Value Is Set to 0000h in Complementary PWM Mode

37.10.8 Count Source fOCO40M

- The count source fOCO40M can be used with supply voltage VCC = 2.7 to 5.5 V. For supply voltage other than that, do not set bits TCK2 to TCK0 in registers TRDCR0 and TRDCR to 110b (fOCO40M selected as the count source).

37.11 Notes on Timer RE

37.11.1 Reset

A reset input does not reset the timer RE data registers that store data of seconds, minutes, hours, and days of the week. This requires the initial setting of all registers after power on.

37.11.2 Starting and Stopping Count

Timer RE has the TSTART bit for instructing the count to start or stop, and the TCSTF bit, which indicates count start or stop. Bits TSTART and TCSTF are in the TRECR1 register.
When the TSTART bit is set to 1 (count starts), timer RE starts counting and the TCSTF bit is set to 1 (count starts). It takes up to two cycles of the count source until the TCSTF bit is set to 1 after setting the TSTART bit to 1. During this time, do not access registers associated with timer RE (1) other than the TCSTF bit.
Similarly, when the TSTART bit is set to 0 (count stops), timer RE stops counting and the TCSTF bit is set to 0 (count stops). It takes the time for up to two cycles of the count source until the TCSTF bit is set to 0 after setting the TSTART bit to 0. During this time, do not access registers associated with timer RE other than the TCSTF bit.

Note:
1. Registers associated with timer RE:
   TRESEC, TREMIN, TREHR, TREWK, TRECR1, TRECR2, and TRECSR

37.11.3 Register Setting

Write to the following registers or bits while timer RE is stopped.

- Registers TRESEC, TREMIN, TREHR, TREWK, and TRECR2
- Bits H12_H24, PM, and INT in the TRECR1 register
- Bits RCS0 to RCS3 in the TRECSR register

Timer RE is stopped while bits TSTART and TCSTF in the TRECR1 register are set to 0 (timer RE stopped).

Set all above-mentioned registers and bits (immediately before timer RE count starts) before setting the TRECR2 register.
Figure 37.6 shows a Setting Example in Real-Time Clock Mode.

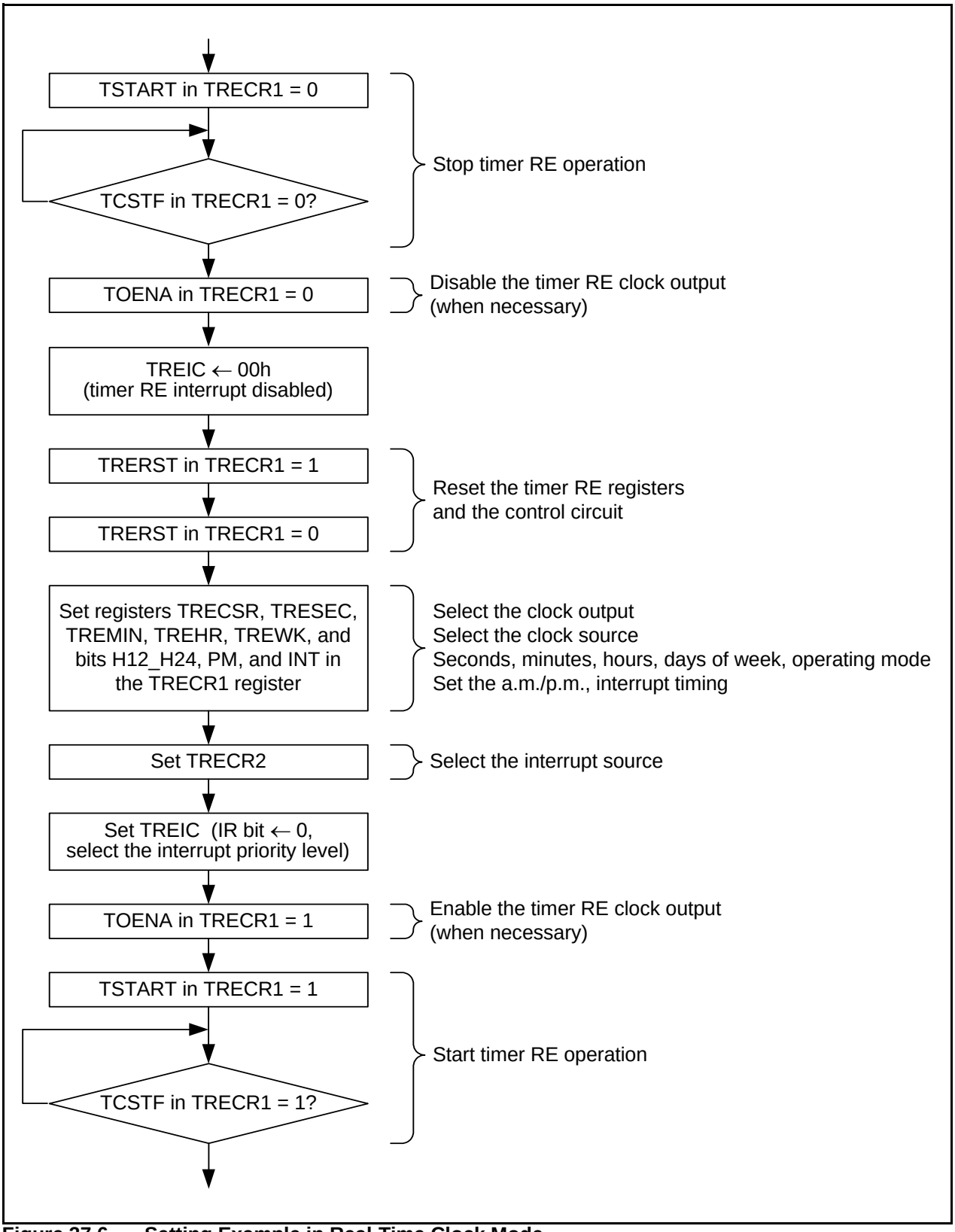


Figure 37.6 Setting Example in Real-Time Clock Mode

37.11.4 Time Reading Procedure in Real-Time Clock Mode

In real-time clock mode, read registers TRESEC, TREMIN, TREHR, and TREWK when time data is updated and read the PM bit in the TRECR1 register when the BSY bit is set to 0 (data is not being updated).
When reading several registers, an incorrect time will be read if data is updated before another register is read after reading any register.
In order to prevent this, use the reading procedure shown below.

- Using an interrupt
  Read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register in the timer RE interrupt routine.

- Monitoring with a program 1
  Monitor the IR bit in the TREIC register with a program and read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register after the IR bit in the TREIC register is set to 1 (timer RE interrupt request generated).

- Monitoring with a program 2

(1) Monitor the BSY bit.
(2) Monitor until the BSY bit is set to 0 after the BSY bit is set to 1 (approximately 62.5 ms while the BSY bit is set to 1).
(3) Read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register after the BSY bit is set to 0.

- Using read results if they are the same value twice

(1) Read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register.
(2) Read the same register as (1) and compare the contents.
(3) Recognize as the correct value if the contents match. If the contents do not match, repeat until the read contents match with the previous contents.

Also, when reading several registers, read them as continuously as possible.

37.12 Notes on Timer RG

37.12.1 Phase Difference, Overlap, and Pulse Width in Phase Counting Mode

The phase difference and overlap between the external input signals from pins TRGCLKA and TRGCLKB should be 1.5 f1 or more, respectively. The pulse width should be 2.5 f1 or more. Figure 37.7 shows the Phase Difference, Overlap, and Pulse Width in Phase Counting Mode.

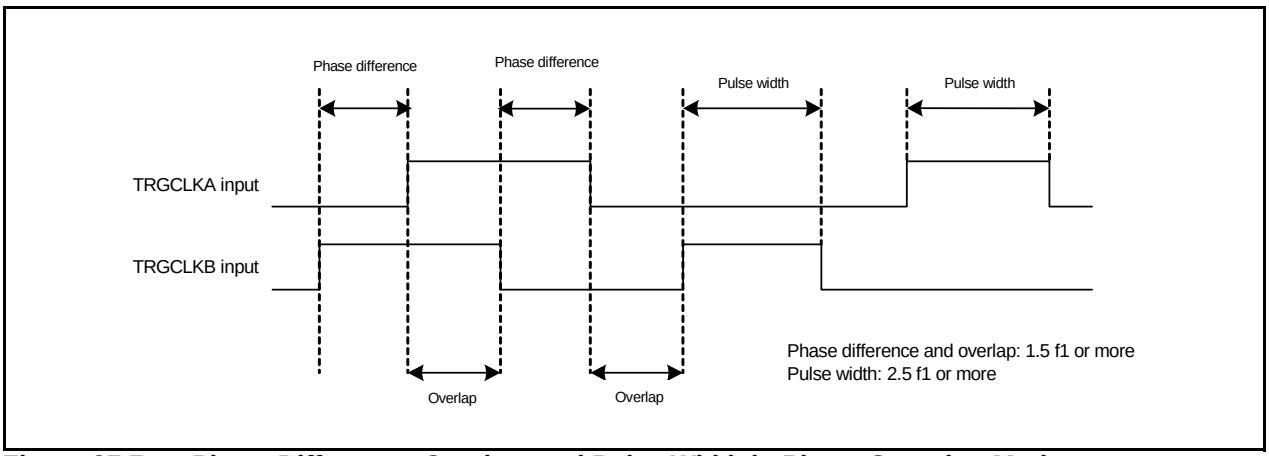


Figure 37.7 Phase Difference, Overlap, and Pulse Width in Phase Counting Mode

37.13 Notes on Serial Interface (UARTi (i = 0 or 1))

- When reading data from the UiRB (i = 0 or 1) register either in clock synchronous serial I/O mode or in clock asynchronous serial I/O mode, always read data in 16-bit units.
  When the high-order byte of the UiRB register is read, bits PER and FER in the UiRB register and the RI bit in the UiC1 register are set to 0.
  To check receive errors, read the UiRB register and then use the read data.

  Program example to read the receive buffer register:
  ```
  MOV.W    00A6H,R0    ; Read the U0RB register
  ```

- When writing data to the UiTB register in clock asynchronous serial I/O mode with 9-bit transfer data length, write data to the high-order byte first and then the low-order byte, in 8-bit units.

  Program example to write to the transmit buffer register:
  ```
  MOV.B    #XXH,00A3H    ; Write to the high-order byte of the U0TB register
  MOV.B    #XXH,00A2H    ; Write to the low-order byte of the U0TB register
  ```

37.14 Notes on Serial Interface (UART2)

37.14.1 Clock Synchronous Serial I/O Mode

37.14.1.1 Transmission/Reception

When the $\overline{\text{RTS}}$ function is used with an external clock, the $\overline{\text{RTS2}}$ pin outputs a low-level signal, which informs the transmitting side that the MCU is ready for a receive operation. The $\overline{\text{RTS2}}$ pin outputs a high-level signal when a receive operation starts. Therefore, the transmit timing and receive timing can be synchronized by connecting the $\overline{\text{RTS2}}$ pin to the $\overline{\text{CTS2}}$ pin of the transmitting side. The $\overline{\text{RTS}}$ function is disabled when an internal clock is selected.

37.14.1.2 Transmission

If an external clock is selected, the following conditions must be met while the external clock is held high when the CKPOL bit in the U2C0 register is set to 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock), or while the external clock is held low when the CKPOL bit is set to 1 (transmit data output at the rising edge and receive data input at the falling edge of the transfer clock).

- The TE bit in the U2C1 register is set to 1 (transmission enabled).
- The TI bit in the U2C1 register is set to 0 (data in the U2TB register).
- If the $\overline{\text{CTS}}$ function is selected, input to the $\overline{\text{CTS2}}$ pin is low.

37.14.1.3 Reception

In clock synchronous serial I/O mode, the shift clock is generated by activating the transmitter. Set the UART2-associated registers for transmission even if the MCU is used for reception only. Dummy data is output from the TXD2 pin during reception.

When an internal clock is selected, the shift clock is generated by setting the TE bit in the U2C1 register to 1 (transmission enabled) and setting dummy data in the U2TB register. When an external clock is selected, the shift clock is generated by setting the TE bit to 1 (transmission enabled), setting dummy data in the U2TB register, and inputting an external clock.

If data is received consecutively, an overrun error occurs when the RE bit in the U2C1 register is set to 1 (data in the U2RB register) and the next receive data is received in the UART2 receive register. Then, the OER bit in the U2RB register is set to 1 (overrun error). At this time, the U2RB register value is undefined. If an overrun error occurs, the IR bit in the S2RIC register remains unchanged.

To receive data consecutively, set dummy data in the low-order byte in the U2TB register per each receive operation.

If an external clock is selected, the following conditions must be met while the external clock is held high when the CKPOL bit is set to 0, or while the external clock is held low when the CKPOL bit is set to 1.

- The RE bit in the U2C1 register is set to 1 (reception enabled).
- The TE bit in the U2C1 register is set to 1 (transmission enabled).
- The TI bit in the U2C1 register is set to 0 (data in the U2TB register).

37.14.2 Clock Asynchronous Serial I/O (UART) Mode

37.14.2.1 Transmission/Reception

When the $\overline{\text{RTS}}$ function is used with an external clock, the $\overline{\text{RTS2}}$ pin outputs a low-level signal, which informs the transmitting side that the MCU is ready for a receive operation. The $\overline{\text{RTS2}}$ pin outputs a high-level signal when a receive operation starts. Therefore, the transmit timing and receive timing can be synchronized by connecting the $\overline{\text{RTS2}}$ pin to the $\overline{\text{CTS2}}$ pin of the transmitting side. The $\overline{\text{RTS}}$ function is disabled when an internal clock is selected.

37.14.2.2 Transmission

If an external clock is selected, the following conditions must be met while the external clock is held high when the CKPOL bit in the U2C0 register is set to 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock), or while the external clock is held low when the CKPOL bit is set to 1 (transmit data output at the rising edge and receive data input at the falling edge of the transfer clock).

- The TE bit in the U2C1 register is set to 1 (transmission enabled)
- The TI bit in the U2C1 register is set to 0 (data in the U2TB register)
- If the $\overline{\text{CTS}}$ function is selected, input on the $\overline{\text{CTS2}}$ pin is low.

37.14.3 Special Mode 1 (I^2C Mode)

To generate start, stop, and restart conditions, set the STSPSEL bit in the U2SMR4 register to 0 and wait for more than half cycle of the transfer clock before changing each condition generation bit (STAREQ, RSTAREQ, and STPREQ) from 0 to 1.

37.15 Notes on Synchronous Serial Communication Unit

To use the synchronous serial communication unit, set the IICSEL bit in the SSUIICSR register to 0 (SSU function selected).

37.16 Notes on I²C bus Interface

To use the I²C bus interface, set the IICSEL bit in the SSUIICSR register to 1 (I²C bus interface function selected).

37.17 Notes on Hardware LIN

For the time-out processing of the header and response fields, use another timer to measure the duration of time with a Synch Break detection interrupt as the starting point.

37.18 Notes on A/D Converter

- Write to the ADMOD, ADINSEL, ADCON0 (other than the ADST bit), ADCON1, or OCVREFCR register must be performed while A/D conversion is stopped (before a trigger occurs).
- To use the A/D converter in repeat mode 0, repeat mode 1, or repeat sweep mode, select the frequency of the A/D converter operating clock ϕAD or more for the CPU clock during A/D conversion.
  Do not select fOCO-F as ϕAD.
- Connect 0.1 μF capacitor between pins VREF and AVSS.
- Do not enter stop mode during A/D conversion.
- Do not enter wait mode during A/D conversion regardless of the state of the CM02 bit in the CM0 register (1: Peripheral function clock stops in wait mode or 0: Peripheral function clock does not stop in wait mode).
- Do not set the FMSTP bit in the FMR0 register to 1 (flash memory stops) during A/D conversion.

37.19 Notes on LCD Drive Control Circuit

37.19.1 Voltage Multiplier

The voltage multiplier boosts the VL1 pin voltage by charging/discharging the capacitor connected between pins CL1 and CL2. As a result, the expected level from the VL4 pin may not achieved when driving a large LCD panel. An external power source is recommended to obtain a stable power supply in these cases.

37.19.2 When Division Resistors are Connected Externally

Set the resistor value between pins VL4 and VCC (the total of R1 to R4 as shown in Figure 34.4) to the highest value 100 kΩ or more.

37.20 Notes on Flash Memory

37.20.1 CPU Rewrite Mode

37.20.1.1 Prohibited Instructions

The following instructions cannot be used while the program ROM area is being rewritten in EW0 mode because they reference data in the flash memory: UND, INTO, and BRK.

37.20.1.2 Non-Maskable Interrupts

Tables 37.2 and 37.3 list CPU Rewrite Mode Interrupts (1) and (2), respectively.

Table 37.2 CPU Rewrite Mode Interrupts (1)

Mode	Erase/ Write Target	Status	Maskable Interrupt	• Address Match • Address Break (Note 1)
EW0	Data flash	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request). The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0 (erase-suspend request disabled by interrupt request), set the FMR 21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read. Auto-erasure can be restarted by setting the FMR21 bit to 0 (erase restart).	
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.	
		During auto-programming		
	Program ROM	During auto-erasure (suspend enabled)	Usable by allocating a vector in RAM.	Not usable during auto-erasure or auto-programming.
		During auto-erasure (suspend disabled)		
		During auto-programming		
EW1	Data flash	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1, the FMR21 bit is automatically set to 1. The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0, set the FMR 21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read. Auto-erasure can be restarted by setting the FMR21 bit to 0.	
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.	
		During auto-programming		
	Program ROM	During auto-erasure (suspend enabled)	Auto-erasure suspends after td(SR-SUS) and interrupt handling is executed. Auto-erasure can be restarted by setting the FMR21 bit to 0 after interrupt handling completes. While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read.	
		During auto-erasure (suspend disabled or FMR22 = 0)	Auto-erasure and auto-programming have priority and interrupt requests are put on standby. Interrupt handling is executed after auto-erase and auto-program complete.	
		During auto-programming		

FMR21, FMR22: Bits in FMR2 register

Note:

1. Do not use a non-maskable interrupt while block 0 is being auto-erased because the fixed vector is allocated in block 0.

Table 37.3 CPU Rewrite Mode Interrupts (2)

Mode	Erase/ Write Target	Status	• Watchdog Timer • Oscillation Stop Detection • Voltage Monitor 2 • Voltage Monitor 1 • NMI (Note 1)	• Undefined Instruction • INTO Instruction • BRK Instruction • Single Step (Note 1)
EW0	Data flash	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request). The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0 (erase-suspend request disabled by interrupt request), set the FMR 21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read. Auto-erasure can be restarted by setting the FMR21 bit is set to 0 (erase restart).	
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.	
		During auto-programming		
	Program ROM	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period. Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally. The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the erase-suspend function.	Not usable during auto-erasure or auto-programming.
		During auto-erasure (suspend disabled)		
		During auto-programming		
EW1	Data flash	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1, the FMR21 bit is automatically set to 1. The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0, set the FMR 21 bit to 1 during interrupt handling. The flash memory suspends auto-programming after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read. Auto-erasure can be restarted by setting the FMR21 bit is set to 0.	
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.	
		During auto-programming		
	Program ROM	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period. Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally. The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the erase-suspend function.	Not usable during auto-erasure or auto-programming.
		During auto-erasure (suspend disabled or FMR22 = 0)		
		During auto-programming		

FMR21, FMR22: Bits in FMR2 register

Note:

1. Do not use a non-maskable interrupt while block 0 is being auto-erased because the fixed vector is allocated in block 0.

37.20.1.3 How to Access

To set one of the following bits to 1, first write 0 and then 1 immediately. Do not generate an interrupt between writing 0 and writing 1.

- The FMR01 or FMR02 bit in the FMR0 register
- The FMR13 bit in the FMR1 register
- The FMR20, FMR22, or FMR 27 bit in the FMR2 register

To set one of the following bits to 0, first write 1 and then 0 immediately. Do not generate an interrupt between writing 1 and writing 0.

- The FMR14, FMR15, FMR16, or FMR17 bit in the FMR1 register

37.20.1.4 Rewriting User ROM Area

In EW0 Mode, if the supply voltage drops while rewriting any block in which a rewrite control program is stored, it may not be possible to rewrite the flash memory because the rewrite control program cannot be rewritten correctly. In this case, use standard serial I/O mode.

37.20.1.5 Programming

Do not write additions to the already programmed address.

37.20.1.6 Entering Stop Mode or Wait Mode

Do not enter stop mode or wait mode during erase-suspend.
When the FST7 in the FST register is set to 0 (busy (during programming or erasure execution), do not enter to stop mode or wait mode.

37.20.1.7 Programming and Erasure Voltage for Flash Memory

To perform programming and erasure, use VCC = 2.7 V to 5.5 V as the supply voltage. Do not perform programming and erasure at less than 2.7 V.

37.21 Notes on Noise

37.21.1 Inserting Bypass Capacitor between Pins VCC and VSS as Countermeasure against Noise and Latch-up

Connect a bypass capacitor (at least 0.1 μF) using the shortest and thickest write possible.

37.21.2 Countermeasures against Noise Error of Port Control Registers

During rigorous noise testing or the like, external noise (mainly power supply system noise) can exceed the capacity of the MCU internal noise control circuitry. In such cases the contents of the port related registers may be changed.

As a firmware countermeasure, it is recommended that the port registers, port direction registers, and pull-up control registers be reset periodically. However, examine the control processing fully before introducing the reset routine as conflicts may be created between the reset routine and interrupt routines.

38. Notes on On-Chip Debugger

When using the on-chip debugger to develop and debug programs for the R8C/L35A Group, R8C/L35B Group, R8C/L36A Group, R8C/L36B Group, R8C/L38A Group, R8C/L38B Group, R8C/L3AA Group, R8C/L3AB Group, take note of the following:

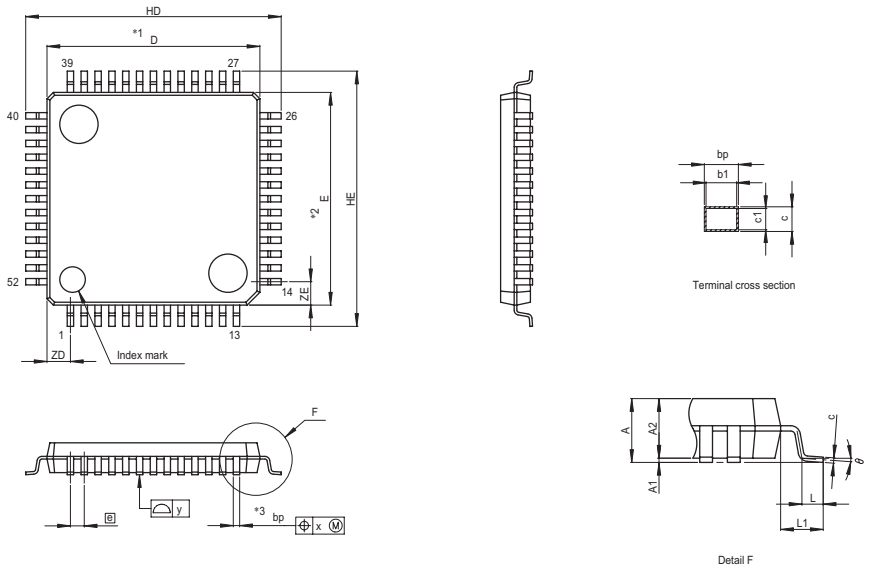
(1) Some of the user flash memory and RAM areas are used by the on-ship debugger. These areas cannot be accessed by the user.
Refer to the on-chip debugger manual for which areas are used.
(2) Do not set the address match interrupt (registers AIER0, AIER1, RMAD0, and RMAD1 and fixed vector tables) in a user system.
(3) Do not use the BRK instruction in a user system.
(4) Debugging is available under the condition of supply voltage VCC = 1.8 to 5.5 V. Set the supply voltage to 2.7 V or above for rewriting the flash memory.

Connecting and using the on-chip debugger has some special restrictions. Refer to the on-chip debugger manual for details.

Appendix 1. Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology web site.

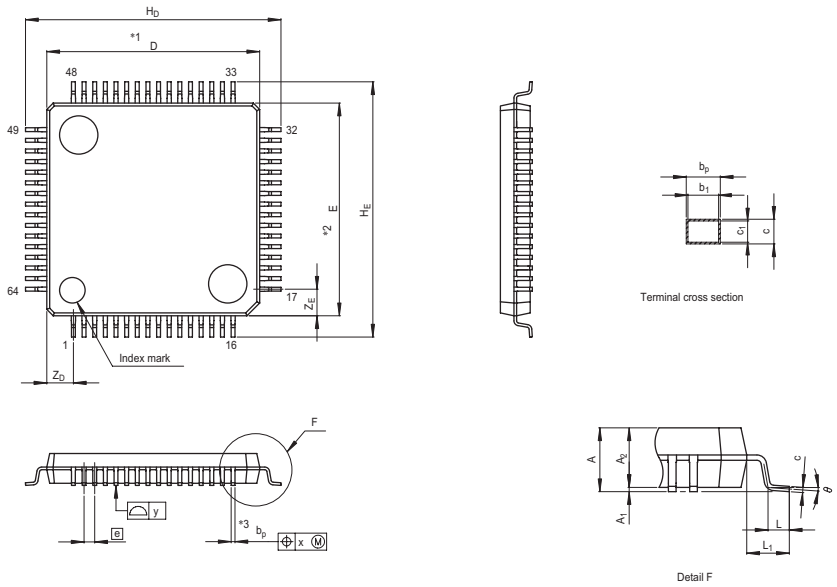
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP52-10x10-0.65	PLQP0052JA-A	52P6A-A	0.3g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.27	0.32	0.37
b_1	—	0.30	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	1.1	—
Z_E	—	1.1	—
L	0.35	0.5	0.65
L_1	—	1.0	—

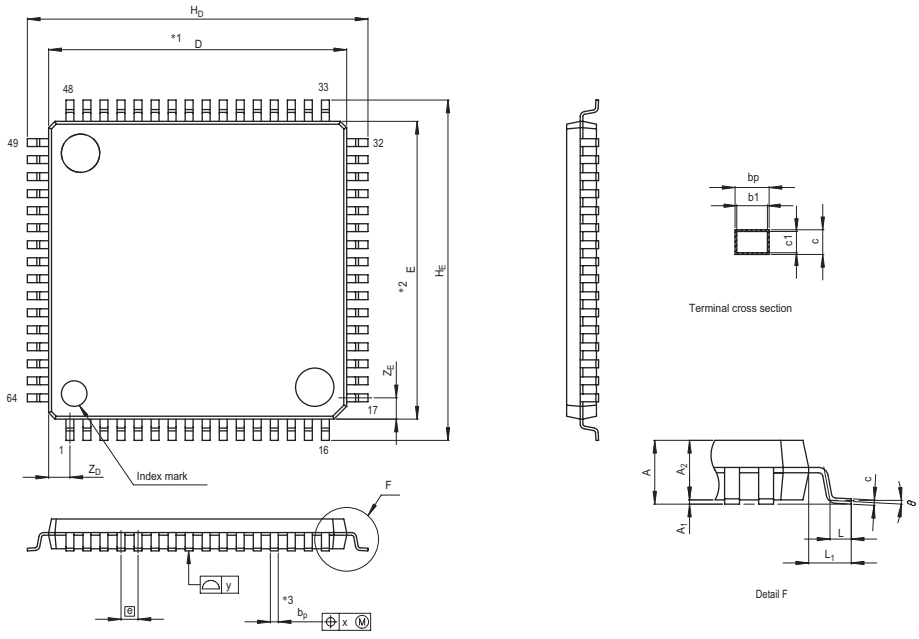
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

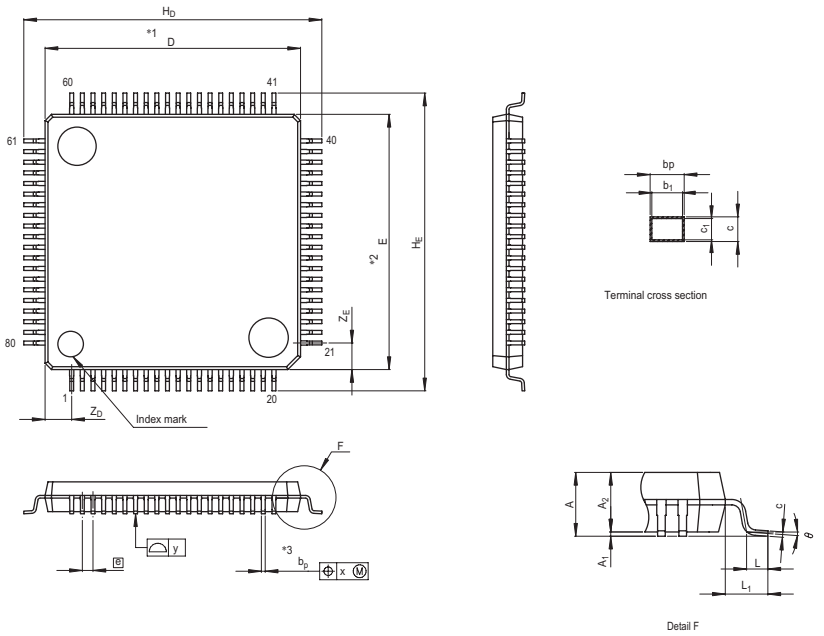
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-14x14-0.80	PLQP0064GA-A	64P6U-A	0.7g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.3	0.5	0.7
L_1	—	1.0	—

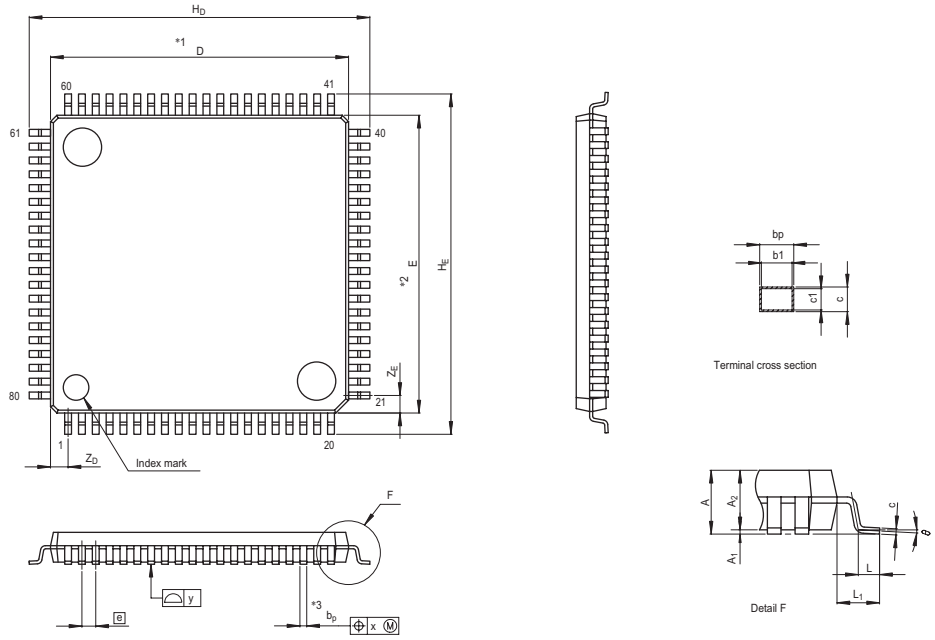
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP80-12x12-0.50	PLQP0080KB-A	80P6Q-A	0.5g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	10°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.3	0.5	0.7
L_1	—	1.0	—

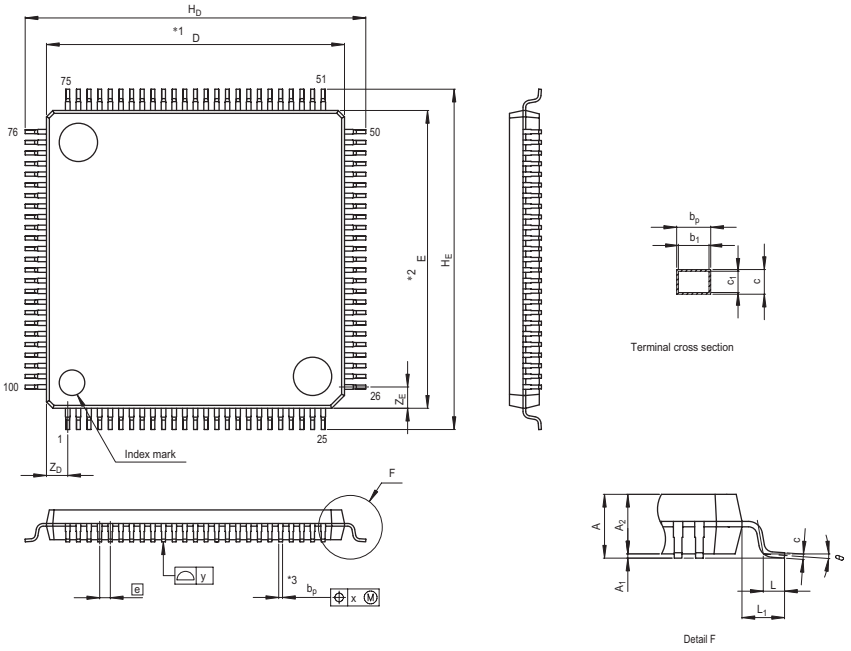
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP80-14x14-0.65	PLQP0080JA-A	FP-80W / FP-80WV	0.6g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.27	0.32	0.37
b_1	—	0.30	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	0.825	—
Z_E	—	0.825	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g

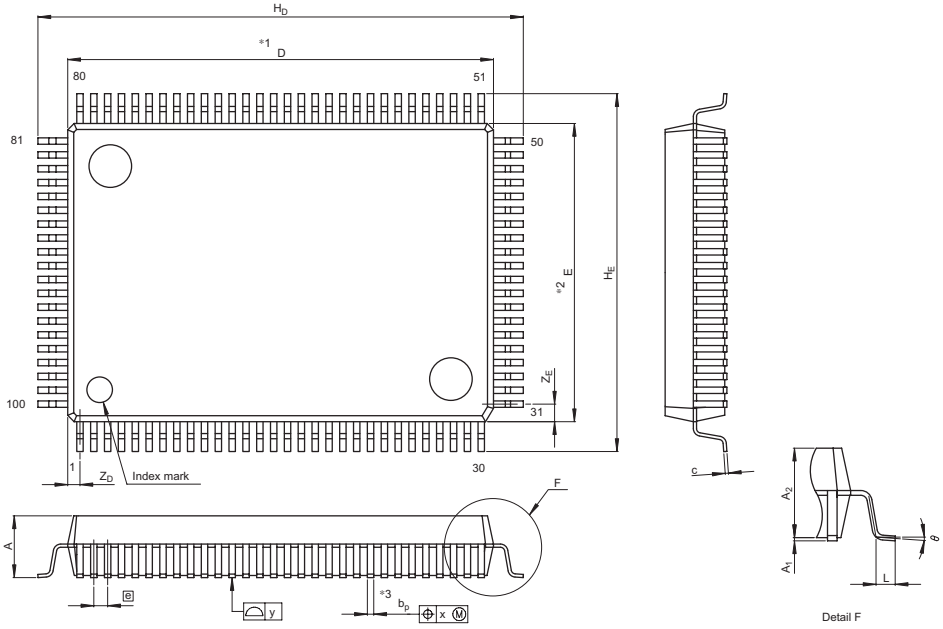


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP100-14x20-0.65	PRQP0100JD-B	100P6F-A	1.8g

Under development

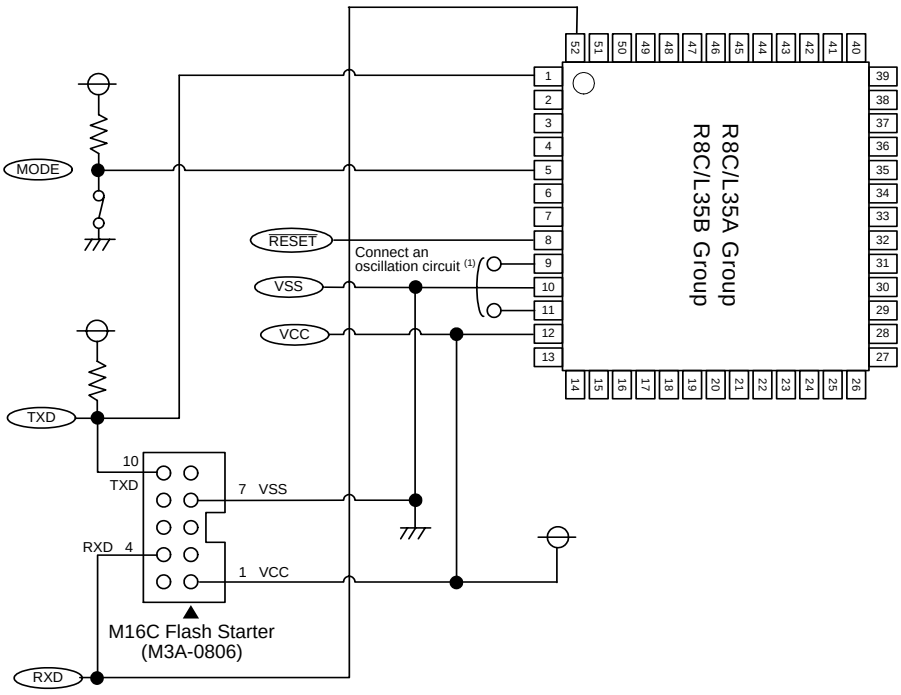


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.8	20.0	20.2
E	13.8	14.0	14.2
A_2	—	2.8	—
H_D	22.5	22.8	23.1
H_E	16.5	16.8	17.1
A	—	—	3.05
A_1	0	0.1	0.2
b_p	0.25	0.3	0.4
c	0.13	0.15	0.2
θ	0°	—	10°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	0.575	—
Z_E	—	0.825	—
L	0.4	0.6	0.8

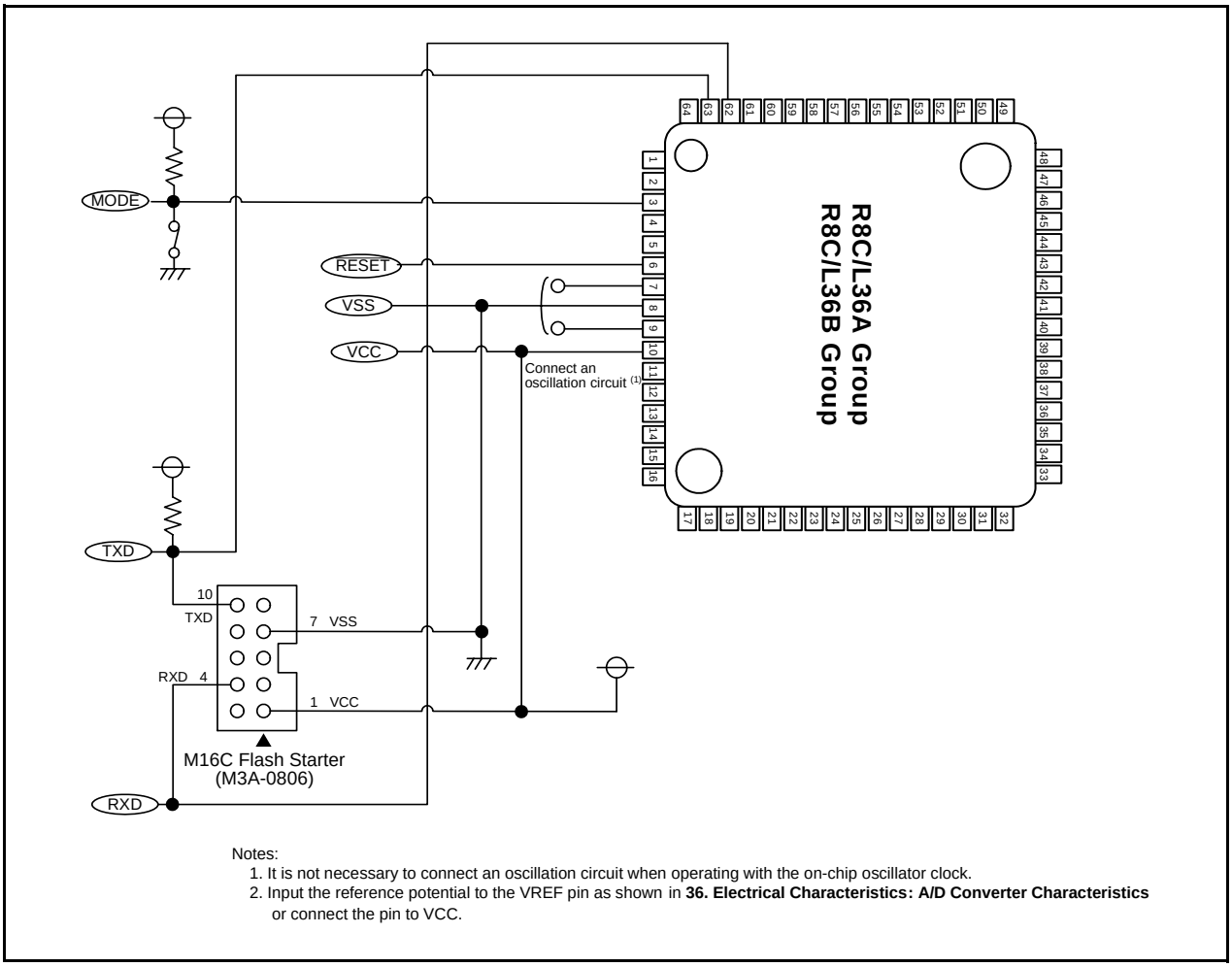
Appendix 2. Connection Examples with M16C Flash Starter

Appendix Figures 2.1 to 2.5 show connection examples with the M16C Flash Starter (M3A-0806).



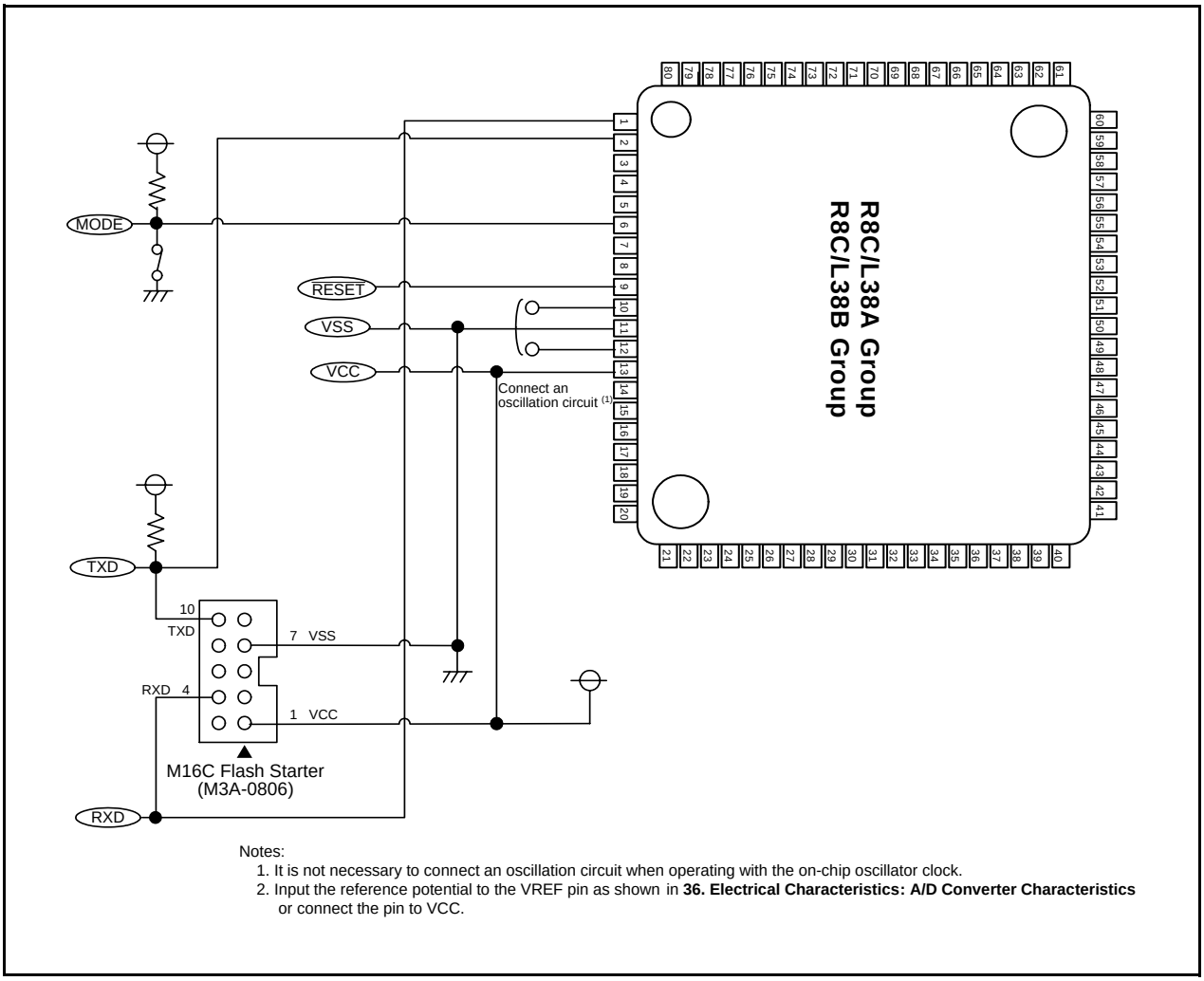
Notes:
1. It is not necessary to connect an oscillation circuit when operating with the on-chip oscillator clock.
2. Input the reference potential to the VREF pin as shown in **36. Electrical Characteristics: A/D Converter Characteristics** or connect the pin to VCC.

Appendix Figure 2.1 Connection Example with M16C Flash Starter (1)



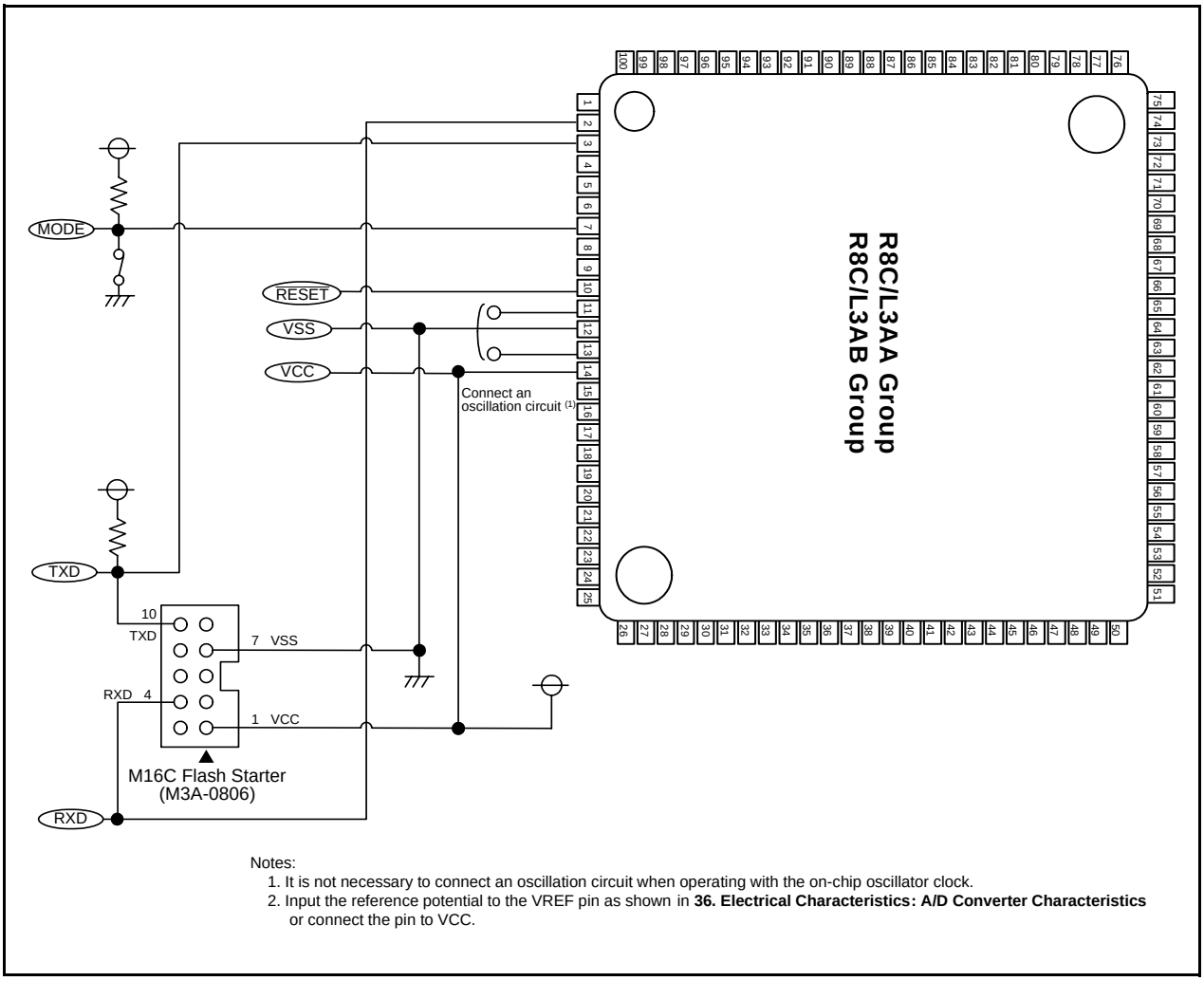
Notes:
1. It is not necessary to connect an oscillation circuit when operating with the on-chip oscillator clock.
2. Input the reference potential to the VREF pin as shown in **36. Electrical Characteristics: A/D Converter Characteristics** or connect the pin to VCC.

Appendix Figure 2.2 Connection Example with M16C Flash Starter (2)



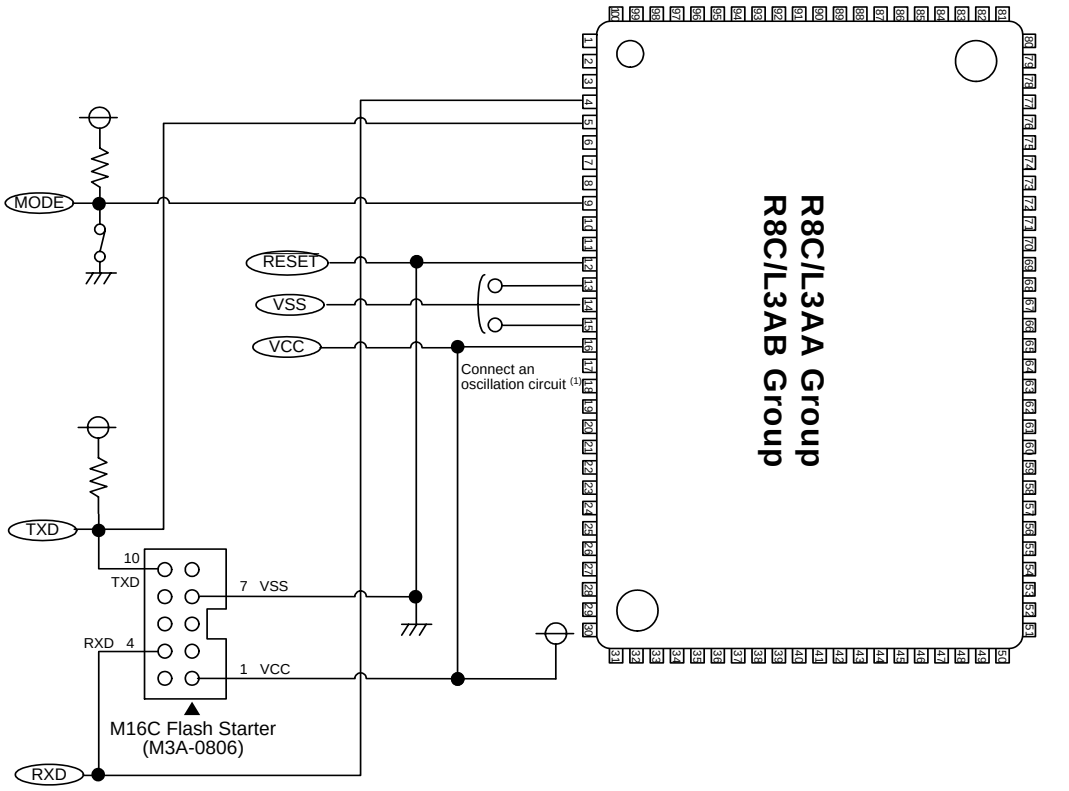
Notes:
1. It is not necessary to connect an oscillation circuit when operating with the on-chip oscillator clock.
2. Input the reference potential to the VREF pin as shown in **36. Electrical Characteristics: A/D Converter Characteristics** or connect the pin to VCC.

Appendix Figure 2.3 Connection Example with M16C Flash Starter (3)



Notes:
1. It is not necessary to connect an oscillation circuit when operating with the on-chip oscillator clock.
2. Input the reference potential to the VREF pin as shown in **36. Electrical Characteristics: A/D Converter Characteristics** or connect the pin to VCC.

Appendix Figure 2.4 Connection Example with M16C Flash Starter (4)

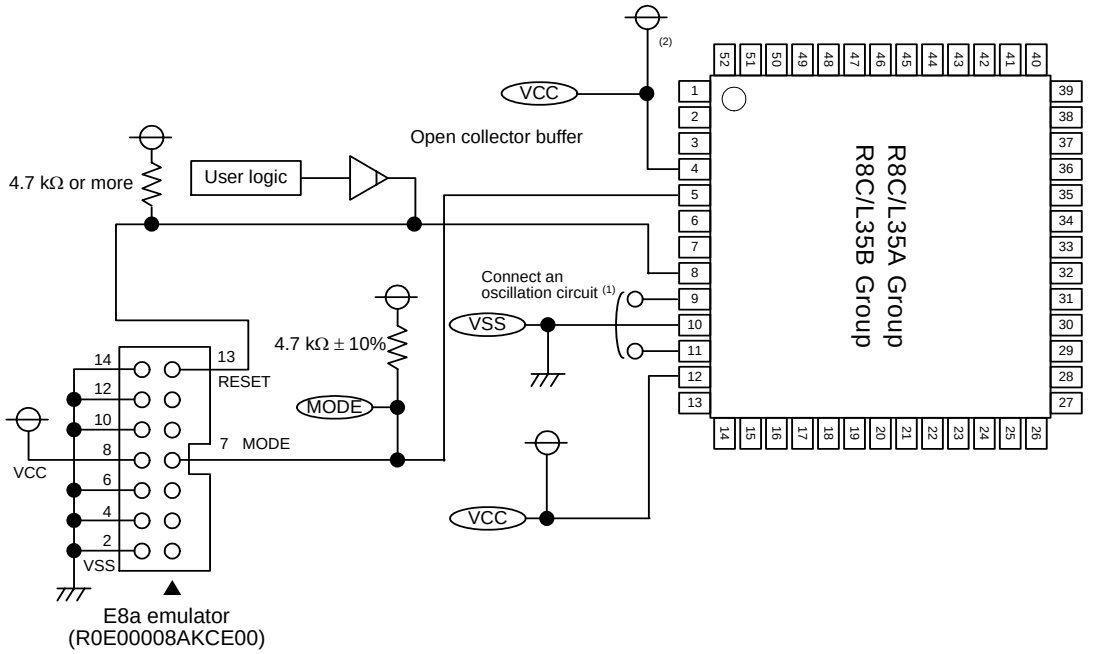


Notes:
1. It is not necessary to connect an oscillation circuit when operating with the on-chip oscillator clock.
2. Input the reference potential to the VREF pin as shown in **36. Electrical Characteristics: A/D Converter Characteristics** or connect the pin to VCC.

Appendix Figure 2.5 Connection Example with M16C Flash Starter (5)

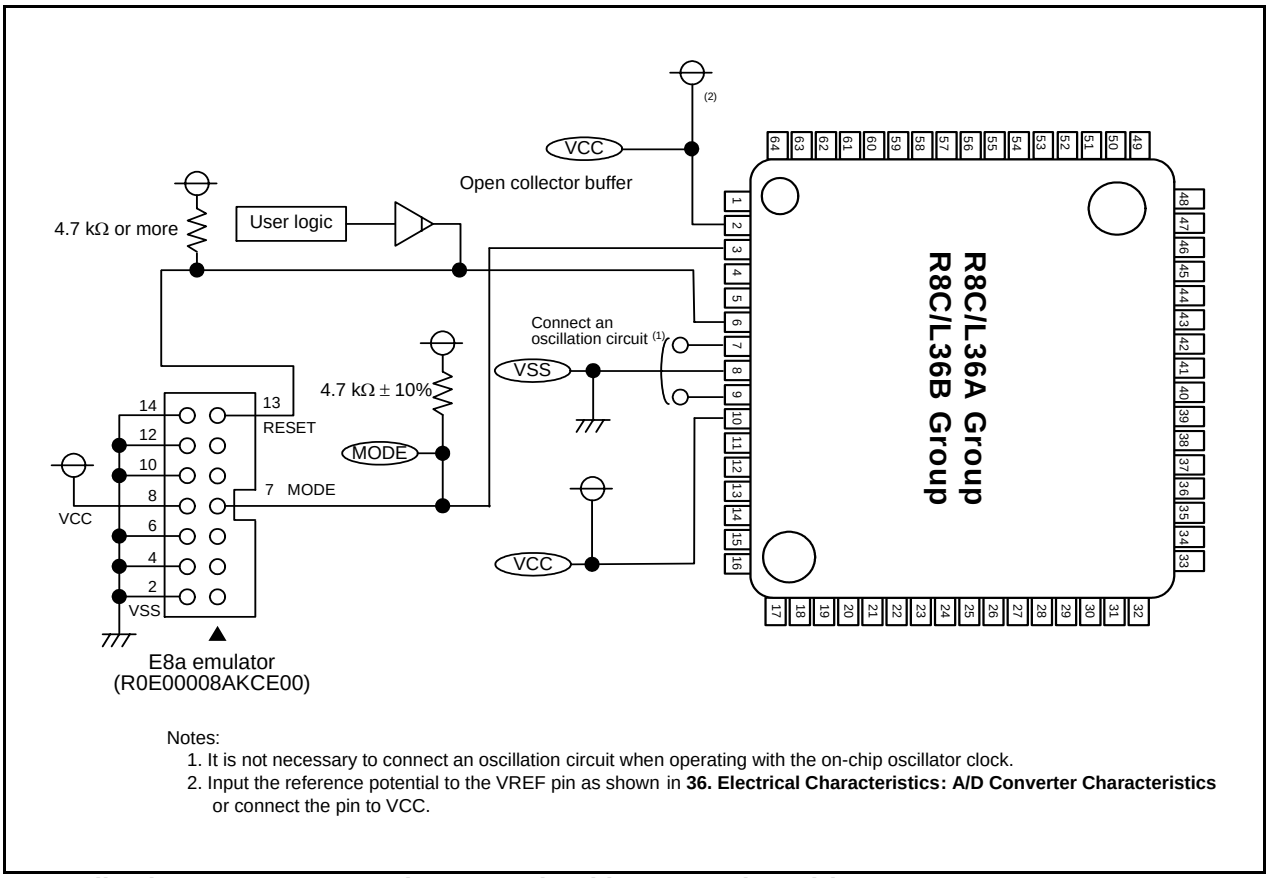
Appendix 3. Connection Examples with E8a Emulator

Appendix Figures 3.1 to 3.5 show connection examples with the E8a Emulator (R0E00008AKCE00).



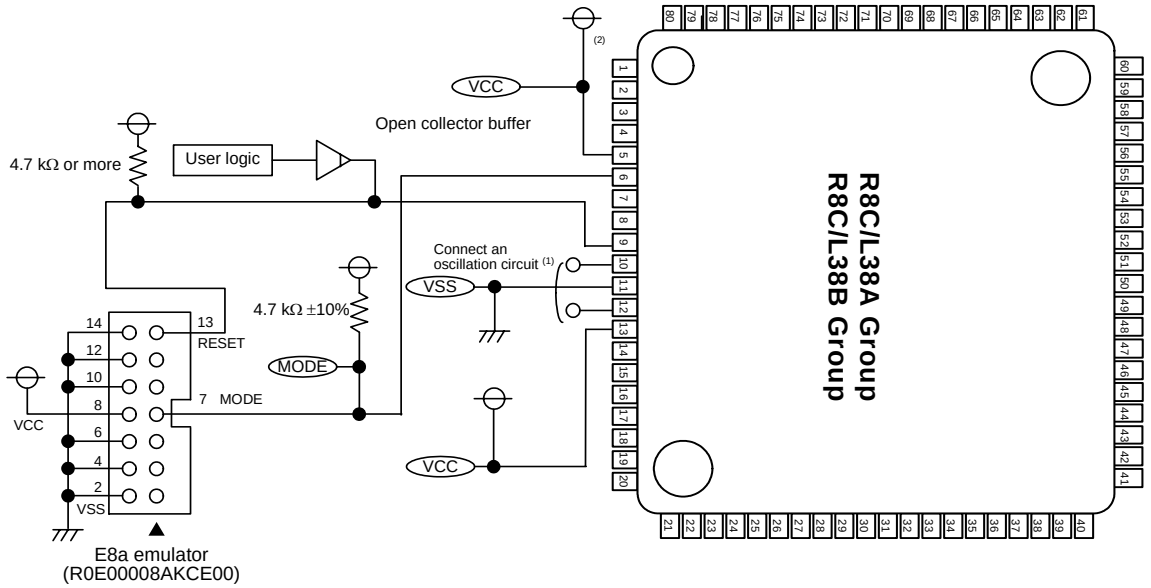
Notes:
1. It is not necessary to connect an oscillation circuit when operating with the on-chip oscillator clock.
2. Input the reference potential to the VREF pin as shown in **36. Electrical Characteristics: A/D Converter Characteristics** or connect the pin to VCC.

Appendix Figure 3.1 Connection Example with E8a Emulator (1)



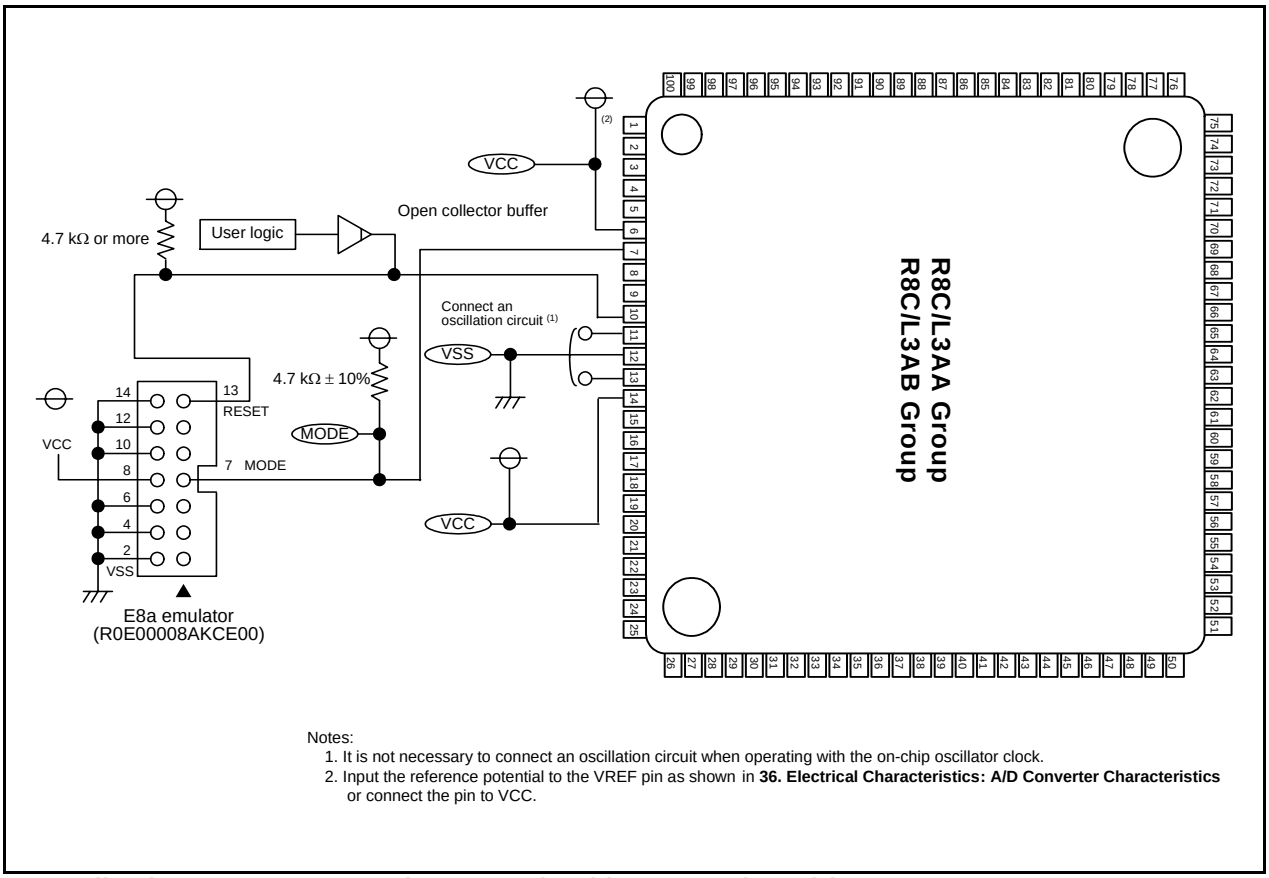
Notes:
1. It is not necessary to connect an oscillation circuit when operating with the on-chip oscillator clock.
2. Input the reference potential to the VREF pin as shown in **36. Electrical Characteristics: A/D Converter Characteristics** or connect the pin to VCC.

Appendix Figure 3.2 Connection Example with E8a Emulator (2)



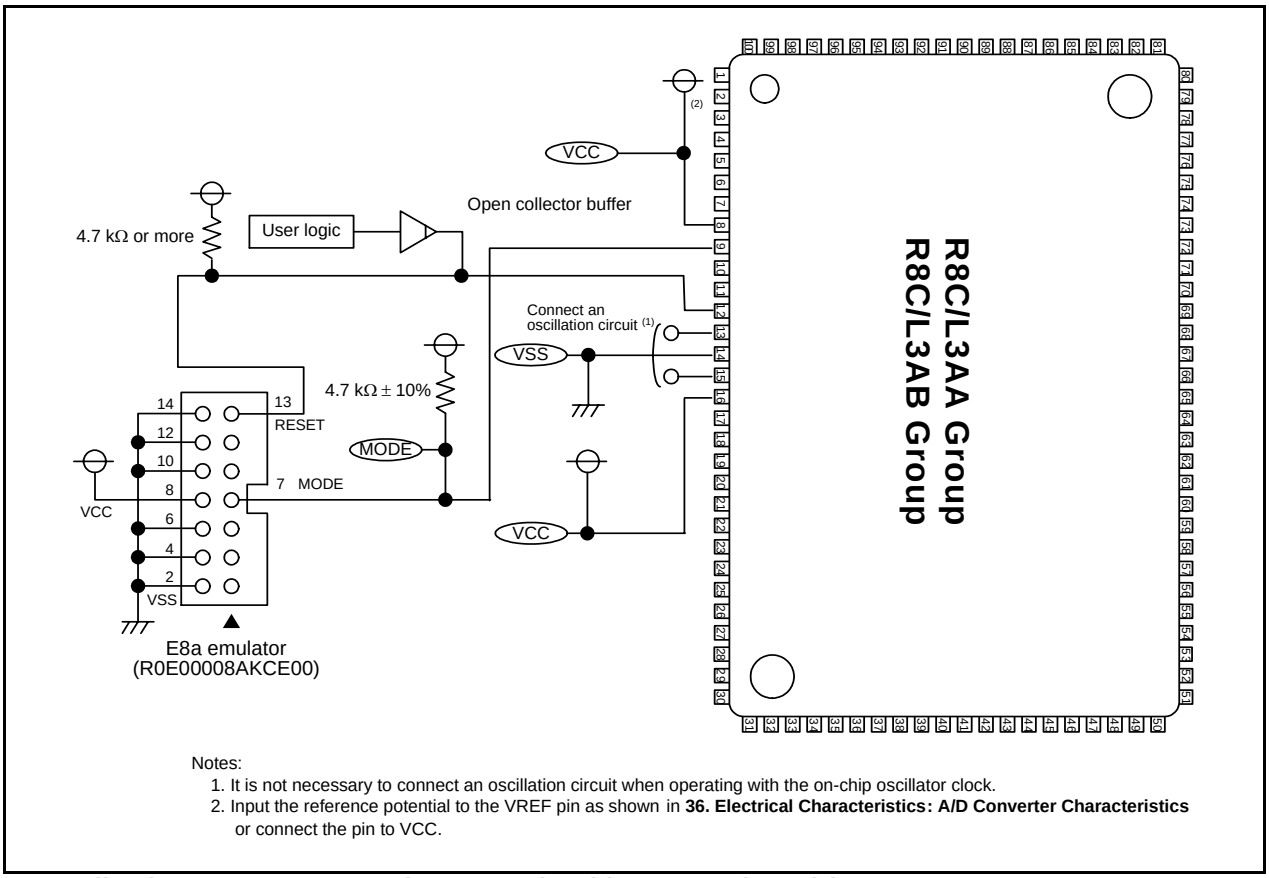
Notes:
1. It is not necessary to connect an oscillation circuit when operating with the on-chip oscillator clock.
2. Input the reference potential to the VREF pin as shown in **36. Electrical Characteristics: A/D Converter Characteristics** or connect the pin to VCC.

Appendix Figure 3.3 Connection Example with E8a Emulator (3)



Notes:
1. It is not necessary to connect an oscillation circuit when operating with the on-chip oscillator clock.
2. Input the reference potential to the VREF pin as shown in **36. Electrical Characteristics: A/D Converter Characteristics** or connect the pin to VCC.

Appendix Figure 3.4 Connection Example with E8a Emulator (4)

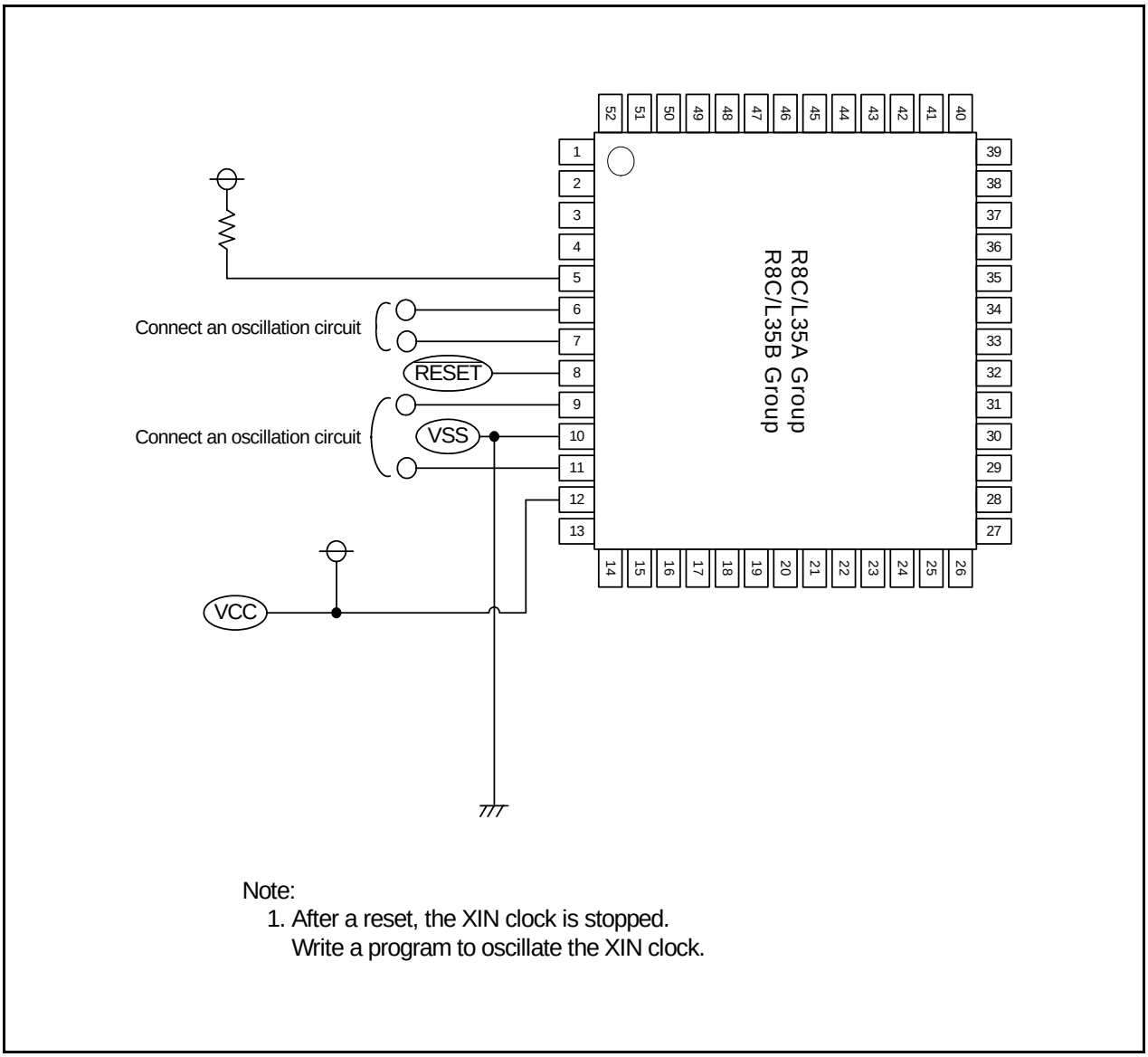


Notes:
1. It is not necessary to connect an oscillation circuit when operating with the on-chip oscillator clock.
2. Input the reference potential to the VREF pin as shown in **36. Electrical Characteristics: A/D Converter Characteristics** or connect the pin to VCC.

Appendix Figure 3.5 Connection Example with E8a Emulator (5)

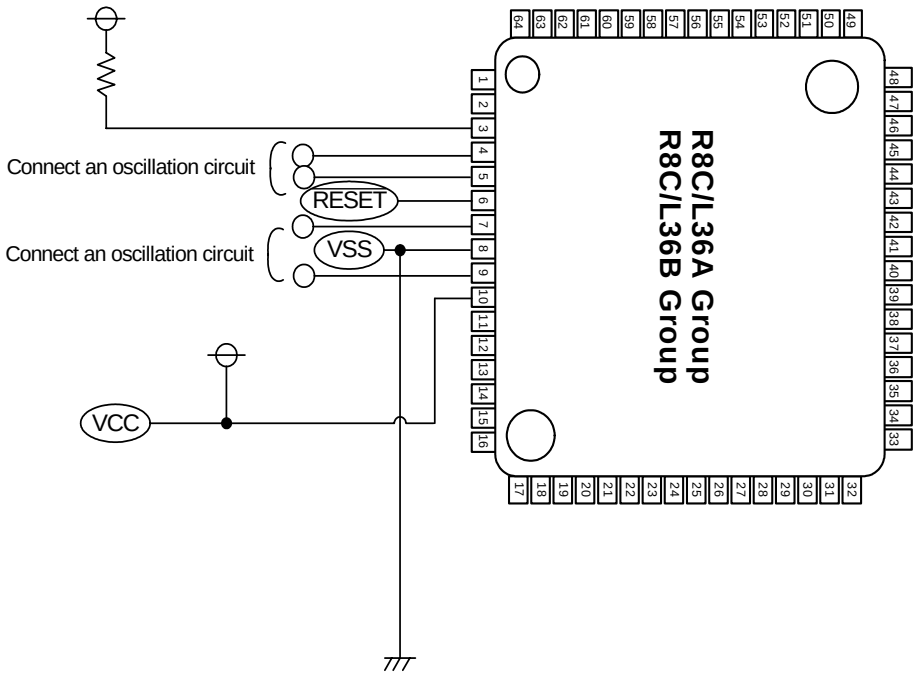
Appendix 4. Examples of Oscillation Evaluation Circuit

Appendix Figures 4.1 to 4.5 show examples of the oscillation evaluation circuit.



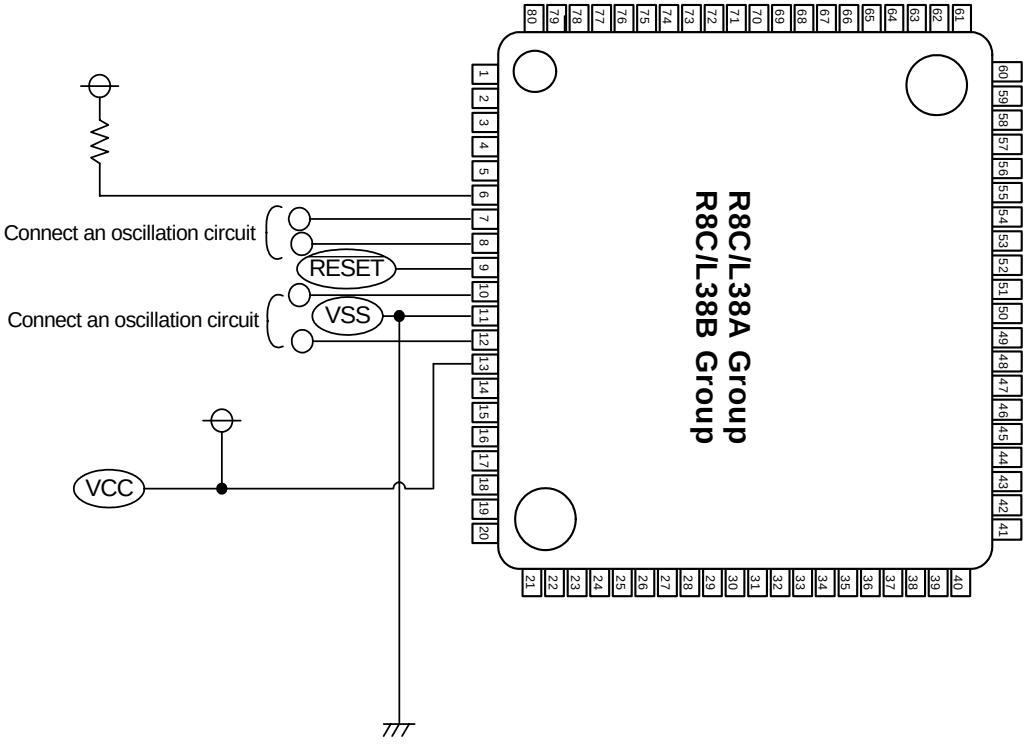
Note:
1. After a reset, the XIN clock is stopped.
Write a program to oscillate the XIN clock.

Appendix Figure 4.1 Example of Oscillation Evaluation Circuit (1)



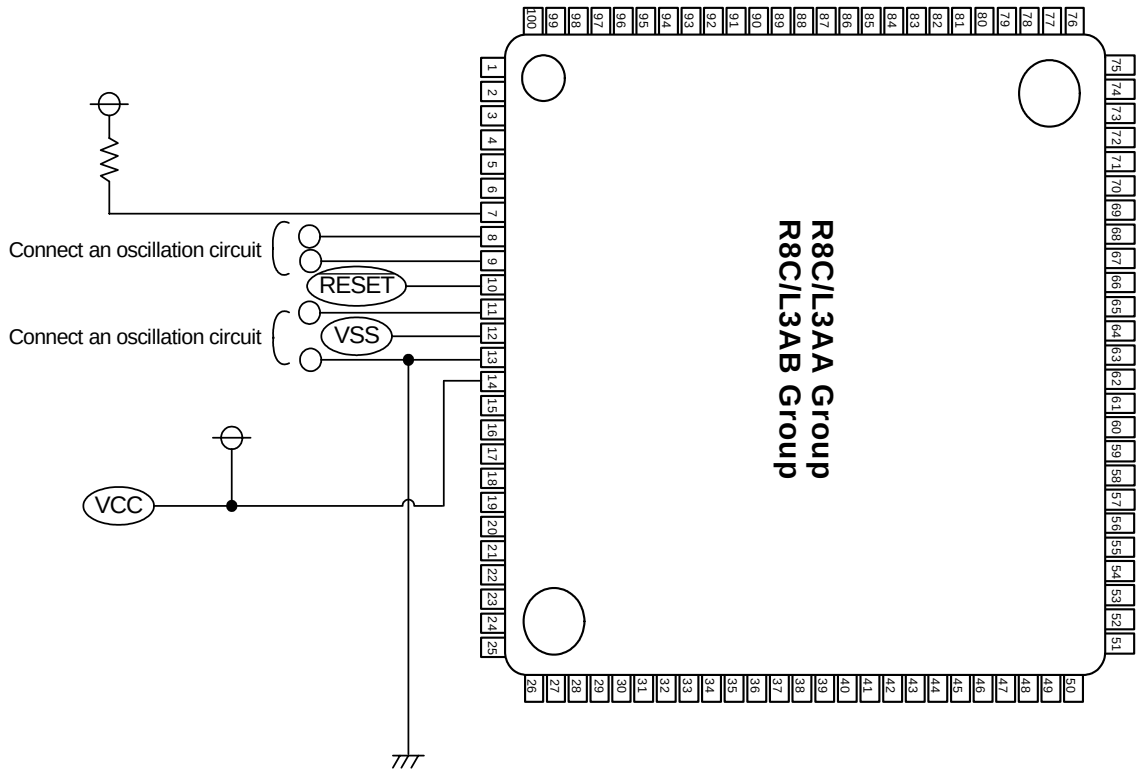
Note:
1. After a reset, the XIN clock is stopped.
   Write a program to oscillate the XIN clock.

Appendix Figure 4.2 Example of Oscillation Evaluation Circuit (2)



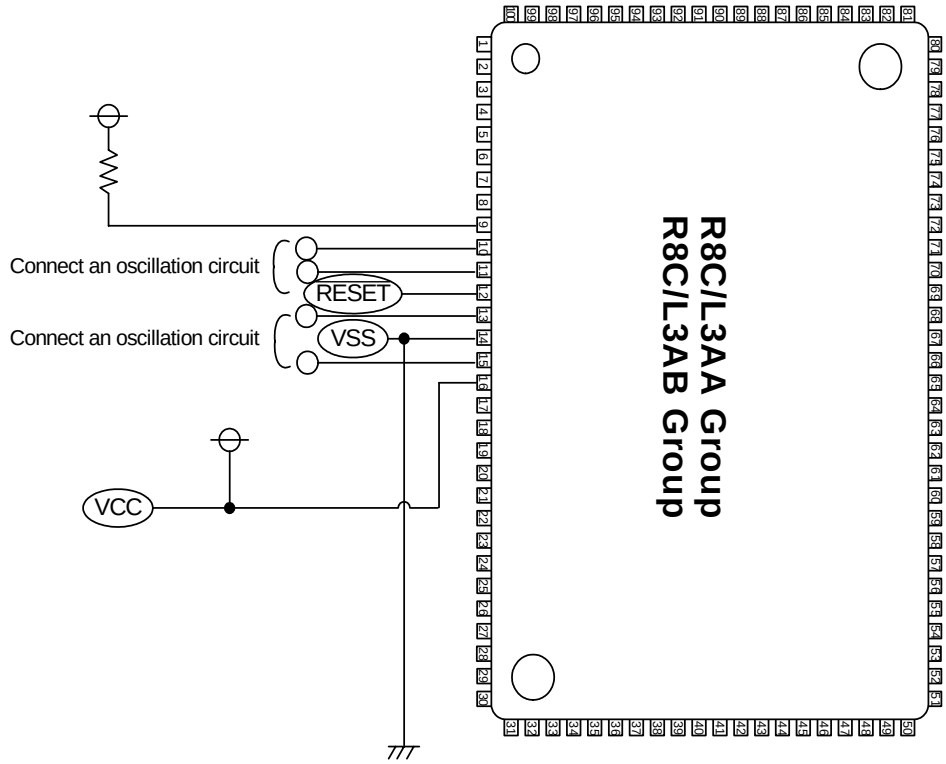
Note:
1. After a reset, the XIN clock is stopped.
   Write a program to oscillate the XIN clock.

Appendix Figure 4.3 Example of Oscillation Evaluation Circuit (3)



Note:
1. After a reset, the XIN clock is stopped.
Write a program to oscillate the XIN clock.

Appendix Figure 4.4 Example of Oscillation Evaluation Circuit (4)



Note:
1. After a reset, the XIN clock is stopped.
Write a program to oscillate the XIN clock.

Appendix Figure 4.5 Example of Oscillation Evaluation Circuit (5)

Index

REVISION HISTORY	R8C/L35A Group, R8C/L36A Group, R8C/L38A Group, R8C/L3AA Group R8C/L35B Group, R8C/L36B Group, R8C/L38B Group, R8C/L3AB Group Hardware Manual

Rev.	Date	Description	
		Page	Summary
0.02	Jun 24, 2008	-	First Edition issued
0.10	Jul 30, 2008	-	Revised Edition issued

R8C/L35A Group, R8C/L36A Group, R8C/L38A Group, R8C/L3AA Group,
R8C/L35B Group, R8C/L36B Group, R8C/L38B Group, R8C/L3AB Group
Hardware Manual

Publication Date: Rev.0.02 Jun 24, 2008
Rev.0.10 Jul 30, 2008

Published by: Sales Strategic Planning Div.
Renesas Technology Corp.

R8C/L35A Group, R8C/L36A Group, R8C/L38A Group, R8C/L3AA Group, R8C/L35B Group, R8C/L36B Group, R8C/L38B Group, R8C/L3AB Group

Hardware Manual

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