DESCRIPTION

R8A66150 is a semiconductor integrated circuit which has 12-bit shift register function to execute serial in - parallel out conversion and parallel in - serial out conversion.
Built in two shift registers for serial in - parallel out and parallel in - serial out are constructed independently, This IC is able to read serial input data into a shift register while output the serial data converting from the parallel data input.
Also, parallel data I/O pins can be set to input mode or output mode by a bit.
R8A66150 is useful in a wide range of applications, such as MCU (micro controller unit) I/O port extension and serial bus system data communication. R8A66150 is the succession product of M66006.

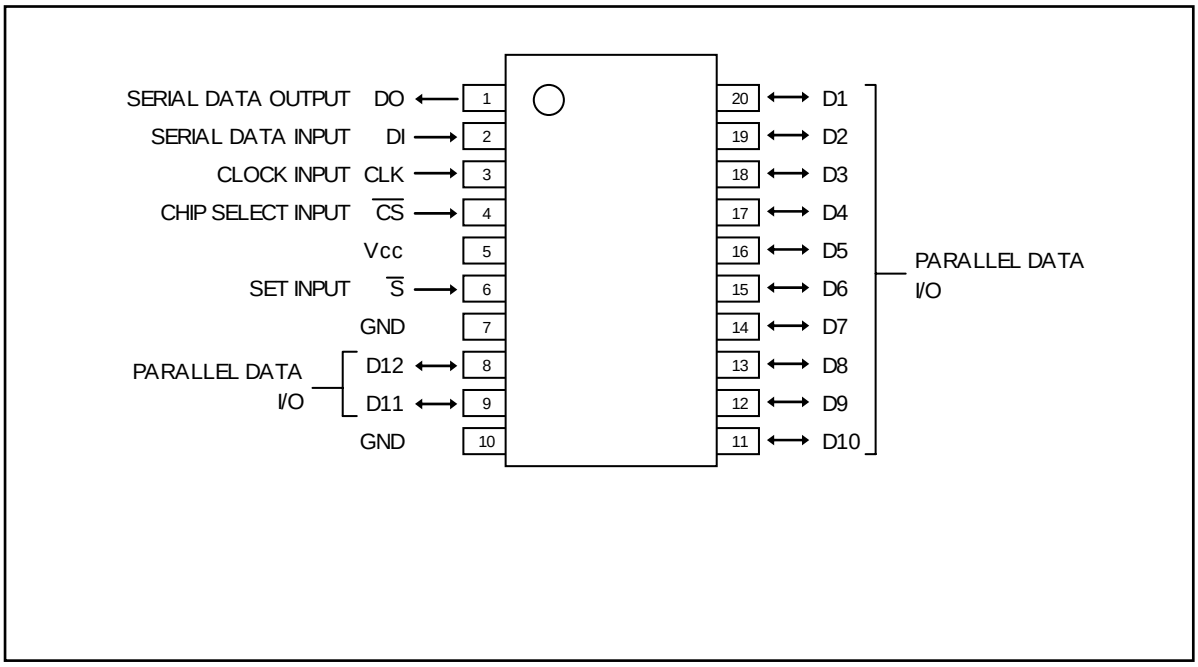
FEATURES

- Bi-directional serial communication with MCU
- Serial data can be input during parallel to serial data conversion
- Parallel data I/O pins can be set input mode or output mode by a bit
- Schmitt input (DI, CLK, /S, /CS)
- N-ch open drain output (DO, D1~D12)
- Parallel data I/O pins (D1~D12)
- Wide supply voltage range (Vcc=2.0 to 6.0V)
- Wide operating temperature range (Ta=-40 to 85°C)

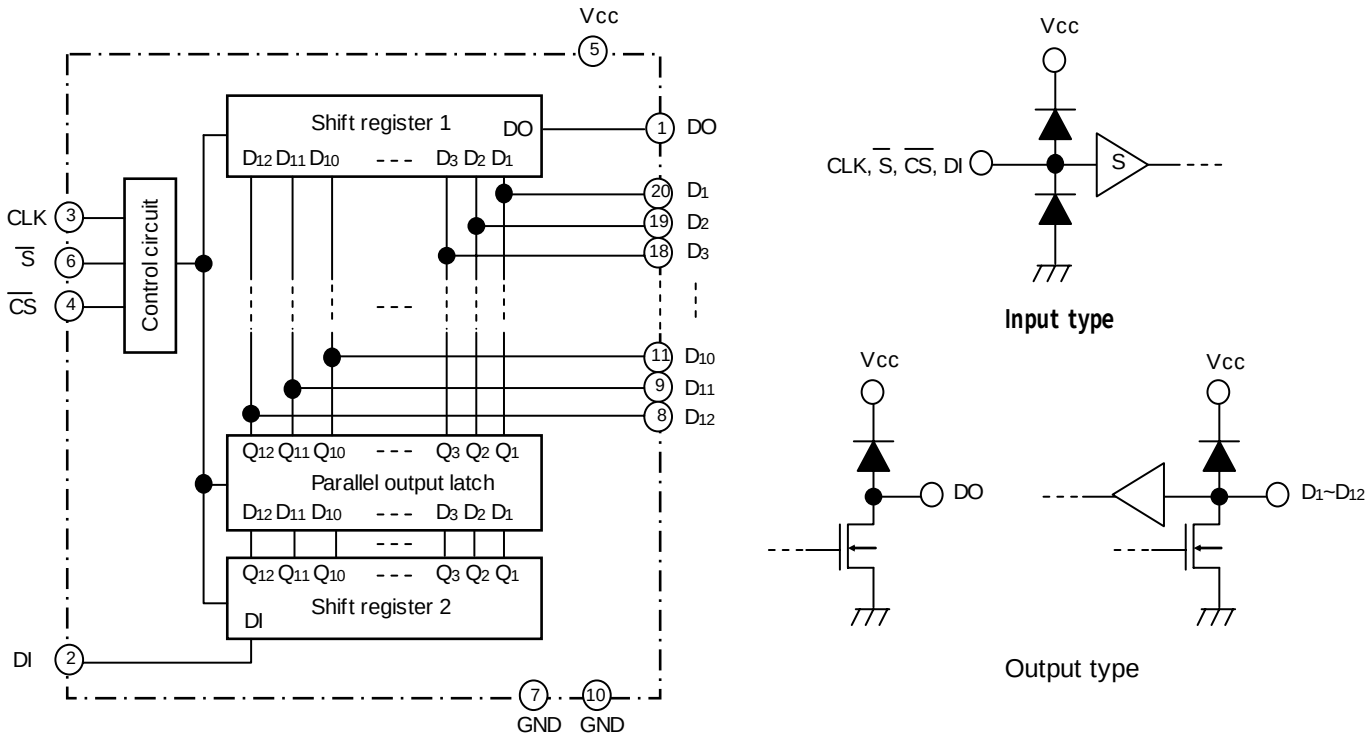
APPLICATION

- Serial - parallel or parallel - serial data conversion for MCU peripheral.
- Serial bus control by MCU.

PIN CONFIGURATION (TOP VIEW)



BLOCK DIAGRAM



FUNCTION

The R8A66150 is produced by using the silicon gate CMOS technology and has low power dissipation and high noise margin.

Built in two shift registers for serial in-parallel out (Shift register 2) and parallel in-serial out (Shift register 1) are constructed independently, R8A66150 is able to read serial input data into a shift register while output the serial data converting from the parallel data input.

Serial output operation of 12-bit parallel latched data and serial input operation from MCU are started when /CS is changed from "H" to "L".

12-bits parallel data are latched by the negative edge of /CS and are output from the DO terminal synchronously to the negative edge of CLK, and also the DI terminal read serial input data from MCU and are written into the internal shift register 2.

The 13th and following shift clock pulse are ignored and serial input data is masked, and DO terminal becomes high-impedance ("High-Z").

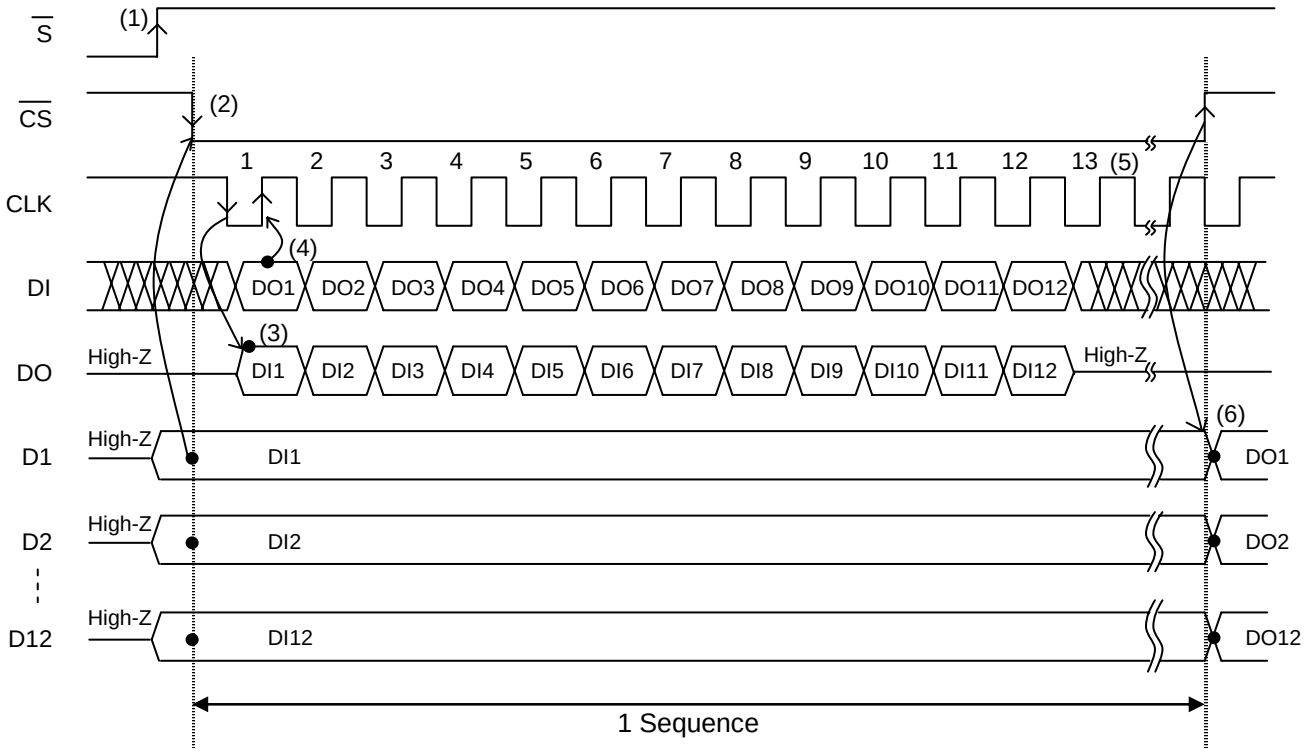
When /CS is changed from "L" to "H", 12-bits serial data which is read from the DI terminal are output to the D1~D12 terminals as parallel data.

As the output circuit type of D1~D12 terminals is N-ch open drain output, write data "H" for pins which should be set to input mode.

DESCRIPTION OF OPERATION

(1) When power ON, the status of DO and D1~D12 terminals are not determined. These terminals are turn to high-impedance when "L" is input to the /S terminal.
(2) By the negative edge of /CS, the status of D1~D12 terminals is loaded on shift register 1.
(3) Synchronous to the negative edge of CLK, 12-bit loaded data is serial output from the DO terminal.
(4) Synchronous to the positive edge of CLK, 12-bit serial input data from DI is write into the shift register 2.
(5) The 13th and following shift clock pulse are ignored and the serial data input operation is stopped. And the DO terminal becomes high-impedance ("High-Z").
(6) By the positive edge of /CS, input data described in (4) is output to D1~D12 terminals.
(7) Shift register 1 loads the AND tie data of external parallel input data and latched data on parallel output latch.
(8) If the /CS is changed from "L" to "H" before reaches the 12th bit of CLK, parallel output latch latches data which has been written on shift register 2 and output it to D1~D12 terminals. Serial data after this since is ignored and the DO terminal becomes high-impedance.
(9) Input/output mode set to D1~D12 terminals is done by the serial input data to the DI terminal. Terminals which "H" is written are set to input, and "L" is written are set to output.

OPERATION TIMING CHART



ABSOLUTE MAXIMUM RATINGS (Ta=-40~85 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5 ~ +7.0	V
VI	Input voltage		-0.5 ~ Vcc+0.5	V
Vo	Output voltage		-0.5 ~ Vcc+0.5	V
Tstg	Storage temperature range		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
Vcc	Supply voltage	2.0		6.0	V
VI	Input voltage	0		Vcc	V
Vo	Output voltage	0		Vcc	V
Topr	Operating temperature range	-40		85	°C

ELECTRICAL CHARACTERISTICS (Vcc=2.0~6.0V, Ta=-40~85°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
VT+	Positive going threshold voltage (*1)	Vo=0.1V, Vcc-0.1V I Io I=20uA		0.35 x Vcc		0.80 x Vcc	V
VT-	Negative going threshold voltage (*1)			0.20 x Vcc		0.65 x Vcc	V
VIH	"H" input voltage (*2)			0.75 x Vcc			V
VIL	"L" input voltage (*2)					0.25 x Vcc	V
VOL	"L" output voltage	Vcc=4.5V, IOL=3mA				0.5	V
IO	Output leakage current	Vcc=6V	Vo=Vcc			10	uA
			Vo=GND			-10	
IIH	"H" input current	VI=Vcc,	Vcc=6V			1	uA
IIL	"L" input current	VI=GND,	Vcc=6V			-1	
Icc	Quiescent supply current	VI=Vcc, GND Vcc=6V				100	uA

*1 : DI, CLK, /CS, /S
*2 : D1~D12

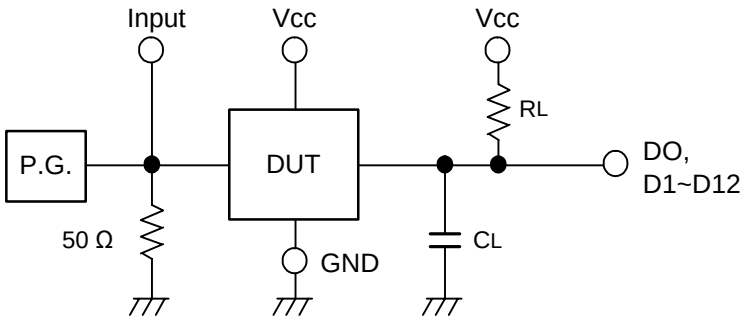
SWITCHING CHARACTERISTICS (Vcc=2.0~6.0V, Ta=-40~85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
fmax	Maximum repeat frequency	CL=50pF RL=1kΩ (note1)			1.9	MHz
tPLZ	Output "L-Z" and "Z-L" propagation time CLK - DO				400	ns
tPZL					400	ns
tPLZ	Output "L-Z" and "Z-L" propagation time /CS - D1~D12				400	ns
tPZL					400	ns
tPLZ	Output "L-Z" propagation time /S - DO, /S - D1~D12				400	ns

TIMING REQUIREMENTS (Vcc=2.0~6.0V, Ta=-40~85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
tw	CLK, /CS, /S pulse width		260			ns
tsu	Setup time of DI to CLK		130			ns
	Setup time of /CS to CLK		130			ns
	Setup time of D1~D12 to /CS		130			ns
th	Hold time of DI to CLK		130			ns
	Hold time of /CS to CLK		130			ns
	Hold time of D1~D12 to /CS		130			ns
trec	Recovery time of /CS to /S		130			ns

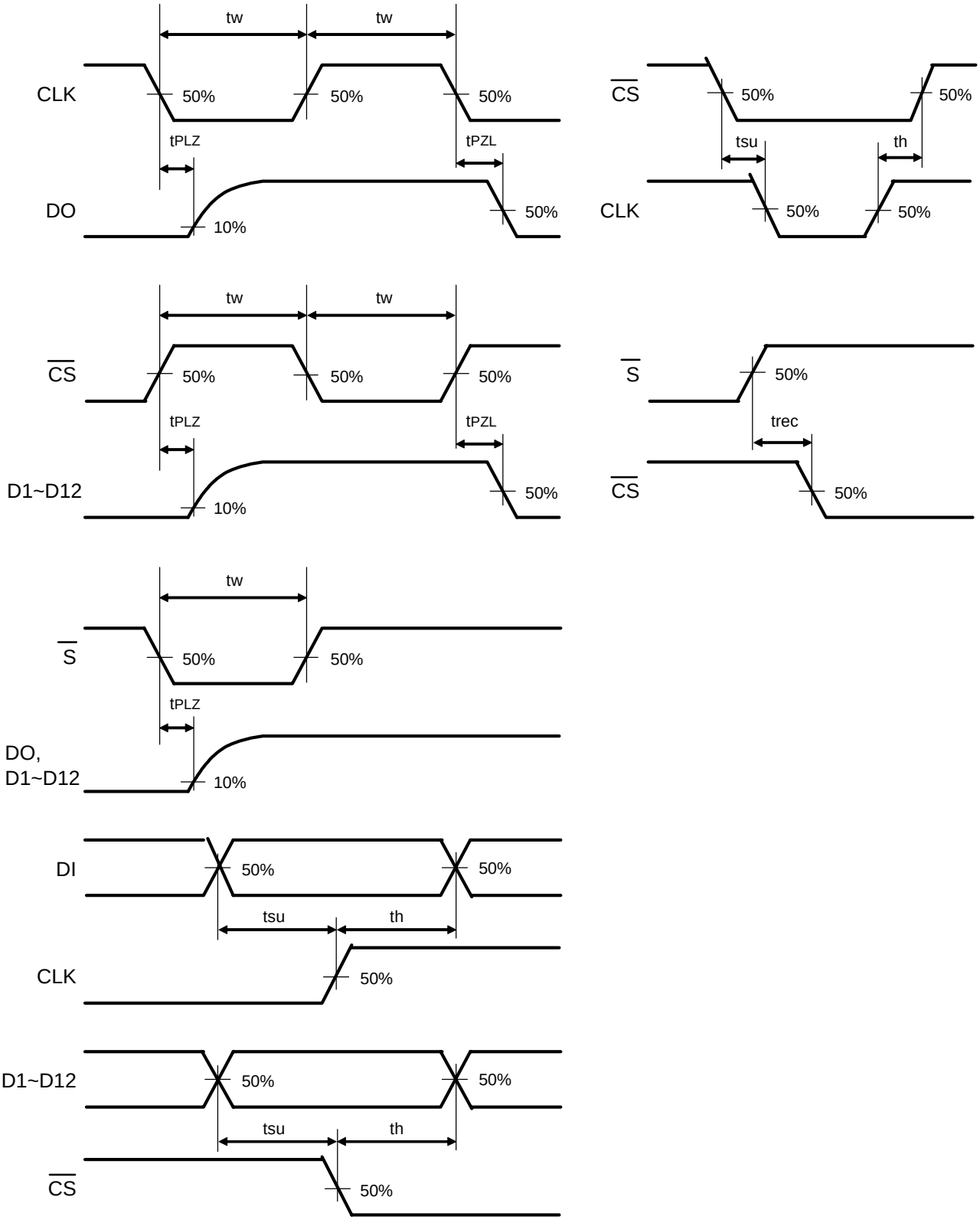
NOTE1: TEST CIRCUIT



(1) The pulse generator (P.G.) has the following characteristics (10%~90%) tr=6ns, tf=6ns, Zo=50 Ω

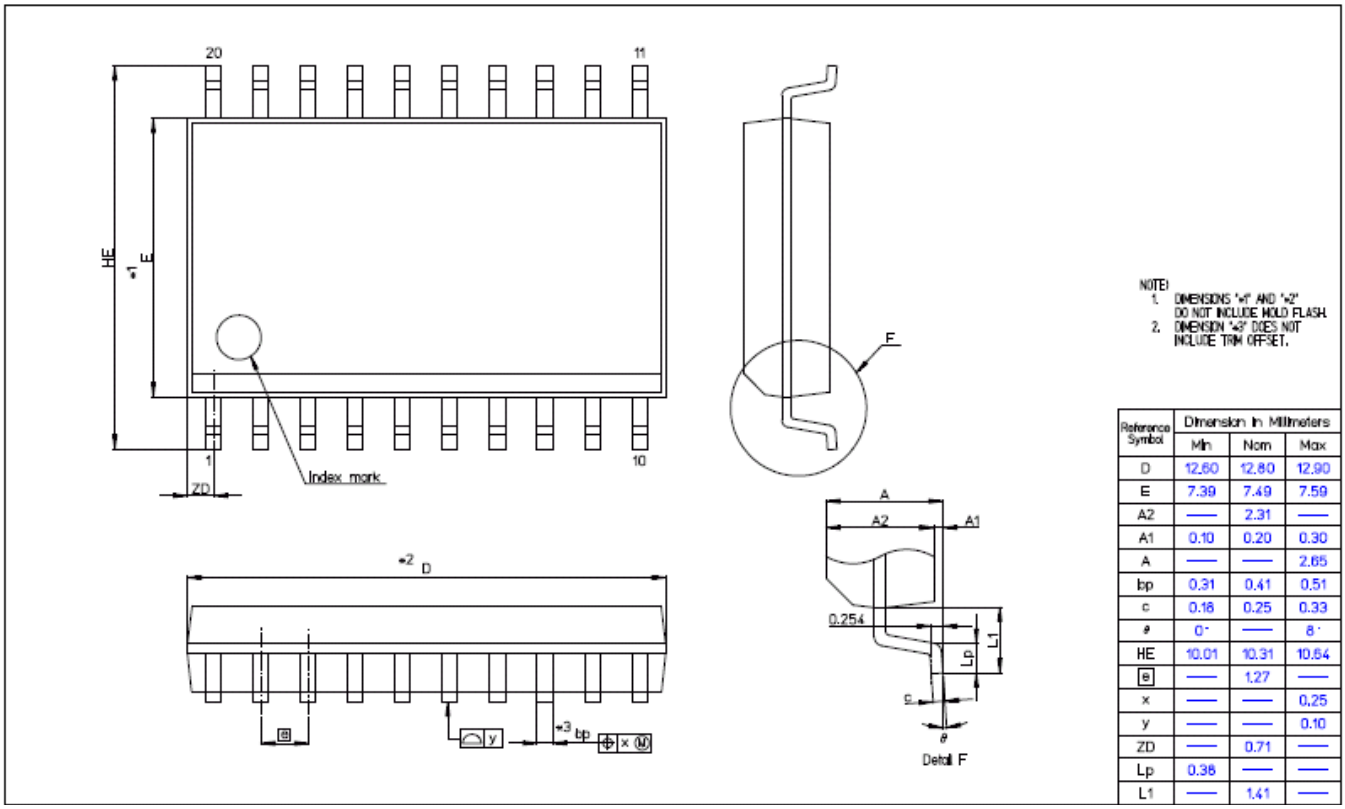
(2) The capacitance CL includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



PACKAGE OUTLINE

Package	RENESAS Code	Previous Code
20pin SOP	PRSP0020DG-A	20P2X-C



NOTE:
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	12.60	12.80	12.90
E	7.39	7.49	7.59
A2	—	2.31	—
A1	0.10	0.20	0.30
A	—	—	2.65
bp	0.31	0.41	0.51
c	0.16	0.25	0.33
θ	0°	—	8°
HE	10.01	10.31	10.64
e	—	1.27	—
x	—	—	0.25
y	—	—	0.10
ZD	—	0.71	—
Lp	0.38	—	—
L1	—	1.41	—

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