



Product List

SM89516L25, 25MHz 64KB internal flash MCU
SM89516C25, 25MHz 64KB internal flash MCU

Description

The SM89516 series product is an 8-bit single chip micro controller with 64KB flash & 1KB RAM embedded. It is a derivative of the 8052 micro controller family. With its hardware features and powerful instruction set, it's straight forward to make it a versatile and cost effective controller for those applications which demand up to 32 I/O pins for PDIP package or up to 36 I/O pins for PLCC/QFP package, or applications which need up to 64KB memory either for program or for data or mixed. To program the on-chip flash memory, a commercial writer is available to do it in parallel programming method.

Ordering Information

yymm
SM89516ihhkL

yy: year, ww: month
v: version identifier { , A, B,... }
i: process identifier {L=3.0V~3.6V,C=4.5V~ 5.5V}
hh: working clock in MHz {25}
k: package type postfix {as below table}
L:PB Free identifier
{No text is Non-PB Free , " P" is PB Free}

Features

- Working Voltage: 3.0V ~ 3.6V For L Version.
4.5V ~ 5.5V For C Version.
- General 8052 family compatible
- 12 clocks per machine cycle
- 64K byte on chip program flash
- 1024 bytes data RAM
- Three 16 bit Timers/Counters
- Four 8-bit I/O ports for PDIP package
- Four 8-bit I/O ports + one 4-bit I/O ports for PLCC or QFP package
- Full duplex serial channel
- Bit operation instruction
- Page free jumps
- 8-bit Unsigned Division
- 8-bit Unsigned Multiply
- BCD arithmetic operation
- Direct Addressing
- Indirect Addressing
- Nested Interrupt
- Two priority level interrupts
- A serial I/O port
- Power save modes: Idle mode and Power down mode
- Code protection function
- One watch dog timer (WDT)
- Low EMI (inhibit ALE)

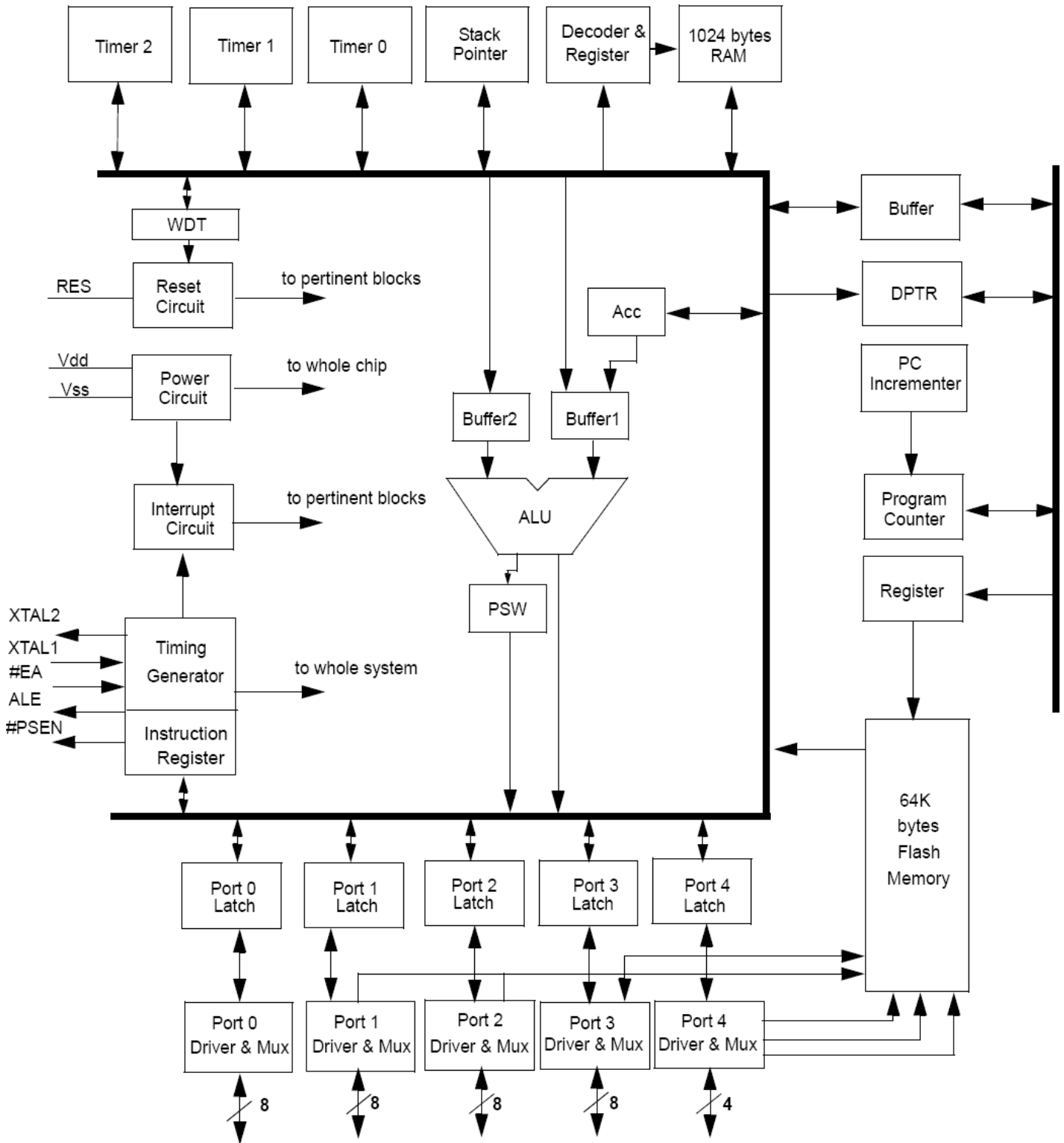
| Postfix | Package | Pin / Pad Configuration | Dimension |
|---------|----------|-------------------------|-----------|
| P | 40L PDIP | Page 2 | Page 16 |
| J | 44L PLCC | Page 2 | Page 17 |
| Q | 44L QFP | Page 2 | Page 18 |

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Block Diagram





Pin Description

| 40L PDIP Pin# | 44L QFP Pin# | 44L PLCC Pin# | Symbol | Active | I/O | Names |
|---------------|--------------|---------------|------------|--------|-----|---|
| 1 | 40 | 2 | P1.0 | | i/o | bit 0 of port 1 |
| 2 | 41 | 3 | P1.1 | | i/o | bit 1 of port 1 |
| 3 | 42 | 4 | P1.2 | | i/o | bit 2 of port 1 |
| 4 | 43 | 5 | P1.3 | | i/o | bit 3 of port 1 |
| 5 | 44 | 6 | P1.4 | | i/o | bit 4 of port 1 |
| 6 | 1 | 7 | P1.5 | | i/o | bit 5 of port 1 |
| 7 | 2 | 8 | P1.6 | | i/o | bit 6 of port 1 |
| 8 | 3 | 9 | P1.7 | | i/o | bit 7 of port 1 |
| 9 | 4 | 10 | RES | H | i | Reset |
| 10 | 5 | 11 | P3.0/RXD | | i/o | bit 0 of port 3 & Receiver data |
| 11 | 7 | 13 | P3.1/TXD | | i/o | bit 1 of port 3 & Transmit data |
| 12 | 8 | 14 | P3.2/#INT0 | L/- | i/o | bit 2 of port 3 & low true interrupt 0 |
| 13 | 9 | 15 | P3.3/#INT1 | L/- | i/o | bit 3 of port 3 & low true interrupt 1 |
| 14 | 10 | 16 | P3.4/T0 | | i/o | bit 4 of port 3 & Timer 0 |
| 15 | 11 | 17 | P3.5/T1 | | i/o | bit 5 of port 3 & Timer 1 |
| 16 | 12 | 18 | P3.6/#WR | L/- | i/o | bit 6 of port 3 & external memory write |
| 17 | 13 | 19 | P3.7/#RD | L/- | i/o | bit 7 of port 3 & external memory read |
| 18 | 14 | 20 | XTAL2 | | o | Crystal out |
| 19 | 15 | 21 | XTAL1 | | i | Crystal in |
| 20 | 16 | 22 | VSS | | | Sink Voltage, Ground |
| 21 | 18 | 24 | P2.0/A8 | | i/o | bit 0 of port 2 & bit 8 of ext. memory address |
| 22 | 19 | 25 | P2.1/A9 | | i/o | bit 1 of port 2 & bit 9 of ext. memory address |
| 23 | 20 | 26 | P2.2/A10 | | i/o | bit 2 of port 2 & bit 10 of ext. memory address |
| 24 | 21 | 27 | P2.3/A11 | | i/o | bit 3 of port 2 & bit 11 of ext. memory address |
| 25 | 22 | 28 | P2.4/A12 | | i/o | bit 4 of port 2 & bit 12 of ext. memory address |
| 26 | 23 | 29 | P2.5/A13 | | i/o | bit 5 of port 2 & bit 13 of ext. memory address |
| 27 | 24 | 30 | P2.6/A14 | | i/o | bit 6 of port 2 & bit 14 of ext. memory address |
| 28 | 25 | 31 | P2.7/A15 | | i/o | bit 7 of port 2 & bit 15 of ext. memory address |
| 29 | 26 | 32 | #PSEN | L | o | program storage enable |
| 30 | 27 | 33 | ALE | - | o | address latch enable |
| 31 | 29 | 35 | #EA | L | i | External access |
| 32 | 30 | 36 | P0.7/AD7 | | i/o | bit 7 of port 0 & data/address bit 7 of ext. memory |
| 33 | 31 | 37 | P0.6/AD6 | | i/o | bit 6 of port 0 & data/address bit 6 of ext. memory |
| 34 | 32 | 38 | P0.5/AD5 | | i/o | bit 5 of port 0 & data/address bit 5 of ext. memory |
| 35 | 33 | 39 | P0.4/AD4 | | i/o | bit 4 of port 0 & data/address bit 4 of ext. memory |
| 36 | 34 | 40 | P0.3/AD3 | | i/o | bit 3 of port 0 & data/address bit 3 of ext. memory |
| 37 | 35 | 41 | P0.2/AD2 | | i/o | bit 2 of port 0 & data/address bit 2 of ext. memory |
| 38 | 36 | 42 | P0.1/AD1 | | i/o | bit 1 of port 0 & data/address bit 1 of ext. memory |
| 39 | 37 | 43 | P0.0/AD0 | | i/o | bit 0 of port 0 & data/address bit 0 of ext. memory |
| 40 | 38 | 44 | VDD | | | Drive Voltage, +5 Vcc |
| | 17 | 23 | P4.0 | | i/o | bit 0 of Port 4 |
| | 28 | 34 | P4.1 | | i/o | bit 1 of Port 4 |
| | 39 | 1 | P4.2 | | i/o | bit 2 of Port 4 |
| | 6 | 12 | P4.3 | | i/o | bit 3 of port 4 |



Special Function Register (SFR)

The address \$80 to \$FF can be accessed by direct addressing mode only.

Address \$80 to \$FF is SFR area.

The following table lists the SFRs which are identical to general 8052, as well as SM89516A Extension SFRs.

Special Function Register (SFR) Memory Map

| | | | | | | | | |
|------|-----------|------|--------|--------|-----|-------------|-------|------|
| \$F8 | | | | | | | | \$FF |
| \$F0 | B | | | | | | | \$F7 |
| \$E8 | | | | | | | | \$EF |
| \$E0 | ACC | | | | | | | \$E7 |
| \$D8 | P4 | | | | | | | \$DF |
| \$D0 | PSW | | | | | | | \$D7 |
| \$C8 | T2CON | | RCAP2L | RCAP2H | TL2 | TH2 | | \$CF |
| \$C0 | | | | | | | | \$C7 |
| \$B8 | IP | | | | | | SCONF | \$BF |
| \$B0 | P3 | | | | | | | \$B7 |
| \$A8 | IE | | | | | | | \$AF |
| \$A0 | P2 | | | | | | | \$A7 |
| \$98 | SCON | SBUF | | | | | WDTC | \$9F |
| \$90 | P1 | | | | | | | \$97 |
| \$88 | TCON | TMOD | TL0 | TL1 | TH0 | TH1 | | \$8F |
| \$80 | P0 | SP | DPL | DPH | | RCON | PCON | \$87 |

Note: The text of SFRs with bold type characters are Extension Special Function Registers for SM89516

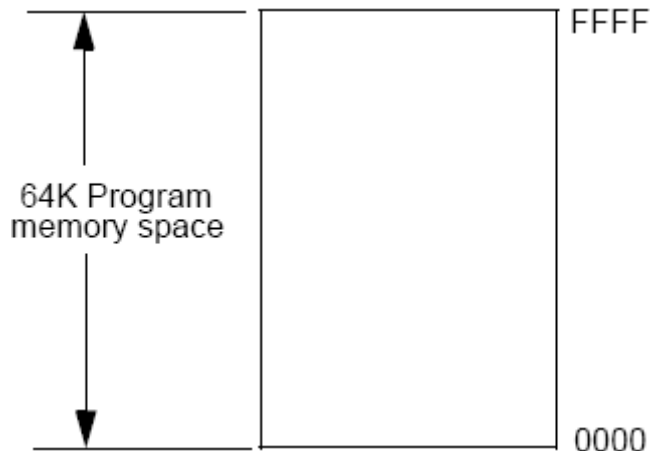
Extension Function Description

1. Memory Structure

The SM89516 is the general 8052 hardware core to integrate the expanded 768B data RAM and 64KB flash program memory as a single chip micro controller. Its memory structure follows general 8052 structure.

1.1 Program Memory

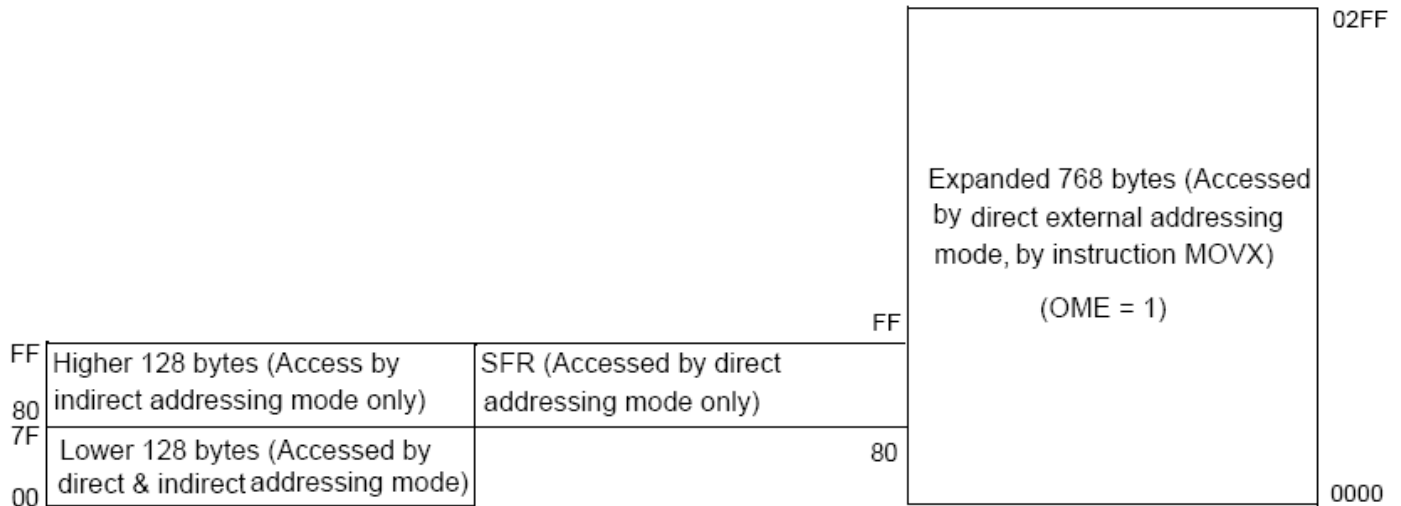
The SM89516 has 64K bytes on-chip flash memory which can be used as general program memory.





1.2 Data Memory

The SM89516 has 1K bytes on-chip RAM, 256 bytes of it are the same as general 8052 internal memory structure while the expanded 768 bytes on-chip RAM can be accessed by external memory addressing method (by instruction MOVX).



Data Memory - Lower 128 byte

Data memory \$00 to \$FF is the same as 8052
The address \$00 to \$7F can be accessed by direct and indirect addressing modes.
Address \$00 to \$1F is register area.
Address \$20 to \$2F is memory bit area.
Address \$30 to \$7F is for general memory area.

Data memory - Higher 128 byte

The address \$80 to \$FF can be accessed by indirect addressing mode only.
Addressing \$80 to \$FF is data area.

Data Memory - Expanded 768 bytes

From external address \$0000 to \$02FF is the on-chip expanded RAM area, total 768 bytes. This area can be accessed by external direct addressing mode only (by instruction MOVX).



Internal RAM Control Register (RCON, \$85)

| | | | | | | | | |
|---------------|--------|--------|--------|--------|--------|--------|-------|-------|
| | bit-7 | | | | | | bit-0 | |
| | Unused | Unused | Unused | Unused | Unused | Unused | RAMS1 | RAMS0 |
| Read / Write: | - | - | - | - | - | - | R/W | R/W |
| Reset value: | * | * | * | * | * | * | 0 | 0 |

SM89516A has 768 byte on-chip RAM which can be accessed by external memory addressing method only. (By instruction MOVX). The address space of instruction MOVX @Rn is determined by bit 1 and bit 0 (RAMS1, RAMS0) of RCON. The default setting of RAMS1, RAMS0 bits is 00 (page0).

| RAMS1 | RAMS0 | MOVX @Ri i=0,1 mapping to expended RAM address |
|-------|-------|--|
| 0 | 0 | \$0000 ~ \$00FF |
| 0 | 1 | \$0100 ~ \$01FF |
| 1 | 0 | \$0200 ~ \$02FF |

The port 0, port2, port3.6 and port3.7 can be used as general purpose I/O pin while port0 is open-drain structure.

System Control Register (SCONF, \$BF)

| | | | | | | | | |
|---------------|-------|--------|--------|--------|--------|--------|-------|------|
| | bit-7 | | | | | | bit-0 | |
| | WDR | Unused | Unused | Unused | Unused | Unused | OME | ALEI |
| Read / Write: | R/W | - | - | - | - | - | R/W | R/W |
| Reset value: | 0 | * | * | * | * | * | 1 | 0 |

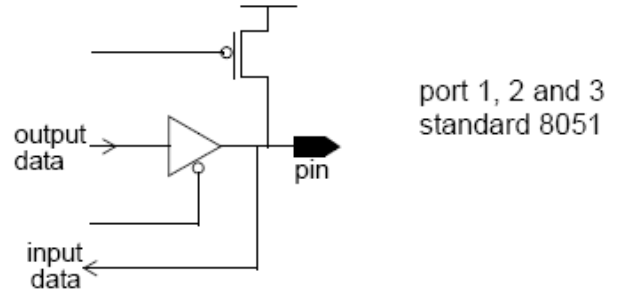
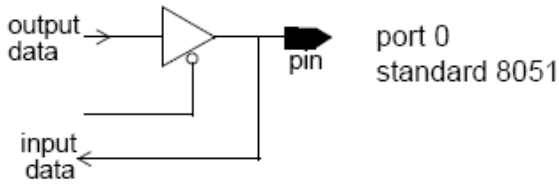
WDR: Watch Dog Timer Reset. When system reset by Watch Dog Timer overflow, WDR will be set to 1
 OME: 768 bytes on-chip RAM enable bit
 ALEI: ALE output inhibit bit, to reduce EMI

The bit 7(WDR) of SCONF is Watch Dog Timer Reset bit. It will be set to 1 when reset signal generated by WDT overflow. User should check WDR bit whenever un-predicted reset happened.

1.3 I/O Pin Configuration

The ports 1, 2 and 3 of standard 8051 have internal pull-up resistor, and port 0 has open-drain outputs. Each I/O pin can be used independently as an input or an output. For I/O ports to be used as an input pin, the port bit latch must contain a '1' which turns off the output driver FET. Then for port 1, 2 and 3 port pin is pulled high by a weak internal pull-up, and can be pulled low by an external source. The port 0 has open-drain outputs which means its pull-ups are not active during normal port operation. Writing '1' to the port 0 bit latch will causing bit floating so that it can be used as a high-impedance input.

The port 4 used as GPIO will has the same function as port 1, 2 and 3.



2. Port 4 for PLCC or QFP package :

The bit addressable port 4 is available with PLCC or QFP package. The port 4 has only 4 pins and its port address is located at 0D8H. The function of port 4 is the same as the function of port 1, port 2 and port 3.

Port4 (P4, \$D8)

| | | | | | | | | |
|---------------|--------|--------|--------|--------|-------|------|------|------|
| | bit-7 | | | | bit-0 | | | |
| | Unused | Unused | Unused | Unused | P4.3 | P4.2 | P4.1 | P4.0 |
| Read / Write: | - | - | - | - | R/W | R/W | R/W | R/W |
| Reset value: | * | * | * | * | 1 | 1 | 1 | 1 |

The bit 3, bit 2, bit 1, bit 0 output the setting to pin P4.3, P4.2, P4.1, P4.0 respectively.

The port 4 output buffers can sink 20mA and can drive LED display directly.



Extension Function Description

3. Watch Dog Timer

The Watch Dog Timer (WDT) is a 16-bit free-running counter that generate reset signal if the counter overflows. The WDT is useful for systems which are susceptible to noise, power glitches, or electronics discharge which causing software dead loop or runaway. The WDT function can help user software recover form abnormal software condition. The WDT is different from Timer0, Timer1 and Timer2 of general 8052. To prevent a WDT reset can be done by software periodically clearing the WDT counter.

The SM89516 WDT has selectable divider input for the time base source clock. To select the divider input, the setting of bit2~bit0 (PS2~PS0) OF Watch Dog Timer Control Register (WDTC) should be set accordingly.

The WDT is enable by setting 1 to the bit 7 (WDTE) of WDTC. After WDTE set to 1, the 16-bit counter starts to count with the selected time base source clock which set by PS2~PS0. It will generate a reset signal when overflows. The WDTE bit will be cleared to 0 automatically when SM89516 been reset, either hardware reset or WDT reset.

To reset the WDT is done by setting 1 to the bit 5 (CLEAR) of WDTC. This will clear the content of the 16-bit counter and let the counter re-start to count from the beginning.

3.1 Watch Dog Timer Registers: WDT Control Register (WDTC, \$9F)

| | | | | | | | | |
|---------------|-------|---|-------|--------|--------|-------|-----|-----|
| | bit-7 | | | | | bit-0 | | |
| | WDTE | R | Clear | Unused | Unused | PS2 | PS1 | PS0 |
| Read / Write: | R/W | - | R/W | - | - | R/W | R/W | R/W |
| Reset value: | 0 | * | 0 | * | * | 0 | 0 | 0 |

WDTE : Watch Dog Timer enable bit
CLEAR : Watch Dog Timer reset bit
PS2~PS0 : clock source divider selection bit

| PS [2:0] | Divider (OSC in) | Time Period (ms) @40MHz |
|----------|------------------|-------------------------|
| 000 | 8 | 13.1 |
| 001 | 16 | 26.21 |
| 010 | 32 | 52.42 |
| 011 | 64 | 104.8 |
| 100 | 128 | 209.71 |
| 101 | 256 | 419.43 |
| 110 | 512 | 838.86 |
| 111 | 1024 | 1677.72 |

4. Reduce EMI Function

The SM89516 allows user to reduce the EMI emission by setting 1 to the bit 0 (ALEI) of SCONF register. This function will inhibit the clock signal in Fosc/6Hz output to the ALE pin. This function is available when there is no external program memory or no external data RAM in the system.

**Operating Conditions**

| Symbol | Description | Min. | Typ. | Max. | Unit. | Remarks |
|---------|-----------------------|------|------|------|-------|--------------------------------|
| TA | Operating temperature | 0 | 25 | 70 | °C | Ambient temperature under bias |
| VCC5 | Supply voltage | 4.5 | 5.0 | 5.5 | V | For C Version |
| VCC3 | Supply voltage | 3 | 3.3 | 3.6 | V | For L Version |
| Fosc 25 | Oscillator Frequency | 3.0 | 16 | 16 | MHz | For 5V, 3.3V application |
| Fosc 40 | Oscillator Frequency | 3.0 | 25 | 25 | MHz | For 5V, 3.3V application |

DC Characteristics

(12MHz, typical operating conditions, valid for SM89516 series)

| Symbol | Parameter | Valid | Min. | Max. | Unit | Test Conditions |
|--------|----------------------------|------------------------|--------------------|----------------------|------|--|
| VIL1 | Input Low Voltage | port 0,1,2,3,4,#EA | -0.5 | 0.8 | V | |
| VIL2 | Input Low Voltage | RES, XTAL1 | 0 | 0.8 | V | |
| VIH1 | Input High Voltage | port 0,1,2,3,4,#EA | 2.0 | V _{cc} +0.5 | V | |
| VIH2 | Input High Voltage | RES, XTAL1 | 70%V _{cc} | V _{cc} +0.5 | V | |
| VOL1 | Output Low Voltage | port 0, ALE, #PSEN | | 0.45 | V | IOL=3.2mA |
| VOL2 | Output Low Voltage | port 1,2,3,4 | | 0.45 | V | IOL=1.6mA |
| VOH1 | Output High Voltage | port 0 | 2.4 | | V | IOH=-800uA (only for VCC =5V) |
| | | | 90%V _{cc} | | V | IOH=-80uA |
| VOH2 | Output High Voltage | port 1,2,3,4,ALE,#PSEN | 2.4 | | V | IOH=-60uA (only for VCC =5 V) |
| | | | 90%V _{cc} | | V | IOH=-10uA |
| IIL | Logical 0 Input Current | port 1,2,3,4 | | -75 | uA | V _{in} =0.45V |
| ITL | Logical Transition Current | port 1,2,3,4 | | -650 | uA | V _{in} =2.0V |
| ILI | Input Leakage Current | port 0, #EA | | ±10 | uA | 0.45V<V _{in} <V _{cc} |
| R RES | Reset Pull-down Resistance | RES | 50 | 300 | Kohm | |
| C IO | Pin Capacitance | | | 10 | pF | Freq=1MHz, Ta=25 °C |
| I CC | Power Supply Current | Vdd | | 20 | mA | Active mode, 16MHz |
| | | | | 6.5 | mA | Idle mode, 16MHz |
| | | | | 50 | uA | Power down mode |



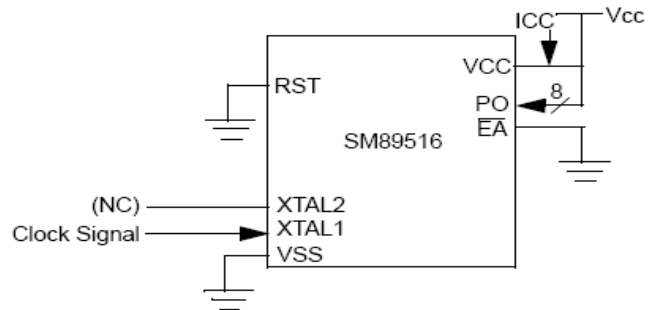
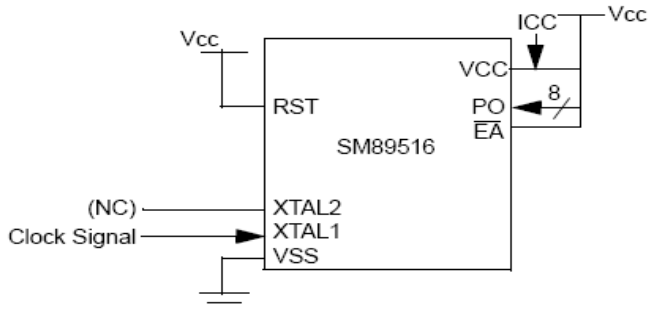
AC Characteristics

(16/25MHz, operating conditions; CL for Port 0, ALE and PSEN Outputs=100pF; CL for all Other Output=80pF)

| Symbol | Parameter | Valid Cycle | fosc=16MHz | | | Variable fosc | | | Unit | Remarks |
|----------|-----------------------------------|-------------|------------|------|-----|---------------|--------|----------|------|---------|
| | | | Min. | Typ. | Max | Min. | Typ. | Max | | |
| T LHLL | ALE pulse width | RD/WRT | 115 | | | 2xT - 10 | | | nS | |
| T AVLL | Address Valid to ALE low | RD/WRT | 43 | | | T - 20 | | | nS | |
| T LLAX | Address Hold after ALE low | RD/WRT | 53 | | | T - 10 | | | nS | |
| T LLIV | ALE low to Valid Instruction In | RD | | | 240 | | | 4xT - 10 | nS | |
| T LLPL | ALE low to #PSEN low | RD | 53 | | | T - 10 | | | nS | |
| T PLPH | #PSEN pulse width | RD | 173 | | | 3xT - 15 | | | nS | |
| T PLIV | #PSEN low to Valid Instruction In | RD | | | 177 | | | 3xT - 10 | nS | |
| T PXIX | Instruction Hold after #PSEN | RD | 0 | | | 0 | | | nS | |
| T PXIZ | Instruction Float after #PSEN | RD | | | 87 | | | T + 25 | nS | |
| T AVIV | Address to Valid Instruction In | RD | | | 292 | | | 5xT -20 | nS | |
| T PLAZ | #PSEN low to Address Float | RD | | | 10 | | | 10 | nS | |
| T RLRH | #RD pulse width | RD | 365 | | | 6xT - 10 | | | nS | |
| T WLWH | #WR pulse width | WRT | 365 | | | 6xT - 10 | | | nS | |
| T RLDV | #RD low to Valid Data In | RD | | | 302 | | | 5xT - 10 | nS | |
| T RHDX | Data Hold after #RD | RD | 0 | | | 0 | | | nS | |
| T RHDZ | Data Float after #RD | RD | | | 145 | | | 2xT+20 | nS | |
| T LLDV | ALE low to Valid Data In | RD | | | 590 | | | 8xT - 10 | nS | |
| T AVDV | Address to Valid Data In | RD | | | 542 | | | 9xT - 20 | nS | |
| T LLYL | ALE low to #WR High or #RD low | RD/WRT | 178 | | 197 | 3xT - 10 | | 3xT+10 | nS | |
| T AVYL | Address Valid to #WR or #RD low | RD/WRT | 230 | | | 4xT - 20 | | | nS | |
| T QVWH | Data Valid to #WR High | WRT | 403 | | | 7xT - 35 | | | nS | |
| T QVWX | Data Valid to #WR transition | WRT | 38 | | | T - 25 | | | nS | |
| T WHQX | Data hold after #WR | WRT | 73 | | | T + 10 | | | nS | |
| T RLAZ | #RD low to Address Float | RD | | | | | | 5 | nS | |
| T YALH | #WR or #RD high to ALE high | RD/WRT | 53 | | 72 | T -10 | | T + 10 | nS | |
| T CHCL | clock fall time | | | | | | | | nS | |
| T CLCX | clock low time | | | | | | | | nS | |
| T CLCH | clock rise time | | | | | | | | nS | |
| T CHCX | clock high time | | | | | | | | nS | |
| T, TCLCL | clock period | | | 63 | | | 1/fosc | | nS | |

ICC Active mode test circuit

ICC Idle mode test circuit

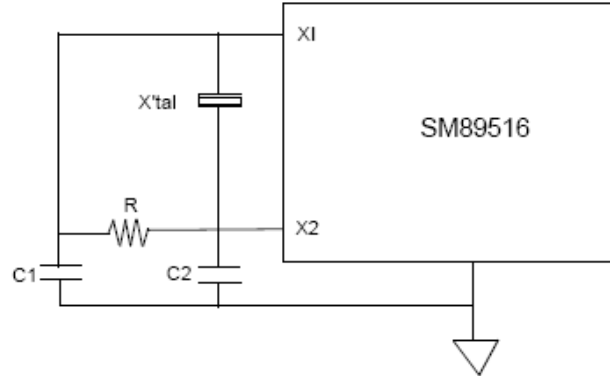


Specifications subject to change without notice contact your sales representatives for the most recent information.



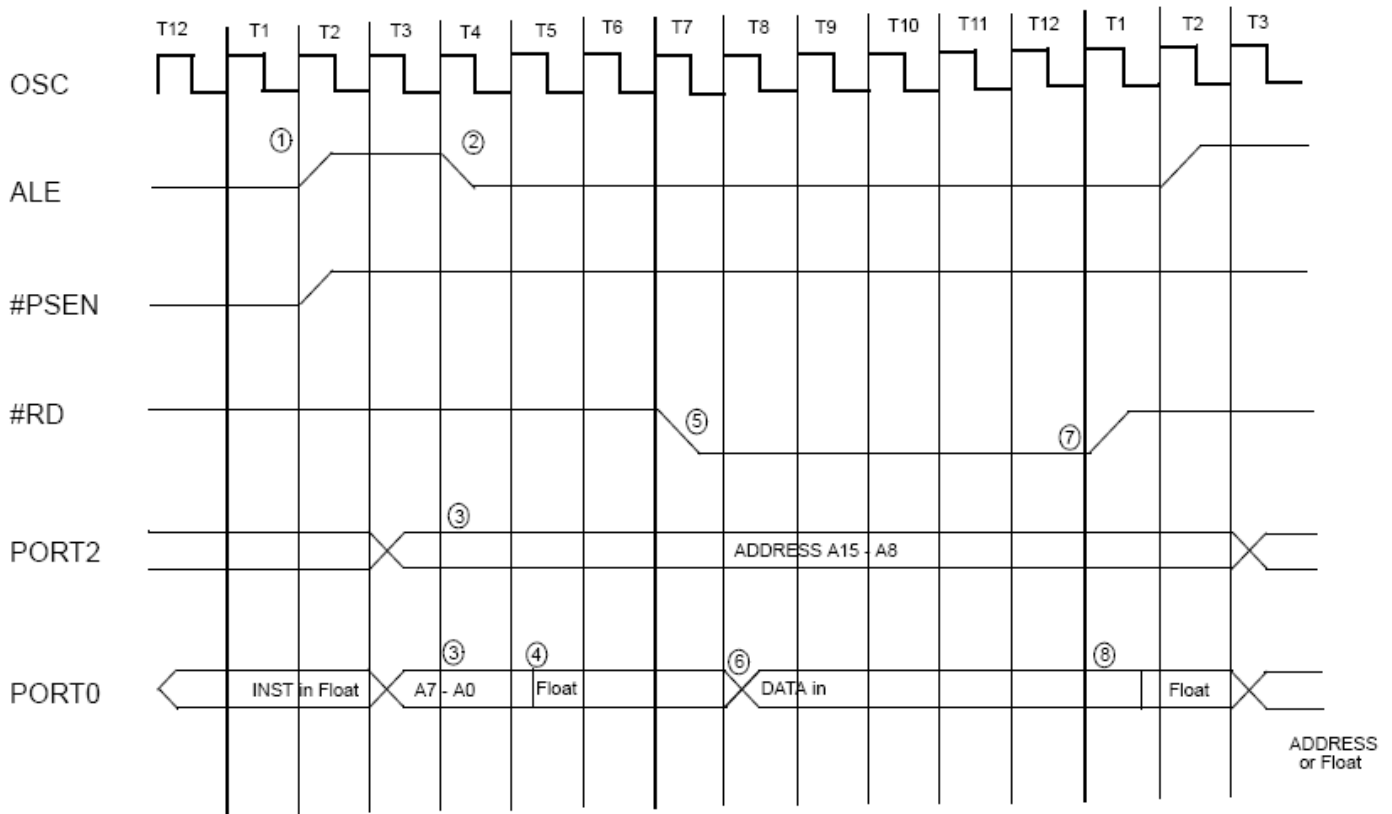
Application Reference

| Valid for SM89516 | | | | |
|-------------------|-------|-------|-------|-------|
| X'tal | 3MHz | 6MHz | 9MHz | 12MHz |
| C1 | 30 pF | 30 pF | 30 pF | 22 pF |
| C2 | 30 pF | 30 pF | 30 pF | 22 pF |
| R | open | open | open | open |
| | | | | |
| X'tal | 16MHz | 25MHz | | |
| C1 | 30 pF | 15 pF | | |
| C2 | 30 pF | 15 pF | | |
| R | open | open | | |



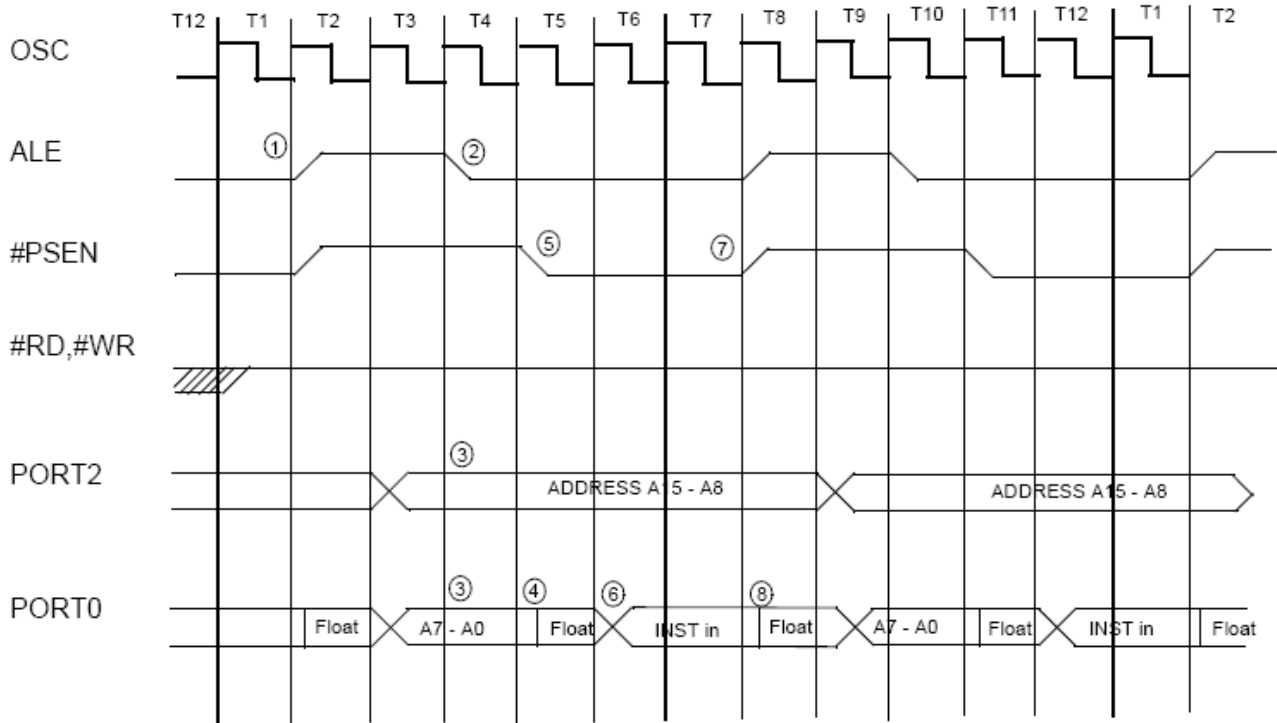
NOTE: Oscillation circuit may differ with different crystal or ceramic resonator in higher oscillation frequency which is due to each crystal or ceramic resonator having its own characteristics. User should check with the crystal or ceramic resonator manufacturer for appropriate values of external components.

Data Memory Read Cycle Timing

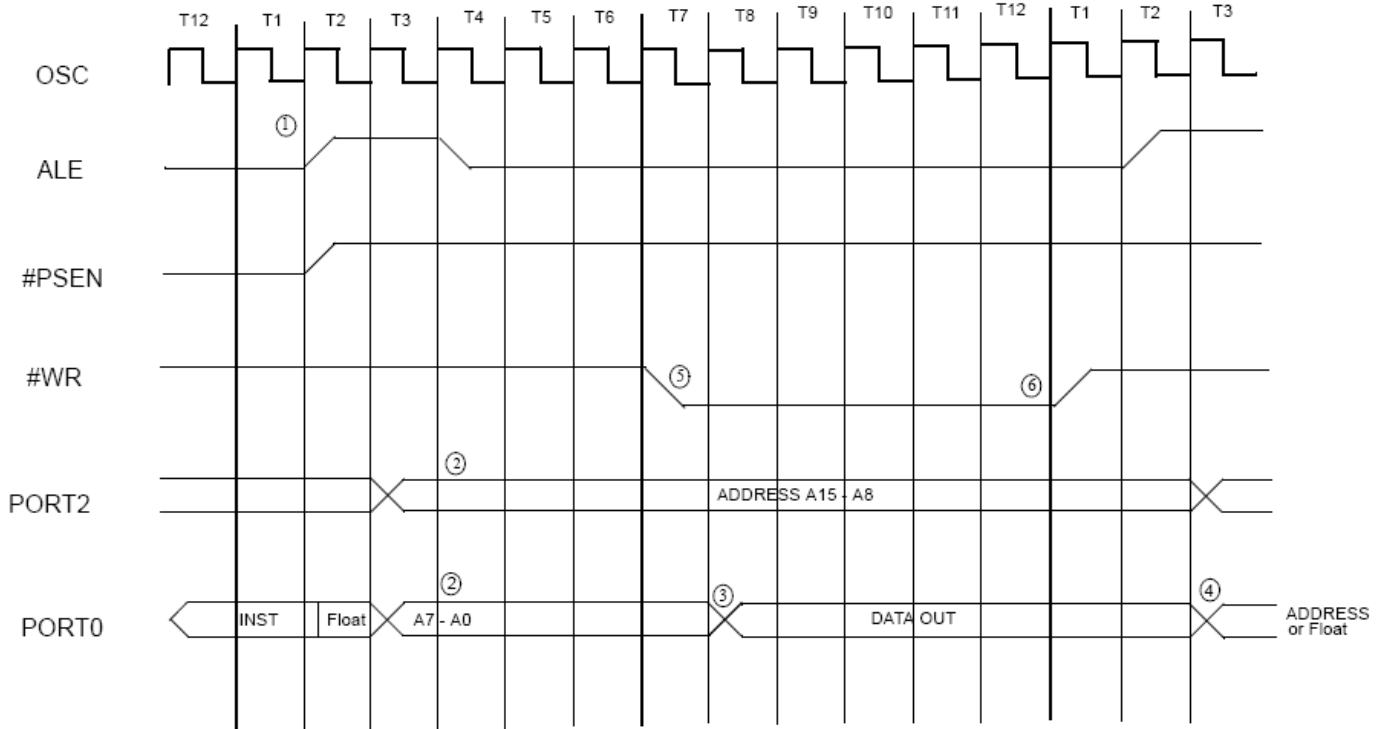




Program Memory Read Cycle Timing

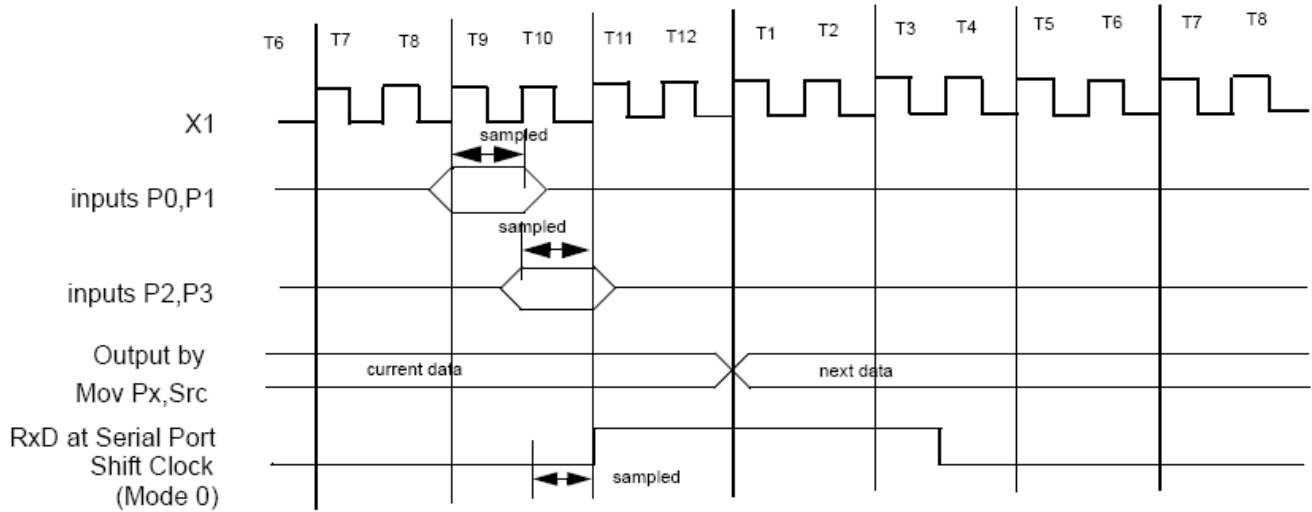


Data Memory Write Cycle Timing

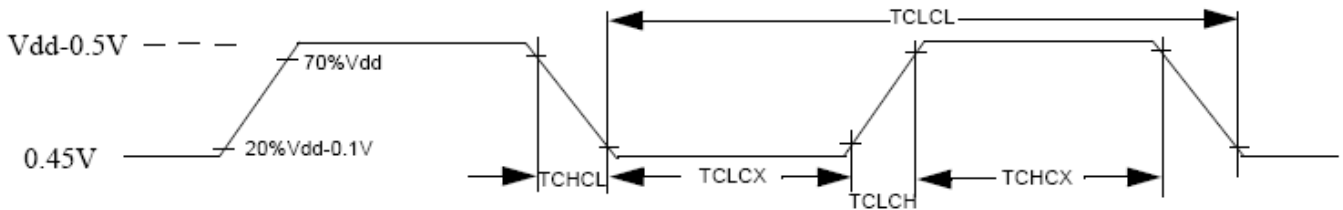




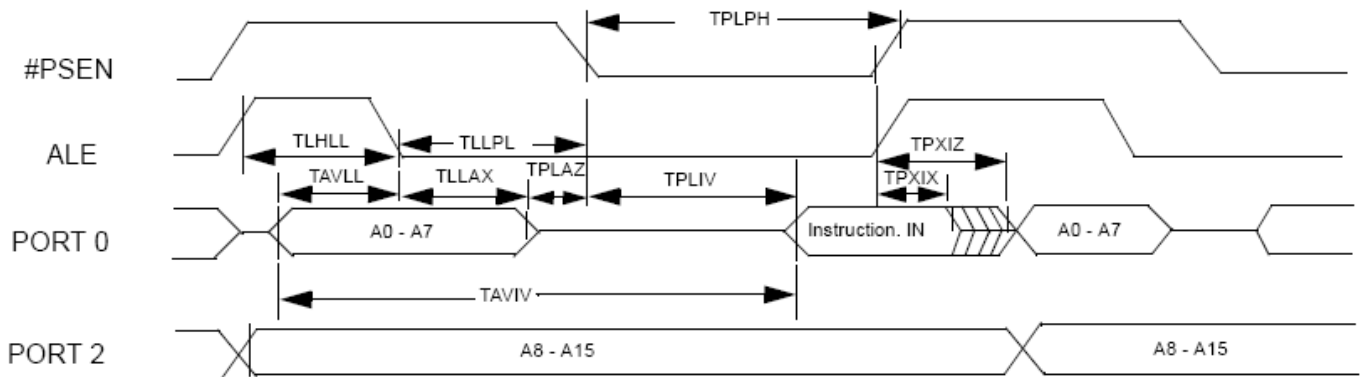
I/O Ports Timing



Timing Critical, Requirement of External Clock (Vss=0.0V is assumed)

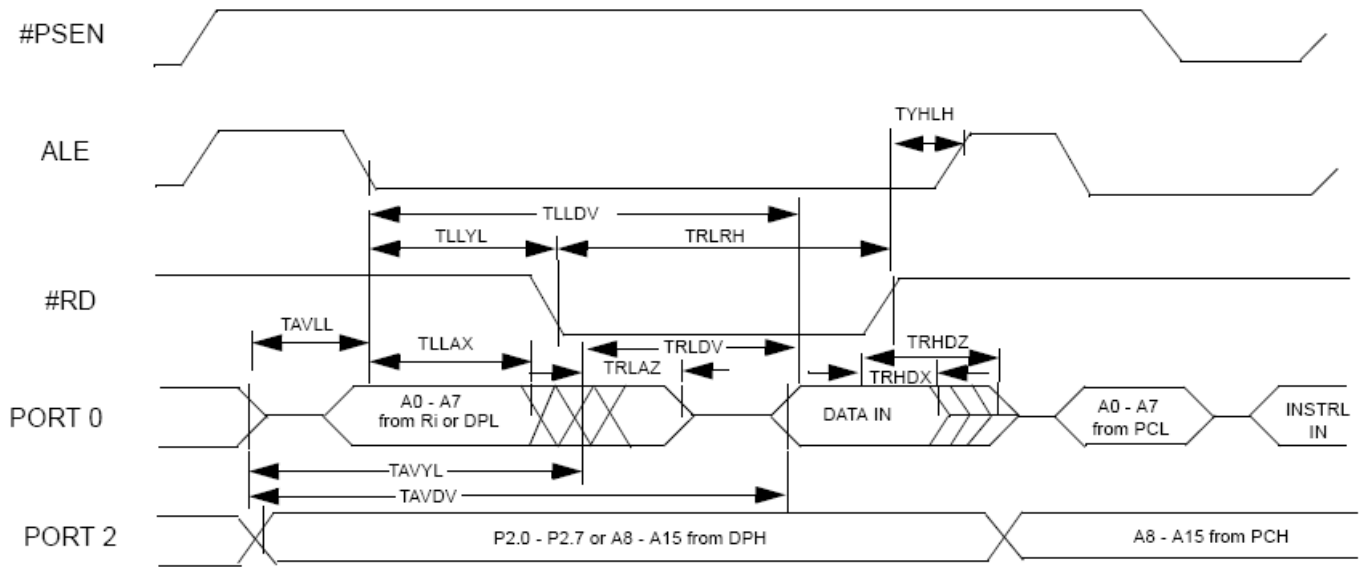


Tm.I External Program Memory Read Cycle

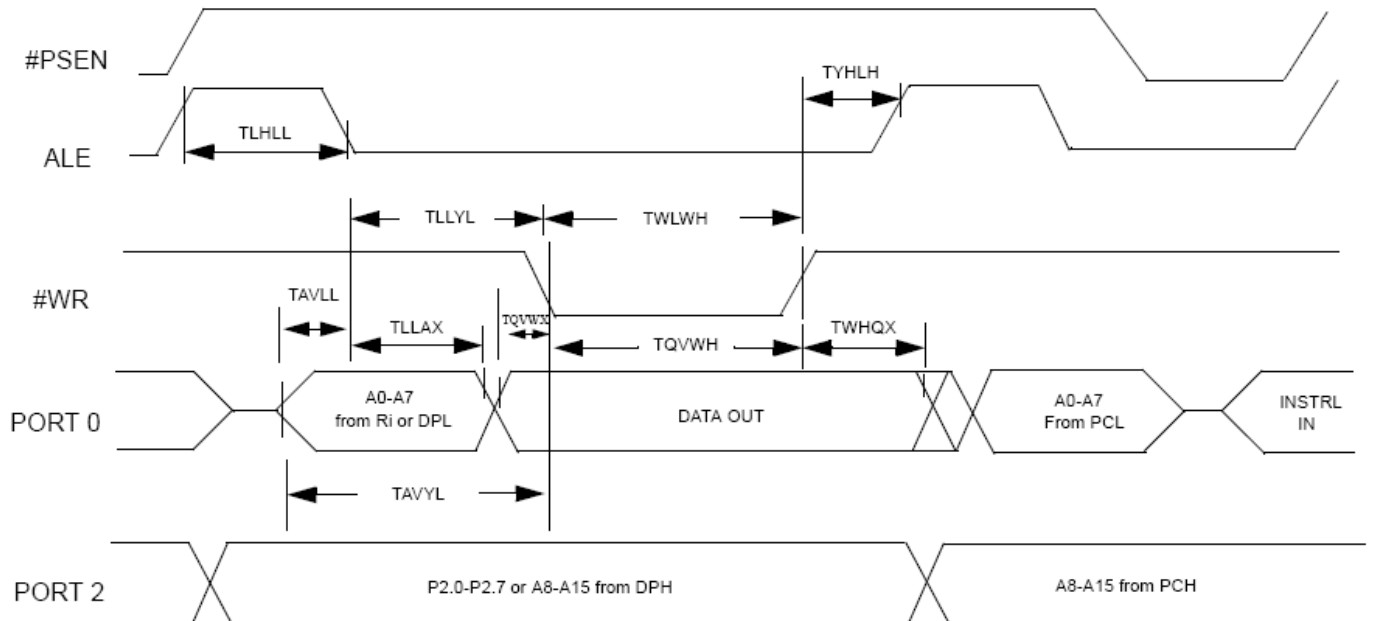




Tm.II External Data Memory Read Cycle

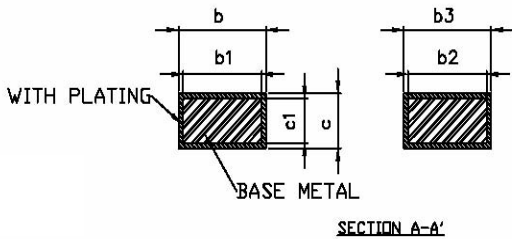
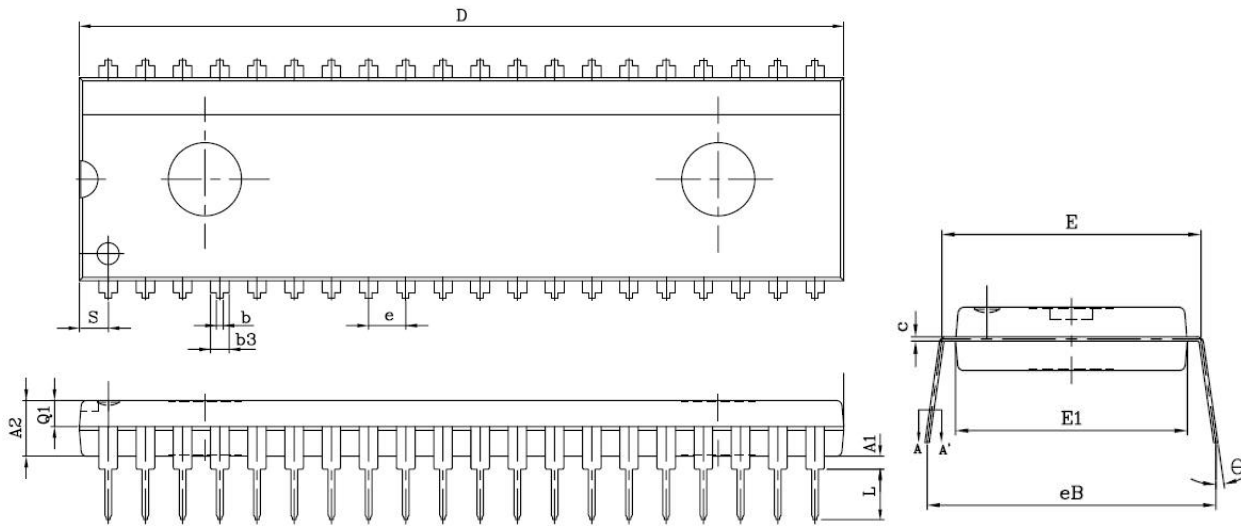


Tm.III External Data Memory Write Cycle





PDIP 40L (600mil) Package Information :



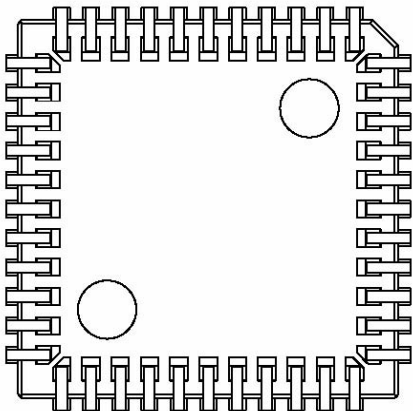
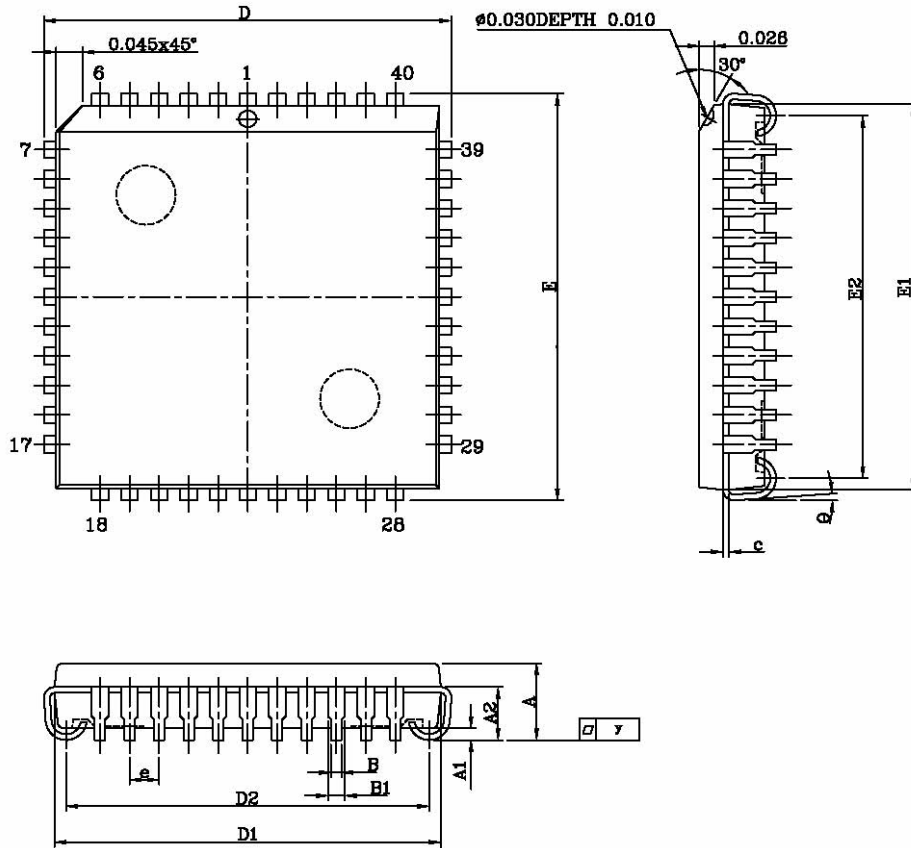
| Symbol | Dimension in mm | | | Dimension in MIL | | |
|-----------|-----------------|-------|-------|------------------|------|------|
| | Min | Nom | Max | Min | Nom | Max |
| A1 | 0.254 | — | — | 10 | — | — |
| A2 | 3.683 | 3.810 | 3.937 | 145 | 150 | 155 |
| b | 0.356 | 0.500 | 0.660 | 14 | 20 | 26 |
| b1 | 0.356 | 0.457 | 0.508 | 14 | 18 | 22 |
| b2 | 1.016 | 1.270 | 1.524 | 40 | 50 | 60 |
| b3 | 1.016 | 1.321 | 1.626 | 40 | 52 | 64 |
| c | 0.203 | 0.254 | 0.432 | 8 | 10 | 17 |
| c1 | 0.203 | 0.254 | 0.356 | 8 | 10 | 14 |
| D | 52.07 | 52.2 | 52.32 | 2050 | 2055 | 2060 |
| E | 14.99 | 15.24 | 15.49 | 590 | 600 | 610 |
| E1 | 13.69 | 13.87 | 13.94 | 539 | 546 | 549 |
| e | — | 2.540 | — | — | 100 | — |
| eB | 15.75 | 16.26 | 16.76 | 620 | 640 | 660 |
| L | 2.921 | 3.302 | 3.683 | 115 | 130 | 145 |
| S | 1.727 | 1.981 | 2.235 | 68 | 78 | 88 |
| Q1 | 1.651 | 1.778 | 1.905 | 65 | 70 | 75 |
| θ | 0° | — | 10° | 0° | — | 10° |

Note:

1. Refer to JEDEC STD.MS-011(AC).
2. Dimension D and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. D and E1 are maximum plastic body size dimension include mold mismatch.
3. Dimension b3 does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b3 dimension by more than 0.2mm.



PLCC 44L Package Information :

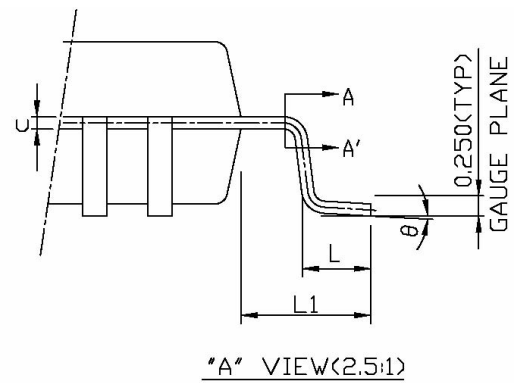
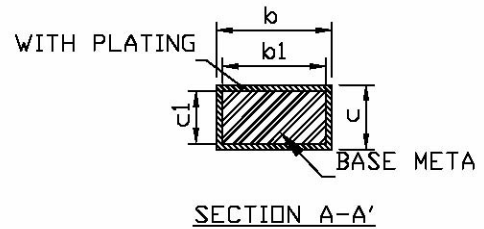
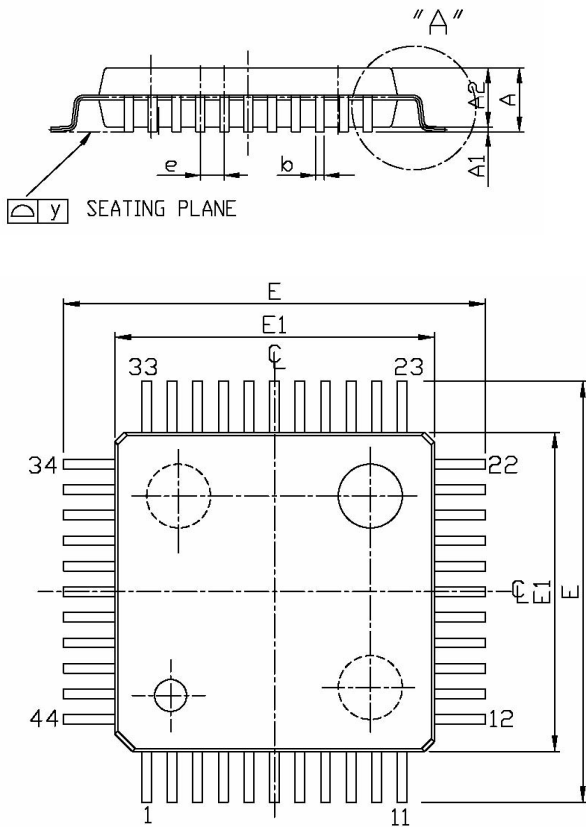


| UNIT SYMBOL | INCH(REF) | MM(BASE) |
|-------------|--------------------------|--------------------------|
| A | 0.180(MAX) | 4.572(MAX) |
| A1 | 0.024 ±0.005 | 0.52 ±0.14 |
| A2 | 0.105 ±0.005 | 2.667 ±0.127 |
| B | 0.018 + 0.004 - 0.002 | 0.457 + 0.102 - 0.051 |
| B1 | 0.028 + 0.004 - 0.002 | 0.711 + 0.102 - 0.051 |
| c | 0.010(TYP) | 0.254(TYP) |
| D | 0.690 ±0.010 | 17.526 ±0.254 |
| D1 | 0.653 ±0.003 | 16.586 ±0.076 |
| D2 | 0.610 ±0.020 | 15.494 ±0.508 |
| E | 0.690 ±0.010 | 17.526 ±0.254 |
| E1 | 0.653 ±0.003 | 16.586 ±0.076 |
| E2 | 0.610 ±0.010 | 15.494 ±0.254 |
| e | 0.050(TYP) | 1.270(TYP) |
| y | 0.003(MAX) | 0.076(MAX) |
| θ | 0~5° | 0~5° |

Specifications subject to change without notice contact your sales representatives for the most recent information.



QFP 44L(10x10x2.0mm) Package Information :



| Symbol | Dimension in mm | | | Dimension in MIL | | |
|------------|-----------------|-------|-------|------------------|------|------|
| | Min | Nom | Max | Min | Nom | Max |
| A | — | — | 2.45 | — | — | 964 |
| A1 | 0.05 | 0.15 | 0.25 | 2.1 | 6.0 | 9.6 |
| A2 | 1.90 | 2.00 | 2.10 | 74.8 | 78.7 | 82.7 |
| b | 0.29 | 0.32 | 0.45 | 11.4 | 12.6 | 17.7 |
| b1 | 0.29 | 0.30 | 0.41 | 11.4 | 11.8 | 16.1 |
| c | 0.11 | 0.17 | 0.23 | 4.3 | 6.7 | 9.1 |
| c1 | 0.11 | 0.15 | 0.19 | 4.3 | 5.9 | 7.5 |
| E | 13.00 | 13.20 | 13.40 | 512 | 520 | 528 |
| E1 | 9.90 | 10.00 | 10.10 | 390 | 394 | 398 |
| [e] | — | 0.800 | — | — | 31.5 | — |
| L | 0.73 | 0.88 | 1.03 | 28.7 | 34.6 | 40.6 |
| L1 | 1.50 | 1.60 | 1.70 | 59.1 | 63.0 | 66.9 |
| y | — | — | 0.076 | — | — | 3 |
| θ | 0° | — | 7° | 0° | — | 7° |

Note:

1. Refer to JEDC STD.MS-022(AB).
2. Dimension E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side.E1 are maximum plastic body size dimension include mold mismatch .
3. Dimension b does not include dambar protrusion .Allowable dambar protrusion shall not cause the lead width to exceed the maximum b3 dimension by more than 0.1 mm.

Specifications subject to change without notice contact your sales representatives for the most recent information.



| e MCU writer list | | |
|--|--|--|
| Company | Contact info | Programmer Model Number |
| <u>Advantech</u> 7F, No.98, Ming-Chung Rd., Shin-Tien City, Taipei, Taiwan, ROC Web site: http://www.aec.com.tw | Tel:02-22182325 Fax:02-22182435 E-mail: aecwebmaster@advantech.com.tw | Lab Tool - 48XP (1 * 1) Lab Tool - 848 (1*8) |
| <u>Hi-Lo</u> 4F, No. 20, 22, LN, 76, Rui Guang Rd., Nei Hu, Taipei, Taiwan, ROC. Web site: http://www.hilosystems.com.tw | Tel:02-87923301 Fax:02-87923285 E-mail: support@hilosystems.com.tw | All - 11 (1*1) Gang - 08 (1*8) |
| <u>Leap</u> 6th F1-4, Lane 609, Chunghsin Rd., Sec. 5, Sanchung, Taipei Hsien, Taiwan, ROC Web site: http://www.leap.com.tw | Tel:02-29991860 Fax:02-29990015 E-mail: service@leap.com.tw | Leap-48 (1*1) SU - 2000 (1*8) |
| <u>Xeltek Electronic Co., Ltd</u> 338 Hongwu Road, Nanjing, China 210002 Web site: http://www.xeltek-cn.com | Tel:+86-25-84408399, 84543153-206 E-mail: xelclw@jlonline.com , xelgbw@jlonline.com | Superpro/2000 (1*1) Superpro/280U (1*1) Superpro/L+(1*1) |