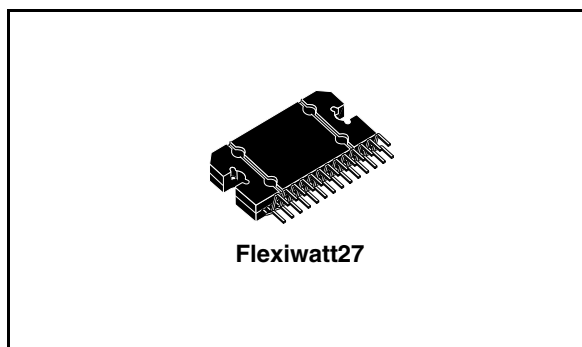


## Quad power amplifier with built-in voltage converter

### Features

- Multipower BCD technology
- DMOS power output
- Non-switching high efficiency amplifier
- Switching high efficiency voltage converter
- High output power capability 4x60W EIAJ/4Ω
- Full I<sup>2</sup>C Bus driving:
  - St-by
  - Independent front/rear soft play/mute
  - Selectable gain 26dB - 12dB (for low noise line output function)
  - High efficiency enable/disable
  - Voltage converter enable/disable
  - Regulated voltage selection
  - Switching frequency selection
- Hardware mute function
- Full fault protection
- DC offset detection
- Four independent short circuit protection
- Clipping detector with selectable threshold (1 % / 10 %) via I<sup>2</sup>C bus



### Description

The TDA7565 is a new BCD technology quad bridge type of car radio amplifier in Flexiwatt27 package specially intended for car radio applications. Thanks to the DMOS output stage the TDA7565 has a very low distortion allowing a clear powerful sound.

The built-in voltage converter control block assures a very high output power with an extremely low number of added components.

The dissipated power under average listening condition is aligned to the conventional solutions (4 x 40 W).

**Table 1. Device summary**

Order code	Package	Packing
TDA7565	Flexiwatt27	Tube

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# 1 Block and pins connection diagrams

Figure 1. Block diagram

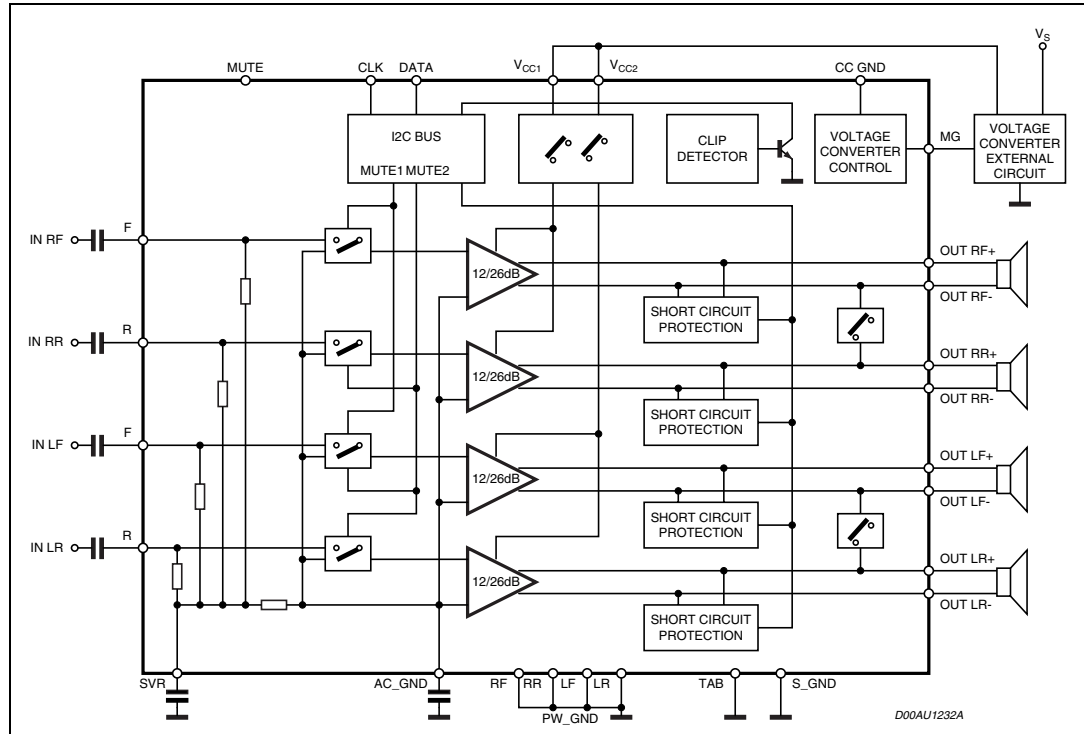
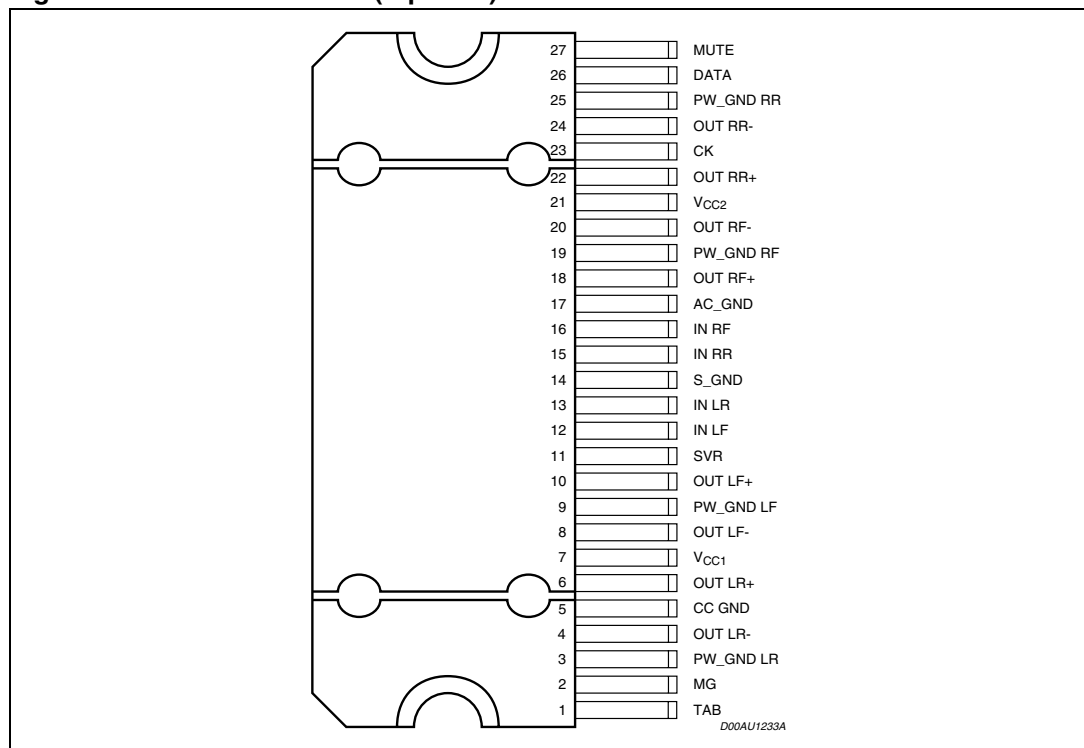


Figure 2. Pins connection (top view)



## 2 Electrical specification

### 2.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{\text{opc OFF}}$	Operating supply voltage, converter off	18	V
$V_{\text{opc ON}}$	Operating supply voltage, converter on	25	V
$V_S$	DC supply voltage	28	V
$V_{\text{peak}}$	Peak supply voltage (for $t = 50$ ms)	50	V
$V_{\text{CK}}$	CK pin voltage	6	V
$V_{\text{DATA}}$	Data pin voltage	6	V
$I_O$	Output peak current (not repetitive $t = 100$ $\mu\text{s}$ )	8	A
$I_O$	Output peak current (repetitive $f > 10$ Hz)	6	A
$P_{\text{tot}}$	Power dissipation $T_{\text{case}} = 70$ °C	80	W
$T_{\text{stg}}, T_j$	Storage and junction temperature	-55 to 150	°C

### 2.2 Thermal data

Table 3. Thermal data

Symbol	Description	Value	Unit
$R_{\text{th j-case}}$	Thermal resistance junction to case	Max. 1	°C/W

### 2.3 Electrical characteristics

Table 4. Electrical characteristics

(Refer to the test circuit,  $V_S = 13.5\text{V}$ ;  $R_L = 4\Omega$ ;  $f = 1$  kHz; voltage converter disabled ( $V_{\text{Coff}}$ );  $T_{\text{amb}} = 25^\circ\text{C}$ ; unless otherwise specified).

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
<b>Power amplifier</b>						
$V_S$	Supply voltage range		8		18	V
$I_d$	Total quiescent drain current			180	300	mA
$I_d$	Total quiescent drain current ( $V_{\text{Con}}$ )			TBD		mA
$P_O$	Output power ( $V_{\text{Coff}}$ ) $V = 14.4$ V	EIAJ ( $V_S = 13.7$ V)		35		W
		THD = 10 %		25		W
		THD = 1 %		20		W

**Table 4. Electrical characteristics (continued)**

(Refer to the test circuit,  $V_S = 13.5V$ ;  $R_L = 4\Omega$ ;  $f = 1\text{ kHz}$ ; voltage converter disabled ( $V_{COff}$ );  $T_{amb} = 25^\circ C$ ; unless otherwise specified).

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$P_O$	Output power ( $V_{COn}$ ) $V = 14.4V$	EIAJ ( $V_S = 13.7V$ )		60		W
		THD = 10%		40		W
		THD = 1%		31		W
THD	Total harmonic distortion	$P_O = 1\text{ W to }12\text{ W}$ ; STD MODE HE MODE; $P_O = 1\text{-}2\text{ W}$ HE MODE; $P_O = 4\text{-}12\text{ W}$		0.03 0.03 0.1	0.1	% % %
		$P_O = 1\text{-}12\text{ W}$ , $f = 10\text{ kHz}$		0.15	0.5	%
$C_T$	Cross talk	$f = 1\text{ kHz to }10\text{ kHz}$ , $R_G = 600\ \Omega$	50	55		dB
$R_{IN}$	Input impedance		60	100	130	$K\Omega$
$G_{V1}$	Voltage gain 1		25.5	26	26.5	dB
$\Delta G_{V1}$	Voltage gain match 1		-1		1	dB
$G_{V2}$	Voltage gain 2		11.5	12	12.5	dB
$\Delta G_{V2}$	Voltage gain match 2		-1		1	dB
$E_{IN1}$	Output noise voltage 1	$R_g = 600\ \Omega$ ; $G_V = 26\text{ dB}$ filter 20 Hz to 22 kHz		60	100	$\mu V$
$E_{IN2}$	Output noise voltage 2	$R_g = 600\ \Omega$ ; $G_V = 26\text{ dB}$ filter 20 Hz to 12 kHz		15	20	$\mu V$
SVR	Supply voltage rejection	$f = 100\text{ Hz to }10\text{ kHz}$ ; $V_r = 1V\text{ pk}$ ; $R_g = 600\ \Omega$	50	60		dB
BW	Power bandwidth	(-3 dB)	75			KHz
$A_{SB}$	Stand-by attenuation		70	100		dB
$I_{SB}$	Stand-by current				100	$\mu A$
$A_M$	Mute attenuation		70	90		dB
$V_{OS}$	Offset voltage	Mute and play	-100		100	mV
$V_{AM}$	Min. supply voltage threshold		6.5	7	7.5	V
	Slew rate		1.5			V/ $\mu s$
$T_{ON}$	Turn on delay	D2/D1 (IB1) 0 to 1		10	20	ms
$T_{OFF}$	Turn off delay	D2/D1 (IB1) 1 to 0		10	20	ms
	Thermal foldback junction temperature		155	170	185	$^\circ C$
$CD_{THD}$	Clip det thd. level	D0 (IB1) = 0	0	1	2	%
		D0 (IB1) = 1	5	10	15	%
$V_O$	Offset detection	Power amplifier = play AC Input = 0	$\pm 1.5$	$\pm 2$	$\pm 2.5$	V
$T_{hw}$	Thermal warning			165		$^\circ C$

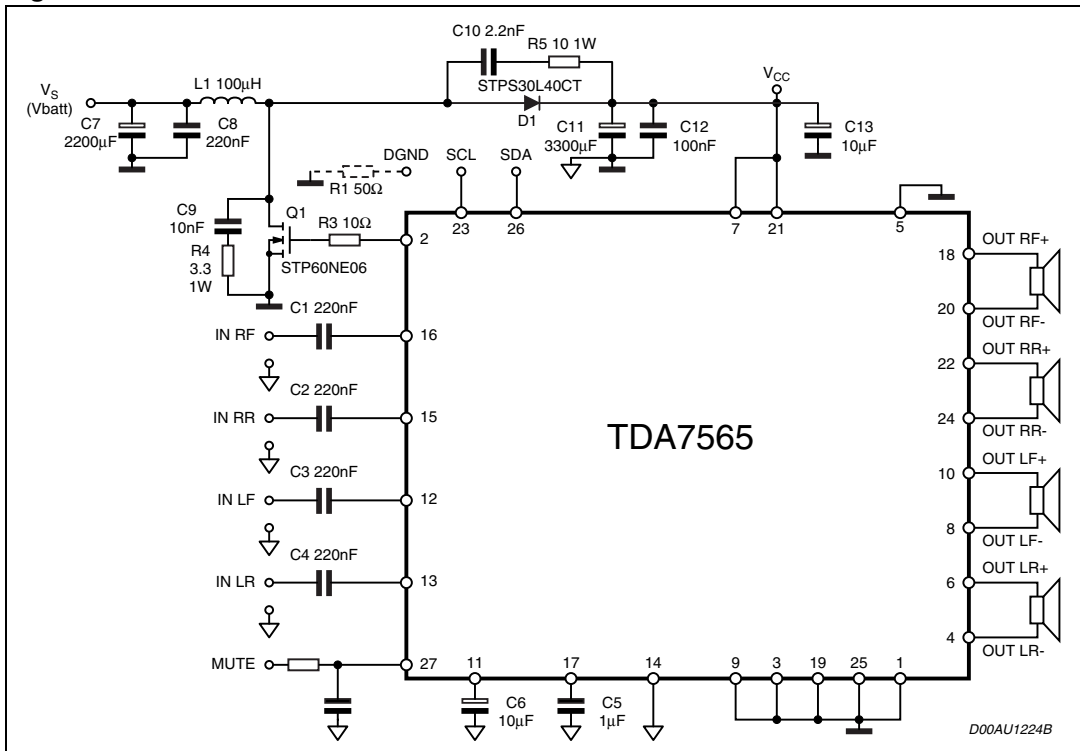
**Table 4. Electrical characteristics (continued)**

(Refer to the test circuit,  $V_S = 13.5V$ ;  $R_L = 4\Omega$ ;  $f = 1\text{ kHz}$ ; voltage converter disabled ( $VC_{Off}$ );  $T_{amb} = 25^\circ C$ ; unless otherwise specified).

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
<b>I<sup>2</sup>C Bus interface</b>						
$f_{SCL}$	Clock frequency				400	KHz
$V_{IL}$	Input low voltage				1.5	V
$V_{IH}$	Input high voltage		2.3			V
$V_{Min(pin27)}$	Mute in threshold voltage	Amp. mute			1.5	V
$V_{Mout(pin27)}$	Mute out threshold voltage		3.5			V
$A_{M(pin\ 27)}$	Mute attenuation		80	90		
<b>Voltage converter</b>						
$V_{cc1}$ , $V_{cc2}$	Converter output voltage ( $VC = ON$ )	$V_S = 14\text{ V}$ D3 (IB2) = 0; D6 (IB2) = 0 D3 (IB2) = 1; D6 (IB2) = 0 D3 (IB2) = 0; D6 (IB2) = 1 D3 (IB2) = 1; D6 (IB2) = 1		15 16.5 17.5 18.5		V V V V
$F_s$	Voltage converter switching frequency	D6 (IB1) = 0; D7 (IB1) = 0 D6 (IB1) = 1; D7 (IB1) = 0 D6 (IB1) = 0; D7 (IB1) = 1 D6 (IB1) = 1; D7 (IB1) = 1		100 150 260 400		kHz kHz kHz kHz
$V_{mgl}$	MOS gate output low voltage	$I_o = 250\text{ mA}$			1	V
$V_{mgh}$	MOS gate output high voltage	$I_o = 20\text{ mA}$ $I_o = 200\text{ mA}$		10.5 10		V V
$V_{mgclamp}$	MOS gate output clamp voltage	$I_o = 5\text{ mA}$		TBD		V
$t_f$	Fall time	$C_o = 1\text{ nF}$		20		ns
$t_r$	Rise time	$C_o = 1\text{ nF}$		50		ns
$V_{mgl}$ ( $VC_{off}$ )	MOS gate output voltage with voltage converter disabled	$I_o = 5\text{ mA}$			0.5	V



Figure 3. Demoboard schematic



## 3 I<sup>2</sup>C bus interface

Data transmission from microprocessor to the TDA7565 and vice versa takes place through the 2 wires I<sup>2</sup>C bus interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

### 3.1 Data validity

As shown by [Figure 4](#), the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

### 3.2 Start and stop conditions

As shown by [Figure 5](#) a start condition is a high to low transition of the SDA line while SCL is HIGH. The stop condition is a low to high transition of the SDA line while SCL is high.

### 3.3 Byte format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

### 3.4 Acknowledge

The transmitter\* puts a resistive high level on the SDA line during the acknowledge clock pulse (see [Figure 6](#)). The receiver\*\* the acknowledges has to pull-down (low) the SDA line during the acknowledge clock pulse, so that the SDA line is stable low during this clock pulse.

\* Transmitter

- master ( $\mu$ P) when it writes an address to the TDA7565
- slave (TDA7565) when the  $\mu$ P reads a data byte from TDA7565

\*\* Receiver

- slave (TDA7565) when the  $\mu$ P writes an address to the TDA7565
- master ( $\mu$ P) when it reads a data byte from TDA7565

**Figure 4. Data validity on the I<sup>2</sup>C bus**

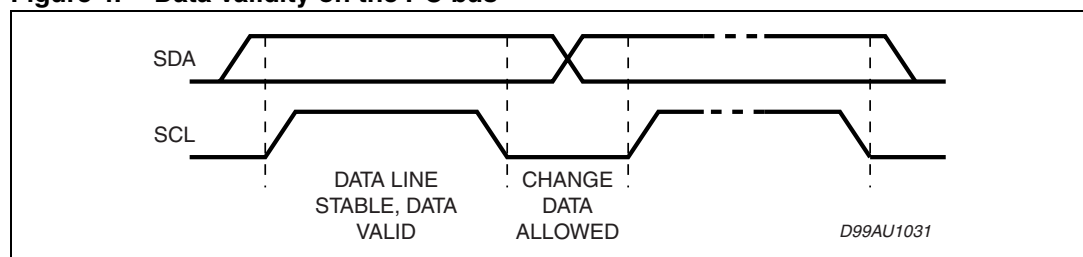


Figure 5. Timing diagram on the I<sup>2</sup>C bus

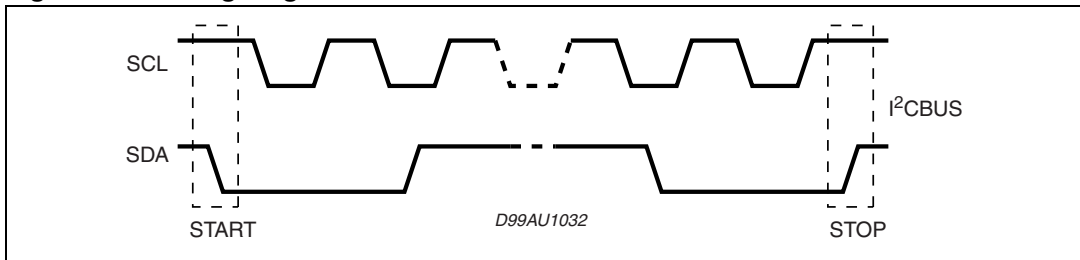
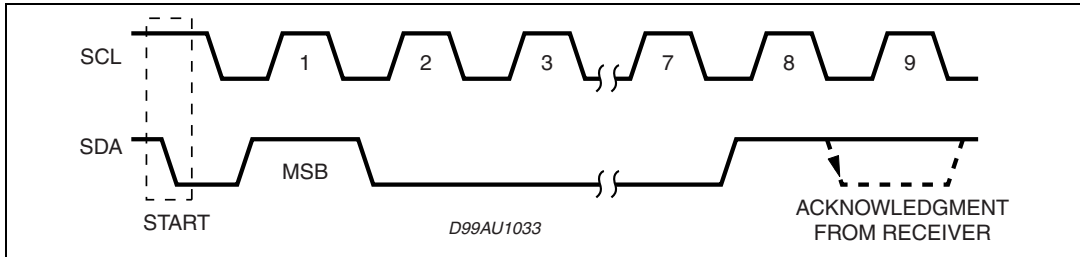


Figure 6. Acknowledge on the I<sup>2</sup>C bus



## 4 Software specifications

All the functions of the TDA7565 are activated by I<sup>2</sup>C interface.

The bit 0 of the "ADDRESS BYTE" defines if the next bytes are write instruction (from  $\mu$ P to TDA7565) or read instruction (from TDA7565 to  $\mu$ P).

**Table 5. Chip address**

Bit	Instruction
D7	Address bit
D6	Address bit
D5	Address bit
D4	Address bit
D3	Address bit
D2	Address bit
D1	Address bit
D0(R/W)	Read/Write bit 0 = Write instruction 1 = read instruction

If R/W = 0, the  $\mu$ P sends 2 "Instruction Bytes": IB1 and IB2.

**Table 6. IB1**

Bit	Instruction
D7	Sel. freq. switch 1
D6	Sel. freq. switch 2
D5	Offset detection start (D5 = 1) Offset detection stop (D5 = 0) (off)
D4	Front channel Gain = 26dB (D4 = 0) Gain = 12dB (D4 = 1)
D3	Rear channel Gain = 26dB (D3 = 0) Gain = 12dB (D3 = 1)
D2	Mute front channels (D2 = 0) Unmute front channels (D2 = 1)
D1	Mute rear channels (D1 = 0) Unmute rear channels (D1 = 1)
D0	CD 1% (D0 = 0) CD 10% (D0 = 1)

**Table 7. IB2**

Bit	Instruction
D7	Voltage converter enabled (D7 = 1) Voltage converter disabled (D7 = 0)
D6	Regulated voltage selection 1
D5	Test speed
D4	Stand-by on - amplifier not working - (D4 = 0) Stand-by off - amplifier working - (D4 = 1)
D3	Regulated voltage selection 0)
D2	To be forced to "Level 1"
D1	Right channel Power amplifier working in standard mode (D1 = 0) Power amplifier working in Hi Eff. mode(D1 = 1)
D0	Left channel Power amplifier working in standard mode (D0 = 0) Power amplifier working in Hi Eff. mode(D0 = 1)

**Table 8. DB1**

Bit	Instruction
D7	Thermal warning
D6	X
D5	X
D4	X
D3	X
D2	Offset (LF)
D1	Short circuit protection (CH1)
D0	X

**Table 9. DB2**

Bit	Instruction
D7	Off status
D6	X
D5	Clip detector output
D4	X
D3	X
D2	Offset (LR)
D1	Short circuit protection (CH2)
D0	X

**Table 10. DB3**

Bit	Instruction
D7	St-by status
D6	X
D5	X
D4	X
D3	X
D2	Offset (RF)
D1	Short circuit protection (CH3)
D0	X

**Table 11. DB4**

Bit	Instruction
D7	X
D6	X
D5	X
D4	X
D3	X
D2	Offset (RR)
D1	Short circuit protection (CH4)
D0	X

## 5 Examples of bytes sequence

1 - Turn-on of the power amplifier with 26 dB gain, mute on, diagnostic defeat, high eff. mode, voltage converter disabled.

Start	Address byte with D0 = 0	ACK	IB1	ACK	IB2	ACK	STOP
			XX00X000		0XX1XX10		

2 - Turn-off of the power amplifier

Start	Address byte with D0 = 0	ACK	IB1	ACK	IB2	ACK	STOP
			XXXXXXXX		XXX0XXX0		

4 - Offset detection procedure start

Start	Address byte with D0 = 0	ACK	IB1	ACK	IB2	ACK	STOP
			XX1XX11X		XXX1XXX0		

5 - Offset detection procedure stop and reading operation.

Start	Address byte with D0 = 1	ACK	DB1	STOP

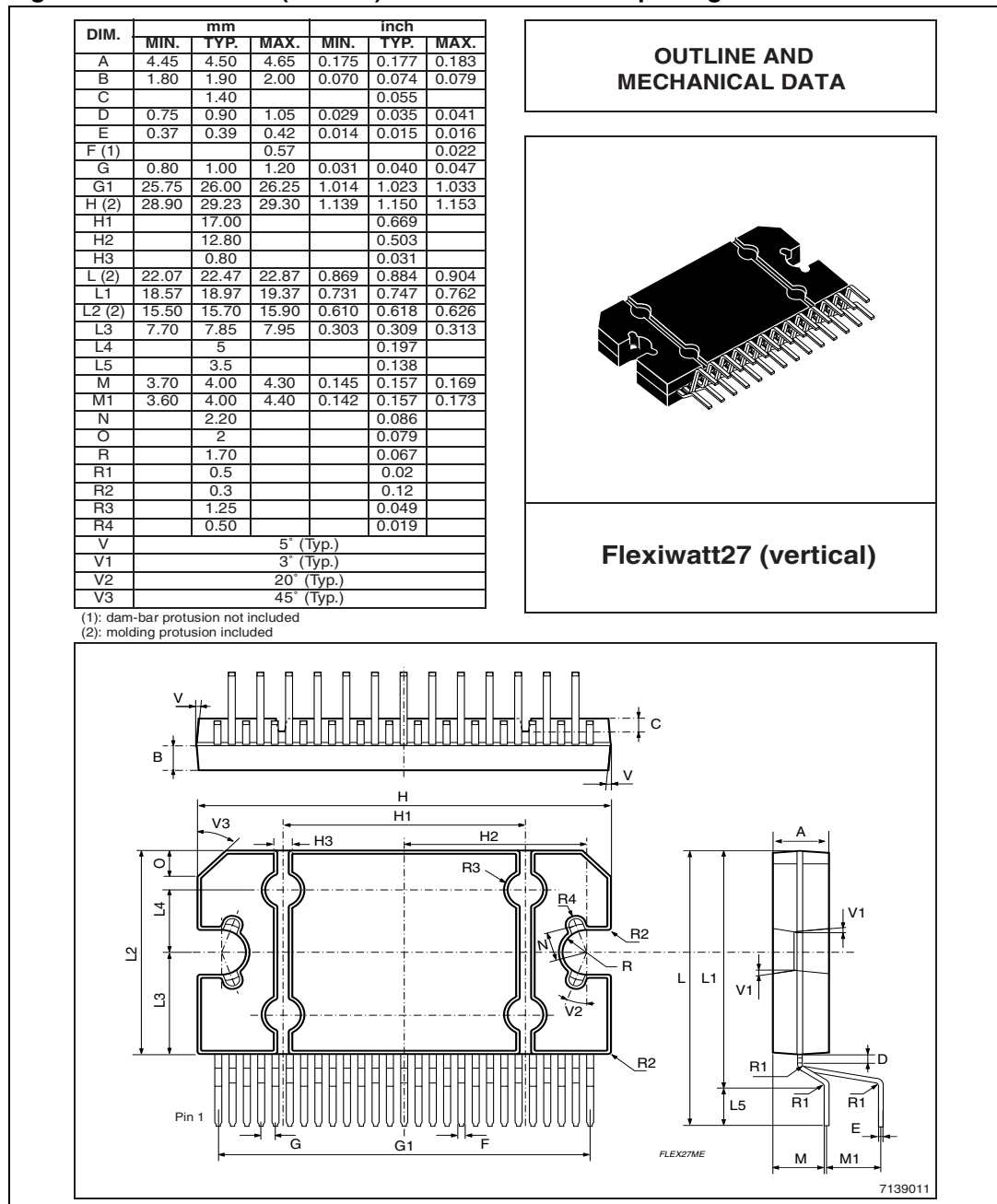
- The purpose of this test is to check if a D.C. offset (2V typ.) is present on the outputs, produced by input capacitor with anomalous leakage current or humidity between pins.
- The delay from 3 to 4 can be selected by software, starting from 1 ms

# 6 Package information

In order to meet environmental requirements, ST (also) offers these devices in ECOPACK® packages. ECOPACK® packages are lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

**Figure 7. Flexiwatt27 (vertical) mechanical data and package dimensions**





## 7 Revision history

**Table 12. Document revision history**

Date	Revision	Changes
20-Sep-2003	1	Initial release.
01-Jul-2008	2	Document reformatted. Document status promoted from product preview to datasheet.

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