PRELIMINARY

CYU01M16ZFC
MoBL3™

16-Mbit (1M x 16) Pseudo Static RAM

Features

- **Wide voltage range: 1.7V–1.95V**
- **Access Time: 70 ns**
- **Ultra-low active power**
  - **Typical active current: 3 mA @ f = 1 MHz**
  - **Typical active current: 18 mA @ f = f_{max}**
- **Ultra low standby power**
- **16-word Page Mode**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Deep Sleep Mode**
- **Offered in a Lead-Free 48-ball BGA Package**
- **Operating Temperature: –40°C to +85°C**

Functional Description[1]

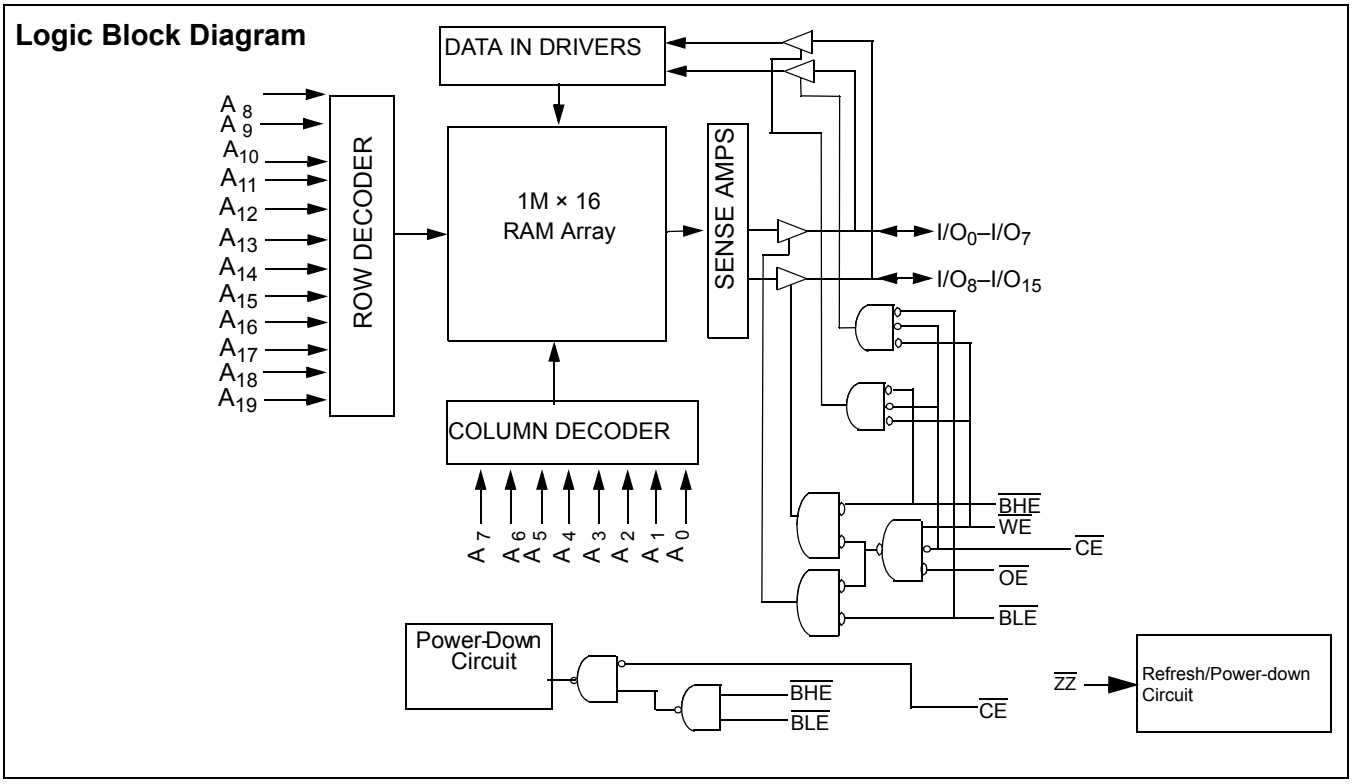
The CYU01M16ZFC is a high-performance CMOS Pseudo Static RAM organized as 1M words by 16 bits that supports an asynchronous memory interface. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device can be put into standby mode when deselected ($\overline{CE}$ HIGH or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH). The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected ($\overline{CE}$ HIGH), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$ LOW) and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{19}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{19}).

Reading from the device is accomplished by taking Chip Enables ($\overline{CE}$ LOW) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. Refer to the truth table for a complete description of read and write modes.

Deep Sleep Mode is enabled by driving $\overline{ZZ}$ LOW. See the Truth Table for a complete description of Read, Write, and Deep Sleep mode.

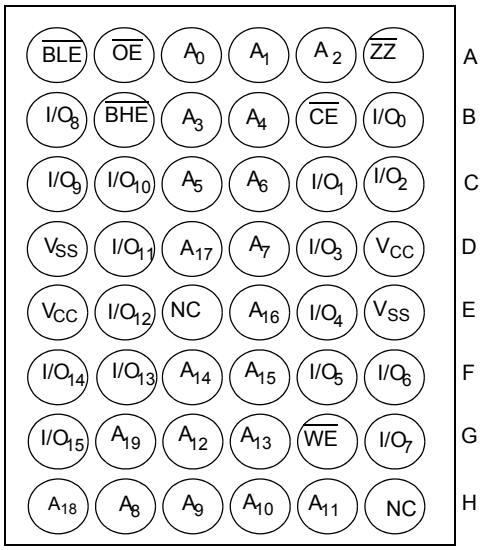
Logic Block Diagram



Note:
1. For best-practice recommendations, please refer to the Cypress application note “System Design Guidelines” on http://www.cypress.com.

Pin Configuration[2, 3]

VFBGA
Top View



Product Portfolio[4]

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
					f = 1MHz		f = f_{max}			
	Min.	Typ.[4]	Max.		Typ.[4]	Max.	Typ.[4]	Max.	Typ.[4]	Max.
CYU01M16ZFC	1.7	1.8	1.95	70	3	5	18	25	55	70

Low-Power Modes

At power-up, all four sections of the die are activated and the PSRAM enters into its default state of full memory size and refresh space. This device provides four different Low-Power Modes.

1. Reduced Memory Size Operation
2. Partial Array Refresh
3. Deep Sleep Mode
4. Temperature Controlled Refresh

Reduced Memory Size Operation

In this mode, the 16 Mb PSRAM can be operated as a 12-Mbit, 8-Mbit or a 4-Mbit memory block. Please refer to “Variable Address Space Register (VAR)” on page 4 for the protocol to turn on/off sections of the memory. The device remains in RMS mode until changes to the Variable Address Space register are made to revert back to a complete 16-Mbit PSRAM.

Partial Array Refresh

The Partial Array Refresh mode allows customers to turn off sections of the memory block in the Stand-by mode (with $\overline{ZZ}$ tied low) to reduce standby current. In this mode the PSRAM will only refresh certain portions of the memory in the Stand-By Mode, as configured by the user through the settings in the Variable Address Register.

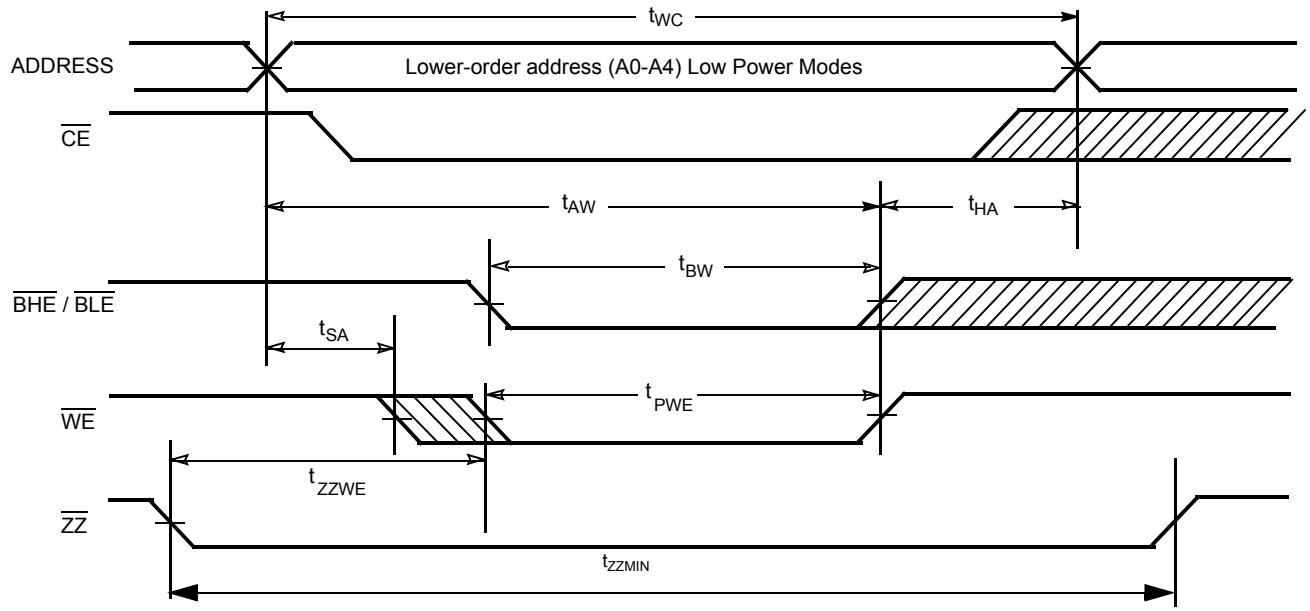
Once $\overline{ZZ}$ returns high in this mode, the PSRAM goes back to operating in full address refresh. Please refer to “Variable Address Space Register (VAR)” on page 4 for the protocol to turn off sections of the memory in Stand-By mode. If the VAR register is not updated after the power up, the PSRAM will be in its default state. In the default state the whole memory array will be refreshed in the Stand-By Mode. The 16-Mbit MoBL3 is divided into four 4-Mbit sections allowing certain sections to be active (i.e., refreshed).

Deep Sleep Mode

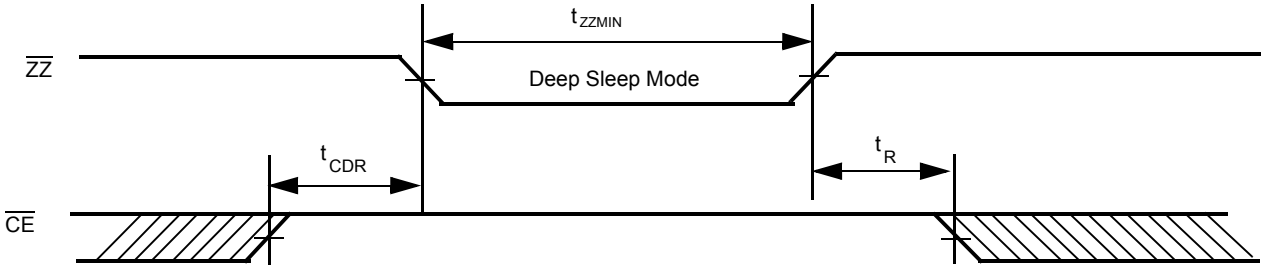
In this mode, the data integrity in the PSRAM is not guaranteed. This mode can be used to lower the power consumption of the PSRAM in an application. This mode can be enabled and disabled through VAR similar to the RMS and PAR mode. Deep Sleep Mode is activated by driving $\overline{ZZ}$ LOW. The device stays in the deep sleep mode until $\overline{ZZ}$ is driven HIGH.

Notes:
2. Ball H6, E3 can be used to upgrade to 32M and 64M density respectively.
3. NC “no connect” - not connected internally to the die.
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25°C$. Tested initially and after any design changes that may affect the parameter.

Variable Address Mode Register (VAR) Update[5, 6]



Deep Sleep Mode—Entry/Exit [7]

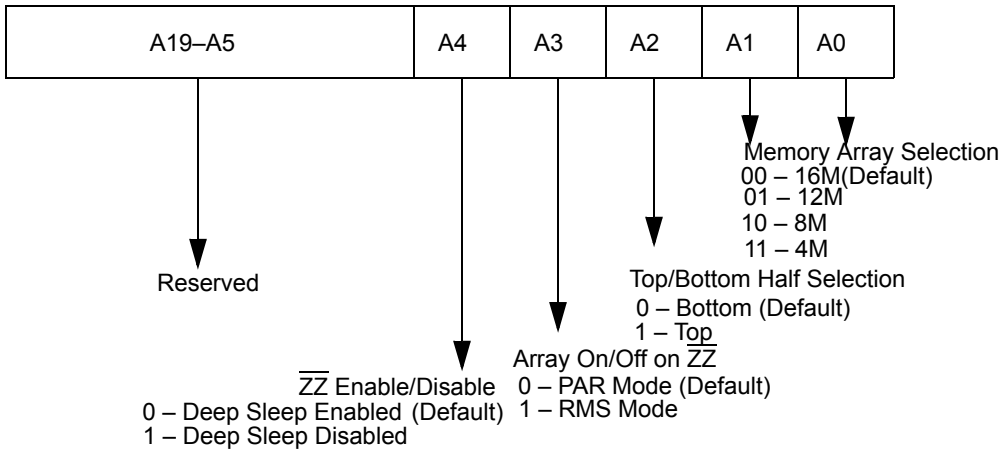


VAR Update and Deep Sleep Mode Timing[5, 6]

Parameter	Description	Min.	Max.	Unit
t_{ZZWE}	$\overline{ZZ}$ LOW to Write Start		1	µs
t_{CDR}	Chip deselect to $\overline{ZZ}$ LOW	0		ns
t_R[7]	Operation Recovery Time (Deep Sleep Mode only)	200		µs
t_{ZZMIN}	Deep Sleep Mode Time	8		µs

Notes:
5. $\overline{OE}$ and the data pins are in a don't care state while the device is in variable address mode.
6. All other timing parameters are as shown in the data sheets.
7. t_R applies only in the deep sleep mode.

Variable Address Space Register (VAR)



Variable Address Space—Address Patterns

Partial Array Refresh Mode (A3 = 0, A4 = 1)					
A2	**A1, A0**	**Refresh Section**	**Address**	**Size**	**Density**
0	1 1	1/4th of the array	00000h - 3FFFFh (A19 = A18 = 0)	256K x 16	4M
0	1 0	1/2th of the array	00000h - 7FFFFh (A19 = 0)	512K x 16	8M
0	0 1	3/4th of the array	00000h - BFFFFh (A19:A18 not equal to 1 1)	768K x 16	12M
1	1 1	1/4th of the array	C0000h - FFFFFh (A19 = A18= 1)	256K x 16	4M
1	1 0	1/2th of the array	80000h - FFFFFh (A19 = 1)	512K x16	8M
1	0 1	3/4th of the array	40000h - FFFFFh (A19:A18 not equal to 0 0)	786K x16	12M
Reduced Memory Size Mode (A3 = 1, A4 = 1)					
0	1 1	1/4th of the array	00000h - 3FFFFh (A19 = A18 = 0)	256K x 16	4M
0	1 0	1/2th of the array	00000h - 7FFFFh (A19 = 0)	512K x 16	8M
0	0 1	3/4th of the array	00000h - BFFFFh (A19:A18 not equal to 1 1)	768K x 16	12M
0	0 0	Full array	00000h - FFFFFh (Default)	1M x 16	16M
1	1 1	1/4th of the array	C0000h - FFFFFh (A19 = A18 = 1)	256K x 16	4M
1	1 0	1/2th of the array	80000h - FFFFFh (A19 = 1)	512K x 16	8M
1	0 1	3/4 h of the array	40000h - FFFFFh (A19:A18 not equal to 0 0)	768K x 16	12M
1	0 0	Full array	00000h - FFFFFh (Default)	1M x 16	16M

Page Mode

This device can be operated in a page read mode. This is accomplished by initiating a normal read of the device.

In order to operate the device in page mode, the upper order address bits should be fixed for four-word page access operation, all address bits except for A1 and A0 should be fixed until the page access is completed. For an eight-word page access, all address bits, except for A2, A1, and A0, should be fixed. For a sixteen-word page mode all address bits, except for A3, A2, A1, and A0, should be fixed.

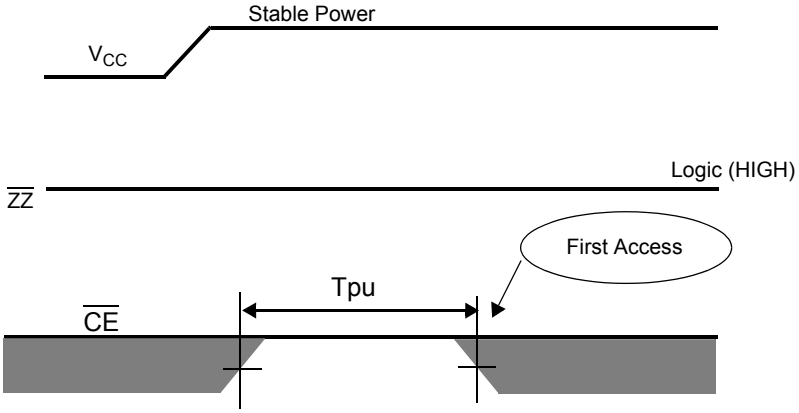
The supported page lengths are four, eight, and sixteen words. Random page read is supported for all three four, eight, and sixteen-word page read options. Therefore, any address can be used as the starting address.

Please, refer to the table below for an overview of the page read modes.

Page Mode Feature	4-Word Mode	8-Word Mode	16-Word Mode
Page Length	4 words	8 words	16 words
Page Read Corresponding Addresses	A1, A0	A2, A1, A0	A3, A2, A1, A0
Page Read Start Address	Don't Care	Don't Care	Don’t Care
Page Direction	Don't Care	Don't Care	Don’t Care

Power-up Characteristics

The initialization sequence is shown in the figure below. Chip Select ($\overline{CE}$) should be HIGH for at least 200 µs after V_{CC} has reached a stable value. No access must be attempted during this period of 200 µs.The state of $\overline{ZZ}$ has to be high (H) for the duration of power-up.



Parameter	Description	Min.	Typ.	Max.	Unit
Tpu	Chip Enable Low After Stable V_{CC}	200			µs

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage to Ground Potential .–0.2V to V_{CCMAX} + 0.3V

DC Voltage Applied to Outputs in High Z State[8, 9, 10] .....–0.2V to V_{CCMAX} + 0.3V

DC Input Voltage[8, 9, 10] .....–0.2V to V_{CCMAX} + 0.3V

Output Current into Outputs (LOW).....20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current.....> 200 mA

Device	Range	Operating Temperature (T_A)	V_{CC}
CYU01M16ZFC	Industrial	–40°C to +85°C	1.7V to 1.95V

DC Electrical Characteristics Over the Operating Range [8, 9, 10]

Parameter	Description	Test Conditions	CYU01M16ZFC-70 Min.	Typ.[4]	Max.	Unit
V_{CC}	Supply Voltage		1.7	1.8	1.95	V
V_{OH}	Output HIGH Voltage	I_{OH} = –0.1 mA, V_{CC}= 1.7V to 1.95V	V_{CC} – 0.2			V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA, V_{CC}= 1.7V to 1.95V			0.2	V
V_{IH}	Input HIGH Voltage	1.7V ≤ V_{CC} ≤ 1.95	0.8 * V_{CC}		V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage	V_{CC}= 1.7V to 1.95V	–0.2		0.2 * V_{CC}	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}	–1		+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}	–1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	f = f_{MAX} = $1/t_{RC}$; V_{CC}= V_{CCmax}, I_{OUT} = 0 mA, CMOS levels		18	25	mA
		f = 1 MHz		3	5	mA
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current — CMOS Inputs	$\overline{CE}$ > V_{CC} – 0.2V, V_I > V_{CC} – 0.2V, V_{IN} < 0.2V, f = f_{MAX} (Address and Data Only), f = 0 ($\overline{OE}$, $\overline{WE}$, $\overline{BHE}$ and $\overline{BLE}$), V_{CC} = 1.95V, $\overline{ZZ}$ >= V_{CC} – 0.2V		55	70	µA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current — CMOS Inputs	$\overline{CE}$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0, V_{CC} = V_{CCMAX}, $\overline{ZZ}$>= V_{CC} – 0.2V		55	70	µA
I_{ZZ}	Deep Sleep Current	V_{CC} = V_{CCMAX}, $\overline{ZZ}$ ≤ 0.2V, $\overline{CE}$ = HIGH or $\overline{BHE}$ and $\overline{BLE}$ = HIGH			10	µA

Capacitance[11]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	8	pF
C_{OUT}	Output Capacitance		8	pF

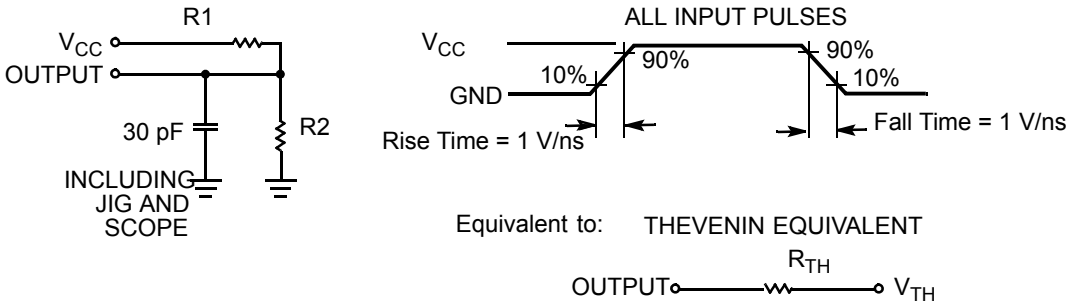
Notes:

8. $V_{IL(MIN)}$ = –0.5V for pulse durations less than 20 ns.
9. $V_{IH(Max)}$ = V_{CC} + 0.5V for pulse durations less than 20 ns.
10. Overshoot and undershoot specifications are characterized and are not 100% tested.
11. Tested initially and after any design or process changes that may affect these parameters.

Thermal Resistance[11]

Parameter	Description	Test Conditions	VFBGA	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedence, per EIA / JESD51.	56	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		11	°C/W

AC Test Loads and Waveforms



Parameters	1.8V (V_{CC})	Unit
R1	14000	Ω
R2	14000	Ω
R_{TH}	7000	Ω
V_{TH}	0.90	V

Switching Characteristics Over the Operating Range[12, 13, 14, 15, 18]

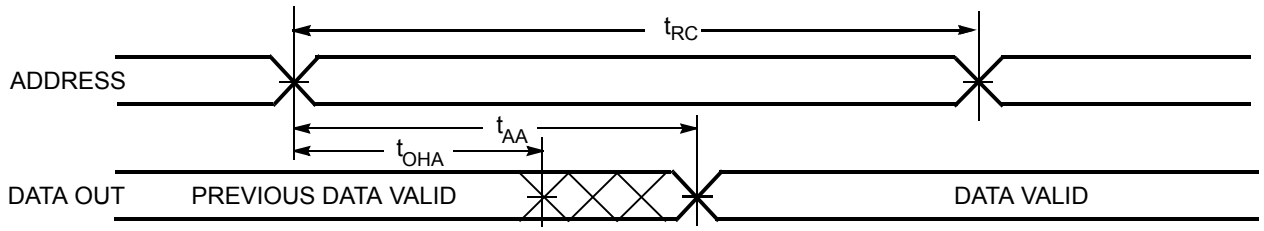
Parameter	Description	70 ns		Unit
		Min.	Max.	
Read Cycle				
t_{RC} [17]	Read Cycle Time	70	40000	ns
t_{CD}	Chip Deselect Time CE, BLE/BHE High Pulse Time	15		ns
t_{AA}	Address to Data Valid		70	ns
t_{OHA}	Data Hold from Address Change	5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[13, 14, 16]	5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[13, 14, 16]		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[13, 14, 16]	10		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[13, 14, 16]		25	ns
t_{DBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to Data Valid		70	ns
t_{LZBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to Low Z[13, 14, 16]	5		ns
t_{HZBE}	$\overline{BLE}$/$\overline{BHE}$ HIGH to High Z[13, 14, 16]		25	ns
Page Read Cycle				
t_{PC}	Page Mode Read Cycle Time	35	40000	ns
t_{PA}	Page Mode Address Access		35	ns
Write Cycle[15]				
t_{WC}	Write Cycle Time	70	40000	ns
t_{SCE}	$\overline{CE}$ LOW to Write End	60		ns
t_{CD}	Chip Deselect Time CE, BLE/BHE High Pulse Time	15		ns
t_{AW}	Address Set-Up to Write End	60		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Set-Up to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	50		ns
t_{BW}	$\overline{BLE}$/$\overline{BHE}$ LOW to Write End	60		ns
t_{SD}	Data Set-Up to Write End	25		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[13, 14, 16]		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[13, 14, 16]	10		ns

Notes:

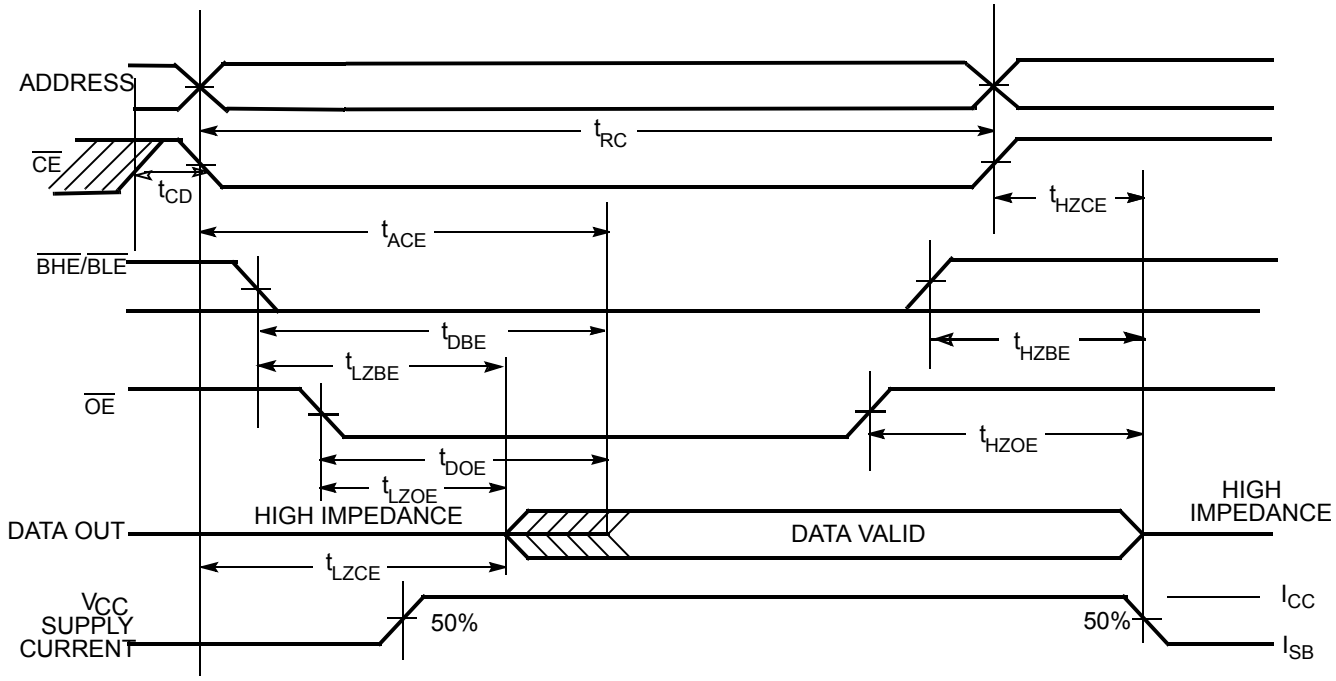
12. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 ns/V, timing reference levels of $V_{CC}/2$, input pulse levels of 0V to V_{CC}, and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" section.
13. At any given temperature and voltage conditions t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than $t_{LZWE}$for any given device. All low-Z parameters will be measured with a load capacitance of 30 pF (1.8V)
14. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
15. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.
16. High-Z and Low-Z parameters are characterized and are not 100% tested.
17. If invalid address signals shorter than min. t_{RC} are continuously repeated for 40 µs, the device needs a normal read timing (t_{RC}) or needs to enter standby state at least once in every 40 µs.
18. In order to achieve 70ns performance, the read access must be $\overline{CE}$ controlled. That is, the addresses must be stable prior to $\overline{CE}$ going active.

Switching Waveforms

Read Cycle 1 (Address Transition Controlled)[20, 21]



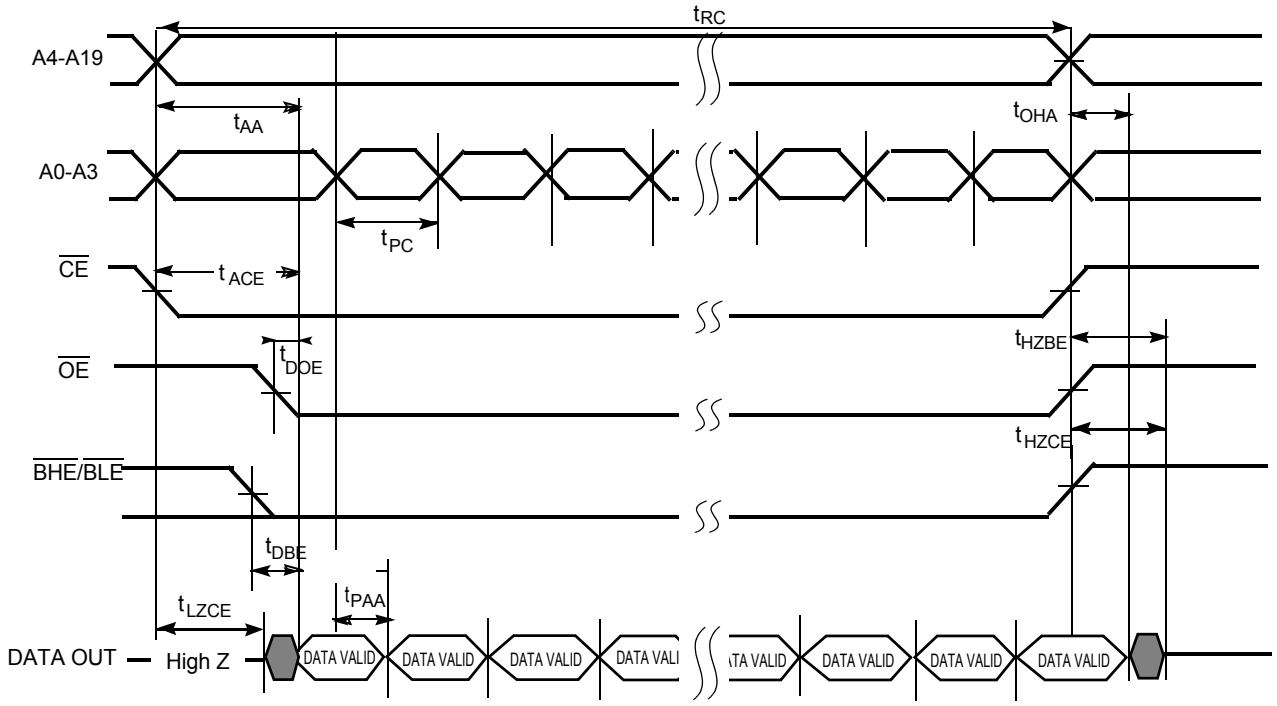
Read Cycle 2 (OE Controlled)[19, 21]



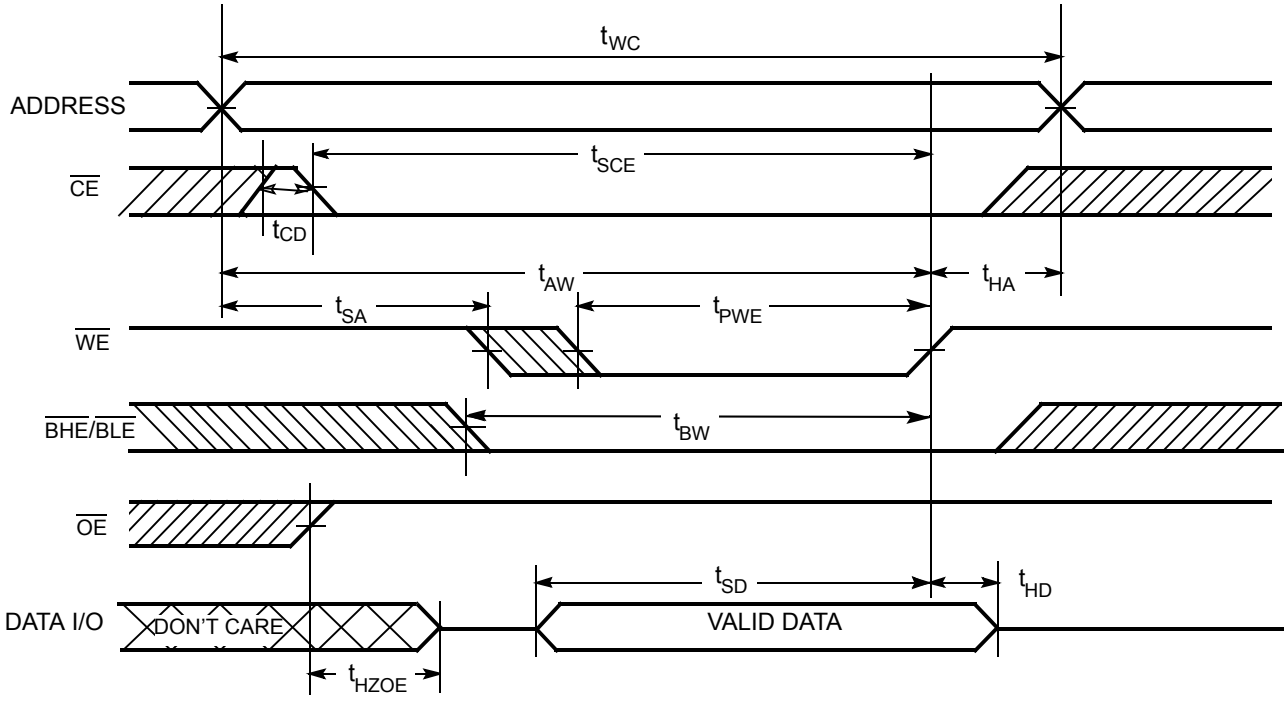
Notes:
19. Whenever CE, BHE/BLE are taken inactive, they must remain inactive for a minimum of 15 ns
20. Device is continuously selected. OE, CE = V_{IL}.
21. WE is HIGH for Read Cycle.

Switching Waveforms (continued)

Page Read Cycle ($\overline{ZZ}$ = $\overline{WE}$ = V_{IH}, 16 word access)[17, 21]



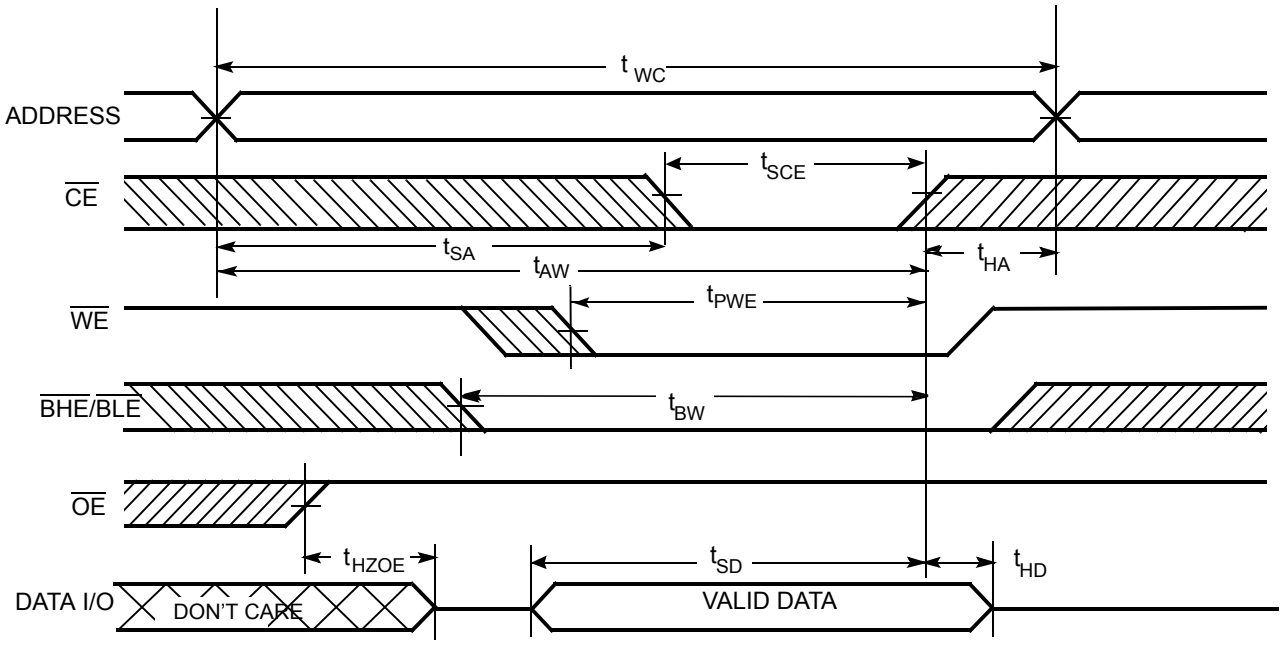
Write Cycle 1 ($\overline{WE}$ Controlled)[15, 16, 19, 22, 23]



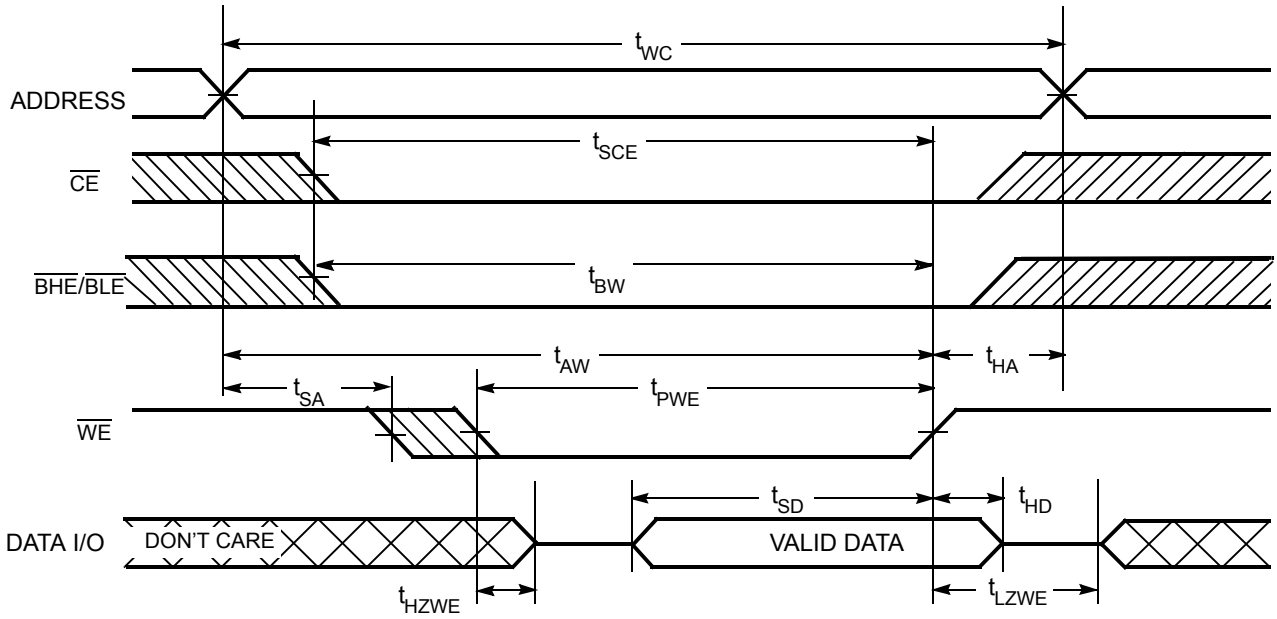
Notes:
22. Data I/O is high-impedance if $\overline{OE} \geq V_{IH}$.
23. During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle 2 ($\overline{CE}$ Controlled)[15, 16, 19, 22, 23]

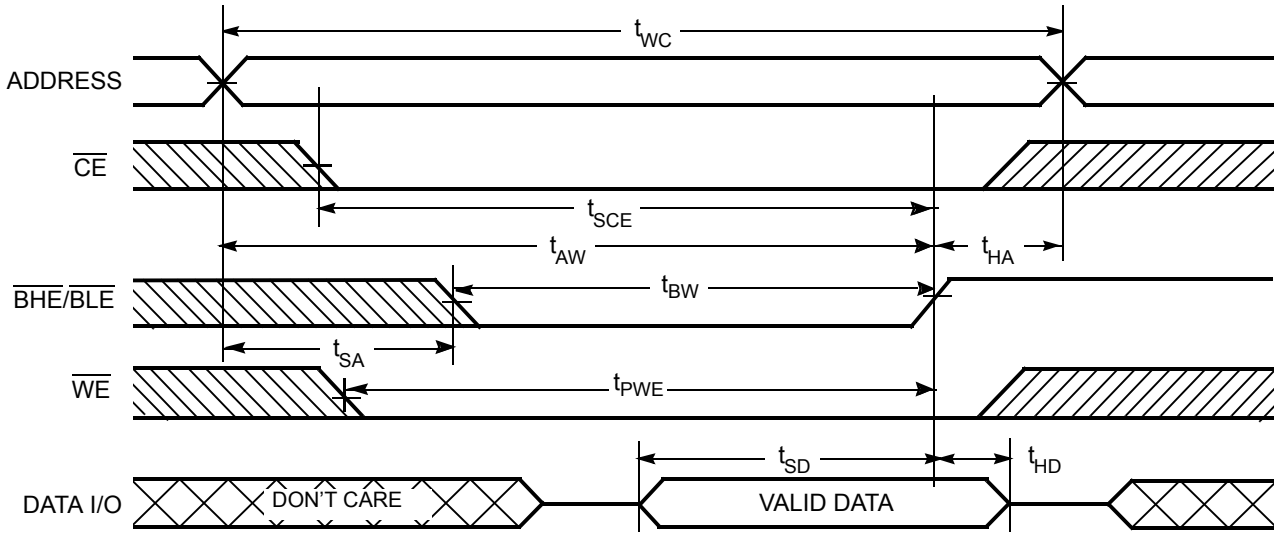


Write Cycle 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[19, 23]



Switching Waveforms (continued)

Write Cycle 4 (BHE/BLE Controlled, OE LOW)[15, 19, 22, 23]



Truth Table[24, 25]

ZZ	CE	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
H	H	X	X	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
H	X	X	X	H	H	High Z	Deselect/Power-down	Standby (I_{SB})
H	L	X	X	H	H	High Z	Deselect/Power-down	Standby (I_{SB})
H	L	H	L	L	L	Data Out (I/O_0–I/O_{15})	Read	Active (I_{CC})
H	L	H	L	H	L	Data Out (I/O_0–I/O_7); I/O_8–I/O_{15} in High Z	Read	Active (I_{CC})
H	L	H	L	L	H	Data Out (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Read	Active (I_{CC})
H	L	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
H	L	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
H	L	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
H	L	L	X	L	L	Data In (I/O_0–I/O_{15})	Write (Upper Byte and Lower Byte)	Active (I_{CC})
H	L	L	X	H	L	Data In (I/O_0–I/O_7); I/O_8–I/O_{15} in High Z	Write (Lower Byte Only)	Active (I_{CC})
H	L	L	X	L	H	Data In (I/O_8–I/O_{15}); I/O_0 –I/O_7 in High Z	Write (Upper Byte Only)	Active (I_{CC})
L	H	X	X	H	H	Data in (A_0–A_4)	Write (Variable Address Mode Register)	Active (I_{CC})
L	H	X	X	X	X	High Z	Deep Power-down / PAR	Deep Sleep (I_{ZZ}) / Stand by

Notes:
24. H = Logic HIGH, L = Logic LOW, X = Don't Care.
25. During ZZ = L and CE = H, Mode depends on how the VAR is set up either in PAR or Deep Sleep Modes.

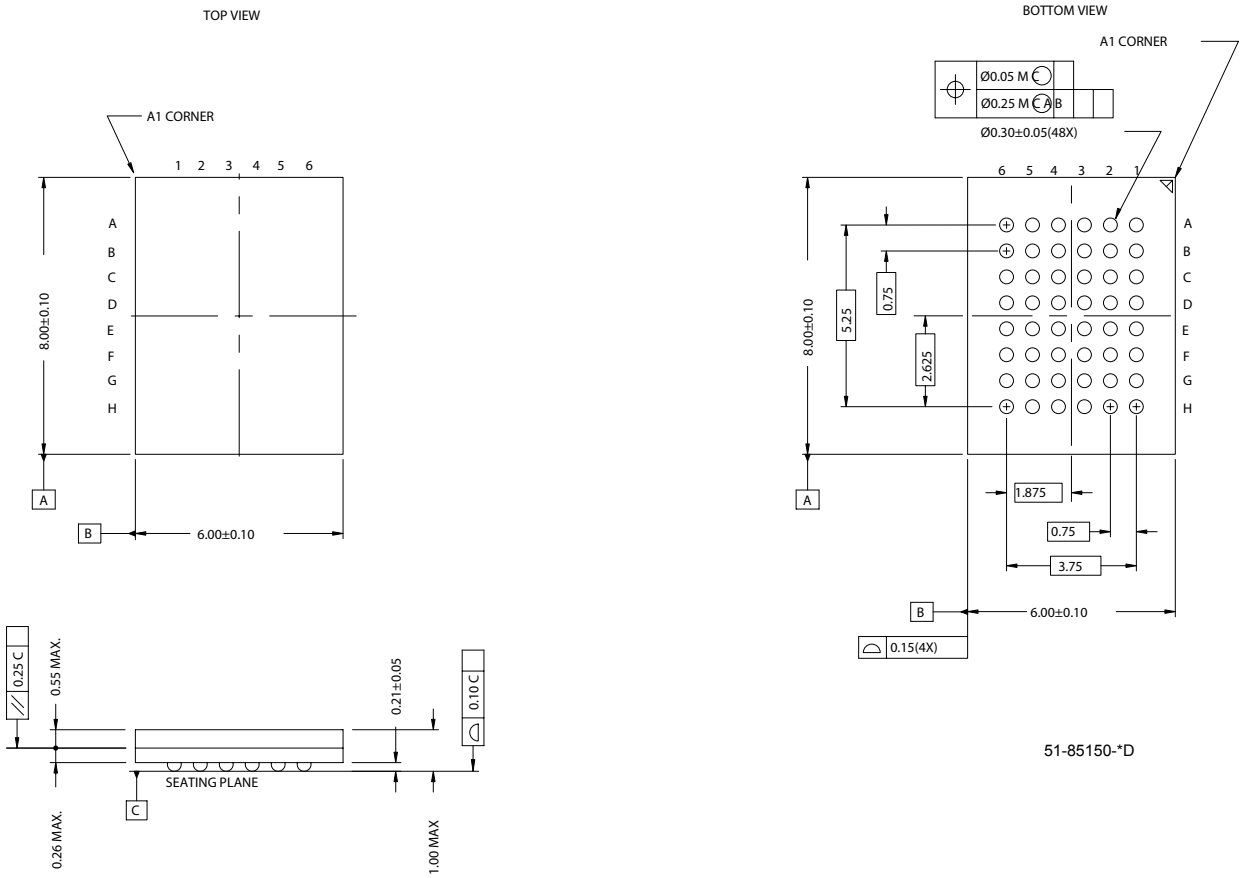
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CYU01M16ZFCU-70BVXI	BV48	48-ball Fine Pitch VFBGA (6 mm × 8 mm × 1 mm) Lead-Free	Industrial

Please contact your local Cypress Sales representative for availability of other parts.

Package Diagram

48-Lead VFBGA (6 x 8 x 1 mm) BV48



Document History Page

Document Title: CYU01M16ZFC MoBL3™ 16-Mbit (1M x 16) Pseudo Static RAM Document Number: 38-05604				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	278869	See ECN	SYT	New Data Sheet
*A	280850	See ECN	REF	Updated Ordering information to incorporate lead-free parts.
*B	314034	See ECN	PCI	Corrected Part Number Added Operating Range in Features Section Moved address lines A8 - A10 from Column decoder to Row decoder in the Logic Block Diagram Changed Pin Configuration Diagram Name from FBGA to VFBGA Added pin E3 in note #2 Modified description on Deep Sleep Mode Changed t_{ZZWE} description Changed Θ_{JA} and Θ_{JC} from 55 and 17 °C/W to 56 and 11°C/W respectively Modified Test Condition for I_{IX} and I_{OZ} Changed $V_{CC(typ)}$ to V_{CC} in note # 12 Changed t_{OHA} from 10 ns to 5 ns Changed t_{SCE}, t_{AW} and t_{BW} from 45 to 50 ns Changed t_{RC} and t_{WC} from 6000 ns to 40000 ns Changed t_{PC} and t_{PA} from 15 ns to 20 ns Added Parameter t_{CD} in AC Table and its corresponding footnote in Notes Section Changed R1 and R2 from 13500 and 10800 Ω to 14000 Ω Changed R_{TH} from 6000 to 7000 Ω Parameter t_{CD} added in Read Cycle 2 and Write Cycle 1 Timing Diagrams Changed from Advance Information to Preliminary
*C	351780	See ECN	PCI	Modified Logic Block Diagram Modified description on Deep Sleep Mode Deleted Page Write in the Page Mode Feature Table Added $\overline{CE}$, $\overline{BHE}$ and $\overline{BLE}$ in test conditions for I_{ZZ} in DC Table Modified condition in the third row of the Truth Table for $\overline{ZZ}$ Pin from X to H
*D	386551	See ECN	PCI	Changed t_{PC} and t_{PA} from 20 to 25 ns Replaced TBDs with appropriate values
*E	406266	See ECN	NXR	Changed address of Cypress Semiconductor Corporation on Page# 1 from “3901 North First Street” to “198 Champion Court” Removed 55 ns Speed Bin. Removed Reference to $\overline{BHE}$/ $\overline{BLE}$ from DPD wave form on page # 3. Added $\overline{ZZ}$ in Power Up characteristics on page# 5. Added I_{SB1} specification in the DC characteristics table on page #6. Added test condition $\overline{ZZ}$>= V_{CC}-0.2V for ISB2 Updated the Truth Table for DPD / PAR and Write (Variable Address Mode Register) Modes.
*F	420604	See ECN	HRT	Changed T_{CD} value to 15 ns from 5 ns on Read and Write Cycles Changed T_{PC} and T_{PAA} values to 35 ns from 25 ns Included “Chip Enable Access” footnote in AC Parameters Changed Isb2 value from 60µA to 70µA