

# RQK2001HQDQA

Silicon N Channel MOS FET  
Power Switching

REJ03G1731-0100

Rev.1.00

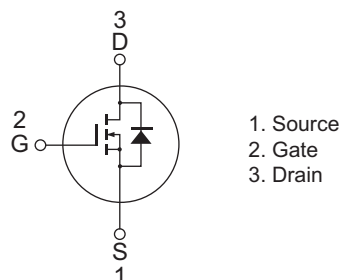
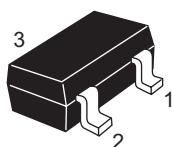
Sep 01, 2008

## Features

- High drain to source voltage and Low gate drive  
 $V_{DSS} : 200\text{ V}$  and  $V_{GSS} : \pm 30\text{ V}$
- Low drive current
- High speed switching
- Small traditional package (MPAK)

## Outline

RENESAS Package code: PLSP0003ZB-A  
(Package name: MPAK)



Note: Marking is "HQ".

## Absolute Maximum Ratings

( $T_a = 25^\circ\text{C}$ )

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	200	V
Gate to source voltage	$V_{GSS}$	$\pm 30$	V
Drain current	$I_D$	0.4	A
Drain peak current	$I_{D(pulse)}$ <sup>Note1</sup>	1.6	A
Body - drain diode reverse drain current	$I_{DR}$	0.4	A
Channel dissipation	$P_{ch}$ <sup>Note2</sup>	0.8	W
Thermal resistance	$R_{th(ch-a)}$ <sup>Note2</sup>	156	$^\circ\text{C} / \text{W}$
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

Notes: 1.  $PW \leq 10\text{ }\mu\text{s}$ , Duty cycle  $\leq 1\%$

2. When using the glass epoxy board (FR-4  $40 \times 40 \times 1\text{ mm}$ )

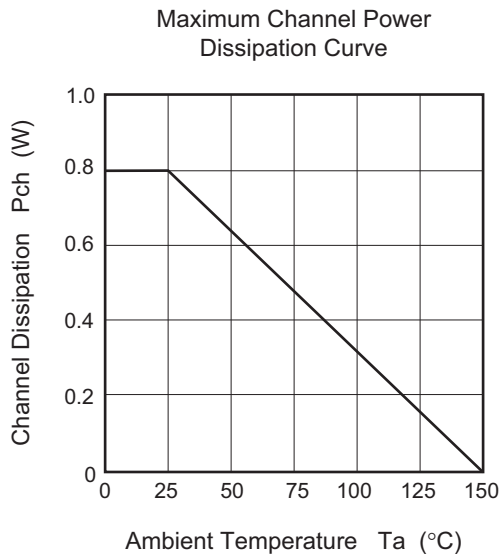
## Electrical Characteristics

(Ta = 25°C)

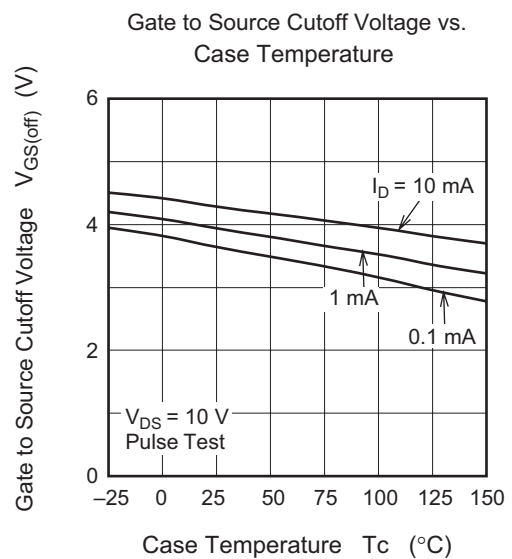
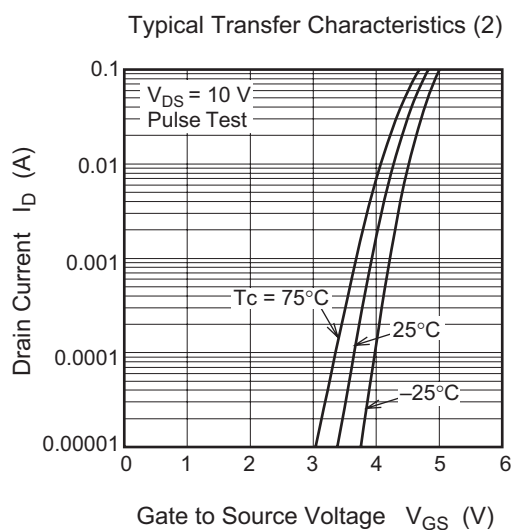
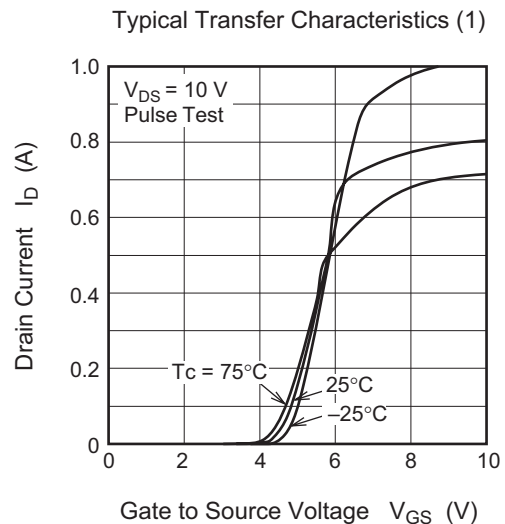
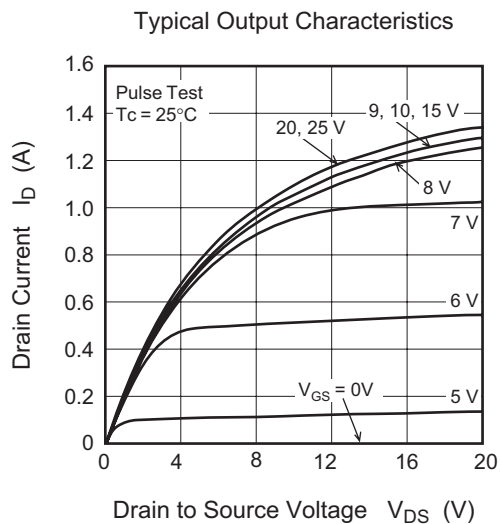
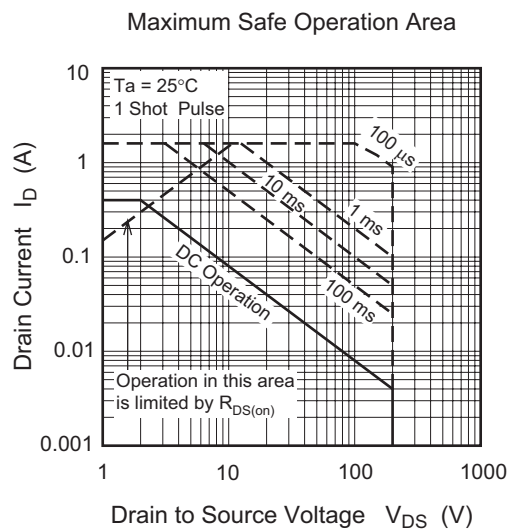
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	200	—	—	V	$I_D = 10 \text{ mA}$ , $V_{GS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	+0.1	$\mu\text{A}$	$V_{GS} = +30 \text{ V}$ , $V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	-0.1	$\mu\text{A}$	$V_{GS} = -30 \text{ V}$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	1	$\mu\text{A}$	$V_{DS} = 200 \text{ V}$ , $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	3	—	4.5	V	$V_{DS} = 10 \text{ V}$ , $I_D = 1 \text{ mA}$
Drain to source on state resistance	$R_{DS(on)}$	—	5.0	6.7	$\Omega$	$I_D = 0.15 \text{ A}$ , $V_{GS} = 10 \text{ V}$ <sup>Note3</sup>
Forward transfer admittance	$ y_{fs} $	0.2	0.3	—	S	$I_D = 0.15 \text{ A}$ , $V_{DS} = 10 \text{ V}$ <sup>Note3</sup>
Input capacitance	$C_{iss}$	—	30	—	pF	$V_{DS} = 25 \text{ V}$ $V_{GS} = 0$ $f = 1 \text{ MHz}$
Output capacitance	$C_{oss}$	—	5	—	pF	
Reverse transfer capacitance	$C_{rss}$	—	2	—	pF	
Turn - on delay time	$t_{d(on)}$	—	13	—	ns	$I_D = 0.15 \text{ A}$ $V_{GS} = 10 \text{ V}$ $R_L = 667 \Omega$ $R_g = 50 \Omega$
Rise time	$t_r$	—	12	—	ns	
Turn - off delay time	$t_{d(off)}$	—	42	—	ns	
Fall time	$t_f$	—	38	—	ns	
Total gate charge	$Q_g$	—	1.8	—	nC	$V_{DD} = 100 \text{ V}$ $V_{GS} = 10 \text{ V}$ $I_D = 0.4 \text{ A}$
Gate to Source charge	$Q_{gs}$	—	0.4	—	nC	
Gate to drain charge	$Q_{gd}$	—	0.9	—	nC	
Body - drain diode forward voltage	$V_{DF}$	—	0.8	1.2	V	$I_F = 0.4 \text{ A}$ , $V_{GS} = 0$ <sup>Note3</sup>

Notes: 3. Pulse test

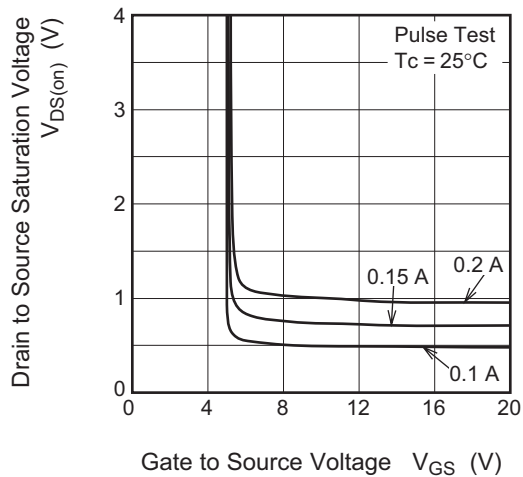
## Main Characteristics



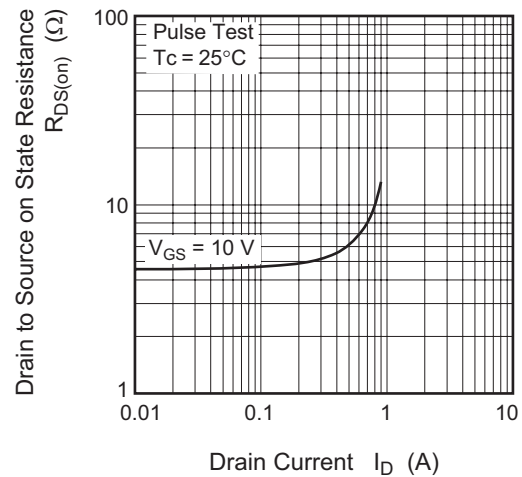
\*When using the glass epoxy board (FR-4 40 x 40 x 1 mm)



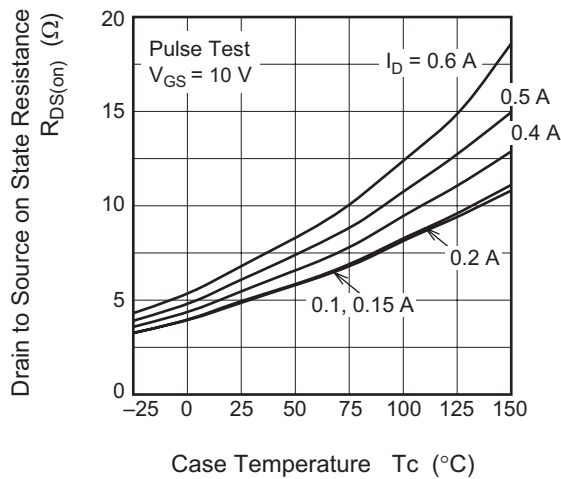
Drain to Source Saturation Voltage vs.  
Gate to Source Voltage



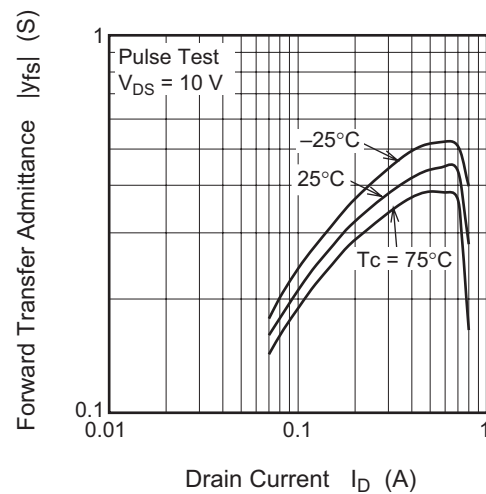
Static Drain to Source on State Resistance  
vs. Drain Current



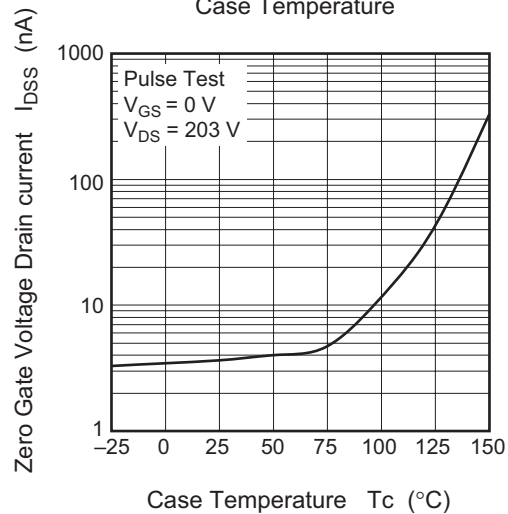
Static Drain to Source on State Resistance  
vs. Case Temperature (1)



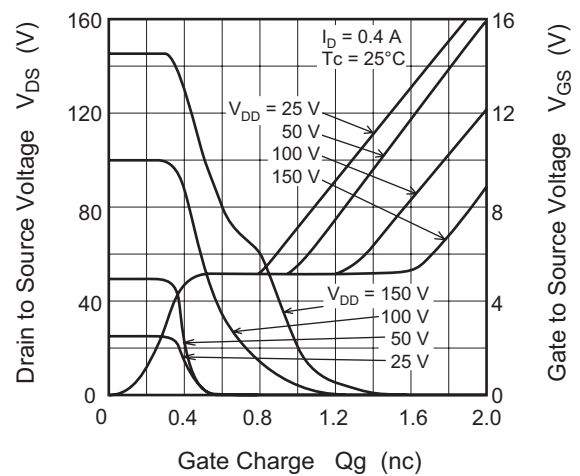
Forward Transfer Admittance vs.  
Drain Current



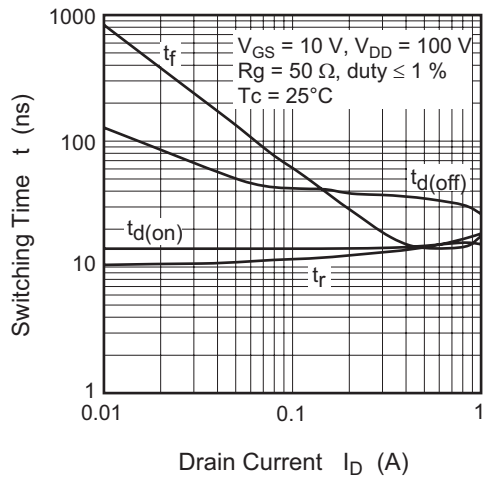
Zero Gate Voltage Drain current vs.  
Case Temperature



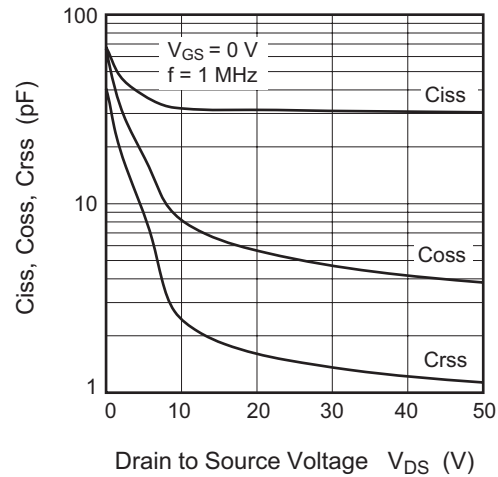
Dynamic Input Characteristics



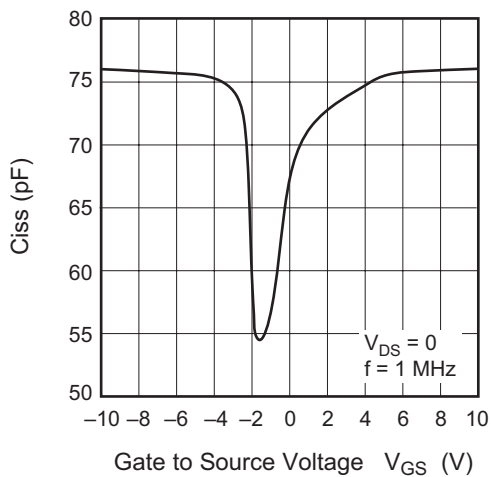
Switching Characteristics



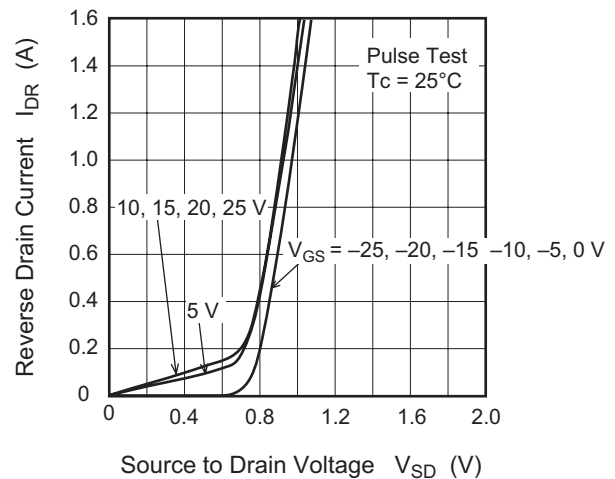
Typical Capacitance vs. Drain to Source Voltage



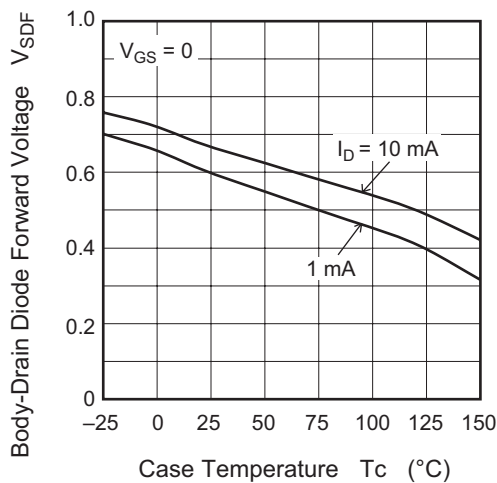
Input Capacitance vs. Gate to Source Voltage



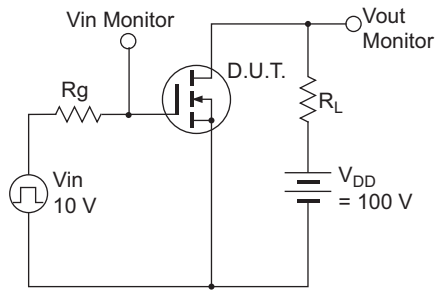
Reverse Drain Current vs. Source to Drain Voltage



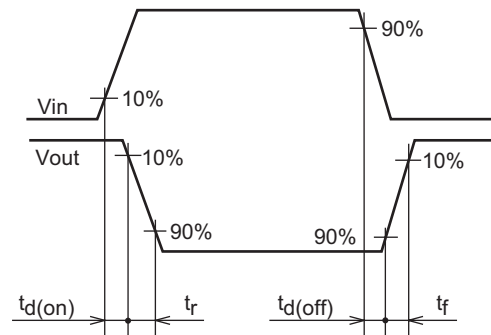
Body-Drain Diode Forward Voltage vs. Case Temperature



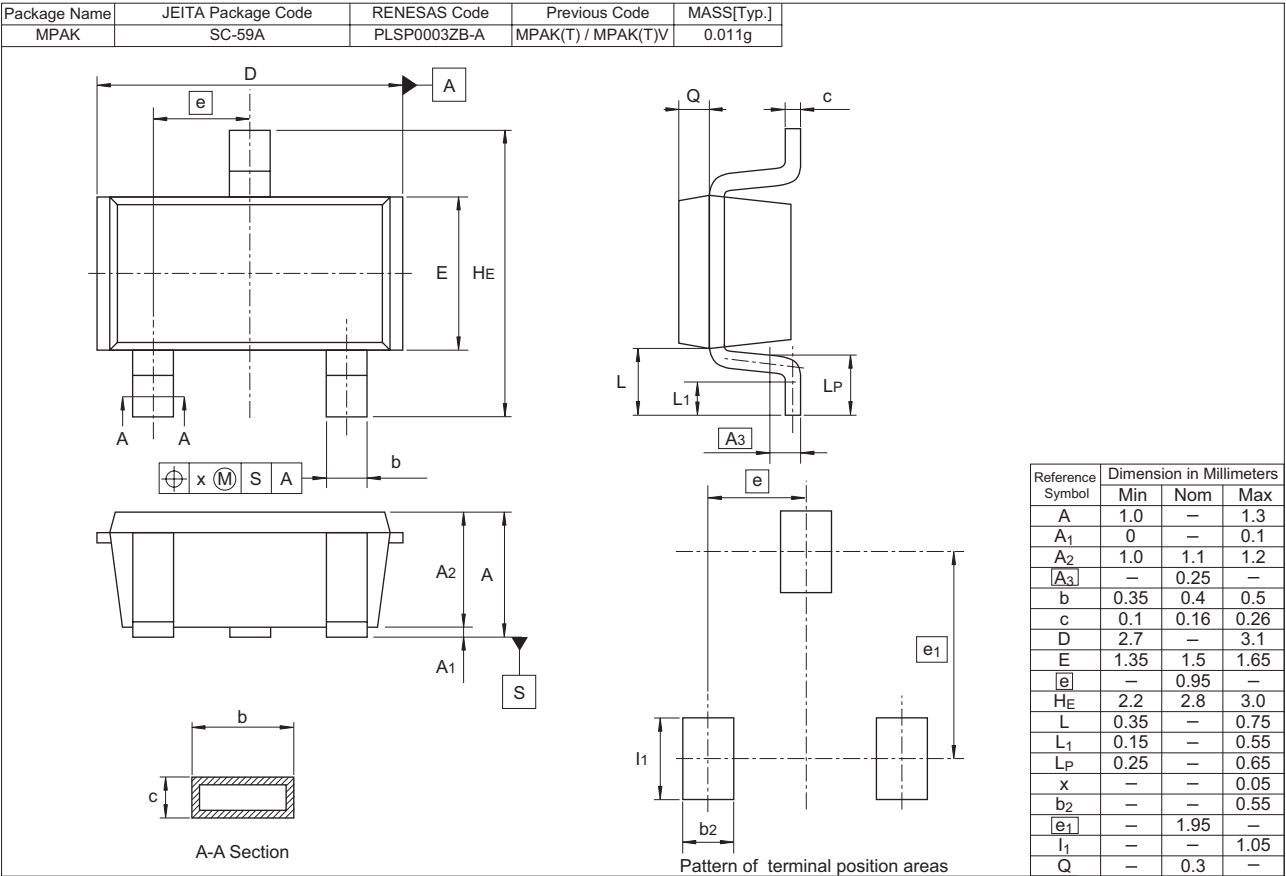
Switching Time Test Circuit



Switching Time Waveform



Package Dimensions



Ordering Information

Part No.	Quantity	Shipping Container
RQK2001HQDQATL-E	3000 pcs.	φ178 mm reel, 8 mm Emboss taping

Notes:

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