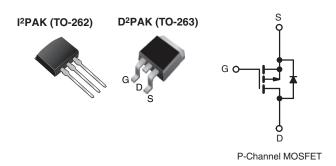


Power MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	- 60			
$R_{DS(on)}\left(\Omega\right)$	V _{GS} = - 10 V 0.50			
Q _g (Max.) (nC)	12			
Q _{gs} (nC)	3.8			
Q _{gd} (nC)	5.1			
Configuration	Single			



FEATURES

- Advanced Process Technology
- Surface Mount (IRF9Z14S/SiHF9Z14S)



• 175 °C Operating Temperature

Z14L) RoHS* COMPLIANT

- · Fast Switching
- P-Channel
- · Fully Avalanche Rated
- Lead (Pb)-free Available

DESCRIPTION

Third generation Power MOSFETs from Vishay utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D²PAK is a surface mount power package capable of accommodating die size up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²PAK is suitable for high current applications because of is low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

The through-hole version (IRF9Z14L/SiHF9Z14L) is available for low-profile applications.

ORDERING INFORMATION				
Package	D ² PAK (TO-263)	D ² PAK (TO-263)	I ² PAK (TO-262)	
Lead (Pb)-free	IRF9Z14SPbF	IRF9Z14STRLPbFa	IRF9Z14LPbF	
	SiHF9Z14S-E3	SiHF9Z14STL-E3 ^a	SiHF9Z14L-E3	
SnPb	IRF9Z14S	IRF9Z14STRL ^a	-	
	SiHF9Z14S	SiHF9Z14STL ^a	-	

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS $T_C = 25 ^{\circ}C$, unless otherwise noted						
PARAMETER	SYMBOL	LIMIT	UNIT			
Drain-Source Voltage		V_{DS}	- 60	.,		
Gate-Source Voltage	V_{GS}	± 20	V			
Continuous Drain Currente	V_{GS} at - 10 V $T_{C} = 25 ^{\circ}\text{C}$ $T_{C} = 100 ^{\circ}\text{C}$	I _D	- 6.7			
	V_{GS} at - 10 V_{C} $T_{C} = 100 ^{\circ}C$		- 4.7	Α		
Pulsed Drain Current ^{a, e}	I _{DM}	- 27				
Linear Derating Factor		0.29	W/°C			
Single Pulse Avalanche Energy ^{b, e}	E _{AS}	140	mJ			
Avalanche Current ^a	I _{AR}	- 6.7	Α			
Repetiitive Avalanche Energy ^a	E _{AR}	4.3	mJ			
Maximum Power Dissipation	T _C = 25 °C	P _D	3.7	W		
	T _A = 25 °C		43	l vv		

^{*} Pb containing terminations are not RoHS compliant, exemptions may apply

IRF9Z14S, SiHF9Z14S, IRF9Z14L, SiHF9Z14L

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ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted					
PARAMETER	SYMBOL	LIMIT	UNIT		
Peak Diode Recovery dV/dtc, e	dV/dt	- 4.5	V/ns		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to + 175	°C	
Soldering Recommendations (Peak Temperature)	for 10 s		300 ^d	C	

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11). b. $V_{DD} = -25$ V, starting $T_J = 25$ °C, L = 3.6 mH, $R_G = 25$ Ω , $I_{AS} = -6.7$ A (see fig. 12). c. $I_{SD} \le -6.7$ A, $I_{AS} = -6.7$ A, $I_{AS} = -6.7$ A (see fig. 12). d. $I_{AS} = -6.7$ A, $I_{AS} = -6.7$ A (see fig. 12).

- e. Uses IRF9Z14/SiHF9Z14 data and test conditions.

THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	TYP.	MAX.	UNIT		
Maximum Junction-to-Ambient (PCB Mounted, steady-state) ^a	R _{thJA}	-	40	°C/W		
Maximum Junction-to-Case (Drain)	R _{thJC}	-	3.5			

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS $T_J = 25 ^{\circ}C$,	unless other	wise noted					
PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT	
Static						l.	
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} =	0 V, I _D = - 250 μA	- 60	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference	e to 25 °C, I _D = - 1 mA ^c	-	- 0.06	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} =	V _{GS} , I _D = - 250 μA	- 2.0	-	- 4.0	V
Gate-Source Leakage	I _{GSS}	,	V _{GS} = ± 20 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =	- 60 V, V _{GS} = 0 V	-	-	- 100	μΑ
	.033	V _{DS} = - 48 V	, V _{GS} = 0 V, T _J = 150 °C	-	-	- 500	,
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = - 10 V	I _D = - 4.0 A ^b	-	-	0.5	Ω
Forward Transconductance	9 _{fs}	V _{DS} =	- 25 V, I _D = - 4.0 A ^c	1.4	-	-	S
Dynamic							
Input Capacitance	C_{iss}	V _{GS} = 0 V,		-	270	-	pF
Output Capacitance	C _{oss}		$V_{DS} = -25 \text{ V},$ $f = 1.0 \text{ MHz}, \text{ see fig. } 5^{\circ}$		170	-	
Reverse Transfer Capacitance	C _{rss}	t = 1.			31	-	
Total Gate Charge	Qg			-	-	12	
Gate-Source Charge	Q _{gs}	V _{GS} = - 10 V	$I_D = -6.7 \text{ A}, V_{DS} = -48 \text{ V},$ see fig. 6 and 13 ^{b, c}	-	-	3.8	nC
Gate-Drain Charge	Q _{gd}]	ground to	-	-	5.1	
Turn-On Delay Time	t _{d(on)}				11	-	
Rise Time	t _r	V _{DD} =	- 30 V. In = - 6.7 A.	-	63	-	no
Turn-Off Delay Time	t _{d(off)}	00	$R_{\rm G} = 24 \Omega$, $R_{\rm D} = 4.0 \Omega$, see fig. $10^{\rm b}$		10	-	ns
Fall Time	t _f]			31	-	
Internal Source Inductance	L _S	Between lead, and center of die contact		-	7.5	-	nΗ
Drain-Source Body Diode Characteristic	s						
Continuous Source-Drain Diode Current	I _S	MOSFET sym showing the	MOSFET symbol showing the		-	- 6.7	A
Pulsed Diode Forward Current ^a	I _{SM}	integral reverse p - n junction diode		-	-	- 27	
Body Diode Voltage	V _{SD}	T _J = 25 °C,	$I_S = -6.7 \text{ A}, V_{GS} = 0 \text{ V}^b$	-	-	- 5.5	V

SPECIFICATIONS T _J = 25 °C, unless otherwise noted						
PARAMETER	SYMBOL	SYMBOL TEST CONDITIONS			MAX.	UNIT
Drain-Source Body Diode Characteristics						
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = - 6.7 A, dI/dt = 100 A/μs ^{b, c}	-	80	160	ns
Body Diode Reverse Recovery Charge	Q _{rr}	$f(1) = 25$ C, $f_F = -6.7$ A, $f(1) = 100$ A/ $f(1) = 100$	-	96	190	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				_D)

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width \leq 300 μ s; duty cycle \leq 2 %.
- c. Uses IRF9Z14/SiHF9Z14 data and test conditions.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

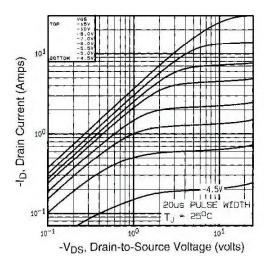


Fig. 1 - Typical Output Characteristics

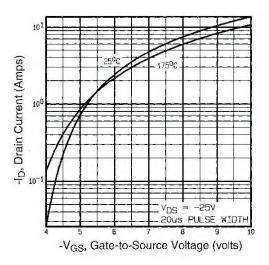


Fig. 3 - Typical Transfer Characteristics

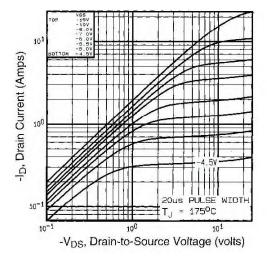


Fig. 2 - Typical Output Characteristics

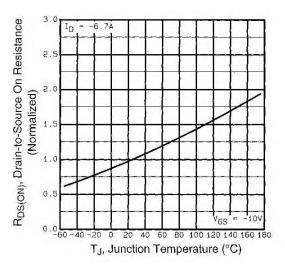


Fig. 4 - Normalized On-Resistance vs. Temperature

IRF9Z14S, SiHF9Z14S, IRF9Z14L, SiHF9Z14L

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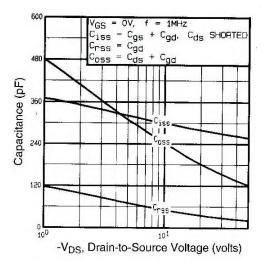


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

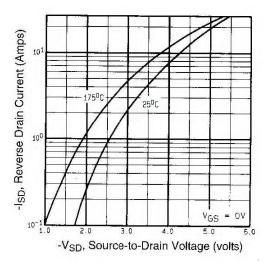


Fig. 7 - Typical Source-Drain Diode Forward Voltage

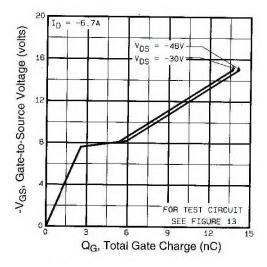


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

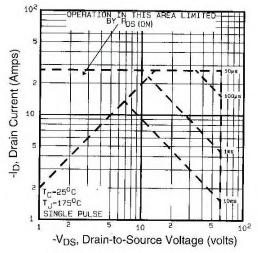


Fig. 8 - Maximum Safe Operating Area



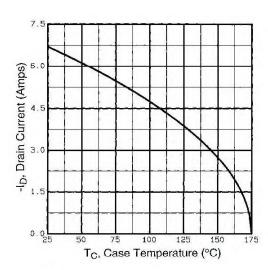


Fig. 9 - Maximum Drain Current vs. Case Temperature

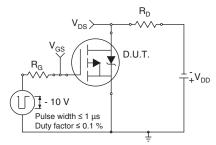


Fig. 10a - Switching Time Test Circuit

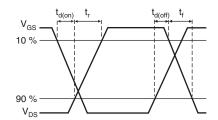


Fig. 10b - Switching Time Waveforms

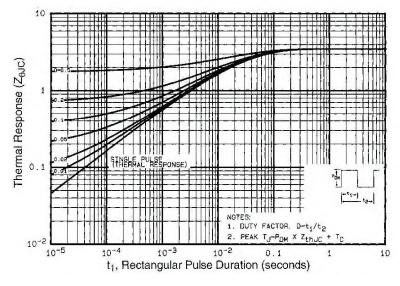


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

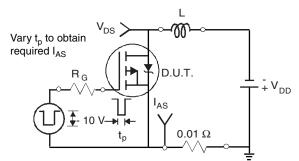


Fig. 12a - Unclamped Inductive Test Circuit

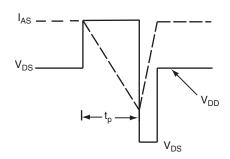


Fig. 12b - Unclamped Inductive Waveforms



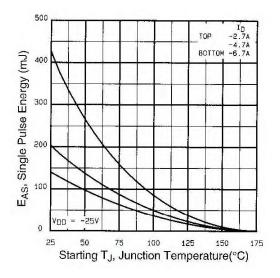


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

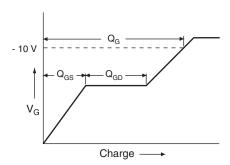


Fig. 13a - Basic Gate Charge Waveform

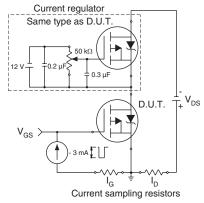
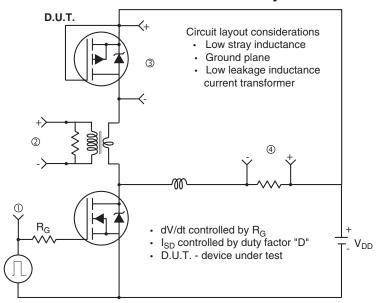
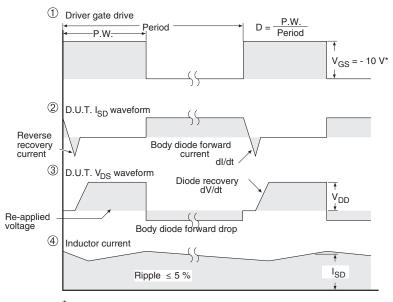


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



• Compliment N-Channel of D.U.T. for driver



* V_{GS} = - 5 V for logic level and - 3 V drive devices

Fig. 14 - For P-Channel

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