

23-26GHz Reflective SP4T Switch

Preliminary

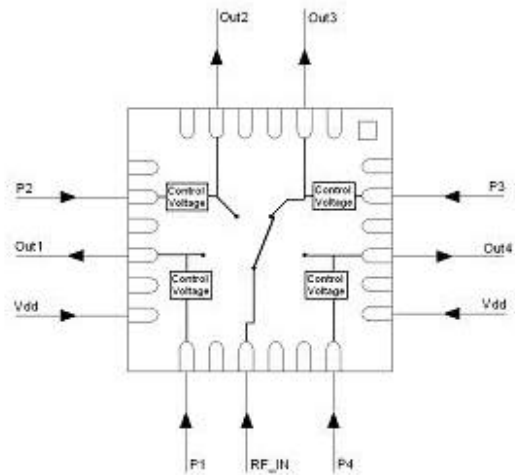
GaAs Monolithic Microwave IC In QFN package

Description

- The CHS2411 is a monolithic reflective SP4T Switch in K-Band. Positive supply voltage only is required.

The circuit is manufactured with a standard PHEMT process : 0.25 μ m gate length, via holes through the substrate, air bridges and electron beam gate lithography.

The chip is delivered in a 24 Leads RoHS compliant QFN4x4 package.



Functional Block Diagram

Main Features

Low insertion loss : 4 dB max
High Isolation : 32 dB min
Fast switching time

- Low consumption
- High temperature range
- Positive supply voltage
- Standard SMD package : QFN 24L 4x4



Plastic Package

Main Characteristics in QFN package

Parameters	Min	Typ	Max	Unit
Frequency range	23		26	GHz
Insertion loss		2.9		dB
Isolation		35		dB
Return Loss		15		dB

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !

Electrical Characteristics in QFN package

Preliminary

Full Temperature Range

Symbol/Pins	Parameters	Min	Typ	Max	Unit
	Frequency range	23		26	GHz
	Isolation	32	35		dB
	Insertion loss		2.9		dB
	Return loss		15		dB
	Input power at 1 dBc@24GHz	18	23.5		dBm
	Switching speed		80		ns
	Operating temperature range	-40	25	100	°C

Vdd/5V	Positive Supply Voltage		5		V
	Supply current		5.5	8	mA
Pi (i=1,2,3,4)	Leakage Current		1	5	uA
Pi (i=1,2,3,4)	OFF state Control Voltage (High state)	4	5		V
Pi (i=1,2,3,4)	ON state Control Voltage (Low State)		0	2	V

Remarks :

- By design the ports OUT1 and OUT2 are respectively symmetrical to ports OUT4 and OUT3.

These performance has been obtained with the chip in QFN package mounted on the recommended boards (ref. 96148 & 95619) described in the document. The performances are highly dependent on this environment.

Truth Table

Control Pin				Signal Path State			
P1	P2	P3	P4	IN to Out1	IN to Out2	IN to Out3	IN to Out4
Low	High	High	High	ON	OFF	OFF	OFF
High	Low	High	High	OFF	ON	OFF	OFF
High	High	Low	High	OFF	OFF	ON	OFF
High	High	High	Low	OFF	OFF	OFF	ON

Absolute Maximum Ratings (1)

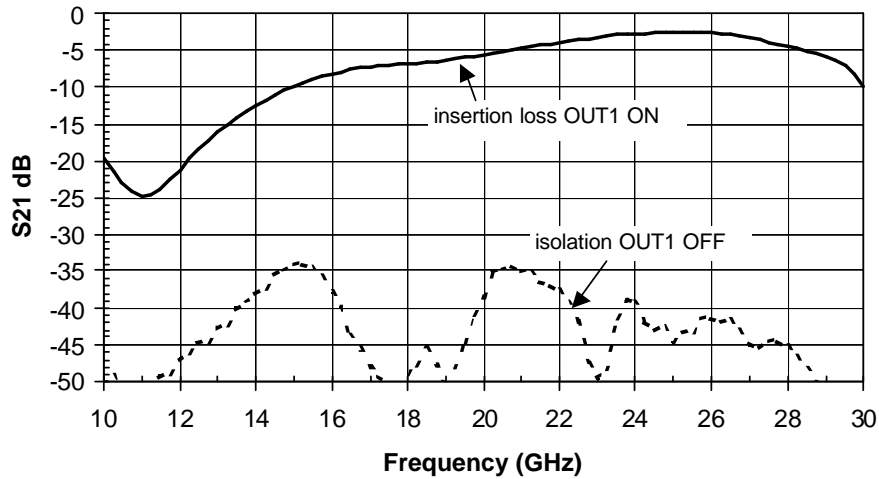
Symbol	Parameters	Values	Unit
Vdd	Positive supply voltage	6	V
Pin	Maximum peak input power overdrive	26	dBm
Top	Operating temperature range	-40 to +100	°C
Tch	Storage temperature range	-55 to +125	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage. Duration < 1s

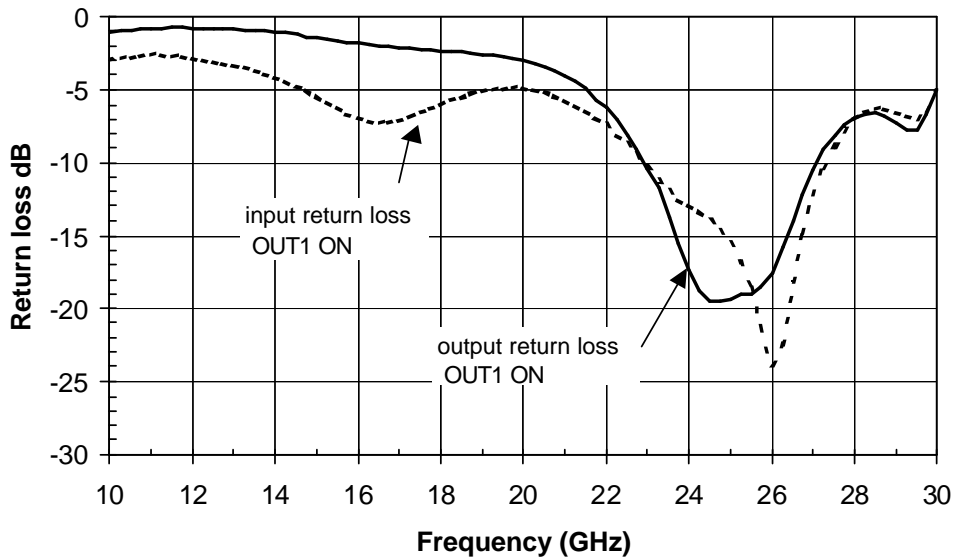
Typical QFN measurements on board 95619 (QFN plan)

Preliminary

Typical Sij Parameters vs Frequency in QFN package plans
(RF - OUT1 path)

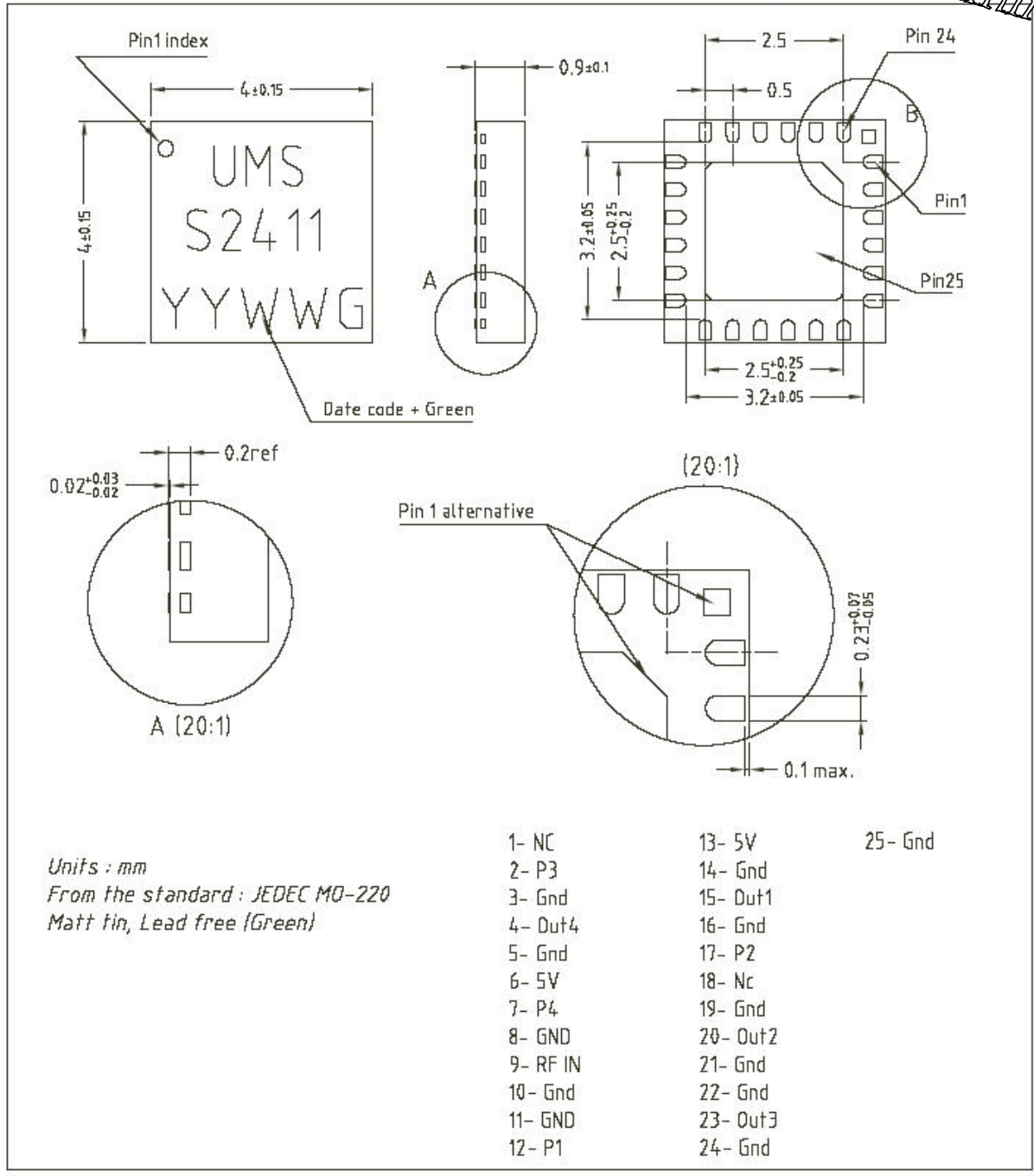


Typical Sij Parameters vs Frequency in QFN package plans
(RF - OUT1 path)



QFN Outlines and Pin-out

Preliminary

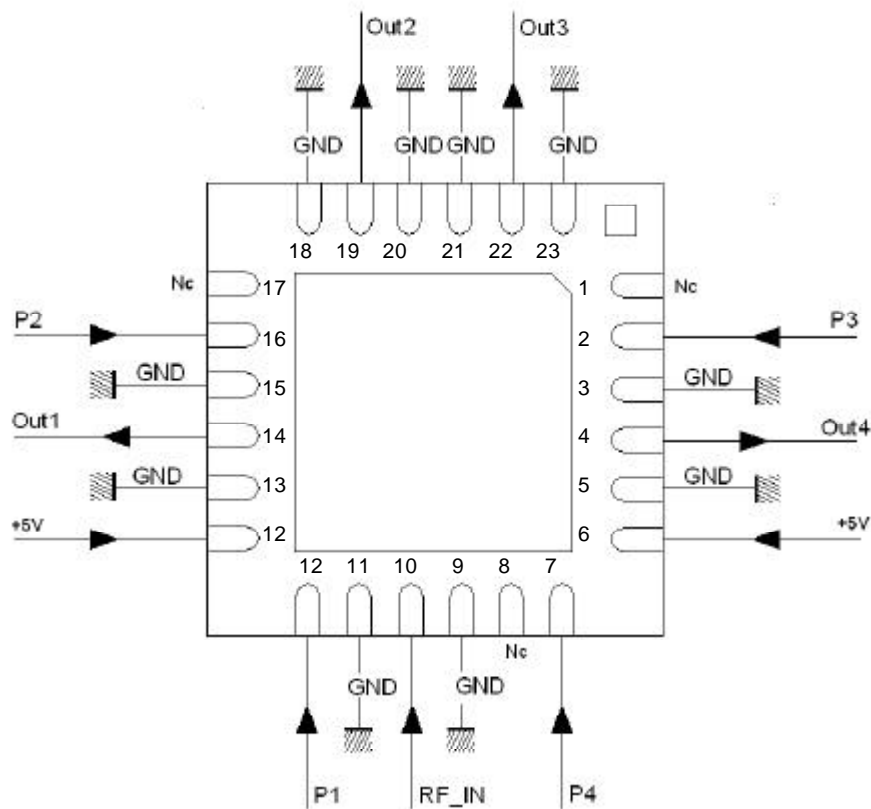


QFN Pin-out description

Preliminary

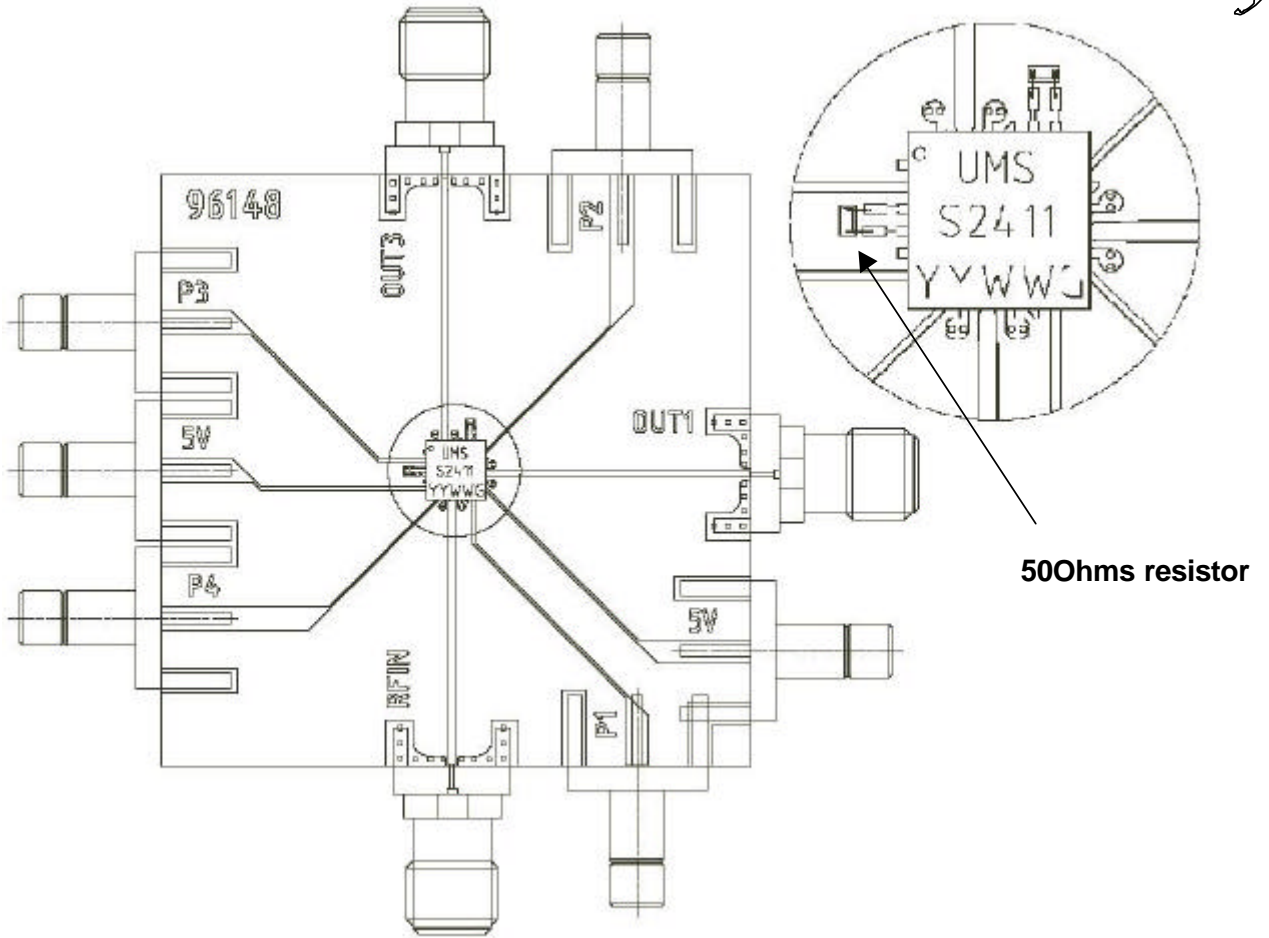
Pin number	Pin name	Symbol Name	Description
12, 17, 2, 17	P1, P2, P3, P4		Control Voltage port
9, 15, 20, 23, 4	RF IN, Out1, Out2, Out3, Out4		RF1 Input/Output ports
6, 13	5V		Positive supply voltage
3, 5, 8, 10, 11, 14, 16, 19, 21, 22, 24	GND		Ground
1,18	Nc		Not connected

External Components and bias configuration (recommended)



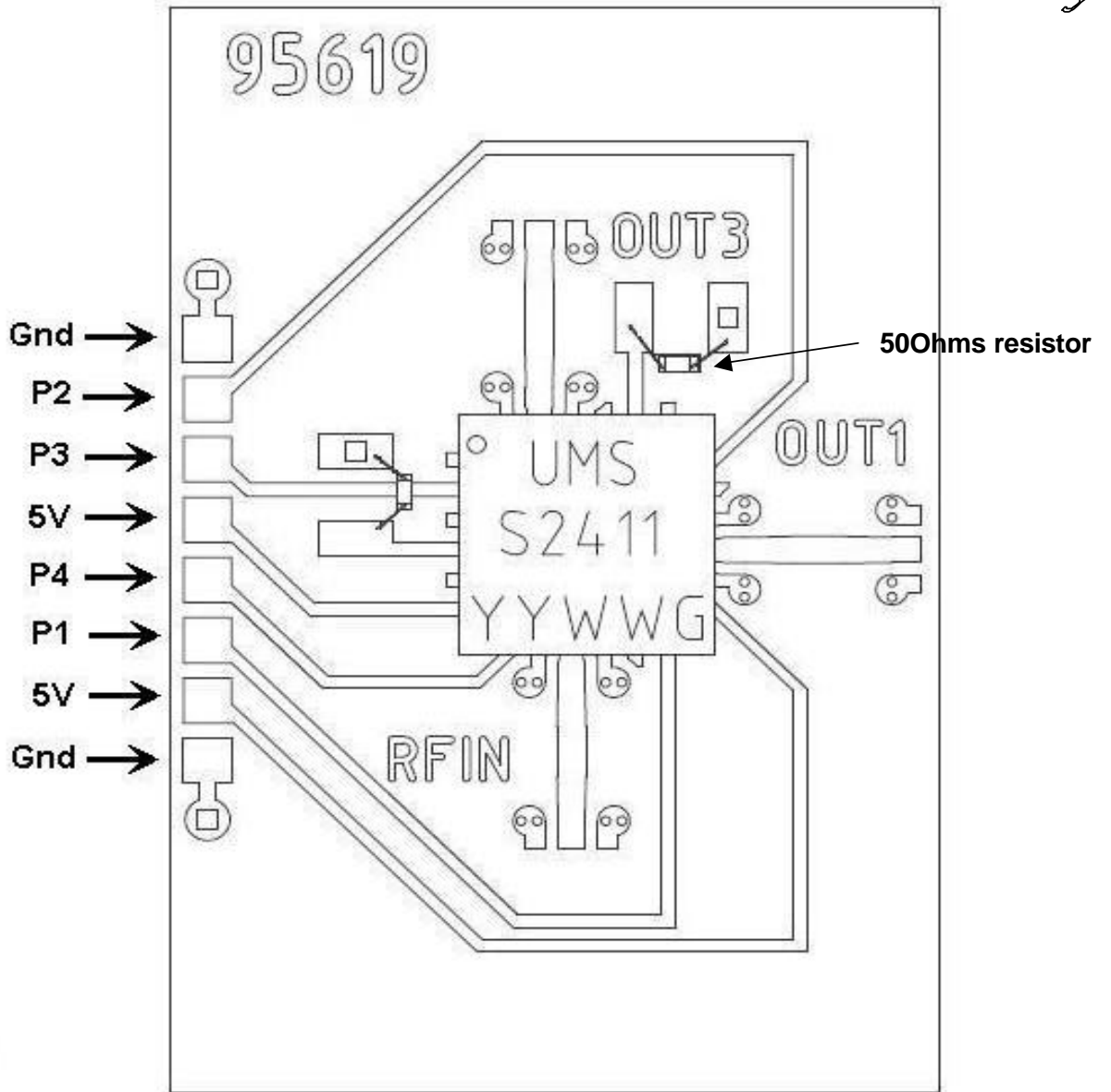
Recommended Test Fixture (Ref. 96148) for measurements over Temperature Range

Preliminary



Recommended Test Fixture (Ref. 95619) for measurements in the package's plans with probes

Preliminary



ESD sensitivity

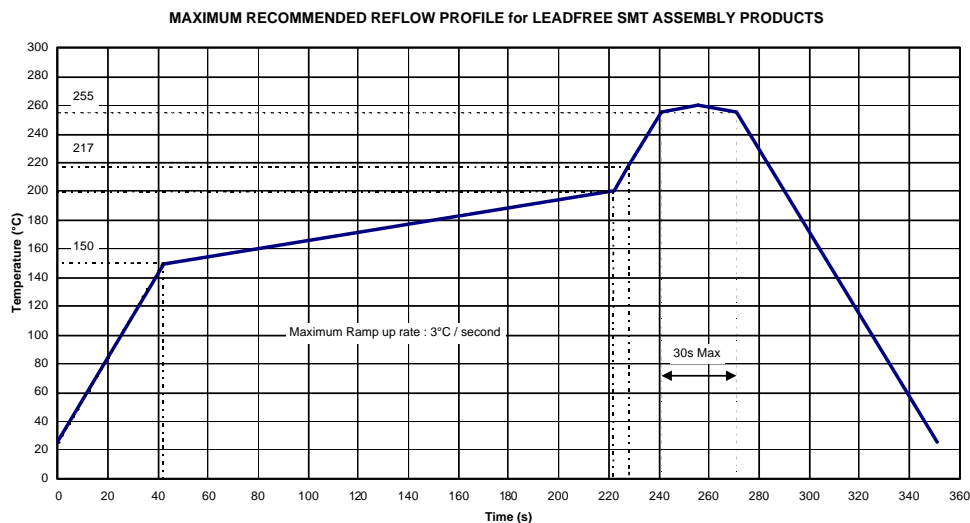
Norm	Value
MIL-STD-1686C	HBM Class 1 (<1000V)
ESD STM5.1-1998	HBM Class 0 (<250V)

*Preliminary***Package Information**

Parameter	
Package body material	RoHS-compliant Low stress Injection Molded Plastic
Lead finish	100% matte Sn
MSL Rating	MSL1

**Recommended surface mount package assembly
(see UMS AN0017)**

For volume production the SMD type package can be treated as a standard surface mount component (please refer to the IPC/JEDEC JSTD-020C standard or equivalent). The assembly on the motherboard can be performed using a standard assembly process (e.g. stencil solder printing, standard pick-and-place machinery, and solder reflow oven). However, caution should be taken to perform a good and reliable contact over the whole pad area.

**Attention:**

The solder thickness after reflow should be typical 50µm [2 mils] and the lateral alignment between the package and the motherboard should be within 50µm [2 mils].

It is important for the performance of the product that the whole overlapping area between the motherboard and package pads is connected. Voids or other improper connections, in particular, between the ground pads on motherboard and package will lead to a deterioration of the RF performance and the heat dissipation. The latter effect can reduce drastically reliability and lifetime of the product.

Preliminary

Ordering Information

24L-QFN4x4 Lead Free Package : CHS2411-QDG/XY

Stick: XY=20 Tape and reel: XY=21

Information furnished is believed to be accurate and reliable. However **United Monolithic Semiconductors S.A.S.** assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of **United Monolithic Semiconductors S.A.S.**. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. **United Monolithic Semiconductors S.A.S.** products are not authorised for use as critical components in life support devices or systems without express written approval from **United Monolithic Semiconductors S.A.S.**