

CRYSTAL CONTROLLED OSCILLATORS

SURFACE MOUNT 3.3V LVPECL CLOCK



FPLA521

ABSOLUTE MAXIMUM RATINGS

TABLE 1.0

PARAMETER	UNITS	MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTE
Storage Temperature		-40	-	85	°C	
Supply Voltage	(Vcc)	-0.5	-	7.0	Vdc	

OPERATING SPECIFICATIONS

TABLE 2.0

PARAMETER		MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTE
Center Frequency	(Fo)	44.736	-	500	MHz	
Total Frequency Tolerance		-50	-	50	ppm	1
Operating Temperature Range		0	-	70	°C	
Supply Voltage	(Vcc)	3.135	3.3	3.465	Vdc	
Supply Current	(Icc)	-	-	80	mA	
Jitter (BW=10Hz to 20MHz)		-	-	5	pS RMS	
Jitter (BW=12kHz to 20MHz)		-	-	1	pS RMS	

LVPECL OUTPUT CHARACTERISTICS

TABLE 3.0

PARAMETER		MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTE
LOAD		-	-	50	Ohms	2
Voltage (High)	(Voh)	2.275	-	-	Vdc	
(Low)	(Vol)	-	-	1.68	Vdc	
Duty Cycle		45	50	55	%	3
Rise / Fall Time 20% to 80%		-	-	1	nS	

PACKAGE CHARACTERISTICS

TABLE 4.0

Package	Non-hermetic package consisting of an FR4 substrate with grounded metal cover.
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PROCESS RECOMMENDATIONS

TABLE 5.0

Solder Reflow	The component solder used internal to this device has a melting point of 221°C. The peak temperature inside the device should be less than or equal to 220°C for a maximum of 10 seconds.
Wash	Ultrasonic cleaning is not recommended.

NOTES:

1. Includes initial tolerance, deviation over temperature, supply and load variations, shock, vibration and 10 years aging.
2. Output must be terminated into 50 ohms to Vcc - 2V Thevenin equivalent.
3. Duty Cycle measured at 1.977V.

DESCRIPTION

The Connor-Winfield FPLA521 is a fixed frequency, surface mount Crystal Controlled Oscillator (XO) designed for applications requiring low jitter and a ± 50 ppm overall stability. Operating at 3.3V supply voltage, the FPLA521 provides LVPECL complementary outputs.

FEATURES

- 3.3V OPERATION
- LOW JITTER <1pS RMS
- OVERALL FREQUENCY TOLERANCE ± 50 ppm
- TEMPERATURE RANGE: 0 to 70°C
- SURFACE MOUNT PACKAGE
- TAPE AND REEL PACKAGING

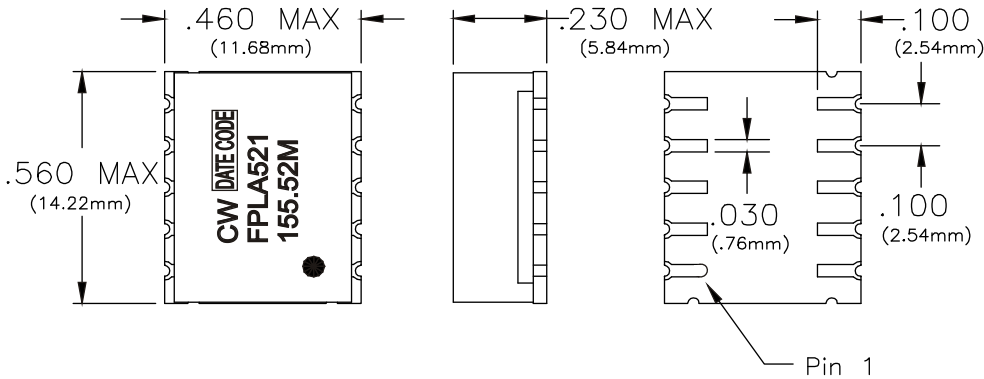
ORDERING INFORMATION

FPLA521 - 155.52MHz



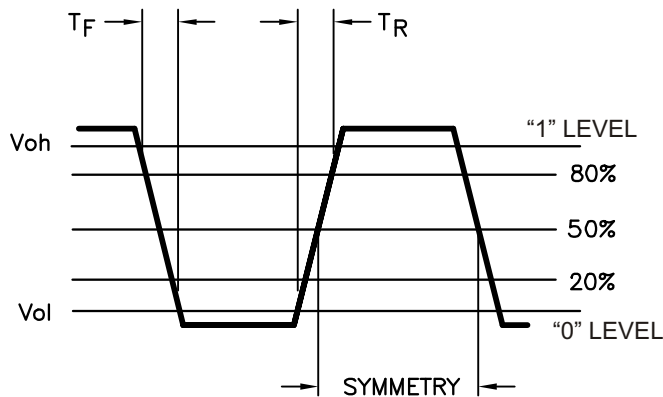
Specifications subject to change without notice.

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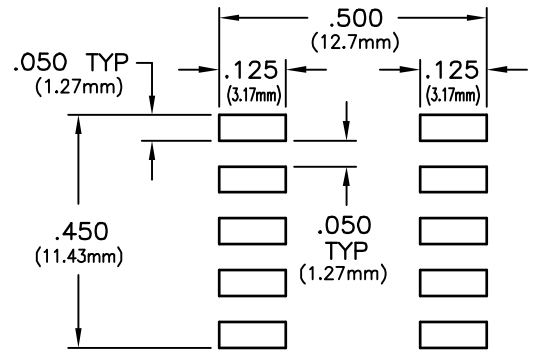


PIN	CONNECTION
1	N/C
2	N/C
3	N/C
4	GROUND
5	N/C
6	Q OUTPUT
7	Q OUTPUT
8	N/C
9	Vcc
10	N/C

OUTPUT WAVEFORM



SUGGESTED PAD LAYOUT



TEST CIRCUIT

