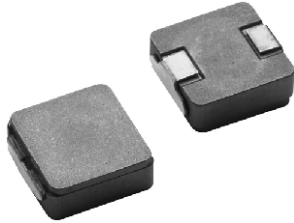




## Low Profile, High Current IHLP® Inductor



Manufactured under one or more of the following:  
**US Patents; 6,198,375/6,204,744/6,449,829/6,460,244.**  
 Several foreign patents, and other patents pending.

STANDARD ELECTRICAL SPECIFICATIONS				
INDUCTANCE $L_o$ $\mu\text{H} \pm 20\% \text{ AT}$ 100 kHz, 0.25 V, 0 A	DCR $m\Omega$ TYP. 25 °C	DCR $m\Omega$ MAX. 25 °C	HEAT RATING CURRENT DC AMPS <sup>3</sup> TYP.	SATURATION CURRENT DC AMPS <sup>4</sup> TYP.
0.19	0.70	0.80	40	46
0.22	0.85	0.95	33	44
0.24	0.85	0.95	33	44
0.36	1.05	1.15	32	30
0.47	1.53	1.68	30	30
0.56	1.60	1.80	32	22
0.78	1.80	1.90	27	22
1.0	2.30	2.50	25	20
1.8	4.50	5.00	17	16
2.0	5.20	5.80	16	14
4.7	12.9	14.2	9.5	7.6
6.8	17.5	19.3	9.0	7.5
10.0	27.8	30.5	7.5	7.1
15.0	40.9	45.0	6.25	6.0
22.0	60.4	66.0	5.0	4.5
33.0	87.5	94.5	4.4	4.0
47.0	132.0	145.0	3.3	3.0
100.0	249.0	270.0	2.5	2.25

**Notes**

- (1) All test data is referenced to 25 °C ambient
- (2) Operating Temperature Range - 55 °C to + 125 °C
- (3) DC current (A) that will cause an approximate  $\Delta T$  of 40 °C
- (4) DC current (A) that will cause  $L_o$  to drop approximately 20 %
- (5) The part temperature (ambient + temp rise) should not exceed 125 °C under worst case operating conditions. Circuit design, component placement, PWB trace size and thickness, airflow and other cooling provisions all affect the part temperature. Part temperature should be verified in the end application.

**FEATURES**

- Shielded construction
- Frequency range up to 1.0 MHz
- Lowest DCR/ $\mu\text{H}$ , in this package size
- Handles high transient current spikes without saturation
- Ultra low buzz noise, due to composite construction
- Excellent temperature stability for inductance and saturation
- 100 % lead (Pb)-free and RoHS compliant



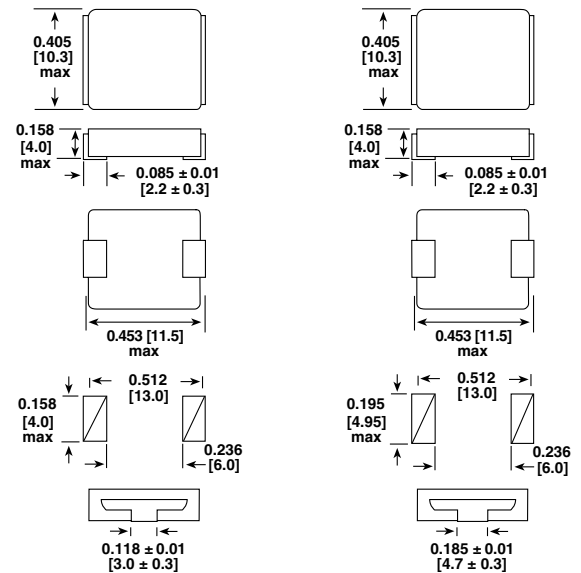
**RoHS**  
COMPLIANT

**APPLICATIONS**

- PDA/Notebook/Desktop/Server applications
- High current POL converters
- Low profile, high current power supplies
- Battery powered devices
- DC/DC converters in distributed power systems
- DC/DC converter for Field Programmable Gate Array (FPGA)

**DIMENSIONS** in inches [millimeters]

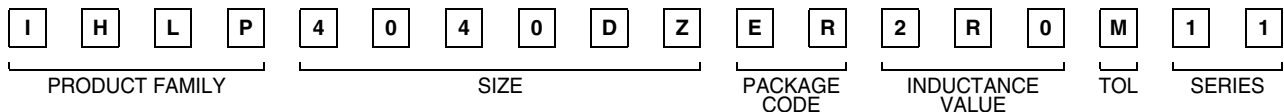
Typical Pad Layout



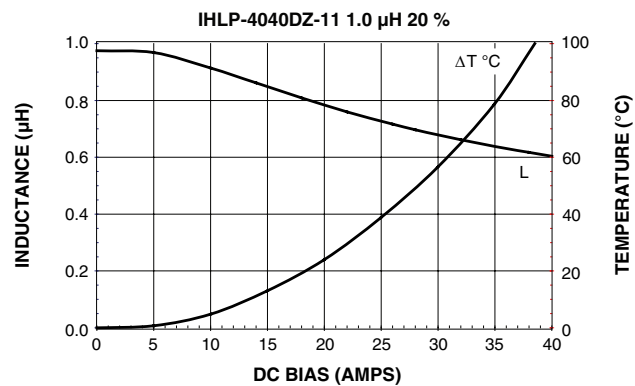
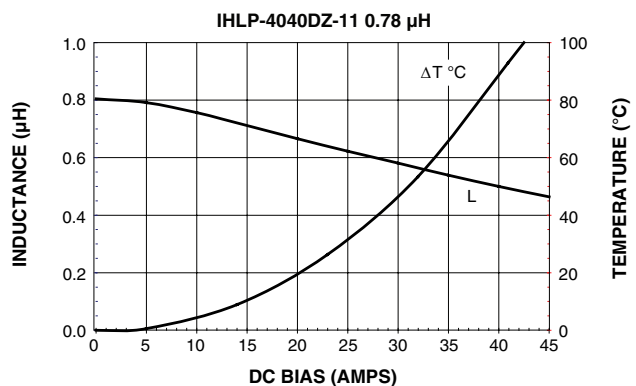
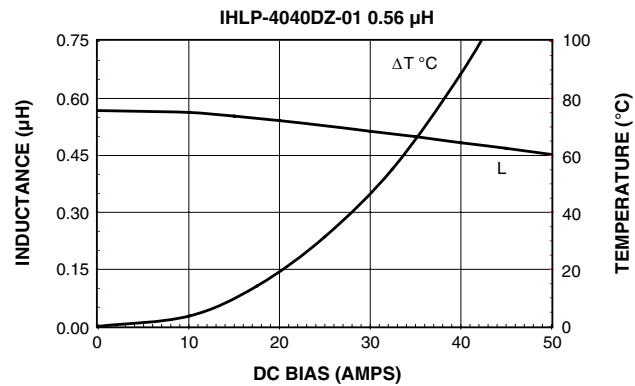
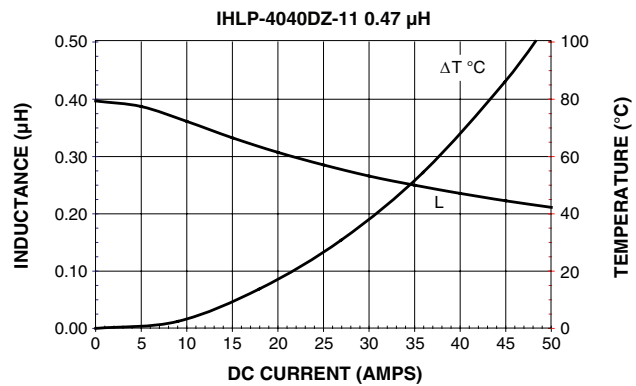
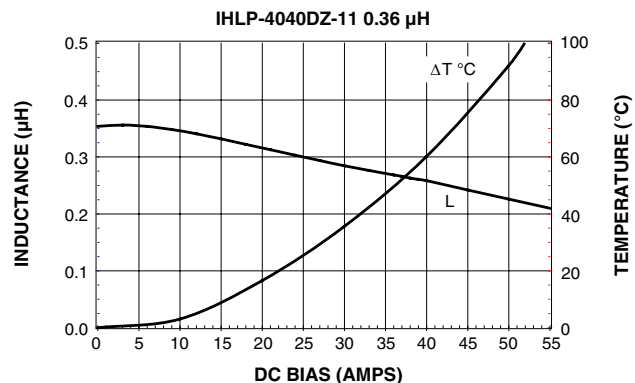
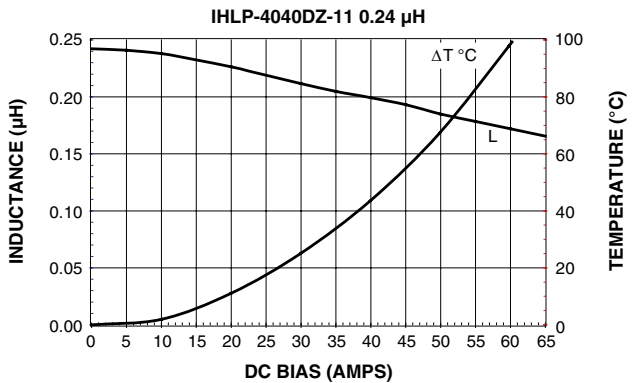
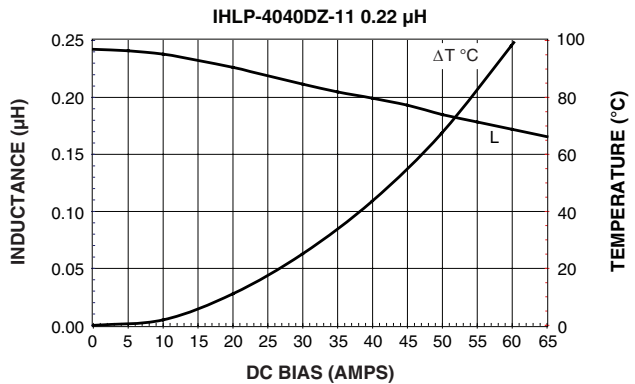
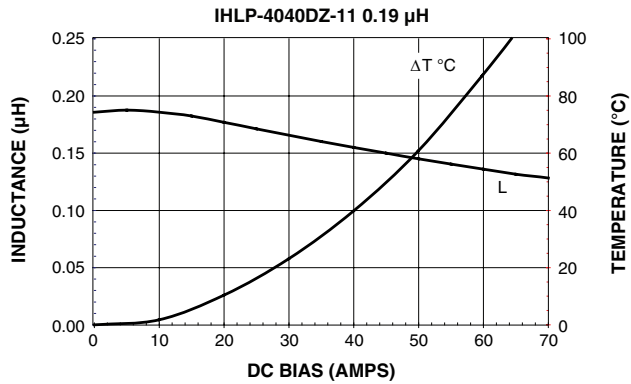
**DESCRIPTION**

IHLP-4040DZ-11	2.0 $\mu\text{H}$	$\pm 20\%$	ER	e3	WEB CODE
MODEL	INDUCTANCE VALUE	INDUCTANCE TOLERANCE	PACKAGE CODE	JEDEC LEAD (Pb)-FREE STANDARD	sm, pi, au, cm, in, ps, te

**GLOBAL PART NUMBER**

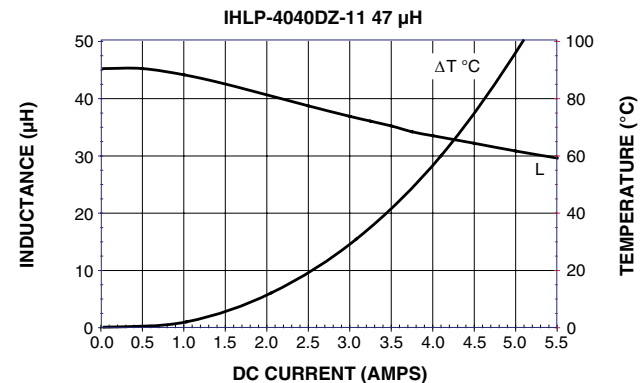
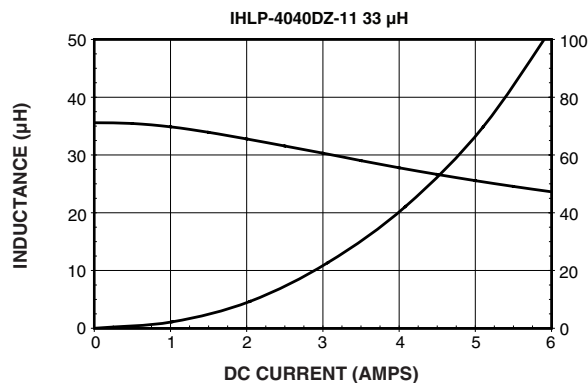
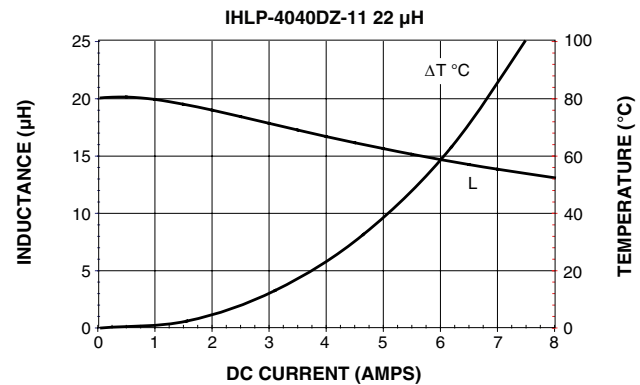
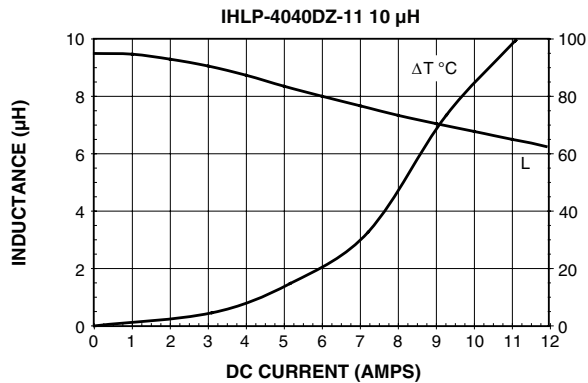
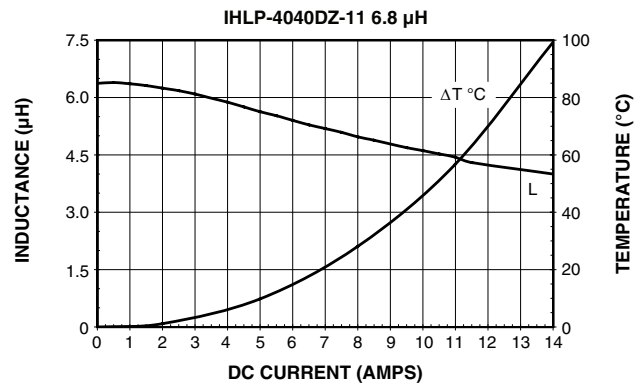
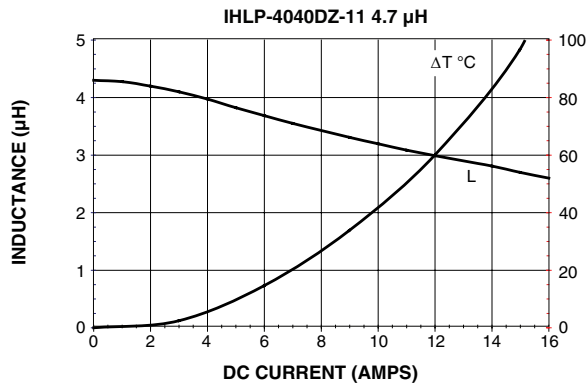
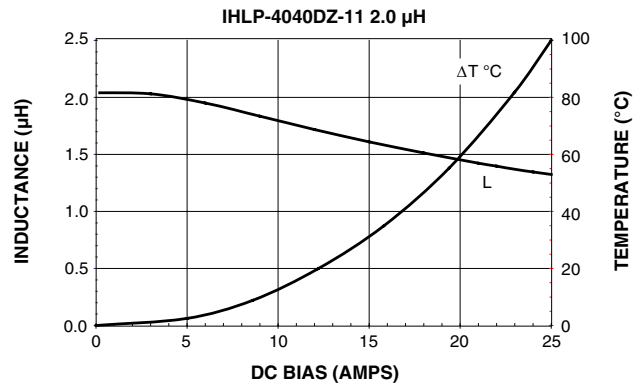
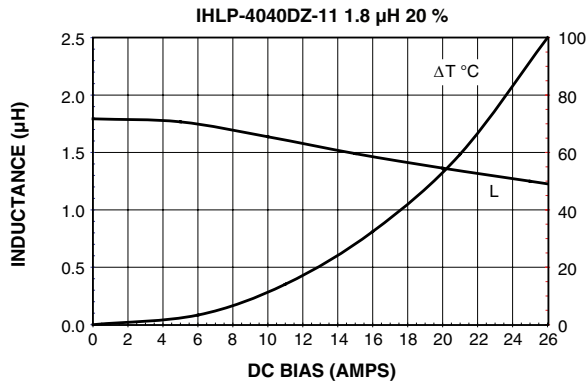


## PERFORMANCE GRAPHS

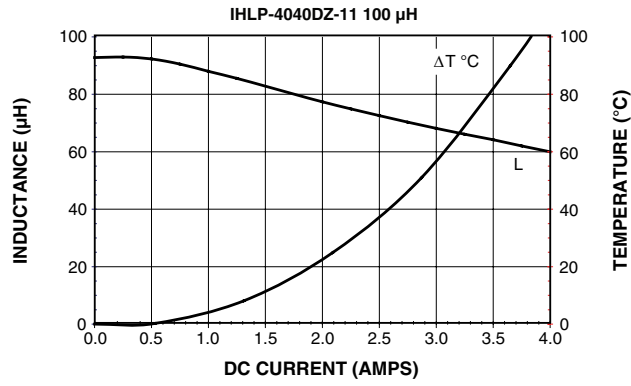




## PERFORMANCE GRAPHS



## PERFORMANCE GRAPHS





## Disclaimer

All product specifications and data are subject to change without notice.

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