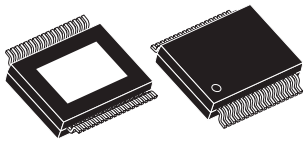
STA333W

2-channel high-efficiency digital audio system

Features

- Wide supply voltage range (4.5 V - 18 V)
- 2 power output configurations
  - 2 channels of binary PWM (stereo mode)
  - 2 channels of ternary PWM
- Power SSO-36 slug down package
- 2 channels of 24-bit DDX®
- 100 dB SNR and dynamic range
- Selectable 32 kHz to 192 kHz input sample rates
- I^2C control with selectable device address
- Digital gain/attenuation +48 dB to -80 dB steps
- Software volume update
- Individual channel and master gain/attenuation
- Individual channel and master software and hardware mute
- Independent channel volume bypass
- Automatic zero-detect mute
- Automatic invalid input detect mute
- 2-channel I^2S input data Interface
- Selectable clock input ratio
- Input channel mapping
- Variable max power correction for lower fullpower
- 96 kHz internal processing sample rate, 24-bit precision
- Advanced AM interference frequency switching and noise suppression modes
- Thermal overload and short-circuit protection embedded
- Video application: 576 x fs input mode support



PowerSSO36 slug (or exposed pad) down

Applications

- LCD
- DVD
- Cradle
- Digital speaker
- Wireless speaker cradle

Description

The STA333W is an integrated solution of digital audio processing, digital amplifier control, and DDX®-power output stage, thereby creating a high-power single-chip DDX® solution comprising of high-quality, high-efficiency, all digital amplification.

The STA333W power section consists of four independent half-bridges. These can be configured via digital control to operate in different modes. 2 channels can be provided by two full-bridges, providing up to 2 x 20 W of power.

Also provided in the STA333W are new advanced AM radio interference reduction modes. The serial audio data input interface accepts all possible formats, including the popular I^2S format.

The STA333W is part of the Sound Terminal™ family that provides full digital audio streaming to the speaker offering cost effectiveness, low power dissipation and sound enrichment.

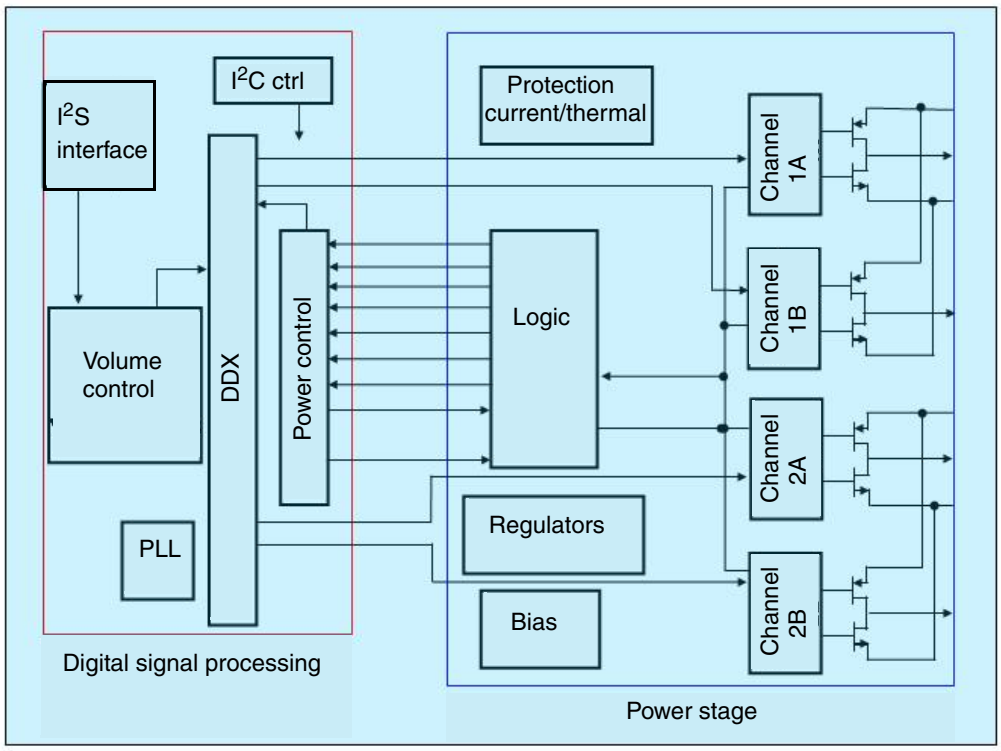
Table 1. Device summary

Part number	Package	Packing
STA333W	PowerSSO36 (slug down)	Tube
STA333W13TR	PowerSSO36 (slug down)	Tape and reel

Contents

1 Block diagram

Figure 1. Block diagram



2 Pin description

Figure 2. Pin connection (Top view)

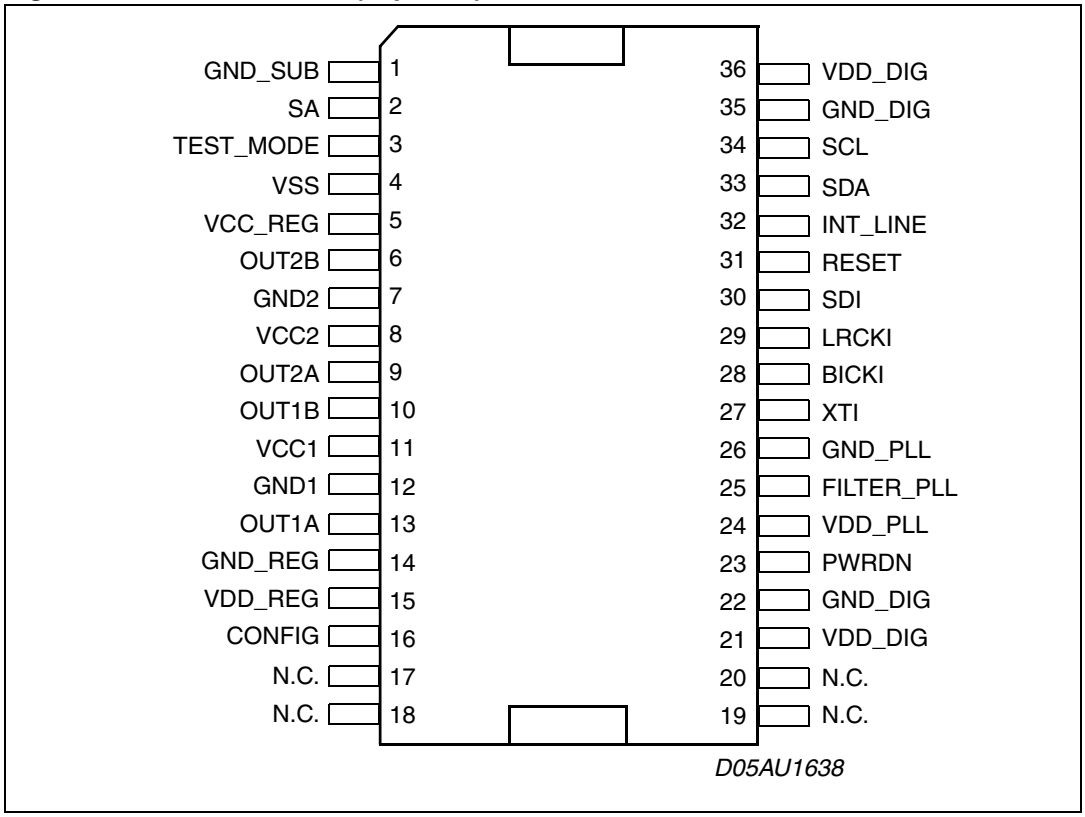


Table 2. Pin description

Pin	Type	Name	Description
1	Gnd	GND_SUB	Substrate ground
2	I	SA	I^2C select address
3	I	TEST_MODE	This pin must be connected to GROUND
4	I/O	VSS	Internal reference at Vcc - 3.3 V
5	I/O	VCC_REG	Internal Vcc reference
6	O	OUT2B	Output half bridge 2B
7	Gnd	GND2	Power negative supply
8	Power	VCC2	Power positive supply
9	O	OUT2A	Output half bridge 2A
10	O	OUT1B	Output half bridge 1B
11	Power	VCC1	Power positive supply
12	Gnd	GND1	Power negative supply
13	O	OUT1A	Output half bridge 1A

Table 2. Pin description (continued)

Pin	Type	Name	Description
14	Gnd	GND_REG	Internal ground reference
15	Power	VDD_REG	Internal 3.3 V reference voltage
16	I	CONFIG	Paralleled mode command
17	-	N.C.	Not connected
18	-	N.C.	Not connected
19	-	N.C.	Not connected
20	-	N.C.	Not connected
21	Power	VDD_DIG	Positive supply digital
22	Gnd	GND_DIG	Digital ground
23	I	PWRDN	Power down 0: low-power mode 1: normal operating mode
24	Power	VDD_PLL	Positive supply for PLL
25	I	FILTER_PLL	Connection to PLL filter
26	Gnd	GND_PLL	Negative supply for PLL
27	I	XTI	PLL input clock, 256 Fs, or 384 Fs
28	I	BICKI	I^2S serial clock
29	I	LRCKI	I^2S left/right clock
30	I	SDI	I^2S serial data channel
31	I	RESET	Reset
32	O	INT_LINE	Fault interrupt
33	I/O	SDA	I^2C serial data
34	I	SCL	I^2C serial clock
35	Gnd	GND_DIG	Digital ground
36	Power	VDD_DIG	Digital supply

3 Electrical specification

3.1 Thermal data

Table 3. Thermal data

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{Th(j\text{-}case)}$	Thermal resistance junction to case (thermal pad)		1.5	2.0	°C/W
T_{sd}	Thermal shut-down junction temperature		150		°C
T_w	Thermal warning temperature		130		°C
T_{hsd}	Thermal shut-down hysteresis		20		°C

3.2 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Analog supply voltage (pins VCCxA, VCCxB)			20	V
V_{DD}	Digital supply voltage (pins VDD_DIG)			3.6	V
I_L	Logic input interface	-0.3		4	V
T_{op}	Operating junction temperature	0		150	°C
T_{stg}	Storage temperature	-40		150	°C

3.3 Recommended operating condition

Table 5. Recommended operating condition

Min.	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Analog supply voltage (VCCxA,VCCxB)	4.5		18.0	V
V_{DD}	Digital supply voltage (VDD_DIG)	2.7	3.3	3.6	V
I_L	Logic input interface	2.7	3.3	3.6	V
T_{amb}	Ambient temperature	0		70	°C

3.4 Electrical characteristics

Table 6. Electrical characteristics
(V_{CC} = 18 V, V_{DD} = 3.3 V, f_{sw} = 384 kHz, T_{amb} = 25° C, R_L = 8 Ω unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Po	Output power BTL	THD = 1%		16		W
		THD = 10%		20		
	Output power SE	R_L = 4 Ω, f = 1 kHz, THD = 1%		7		
		R_L = 4 Ω, f = 1 kHz, THD = 10%		9		
R_{dsON}	Power Pchannel/Nchannel MOSFET (Total bridge)	Id = 1 A		180	250	mΩ
I_{dss}	Power Pchannel/Nchannel leakage	V_{cc} = 18 V			10	µA
gP	Power Pchannel R_{dsON} matching	Id = 1 A	95			%
gN	Power Nchannel R_{dsON} matching	Id = 1 A	95			%
I_{LDT}	Low current dead time (static)	Resistive load, refer to *Figure 3*		5	10	ns
I_{HDT}	High current dead time (dynamic)	Refer to *Figure 4*		10	20	ns
t_r	Rise time	Resistive load, refer to *Figure 3*		8	10	ns
t_f	Fall time	Resistive load, refer to *Figure 3*		8	10	ns
V_{CC}	Supply voltage operating voltage		4.5		18	V
Ivcc	Supply current from Vcc in power down	PWRDN = 0	0.03	0.06	0.2	mA
	Supply current from Vcc in operation	PCM input signal = -60 dBFS Switching frequency = 384 KHz No LC filters		30		mA
Ivdd-dig	Supply current for DDX processing (reference only)	Internal clock = 49.152 MHz	10	30	50	mA
	Supply current in standby		8	11	25	mA
I_{LIM}	Over-current limit	Non-linear output (1)	2.2	3.5	4.3	A
I_{SC}	Short-circuit protection	Hi-Z output (2)	2.7	3.8	5.0	A
UVL	Under-voltage protection threshold			3.5	4.3	V
t_{min}	Output minimum pulse width	No load	20	30	60	ns
THD+N	Total harmonic distortion and noise	DXX stereo mode, Po = 1 W, f = 1 kHz		0.05	0.2	%

Table 6. Electrical characteristics (continued)
(V_{CC} = 18 V, V_{DD} = 3.3 V, f_{sw} = 384 kHz, T_{amb} = 25° C, R_L = 8 Ω unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SNR	Signal to noise ratio in ternary mode	A weighted		100		dB
	Signal to noise ratio in binary mode	A weighted		90		
PSRR	Power supply rejection ratio	DXX stereo mode, < 5 kHz, Vripple = 1 V RMS audio input = dither only		80		dB
X_{TALK}	Crosstalk	DXX stereo mode, < 5 kHz, One channel driven at 1 W the other channel measured		80		dB
η	Peak efficiency in DXX mode	Po = 2 x 20 W into 8 Ω		90		%

1. The I_{LIM} data is for 1 channel of BTL configuration, thus, 2 x I_{LIM} drives the 2-channel BTL configuration. The current limit is active when OCRB = 0 (see *Table 24: Over current warning detect adjustment bypass on page 26*. When OCRB = 1 then I_{SC} applies.
2. The I_{SC} current limit data is for 1 channel of BTL configuration, thus, 2 x I_{SC} drives the 2-channel BTL configuration. The short-circuit current is applicable when OCRB = 1 (see *Table 24: Over current warning detect adjustment bypass on page 26*.

4 Testing

Figure 3. Test circuit

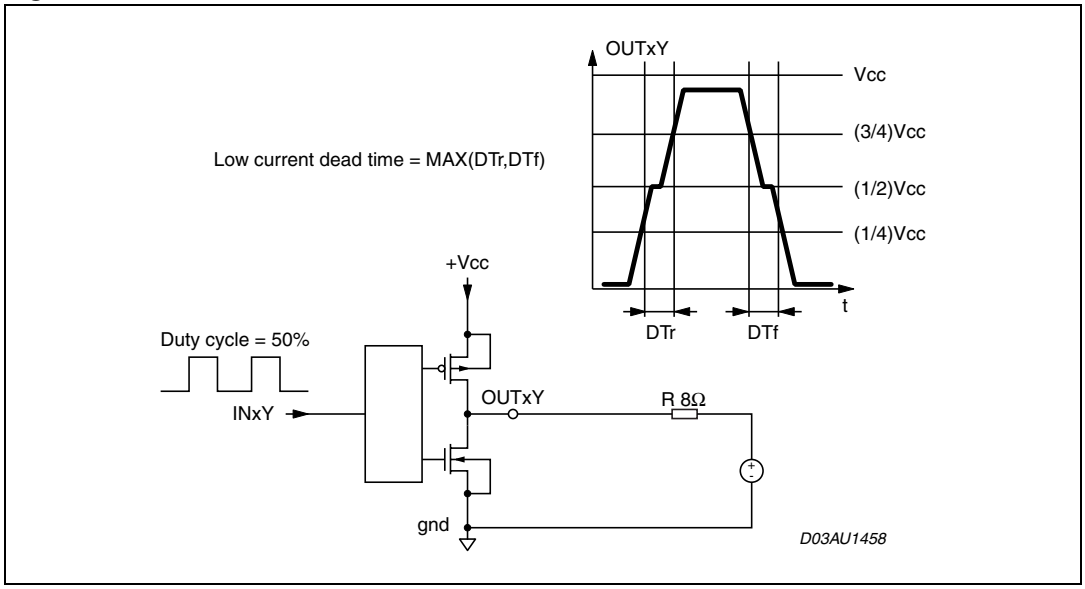
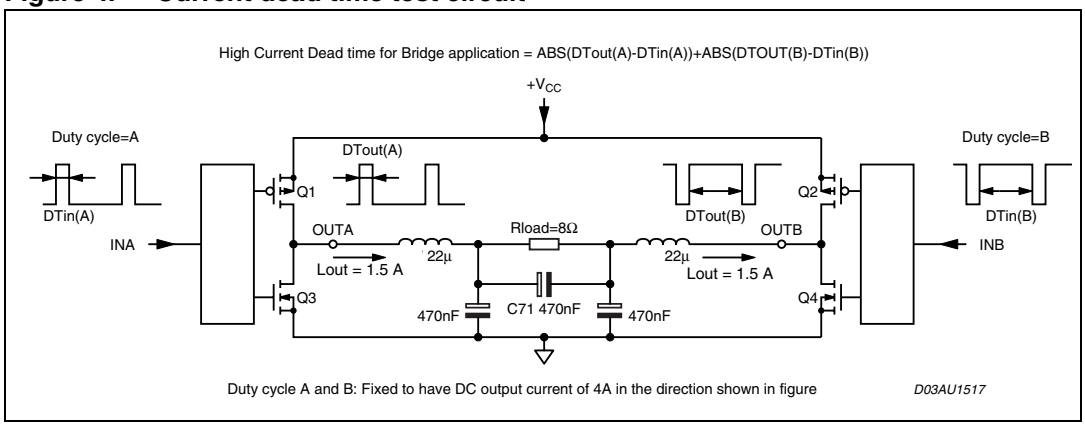


Figure 4. Current dead time test circuit



5 Characterization data

Figure 5. Output power 1% THD

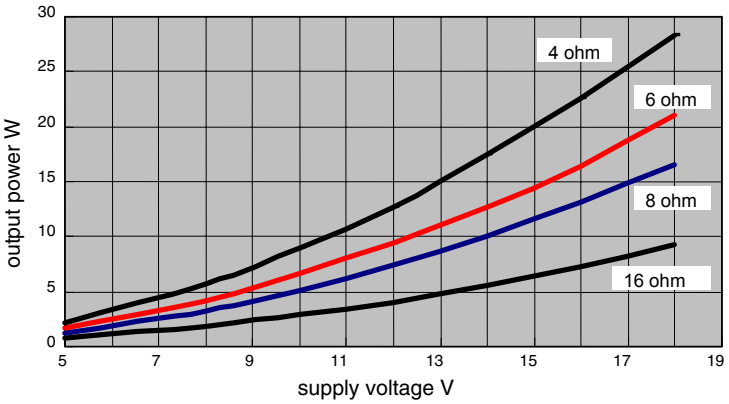


Figure 6. FFT 0 dBfs 1 kHz, Vcc = 12 V, R_L = 8 Ω

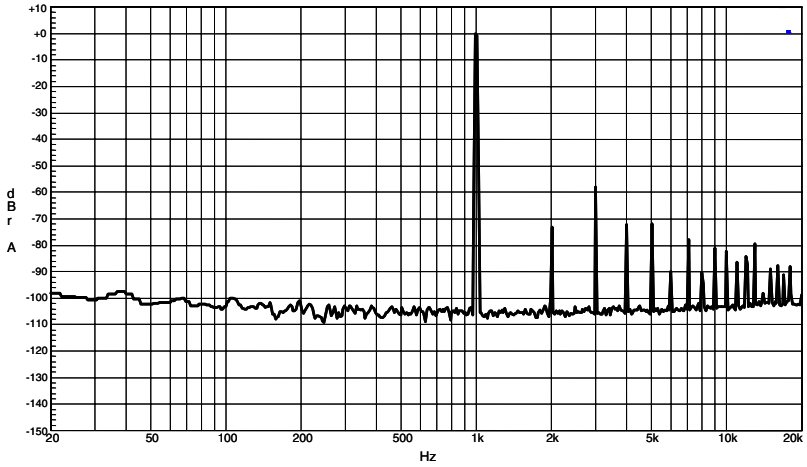


Figure 7. FFT -60 dBfs 1 kHz, Vcc = 12 V, R_L = 8 Ω

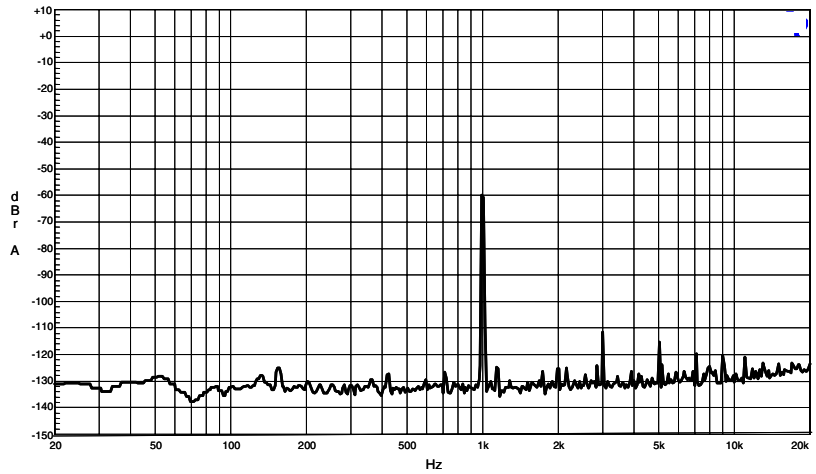


Figure 8. THD vs. Freq, Vcc = 12 V, Po = 1 W

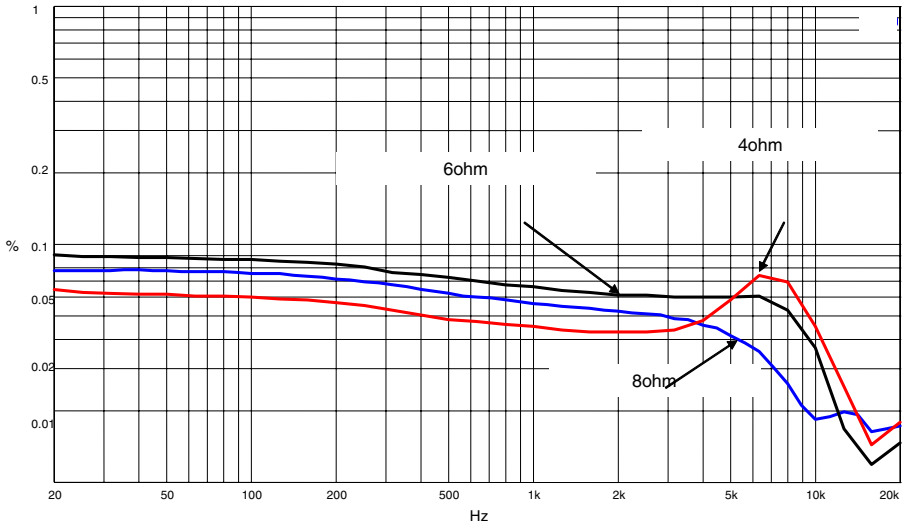


Figure 9. FFT 0 dBfs 1 kHz, Vcc = 18 V, R_L = 8 Ω

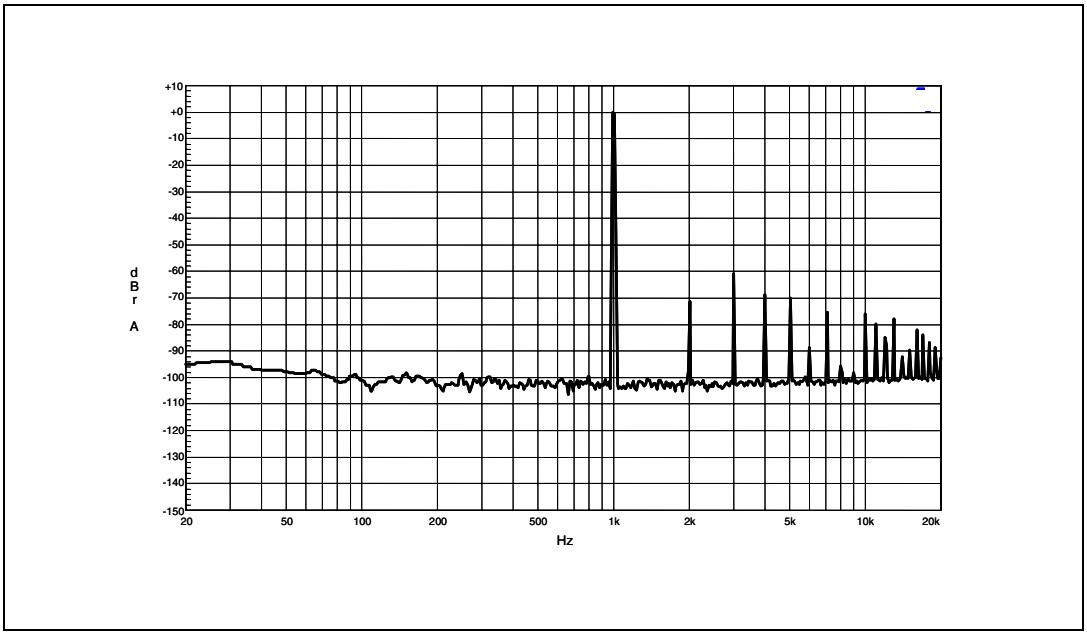


Figure 10. FFT -60 dBfs 1 kHz, Vcc = 18 V, R_L = 8 Ω

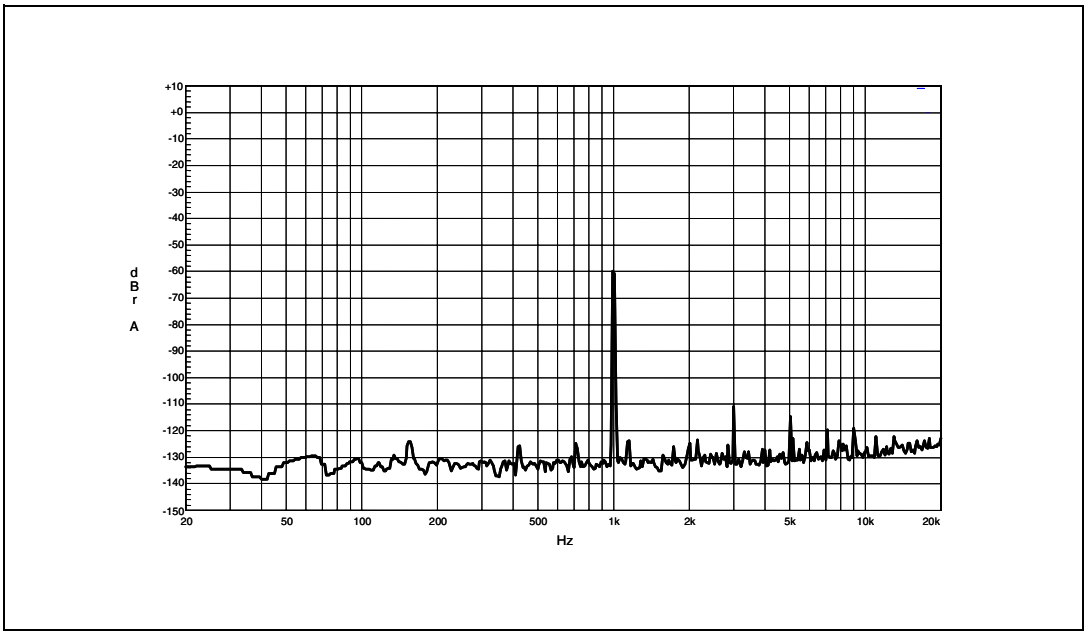
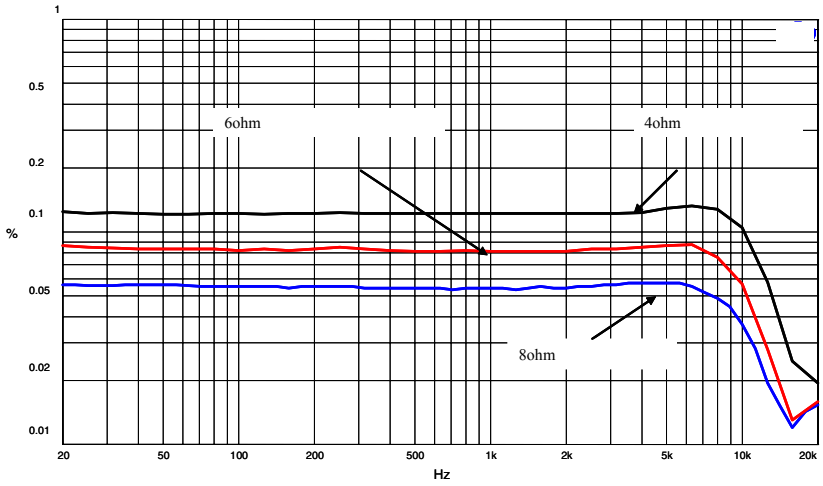


Figure 11. THD vs. Freq, Vcc = 18 V, Po = 1 W



6 I²C bus specification

The STA333W supports the I²C protocol via the input ports SCL and SDA_IN (master to slave) and the output port SDA_OUT (slave to master). This protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master always starts the transfer and provides the serial clock for synchronization. The STA333W is always a slave device in all of its communications. It supports up to 400 kB/sec rate (fast-mode bit rate).

6.1 Communication protocol

6.1.1 Data transition or change

Data changes on the SDA line must only occur when the SCL clock is low. SDA transition while the clock is high is used to identify a START or STOP condition.

6.1.2 Start condition

START is identified by a high to low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must precede any command for data transfer.

6.1.3 Stop condition

STOP is identified by low to high transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A STOP condition terminates communication between STA333W and the bus master.

6.1.4 Data input

During the data input the STA333W samples the SDA signal on the rising edge of clock SCL. For correct device operation the SDA signal must be stable during the rising edge of the clock and the data can change only when the SCL line is low.

6.2 Device addressing

To start communication between the master and the STA333W, the master must initiate with a start condition. Following this, the master sends onto the SDA line 8 bits (MSB first) corresponding to the device select address and read or write mode.

The 7 most significant bits are the device address identifiers, corresponding to the I²C bus definition. In the STA333W the I²C interface has two device addresses depending on the SA port configuration, 0x38 when SA = 0, and 0x3A when SA = 1.

The 8th bit (LSB) identifies read or write operation RW, this bit is set to 1 in read mode and 0 for write mode. After a START condition the STA333W identifies on the bus the device address and if a match is found, it acknowledges the identification on SDA bus during the 9th bit time. The byte following the device identification byte is the internal space address.

6.3 Write operation

Following the START condition the master sends a device select code with the RW bit set to 0. The STA333W acknowledges this and the writes for the byte of internal address. After receiving the internal byte address the STA333W again responds with an acknowledgement.

6.3.1 Byte write

In the byte write mode the master sends one data byte, this is acknowledged by the STA333W. The master then terminates the transfer by generating a STOP condition.

6.3.2 Multi-byte write

The multi-byte write modes can start from any internal address. The master generating a STOP condition terminates the transfer.

Figure 12. Write mode sequence

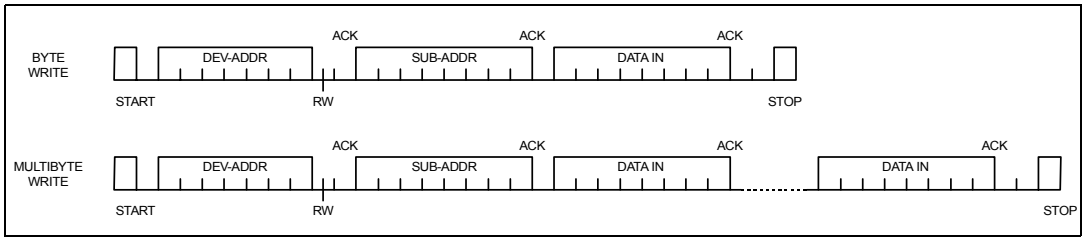
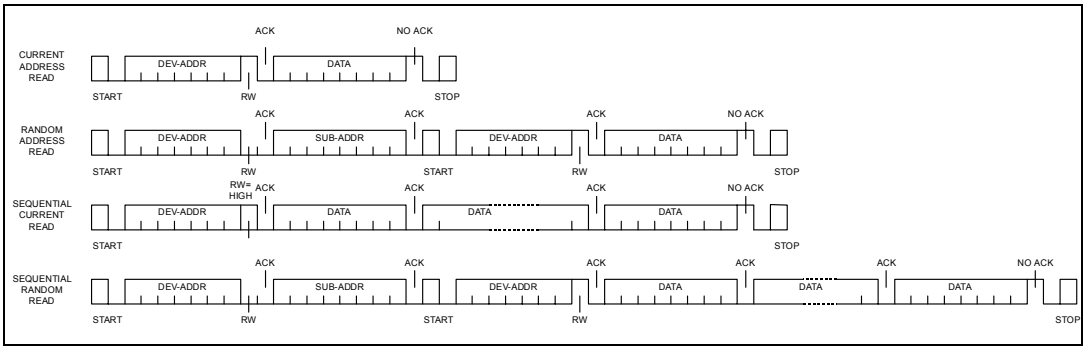


Figure 13. Read mode sequence



7 Register description

Table 7. Register summary(1)

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x00	ConfA	FDRB	TWAB	TWRB	IR1	IR0	MCS2	MCS1	MCS0
0x01	ConfB	C2IM	C1IM	-	SAIFB	SAI3	SAI2	SAI1	SAI0
0x02	ConfC	OCRB	-	CSZ3	CSZ2	CSZ1	CSZ0	OM1	OM0
0x03	ConfD	-	ZDE	-	-	PSL	-	-	-
0x04	ConfE	SVE	ZCE	DCCV	PWMS	AME	NSBW	MPC	MPCV
0x05	ConfF	EAPD	PWDN	ECLE	LDTE	BCLE	IDE	-	-
0x06	Mute	-	-	-	-	-	C2M	C1M	MMute
0x07	Mvol	MV7	MV6	MV5	MV4	MV3	MV2	MV1	MV0
0x08	C1Vol	C1V7	C1V6	C1V5	C1V4	C1V3	C1V2	C1V1	C1V0
0x09	C2Vol	C2V7	C2V6	C2V5	C2V4	C2V3	C2V2	C2V1	C2V0
0x0A	Unused	-	-	-	-	-	-	-	-
0x0B	Unused	-	-	-	-	-	-	-	-
0x0C	Auto	RFU	RFU	RFU	RFU	AMAM2	AMAM1	AMAM0	AMAME
0x0D	Unused	-	-	-	-	-	-	-	-
0x0E	C1Cfg	-	-	-	-	-	C1VBP	-	-
0x0F	C2Cfg	-	-	-	-	-	C2VBP	-	-
0x10	Unused	-	-	-	-	-	-	-	-
0x11	Unused	-	-	-	-	-	-	-	-
0x12	Unused	-	-	-	-	-	-	-	-
0x13	Unused	-	-	-	-	-	-	-	-
0x14	Unused	-	-	-	-	-	-	-	-
0x15	Unused	-	-	-	-	-	-	-	-
0x16	Unused	-	-	-	-	-	-	-	-
0x17	Unused	-	-	-	-	-	-	-	-
0x18	Unused	-	-	-	-	-	-	-	-
0x19	Unused	-	-	-	-	-	-	-	-
Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x1A	Unused	-	-	-	-	-	-	-	-
0x1B	Unused	-	-	-	-	-	-	-	-
0x1C	Unused	-	-	-	-	-	-	-	
0x1D	Unused	-	-	-	-	-	-	-	-
0x1E	Unused	-	-	-	-	-	-	-	-

Table 7. Register summary[1] (continued)

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x1F	Unused	-	-	-	-	-	-	-	-
0x20	Unused	-	-	-	-	-	-	-	-
0x21	Unused	-	-	-	-	-	-	-	-
0x22	Unused	-	-	-	-	-	-	-	-
0x23	Unused	-	-	-	-	-	-	-	-
0x24	Unused	-	-	-	-	-	-	-	-
0x25	Unused	-	-	-	-	-	-	-	-
0x26	Unused	-	-	-	-	-	-	-	-
0x27	MPCC1	MPCC15	MPCC14	MPCC13	MPCC12	MPCC11	MPCC10	MPCC9	MPCC8
0x28	MPCC2	MPCC7	MPCC6	MPCC5	MPCC4	MPCC3	MPCC2	MPCC1	MPCC0
0x29	DCC1	DCC15	DCC14	DCC13	DCC12	DCC11	DCC10	DCC9	DCC8
0x2A	DCC2	DCC7	DCC6	DCC5	DCC4	DCC3	DCC2	DCC1	DCC0
0x2B	FDRC1	FDRC15	FDRC14	FDRC13	FDRC12	FDRC11	FDRC10	FDRC9	FDRC8
0x2C	FDRC2	FDRC7	FDRC6	FDRC5	FDRC4	FDRC3	FDRC2	FDRC1	FDRC0
0x2D	Status	PLLUL	FAULT	UVFAULT	OVFAULT	OCFAULT	OCWARN	TFAULT	TWARN
0x2E	BIST1	RFU	RFU	RO1BACT	R5BACT	R4BACT	R3BACT	R2BACT	R1BACT
0x2F	BIST2	RFU	RFU	R01BEND	R5BEND	R4BEND	R3BEND	R2BEND	R1BEND
0x30	BIST3	RFU	RFU	RFU	R5BBAD	R4BBAD	R3BBAD	R1BBAD	R1BBAD
0x31	TSTCTL	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
0x32	C1PS	C1PS7	C1PS6	C1PS5	C1PS4	C1PS3	C1PS2	C1PS1	C1PS0
0x33	C2PS	C2PS7	C2PS6	C2PS5	C2PS4	C2PS3	C2PS2	C2PS1	C2PS0
0x34	OLIM	OLIM7	OLIM6	OLIM5	OLIM4	OLIM3	OLIM2	OLIM1	OLIM0

1. RFU: reserved for future use.

7.1 Configuration registers (0x00 - 0x05)

7.1.1 Configuration register A (address 0x00)

D7	D6	D5	D4	D3	D2	D1	D0
FDRB	TWAB	TWRB	IR1	IR0	MCS2	MCS1	MCS0
0	1	1	0	0	0	1	1

Master clock select

Table 8. Master clock select

Bit	R/W	RST	Name	Description
0	R/W	1	MCS0	Master clock select: Selects the ratio between the input I^2S sample frequency and the input clock.
1	R/W	1	MCS1	
2	R/W	0	MCS2	

The STA333W will support sample rates of 32 kHz, 44.1 kHz, 48 KHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz. Therefore the internal clock will be:

- 32.768 MHz for 32 kHz
- 45.1584 MHz for 44.1 kHz, 88.2 kHz, and 176.4 kHz
- 49.152 MHz for 48 kHz, 96 kHz, and 192 kHz

The external clock frequency provided to the XTI pin must be a multiple of the input sample frequency (f_S).

The relationship between the input clock and the input sample rate is determined by both the MCSx and the IR (input rate) register bits. The MCSx bits determine the PLL factor generating the internal clock and the IR bit determines the oversampling ratio used internally.

Table 9. MCS bits

Input sample rate fs (kHz)	IR	MCS(2..0)					
		101	100	011	010	001	000
32, 44.1, 48	00	576 fs	128 fs	256 fs	384 fs	512 fs	768 fs
88.2, 96	01	NA	64 fs	128 fs	192 fs	256 fs	384 fs
176.4, 192	1X	NA	32 fs	64 fs	96 fs	128 fs	192 fs

Interpolation ratio select

Table 10. Interpolation ratio select

Bit	R/W	RST	Name	Description
4:3	R/W	00	IR [1:0]	Interpolation ratio select: Selects internal interpolation ratio based on input I^2S sample frequency.

The STA333W has variable interpolation (oversampling) settings such that internal processing and DDX output rates remain consistent. The first processing block interpolates by either 2 times or 1 time (pass-through) or provides a 2-times downsample. The oversampling ratio of this interpolation is determined by the IR bits.

Table 11. IR bit settings as a function of input sample rate

Input sample rate Fs (kHz)	IR	1st stage interpolation ratio
32	00	2 times oversampling
44.1	00	2 times oversampling
48	00	2-times oversampling
88.2	01	Pass-through
96	01	Pass-through
176.2	10	2-times downsampling
192	10	2-times downsampling

Thermal warning recovery bypass

Table 12. Thermal warning recovery

Bit	R/W	RST	Name	Description
5	R/W	1	TWRB	Thermal warning recovery bypass: 0: thermal warning recovery enabled 1: thermal warning recovery disabled

If the thermal warning adjustment is enabled (TWAB = 0), then the thermal warning recovery determines if the -3 dB output limit is removed when thermal warning is negative.

If TWRB = 0 and TWAB = 0, then when a thermal warning disappears the -3 dB output limit is removed and the gain is added back to the system. If TWRB = 1 and TWAB = 0, then when a thermal warning disappears the -3 dB output limit remains until TWRB is changed to zero or the device is reset.

Thermal warning adjustment bypass

Table 13. Thermal warning adjustment

Bit	R/W	RST	Name	Description
6	R/W	1	TWAB	Thermal warning adjustment bypass: 0: thermal warning adjustment enabled 1: thermal warning adjustment disabled

The on-chip STA333W power output block provides feedback to the digital controller using inputs to the power control block. The TWARN input is used to indicate a thermal warning condition. When TWARN is asserted (set to 0) for a period of time greater than 400 ms, the power control block will force a -3dB output limit (determined by TWOCL in coeff RAM) to the modulation limit in an attempt to eliminate the thermal warning condition. Once the thermal warning output limit adjustment is applied, it remains in this state until reset, unless FDRB = 0.

Fault detect recovery bypass

Table 14. Fault detect recovery

Bit	R/W	RST	Name	Description
7	R/W	0	FDRB	Fault detect recovery bypass: 0: fault detect recovery enabled 1: fault detect recovery disabled

The on-chip STA333W power output block provides feedback to the digital controller using inputs to the power control block. The FAULT input is used to indicate a fault condition (either over-current or thermal). When FAULT is asserted (set to 0), the power control block will attempt a recovery from the fault by asserting the tri-state output (setting it to 0 which directs the power output block to begin recovery), hold it at 0 for period of time in the range of .1ms to 1 second as defined by the fault detect recovery constant register (FDRC registers 0x29-2A), then toggle it back to 1. This sequence is repeated as log as the fault indication exists. This feature is enabled by default but can be bypassed by setting the FDRB control bit to 1.

7.1.2 Configuration register B (address 0x01)

D7	D6	D5	D4	D3	D2	D1	D0
C2IM	C1IM	RES	SAIFB	SAI3	SAI2	SAI1	SAI0
1	0	0	0	0	0	0	0

Serial audio input interface format

Table 15. Serial audio input interface format

Bit	R/W	RST	Name	Description
0	R/W	0	SAI0	The serial audio input interface format determines the interface format of the input serial digital audio interface.
1	R/W	0	SAI1	
2	R/W	0	SAI2	
3	R/W	0	SAI3	

7.1.3 Serial data interface

The STA333W audio serial input was designed to interface with standard digital audio components and to accept a number of serial data formats. STA333W always acts a slave when receiving audio input from standard digital audio components. Serial data for two channels is provided using 3 inputs: left/right clock LRCKI, serial clock BICKI, and serial data 1 and 2 SDI12.

The SAI register (configuration register B - 0x01, bits D3-D0) and the SAIFB register (configuration register B - 0x01, bit D4) are used to specify the serial data format. The default serial data format is I^2S, MSB first. Available formats are shown in the tables and figure that follow.

Serial data first bit

Table 16.

SAIFB	Format	Notes
0	MSB-first	Default value
1	LSB-first	Default value

Table 17. Support serial audio input formats for MSB first (SAIFB = 0)

BICKI	SAI [3:0]	SAIFB	Interface format
32fs	0000	0	I^2S 15-bit data
	0001	0	Left/right justified 16-bit data
48fs	0000	0	I^2S 16 - 23-bit data
	0001	0	Left justified 16 - 24-bit data
	0010	0	Right justified 24-bit data
	0110	0	Right justified 20-bit data
	1010	0	Right justified 18-bit data
	1110	0	Right justified 16-bit data
64fs	0000	0	I^2S 16 - 24-bit data
	0001	0	Left justified 16 - 24-bit data
	0010	0	Right justified 24-bit data
	0110	0	Right justified 20-bit data
	1010	0	Right justified 18-bit data
	1110	0	Right justified 16-bit data

Table 18. Supported serial audio input formats for LSB-First (SAIFB = 1)

BICKI	SAI[3:0]	SAIFB	Interface format
32fs	1100	1	I^2S 15-bit data
	1110	1	Left/right justified 16-bit data
48fs	0100	1	I^2S 23-bit data
	0100	1	I^2S 20-bit data
	1000	1	I^2S 18-bit data
	1100	1	LSB first I^2S 16-bit data
	0001	1	Left justified 24-bit data
	0101	1	Left justified 20-bit data
	1001	1	Left justified 18-bit data
	1101	1	Left justified 16-bit data
	0010	1	Right justified 24-bit data
48fs	0110	1	Right justified 20-bit data
	1010	1	Right justified 18-bit data
	1110	1	Right justified 16-bit data
64fs	0000	1	I^2S 24-bit data
	0100	1	I^2S 20-bit data
	1000	1	I^2S 18-bit data
	1100	1	LSB First I^2S 16-bit data
	0001	1	Left justified 24-bit data
	0101	1	Left justified 20-bit data
	1001	1	Left justified 18-bit data
	1101	1	Left justified 16-bit data
	0010	1	Right justified 24-bit data
	0110	1	Right justified 20-bit data
	1010	1	Right justified 18-bit data
	1110	1	Right justified 16-bit data

Channel input mapping

Table 19. Channel input mapping

Bit	R/W	RST	Name	Description
6	R/W	0	C1IM	0: processing channel 1 receives left I^2S input 1 : processing channel 1 receives right I^2S input
7	R/W	0	C2IM	0: processing channel 2 receives left I^2S input 1: processing channel 2 receives right I^2S input

Each channel received via I^2S can be mapped to any internal processing channel via the channel input mapping registers. This allows for flexibility in processing. The default settings of these registers map each I^2S input channel to its corresponding processing channel.

7.1.4 Configuration register C (address 0x02)

D7	D6	D5	D4	D3	D2	D1	D0
OCRB		CSZ3	CSZ2	CSZ1	CSZ0	OM1	OM0
1		0	1	0	1	1	1

DDX power output mode

Table 20. DDX power output mode

Bit	R/W	RST	Name	Description
0	R/W	1	OM0	The DDX power output mode selects configuration of DDX output.
1	R/W	1	OM1	

The DDX power output mode selects how the DDX output timing is configured. Different power devices use different output modes. The STA50x or STA51x recommended use is OM = 10.

Table 21. Output modes

OM[1:0]	Output stage – mode
00	STA50x: drop compensation
01	Discrete output stage: tapered compensation
10	STA50x: full power mode
11	Variable drop compensation (CSZx bits)

DDX compensation pulse size register

Table 22. DDX compensating pulse size

Bit	R/W	RST	Name	Description
2	R/W	1	CSZ0	When OM[1:0]: 11, this register determines the size of the DDX compensating pulse from 0 to 15 clock periods.
3	R/W	0	CSZ1	
4	R/W	1	CSZ2	
5	R/W	0	CSZ3	

Table 23. Compensating pulse size

CSZ(3..0)	Compensating pulse size
0000	0 ns (0 ticks) compensating pulse size
0001	20 ns (1 tick) clock period compensating pulse size
…	…
1111	300 ns (15 ticks) clock period compensating pulse size

Over-current warning detect adjustment bypass

Table 24. Over current warning detect adjustment bypass

Bit	R/W	RST	Name	Description
7	R/W	1	OCRB	0: over current warning adjustment enabled 1: over current warning adjustment disabled

The OCWARN input is used to indicate an over current warning condition. When OCWARN is asserted (set to 0), the power control block will force an adjustment to the modulation limit (default -3dB) in an attempt to eliminate the over-current warning condition. Once the over-current warning volume adjustment is applied, it remains in this state until reset is applied. The level of adjustment can be changed via the TWOCL (thermal warning/over current limit) setting which is address 0x37 of the user defined coefficient RAM.

7.1.5 Configuration register D (address 0x03)

D7	D6	D5	D4	D3	D2	D1	D0
MME	ZDE						
X	1	X	X	X	X	X	X

Zero-detect mute enable

Table 25. Zero detect mute enable

Bit	R/W	RST	Name	Description
6	R/W	1	ZDE	Setting of 1 enables the automatic zero-detect mute

Setting the ZDE bit enables the zero-detect automatic mute. The zero-detect circuit looks at the data for each processing channel at the output of the crossover (bass management)

filter. If any channel receives 2048 consecutive zero value samples (regardless of fs) then that individual channel is muted if this function is enabled.

7.1.6 Configuration register E (address 0x04)

D7	D6	D5	D4	D3	D2	D1	D0
SVE	ZCE	DCCV	PWMS	AME	NSBW	MPC	MPCV
1	1	0	0	0	0	1	0

Max power correction variable

Table 26. Max power correction variable

Bit	R/W	RST	Name	Description
0	R/W	1	MPCV	0: use standard MPC coefficient 1: use MPCC bits for MPC coefficient

Max power correction

Table 27. Max power correction

Bit	R/W	RST	Name	Description
1	R/W	1	MPC	Setting of 1 enables STA50x correction for THD reduction near maximum power output.

Setting the MPC bit turns on special processing that corrects the STA50x power device at high power. This mode should lower the THD+N of a full DDX system at maximum power output and slightly below. If enabled, MPC is operational in all output modes except tapered (OM[1:0] = 01) and binary. When OCFG = 00, MPC will not effect channels 3 and 4, the line-out channels.

Noise-shaper bandwidth selection

Table 28. Noise shaper bandwidth selection

Bit	R/W	RST	Name	Description
2	R/W	0	NSBW	1: 3rd order NS 0: 4th order NS

AM mode enable

Table 29. AM mode enable

Bit	R/W	RST	Name	Description
3	R/W	0	AME	0: normal DDX operation 1: AM reduction mode DDX operation

The STA333W features a DDX processing mode that minimizes the amount of noise generated in frequency range of AM radio. This mode is intended for use when DDX is operating in a device with an AM tuner active. The SNR of the DDX processing is reduced to ~83 dB in this mode, which is still greater than the SNR of AM radio.

PWM speed mode

Table 30. PWM speed mode

Bit	R/W	RST	Name	Description
4	R/W	0	PWMS	0: normal speed (384 kHz) all channels 1: odd speed (341.3 kHz) all channels

Distortion compensation variable enable

Table 31. Distortion compensation variable enable

Bit	R/W	RST	Name	Description
5	R/W	0	DCCV	0: uses preset DC coefficient. 1: uses DCC coefficient.

Zero-crossing volume enable

Table 32. Zero-crossing volume enable

Bit	R/W	RST	Name	Description
6	R/W	1	ZCE	1: volume adjustments will only occur at digital zero-crossings 0: volume adjustments will occur immediately

The ZCE bit enables zero-crossing volume adjustments. When volume is adjusted on digital zero-crossings no clicks will be audible.

Soft volume update enable

Table 33. Zero-crossing volume enable

Bit	R/W	RST	Name	Description
7	R/W	1	SVE	1: volume adjustments ramp according to SVR settings 0 : volume adjustments will occur immediately

7.1.7 Configuration register F(address 0x05)

D7	D6	D5	D4	D3	D2	D1	D0
EAPD	PWDN	ECLE	LDTE	BCLE	IDE		
0	1	0	1	1	1	X	X

Invalid Input detect mute enable

Table 34. Invalid input detect mute enable

Bit	R/W	RST	Name	Description
2	R/W	1	IDE	1: enables the automatic invalid input detect mute

Setting the IDE bit enables this function, which looks at the input I^2S data and will automatically mute if the signals are perceived as invalid.

Binary output mode clock loss detection

Table 35. Binary output mode clock loss detection

Bit	R/W	RST	Name	Description
3	R/W	1	BCLE	Binary output mode clock loss detection enable

Detects loss of input MCLK in binary mode and outputs 50% of the duty cycle.

LRCK double trigger protection

Table 36. LRCK double trigger protection

Bit	R/W	RST	Name	Description
4	R/W	1	LDTE	LRCLK double trigger protection enable

Actively prevents double trigger of LRCLK.

Auto EAPD on clock loss

Table 37. Auto EAPD on clock loss

Bit	R/W	RST	Name	Description
5	R/W	0	ECLE	Auto EAPD on clock loss

When active will issue a power device power down signal (EAPD) on clock loss detection.

IC power down

Table 38. Power down

Bit	R/W	RST	Name	Description
6	R/W	1	PWDN	0: IC power down low-power condition 1: IC normal operation

The PWDN register is used to place the IC in a low-power state. When PWDN is written as 0, the output will begin a soft-mute. After the mute condition is reached, EAPD will be asserted to power down the power-stage, then the master clock to all internal hardware expect the I^2C block will be gated. This places the IC in a very low power consumption state.

External amplifier power down

Table 39. External amplifier power down

Bit	R/W	RST	Name	Description
7	R/W	1	EAPD	0: external power stage power down active 1: normal operation

The EAPD register directly disables/enables the internal power circuitry.

When EAPD = 0, the internal power section is placed on a low-power state (disabled).

7.2 Volume control registers (addresses 0x06 - 0x0A)

7.2.1 Mute/line output configuration register

D7	D6	D5	D4	D3	D2	D1	D0
					C2M	C1M	MMUTE
					0	0	0

Master mute

Table 40. Master mute

Bit	R/W	RST	Name	Description
0	R/W	0	MMUTE	0: normal operation 1: all channels are in mute condition

Channel mute

Table 41. Channel mute

Bit	R/W	RST	Name	Description
1	R/W	0	C1M	Channel 1 mute: 0: no mute condition. It is possible to set the channel volume 1: Channel 1 in hardware mute
2	R/W	0	C2M	Channel 2 mute: 0: no Mute condition. It is possible to set the channel volume 1: Channel 2 in hardware mute

7.2.2 Master volume register

D7	D6	D5	D4	D3	D2	D1	D0
MV7	MV6	MV5	MV4	MV3	MV2	MV1	MV0
1	1	1	1	1	1	1	1

7.2.3 Channel 1 volume

D7	D6	D5	D4	D3	D2	D1	D0
C1V7	C1V6	C1V5	C1V4	C1V3	C1V2	C1V1	C1V0
0	1	1	0	0	0	0	0

7.2.4 Channel 2 volume

D7	D6	D5	D4	D3	D2	D1	D0
C2V7	C2V6	C2V5	C2V4	C2V3	C2V2	C2V1	C2V0
0	1	1	0	0	0	0	0

The volume structure of the STA333W consists of individual volume registers for each channel and a master volume register that provides an offset to each channels volume setting. The individual channel volumes are adjustable in 0.5 dB steps from +48 dB to - 80 dB. As an example if C3V = 0x00 or + 48 dB and MV = 0x18 or – 12 dB, then the total gain for channel 3 = + 36 dB.

The master mute when set to 1 will mute all channels at once, whereas the individual channel mutes(CxM) will mute only that channel. Both the master mute and the channel Mutes provide a “soft mute” with the volume ramping down to mute in 4096 samples from the maximum volume setting at the internal processing rate(~96 kHz). A “hard mute” can be obtained by commanding a value of all 1’s (255) to any channel volume register or the master volume register. When volume offsets are provided via the master volume register any channel that whose total volume is less than – 80 dB will be muted.

All changes in volume take place at zero-crossings when ZCE = 1 (configuration register F) on a per channel basis as this creates the smoothest possible volume transitions. When ZCE = 0, volume updates will occur immediately.

Table 42. Master volume offset as a function of MV[7:0]

MV(7..0)	Volume offset from channel value
00000000 (0x00)	0 dB
00000001 (0x01)	-0.5 dB
00000010 (0x02)	-1 dB
…	…
01001100 (0x4C)	-38 dB
…	…
11111110 (0xFE)	-127.5 dB
11111111 (0xFF)	Hard master mute

Table 43. Channel volume as a function of CxV[7:0]

CxV[7:0]	Volume
00000000 (0x00)	+48 dB
00000001 (0x01)	+47.5 dB
00000010 (0x02)	+47 dB
…	…
01011111 (0x5F)	+0.5 dB
01100000 (0x60)	0 dB
01100001 (0x61)	-0.5 dB

Table 43. Channel volume as a function of CxV[7:0] (continued)

…	…
11010111 (0xD7)	-59.5 dB
11011000 (0xD8)	-60 dB
11011001 (0xD9)	-61 dB
11011010 (0xDA)	-62 dB
…	…
11101100 (0xEC)	-80 dB
11101101 (0xED)	Hard channel mute
…	…
11111111 (0xFF)	Hard channel mute

7.3 Auto mode registers (0x0C)

7.3.1 Auto mode register 2 (address 0x0C)

D7	D6	D5	D4	D3	D2	D1	D0
XO3	XO2	XO1	XO0	AMAM2	AMAM1	AMAM0	AMAME
0	0	0	0	0	0	0	0

AM interference frequency switching

Table 44. AM interference frequency switching

Bit	R/W	RST	Name	Description
0	R/W	0	AMAME	0: switching frequency determined by PWMS setting 1: switching frequency determined by AMAM setting

AMAM bits

Table 45. AutoMode AM switching frequency selection

AMAM[2:0]	48 kHz / 96 kHz input Fs	44.1 kHz / 88.2 kHz input Fs
000	0.535 MHz – 0.720 MHz	0.535 MHz – 0.670 MHz
001	0.721 MHz – 0.900 MHz	0.671 MHz – 0.800 MHz
010	0.901 MHz – 1.100 MHz	0.801 MHz – 1.000 MHz
011	1.101 MHz – 1.300 MHz	1.001 MHz – 1.180 MHz
100	1.301 MHz – 1.480 MHz	1.181 MHz – 1.340 MHz
101	1.481 MHz – 1.600 MHz	1.341 MHz – 1.500 MHz
110	1.601 MHz – 1.700 MHz	1.501 MHz – 1.700 MHz

7.4 Channel configuration registers (addresses 0x0E-0x0F)

7.4.1 0x0E

D7	D6	D5	D4	D3	D2	D1	D0
					C1VPB		
					0		

7.4.2 0x0F

D7	D6	D5	D4	D3	D2	D1	D0
					C2VPB		
					0		

Volume bypass

Each channel contains an individual channel volume bypass. If a particular channel has volume bypassed via the CxVBP = 1 register then only the channel volume setting for that particular channel affects the volume setting, the master volume setting will not affect that channel.

7.5 Variable max power correction registers (addresses 0x27-0x29)

MPCC bits determine the 16 MSBs of the MPC compensation coefficient. This coefficient is used in place of the default coefficient when MPCV = 1.

7.5.1 Variable max power correction registers (bits [15:8])

D7	D6	D5	D4	D3	D2	D1	D0
MPCC15	MPCC14	MPCC13	MPCC12	MPCC11	MPCC10	MPCC9	MPCC8
0	0	0	1	1	0	1	0

7.5.2 Variable max power correction registers (bits [7:0])

D7	D6	D5	D4	D3	D2	D1	D0
MPCC7	MPCC6	MPCC5	MPCC4	MPCC3	MPCC2	MPCC1	MPCC0
1	1	0	0	0	0	0	0

7.6 Variable distortion compensation registers (addresses 0x29 - 0x2A)

DCC bits determine the 16 MSBs of the Distortion compensation coefficient. This coefficient is used in place of the default coefficient when DCCV = 1.

7.6.1 Variable distortion compensation register (bits [15:8])

D7	D6	D5	D4	D3	D2	D1	D0
DCC15	DCC14	DCC13	DCC12	DCC11	DCC10	DCC9	DCC8
1	1	1	1	0	0	1	1

7.6.2 Variable distortion compensation register (bits [7:0])

D7	D6	D5	D4	D3	D2	D1	D0
DCC7	DCC6	DCC5	DCC4	DCC3	DCC2	DCC1	DCC0
0	0	1	1	0	0	1	1

7.7 Fault detect recovery constant registers (addresses 0x2B - 0x2C)

FDRC bits specify the 16-bit fault detect recovery time delay. When FAULT is asserted, the TRISTATE output will be immediately asserted low and held low for the time period specified by this constant. A constant value of 0x0001 in this register is approximately 0.083 ms. The default value of 0x000C specifies approximately 0.1 ms.

7.7.1 Fault detect recovery constant register (bits [15:8])

D7	D6	D5	D4	D3	D2	D1	D0
FDRC15	FDRC14	FDRC13	FDRC12	FDRC11	FDRC10	FDRC9	FDRC8
0	0	0	0	0	0	0	0

7.7.2 Fault detect recovery constant register (bits [7:0])

D7	D6	D5	D4	D3	D2	D1	D0
FDRC7	FDRC6	FDRC5	FDRC4	FDRC3	FDRC2	FDRC1	FDRC0
0	0	0	0	1	1	0	0

7.8 Device status register (address 0x2D)

7.8.1 Device status register

D7	D6	D5	D4	D3	D2	D1	D0
PLLUL	FAULT	UVFAULT	OVFAULT	OCFAULT	OCWARN	TFAULT	TWARN

This read-only register provides fault and thermal-warning status information from the power control block.

7.9 Reserved registers (address 0x2E – 0x31)

7.9.1 Reserved register (0x2E)

D7	D6	D5	D4	D3	D2	D1	D0
RES	RES	RES	RES	RES	RES	RES	RES

7.9.2 Reserved register (0x2F)

D7	D6	D5	D4	D3	D2	D1	D0
RES	RES	RES	RES	RES	RES	RES	RES

7.9.3 Reserved register (0x30)

D7	D6	D5	D4	D3	D2	D1	D0
RES	RES	RES	RES	RES	RES	RES	RES

7.9.4 Reserved register (0x31)

D7	D6	D5	D4	D3	D2	D1	D0
RES	RES	RES	RES	RES	RES	RES	RES

7.10 Post scale registers (address 0x32 – 0x33)

7.10.1 Channel 1 post scale

D7	D6	D5	D4	D3	D2	D1	D0
C1PS7	C1PS6	C1PS5	C1PS4	C1PS3	C1PS2	C1PS1	C1PS0
0	1	1	1	1	1	1	1

7.10.2 Channel 2 post scale

D7	D6	D5	D4	D3	D2	D1	D0
C2PS7	C2PS6	C2PS5	C2PS4	C2PS3	C2PS2	C2PS1	C2PS0
0	1	1	1	1	1	1	1

The STA333W provides one additional multiplication after the last interpolation stage and the distortion compensation on each channel, which can be used to limit the maximum modulation index and therefore the peak current through the power device. The register values represent an 8-bit signed fractional number. This number is extended to a 24-bit number by adding zeros to the right and then directly multiplied by the data on that channel. An independent post-scale is provided for each channel but all channels can use the channel 1 post-scale factor by setting the post-scale link bit. By default, all post-scale factors are set to 0x7F (pass-through).

7.11 Output limit register (address 0x34)

7.11.1 Thermal and over-current warning output limit register

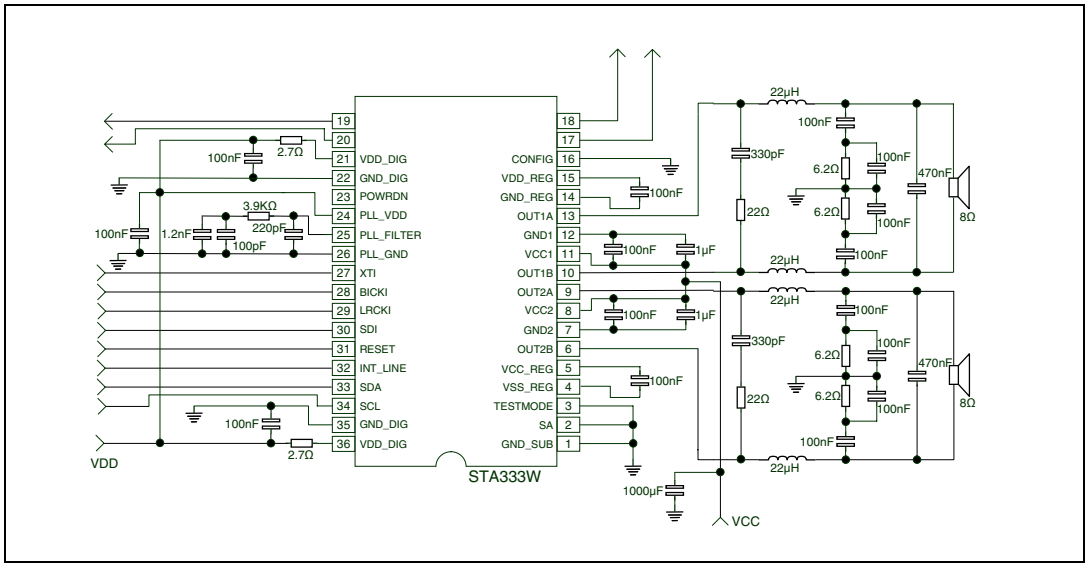
D7	D6	D5	D4	D3	D2	D1	D0
OLIM7	OLIM6	OLIM5	OLIM4	OLIM3	OLIM2	OLIM1	OLIM0
0	1	0	1	1	0	1	0

The STA333W provides a simple mechanism for reacting to a thermal or over-current warning in the power-device. When the TWARN or OCWARN input is asserted, the OLIM setting is used to limit the output to that value. The default setting of 0x5A provides -3dB limit. The limit in this situation can be adjusted by modifying the thermal warning/over-current output limit value.

If the cause of the limiting was a thermal warning, the output limiting is removed when the thermal warning situation disappears. If the cause of the limiting was an over-current warning, the output limiting remains in effect until the device is reset.

8 Application

Figure 14. Application diagram

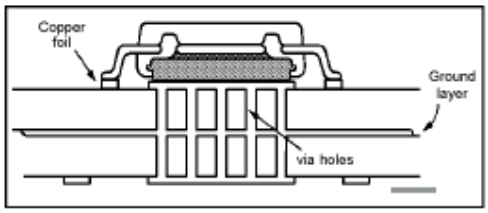


9 Package thermal characteristics

A thermal resistance of 25° C/W can be achieved using a ground copper area of 3 x 3 cm, and using 16 vias, on the PCB (see *Figure 15*). The amount of power dissipated within the device depends primarily on the supply voltage, load impedance and output modulation level.

The max estimated dissipated power for the STA333W is 3 W. This gives, with the suggested board copper area, a maximum ΔTj of 75 °C. This gives a safety margin before the thermal protection intervention is invoked (T_j = 150 °C) in consumer environments where a 50 °C is the maximum ambient temperature.

Figure 15. Thermal characteristics



10 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

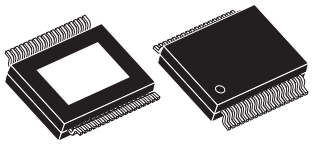
ECOPACK specifications are available at: www.st.com.

Figure 16. PowerSSO36 slug down package information

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.15		2.47	0.084		0.097
A2	2.15		2.40	0.084		0.094
a1	0		0.075	0		0.003
b	0.18		0.36	0.007		0.014
c	0.23		0.32	0.009		0.012
D (1)	10.10		10.50	0.398		0.413
E (1)	7.4		7.6	0.291		0.299
e		0.5			0.019	
e3		8.5			0.335	
F		2.3			0.090	
G			0.10			0.004
G1			0.06			0.002
H	10.10		10.50	0.398		0.413
h			0.40			0.016
k		5°			5°	
L	0.55		0.90	0.022		0.035
M		4.3			0.169	
N			10°			10°
O		1.2			0.047	
Q		0.8			0.031	
S		2.9			0.114	
T		3.65			0.144	
U		1.0			0.039	
X	4.1		4.7	0.161		0.185
Y	6.5		7.3	0.256		0.287

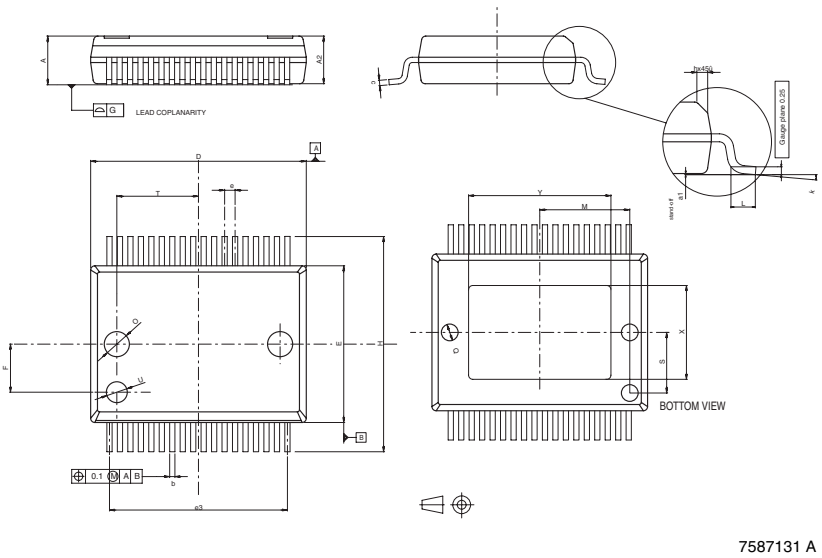
(1) "D" and "E" do not include mold flash or protrusions Mold flash or protrusions shall not exceed 0.15 mm per side(0.006")

Outline and mechanical data



PowerSSO-36

Exposed pad (or slug) down



11 Trademarks and other acknowledgements

DDX is a registered trademark of Apogee Technology Inc.

ECOPACK is a registered trademark of STMicroelectronics.

Sound Terminal is a trademark of STMicroelectronics.

12 Revision history

Table 46. Document revision history

Date	Revision	Changes
25-May-2007	1	Initial release.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com