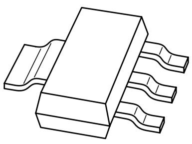


BUK7880-55A

N-channel TrenchMOS standard level FET

Rev. 01 — 1 November 2007 **Product data sheet**

1. Product profile

1.1 General description

N-channel enhancement mode power Field-Effect Transistor (FET) in a plastic package using NXP General Purpose Automotive (GPA) TrenchMOS technology.

1.2 Features

- Very low on-state resistance
- 150 °C rated
- Q101 compliant
- Standard level compatible

1.3 Applications

- Automotive systems
- Motors, lamps and solenoids
- General purpose power switching
- 12 V and 24 V loads

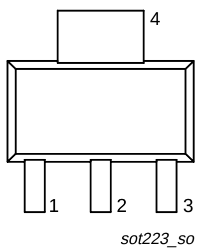
1.4 Quick reference data

- $E_{DS(AL)S} \leq 53$ mJ
- $I_D \leq 7$ A
- $R_{DSon} = 68$ mΩ (typ)
- $P_{tot} \leq 8$ W

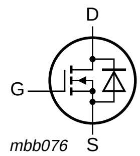
2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1	gate (G)		
2	drain (D)		
3	source (S)		
4	solder point; connected to drain (D)		



SOT223 (SC-73)



3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
BUK7880-55A	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223

4. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage			-	55	V
V_{DGR}	drain-gate voltage (DC)	R_{GS} = 20 kΩ		-	55	V
V_{GS}	gate-source voltage			-	±20	V
I_D	drain current	T_{sp} = 25 °C; V_{GS} = 10 V; see Figure 2 and 3		-	7	A
		T_{sp} = 100 °C; V_{GS} = 10 V; see Figure 2		-	5	A
I_{DM}	peak drain current	T_{sp} = 25 °C; pulsed; $t_p \leq 10$ µs; see Figure 3		-	30	A
P_{tot}	total power dissipation	T_{sp} = 25 °C; see Figure 1		-	8	W
T_{stg}	storage temperature			–55	+150	°C
T_j	junction temperature			–55	+150	°C
Source-drain diode						
I_{DR}	reverse drain current	T_{sp} = 25 °C		-	7	A
I_{DRM}	peak reverse drain current	T_{sp} = 25 °C; pulsed; $t_p \leq 10$ µs		-	30	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; I_D = 7 A; $V_{DS} \leq 55$ V; R_{GS} = 50 Ω; V_{GS} = 10 V; starting at T_j = 25 °C		-	53	mJ
$E_{DS(AL)R}$	repetitive drain-source avalanche energy		[1]	-	-	J

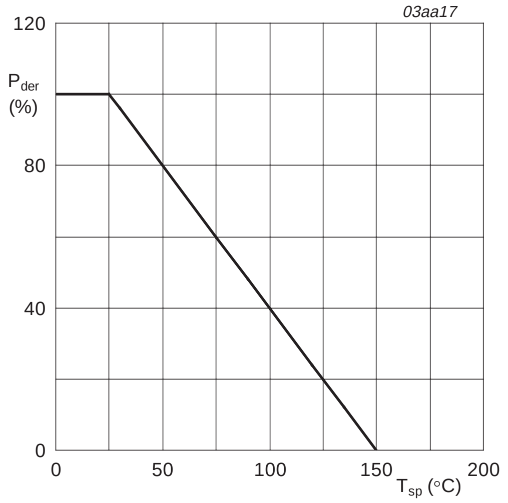
[1] Conditions:

a) Maximum value not quoted. Repetitive rating defined in Figure 16.

b) Single-pulse avalanche rating limited by $T_{j(max)}$ of 150 °C.

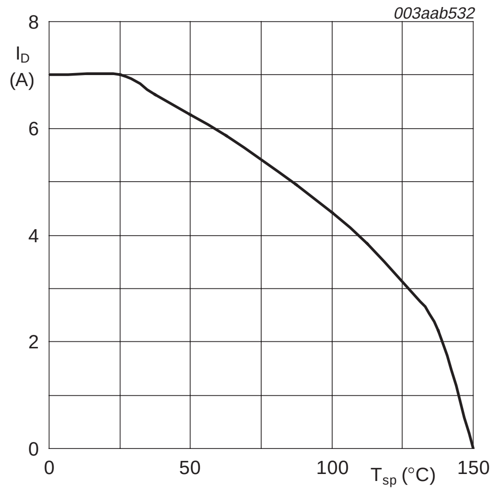
c) Repetitive avalanche rating limited by an average junction temperature of 150 °C.

d) Refer to application note *AN10273* for further information.



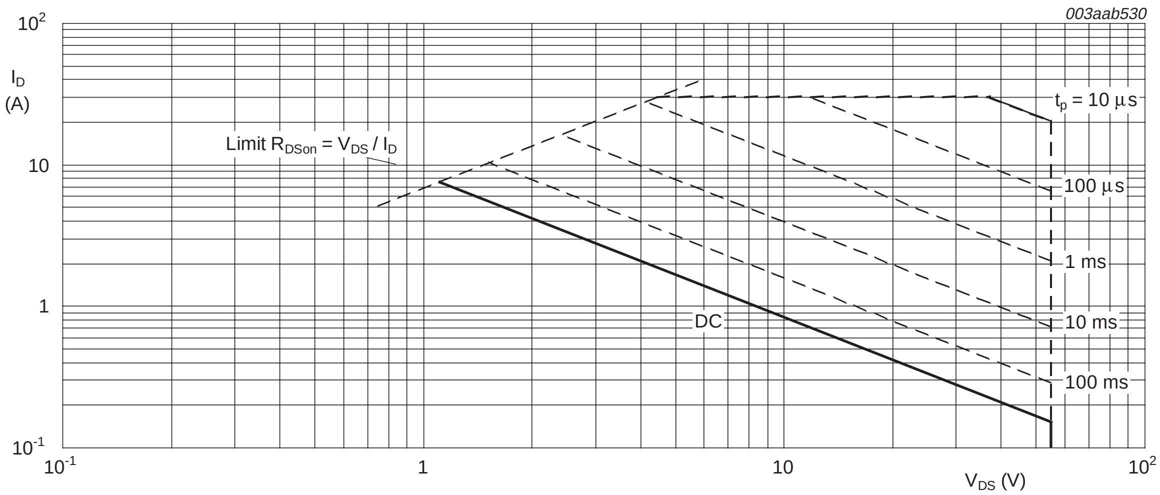
$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature



$V_{GS} \geq 10$ V

Fig 2. Continuous drain current as a function of solder point temperature



T_{sp} = 25 °C; I_{DM} is single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		-	70	-	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	15	K/W

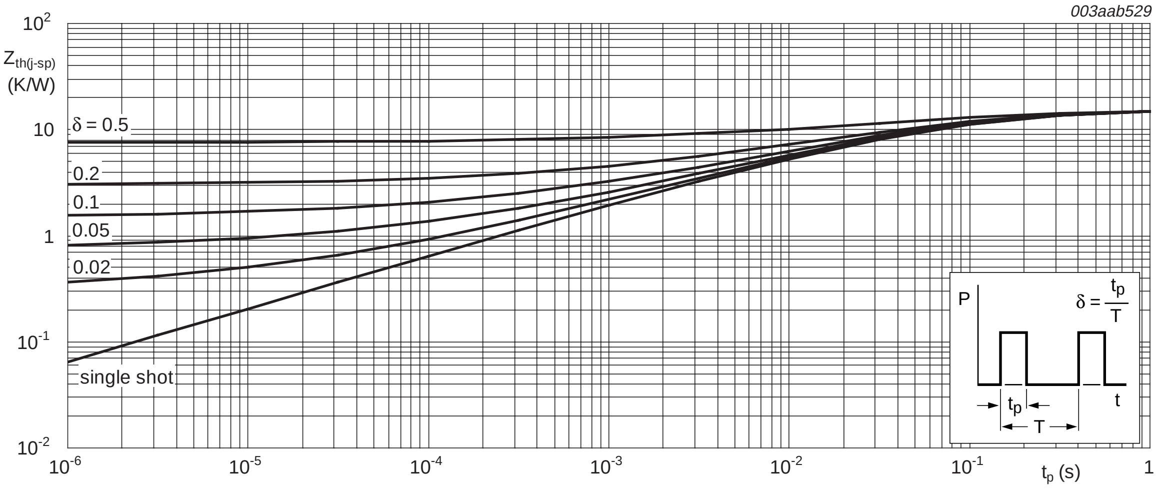


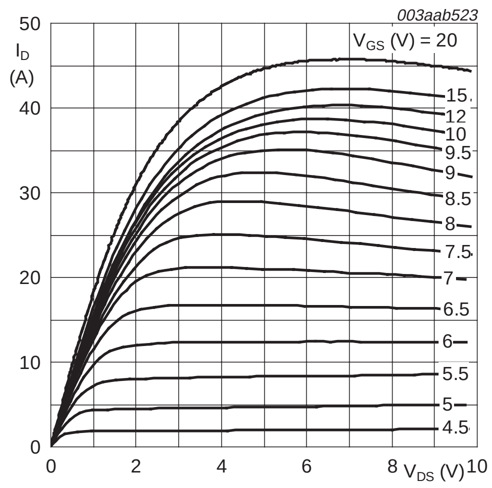
Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

6. Characteristics

Table 5. Characteristics

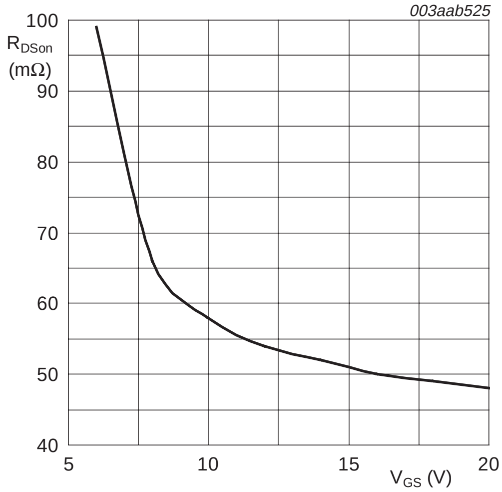
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V				
		T_j = 25 °C	55	-	-	V
		T_j = –55 °C	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; see Figure 9				
		T_j = 25 °C	2	3	4	V
		T_j = 150 °C	1.2	-	-	V
		T_j = –55 °C	-	-	4.4	V
I_{DSS}	drain leakage current	V_{DS} = 55 V; V_{GS} = 0 V				
		T_j = 25 °C	-	0.05	10	µA
		T_j = 150 °C	-	-	500	µA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 10 A; see Figure 6 and 8				
		T_j = 25 °C	-	68	80	mΩ
		T_j = 150 °C	-	-	148	mΩ
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 10 A; V_{DD} = 44 V; V_{GS} = 10 V; see Figure 14	-	12	-	nC
Q_{GS}	gate-source charge		-	2.5	-	nC
Q_{GD}	gate-drain charge		-	5	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; see Figure 12	-	374	500	pF
C_{oss}	output capacitance		-	92	110	pF
C_{rss}	reverse transfer capacitance		-	62	85	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 10 V; R_G = 10 Ω	-	8	-	ns
t_r	rise time		-	52	-	ns
$t_{d(off)}$	turn-off delay time		-	17	-	ns
t_f	fall time		-	9	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 15 A; V_{GS} = 0 V; see Figure 15	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = –100 A/µs; V_{GS} = –10 V; V_R = 30 V	-	33	-	ns
Q_r	recovered charge		-	31	-	nC



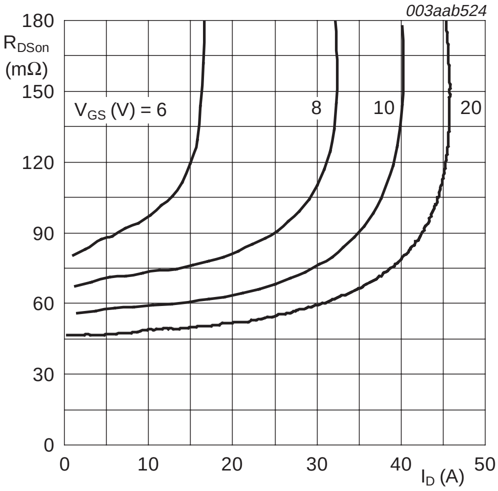
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



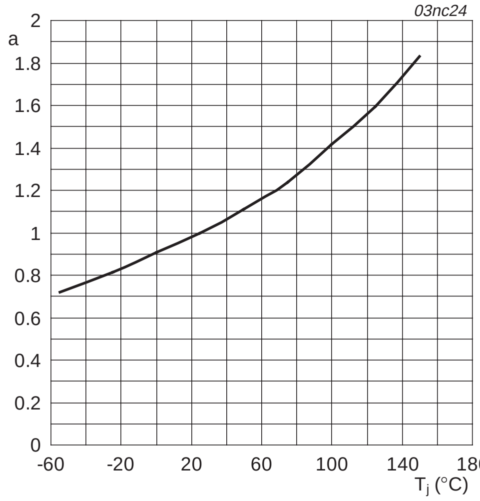
T_j = 25 °C; I_D = 10 A

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values



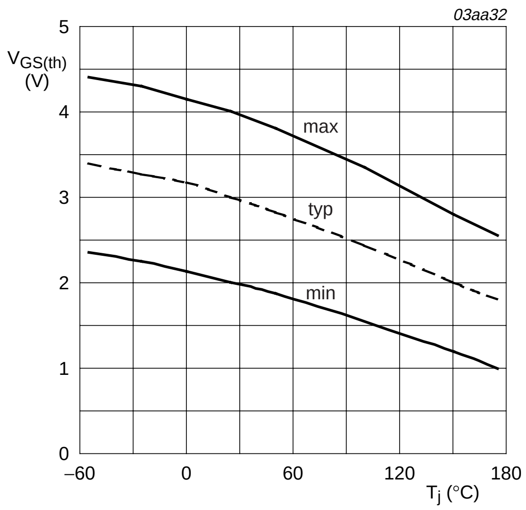
T_j = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values



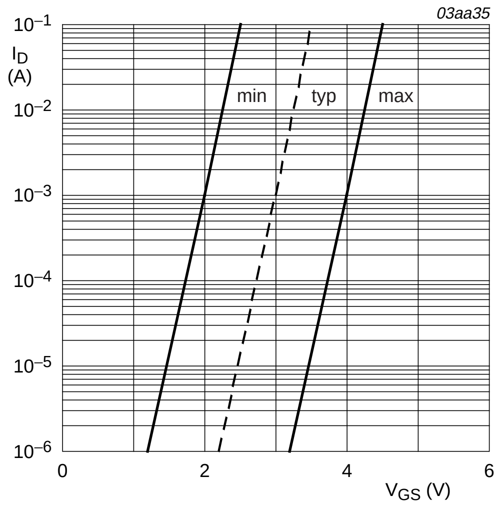
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



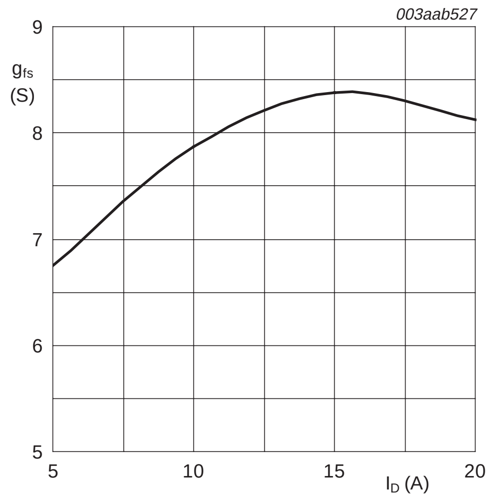
I_D = 1 mA; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



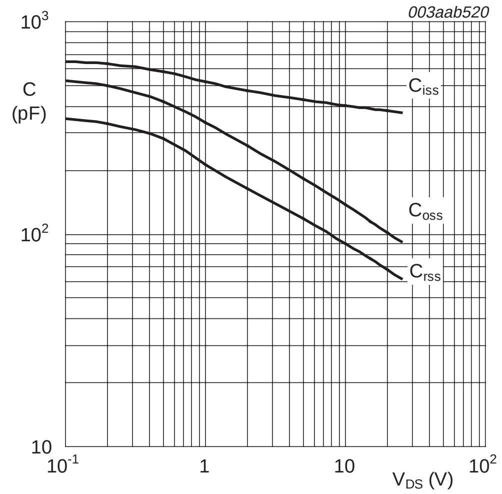
T_j = 25 °C; $V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



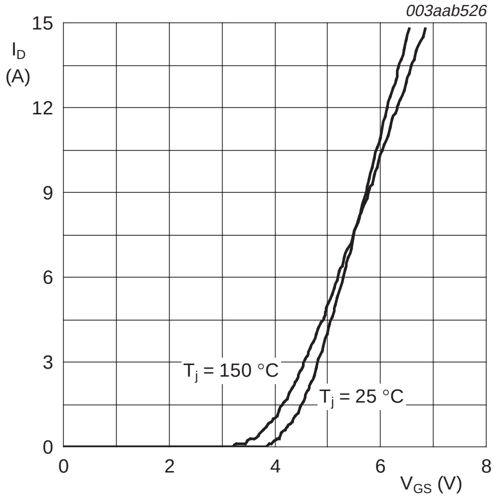
T_j = 25 °C; V_{DS} = 15 V

Fig 11. Forward transconductance as a function of drain current; typical values



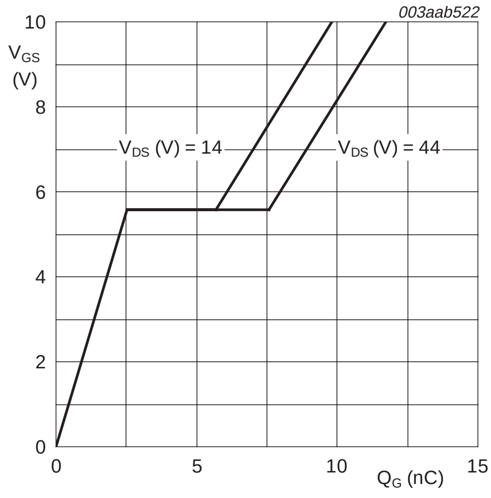
V_{GS} = 0 V; f = 1 MHz

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



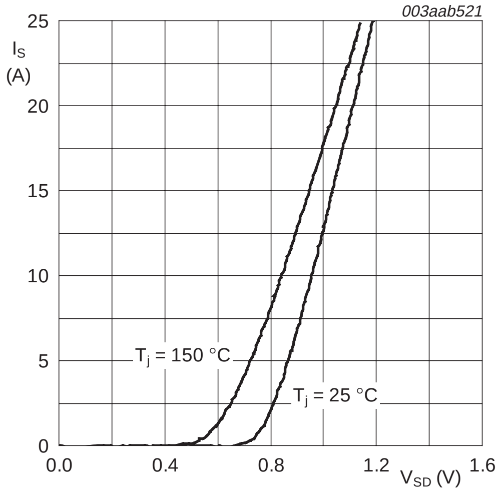
V_{DS} = 15 V

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values



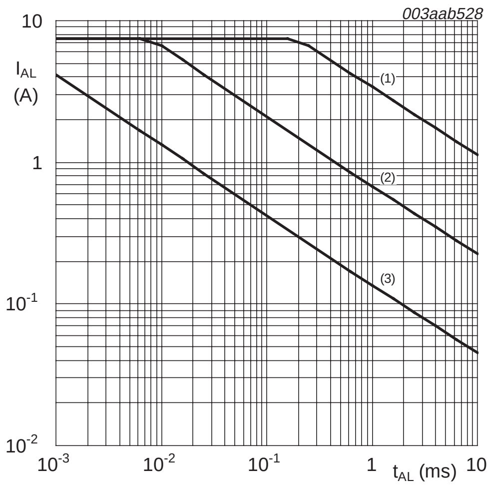
T_j = 25 °C; I_D = 10 A

Fig 14. Gate-source voltage as a function of gate charge; typical values



V_{GS} = 0 V

Fig 15. Source current as a function of source-drain voltage; typical values



See Table note 1 of Table 3 Limiting values.

(1) Single-pulse; T_j = 25 °C.

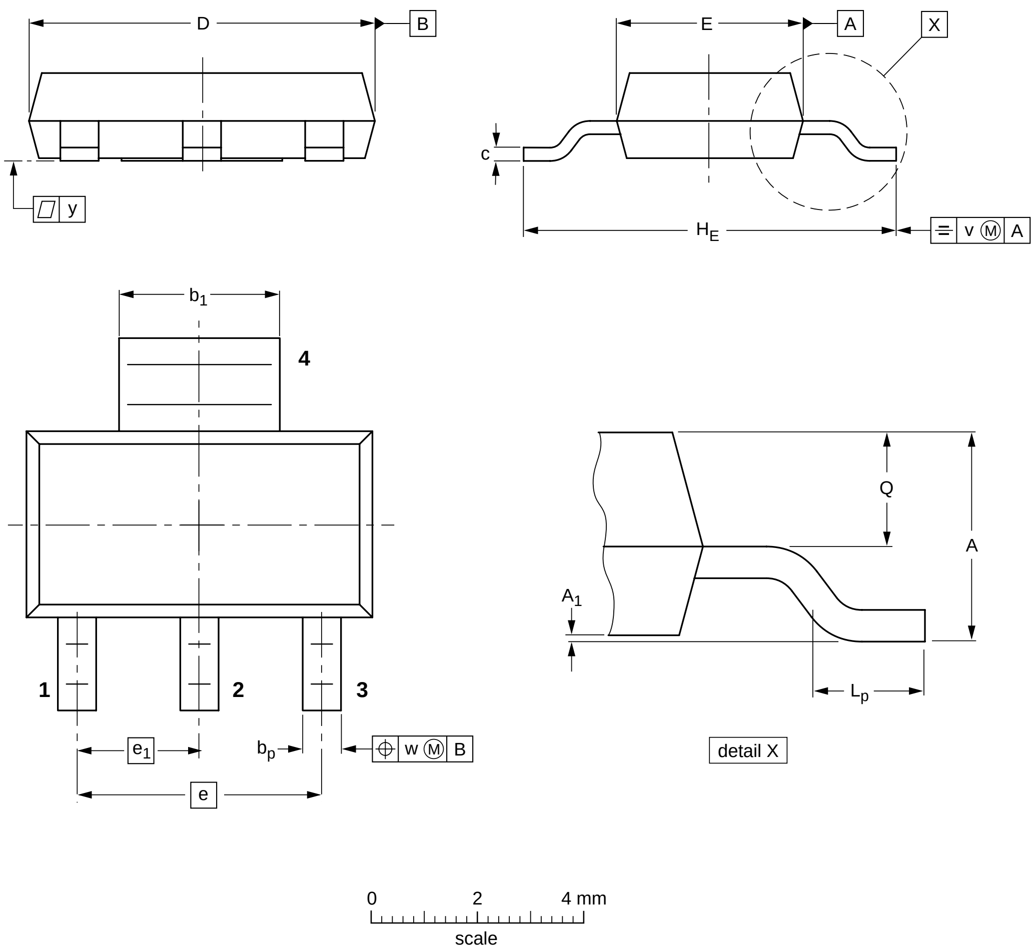
(2) Single-pulse; T_j = 150 °C.

(3) Repetitive.

Fig 16. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time

7. Package outline

Plastic surface-mounted package with increased heatsink; 4 leads **SOT223**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT223			SC-73			~~04-11-10~~ 06-03-16

Fig 17. Package outline SOT223 (SC-73)

8. Soldering

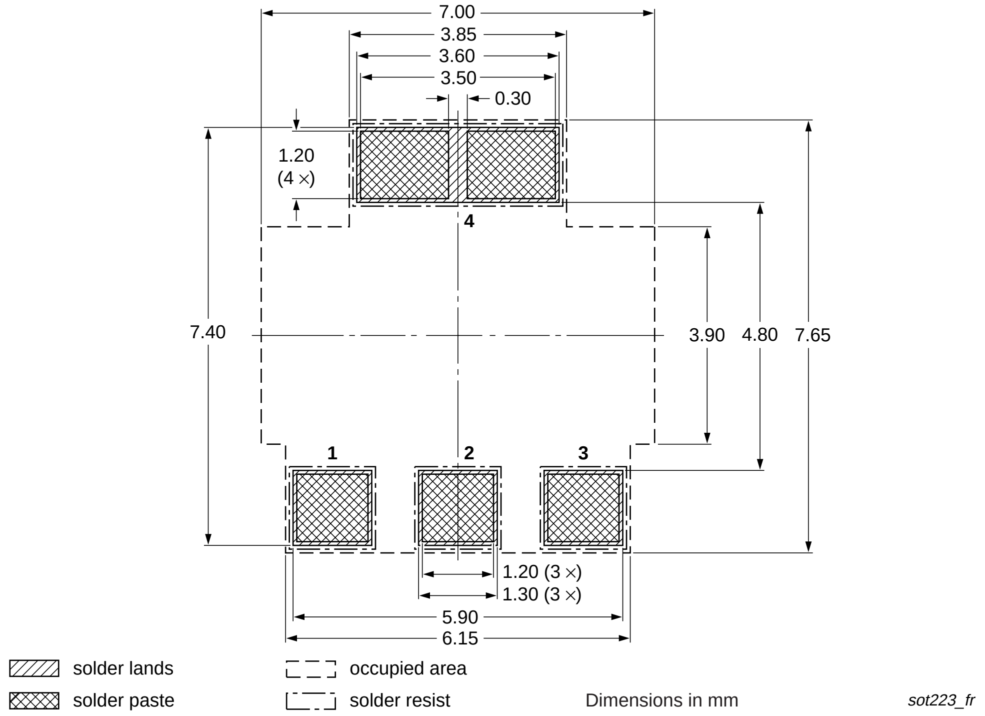


Fig 18. Reflow soldering footprint for SOT223 (SC-73)

9. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK7880-55A_1	20071101	Product data sheet	-	-

10. Legal information

10.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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12. Contents

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