

H5N5006DL, H5N5006DS

Silicon N Channel MOS FET
High Speed Power Switching

REJ03G0397-0100

Rev.1.00

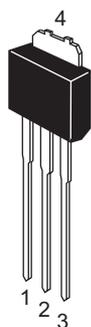
May 30, 2006

Features

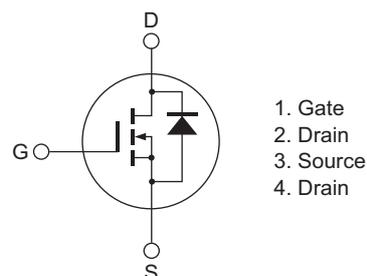
- Low on-resistance: $R_{DS(on)} = 2.5 \Omega$ typ.
- Low leakage current: $I_{DSS} = 1 \mu A$ max. (at $V_{DS} = 500 V$)
- High speed switching: $t_f = 15 ns$ typ. (at $V_{GS} = 10 V$, $V_{DD} \cong 250 V$, $I_D = 1.5 A$)
- Low gate charge: $Q_g = 14 nC$ typ. (at $V_{DD} = 400 V$, $V_{GS} = 10 V$, $I_D = 3 A$)
- Avalanche ratings

Outline

RENESAS Package code: PRSS0004ZD-B
(Package name: DPAK (L)-(2))



RENESAS Package code: PRSS0004ZD-C
(Package name: DPAK (S))



Absolute Maximum Ratings

($T_a = 25^\circ C$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	500	V
Gate to source voltage	V_{GSS}	± 30	V
Drain current	I_D	3	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	12	A
Body-drain diode reverse drain current	I_{DR}	3	A
Body-drain diode reverse drain peak current	$I_{DR(pulse)}$ ^{Note1}	12	A
Avalanche current	I_{AP} ^{Note3}	3	A
Channel dissipation	P_{ch} ^{Note2}	30	W
Channel to case thermal impedance	θ_{ch-c}	4.17	$^\circ C/W$
Channel temperature	T_{ch}	150	$^\circ C$
Storage temperature	T_{stg}	-55 to +150	$^\circ C$

Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$

2. Value at $T_c = 25^\circ C$

3. $ST_{ch} = 25^\circ C$, $T_{ch} \leq 150^\circ C$

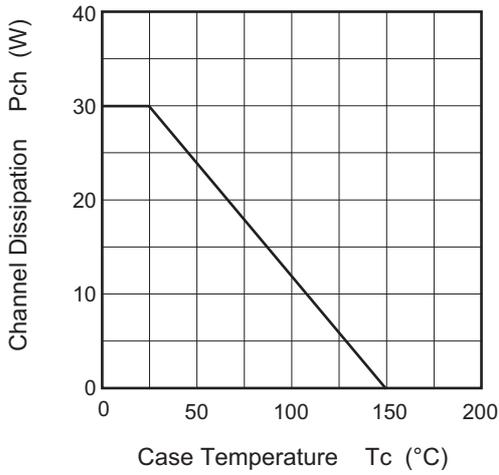
Electrical Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	500	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 500 \text{ V}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 30 \text{ V}$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	3.0	—	4.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Forward transfer admittance	$ y_{fs} $	1.5	2.5	—	S	$I_D = 1.5 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note4}
Static drain to source on state resistance	$R_{DS(on)}$	—	2.5	3.0	Ω	$I_D = 1.5 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	365	—	pF	$V_{DS} = 25 \text{ V}$
Output capacitance	C_{oss}	—	35	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	8	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	20	—	ns	$V_{DD} \cong 250 \text{ V}$, $I_D = 1.5 \text{ A}$
Rise time	t_r	—	12	—	ns	$V_{GS} = 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	48	—	ns	$R_L = 167 \Omega$
Fall time	t_f	—	15	—	ns	$R_g = 10 \Omega$
Total gate charge	Q_g	—	14	—	nC	$V_{DD} = 400 \text{ V}$
Gate to source charge	Q_{gs}	—	2	—	nC	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Q_{gd}	—	8	—	nC	$I_D = 3 \text{ A}$
Body-drain diode forward voltage	V_{DF}	—	0.85	1.3	V	$I_F = 3 \text{ A}$, $V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	270	—	ns	$I_F = 3 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$
Body-drain diode reverse recovery charge	Q_{rr}	—	0.8	—	μC	

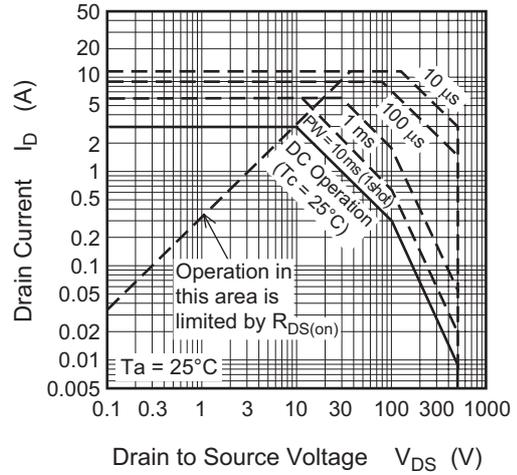
Notes: 4. Pulse test

Main Characteristics

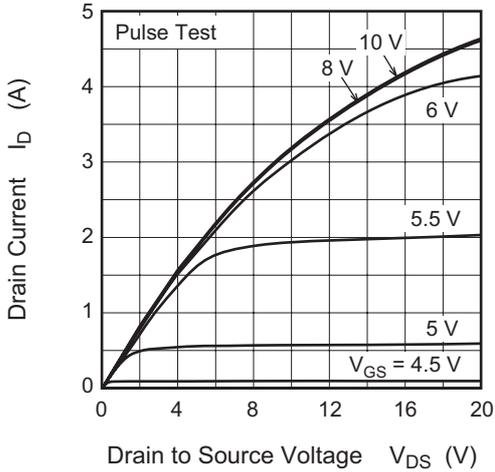
Power vs. Temperature Derating



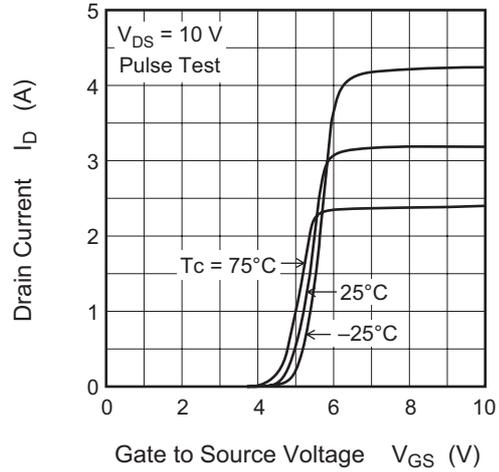
Maximum Safe Operation Area



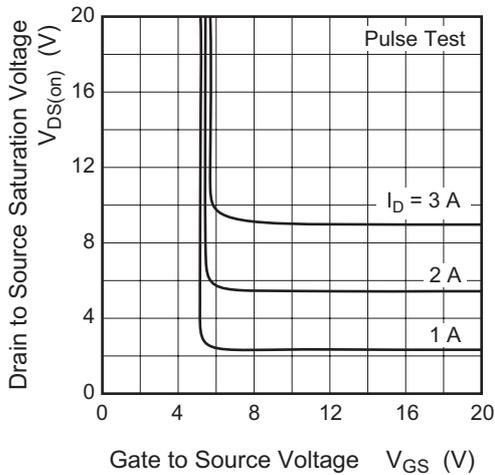
Typical Output Characteristics



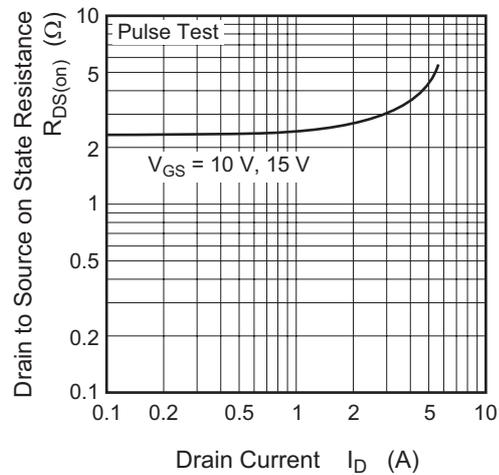
Typical Transfer Characteristics

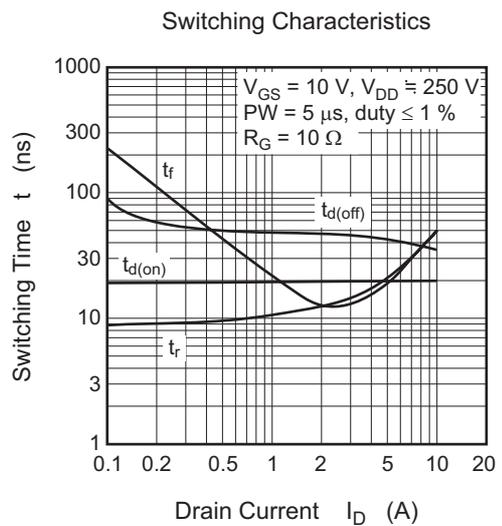
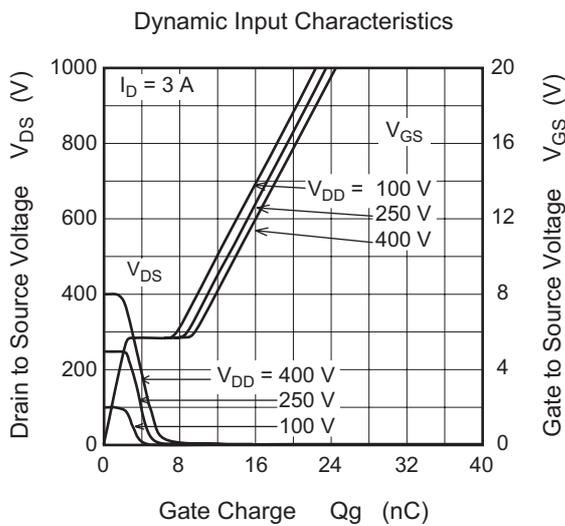
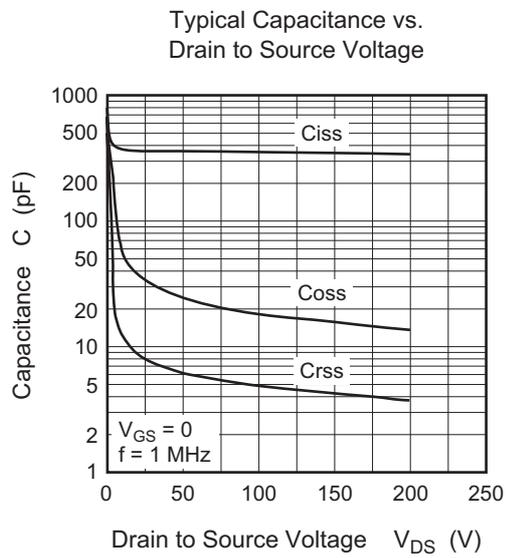
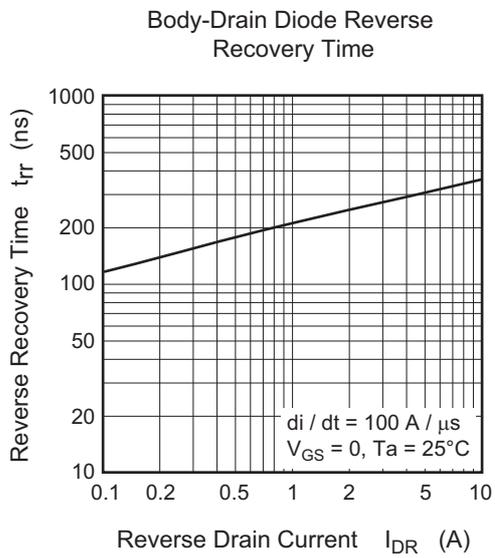
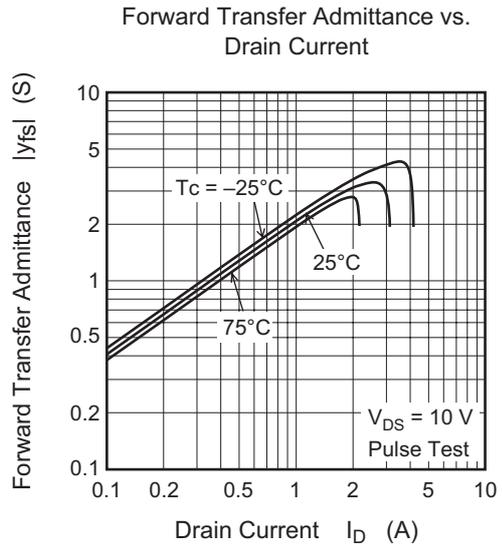
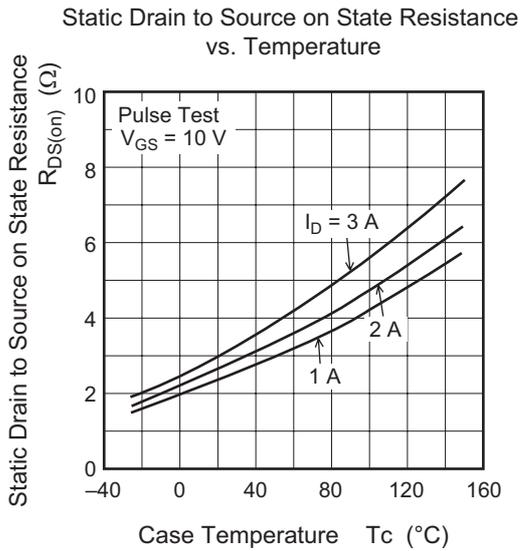


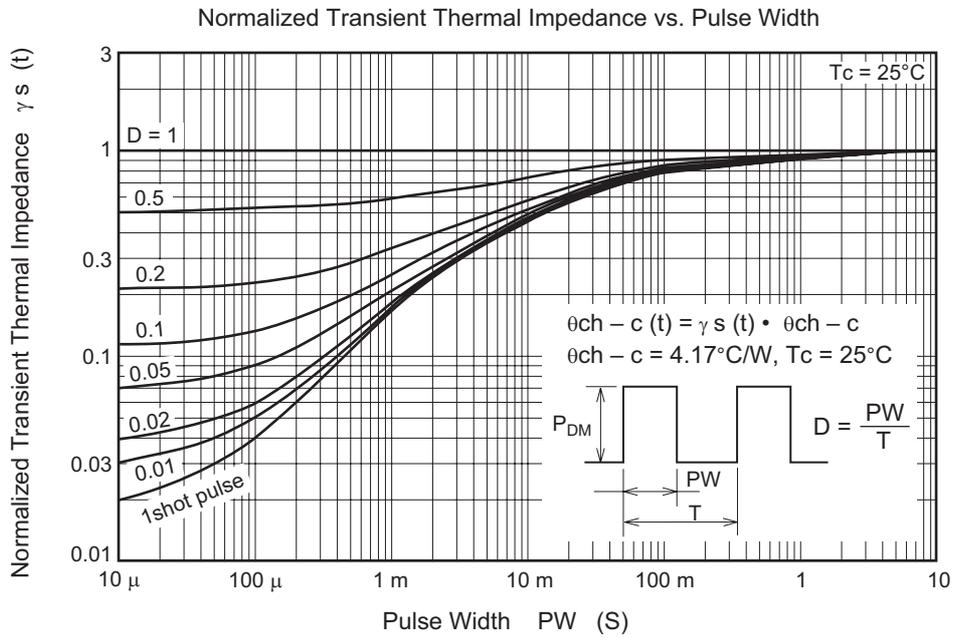
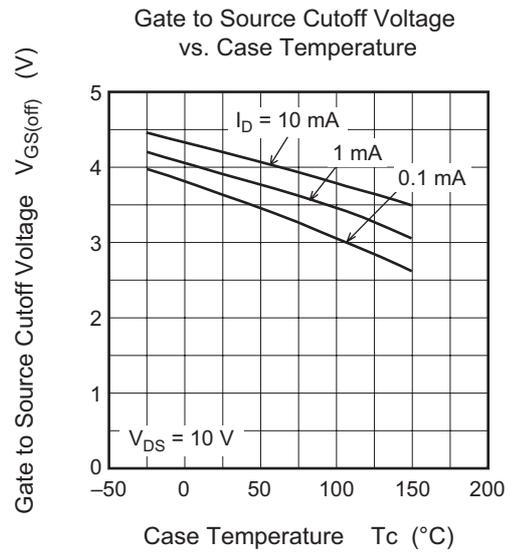
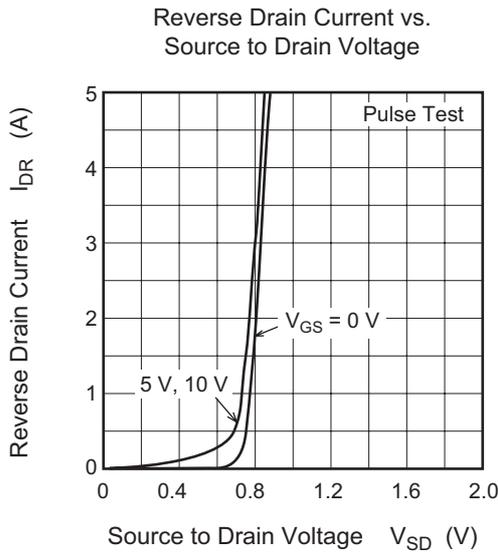
Drain to Source Saturation Voltage vs. Gate to Source Voltage



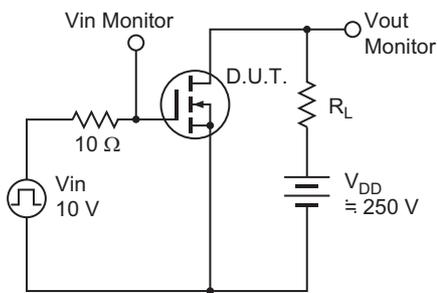
Static Drain to Source on State Resistance vs. Drain Current



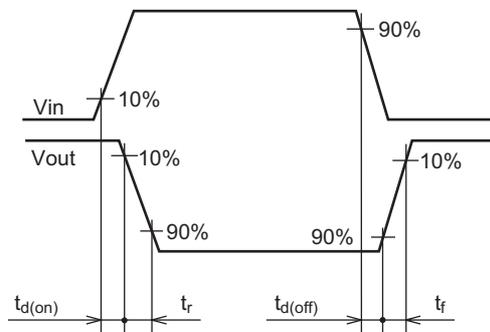




Switching Time Test Circuit

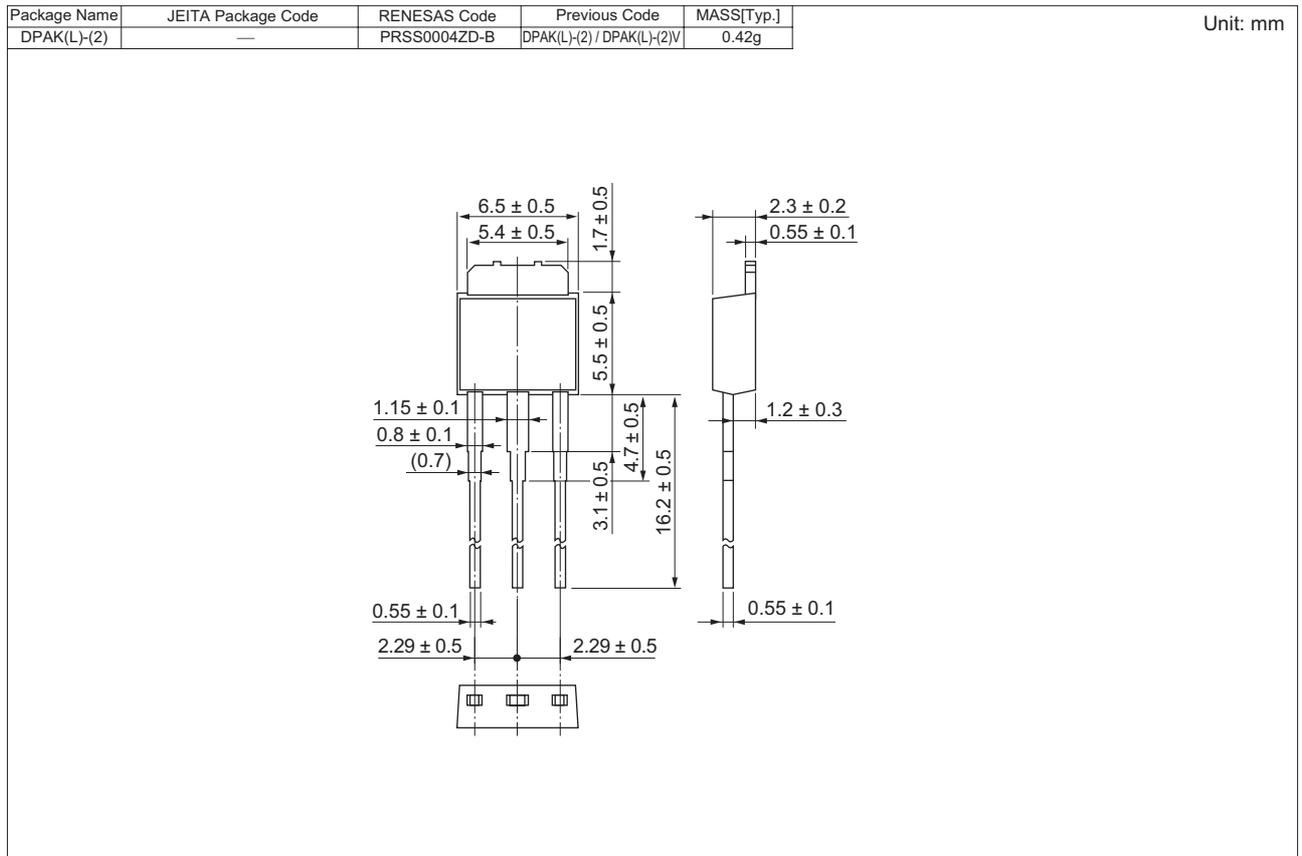


Waveform

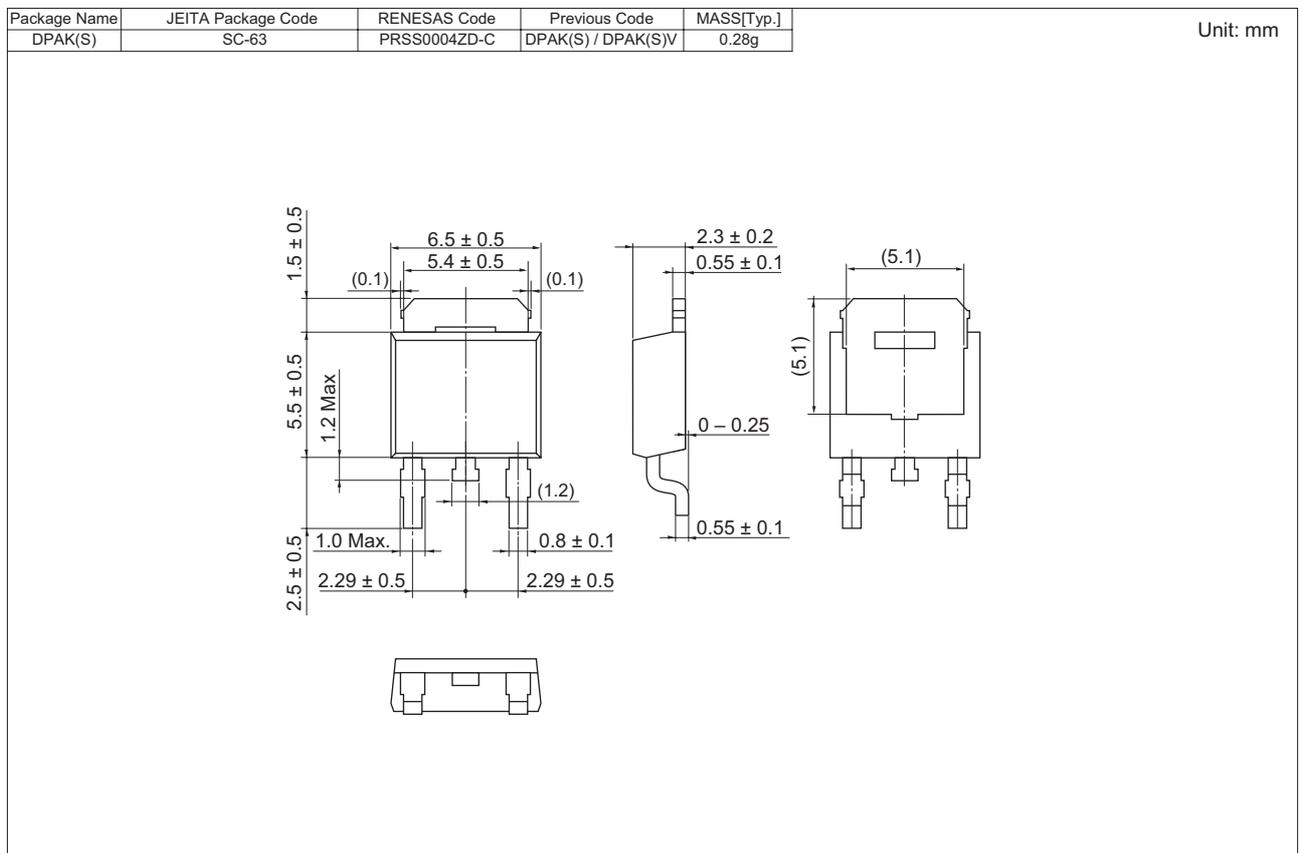


Package Dimensions

• H5N5006DL



• H5N5006DS



Ordering Information

Part Name	Quantity	Shipping Container
H5N5006DL-E	3200 pcs	Box (Sack)
H5N5006DSTL-E	3000 pcs	Taping

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