CAST

CZ80CPU

8-bit Microprocessor Core

Actel CompanionCore

General Description

Implements a fast, fully-functional, single-chip, 8-bit microprocessor with the same instruction set as the Z80.

The core has a 16-bit address bus capable of directly accessing 64kB of memory space. It has 252 root instructions with the reserved 4 bytes as prefixes, and accesses an additional 308 instructions. The microcode-free design is strictly synchronous, with no internal tri-states and a synchronous reset.

Developed for easy reuse in Actel FPGA applications, the CZ80CPU is available optimized for several device families with competitive utilization and performance characteristics.

Symbol
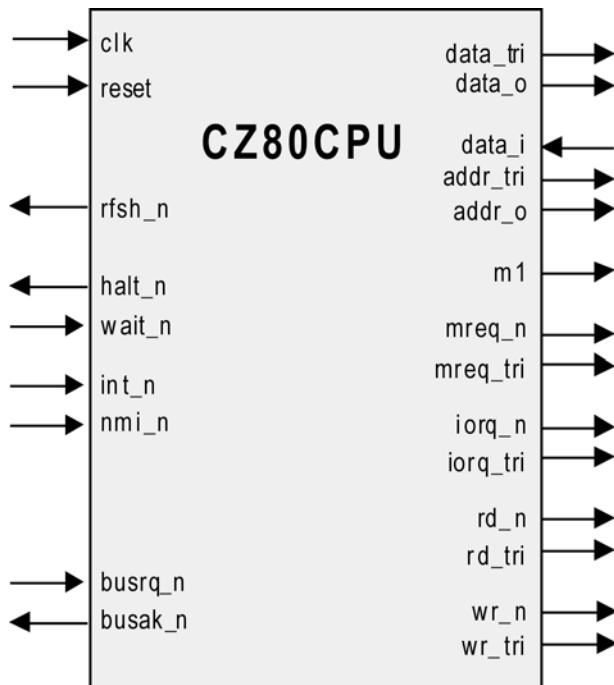
Features

Programming features contain 208 bits of read/write memory that are accessible to the programmer. The internal registers include an accumulator and six 8-bit registers that can be paired as three 16-bit registers. In addition to general registers, a 16-bit stack-pointer, 16-bit program-counter, and two 16-bit index registers are provided.

- Control Unit
  - 8-bit Instruction decoder
- Arithmetic-Logic Unit
  - 8-bit arithmetic and logical operations
  - 16-bit arithmetic operations
  - Boolean manipulations
- Register File Unit
  - Duplicate set of both general purpose and flag registers
  - Two 16-bit index registers
- Interrupt Controller
  - Three modes of maskable interrupts
  - Non maskable interrupt
- External Memory interface
  - Can address up to 64 KB of program memory
  - Can address up to 64 KB of data memory
  - Can address up to 64 KB of input/output devices
- On-core dynamic memory refresh counter

Applications

Suitable for many embedded controller applications, including industrial control systems, point-of-sale terminals, and automotive controls.

Performance

The CZ80CPU is a technology-independent design that can be implemented in a variety of process technologies. Results with representative Actel devices are shown in Table 1.

Family	Device (-speed grade)	Utilization (Cells or Tiles)		
		Sequential	Combinatorial	Total
ProASIC^{PLUS}	APA750-STD	391 Tiles	8014 Tiles	26%
Axcelerator	AX1000-3	479	6298	38%

Table 1: Utilization Table for CZ80CPU Core implemented in Actel Devices

Deliverables

- Post-synthesis EDIF netlist (source code versions are also available; contact CAST)
- Extensive testbench
- Simulation vectors and expected results
- Place and route scripts
- Detailed user's documentation

Verification Methods

The CZ80CPU core's functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model that contained the original Zilog Z84C00 chip, and the results compared with the core's simulation outputs.

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