# M62392P/FP

## 8-bit 12ch I²C BUS D/A Converter with Buffer Amplifiers

REJ03D0883-0300
Rev.3.00
Mar 25, 2008

## Description

The M62392P/FP is a CMOS 12 channels D/A converter with output buffer amplifiers. It can communicate with a microcontroller via few wiring thanks to the adoption of the two-line I²C BUS.

The output buffer amplifier employs AB class output with sinking and sourcing capability of more than 1.0 mA, and an output voltage range is nearly between ground and VrefU.

Maximum 8 ICs can be connected to a bus by using three chip-select pins, so that it is possible to handle up to 96 channels.

## Features

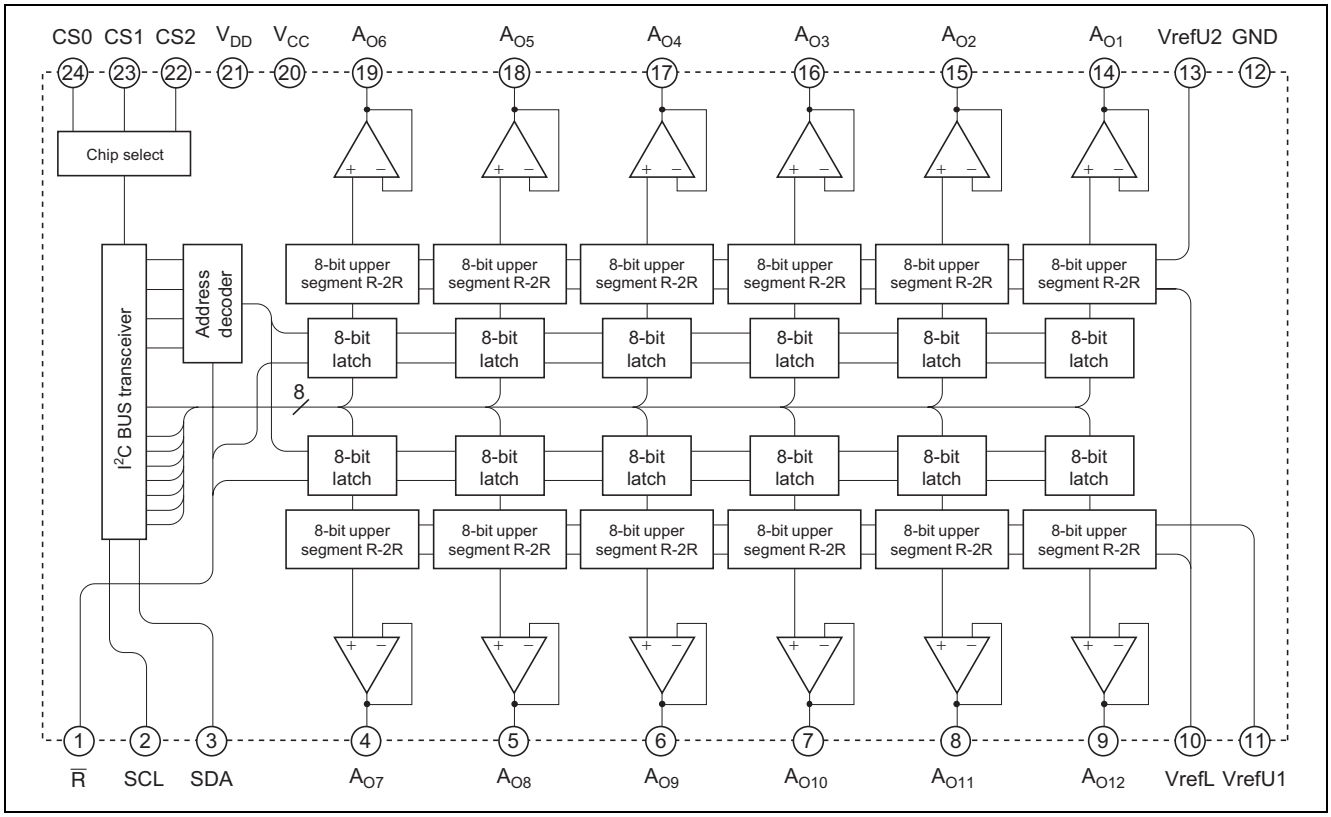
- I²C BUS serial data method
- Wide output voltage range
  Nearly between ground and VrefU (0 to 5 V)
- High output current drive capability over ±1.0 mA
- 2 setting voltage ranges by dual input pins for upper voltage references (VrefU1, U2)

## Application

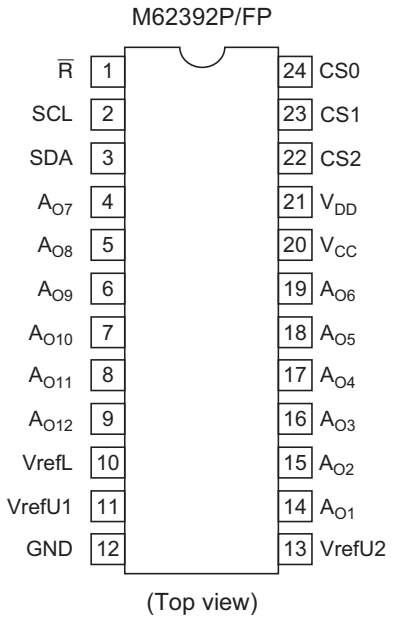
Conversion from digital data to analog control data for both consumer and industrial equipment.

Gain control and automatic adjustment of display-monitor or CTV.

## Block Diagram



## Pin Arrangement




Outline: PRDP0024AA-A (24P4D)
24P2N-B

## Pin Description

| Pin No. | Pin Name | Function |
|---|---|---|
| 3 | SDA | Serial data input terminal |
| 1 | $\overline{R}$ | Reset signal input terminal |
| 2 | SCL | Serial clock input terminal |
| 14 | Ao1 | 8-bit D/A converter output terminal |
| 15 | Ao2 | |
| 16 | Ao3 | |
| 17 | Ao4 | |
| 18 | Ao5 | |
| 19 | Ao6 | |
| 4 | Ao7 | |
| 5 | Ao8 | |
| 6 | Ao9 | |
| 7 | Ao10 | |
| 8 | Ao11 | |
| 9 | Ao12 | |
| 20 | $V_{CC}$ | Analog power supply terminal |
| 21 | $V_{DD}$ | Digital power supply terminal |
| 12 | GND | Analog and digital common GND |
| 10 | VrefL | D/A converter low level reference voltage input terminal |
| 11 | VrefU1 | D/A converter high level reference voltage input terminal 1 |
| 13 | VrefU2 | D/A converter high level reference voltage input terminal 2 |
| 22 | CS2 | Chip select data input terminal 2 |
| 23 | CS1 | Chip select data input terminal 1 |
| 24 | CS0 | Chip select data input terminal 0 |

## Absolute Maximum Ratings

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | –0.3 to +7.0 | V |
| Supply voltage | $V_{DD}$ | –0.3 to +7.0 | V |
| D/A converter high level reference voltage | VrefU1, 2 | –0.3 to +7.0 | V |
| Input voltage | Vin | –0.3 to $V_{DD}$ + 0.3 | V |
| Output voltage | $V_O$ | –0.3 to $V_{CC}$ + 0.3 | V |
| Power dissipation | Pd | 465 (P) / 421 (FP) | mW |
| Operating temperature | Topr | –20 to +85 | °C |
| Storage temperature | Tstg | –40 to +125 | °C |

## Electrical Characteristics

### <Digital Part>

($V_{CC}$, $V_{DD}$, VrefU1, 2 = +5 V ± 10%, $V_{CC}$ ≥ VrefU1, 2, GND = VrefL = 0 V, Ta = –20 to +85°C, unless otherwise noted.)

| Item | Symbol | Limits | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Supply voltage | $V_{DD}$ | 4.5 | 5.0 | 5.5 | V | |
| Supply current | $I_{DD}$ | — | — | 1.0 | mA | CLK = 1 MHz operation, $I_{AO}$ = 0 μA |
| Input leak current | $I_{ILK}$ | –10 | — | 10 | μA | $V_{IN}$ = 0 to $V_{DD}$ |
| Output low voltage (SDA) | $V_{OL}$ | — | — | 0.4 | V | Isink = 3 mA |
| Input low voltage | $V_{IL}$ | — | — | 0.2 $V_{DD}$ | V | |
| Input high voltage | $V_{IH}$ | 0.8 $V_{DD}$ | — | — | V | |

### <Analog Part>

($V_{CC}$, $V_{DD}$, VrefU1, 2 = +5 V ± 10%, $V_{CC}$ ≥ VrefU1, 2, GND = VrefL = 0 V, Ta = –20 to +85°C, unless otherwise noted.)

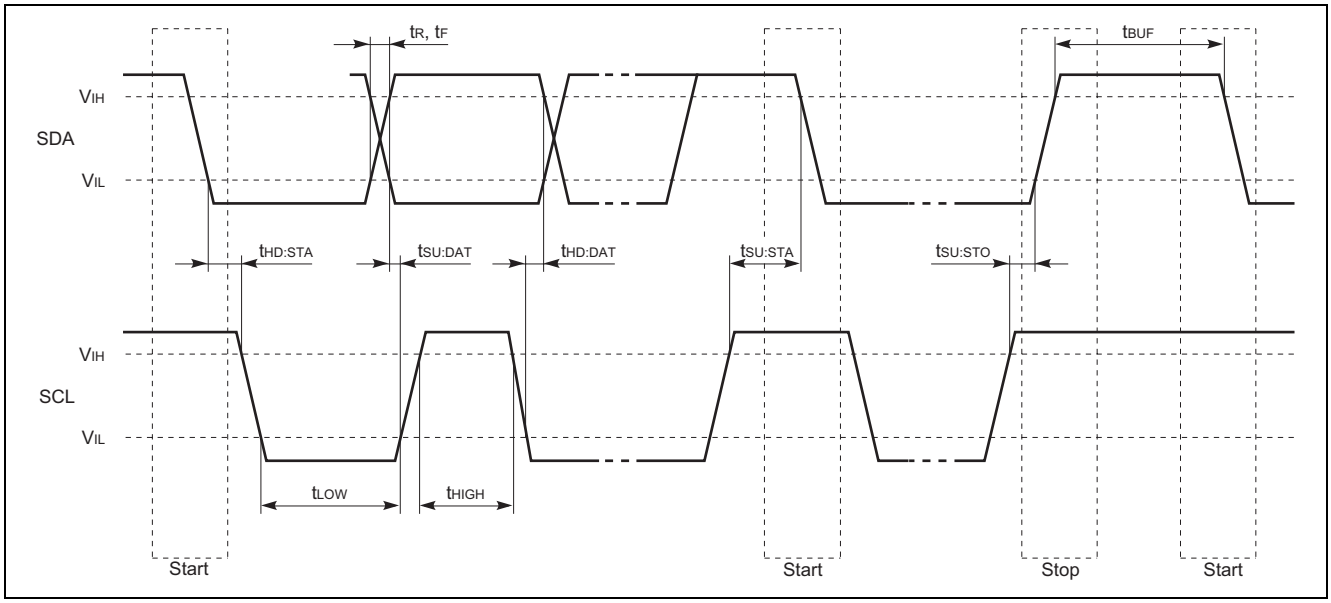
| Item | Symbol | Limits | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Supply voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | |
| Supply current | $I_{CC}$ | — | 1.0 | 3.0 | mA | CLK = 1 MHz operation, $I_{AO}$ = 0 μA |
| D/A converter high level reference voltage input current | IrefU | — | 1.4 | 3.0 | mA | VrefU = 5 V, VrefL = 0 V<br>Data condition: at maximum current |
| D/A converter high level reference voltage range | VrefU | 3.5 | — | $V_{CC}$ | V | The output dose not necessarily be the values within the reference voltage setting range. |
| D/A converter low level reference voltage range | VrefL | GND | — | $V_{CC}$ – 3.5 | V | |
| Buffer amplifier output voltage range | $V_{AO}$ | 0.1 | — | $V_{CC}$ – 0.1 | V | $I_{AO}$ = ±100 μA |
| | | 0.2 | — | $V_{CC}$ – 0.2 | V | $I_{AO}$ = ±500 μA |
| Buffer amplifier output drive range | $I_{AO}$ | –1.0 | — | 1.0 | mA | Upper side saturation voltage = 0.3 V<br>Lower side saturation voltage = 0.2 V |
| Differential nonlinearity | $S_{DL}$ | –1.0 | — | 1.0 | LSB | VrefU = 4.79 V<br>VrefL = 0.95 V<br>$V_{CC}$ = 5.5 V (15 mV/LSB)<br>Without load ($I_{AO}$ = 0) |
| Nonlinearity | $S_L$ | –1.5 | — | 1.5 | LSB | |
| Zero code error | $S_{ZERO}$ | –2.0 | — | 2.0 | LSB | |
| Full scale error | $S_{FULL}$ | –2.0 | — | 2.0 | LSB | |
| Output capacitive load | $C_O$ | — | — | 0.1 | μF | |
| Buffer amplifier output impedance | $R_O$ | — | 5.0 | — | Ω | |

## I²C BUS Line Characteristics

| Item | Symbol | Normal Mode | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| SCL clock frequency | $f_{SCL}$ | 0 | 100 | kHz |
| Time the bus must be free before a new transmission can start | $t_{BUF}$ | 4.7 | — | µs |
| Hold time START condition.<br>After this period, the first clock pulse is generated. | $t_{HD : STA}$ | 4.0 | — | µs |
| Low period of the clock | $t_{LOW}$ | 4.7 | — | µs |
| High period of the clock | $t_{HIGH}$ | 4.0 | — | µs |
| Setup time for START condition<br>(only relevant for a repeated START condition) | $t_{SU : STA}$ | 4.7 | — | µs |
| Hold time DATA | $t_{HD : DAT}$ | 0 | — | µs |
| Setup time DATA | $t_{SU : DAT}$ | 250 | — | ns |
| Rise time of both SDA and SCL lines | $t_R$ | — | 1000 | ns |
| Fall time of both SDA and SCL lines | $t_F$ | — | 300 | ns |
| Setup time for STOP condition | $t_{SU : STO}$ | 4.0 | — | µs |

Note: Transmitter must internally provide at least a hold time to bridge the undefined region (300 ns Max) of the falling edge of SCL.

## Timing Chart

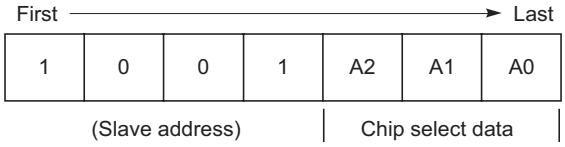


## I²C BUS Format

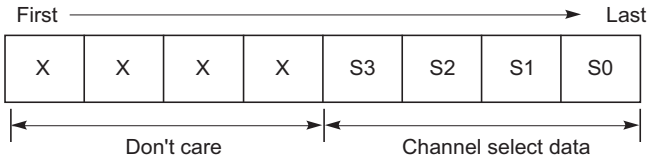
| STA | Slave address | W | A | Sub address | A | DAC data | A | STP |
|---|---|---|---|---|---|---|---|---|

## Digital Data Format

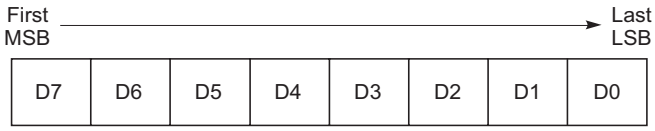
- Slave Address




- Sub Address




- DAC Data




### (1) Chip Select Data

MSB LSB

| A2 | A1 | A0 | CS2 | CS1 | CS0 |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| : | : | : | : | : | : |
| 1 | 1 | 1 | 1 | 1 | 1 |

Note: Lower 3 bits (A0, A1, A2) are a programmable address. This IC is accessed only when the lower 3 bits data of slave address coincide with the data of CS0 to CS2. (Refer to the upper table)

### (2) Channel Select Data

MSB LSB

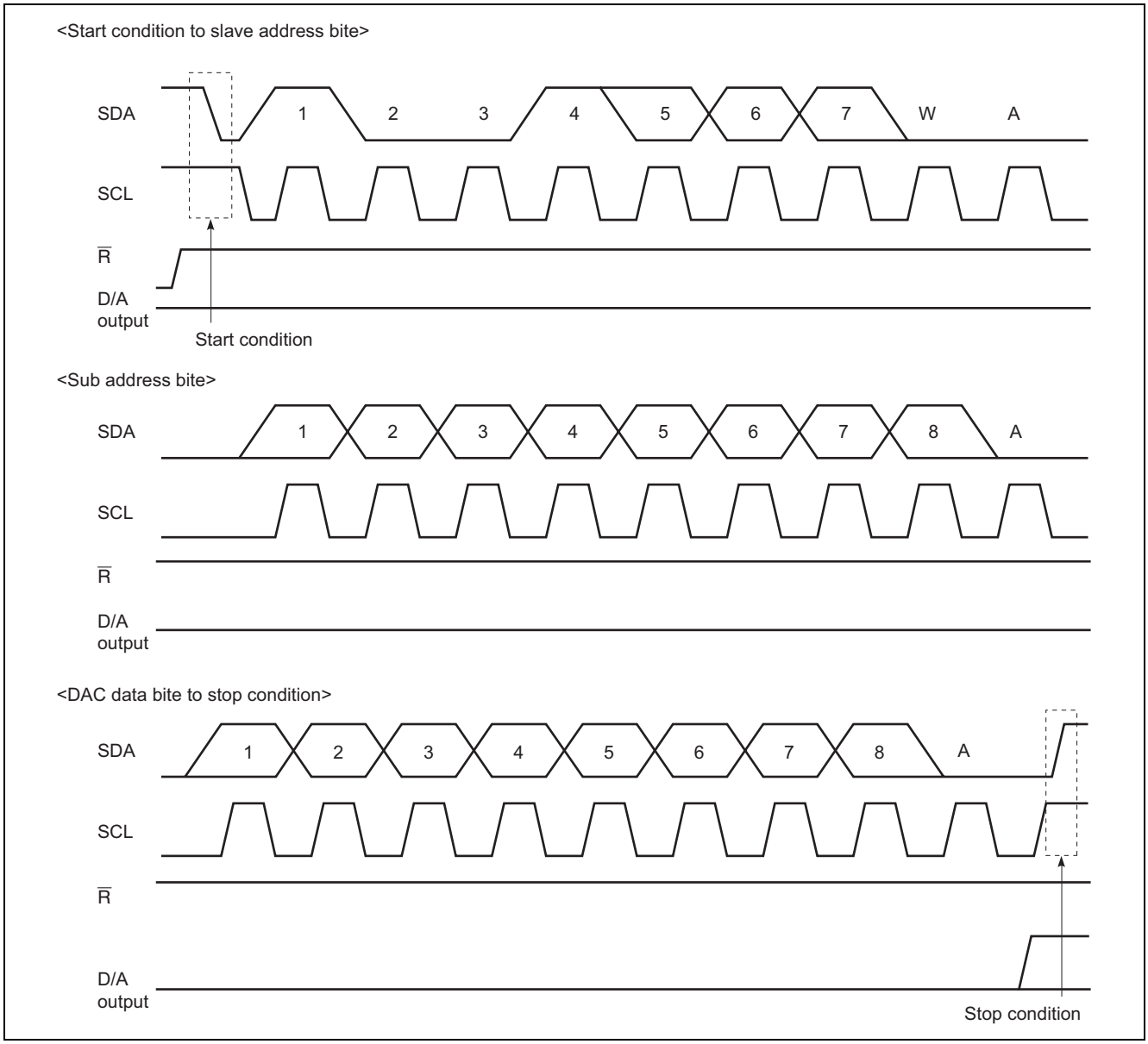
| S3 | S2 | S1 | S0 | Channel Selection |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Don't care |
| 0 | 0 | 0 | 1 | ch1 selection |
| 0 | 0 | 1 | 0 | ch2 selection |
| : | : | : | : | : |
| 1 | 0 | 1 | 1 | ch11 selection |
| 1 | 1 | 0 | 0 | ch12 selection |
| 1 | 1 | 0 | 1 | Don't care |
| : | : | : | : | : |
| 1 | 1 | 1 | 1 | Don't care |

### (3) DAC Data

First MSB → Last LSB

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DAC Output |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | (VrefU – VrefL ) / 256 × 1 + VrefL |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (VrefU – VrefL ) / 256 × 2 + VrefL |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | (VrefU – VrefL ) / 256 × 3 + VrefL |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | (VrefU – VrefL ) / 256 × 4 + VrefL |
| : | : | : | : | : | : | : | : | : |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | (VrefU – VrefL ) / 256 × 255 + VrefL |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | VrefU |

## Timing Chart (Model)




- Start condition: With SCL at high, SDA line goes from high to low
- Stop condition: With SCL at high, SDA line goes from low to high
  (Under normal circumstances, SDA is changed when SCL is low)
- Acknowledge bit: The receiving IC has to pull down SDA line whenever receive slave data.
  (The transmitting IC releases the SDA line just then transmit 8-bit data.)

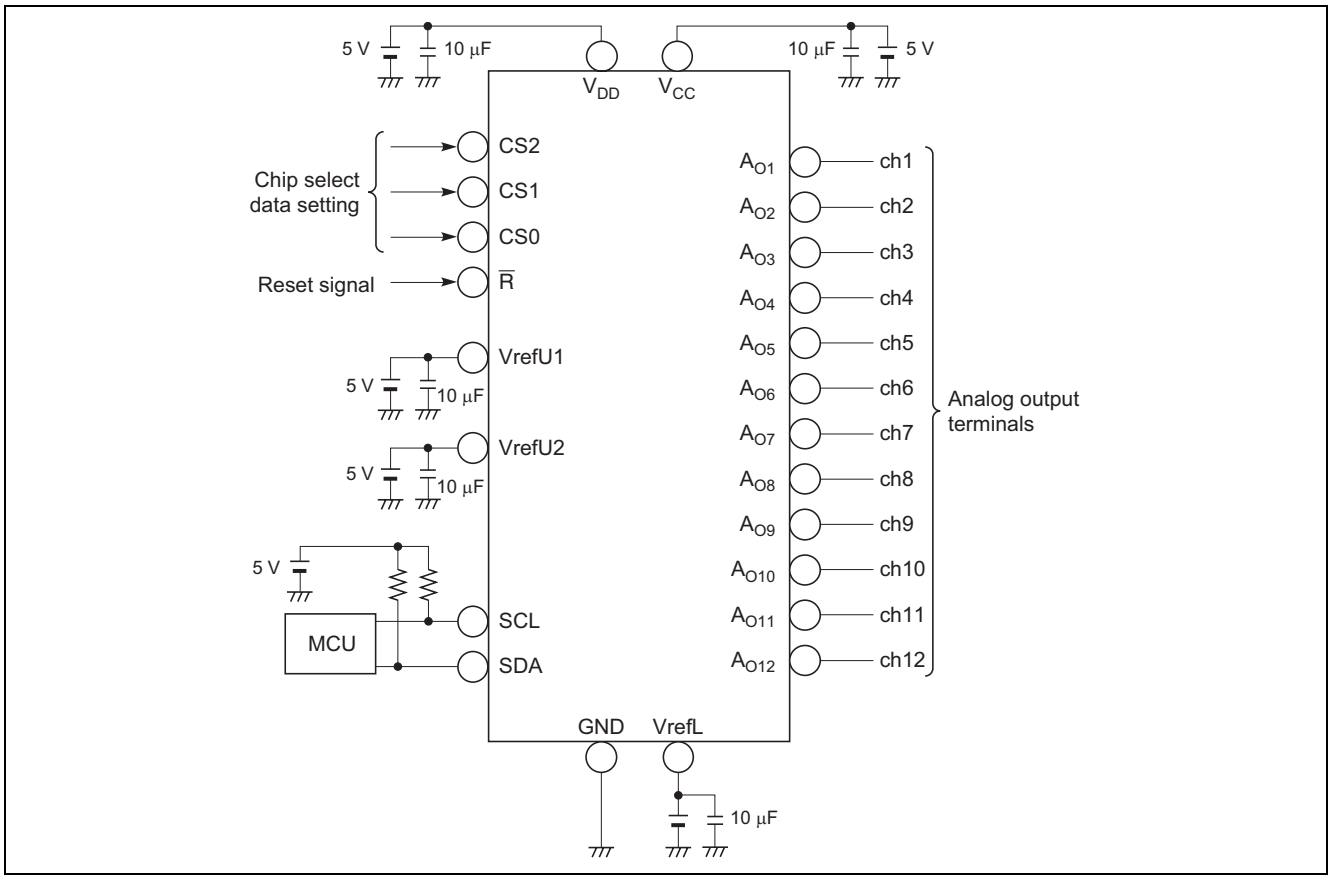
## Precaution for Use

M62392 have 5 terminals ($V_{DD}$, $V_{CC}$, VrefU1, VrefU2, VrefL) for input constant voltage at use. If ripple or spike is input these terminals, accuracy of D/A conversion is down. So, when use this device, please connect capacitor among each terminal to GND for stable D/A conversion.

This IC's output amplifier has an advantage to capacitive load. So it's no problem at device action when connect capacitor (0.1 µF Max) among output to GND for every noise eliminate.

Purchase of Renesas's $I^2C$ components conveys a license under the Philips $I^2C$ Patent Rights to use these components an $I^2C$ system, provided that the system conforms to $I^2C$ Standard Specification as defined by Philips.

## Application Example

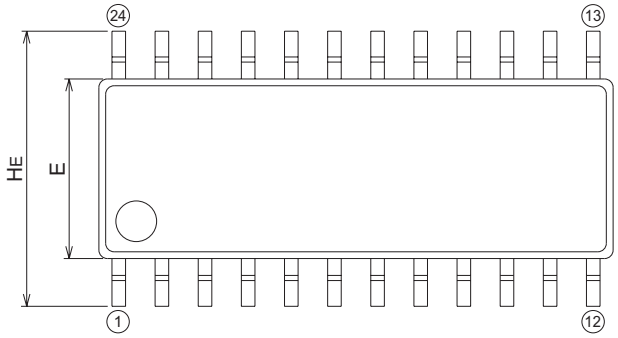


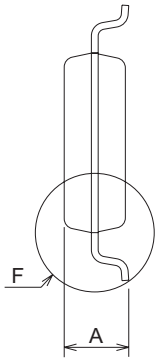
## Package Dimensions

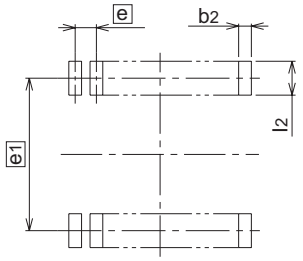
### 24P2N-B

**Plastic 24pin 300mil SOP**

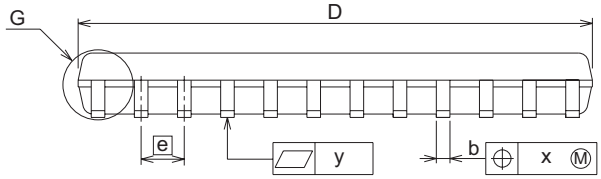
| EIAJ Package Code | JEDEC Code | Weight(g) | Lead Material |
|---|---|---|---|
| SOP24-P-300-1.27 | — | | Cu Alloy |

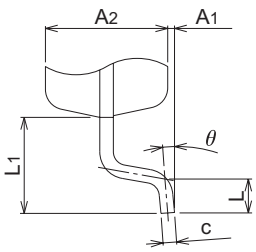


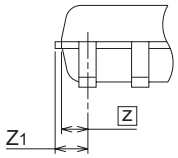




Recommended Mount Pad



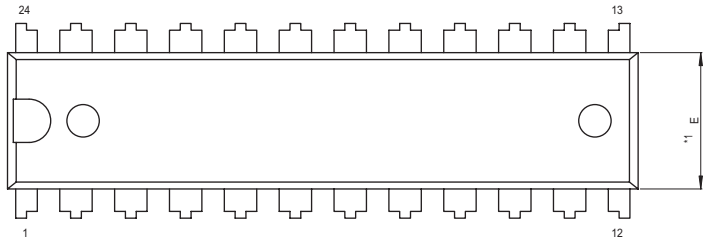



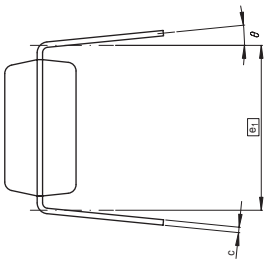

Detail G

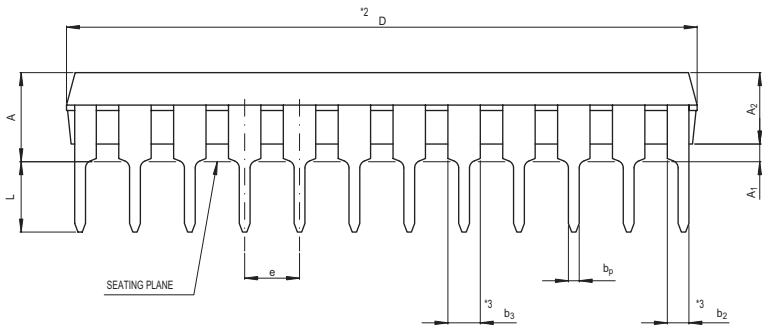
Detail F

| Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| A | — | — | 2.1 |
| $A_1$ | 0 | 0.1 | 0.2 |
| $A_2$ | — | 1.8 | — |
| b | 0.35 | 0.4 | 0.5 |
| c | 0.18 | 0.2 | 0.25 |
| D | 14.92 | 15.02 | 15.12 |
| E | 5.2 | 5.3 | 5.4 |
| e | — | 1.27 | — |
| $H_E$ | 7.82 | 8.12 | 8.42 |
| L | 0.3 | 0.5 | 0.7 |
| $L_1$ | — | 1.41 | — |
| z | — | 0.525 | — |
| $Z_1$ | — | — | 0.675 |
| x | — | — | 0.25 |
| y | — | — | 0.1 |
| θ | 0° | — | 10° |
| $b_2$ | — | 0.76 | — |
| e1 | — | 7.62 | — |
| $l_2$ | 1.27 | — | — |

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-DIP24-6.3x29.2-2.54 | PRDP0024AA-A | 24P4D | 1.6g |




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| e1 | 7.32 | 7.62 | 7.92 |
| D | 29.0 | 29.2 | 29.4 |
| E | 6.15 | 6.3 | 6.45 |
| A | — | — | 4.5 |
| $A_1$ | 0.51 | — | — |
| $A_2$ | — | 3.3 | — |
| $b_p$ | 0.4 | 0.5 | 0.6 |
| $b_2$ | 0.9 | 1.0 | 1.3 |
| $b_3$ | 1.4 | 1.5 | 1.8 |
| c | 0.22 | 0.27 | 0.34 |
| θ | 0° | — | 15° |
| e | 2.29 | 2.54 | 2.79 |
| L | 3.0 | — | — |

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Colophon .7.2