

# M62392P/FP

## 8-bit 12ch I<sup>2</sup>C BUS D/A Converter with Buffer Amplifiers

REJ03D0883-0300

Rev.3.00

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### Description

The M62392P/FP is a CMOS 12 channels D/A converter with output buffer amplifiers. It can communicate with a microcontroller via few wiring thanks to the adoption of the two-line I<sup>2</sup>C BUS.

The output buffer amplifier employs AB class output with sinking and sourcing capability of more than 1.0 mA, and an output voltage range is nearly between ground and VrefU.

Maximum 8 ICs can be connected to a bus by using three chip-select pins, so that it is possible to handle up to 96 channels.

### Features

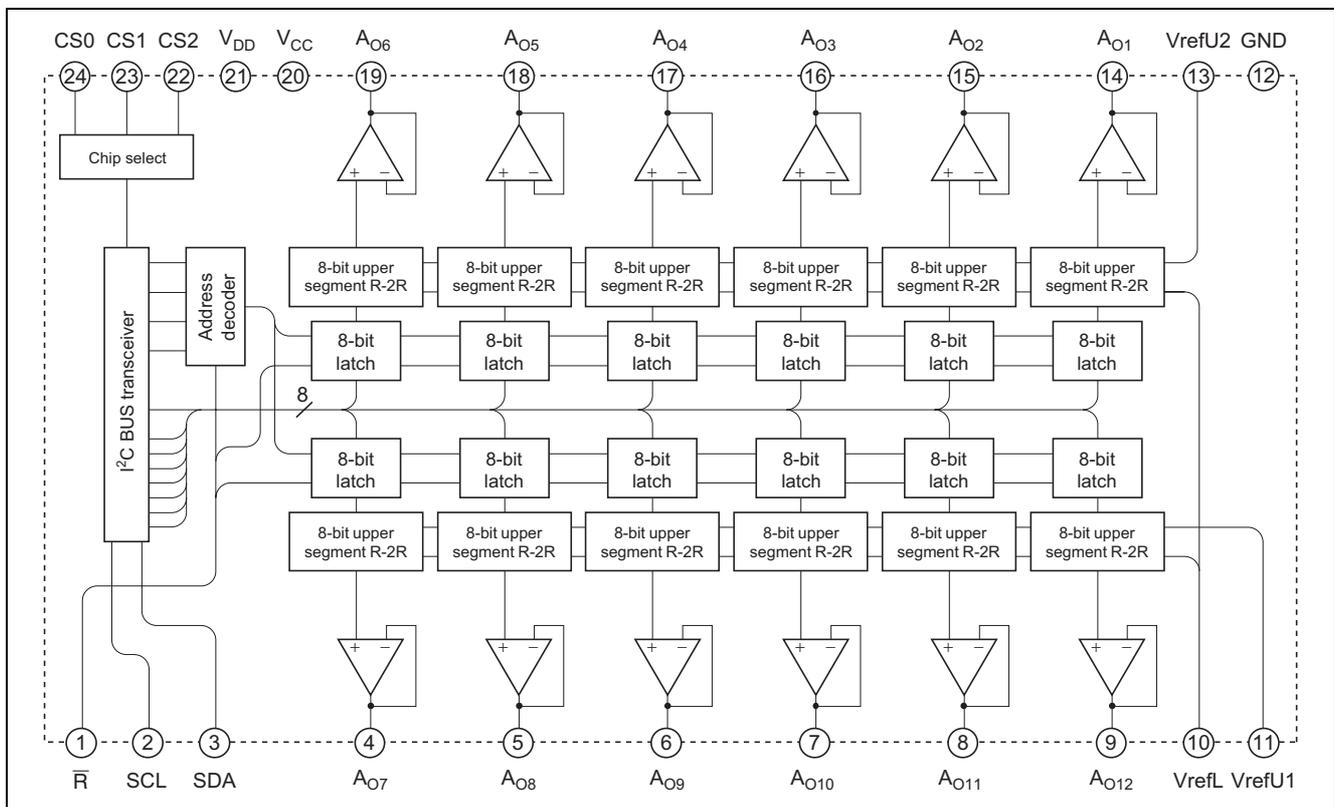
- I<sup>2</sup>C BUS serial data method
- Wide output voltage range  
Nearly between ground and VrefU (0 to 5 V)
- High output current drive capability over  $\pm 1.0$  mA
- 2 setting voltage ranges by dual input pins for upper voltage references (VrefU1, U2)

### Application

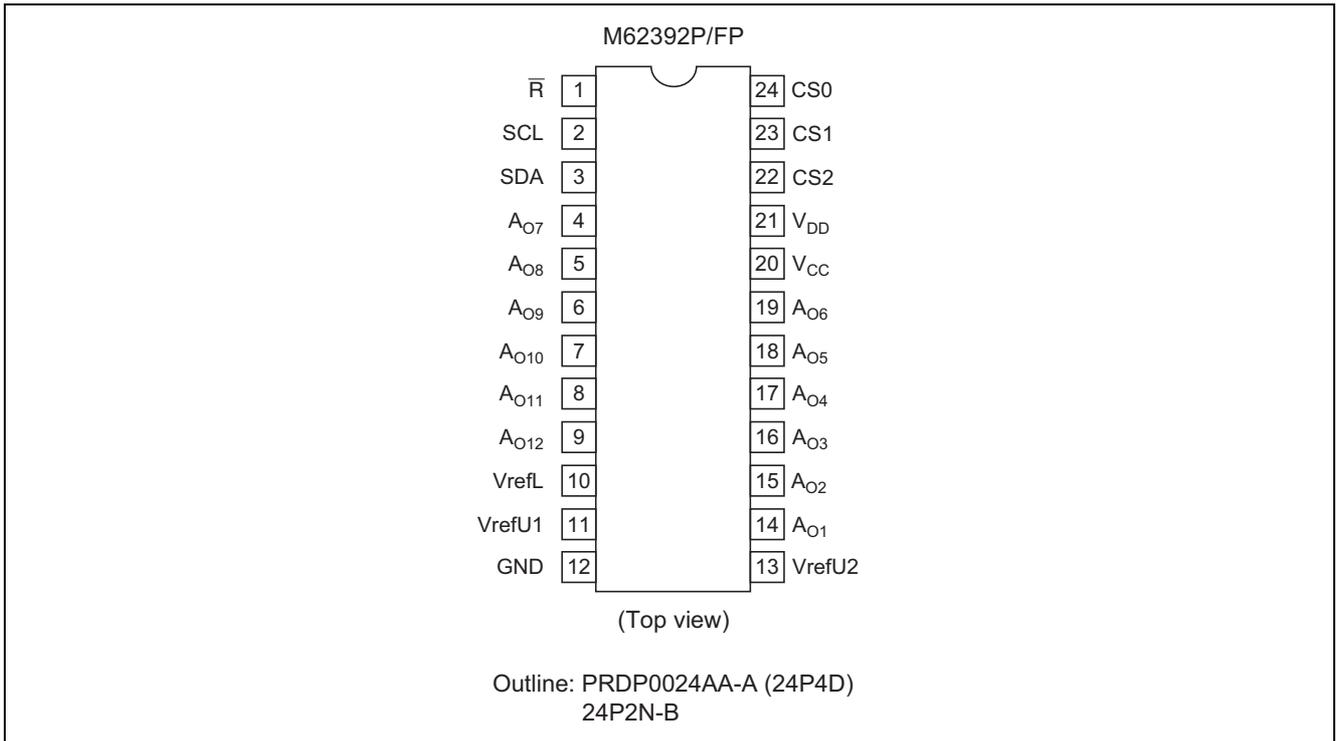
Conversion from digital data to analog control data for both consumer and industrial equipment.

Gain control and automatic adjustment of display-monitor or CTV.

### Block Diagram



## Pin Arrangement



## Pin Description

Pin No.	Pin Name	Function
3	SDA	Serial data input terminal
1	$\bar{R}$	Reset signal input terminal
2	SCL	Serial clock input terminal
14	Ao1	8-bit D/A converter output terminal
15	Ao2	
16	Ao3	
17	Ao4	
18	Ao5	
19	Ao6	
4	Ao7	
5	Ao8	
6	Ao9	
7	Ao10	
8	Ao11	
9	Ao12	
20	V <sub>CC</sub>	Analog power supply terminal
21	V <sub>DD</sub>	Digital power supply terminal
12	GND	Analog and digital common GND
10	VrefL	D/A converter low level reference voltage input terminal
11	VrefU1	D/A converter high level reference voltage input terminal 1
13	VrefU2	D/A converter high level reference voltage input terminal 2
22	CS2	Chip select data input terminal 2
23	CS1	Chip select data input terminal 1
24	CS0	Chip select data input terminal 0

## Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	$V_{CC}$	-0.3 to +7.0	V
Supply voltage	$V_{DD}$	-0.3 to +7.0	V
D/A converter high level reference voltage	$V_{refU1, 2}$	-0.3 to +7.0	V
Input voltage	$V_{in}$	-0.3 to $V_{DD} + 0.3$	V
Output voltage	$V_o$	-0.3 to $V_{CC} + 0.3$	V
Power dissipation	$P_d$	465 (P) / 421 (FP)	mW
Operating temperature	$T_{opr}$	-20 to +85	°C
Storage temperature	$T_{stg}$	-40 to +125	°C

## Electrical Characteristics

### <Digital Part>

( $V_{CC}$ ,  $V_{DD}$ ,  $V_{refU1, 2} = +5\text{ V} \pm 10\%$ ,  $V_{CC} \geq V_{refU1, 2}$ ,  $GND = V_{refL} = 0\text{ V}$ ,  $T_a = -20\text{ to }+85^\circ\text{C}$ , unless otherwise noted.)

Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Supply voltage	$V_{DD}$	4.5	5.0	5.5	V	
Supply current	$I_{DD}$	—	—	1.0	mA	CLK = 1 MHz operation, $I_{AO} = 0\ \mu\text{A}$
Input leak current	$I_{ILK}$	-10	—	10	$\mu\text{A}$	$V_{IN} = 0\text{ to }V_{DD}$
Output low voltage (SDA)	$V_{OL}$	—	—	0.4	V	$I_{sink} = 3\text{ mA}$
Input low voltage	$V_{IL}$	—	—	$0.2 V_{DD}$	V	
Input high voltage	$V_{IH}$	$0.8 V_{DD}$	—	—	V	

### <Analog Part>

( $V_{CC}$ ,  $V_{DD}$ ,  $V_{refU1, 2} = +5\text{ V} \pm 10\%$ ,  $V_{CC} \geq V_{refU1, 2}$ ,  $GND = V_{refL} = 0\text{ V}$ ,  $T_a = -20\text{ to }+85^\circ\text{C}$ , unless otherwise noted.)

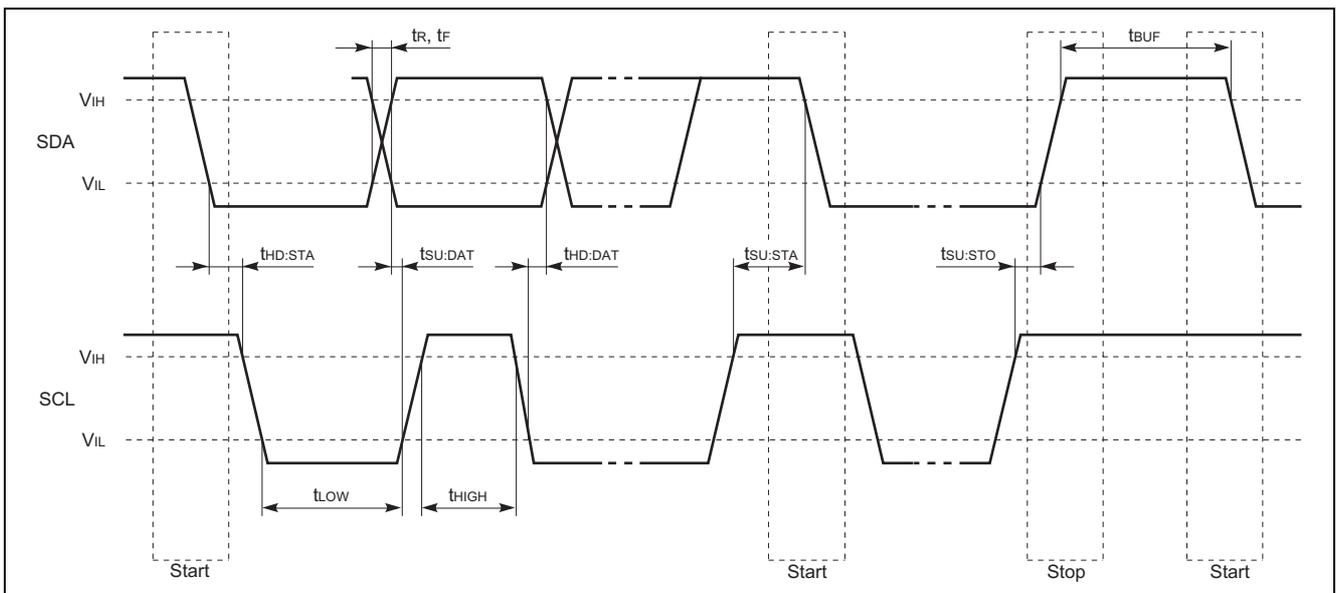
Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V	
Supply current	$I_{CC}$	—	1.0	3.0	mA	CLK = 1 MHz operation, $I_{AO} = 0\ \mu\text{A}$
D/A converter high level reference voltage input current	$I_{refU}$	—	1.4	3.0	mA	$V_{refU} = 5\text{ V}$ , $V_{refL} = 0\text{ V}$ Data condition: at maximum current
D/A converter high level reference voltage range	$V_{refU}$	3.5	—	$V_{CC}$	V	The output dose not necessarily be the values within the reference voltage setting range.
D/A converter low level reference voltage range	$V_{refL}$	GND	—	$V_{CC} - 3.5$	V	
Buffer amplifier output voltage range	$V_{AO}$	0.1	—	$V_{CC} - 0.1$	V	$I_{AO} = \pm 100\ \mu\text{A}$
		0.2	—	$V_{CC} - 0.2$	V	$I_{AO} = \pm 500\ \mu\text{A}$
Buffer amplifier output drive range	$I_{AO}$	-1.0	—	1.0	mA	Upper side saturation voltage = 0.3 V Lower side saturation voltage = 0.2 V
Differential nonlinearity	$S_{DL}$	-1.0	—	1.0	LSB	$V_{refU} = 4.79\text{ V}$
Nonlinearity	$S_L$	-1.5	—	1.5	LSB	$V_{refL} = 0.95\text{ V}$
Zero code error	$S_{ZERO}$	-2.0	—	2.0	LSB	$V_{CC} = 5.5\text{ V}$ (15 mV/LSB)
Full scale error	$S_{FULL}$	-2.0	—	2.0	LSB	Without load ( $I_{AO} = 0$ )
Output capacitive load	$C_O$	—	—	0.1	$\mu\text{F}$	
Buffer amplifier output impedance	$R_O$	—	5.0	—	$\Omega$	

I<sup>2</sup>C BUS Line Characteristics

Item	Symbol	Normal Mode		Unit
		Min	Max	
SCL clock frequency	$f_{SCL}$	0	100	kHz
Time the bus must be free before a new transmission can start	$t_{BUF}$	4.7	—	$\mu$ S
Hold time START condition. After this period, the first clock pulse is generated.	$t_{HD:STA}$	4.0	—	$\mu$ S
Low period of the clock	$t_{LOW}$	4.7	—	$\mu$ S
High period of the clock	$t_{HIGH}$	4.0	—	$\mu$ S
Setup time for START condition (only relevant for a repeated START condition)	$t_{SU:STA}$	4.7	—	$\mu$ S
Hold time DATA	$t_{HD:DAT}$	0	—	$\mu$ S
Setup time DATA	$t_{SU:DAT}$	250	—	ns
Rise time of both SDA and SCL lines	$t_R$	—	1000	ns
Fall time of both SDA and SCL lines	$t_F$	—	300	ns
Setup time for STOP condition	$t_{SU:STO}$	4.0	—	$\mu$ S

Note: Transmitter must internally provide at least a hold time to bridge the undefined region (300 ns Max) of the falling edge of SCL.

## Timing Chart

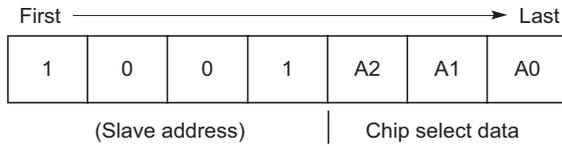


## I<sup>2</sup>C BUS Format

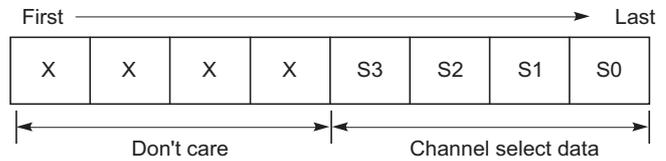
STA	Slave address	W	A	Sub address	A	DAC data	A	STP
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### Digital Data Format

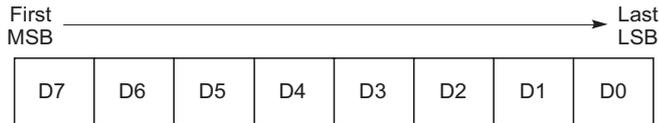
- Slave Address



- Sub Address



- DAC Data



#### (1) Chip Select Data

MSB	LSB				
A2	A1	A0	CS2	CS1	CS0
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
:	:	:	:	:	:
1	1	1	1	1	1

Note: Lower 3 bits (A0, A1, A2) are a programmable address. This IC is accessed only when the lower 3 bits data of slave address coincide with the data of CS0 to CS2. (Refer to the upper table)

#### (2) Channel Select Data

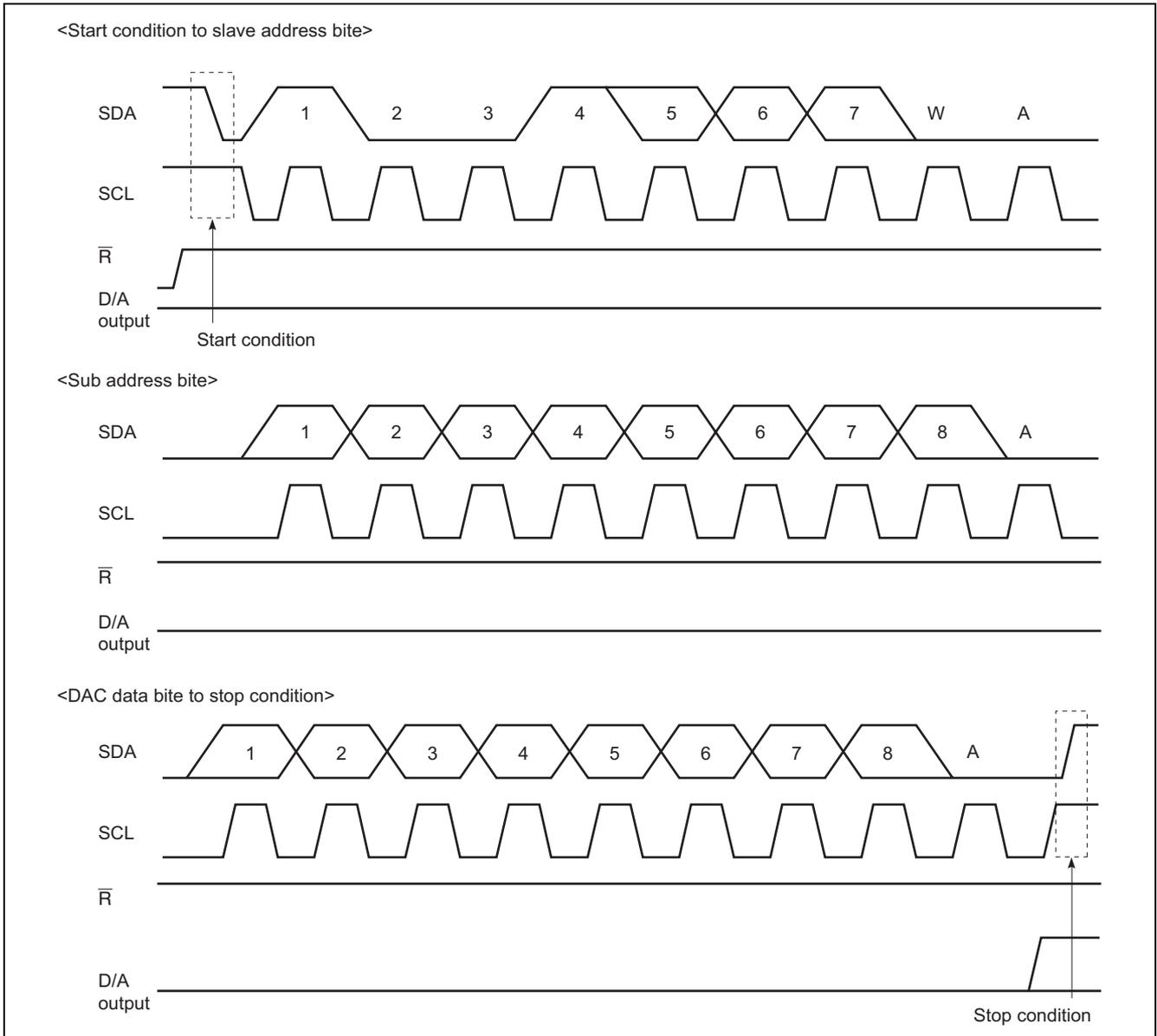
MSB	LSB				Channel Selection
S3	S2	S1	S0		
0	0	0	0	Don't care	
0	0	0	1	ch1 selection	
0	0	1	0	ch2 selection	
:	:	:	:	:	
1	0	1	1	ch11 selection	
1	1	0	0	ch12 selection	
1	1	0	1	Don't care	
:	:	:	:	:	
1	1	1	1	Don't care	

#### (3) DAC Data

First MSB → Last LSB

D7	D6	D5	D4	D3	D2	D1	D0	DAC Output
0	0	0	0	0	0	0	0	$(V_{refU} - V_{refL}) / 256 \times 1 + V_{refL}$
0	0	0	0	0	0	0	1	$(V_{refU} - V_{refL}) / 256 \times 2 + V_{refL}$
0	0	0	0	0	0	1	0	$(V_{refU} - V_{refL}) / 256 \times 3 + V_{refL}$
0	0	0	0	0	0	1	1	$(V_{refU} - V_{refL}) / 256 \times 4 + V_{refL}$
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	0	$(V_{refU} - V_{refL}) / 256 \times 255 + V_{refL}$
1	1	1	1	1	1	1	1	$V_{refU}$

## Timing Chart (Model)



- Start condition: With SCL at high, SDA line goes from high to low
- Stop condition: With SCL at high, SDA line goes from low to high (Under normal circumstances, SDA is changed when SCL is low)
- Acknowledge bit: The receiving IC has to pull down SDA line whenever receive slave data. (The transmitting IC releases the SDA line just then transmit 8-bit data.)

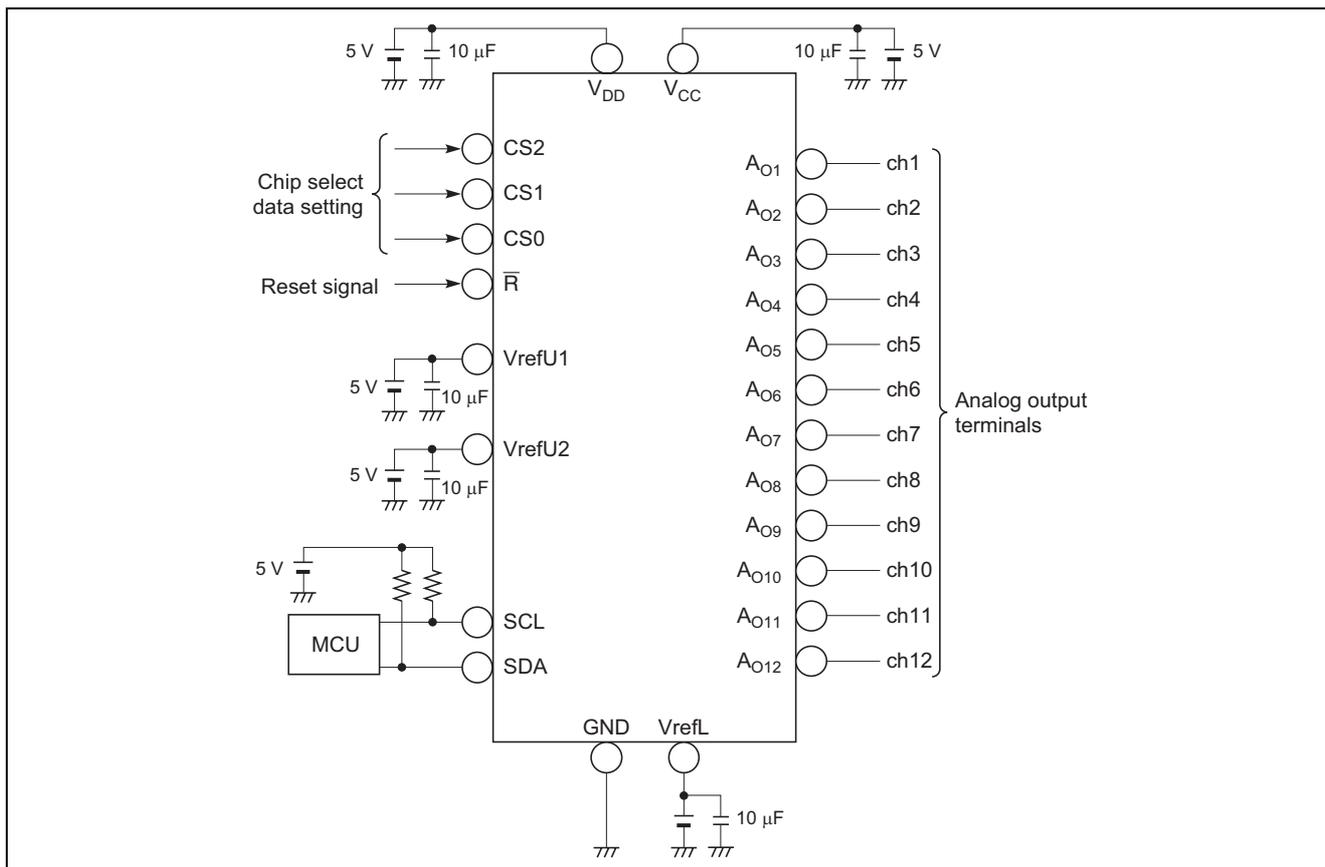
## Precaution for Use

M62392 have 5 terminals ( $V_{DD}$ ,  $V_{CC}$ ,  $V_{refU1}$ ,  $V_{refU2}$ ,  $V_{refL}$ ) for input constant voltage at use. If ripple or spike is input these terminals, accuracy of D/A conversion is down. So, when use this device, please connect capacitor among each terminal to GND for stable D/A conversion.

This IC's output amplifier has an advantage to capacitive load. So it's no problem at device action when connect capacitor (0.1  $\mu$ F Max) among output to GND for every noise eliminate.

Purchase of Renesas's I<sup>2</sup>C components conveys a license under the Philips I<sup>2</sup>C Patent Rights to use these components an I<sup>2</sup>C system, provided that the system conforms to I<sup>2</sup>C Standard Specification as defined by Philips.

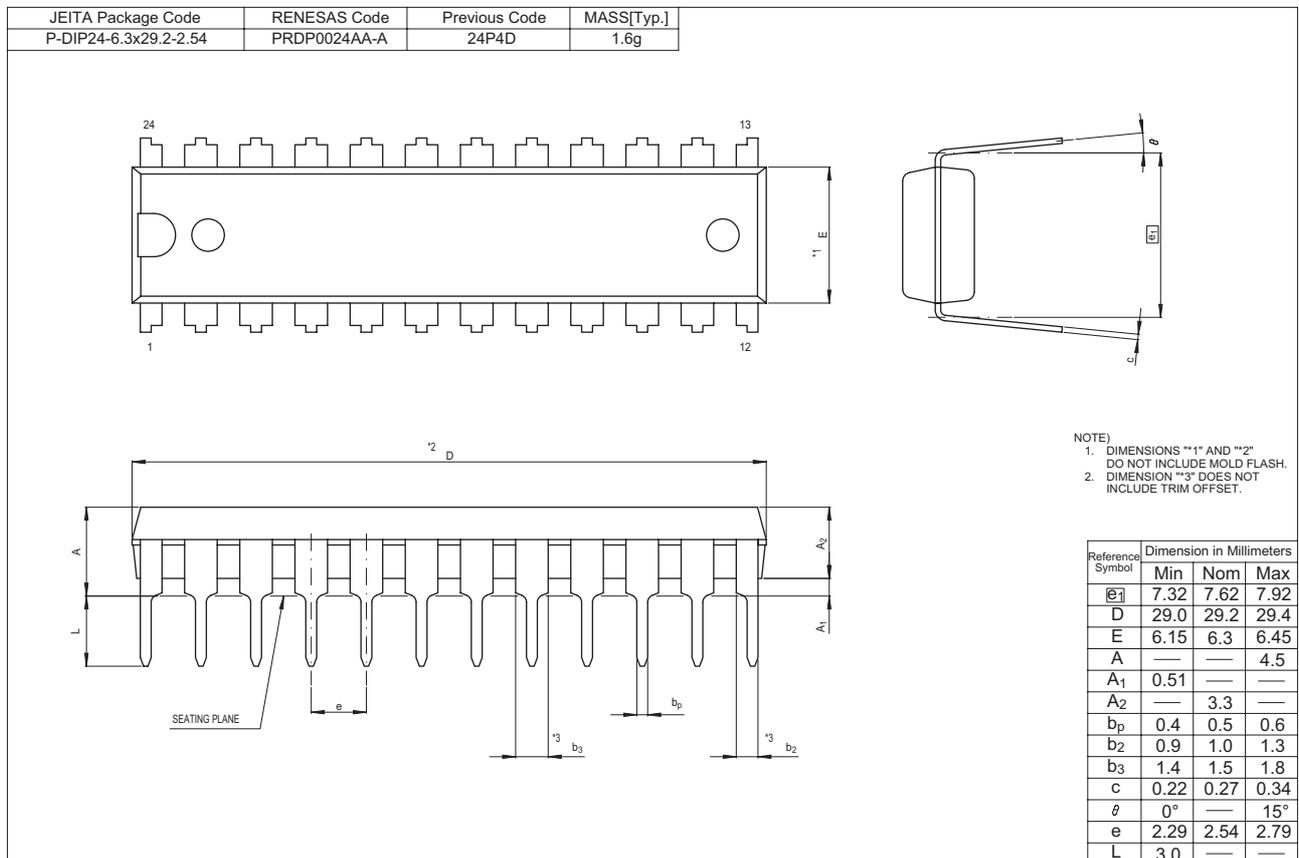
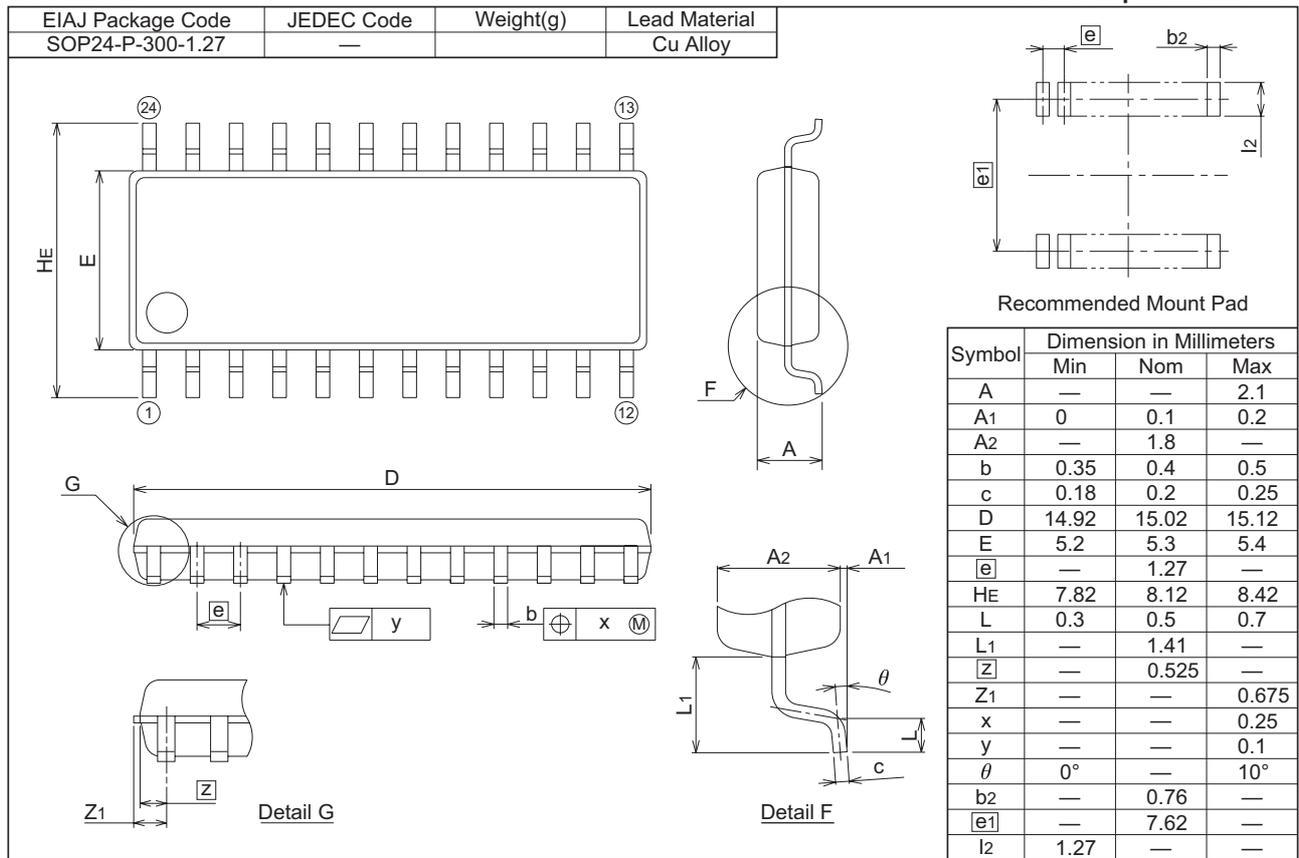
## Application Example



# Package Dimensions

## 24P2N-B

Plastic 24pin 300mil SOP



Notes:

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