



# RF Power Field Effect Transistor

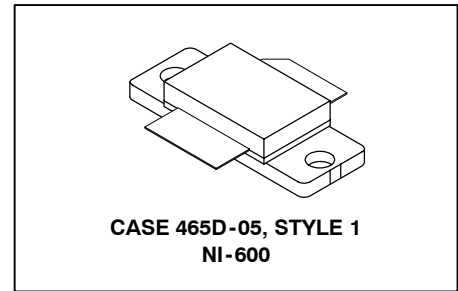
## N-Channel Enhancement-Mode Lateral MOSFET

Designed for GSM 900 frequency band, the high gain and broadband performance of this device make it ideal for large-signal, common source amplifier applications in 26 volt base station equipment.

- Specified Performance @ Full GSM Band, 921-960 MHz, 26 Volts  
 Output Power, P1dB — 80 Watts (Typ)  
 Power Gain @ P1dB — 16 dB (Typ)  
 Efficiency @ P1dB — 58% (Typ)
- Capable of Handling 5:1 VSWR, @ 26 Vdc, 945 MHz, 50 Watts CW Output Power
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 inch Reel.

**MRF6522-70R3**

**921-960 MHz, 70 W, 26 V  
 LATERAL N-CHANNEL  
 RF POWER MOSFET**



**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-0.5, +65	Vdc
Gate-Source Voltage	$V_{GS}$	$\pm 20$	Vdc
Drain Current — Continuous	$I_D$	7	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	159 0.9	W W/ $^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-65 to +150	$^\circ\text{C}$
Case Operating Temperature	$T_C$	150	$^\circ\text{C}$
Operating Junction Temperature	$T_J$	200	$^\circ\text{C}$

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.1	$^\circ\text{C}/\text{W}$

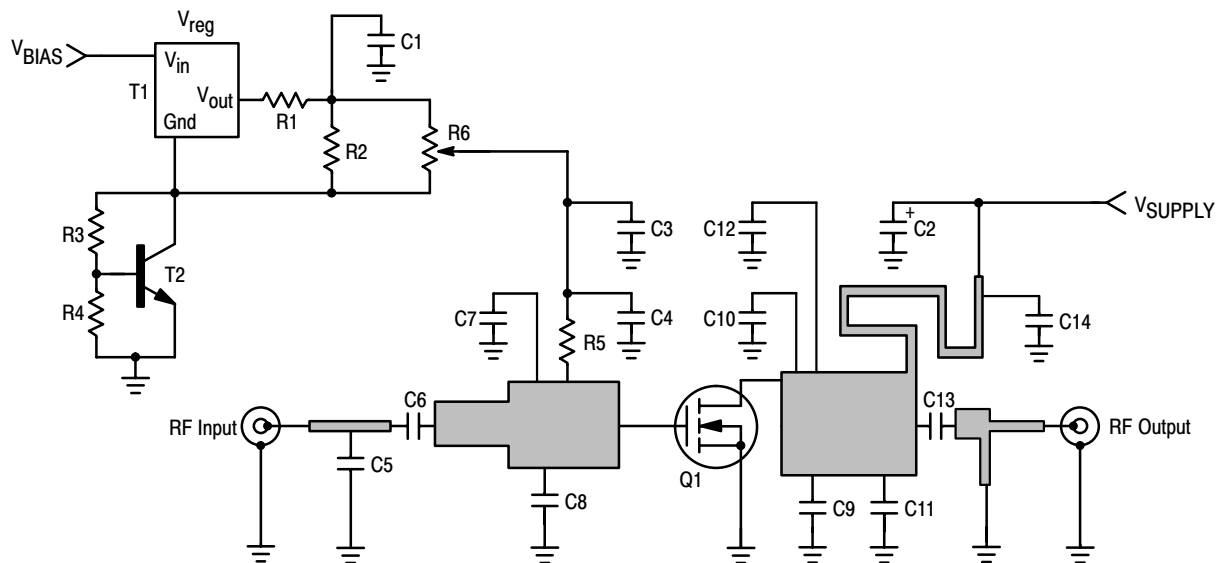
**NOTE - CAUTION** - MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

**Table 3. Electrical Characteristics** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Off Characteristics</b>					
Drain-Source Breakdown Voltage ( $V_{GS} = 0 \text{ Vdc}$ , $I_D = 20 \mu\text{Adc}$ )	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current ( $V_{DS} = 28 \text{ Vdc}$ , $V_{GS} = 0 \text{ Vdc}$ )	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Gate-Source Leakage Current ( $V_{GS} = 20 \text{ Vdc}$ , $V_{DS} = 0 \text{ Vdc}$ )	$I_{GSS}$	—	—	1	$\mu\text{Adc}$
<b>On Characteristics</b>					
Gate Threshold Voltage ( $V_{DS} = 10 \text{ Vdc}$ , $I_D = 300 \mu\text{Adc}$ )	$V_{GS(th)}$	2	3	4	Vdc
Gate Quiescent Voltage ( $V_{DS} = 26 \text{ Vdc}$ , $I_D = 400 \text{ mAdc}$ )	$V_{GS(Q)}$	3	4	5	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10 \text{ Vdc}$ , $I_D = 1 \text{ Adc}$ )	$V_{DS(on)}$	—	0.15	0.6	Vdc
Forward Transconductance ( $V_{DS} = 10 \text{ Vdc}$ , $I_D = 2 \text{ Adc}$ )	$g_{fs}$	2	3	—	S
<b>Dynamic Characteristics</b>					
Input Capacitance <sup>(1)</sup> ( $V_{DS} = 26 \text{ Vdc}$ , $V_{GS} = 0$ , $f = 1 \text{ MHz}$ )	$C_{iss}$	—	130	—	pF
Output Capacitance ( $V_{DS} = 26 \text{ Vdc}$ , $V_{GS} = 0$ , $f = 1 \text{ MHz}$ )	$C_{oss}$	41	47	52	pF
Reverse Transfer Capacitance ( $V_{DS} = 26 \text{ Vdc}$ , $V_{GS} = 0$ , $f = 1 \text{ MHz}$ )	$C_{rss}$	2.4	3	3.4	pF
<b>Functional Tests (In Freescale Test Fixture)</b>					
Output Power <sup>(2)</sup> ( $V_{DD} = 26 \text{ Vdc}$ , $I_{DQ} = 400 \text{ mA}$ , $f = \text{Full GSM Band } 921 - 960 \text{ MHz}$ )	P1dB	73	80	—	W
Common-Source Amplifier Power Gain @ P1dB (Min) <sup>(2)</sup> ( $V_{DD} = 26 \text{ Vdc}$ , $I_{DQ} = 400 \text{ mA}$ , $f = \text{Full GSM Band } 921 - 960 \text{ MHz}$ )	$G_{ps}$	14	16	18	dB
Drain Efficiency @ $P_{out} = 50 \text{ W}$ ( $V_{DD} = 26 \text{ Vdc}$ , $I_{DQ} = 400 \text{ mA}$ , $f = \text{Full GSM Band } 921 - 960 \text{ MHz}$ )	$\eta_1$	47	51	—	%
Drain Efficiency @ P1dB <sup>(2)</sup> ( $V_{DD} = 26 \text{ Vdc}$ , $I_{DQ} = 400 \text{ mA}$ , $f = \text{Full GSM Band } 921 - 960 \text{ MHz}$ )	$\eta_2$	—	58	—	%
Input Return Loss @ $P_{out} = 50 \text{ W}$ ( $V_{DD} = 26 \text{ Vdc}$ , $I_{DQ} = 400 \text{ mA}$ , $f = 921 \text{ MHz}$ and $960 \text{ MHz}$ $f = 940 \text{ MHz}$ )	IRL	—	—	- 10 - 15	dB

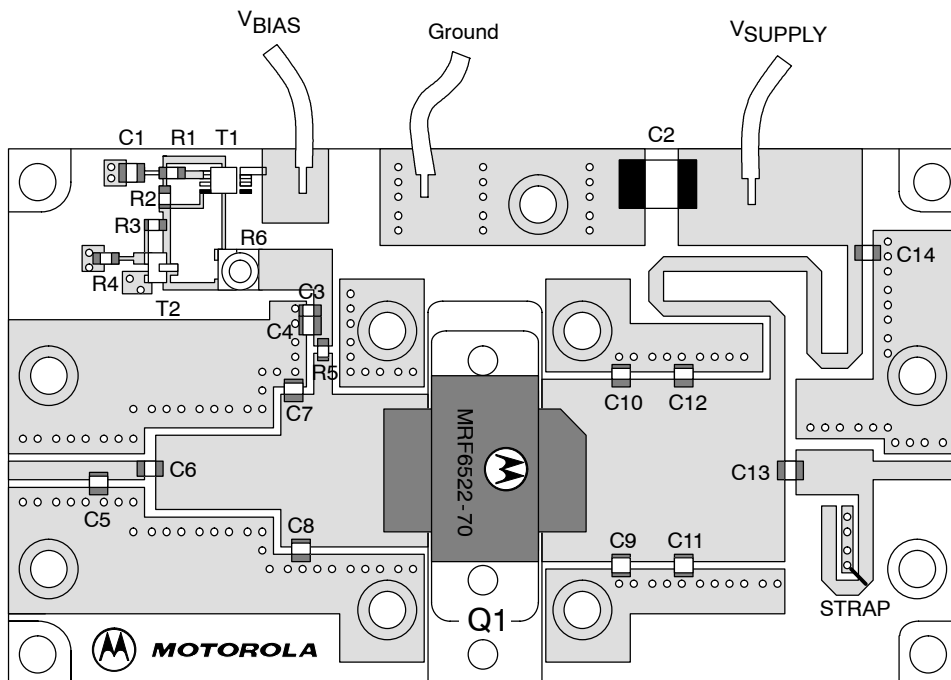
1. Value excludes the input matching.

2. To meet application requirements, Freescale test fixtures have been designed to cover full GSM 900 band ensuring batch-to-batch consistency.



C1	1.0 $\mu$ F Chip Capacitor (0805)	R3	1.2 k $\Omega$ Chip Resistor (0805)
C2	10 $\mu$ F, 35 Vdc Tantalum Capacitor	R4	2.2 k $\Omega$ Chip Resistor (0805)
C3	100 nF Chip Capacitor	R5	220 $\Omega$ Chip Resistor (0805)
C4, C6, C14	22 pF Chip Capacitors, ACCU-P (0805)	R6	5.0 k $\Omega$ SMD Potentiometer
C5	2.7 pF Chip Capacitor, ACCU-P (0805)	T1	LP2951 Micro-8
C7, C8, C13	4.7 pF Chip Capacitors, ACCU-P (0805)	T2	BC847 SOT-23
C9, C10	8.2 pF Chip Capacitors, ACCU-P (0805)		
C11, C12	2.2 pF Chip Capacitors, ACCU-P (0805)		
R1	10 $\Omega$ Chip Resistor (0805)		
R2	1.0 k $\Omega$ Chip Resistor (0805)		
			SUBSTRATE GI180 0.8 mm

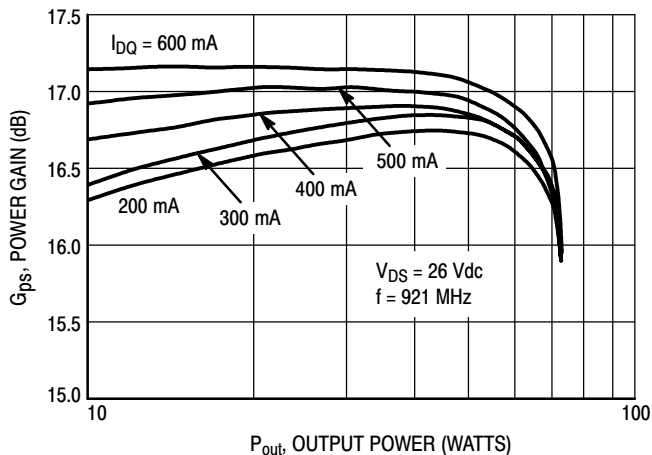
Figure 1. MRF6522-70 Test Circuit Schematic



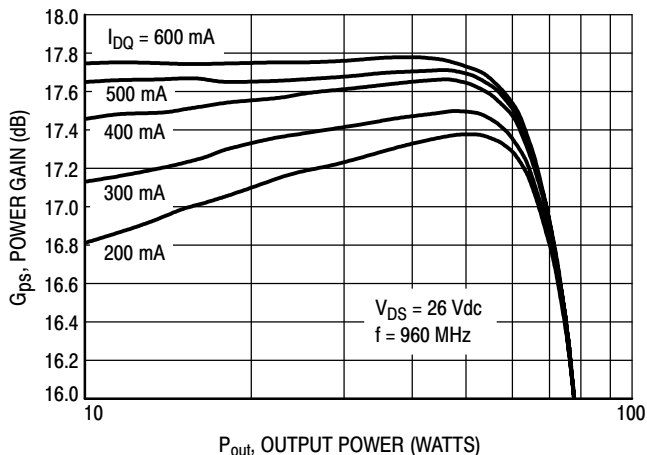
Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 2. MRF6522-70 Test Circuit Component Layout

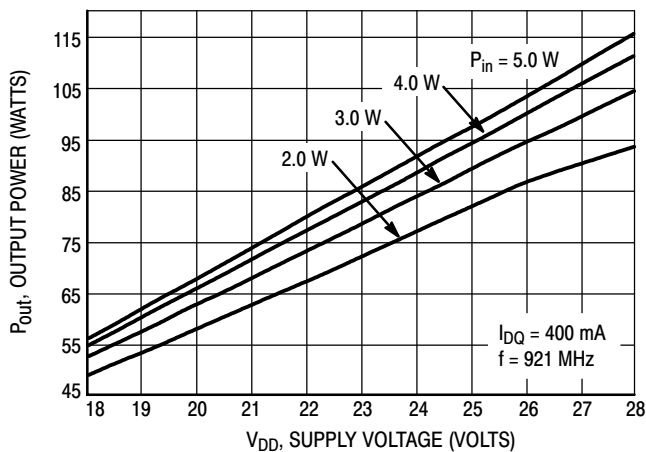
## TYPICAL CHARACTERISTICS



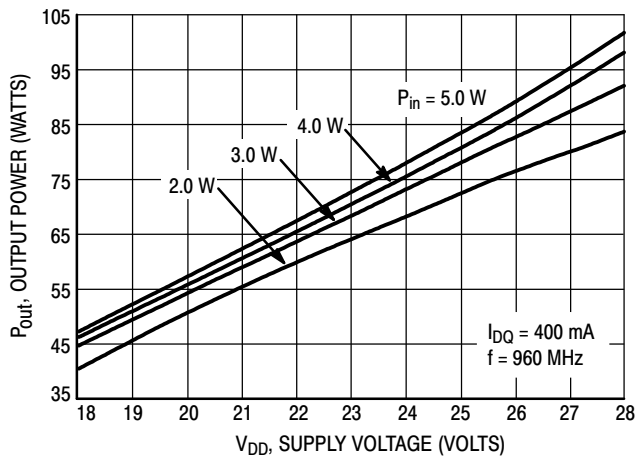
**Figure 3. Power Gain versus Output Power**



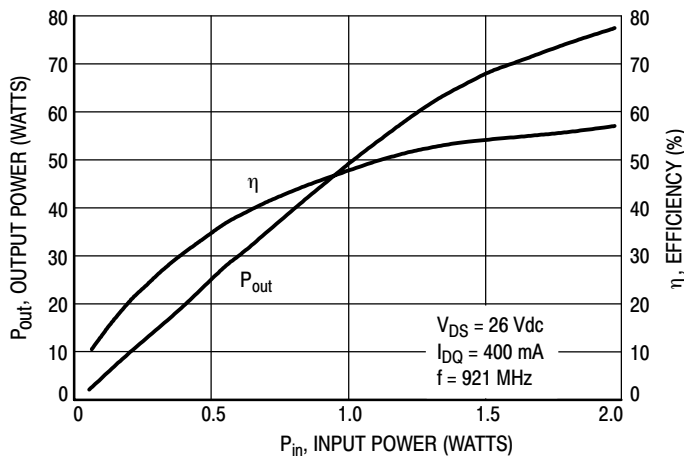
**Figure 4. Power Gain versus Output Power**



**Figure 5. Output Power versus Supply Voltage**

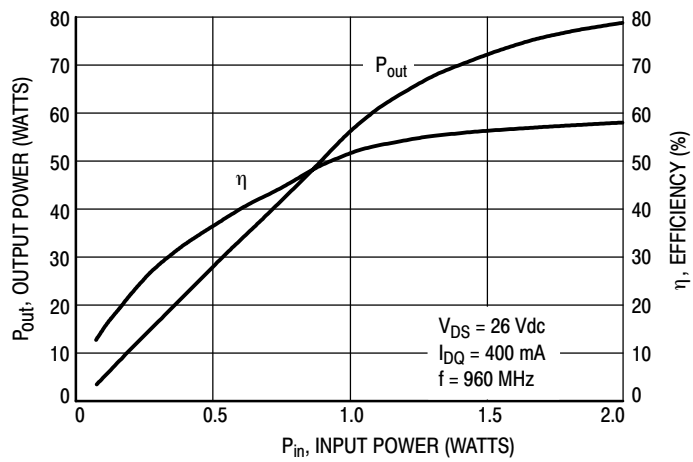


**Figure 6. Output Power versus Supply Voltage**

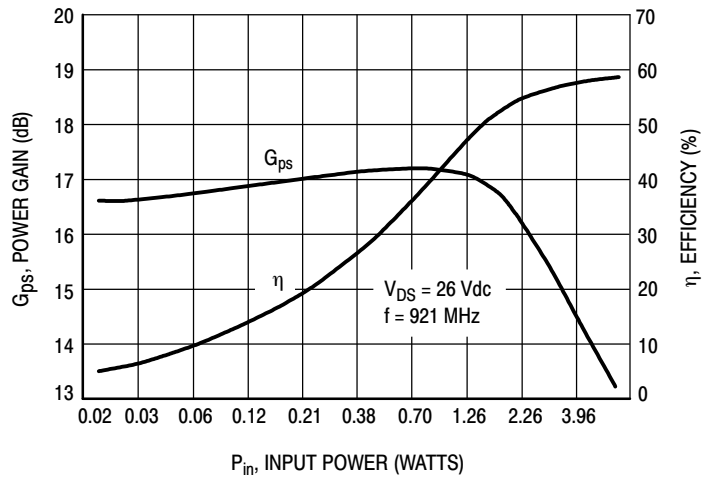


**Figure 7. Efficiency and Output Power versus Input Power**

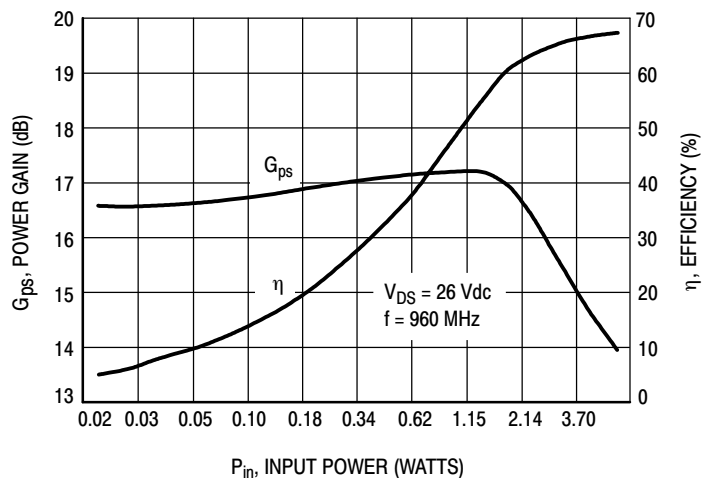
## TYPICAL CHARACTERISTICS



**Figure 8. Efficiency and Output Power versus Input Power**



**Figure 9. Power Gain and Efficiency versus Input Power**



**Figure 10. Power Gain and Efficiency versus Input Power**

## TYPICAL CHARACTERISTICS

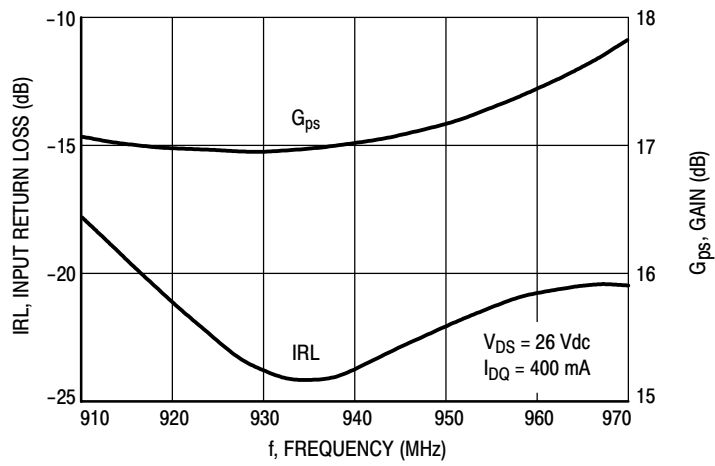
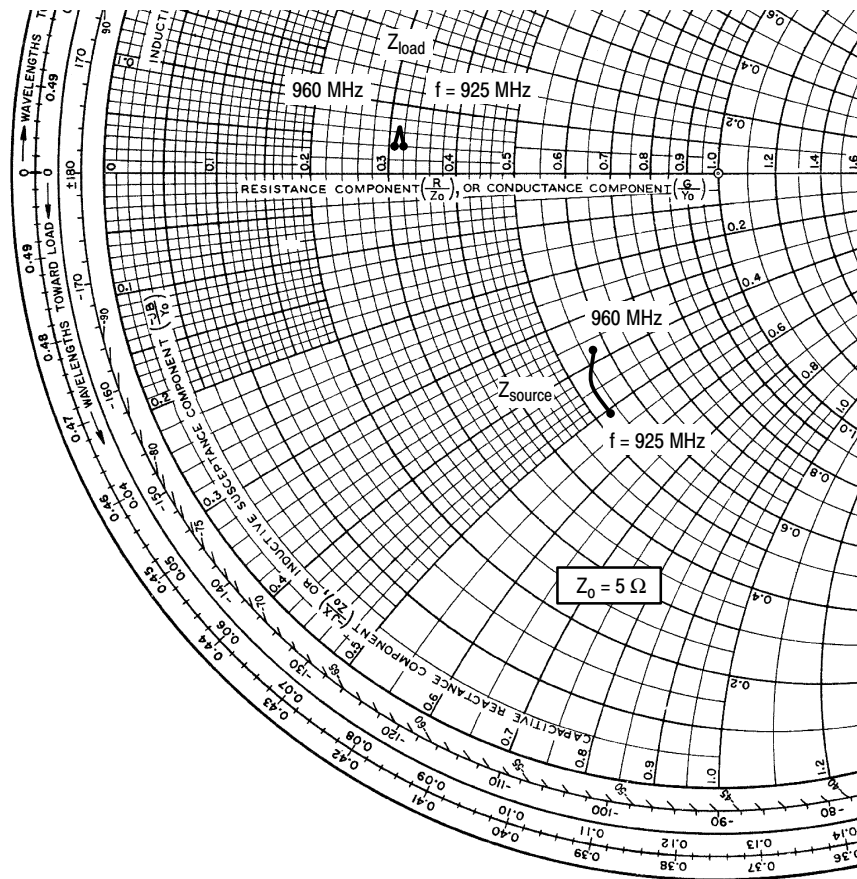


Figure 11. Performance in Broadband Circuit (at Small Signal)



$V_{SUPPLY} = 26 \text{ Vdc}$ ,  $I_{BIAS} = 400 \text{ mA}$ ,  $CW = \text{Room Temperature}$

f MHz	$Z_{source}$ $\Omega$	$Z_{load}$ $\Omega$
925	$2.65 - j2.53$	$1.62 + j0.2$
940	$2.67 - j2.14$	$1.56 + j0.34$
960	$2.85 - j1.87$	$1.55 + j0.2$

$Z_{source}$  = Test circuit impedance as measured from gate to ground.

$Z_{load}$  = Test circuit impedance as measured from drain to ground.

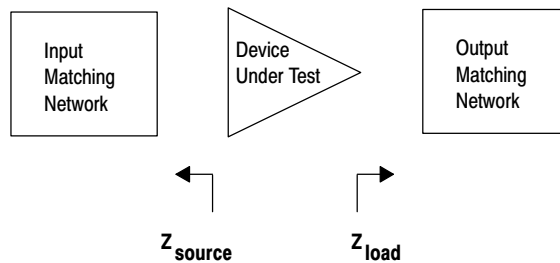


Figure 12. Series Equivalent Source and Load Impedance

# NOTES

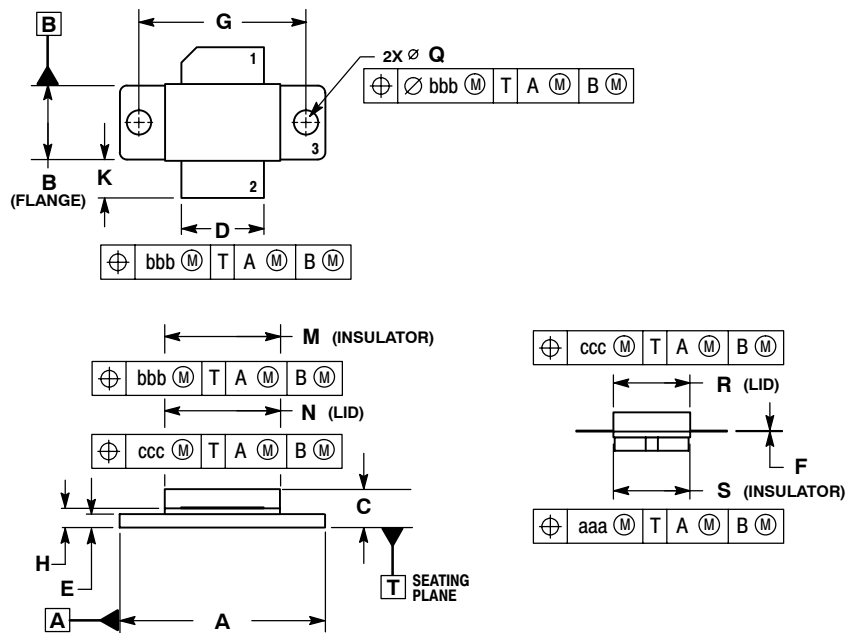




# NOTES

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## PACKAGE DIMENSIONS



**NOTES:**

1. INTERPRET DIMENSIONS AND TOLERANCES PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.065	1.075	27.05	27.30
B	0.380	0.390	9.65	9.91
C	0.160	0.205	4.06	5.21
D	0.425	0.435	10.80	11.05
E	0.060	0.070	1.52	1.78
F	0.004	0.006	0.10	0.15
G	0.870 BSC		22.10 BSC	
H	0.096	0.106	2.44	2.69
K	0.190	0.223	4.83	5.66
M	0.594	0.606	15.09	15.39
N	0.591	0.601	15.01	15.27
Q	0.124	0.130	3.15	3.30
R	0.394	0.404	10.01	10.26
S	0.395	0.405	10.03	10.29
aaa	0.005 REF		0.13 REF	
bbb	0.010 REF		0.25 REF	
ccc	0.015 REF		0.38 REF	

- STYLE 1:  
 PIN 1. DRAIN  
 2. GATE  
 3. SOURCE

**CASE 465D-05  
 ISSUE D  
 NI-600**

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