SC908

Power Management IC for Single-Cell Li-Ion Devices

POWER MANAGEMENT

Features

- Single Cell Li-Ion battery charger — CC/CV charging with current soft start
- Charger regulated output voltage — 4.2V ±1% over temperature with Kelvin sense of battery voltage
- Charger input protection withstands 28V indefinitely
- Charger max constant current setting — 500mA
- Adjustable charge termination current down to 10mA
- Battery NTC interface disables charging if battery temperature out of range
- Programmable low battery detector threshold
- Four status indicators
- Programmable charge completion timer
- Buck converter with enable — output programmable from 1V to 3V, 150mA max output
- Buck converter efficiency — 88% at 50mA
- General purpose low noise LDO regulator with fast enable, active shutdown
- 4x4x0.9 (mm) MLPQ package
- WEEE and RoHS compliant

Applications

- Bluetooth headsets
- MP3 players
- Low cost mobile phones

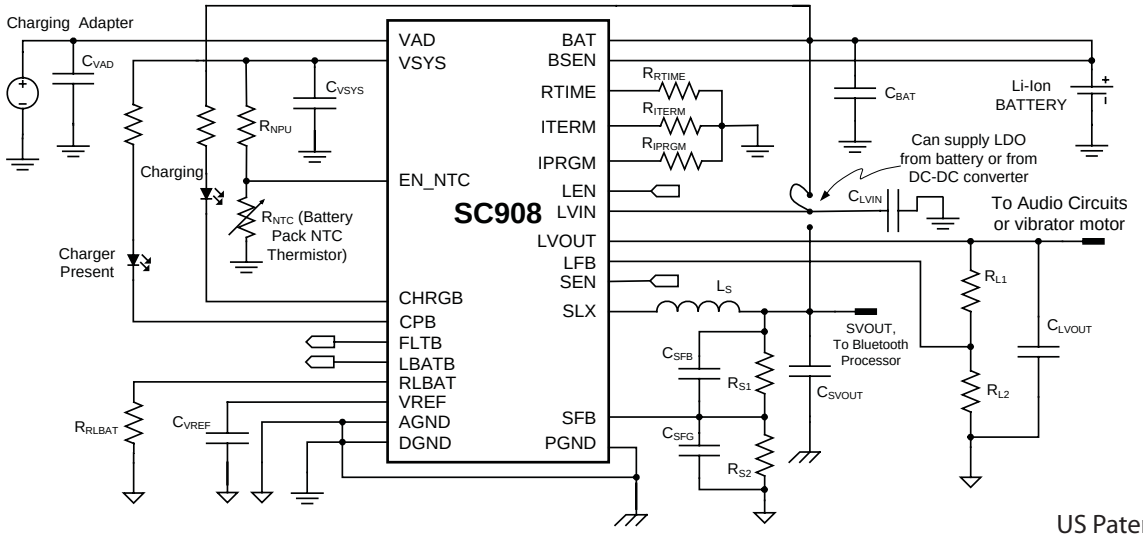
Description

The SC908 is a complete power management system designed for use in Bluetooth wireless headsets, portable media players, and other battery-powered electronics where size is critical. Included are a full featured stand-alone Li-Ion battery charger with a programmable low-battery monitor, a low noise LDO regulator, and a DC-DC buck converter.

Battery charging features include programmable pre-charge, fast-charge, and termination current settings. Charge termination is controlled by a programmable timer and by a resistor that sets the termination current. The 28V max input voltage protects against hotplug over-shoot and faulty adapters without additional protection circuitry. The battery voltage Kelvin sense input elimi-nates errors due to high charging currents. A battery thermistor interface disables charging when the battery temperature exceeds safe-to-charge limits.

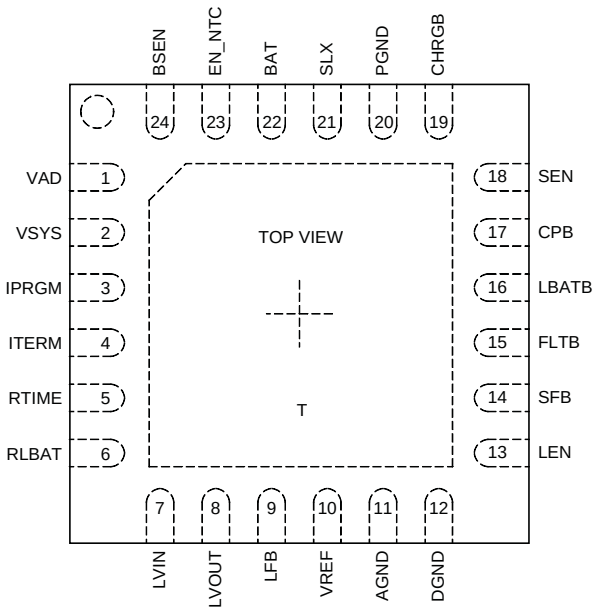
The step-down switching regulator (buck converter) improves system efficiency and extends battery life. The LDO regulator can be powered directly from the battery or from the buck converter output when efficiency is criti-cal. The fast-starting low noise LDO regulator is suitable for audio, RF, or general purpose regulation required by peripheral devices, such as a vibrating alert motor. The low battery detector warns when the battery level is below 3.3V, and when the battery has discharged below a lower programmable voltage limit.

Typical Application Circuit



US Patent: 6,836,095

Pin Configuration



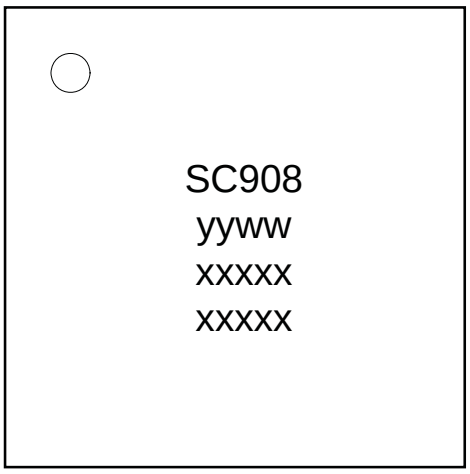
MLP-24; 4x4, 24 LEAD
θ_{JA} = 29°C/W

Ordering Information

Device	Package
SC908MLTRT(1,2)	MLPQ-24
SC908EVB	Evaluation Board

Notes:
(1) Available in tape and reel only. A reel contains 3,000 devices.
(2) Lead-free package only. Device is WEEE and RoHS compliant.

Marking Information



yy = year of manufacture
ww = week of manufacture
xxxx = lot number

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Absolute Maximum Ratings(1)

VAD (V) ..... -0.3 to +28.0
BAT, VSYS, CHRGB, FLTB, LBATB (V) ..... -0.3 to +5.5
CPB (V) ..... -0.3 to V_{SRC} (2) + 0.3
SLX, LVIN, LEN, SEN (V) ..... V_{BAT} + 0.3
LVOUT ..... V_{LVIN} + 0.3
AGND ..... -0.3 to +0.3
PGND ..... -1.0 to +0.3
Pin Voltage — All Other Pins (V) ..... -0.3 to +6.5
BAT Output Current (A) 1
BAT Short Circuit Duration (s) ..... Continuous
DC-DC Converter Output Current (mA)(3) ..... -265, +180
DC-DC Converter Output Current (mA)(4) ..... ±600
Total Power Dissipation (W) 2
ESD Protection Level (kV) (5) 2

Recommended Operating Conditions

Ambient Temperature Range (°C) ..... -40 to +85
Charger Input Voltage Range (V) ..... 4.45 to 7.05
LDO Regulator Input Voltage Range (V) ..... 2.2 to V_{BAT}
Switching Regulator Input Voltage (V) ..... V_{BAT}

Thermal Information

Thermal Resistance, Junction to Ambient (°C/W)(6) 29
Junction Temperature Range (°C) ..... -40 to +150
Storage Temperature Range (°C) ..... -65 to +150
IR Reflow Temperature (°C) ..... +260

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:
(1) All absolute maximum ratings are with respect to DGND unless otherwise noted.
(2) V_{SRC} = larger of V_{BAT} and V_{VSYS}
(3) Continuous
(4) Peak
(5) Tested according to JEDEC standard JESD22-A114-B.
(6) Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Test Conditions: V_{VAD} = 4.75V to 5.25 V; V_{BAT} = 3.7V; $V_{LEN} = V_{VAD}$; Typ values at 25°C; Min and Max at -40°C < T_A < 85°C, unless specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Charger						
VAD Input Voltage	VAD_{OP} (1)	Operating Voltage	4.45	5	7.05	V
	VAD_{UVLO-R}	UVLO Rising Threshold	4.05	4.25	4.45	V
	VAD_{UVLO-F}	UVLO Falling Threshold	3.8	4	4.2	V
	VAD_{UVLO-H}	UVLO Hysteresis (VAD_{UVLO-R} - VAD_{UVLO-F})	150			mV
	VAD_{OVP-R}	OVP Rising Threshold		7.5	7.80	V
	VAD_{OVP-F}	OVP Falling Threshold	7.05	7.3		V
	VAD_{OVP-H}	OVP Hysteresis (VAD_{OVP-R} - VAD_{OVP-F})	50			mV
Battery Leakage Current (2)	$Ileak_{BAT}$	V_{VAD}=V_{SEN}=V_{LEN}=0V, V_{BAT}=4.2V		0.1	2	µA

Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Charger (continued)						
Charging Adapter Operating Current	VAD_{ICCQ}	$V_{EN\_NTC} = 0.5 \times V_{VSYS}$, $I_{CPB} = I_{CHRGB} = I_{FLTB} = I_{LBATB} = I_{ITERM} = I_{IPRGM} = 0mA$, $V_{SEN} = V_{LEN} = 0V$		1.5		mA
CV Regulation Voltage	V_{CV}	Measured at BSEN pin $20mA < I_{BAT} < 500mA$ $0°C < T_J < 125°C$	4.16	4.2	4.24	V
Precharge Threshold (Rising)	VT_{PreQ}	Measured at BSEN pin	2.7	2.8	2.9	V
Recharge Threshold (Falling)	VT_{ReQ}	$V_{CV} - V_{BSEN}$	65	113	160	mV
VSYS output voltage [3]	V_{VSYS}	$V_{VAD} \geq 5V$, $I_{VSYS} \leq 5mA$		4.7		V
VSYS output current	I_{VSYS}				5	mA
ITERM Programming Resistor	R_{ITERM}	Nominal 1%-tol Standard Value	2.67		17.4	kΩ
I_{BAT} Pre-Charge Current	I_{PreQ}	$R_{ITERM} = 4.99k\Omega$ to GND	27	39	52	mA
I_{BAT} Termination Current	I_{TERM}	$R_{ITERM} = 4.99k\Omega$ to GND	27	39	52	mA
IPRGM Programming Resistor	R_{IPRGM}	Nominal 1%-tol Standard Value	2.15		15.0	kΩ
I_{BAT} Fast-Charge Current	I_{FQ}	$R_{IPRGM} = 6.04k\Omega$, $V_{BAT} = 3.7V$	167	173	179	mA
VAD - BAT Dropout Voltage	V_{DO}	$I_{BAT} = 500mA$, $0°C \leq T_J \leq 85°C$			0.8	V
IPRGM Regulated Voltage	V_{IPRGM}	$R_{IPRGM} = 6.04k\Omega$ to GND	1.45	1.5	1.55	V
ITERM Regulated Voltage	V_{ITERM}	$R_{ITERM} = 4.99k\Omega$ to GND	1.45	1.5	1.55	V
RTIME Regulated Voltage	V_{RTIME}	$R_{RTIME} = 37.4k\Omega$ to GND	1.475	1.56	1.625	V
Precharge Fault Time-Out	t_{PreQF}	$R_{RTIME} = 37.4k\Omega$ to GND	38	47	57	mins
		R_{RTIME} connected to VSYS	32	42	53	mins
Charge Complete Time-Out	t_{QComp}	$R_{RTIME} = 37.4k\Omega$ to GND	2.50	3.10	3.70	hrs
		R_{RTIME} connected to VSYS	2.10	2.67	3.50	hrs
EN_NTC Thresholds	VT_{NTC_DIS}	Charger Disable/Reset (Falling)	9	10	11.5	$\%V_{VSYS}$
	VT_{NTC_HF}	NTC Hot (Falling)	27.5	30	31.5	$\%V_{VSYS}$
	VT_{NTC_CR}	NTC Cold (Rising)	74	75	76.5	$\%V_{VSYS}$
EN_NTC Hysteresis	VT_{NTC_HYS}	$V_{VAD} = 5V$		45		mV
EN_NTC Disable/Reset Hold Time	$t_{NTC\_DIS\_H}$	Momentary disable resets charger	500			ns
Charger Over-Temperature Shut-down Temperature (Rising)	T_{CHRGR_OT}	Hysteresis = 10°C typical		145		°C

Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Core Functions (Excluding Charger)						
Core Circuits Quiescent Current (4)	$I_{Q\text{-}Core}$	$V_{VAD} = V_{SEN} = 0V$, $V_{LEN} = V_{BAT} = 4.2V$		100		µA
VREF Reference Voltage	V_{VREF}			0.75		V
VREF Power Supply Rejection	$PSRR_{REF}$	V_{BAT} = 3.7V with 0.5$V_{P\text{-}to\text{-}P}$ ripple, f ≤ 10kHz, C_{VREF} = 10nF		70		dB
VREF Reference Voltage Start-Up Time (5, 10)	t_{SU_REF}	Delay from first of SEN high LEN high, V_{BAT} = 3.7V C_{VREF} = 10nF VREF from 0V to 95% of final		0.4		ms
DC-DC Buck Converter						
Buck Converter Input Voltage	V_{SVIN}	BAT pin is also the switching regulator supply input		V_{BAT}		V
Buck Converter Under-Voltage Lockout Rising Threshold	$VT_{SUVLO\text{-}R}$				2.8	V
Buck Converter Under-Voltage Lockout Falling Threshold	$VT_{SUVLO\text{-}F}$		2.55			V
Buck Converter Under-Voltage Lockout Hysteresis	$VT_{SUVLO\text{-}HYS}$			84		mV
Buck Converter Quiescent Current (2)	$I_{BAT\text{-}Q}$	$V_{SEN} = V_{BAT}$, I_{SVOUT} = 10mA Low I_Q mode of P_{SAVE}		115		µA
Buck Converter Minimum On-Time	t_{SON_MIN}				60	ns
Buck Converter Maximum Duty Cycle (10)	SDC_{MAX}		92			%
Buck Converter Program Output Voltage Minimum (6,10)	V_{SVOUT_MIN}				1	V
Buck Converter Program Output Voltage Maximum(6,7,8,10)	V_{SVOUT_MAX}	$V_{BAT} \geq V_{SVOUT\_MAX}/SDC_{MAX}$+150mV	3			V
Buck Converter Feedback Regulation Voltage	V_{SFB}		0.480	0.500	0.520	V
Buck Converter Output Voltage(6)	V_{SVOUT}	V_{BAT} = 3.7V, L = 4.7µH I_{SVOUT} = 100mA R_{S1} = 340kΩ, R_{S2} = 100kΩ		2.2		V
Buck Converter Line Regulation(6)	V_{SVOUT_LINE}	2.8V ≤ V_{BAT} ≤ 4.5V I_{SVOUT} = 100mA R_{S1} = 340kΩ, R_{S2} = 100kΩ	-0.3		0.3	%/V
Buck Converter Load Regulation (6)	V_{SVOUT_LOAD}	5mA ≤ I_{SVOUT} ≤ 150mA V_{BAT} = 3.7V R_{S1} = 340kΩ, R_{S2} = 100kΩ		0.002		%/mA

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Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
DC-DC Buck Converter (continued)						
Buck Converter P-Channel Peak Current Limit	I_{LIM_P}		410	440	470	mA
Buck Converter P-Channel On-Resistance	$R_{DS(ON)P}$	I_{SVOUT} = 150mA		0.75		Ω
Buck Converter N-channel On-Resistance	$R_{DS(ON)N}$	I_{SVOUT} = 150mA		1.05		Ω
Buck Converter Oscillator Frequency	f_{OSC}		0.85	1.00	1.15	MHz
Buck Converter Start-Up Time (5,10)	$t_{SU-SVOUT}$	I_{SVOUT} = 150mA, V_{SVOUT} to 95% V_{SVOUT} = 1V V_{SVOUT} = 1.8V V_{SVOUT} = 2.2V V_{SVOUT} = 3.0V		0.3 1.3 1.45 1.8	2	ms
Linear Low Drop-Out (LDO) Regulator						
LDO Input Voltage	V_{LVIN}	V_{BAT} ≥ 2.8V	2.2		V_{BAT}	V
LDO Under Voltage Lockout Rising Threshold	$VT_{LUVLO-R}$			1.95	2.05	V
LDO Under Voltage Lockout Falling Threshold	$VT_{LUVLO-F}$		1.75	1.85		V
LDO Under Voltage Lockout Hysteresis	$VT_{LUVLO-HYS}$			120		mV
LDO Nominal Output Voltage Minimum (10)	V_{LVOUT_MIN}	V_{LVIN} > V_{LVOUT} +300mV			1.5	V
LDO Nominal Output Voltage Maximum (10)	V_{LOUT_MAX}	V_{LVIN} > V_{LVOUT} +300mV	3.3			V
LDO Feedback Regulation Voltage	V_{LFB}	V_{LVIN} = 3.7V, I_{LVOUT} = 1mA		0.75		V
LDO Output Voltage	V_{LVOUT}	R_{L1} = 54.9kΩ, R_{L2} = 39.2kΩ V_{LVIN} = 3.7V, I_{LVOUT} = 1mA	1.73	1.8	1.85	V
LDO Dropout Voltage	V_{L_DO}	V_{LVOUT} = 2.2V, I_{LVOUT} = 100mA		115	200	mV
		V_{LVOUT} = 3.0V, I_{LVOUT} = 150mA		130	225	mV
LDO Load Regulation (with respect to 1mA load) (9)	ΔV_{LVOUT_LOAD}	R_{L1} = 54.9kΩ, R_{L2} = 39.2kΩ (V_{LVOUT} = 1.8V), V_{LVIN} = 2.2V 1mA ≤ I_{LVOUT} ≤ 100mA	-10		10	mV
		R_{L1} = 54.9kΩ, R_{L2} = 39.2kΩ (V_{LVOUT} = 1.8V), V_{LVIN} = 3.7V 1mA ≤ I_{LVOUT} ≤150mA	-10		10	mV

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Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Linear Low Drop-Out (LDO) Regulator (continued)						
LDO Line Regulation [9]	ΔV_{LVOUT_LINE}	2.2V ≤ V_{LVIN} ≤ 4.2V referenced to 3.7V, I_{LVOUT} = 1mA, RL1 = 54.9kΩ, RL2 = 39.2kΩ	-5		5	mV
LDO LVOUT/LVIN Power Supply Rejection Ratio	$PSRR_{LLVIN}$	V_{LVIN} = 3.7VDC with 0.5V P-to-P Ripple, f ≤ 10kHz, V_{BAT} = 3.7VDC V_{LVOUT} = 1.8V, I_{LVOUT} = 30mA		60		dB
LDO LVOUT/(BAT and LVIN) Power Supply Rejection Ratio	$PSRR_{LBAT}$	V_{LVIN} = V_{BAT} = 3.7VDC with 0.5V P-to-P Ripple, f ≤ 10kHz V_{LVOUT} = 1.8V, I_{LVOUT} = 30mA		60		dB
LDO Output Noise Voltage [9]	V_{L_NOISE}	10Hz ≤ f ≤ 100kHz C_{LVOUT} = 1µF, V_{LVOUT} = 3.0V V_{LVIN} = 3.7V, I_{LVOUT} = 50mA		50		μV_{RMS}
LDO Quiescent Current (I_{LVIN} - I_{LVOUT}) [4]	I_{LQ}	V_{LVIN} = V_{LEN} = V_{BAT} = 4.2V, V_{VAD} = 0V, I_{LVOUT} = 1mA		91		µA
LDO Current Limit	I_{L_LIM}	V_{LVOUT} = 0V, V_{LEN} = V_{BAT}	300	380	450	mA
LDO Start-Up Time [5, 10]	$t_{SU-LVOUT}$	Time from LEN (with V_{SEN} = V_{BAT}, disregard t_{SU_REF}), V_{LVOUT} from 0V to 95% of final		0.1		ms
		Time from LEN (with V_{VAD} = V_{SEN} = 0, t_{SU_REF} dominates) V_{LVOUT} from 0V to 95% of final		0		ms
LDO Turn-Off Time	$t_{TO-LVOUT}$	Time from LEN = 0, V_{LVOUT} from 100% to 10% of regulation		0.5		ms
Battery Voltage Detector						
Battery Detector Minimum Operating Voltage	V_{DET_MINOP}				2.3	V
Battery Detector Maximum Operating Voltage	V_{DET_MAXOP}		4.5			V
Battery Detector Voltage Warning, Decreasing	V_{WARN}	V_{DET_MINOP} ≤ $V_{Battery}$ ≤ V_{DET_MAXOP}	3.21	3.28	3.35	V
Battery Detector Voltage Fault, Decreasing	V_{DET}	R_{RLBAT} = 309kΩ		2.92		V
Battery Detector Threshold Hysteresis, Warning or Fault	V_{DET_HYS}	V_{DET_MINOP} ≤ $V_{Battery}$ ≤ V_{DET_MAXOP}	150	200	250	mV

Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Logic Control Inputs & Status Outputs						
Battery Detector Sense Leakage (BSEN Current)	I_{BSEN_DET}	$V_{VAD} > VAD_{UVLO}$, or SEN or LEN high, $V_{BSEN} = 4.2V$		5	10	µA
Battery Detector Activation Delay(10)	V_{DET_DEL}	Time from first of LEN or SEN high until LBATB/FAULTB valid, $V_{VAD} = 0V$		70		µs
Logic Input Low	V_{IL}	LEN, SEN; $V_{BAT} = 2.7V$	0.4			V
Logic Input High	V_{IH}	LEN, SEN; $V_{BAT} = 2.7V$			1.5	V
Logic Input Current High	I_{IL}	LEN, SEN; $V_{BAT} = 2.7V$			1	µA
Logic Input Current Low	I_{IH}	LEN, SEN; $V_{BAT} = 2.7V$			1.5	µA
CPB, CHRGB, FLTB, LBATB Outputs	V_{OL}	$I_{SINK} = 2mA$			0.5	V
	I_{OH}	V = 5V (V_{VAD} = 8V for CPB)			1	µA

Notes:

(1) VAD_{OP} is the "Maximum Vsupply" as defined in EIA/JEDEC Standard No. 78, paragraph 2.11.

(2) The value of the buck converter disabled battery leakage current is included in the charger section battery leakage since it cannot be independently measured (because SVIN is tied to BAT internally). The buck converter contribution to this value is also included in the Buck Converter section for design guidance only.

(3) VSYS regulation voltage assumes that V_{VAD} exceeds V_{VSYS} by the VSYS regulator dropout (typically 0.5V at 5mA, for a minimum regulator $R_{DS} = 71\Omega$). If this condition is not met, then $V_{VSYS} = V_{VAD}$ minus the VSYS regulator dropout.

(4) $I_{Q\text{-}Core}$ is the supply current from the battery for common reference circuits into the BAT pin when either the buck converter or LDO or charger are enabled.

(5) t_{SU_REF} is the start-up time of the voltage reference buffer for both the DC-DC buck converter and the LDO, and should be added to the start-up time ($t_{SU\text{-}SVOUT}$ or $t_{SU\text{-}LVOUT}$ respectively) of the first regulator enabled. In the case of the LDO start-up with the switcher disabled, the LDO start-up time $t_{SU\text{-}LVOUT}$ is concurrent with the reference start-up time t_{SU_REF}, and so $t_{SU\text{-}LVOUT}$ is specified as typically zero.

(6) SVOUT is the buck converter output node, which is the node at which the output inductor is connected to the load. It is the top of the feedback resistor divider network. See the Typical Application Circuit.

(7) To guarantee positive load threshold hysteresis for PSAVE-to-PWM mode switching with SVOUT > 2.2V, contact your Semtech representative for application assistance.

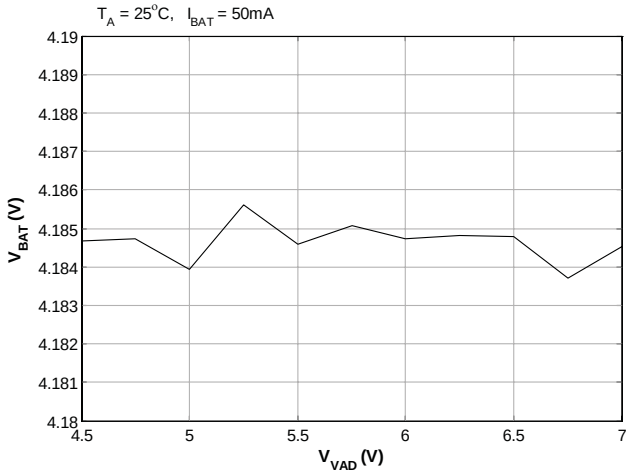
(8) If $V_{BAT} < V_{SVOUT\_Max} / SDC_{MAX} + 150mV$, then the maximum output setting is $V_{BAT} \times SDC_{MAX} + 150mV$. Higher output voltage settings are feasible, but are subject to load-dependent dropout.

(9) Specified with $V_{BAT} = V_{LVIN}$.

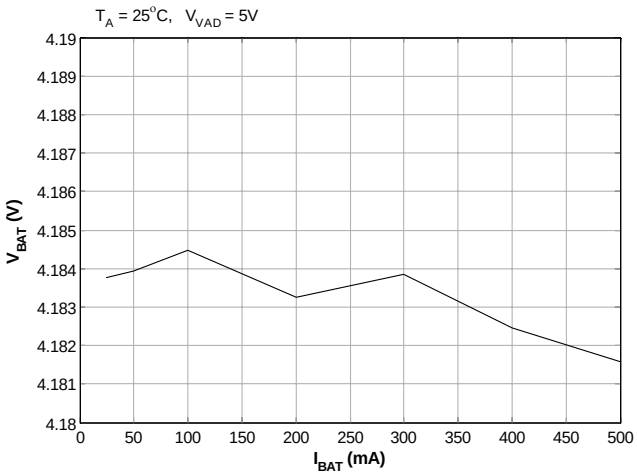
(10) Guaranteed by design.

Typical Characteristics

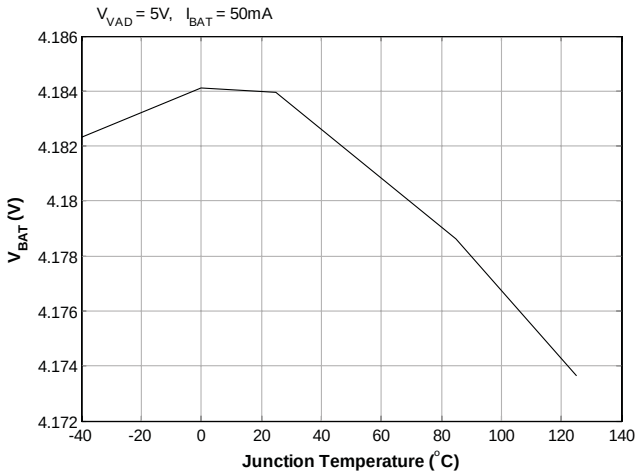
Charger CV Line Regulation



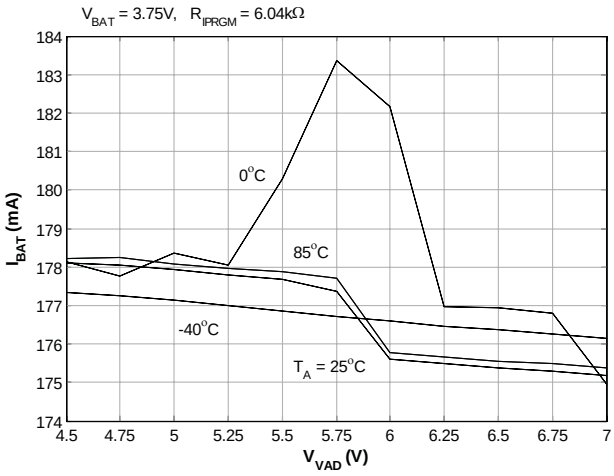
Charger CV Load Regulation



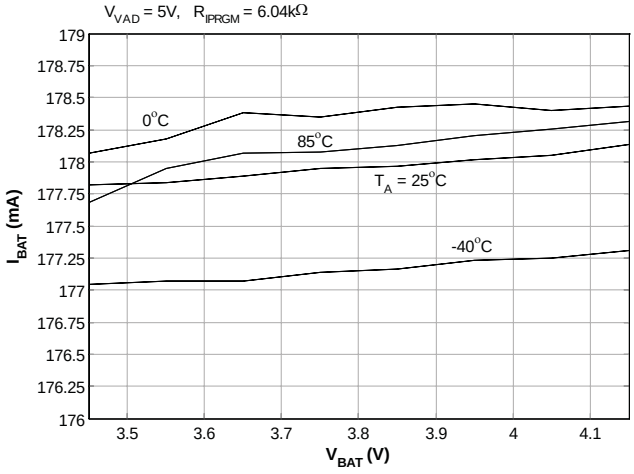
Charger CV Temperature Regulation



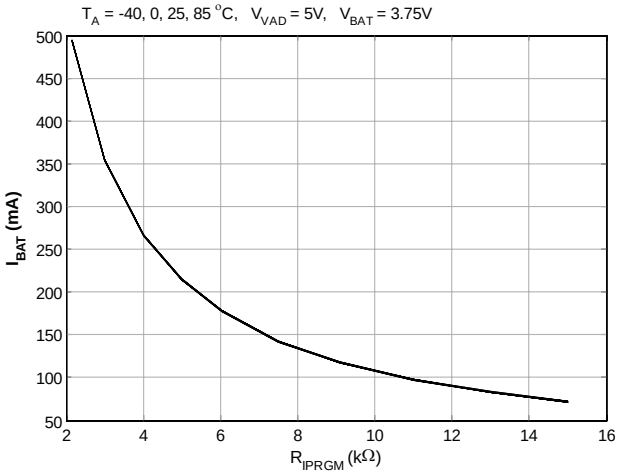
Charger CC Line Regulation



Charger CC V_{BAT} Regulation

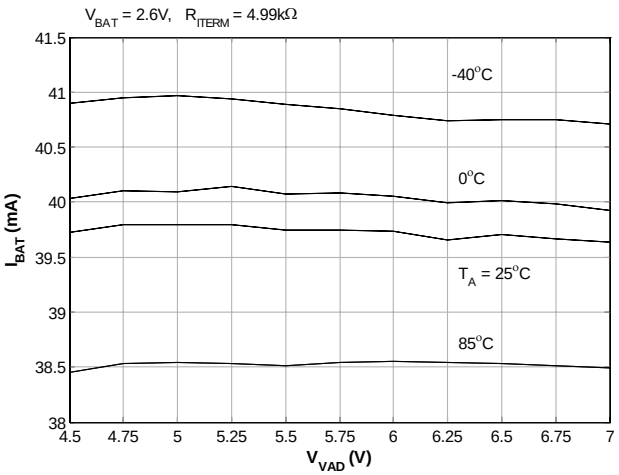


Charger CC I_{FQ} Programming

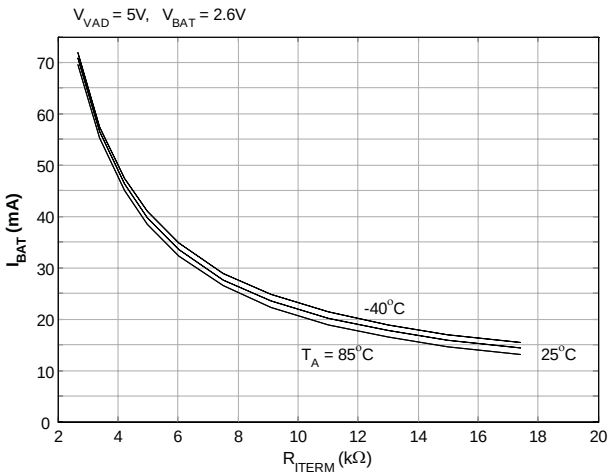


Typical Characteristics (continued)

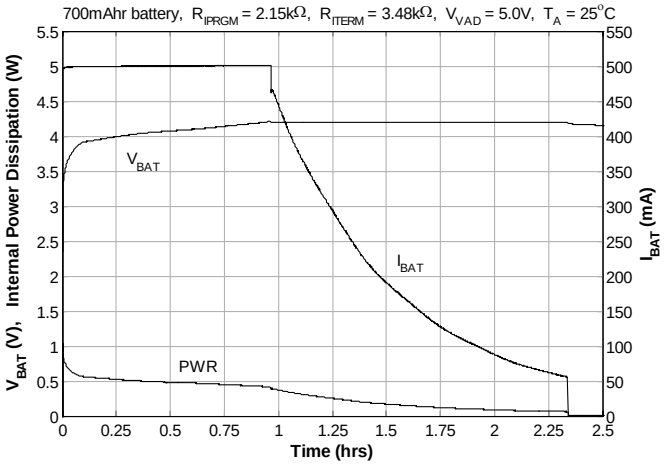
Charger I_{PreQ} Line Regulation



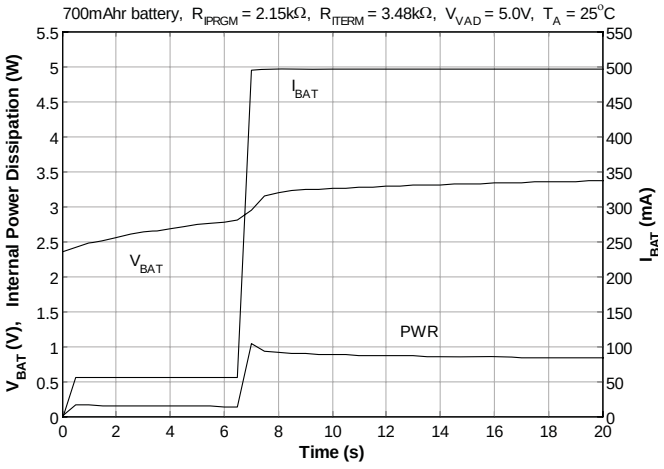
Charger I_{PreQ} Programming



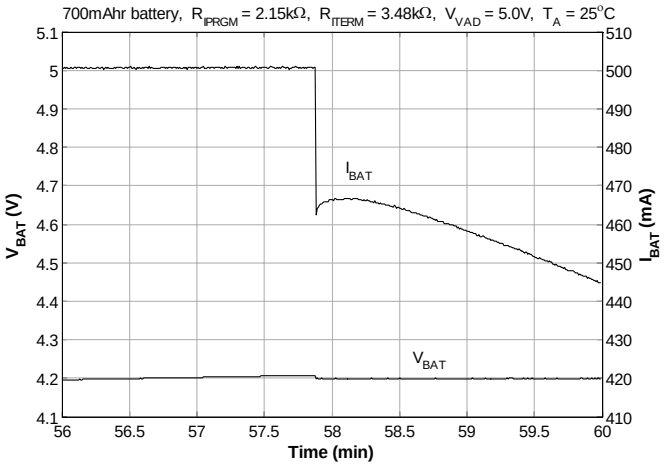
Charging Cycle Battery Voltage and Current



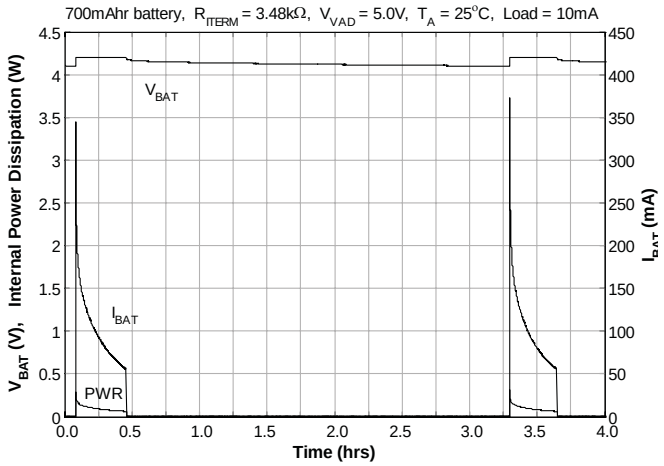
Pre-Charging Battery Voltage and Current



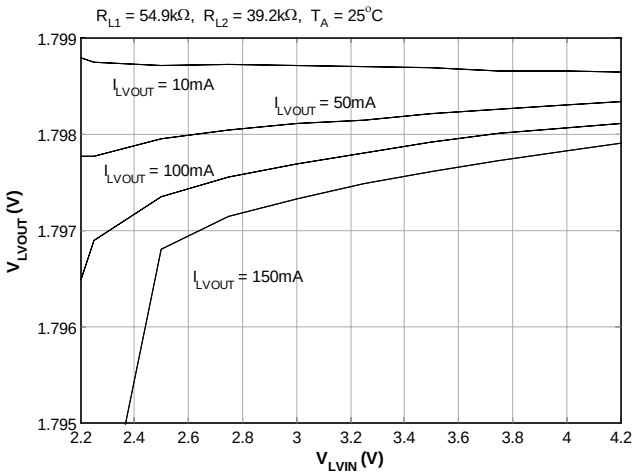
CC-to-CV Battery Voltage and Current



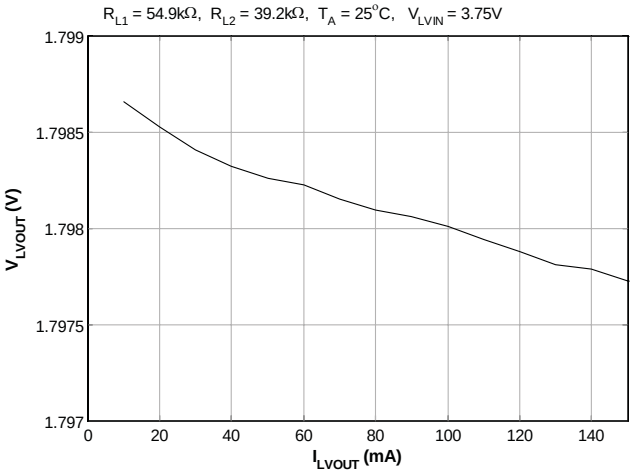
Re-Charge Cycle Battery Voltage and Current



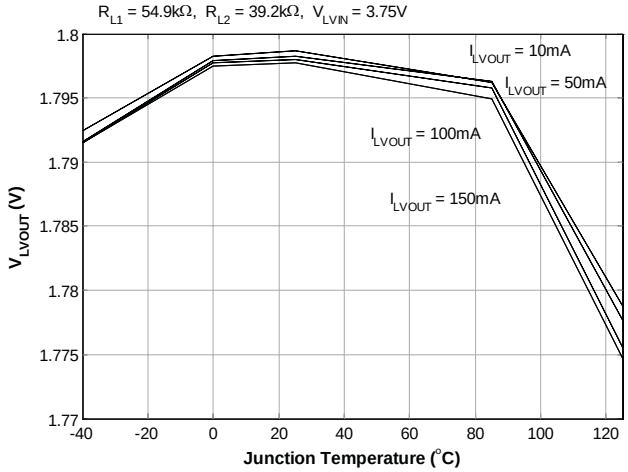
LDO Line Regulation



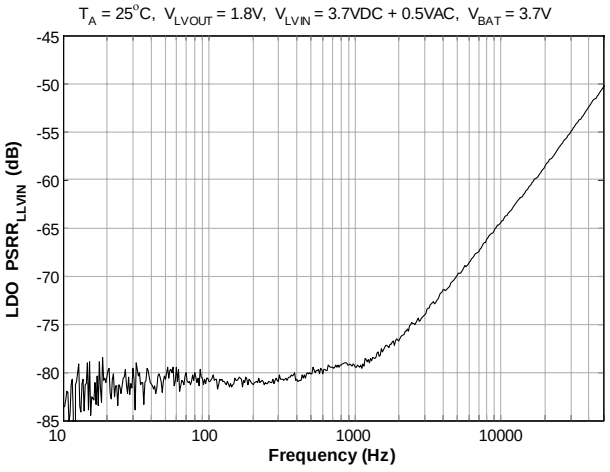
LDO Load Regulation



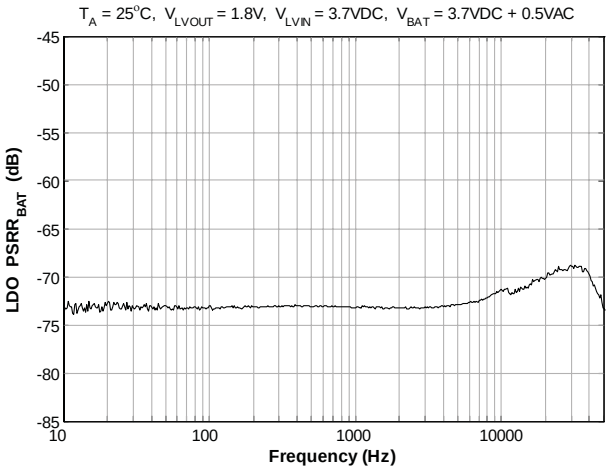
LDO Temperature Regulation



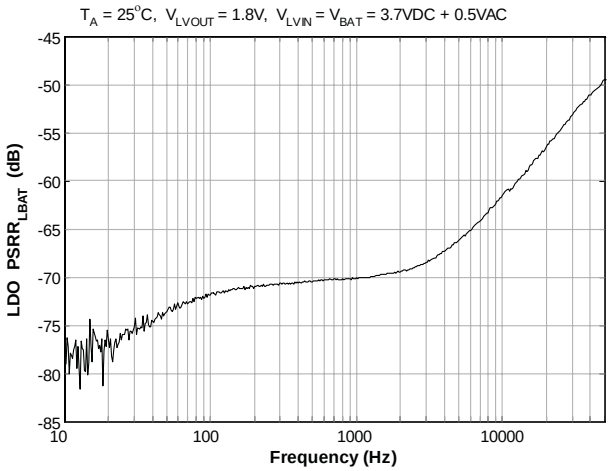
LDO PSRR, LVIN to LVOUT



LDO PSRR, BAT to LVOUT

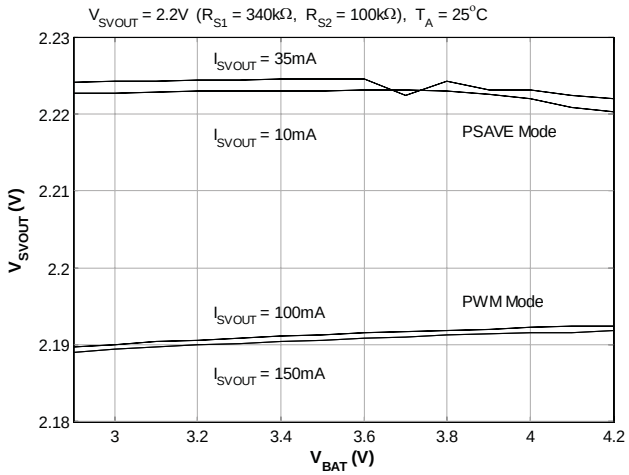


LDO PSRR, LVIN and BAT to LVOUT

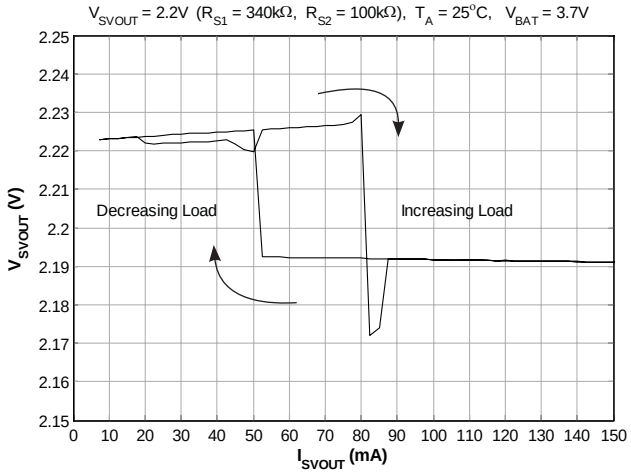


Typical Characteristics (continued)

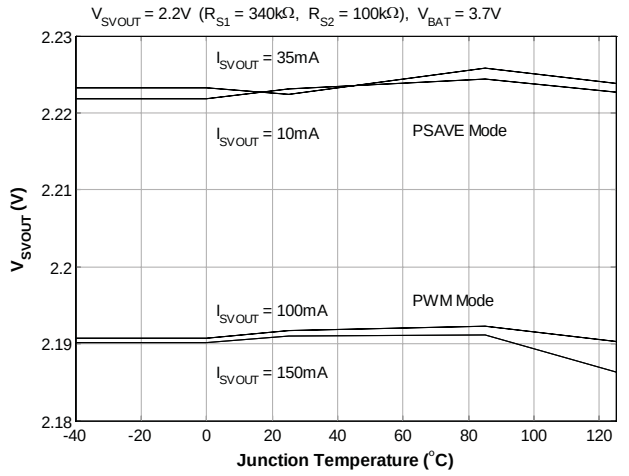
DC/DC Converter Line Regulation



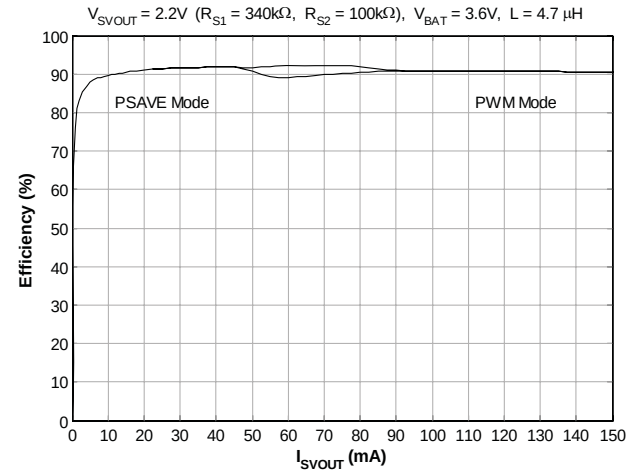
DC/DC Converter Load Regulation



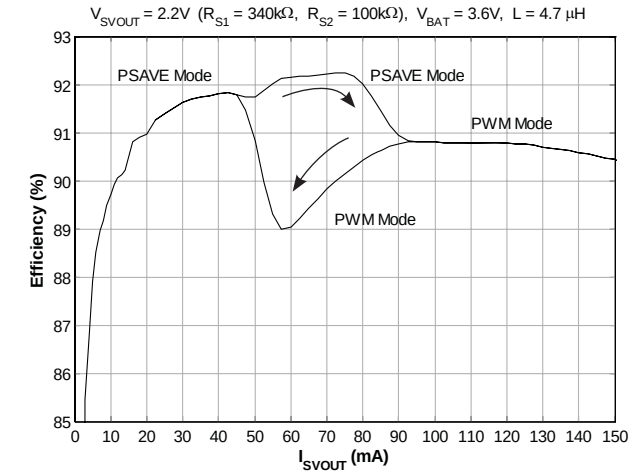
DC/DC Converter Temperature Regulation



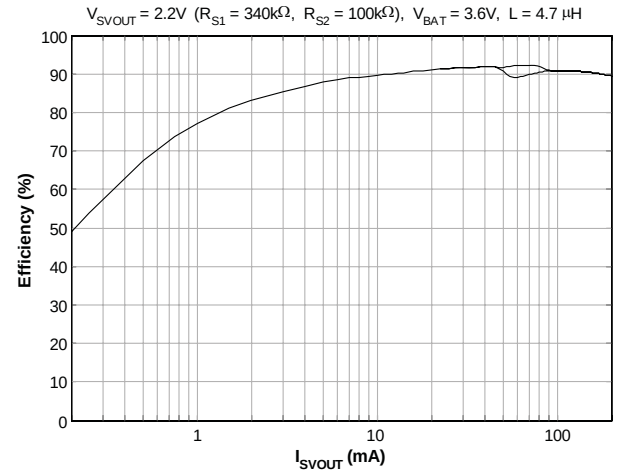
DC/DC Converter Efficiency



DC/DC Converter Efficiency Detail



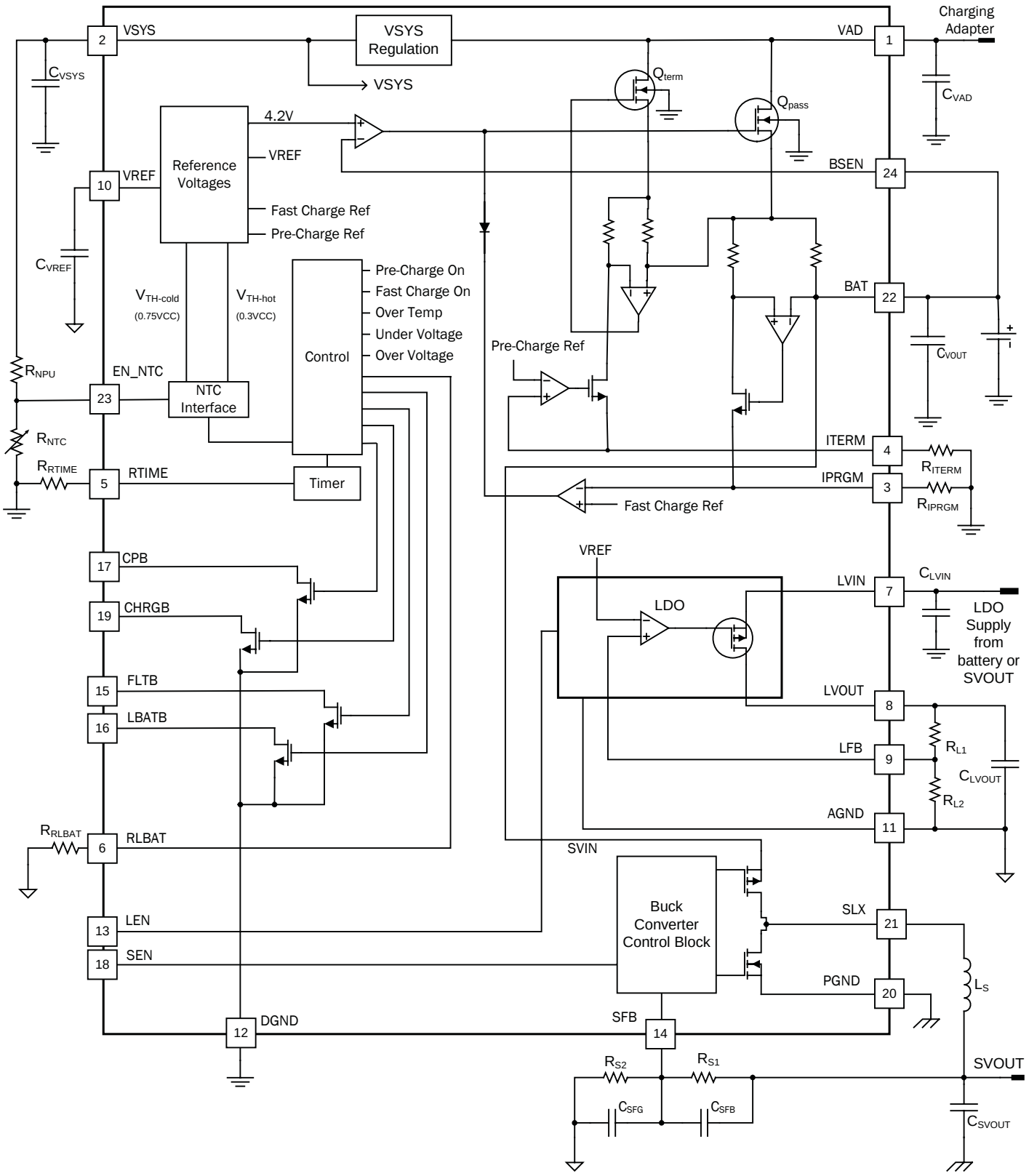
DC/DC Converter Efficiency — Low Loads



Pin Descriptions

Pin #	Pin Name	Pin Function
1	VAD	Charger input pin
2	VSYS	Adapter input internal-regulation node which also serves as supply for EN_NTC, RTIME, and all input-referenced (vs. battery-referenced or regulated output-referenced) pull-ups; load must not exceed 5mA.
3	IPRGM	Pin for setting constant current charging current — connect resistor to ground to set current.
4	ITERM	Pin for setting termination and precharge current — connect resistor to ground to set current.
5	RTIME	Charge timer pin — connect a resistor to ground to set timer, ground to disable the timer. Timer enabled with internally programmed default time is selected with RTIME tied to VSYS.
6	RLBAT	Resistor is connected to ground to set Low Battery voltage threshold.
7	LVIN	LDO voltage input — can be connected to either the battery supply (BAT) or the switching regulator output (SVOUT). No other connections are permitted.
8	LVOUT	LDO voltage output
9	LFB	LDO feedback voltage input
10	VREF	Bandgap reference bypass pin — connected to a 10nF capacitor to analog ground. No other connections are permitted.
11	AGND	Analog ground pin — refer to grounding considerations in application section.
12	DGND	Digital ground pin — refer to grounding considerations in application section.
13	LEN	LDO enable pin — active high
14	SFB	DC-DC converter feedback input — connect voltage divider from output to this pin to set output voltage.
15	FLTB	Charging Fault indicator — open drain output is active low when a charging fault has occurred. Also, together with LBATB, indicates when battery discharges below a programmable voltage set by RLBAT resistor.
16	LBATB	Low Battery indicator — open drain output is active low when battery discharges below 3.3V, and, together with LBATB, indicates when battery discharges below a programmable voltage set by RLBAT resistor.
17	CPB	Charger Present indicator — open drain output is active low when a valid VAD input voltage is present.
18	SEN	DC-DC converter enable pin — active high
19	CHRGB	Charging-In-Progress indicator — open drain output is active low when charging until charging current drops below the programmed termination current, or until charging is disabled by charge timeout or EN_NTC disable or NTC temperature fault.
20	PGND	DC-DC converter power ground pin — No other connection is permitted.
21	SLX	DC-DC converter output — connect to an inductor between this point and SVOUT (the DC-DC converter load connection).
22	BAT	Charger output pin, also DC-DC converter input pin — connect to the positive battery terminal.
23	EN_NTC	NTC thermistor input — charger is enabled if voltage is between 0.3 × VSYS and 0.75 × VSYS. Charger is disabled if voltage is below 1V. Battery temperature fault otherwise.
24	BSEN	Battery Kelvin sense pin — independent connection is tied directly to the battery positive terminal.
T	Thermal Pad	Connect to ground plane with thermal vias directly under pad.

Block Diagram With Typical Application Circuit



Applications Information

Charger Operation

The SC908 Li-Ion battery charger can be configured independently with respect to fast-charge, termination current, and timing. The charging and battery voltage status are indicated by the four status outputs.

A charge cycle is initiated when the power adapter is connected to the device and the SC908 VAD pin voltage is between the Under-Voltage LockOut (UVLO) rising threshold and the input Over Voltage Protection (OVP) threshold. If the battery voltage is less than the pre-charge threshold, the output current is regulated to the programmed pre-charge current. When the pre-charge threshold voltage is exceeded, the fast-charge Constant Current (CC) mode begins, with the charge current rising to the programmed fast-charge current in three soft-start current steps. The charger enters the Constant Voltage (CV) mode when the battery voltage rises to its final value (V_{CV}), typically 4.2V. In the CV mode the BAT voltage is regulated to V_{CV}, and as the battery continues to charge it accepts decreasing current. The CHRGB output turns off when I_{BAT} drops below the programmed termination current. If the charge timer is active, the battery is held in the CV charge mode until the timer cycle ends. The charger then enters the monitor mode, where the output remains off until the voltage at BAT drops by VT_{ReQ}, and a new charge cycle is initiated. If the charge timer is disabled, the monitor mode is immediately entered upon charge termination.

Pre-Charge Mode

The pre-charge mode is automatically entered when the battery voltage is below the pre-charge threshold voltage, which preconditions the battery for fast charging. The pre-charge current value is set by the resistor on the ITERM pin, and is programmable from 14mA to 65mA. The pre-charge current is determined by

$$I_{PreQ} = \frac{V_{ITERM\_Typ}}{R_{ITERM}} \times 130$$

where V_{ITERM_Typ} designates the typical value of V_{ITERM}. (See the Termination Current section for precharge current accuracy.) When the timer is enabled, there is a maximum allowed pre-charge duration. If the pre-charge time exceeds 25% of the total charge cycle, the charger will turn off due to a pre-charge fault. This fault is cleared when VAD is cycled off and on, or when the EN_NTC pin is forced low to disable the charger.

Fast-Charge Constant Current Mode

The fast-charge CC mode is active when the battery voltage is above VT_{PreQ} and less than V_{CV}. The current can be set to a maximum of 0.5A and is selected by the program resistor on the IPRGM pin. The voltage on this pin represents the charger output current. This allows the charging current to be measured by sensing the IPRGM pin voltage using a general purpose Analog-to-Digital Converter (ADC) and the host microporocessor. The fast-charge current is determined by

$$I_{FQ} = \frac{V_{IPRGM\_Typ}}{R_{IPRGM}} \times 697$$

Excellent fast-charge current accuracy is obtained by the use of a patented polarity-switched current sense amplifier (US Patent 6,836,095). This nullifies current measurement offset errors, leaving only a small gain error. The range of expected fast-charge output current versus programming resistance R_{IPRGM} is shown in Figures 1a and 1b.

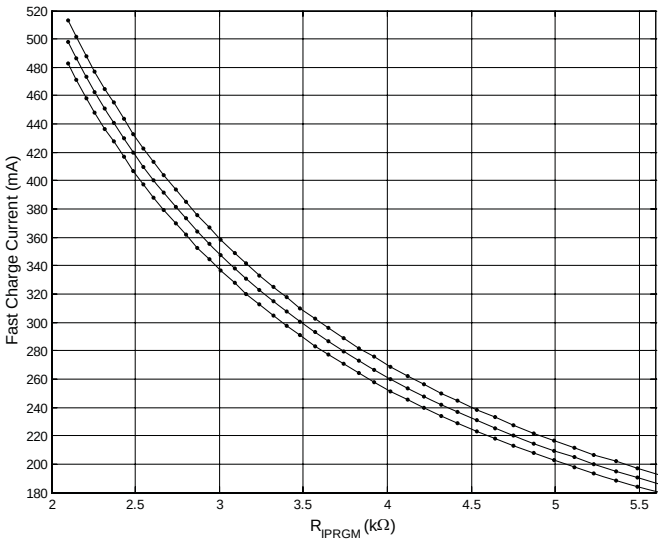


Figure 1a — Fast-charge Current Variation vs. IPRGM Resistance, Low Resistance Range

Applications Information (continued)

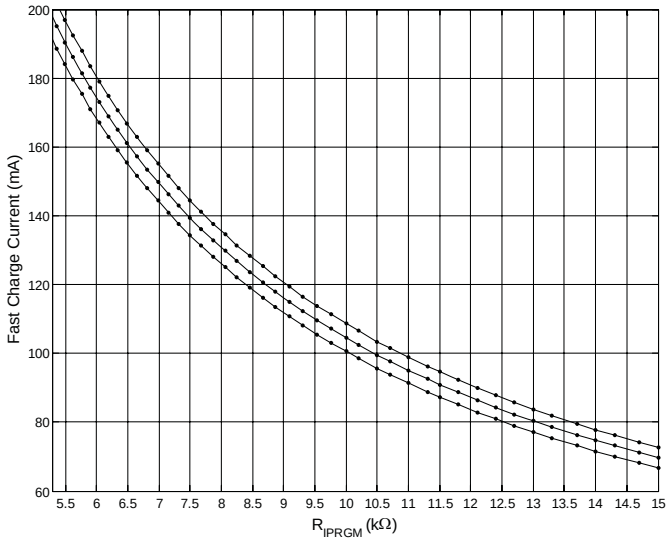


Figure 1b — Fast-charge Current Variation vs. IPRGM Resistance, High Resistance Range

The figures show the nominal current versus nominal R_{IPRGM} resistance as the center plot and two theoretical limit plots indicating maximum and minimum current versus nominal programming resistance. These plots are derived from models of the expected worst-case contribution of error sources depending on programmed current. The current range includes the uncertainty due to 1% tolerance resistors. The dots on each plot indicate the currents obtained with standard value 1% tolerance resistors. The figures show low and high resistance ranges.

Termination Current

When the battery voltage reaches V_{CV}, the SC908 transitions from constant current mode to constant voltage mode. As the output holds the voltage measured at the BSEN pin constant, the current through the battery will decrease as the battery becomes fully charged. CHRGB is disabled when the output current drops below the programmed termination current. If the timer is enabled, the output will continue to float-charge in CV mode until the charge timer expires. If the timer is disabled, the output will turn off as soon as the termination current level is reached. The termination current is determined by

$$I_{TERM} = I_{PreQ} = \frac{V_{ITERM\_Typ}}{R_{ITERM}} \times 130$$

Termination current can be programmed from 14mA to 65mA, and must be less than I_{FQ} for correct operation of the charge cycle. Pre-charge and termination current regulation accuracy is dominated by offset error. The range of expected pre-charge output current and termination threshold current versus programming resistance R_{ITERM} is shown in Figures 2a and 2b. The figures show the nominal pre-charge and termination current versus nominal resistance as the center plot. Two theoretical limit plots indicate maximum and minimum current versus nominal programming resistance. These plots are derived from models of the expected worst-case contribution of error sources depending on programmed current. The current range includes the uncertainty due to 1% tolerance resistors. The dots on each plot indicate the currents obtained with standard value 1% tolerance resistors. The figures show low and high resistance ranges.

A sufficient separation between I_{FQ} and I_{TERM} must be maintained to ensure proper operation of the constant current regulator and charge termination detector. R_{IPRGM} and R_{ITERM} must be chosen to nominally satisfy

$$I_{FQ} > I_{TERM} + 90mA$$

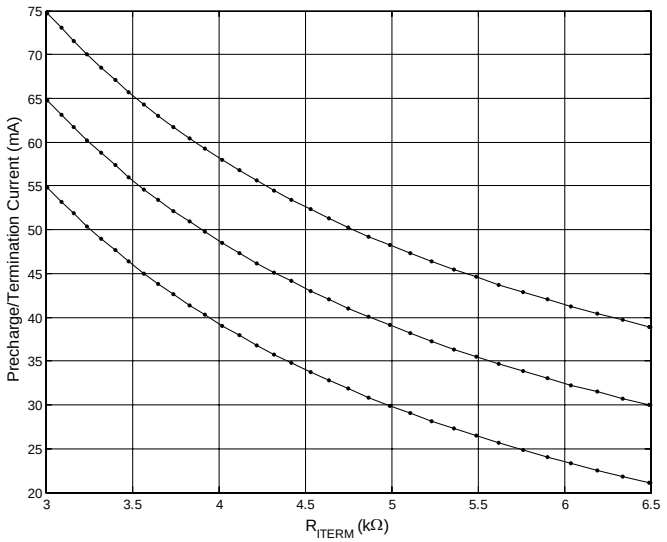


Figure 2a — Pre-charge and Termination Current Variation vs. ITERM Resistance, Low Resistance Range

Applications Information (continued)

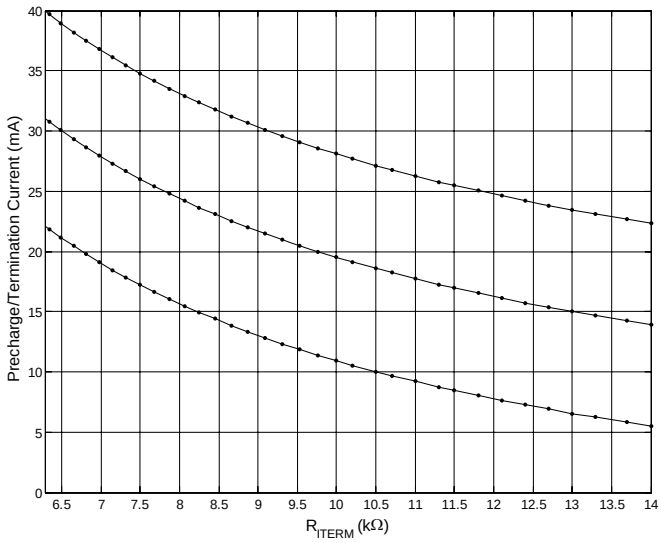


Figure 2b — Pre-charge and Termination Current Variation vs. ITERM Resistance, High Resistance Range

Charge Timer

The timer provides over-charging protection in the event of a faulty battery and maximizes charging capacity. The RTIME pin is connected to VSYS to select the internal (default) time duration of three hours, and to GND to disable the timer. Connecting a resistor between RTIME and GND will program the Charge Complete Time-Out, in hours, according to the equation

$$t_{QComp} = \frac{R_{RTIME}}{3.334} \times \frac{1}{3600}$$

The timer is programmable over the range of 2 to 6 hours. The output is automatically turned off when the charge timer cycle ends.

If the charge cycle remains in precharge for longer than one fourth of the Charge Complete Time-Out period, a charging fault is detected and the charger turns off. The Precharge Fault Time-Out period, in minutes, is

$$t_{PreQF} = \frac{t_{QComp}}{4} \times 60$$

Monitor Mode

When a charge cycle is complete (termination if the timer is disabled, charge timeout if the timer is enabled), the output turns off and the device enters monitor mode. If the battery voltage falls below the recharge threshold ($V_{CV} - V_{ReQ}$), the charger will clear the charge timer and initiate a charge cycle. The status of the charger output as a function of the Charge Complete timer status and I_{BAT} is shown in Table 1.

Table 1 — Charger Output Status

Timer	Iout	Output State
t < Timeout	N/A	On
t > Timeout	N/A	Off
Disabled	$< I_{termination}$	Off

Remote Kelvin Sensing at the Battery

The BSEN pin provides for Kelvin sensing of the battery positive terminal voltage. This prevents feedback error due to charging, battery load, and switching regulator input currents flowing over resistive PCB traces.

Optimal PCB layout routes the BSEN trace directly to the battery positive terminal connection on the PCB to achieve the most accurate sensing of battery cell voltage. Connecting BSEN to BAT directly at the SC908 will introduce battery voltage measurement error that can cause an improper transition from CC to CV regulation, lengthening the charge time. This error could also raise or lower the final battery voltage, and may alter the final state-of-charge.

EN_NTC Interface

The EN_NTC pin is the interface to a battery pack temperature sensing Negative Temperature Coefficient (NTC) thermistor, which can be used to suspend charging if the battery pack temperature is outside of a safe-to-charge range. It is also the charger-disable input. The typical EN_NTC network is a fixed resistor from VSYS to the EN_NTC pin, and the battery pack EN_NTC thermistor from the EN_NTC pin to ground. In this configuration, an increasing battery temperature produces a decreasing NTC pin voltage.

When V_{EN_NTC} is greater than the high (cold) threshold or less than the low (hot) threshold, the charge cycle is suspended by turning off the output. This suspends but does not reset the charge timer, and indicates a fault on the FLTB pin. Hysteresis is included for both high and low

Applications Information (continued)

NTC thresholds to avoid chatter at the NTC fault thresholds. When V_{EN_NTC} returns to the valid range, the charge timer resumes and the charge cycle continues. The charge timer will expire when the output on-time exceeds the timer setting, regardless of how long it has been disabled due to an NTC fault.

Using the recommended NTC external network, the EN_NTC pin voltage and the internal hot and cold NTC thresholds are all ratios of V_{VSYS}, rather than absolute voltages. This ensures that the hot and cold OK-to-charge thresholds are insensitive to the VSYS pin output voltage. The ratiometric thresholds are given by the parameters RT_{NTCH} and RT_{NTCC}. EN_NTC pin voltage V_{EN_NTC} between $RT_{NTCH} \times V_{VSYS}$ and $RT_{NTCC} \times V_{VSYS}$ enables charging. When V_{EN_NTC} is outside this range, charging is suspended and the FLTB output is asserted (pulled low).

When $V_{EN\_NTC} < VT_{NTCDIS}$ (nominally 0.6V), the SC908 charger is disabled. The EN_NTC pin can be pulled to ground by an external n-channel FET or microprocessor GPIO to asnychronously disable or reset the device. When $V_{EN\_NTC} < VT_{NTC\_DIS}$, the charger is turned off, the charge timer is reset, and the CHRGB status output is turned off. While disabled, the VAD input UVLO and OVP threshold detectors remain active, and the CPB pin continues to indicate whether the VAD input voltage is valid for charging.

The response of the SC908 to an EN_NTC pin voltage above the high threshold or below the low threshold (but above VT_{NTCDIS}) is the same. Therefore the EN_NTC network can be configured with the battery pack thermistor between EN_NTC and VSYS, and a fixed resistor between EN_NTC and ground. This configuration may be used to reset the charge timer (and the CHRGB output) when the battery pack is removed; the fixed resistor pulls the NTC pin to ground to disable the charger without indicating a fault.

NTC Design Example

This example uses the conventional NTC network configuration shown in the block diagram. A fixed resistor (R_{NPU}) is connected between EN_NTC and VSYS, and a battery NTC thermistor (R_{NTC}) is connected between the EN_NTC pin and ground. The battery temperature range over which charging is permitted is from 0°C to 40°C. The datasheet for the proposed NTC thermistor, the Mitsubishi TH11-3T223F, indicates that R_{NTC} = 11.93kΩ at 40°C, and R_{NTC} = 69.41kΩ at 0°C, with a dissipation constant DC = 3.0mW/°C. So R_{HOT} = 11.93kΩ and R_{COLD} = 69.41kΩ.

Step 1

Select R_{NPU} to obtain one of the desired temperature thresholds. This example will solve for the hot threshold for the normal (NTC thermistor to ground) configuration, then evaluate the cold threshold. Solve the NTC network voltage divider for R_{NPU} to place the NTC voltage at $RT_{NTC\_HF} \times V_{VSYS}$ when $R_{NTC} = R_{HOT}$.

$$RT_{NTC\_HF} \times V_{VSYS} = \frac{V_{VSYS} \times R_{HOT}}{R_{NPU} + R_{HOT}}$$

or, solving for R_{NPU},

$$R_{NPU} = \frac{1 - RT_{NTC\_HF}}{RT_{NTC\_HF}} \times R_{HOT}$$

Using RT_{NTC_HF} = 0.3, we obtain R_{NPU} = 27.837kΩ exactly. The closest 1% standard nominal value is R_{NPU} = 28.0kΩ.

Step 2

Evaluate the NTC network at the cold threshold. Compute the NTC network resistor divider voltage as a function of V_{VSYS} at the desired cold threshold.

$$NTC_{COLD} = \frac{V_{VSYS} \times R_{COLD}}{R_{NPU} + R_{COLD}} = 0.7126 \times V_{VSYS}$$

The value 0.7126 should be close to the nominal value of RT_{NTC_CR} = 0.75. To evaluate the significance of the discrepancy, an estimate of the actual cold threshold is obtained by evaluating the value of $R_{NTC\_Cold\_Actual}$ that produces the nominal value of RT_{NTC_CR} = 0.75.

$$RT_{NTC\_CR} = \frac{R_{NTC\_Cold\_Actual}}{R_{NTC\_Cold\_Actual} + R_{NPU}}$$

The solution shows $R_{NTC\_Cold\_Actual}$ = 84.0kΩ. Examination of the thermistor specification resistance versus temperature data indicates that the resulting actual cold threshold is approximately -4°C, compared to the target of 0°C.

Applications Information (continued)

Step 3

With the example thermistor, there is no choice of R_{NPU} that will yield the specified results at both hot and cold limits. A more sensitive thermistor, one with a wider percentage variation in resistance at the desired threshold temperatures, may provide a better solution. Steps 1 and 2 are repeated using other devices from the same vendor, seeking a closer match at the cold threshold.

The Mitsubishi TH11-4C153F was the final selection. Its characteristics are: R_{HOT} is 7.73kΩ (at 40°C), R_{COLD} is 53.94kΩ (at 0°C). Its dissipation constant DC = 3.0mW/°C. Step 1 yields R_{NPU} = 18.2kΩ, with the result that $NTC_{COLD}/V_{VSYS} = 0.748 \approx RT_{NTC\_CR}$, $NTC_{HOT}/V_{VSYS} = 0.298 \approx RT_{NTC\_HF}$. The NTC resistances that give the exact cold and hot thresholds RT_{NTC_CR} and RT_{NTC_HF} are 54.6kΩ (which is R_{NTC} at approximately -0.5°C) and 7.80kΩ respectively, closely matching the resistance of the thermistor at the targeted threshold temperatures.

Step 4

Verify acceptable thermistor self heating. The dissipation constant is the power rating of the thermistor resulting in a 1°C self heating error. Since accuracy is important only at the thresholds, self heating is assessed only at 0°C and 40°C.

For V_{VSYS} = 4.6V, the 0°C NTC network current is

$$I_{NTC\_COLD} = V_{VSYS}/(R_{NPU} + R_{COLD}) = 63.8\mu A$$

Power dissipation in the thermistor at this temperature is

$$P_{COLD} = R_{COLD} \times (I_{NTC\_COLD})^2 = 0.219mW$$

The self heating error is

$$T_{SH\_COLD} = \frac{0.219mW}{3\,^{mW}/_{C}} = 0.073°C$$

The 40°C NTC network current

$$I_{NTC\_HOT} = V_{VSYS}/(R_{NPU} + R_{HOT}) = 0.177mA$$

Power dissipation in the thermistor at this temperature is

$$P_{HOT} = R_{HOT} \times (I_{NTC\_HOT})^2 = 0.243mW$$

for self heating of approximately 0.081°C. The actual cold and hot thresholds will be 0.073 and 0.081 degrees lower than designed, respectively, which are negligible errors.

Logical CC-to-CV Transition

The SC908 differs from most monolithic linear single cell Li-Ion chargers, which implement a linear transition from CC to CV regulation. The linear transition method uses two simultaneous feedback signals — output voltage and output current — to the closed-loop controller. When the output voltage is sufficiently below the CV regulation voltage, the influence of the voltage feedback is negligible and the output current is regulated to the desired current. As the battery voltage approaches the CV regulation voltage (4.2V), the voltage feedback signal begins to influence the control loop, which causes the output current to decrease although the output voltage has not reached 4.2V. The output voltage limit dominates the controller when the battery reaches 4.2V and eventually the controller is entirely in CV regulation. This system may be characterized as a dual-constraint (voltage and current) controller, with a soft transition between constraints. The soft transition effectively reduces the charge current below that which is permitted for a portion of the charge cycle, which increases charge time.

In the SC908, a logical transition is implemented from CC to CV to recover the charge current lost due to the soft transition. The controller regulates only current until the output voltage exceeds the transition threshold voltage. It then asynchronously switches to CV regulation. The transition voltage from CC to CV regulation is typically less than 10mV higher than the CV regulation voltage, which provides a sharp and clean transition free of chatter between regulation modes. The difference between the transition voltage and the regulation voltage is the CC/CV overshoot. While in CV regulation, the output current is limited to approximately 105% of the fast-charge current programmed by the IPRGM pin or the IPUSB pin, depending on the charging input selected, providing mode transition hysteresis. If the output current exceeds this current limit threshold, the controller asynchronously reverts to current regulation.

The logical transition from CC to CV results in the fastest possible charging cycle that is compliant with the speci-

Applications Information (continued)

fied current and voltage limits of the Li-Ion cell. The output current is constant at the CC limit, then decreases abruptly when the output voltage steps from the overshoot voltage to the regulation voltage at the transition to CV control. This can be compared to voltage and current trajectories for other monolithic charger devices to show the softness of the linear crossover. This explains the charge-time advantage of the SC908 logical crossover method.

Charger Protection Features

The protection features are:

- Short Circuit Protection
- Over Current and Max Temperature Protection
- Input Overvoltage Protection
- Thermal Protection

Short Circuit Protection

The BAT output can tolerate an indefinite short circuit to ground. The current into a ground short will be equal to the precharge current.

The ITERM pin voltage prior to termination, and the IPRGM pin voltage while in CC mode, are regulated to 1.5V. Precharge current and termination current are proportional to the resulting ITERM current, and CC current is proportional to the resulting IPRGM current. High battery current is prevented by pinshort detectors on both programming pins. Pinshort detection asynchronously forces the charger into reset, turning off the output and clearing the charge timer. When the pinshort condition is removed, the charger begins normal operation automatically.

Over Current and Max Temperature Protection

Over current protection is provided in all modes of operation. When the device is in the charge mode the output is current-limited to either the programmed pre-charge current or the programmed fast charge current, depending on the voltage at the output. Junction over-temperature protection allows operation with maximum power dissipation by disabling the charger output current when the die temperature reaches the maximum operating temperature. This results in operation as a pulse charger in extreme power dissipation applications, delivering the maximum allowable output current while limiting the internal die temperature to a safe level.

Input Over-Voltage Protection

The VAD input is protected from adapter over-voltage to at least 28V above V_{DGND}. When V_{VAD} exceeds its OVP rising threshold VAD_{OVP-R} the charger turns off its output while the charge timer continues to run, and the FLTB status indicator is asserted. When V_{VAD} subsequently falls below the VAD OVP falling threshold VAD_{OVP-F}, charging continues normally and FLTB is released.

Thermal Protection

The charger's internal over-temperature (OT) threshold is set to approximately 145°C. If the temperature exceeds this threshold prior to termination, the charger output is turned off. All other functions remain active, the charger logical state is preserved, and no fault is indicated. This allows thermal pulse charging in conditions of high power dissipation. Following termination, a charger OT condition will be indicated as a fault. Refer to the Indicator Flags subsection for more information.

A second high OT threshold is set to approximately 165°C. Should the die temperature exceed this threshold, all SC908 functions are disabled, and the status outputs indicate an exceptional condition fault. Refer to the Indicator Flags subsection for more information.

Low Battery Detector Operation

The low battery detector provides two low battery detection voltage thresholds: a fixed warning threshold and a resistor programmable detection (shutdown request) threshold. The low battery detector is enabled when either the buck converter is enabled (SEN is high) or the LDO regulator is enabled (LEN is high). The warning and shutdown request are provided by the status output pins FLTB and LBATB, as described in the Status Outputs subsection. When a charging adapter is present (V_{VAD} > VAD_{UVLO-x}), the FLTB and LBATB outputs are redefined to reflect the interaction of battery voltage and charging state.

The low battery detector warning threshold is fixed at 3.28V ± 70mV. The battery voltage fault threshold is programmable, with a resistor from the RLBAT pin to ground,

Applications Information (continued)

from 2.77V to 2.98V, ±10%. The low battery fault threshold is set by the relationship

$$V_{DET} = 3.9\ \mu A \times R_{RLBAT} \times 2.42$$

R_{RLBAT} must satisfy the condition

$$294k\Omega \le R_{RLBAT} \le 316k\Omega$$

Connect RLBAT to GND to disable the Low Battery Detector fault. The Low Battery Detector warning remains active.

Status Outputs

Four charger status outputs/LED drivers are provided.

- CPB (Charger Present)
- CHRGB (Charge Active)
- FLTB (Fault)
- LBATB (Low Battery Warning)

These outputs are active-low, open drain NMOS drivers capable of sinking up to 2mA each. The state of each, in various operating conditions, is defined in Tables 2, 3, and 4.

When the VAD voltage is below its UVLO threshold (no charging adapter is present), the CPB and CHRGB outputs are off (high impedance). The FLTB and LBATB outputs indicate the battery voltage as defined in Table 2.

When V_{VAD} is between its UVLO and OVP thresholds, V_{VAD} is valid to charge, and the CPB output is low indicating that a charging adapter is present.

The CHRGB output indicates the battery charging status. The charger-present status output states are described in Table 3. When pre-charging or when the output current is greater than I_{TERM}, CHRGB is low. The CHRGB output is latched off (high) when the output current becomes less than I_{TERM} during the charge cycle (and the battery voltage is above the recharge threshold, $V_{BSEN} > V_{CV} - VT_{ReQ}$). This latch is reset when the battery enters a recharge cycle ($V_{BSEN} < V_{CV} - VT_{ReQ}$), or for any NTC_EN range other than OK-to-charge, or if V_{VAD} is above or below the VAD valid-to-charge range, allowing CHRGB to become active again when charging resumes.

When a charging adapter is present, the FLTB and LBATB outputs are redefined to reflect the interaction of the battery voltage, charging state, and charging faults, as described in Table 3. The FLTB output is activated when the device experiences a charger fault condition, or (together with LBATB output) when the battery voltage is less than the resistor-programmed low-battery detector threshold, V_{DET}. This output can be used to notify the system controller of a fault condition when connected to an interrupt input, or it can be used like CPB and CHRGB to drive an indicator LED.

Table 2 — Status Output State, Charging Adapter Absent

Status Pins Output State (on = low)				Conditions						Description and Comments
				Adapter Voltage (mutually exclusive)			Battery Voltage (mutually exclusive)			
CPB	CHRGB	FLTB	LBATB	$V_{VAD} < VAD_{UVLO}$	$VAD_{UVLO} < V_{VAD} < VAD_{OVP}$	$V_{VAD} > VAD_{OVP}$	$V_{BSEN} \ge V_{WARN}$	$V_{WARN} > V_{BSEN} > V_{DET}$	$V_{DET} \ge V_{BSEN}$	on = open drain output driver is active off = output is not active T = listed condition is true F = listed condition is false - = don't care Blank = mutually exclusive with another condition
off	off	off	off	T			T			No Charging Adapter, Battery Voltage Good
off	off	off	on	T				T		No Charging Adapter, Low Battery Voltage Warning
off	off	on	on	T					T	No Charging Adapter, Low Battery Shutdown Request

Applications Information (continued)

The fault modes signaled by FLTB are:

- input over-voltage
- battery NTC temperature out of range
- pre-charge timeout.
- charger-only over-temperature (low OT, post-termination only)

When any of these conditions occurs the FLTB output goes low; otherwise it remains high impedance.

The LBATB output is active when the battery voltage is below the low-battery warning voltage, V_{WARN}, if the charging adapter is absent. If CPB and CHRGB outputs are both active, LBATB indicates when the charger is in precharge mode. However, LBATB and FLTB active together always

Table 3 — Status Output State, Charging Adapter Present

Status Pins Output State (on = low)				Conditions														Description and Comments
				Adapter Voltage (mutually exclusive)			Battery Voltage (mutually exclusive)			EN_NTC (mutually exclusive)			Charging State, Charging Faults (Internal signals)					
CPB	CHRGB	FLTB	LBATB	$V_{VAD} < VAD_{UVLO}$	$VAD_{UVLO} < V_{VAD} < VAD_{OVP}$	$V_{VAD} > VAD_{OVP}$	$V_{BSEN} \geq V_{WARN}$	$V_{WARN} > V_{BSEN} > V_{DET}$	$V_{DET} \geq V_{BSEN}$	Disable	NTC OK	NTC Hot or Cold	Charger OT	BAT Short-to-GND	Pre-Charging	Pre-Term Charging	Pre-Charge Timeout	on = open drain output driver is active off = output is not active T = listed condition is true F = listed condition is false - = don't care Blank = mutually exclusive with another condition
on	off	off	off		T		T			T			-	-	-	-	F	V_{VAD} valid, Charger Disable/Reset OR Charging Done (Die Temperature OK)
										F	-	-	F	F	F	F		
on	off	off	on		T			T		T			-	-	-	-	F	V_{VAD} valid and Low Battery Warning, Charger Disable/Reset OR Charge Cycle Pending (about to begin)
											T							
on	off	on	off		T		-	-	F			T	-	F	-	-	F	V_{VAD} valid, Battery Temperature Fault OR Charger Over-Temp Fault (Die Temp > T_{CHRGR_OT})
											T		T					
on	off	on	on		T				T	T			-	-	-	-	F	V_{VAD} valid, Low Battery Detected, with either Charger Disable/Reset OR Battery Temperature Fault OR Charger Over-Temp Fault OR BAT short-to-ground
												T	-	-	-	-		
											T		T	-	F	F		
										F	-	-	-	T	-	-		
on	on	off	off		T		-	-	F		T		-	F	F	T	F	V_{VAD} valid, Pre-termination Charging, Battery Voltage > V_{DET}
on	on	off	on		T		-	-	F		T		F	F	T	T	F	V_{VAD} valid, Pre-Charging (trickle charging), Battery Voltage > V_{DET}
on	on	on	off		T		-	-	F		T		T	F	T	T	F	V_{VAD} valid, Pre-Charging with Charger Over-Temp Fault, Battery Voltage > V_{DET}
on	on	on	on		T				T		T		-	F	-	T	F	V_{VAD} valid, Battery Voltage < V_{DET} Pre-Charging or Pre-Termination Charging

Applications Information (continued)

indicates that the battery voltage is below the low-battery detect threshold, V_{DET}. Table 3 gives a comprehensive description of all combinations of status output states while the adapter input is valid for charging.

Exceptions to these charging conditions occur when certain events happen in combination. Table 4 describes status condition exceptions. These exceptions include V_{VAD} > OVP threshold; a high over temperature condition, in which device temperature exceeds the higher of two over-temperature thresholds, causing charging and both regulators to be disabled; a precharge timeout, which may indicate a faulty battery.

VSYS pin

The voltage of the VSYS pin is regulated from the VAD input and is present only when VAD is powered. VSYS provides an external voltage reference and supply for the NTC network, and a pull-up supply voltage for the CPB status indicator. A capacitor of at least 0.1uF should be connected from VSYS to ground near the pin.

The load on VSYS should not exceed 5mA. If CHRGB is used to operate an indicator LED, it is recommended that the CHRGB status pin be pulled up to the battery or to a battery-powered regulated supply. Since CHRGB is asserted only while charging the battery, the current sunk by CHRGB will be sourced by the charger output and will not discharge the battery.

Because VSYS is powered from VAD, it is unsuitable as a pullup source for the FLTB and LBATB status pins. These status pins must be powered from the battery or battery-powered regulated supply to function as battery level indicators when the charging adapter is not present.

Capacitor Selection

Low cost, low ESR ceramic capacitors such as the X5R and X7R dielectric material types are recommended. The BAT pin capacitor, C_{BAT}, range is 1µF to 22µF. This capacitor functions as both the charger output capacitor and as the switching regulator input capacitor. The VAD pin input capacitor C_{VAD} is typically between 0.1µF to 2.2µF; however, larger values will not degrade performance.

Table 4 — Status Output State, Exception Conditions

Status Pins Output State (on = low)				Conditions														Description and Comments
				Adapter Voltage (mutually exclusive)			Battery Voltage (mutually exclusive)			EN_NTC (mutually exclusive)			Charging State, Charging Faults (Internal signals)					
CPB	CHRGB	FLTB	LBATB	$V_{VAD} < VAD_{UVLO}$	$VAD_{UVLO} < V_{VAD} < VAD_{OVP}$	$V_{VAD} > VAD_{OVP}$	$V_{BSEN} \geq V_{WARN}$	$V_{WARN} > V_{BSEN} > V_{DET}$	$V_{DET} \geq V_{BSEN}$	Disable	NTC OK	NTC Hot or Cold	Charger OT, (High OT)	BAT Short-to-GND	Pre-Charging	Pre-Term Charging	Pre-Charge Timeout	on = open drain output driver is active off = output is not active T = listed condition is true F = listed condition is false - = don't care Blank = mutually exclusive with another condition
off	off	on	off			T	T			-	-	-	-	-	-	-	F	VAD Overvoltage, Battery Voltage Good or Warning
								T										
off	off	on	on			T			T	-	-	-	-	-	-	-	F	VAD Overvoltage, Low Battery Detect
off	on	on	off	-	-	-	-	-	-	-	-	-	Hi OT	-	-	-	-	**High-Over-Temperature Detection** (die temperature > T_{OT}; all functions shutdown.)
off	on	on	on	F	-	-	-	-	-	F	-	-	-	-	-	-	T	Pre-charge Timeout, NTC Not Disable, Adapter Voltage Good or OVP

Applications Information (continued)

LDO Regulator

The low-noise low-dropout (LDO) voltage regulator operates from an LVIN pin input voltage range of 2.2V up to the battery voltage (V_{BAT}), and an output voltage from 1.5V to 3.3V, programmable with external resistors. The SC908 has a VREF bypass pin to enable the user to capacitively decouple the bandgap reference (10nF recommended) for very low output noise (50µV_{RMS} typically).

The output voltage of the LDO regulator is divided externally using a resistor divider and compared to the buffered bandgap voltage, typically 0.75V. The error amplifier drives the gate of a low $R_{DS(ON)}$ P-channel MOSFET pass device.

Enabling the LDO

The LDO has an independent enable input pin (active high). The LDO can be enabled only if $V_{LVIN} \geq VT_{LUVLO}$, typically 2.0V, although performance specifications are guaranteed for $V_{LVIN} \geq 2.2V$. The LDO output will settle to within 5% of its final value in 0.1ms (typically) when the bandgap reference buffer has already settled (when the switching regulator is already enabled, or when the charging adapter is present). A fast start-up circuit is used to speed the initial charging time of the VREF pin bypass capacitor. This is done so that the LDO output voltage will settle to within 5% of its final value in 0.4ms (typically) when the LDO is the first resource enabled. When the battery charger is in its precharge mode of operation (trickle charging of a deeply discharged battery), the LDO enable signal will be disregarded until fast-charging begins (at a battery voltage of 2.8V typically). An exception occurs when either the LDO or switching regulator are already enabled. At this time when a charging source is applied and the charger enters precharge mode, the LDO will remain enabled (or can become enabled). Precharge mode is indicated by the status outputs. (Refer to Table 3.)

The LDO provides active shutdown. The capacitance on LVOUT will be discharged by an on-chip FET when the LDO is disabled.

Programming the LDO Output Voltage

The LDO regulates its output to obtain 0.75V at the LFB pin. The output can be programmed to any voltage from 1.5V to 3.3V by an external resistor divider network from LVOUT to LFB. The output voltage is set by

$$V_{LVOUT} = V_{LFB} \times \left(1 + \frac{R_{L1}}{R_{L2}}\right)$$

LFB is a high impedance input, so large value resistors, even on the order of 500kΩ, may be used to meet the noise specification. When considering the effect of LDO load current on performance specifications, the current flowing in the feedback divider network should be included in the load. The LDO is internally compensated. No feedback capacitor is required for stability.

LDO Dropout

The LDO dropout voltage is the product of the minimum $R_{DS(ON)}$ of the P-channel MOSFET pass device and the LDO output current. As V_{LVIN} decreases, the achievable source-to-gate voltage of the pass device decreases, so the minimum achievable $R_{DS(ON)}$ becomes larger. This is the reason for the two-tier dropout specification. Minimum $R_{DS(ON)}$ increases with die temperature, which is affected not only by LDO power dissipation, but also by switching regulator and charger power dissipation. The maximum dropout is specified for a temperature of 85°C.

LDO Reference Voltage

The internal bandgap reference voltage must be externally bypassed to meet the LDO noise specification. A 10nF ceramic capacitor from the VREF pin to AGND is recommended to bypass the bandgap reference buffer. Increasing this capacitor to 100nF will improve power supply rejection, but at the cost of slower turn-on settling time. All noise and turn-on settling time specifications assume that the VREF bypass capacitor is 10nF. Low cost, low ESR ceramic capacitors such as the X5R and X7R dielectric material types are recommended.

The bandgap reference is trimmed and buffered to obtain 0.75V typically at the LFB pin with respect to AGND while the LDO is operating. V_{VREF} is the reference voltage for LFB, so V_{VREF} will be equal to V_{LFB} within the offset error of the LDO feedback error amplifier. The bandgap reference and reference buffer are powered from the greater of V_{VSYS} (derived from VAD, when present) and V_{BAT} (the battery voltage). The $PSRR_{REF}$ specification is with respect to V_{BAT}. It is evaluated while the charging adapter is not present.

Applications Information (continued)

VREF power supply rejection with respect to VAD will be similar.

The VREF pin is a high impedance source. Any load on VREF will degrade LDO and switching regulator voltage accuracy. Note that the 10MΩ impedance of a typical oscilloscope probe is not large enough to prevent loading of the VREF pin.

LDO Power Supply Rejection

Power supply rejection must be considered with respect to two inputs. The buffered bandgap reference is powered by the greater of two possible sources, V_{VSYS} (an internal/external supply voltage, derived from VAD when present) and V_{BAT}. The LDO is powered from the LVIN pin. $PSRR_L$ is defined as the power supply rejection from LVIN to LVOUT with the reference and reference buffer powered from BAT as DC voltage. The reference voltage VREF power supply rejection specification ($PSRR_{REF}$) is with respect to BAT. Any reference voltage power supply noise or ripple is seen in the LDO as noise on the LFB reference voltage. This noise is then gained-up to the output by the reciprocal of the LFB divider network, or by the gain ($1 + R_{L1}/R_{L2}$).

In the special case $V_{LVIN} = V_{BAT}$ (the LVIN pin is connected directly to the battery), the power supply rejection of the LDO, $PSRR_{LBAT}$, is determined by

$$PSRR_{LBAT} = -20\log_{10}\left(\left(1+\frac{R_{L1}}{R_{L2}}\right)\times 10^{-PSRR_{REF}/20} + 10^{-PSRR_{L}/20}\right)$$

LDO Current Limit and Short-Circuit Protection

The LDO regulator has current limit circuitry to ensure that the output current will not damage the device during output short-circuit to ground, overload, or start-up. The current limit is guaranteed to be greater than 200mA to allow fast charging of the output capacitor and for high transient load currents.

LDO Input and Output Capacitor

A minimum LDO input and output capacitance of 1µF with a maximum equivalent series resistance (ESR) of less than 1Ω over temperature is recommended. Increasing the output capacitance will further reduce output noise and improve load transient response. A larger input capacitor will reduce input droop due to load transients, improving overall load transient response, and may also improve input supply rejection.

Switching Regulator

The SC908 contains a synchronous step-down Pulse Width Modulated (PWM), DC-DC converter (also referred to as a Buck Converter or Switcher) with integrated power devices. The switching frequency is set nominally to 1MHz, allowing the use of small inductors and capacitors. The current limit of the internal PMOS switch (I_{LIM_P}), allows a DC output current of at least 150mA with appropriate external components. For maximum efficiency over the full load range, the switcher will automatically operate in Power Save (PSAVE) mode with light loads, and in PWM (normal switching) mode for heavier loads.

The voltage feedback loop uses an external feedback divider. An internal synchronous NMOS low side switch is used. An external Schottky diode on the LX pin is not required.

Switcher Programmable Output Voltage

The buck converter regulates its output to obtain 0.5V at the SFB pin. The output can be programmed to any voltage from 1.0V to 3.0V by an external resistor divider network from the external circuit node SVOUT to the SFB pin. The equation for setting the output voltage is

$$V_{SVOUT} = V_{SFB}\times\left(1+\frac{R_{S1}}{R_{S2}}\right)$$

SFB is a high impedance input, therefore the magnitude of resistances used will be determined by a trade off between feedback network current and product design practice. A 25pF feedback capacitor, designated C_{SFB}, is required for stability in PWM mode.

When considering the effect of buck converter load current on performance specifications, the current flowing in the feedback divider network should be included in the load. In most situations, PSAVE mode operation will require a capacitor from SFB to AGND. Refer to the PSAVE mode description.

Switcher Power Save (PSAVE) Mode Operation

The PSAVE mode is automatically activated or deactivated with light to heavy loads, maximizing efficiency across the

Applications Information (continued)

full load range. The SC908 automatically detects the load current at which it should enter PSAVE mode. This detection is based on the minimum peak current in the PMOS high side switch in PWM mode. This will vary with input voltage, output voltage, and the converter external inductance (L_S). PSAVE entry DC load current will decrease with decreasing L_S.

In a PSAVE mode burst cycle, V_{SVOUT} rises from a lower to an upper voltage threshold with a switching burst (see Figure 3). Within the burst, the PMOS switch is turned on until the PMOS current reaches a current limit. It is then turned off for a fixed duration, and then turned on again (cycle may be repeated). The low-side NMOS switch is turned on whenever the high-side switch is off. When the upper threshold (1.5% above the programmed regulation voltage) is reached, the switching burst is halted. This reduces the quiescent current by turning off both high-side and low-side switches. V_{SVOUT} decays to the lower threshold (0.8% above the programmed regulation voltage) due to the load current discharging the output capacitor, which initiates another switching burst. The burst-time to off-time ratio in PSAVE will decrease with decreasing load current.

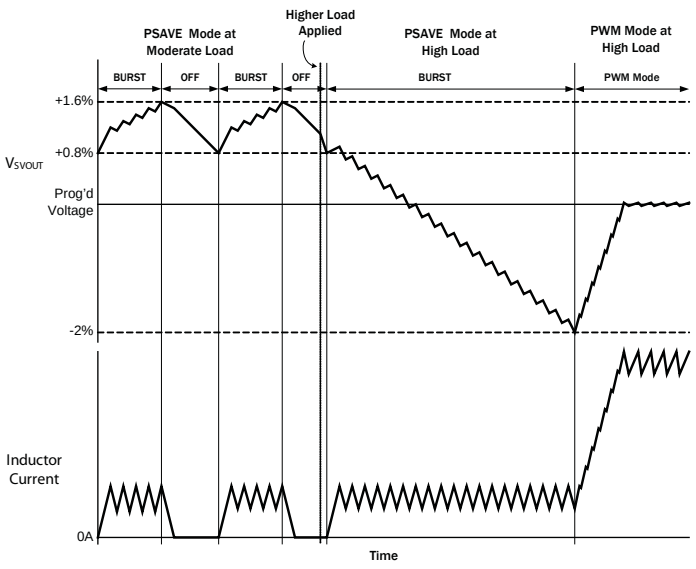


Figure 3 Power Save Operation

The PSAVE switching burst is designed so that the inductor current ripple is similar to that of PWM mode. To prevent audible noise, the PSAVE mode parameters have been chosen such that the minimum PSAVE burst envelope frequency will exceed 20kHz for any load greater than 3mA, if external component recommendations have been followed. The envelope minimum frequency will decrease with increasing C_{SVOUT} capacitance.

The SC908 automatically detects when to exit PSAVE mode by monitoring V_{SFB}, and thus V_{SVOUT}. If the switching burst output current is insufficient to supply the output load, V_{SVOUT} will not rise to the upper threshold during a switching burst, but will instead decrease. If V_{SVOUT} droops to 2% below the programmed regulation voltage, PSAVE mode will be deactivated, and the buck converter will revert immediately to PWM mode. To prevent rapid PWM/PSAVE mode cycling, the PSAVE entry and exit criteria are chosen to provide load hysteresis. After reverting to PWM mode the switcher will remain in PWM mode for 128 switching cycles (approximately 128µs) before it is permitted to re-enter PSAVE mode.

Proper operation of PSAVE mode requires the addition of a capacitor from the SFB pin to ground, designated C_{SFG}, of value

$$C_{SFG} = C_{SFB} \times R_{S1} / R_{S2}.$$

Switcher Efficiency

Switcher efficiency is affected by input voltage, output voltage, temperature, and choice of inductor. It also varies with load, and on which mode, PWM or PSAVE, is active. The mode selection depends not only on the instantaneous load, but also on the immediate past load, since transitions between PSAVE and PWM modes are load dependent, with hysteresis.

For high loads (those that unconditionally place the switcher in PWM mode), the efficiency typically exceeds 90%. For low loads (those that unconditionally place the switcher in PSAVE mode), efficiency can vary from 88 to 92% over all conditions. As the load decreases further, the SC908 quiescent current eventually becomes significant, and efficiency drops off sharply.

At intermediate modes, the switcher could select either PSAVE or PWM mode depending on whether the recent past load was higher or lower, due to load hysteresis. Within the hysteresis load range, efficiency can vary from 86% to 92%, over all conditions.

Applications Information (continued)

Switcher Protection Features

The protection features are:

- Current limit
- Over-voltage protection
- Soft-start

Current Limit

The PMOS power device in the buck switcher stage is protected by a current limit function. If a short to ground on the output occurs, the part enters frequency foldback mode, which causes the switching frequency to divide by a factor determined by the output voltage. This prevents the inductor current from stair-casing.

Over-Voltage Protection

In the event of over-voltage on the output in PWM mode, the PWM drive is disabled. When disabled, the SLX output becomes high impedance (both high-side and low-side switches are turned off). The switcher will not resume switching until the output voltage has fallen to 2% below the programmed regulation voltage.

Soft-Start

The soft-start mode is enabled after every shutdown cycle to limit in-rush current. This controls the maximum current during start-up. The PMOS current limit is stepped up using three soft-start levels to the full value by a timer driven from the internal oscillator. During soft-start, the switching frequency is stepped by 1/8, 1/4, and 1/2 of the internal oscillator frequency up to the full value, under control of three output voltage thresholds. When the output voltage rises to 98% of the regulation voltage, soft-start mode is disabled.

Switcher External Components

The SC908 is designed for use with the inductor $L_S = 4.7\mu H$, although other values can be used. The magnitude of the inductor current ripple is dependent on the inductor value and can be determined by the equation

$$\Delta I_{L_S} = \frac{V_{SVOUT}}{L_S \times f_{osc}} \left(1 - \frac{V_{SVOUT}}{V_{VOUT}}\right)$$

This equation demonstrates the relationship between input voltage, output voltage, and inductor ripple current.

The inductor should have a low DCR to minimize the conduction losses and maximize efficiency. As a minimum requirement, the DC current rating of the inductor should be equal to the maximum load current plus half of the inductor current ripple as shown by the equation

$$I_{L_S(Peak)} = I_{OUT(MAX)} + \frac{\Delta I_{L_S}}{2}$$

Final inductor selection will depend on various design considerations such as efficiency, EMI, PSAVE entry, size and cost.

C_{BAT} Selection

C_{BAT} functions as both the charger output capacitor and as the switching regulator input capacitor. The source input current to a buck converter is non-continuous. To prevent large input voltage ripple a low ESR ceramic capacitor is required. A minimum value of 10µF should be used for sufficient input voltage filtering and a 22µF should be used for improved input voltage filtering.

C_{SVOUT} Selection

The internal compensation is designed to operate with a minimum output capacitor value of 10µF. Larger output capacitor values will improve transient performance.

Output voltage ripple is a combination of the voltage ripple from the inductor current charging and discharging the output capacitor and the voltage created from the inductor current ripple through the output capacitor ESR. Selecting an output capacitor with a low ESR will reduce the output voltage ripple component, as can be seen in the equation

$$\Delta V_{SVOUT(ESR)} = \Delta I_{L_S(ripple)} \times ESR_{C_{SVOUT}}$$

Capacitors with X7R or X5R ceramic dielectric are recommended for their low ESR and superior temperature and voltage characteristics. Y5V capacitors should not be used as their temperature coefficients make them unsuitable for this application.

When selecting an output capacitor, it is essential that C_{SVOUT} capacitance be evaluated at the V_{SVOUT} programmed voltage. The specified capacitance of 0402, and even 0603, package size devices is often severely derated at just

Applications Information (continued)

a few volts of bias. This is especially true of inexpensive dielectrics. Insufficient SVOUT capacitance can cause rapid decay of output voltage between PSAVE bursts, resulting in poor low-load efficiency, PSAVE/PWM mode cycling, and other erratic behaviors.

Switcher Grounding and PCB Layout Considerations

Poor layout can degrade the performance of the DC-DC converter and can contribute to EMI problems, ground bounce and resistive voltage losses. Poor regulation and instability can result.

A few simple design rules can be implemented to ensure good layout:

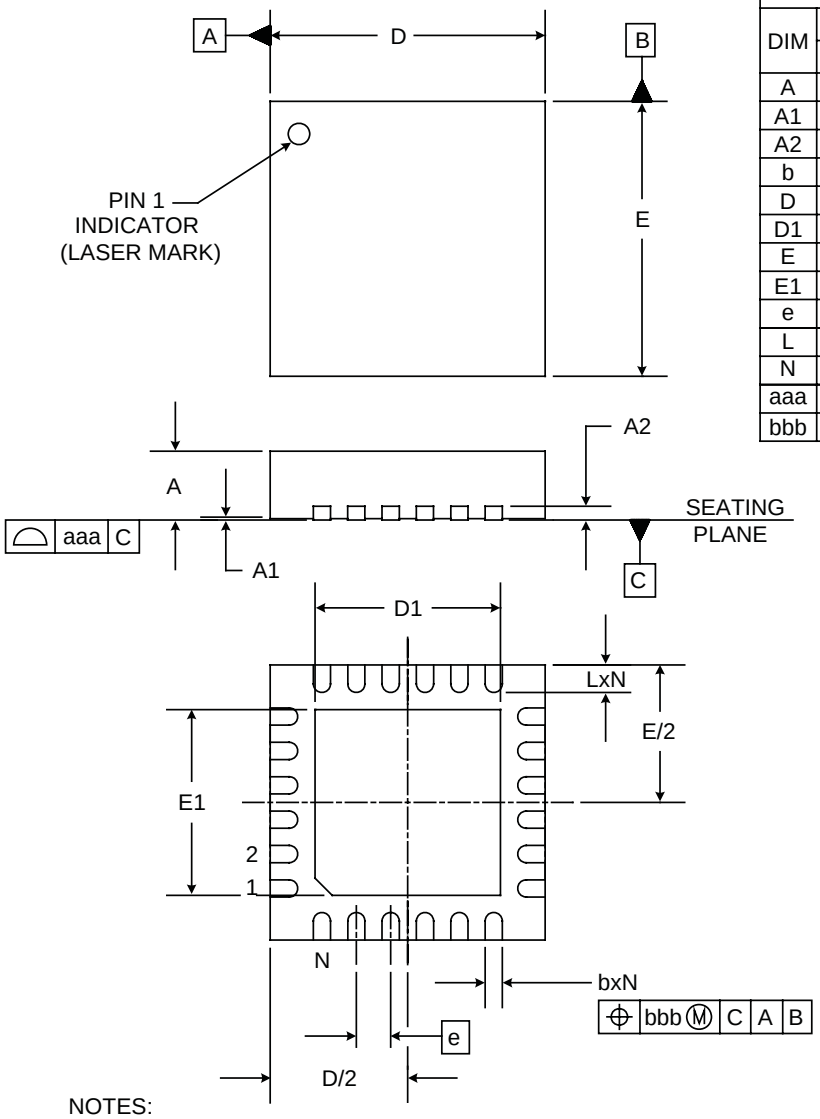
- Place the inductor and filter capacitors as close to the device as possible and use short wide traces between the power components.
- Route the output voltage feedback path away from the inductor and LX node to minimize noise and magnetic interference.
- Maximize ground metal on the component side to improve the return connection and thermal dissipation. Separation between the SLX node and GND should be maintained to avoid coupling of switching noise to the ground plane.
- Use a ground plane with several vias connecting to the component side ground to further reduce noise interference on sensitive circuit nodes.

Charger Grounding and PCB Layout Considerations

While layout for linear devices is generally not as critical as for a switching application, careful attention to detail will ensure reliable operation.

- Attaching the part to a larger copper footprint will enable better heat transfer from the device, especially on PCBs with internal ground and power planes.
- Place the input, output and bypass capacitors close to the device for optimal transient response and device behavior.
- Connect all ground connections directly to the ground plane. If there is no ground plane, connect to a common local ground point before connecting to board ground.
- The DGND pin and PGND pin should be connected directly to the PCB ground plane as close to the part as possible. The thermal pad should be connected to the ground plane with thermal vias under the SC908.
- The nodes indicated as AGND in the Block Diagram should be connected together and to the AGND pin. The AGND pin should be tied to the DGND pin at a single point close to the SC908.
- Route the BSEN trace directly to the battery positive terminal connection on the PCB.

Outline Drawing — MLPQ-24 4x4

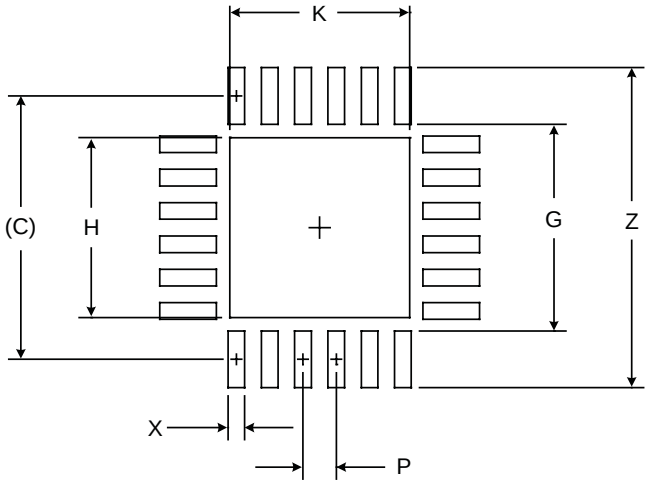


DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	.035	.039	0.80	0.90	1.00
A1	.000	.001	.002	0.00	0.02	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.007	.010	.012	0.18	0.25	0.30
D	.152	.157	.163	3.85	4.00	4.15
D1	.100	.106	.110	2.55	2.70	2.80
E	.152	.157	.163	3.85	4.00	4.15
E1	.100	.106	.110	2.55	2.70	2.80
e	.020 BSC			0.50 BSC		
L	.012	.016	.020	0.30	0.40	0.50
N	24			24		
aaa	.004			0.10		
bbb	.004			0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Land Pattern — MLPQ-24 4x4



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.156)	(3.95)
G	.122	3.10
H	.106	2.70
K	.106	2.70
P	.020	0.50
X	.010	0.25
Y	.033	0.85
Z	.189	4.80

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

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