HD74ALVCH162721

3.3-V 20-bit Flip Flops with 3-state Outputs

REJ03D0044-0400Z
(Previous ADE-205-184B (Z))
Rev.4.00
Oct.02.2003

Description

The HD74ALVCH162721's twenty flip flops are edge triggered D-type flip flops with qualified clock storage. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs, provided that the clock enable ($\overline{\text{CLKEN}}$) input is low. If $\overline{\text{CLKEN}}$ is high, no data is stored. A buffered output enable ($\overline{\text{OE}}$) input can be used to place the twenty outputs in either a normal logic state (high or low level) or a high impedance state. In the high impedance state, the outputs neither load nor drive the bus lines significantly. The high impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components. The output enable ($\overline{\text{OE}}$) input does not affect the internal operation of the flip flops. Old data can be retained or new data can be entered while the outputs are in the high impedance state. Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level. All outputs, which are designed to sink up to 12 mA, include 26 Ω resistors to reduce overshoot and undershoot.

Features

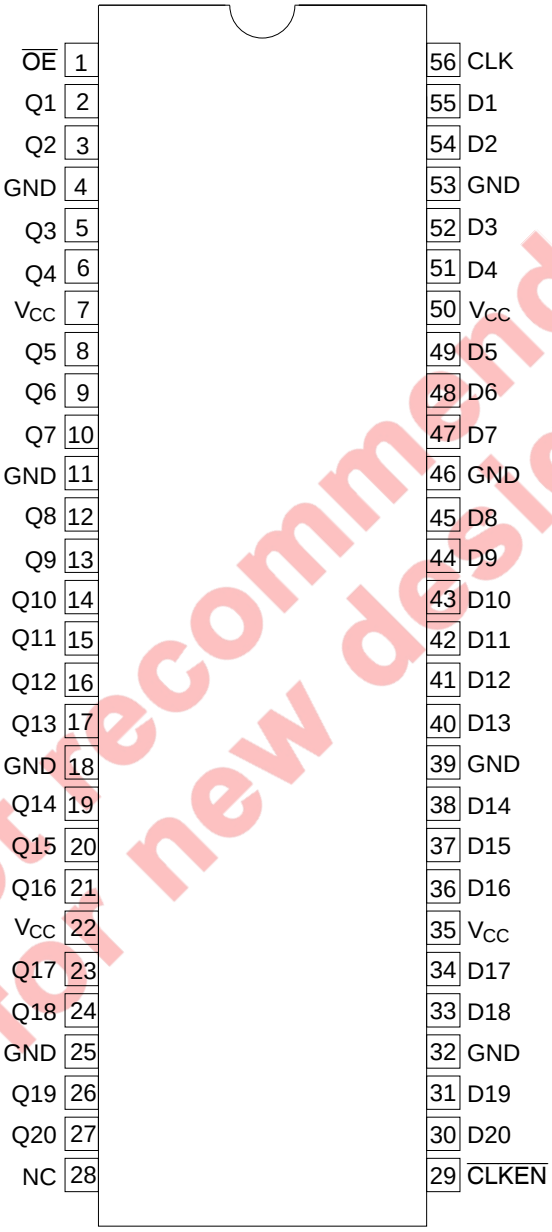
- V_{CC} = 2.3 V to 3.6 V
- Typical V_{OL} ground bounce < 0.8 V (@V_{CC} = 3.3 V, Ta = 25°C)
- Typical V_{OH} undershoot > 2.0 V (@V_{CC} = 3.3 V, Ta = 25°C)
- High output current ±12 mA (@V_{CC} = 3.0 V)
- Bus hold on data inputs eliminates the need for external pullup / pulldown resistors
- All outputs have equivalent 26 Ω series resistors, so no external resistors are required.

Function Table

Inputs				Output Q
$\overline{OE}$	$\overline{CLKEN}$	CLK	D	
L	H	X	X	Q_0 *1
L	L	↑	H	H
L	L	↑	L	L
L	L	L or H	X	Q_0 *1
H	X	X	X	Z

H : High level
L : Low level
X : Immaterial
Z : High impedance
↑ : Low to high transition
Note: 1. Output level before the indicated steady state input conditions were established.

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	–0.5 to 4.6	V	
Input voltage [*1]	V_I	–0.5 to 4.6	V	
Output voltage [*1, 2]	V_O	–0.5 to V_{CC} +0.5	V	
Input clamp current	I_{IK}	–50	mA	$V_I < 0$
Output clamp current	I_{OK}	±50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	±50	mA	V_O = 0 to V_{CC}
V_{CC}, GND current / pin	I_{CC} or I_{GND}	±100	mA	
Maximum power dissipation at Ta = 55°C (in still air) [*3]	P_T	1	W	TSSOP
Storage temperature	Tstg	–65 to 150	°C	

Notes: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

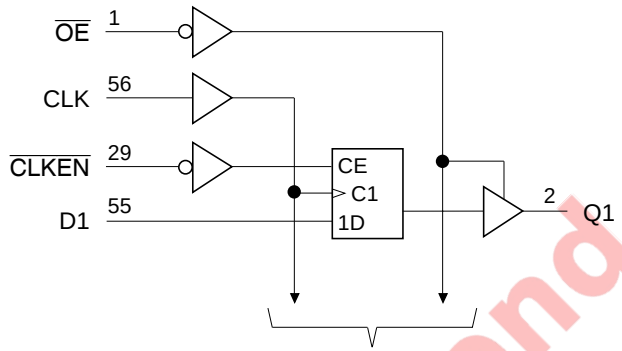
1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{CC}	2.3	3.6	V	
Input voltage	V_I	0	V_{CC}	V	
Output voltage	V_O	0	V_{CC}	V	
High level output current	I_{OH}	—	–6	mA	V_{CC} = 2.3 V
		—	–8		V_{CC} = 2.7 V
		—	–12		V_{CC} = 3.0 V
Low level output current	I_{OL}	—	6	mA	V_{CC} = 2.3 V
		—	8		V_{CC} = 2.7 V
		—	12		V_{CC} = 3.0 V
Input transition rise or fall rate	$\Delta t / \Delta v$	0	10	ns / V	
Operating temperature	Ta	–40	85	°C	

Note: Unused control inputs must be held high or low to prevent them from floating.

Logic Diagram



Electrical Characteristics

(Ta = –40 to 85°C)

Item	Symbol	V_{CC} (V) [*1]	Min	Max	Unit	Test Conditions
Input voltage	V_{IH}	2.3 to 2.7	1.7	—	V	
		2.7 to 3.6	2.0	—		
	V_{IL}	2.3 to 2.7	—	0.7		
		2.7 to 3.6	—	0.8		
Output voltage	V_{OH}	Min to Max	V_{CC}–0.2	—	V	I_{OH} = –100 µA
		2.3	1.9	—		I_{OH} = –4 mA, V_{IH} = 1.7 V
		2.3	1.7	—		I_{OH} = –6 mA, V_{IH} = 1.7 V
		3.0	2.4	—		I_{OH} = –6 mA, V_{IH} = 2.0 V
		2.7	2.0	—		I_{OH} = –8 mA, V_{IH} = 2.0 V
		3.0	2.0	—		I_{OH} = –12 mA, V_{IH} = 2.0 V
	V_{OL}	Min to Max	—	0.2		I_{OL} = 100 µA
		2.3	—	0.4		I_{OL} = 4 mA, V_{IL} = 0.7 V
		2.3	—	0.55		I_{OL} = 6 mA, V_{IL} = 0.7 V
		3.0	—	0.55		I_{OL} = 6 mA, V_{IL} = 0.8 V
		2.7	—	0.6		I_{OL} = 8 mA, V_{IL} = 0.8 V
		3.0	—	0.8		I_{OL} = 12 mA, V_{IL} = 0.8 V
Input current	I_{IN}	3.6	—	±5	µA	V_{IN} = V_{CC} or GND
	$I_{IN\ (hold)}$	2.3	45	—		V_{IN} = 0.7 V
		2.3	–45	—		V_{IN} = 1.7 V
		3.0	75	—		V_{IN} = 0.8 V
		3.0	–75	—		V_{IN} = 2.0 V
		3.6	—	±500		V_{IN} = 0 to 3.6 V
Off state output current [*2]	I_{OZ}	3.6	—	±10	µA	V_{OUT} = V_{CC} or GND
Quiescent supply current	I_{CC}	3.6	—	40	µA	V_{IN} = V_{CC} or GND
	ΔI_{CC}	3.0 to 3.6	—	750	µA	V_{IN} = one input at (V_{CC}–0.6) V, other inputs at V_{CC} or GND

Notes: 1. For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

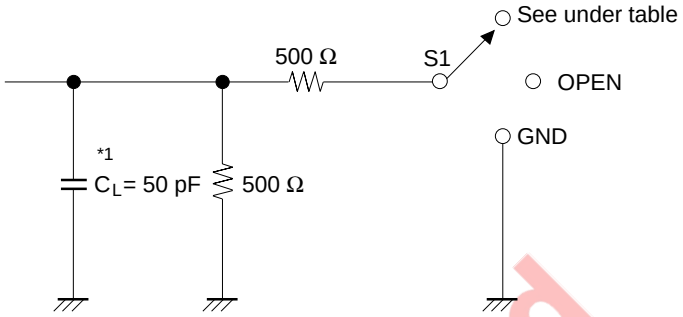
2. For I/O ports, the parameter I_{OZ} includes the input leakage current.

Switching Characteristics

(Ta = –40 to 85°C)

Item	Symbol	V_{CC} (V)	Min	Typ	Max	Unit	FROM (Input)	TO (Output)
Maximum clock frequency	f_{max}	2.5±0.2	150	—	—	MHz		
		2.7	150	—	—			
		3.3±0.3	150	—	—			
Propagation delay time	t_{PLH}	2.5±0.2	1.0	—	6.7	ns	CLK	Q
	t_{PHL}	2.7	1.0	—	6.2			
		3.3±0.3	1.0	—	5.3			
Output enable time	t_{ZH}	2.5±0.2	1.0	—	7.2	ns	$\overline{OE}$	Q
	t_{ZL}	2.7	1.0	—	7.0			
		3.3±0.3	1.0	—	5.8			
Output disable time	t_{HZ}	2.5±0.2	1.0	—	6.3	ns	$\overline{OE}$	Q
	t_{LZ}	2.7	1.0	—	5.4			
		3.3±0.3	1.0	—	5.0			
Setup time	t_{su}	2.5±0.2	4.0	—	—	ns	Data before CLK↑	
		2.7	3.6	—	—			
		3.3±0.3	3.1	—	—			
		2.5±0.2	3.4	—	—		$\overline{CLKEN}$ before CLK↑	
		2.7	3.1	—	—			
		3.3±0.3	2.7	—	—			
Hold time	t_h	2.5±0.2	0	—	—	ns	Data after CLK↑	
		2.7	0	—	—			
		3.3±0.3	0	—	—			
		2.5±0.2	0	—	—		$\overline{CLKEN}$ after CLK↑	
		2.7	0	—	—			
		3.3±0.3	0	—	—			
Pulse width	t_w	2.5±0.2	3.3	—	—	ns		
		2.7	3.3	—	—			
		3.3±0.3	3.3	—	—			
Input capacitance	C_{IN}	3.3	—	3.5	—	pF		
Output capacitance	C_O	3.3	—	7.0	—	pF		

• **Test Circuit**

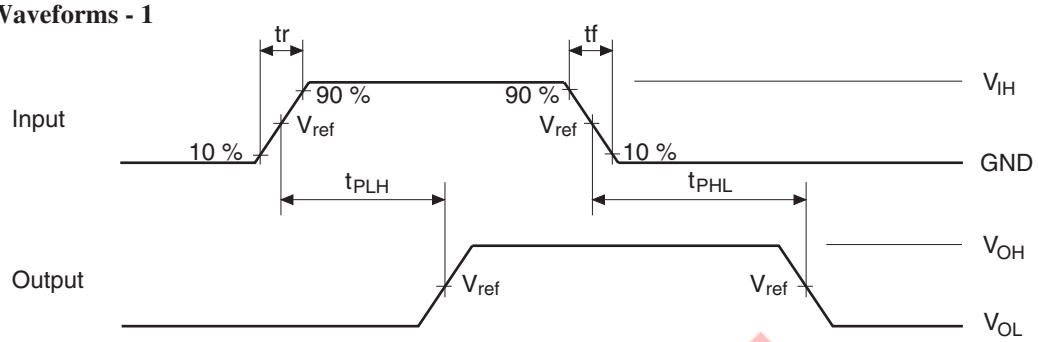


Load Circuit for Outputs

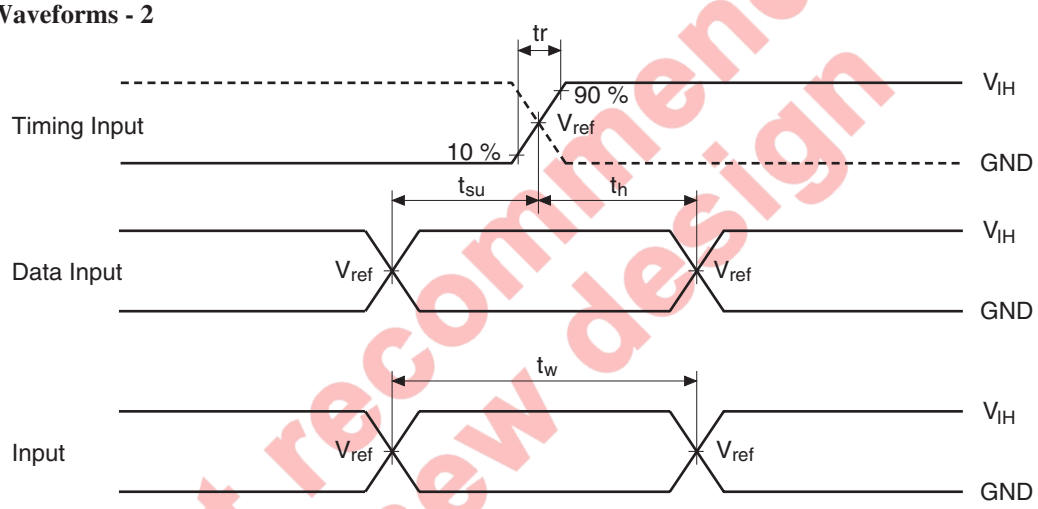
Symbol	Vcc=2.5±0.2V	Vcc=2.7V, 3.3±0.3V
t_{PLH}/ t_{PHL}	OPEN	OPEN
t_{su} / t_h / t_w		
t_{ZH}/ t_{HZ}	GND	GND
t_{ZL}/ t_{LZ}	4.6 V	6.0 V

Note: 1. C_L includes probe and jig capacitance.

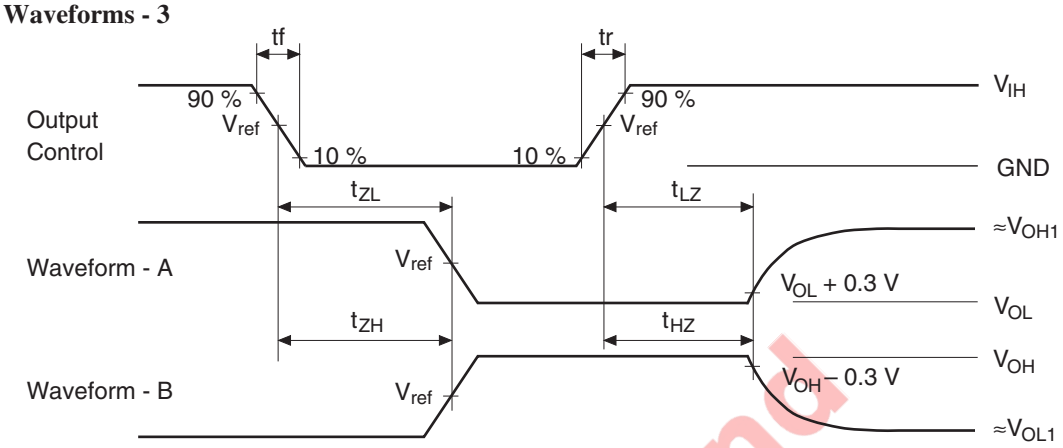
• **Waveforms - 1**



• **Waveforms - 2**



• **Waveforms - 3**



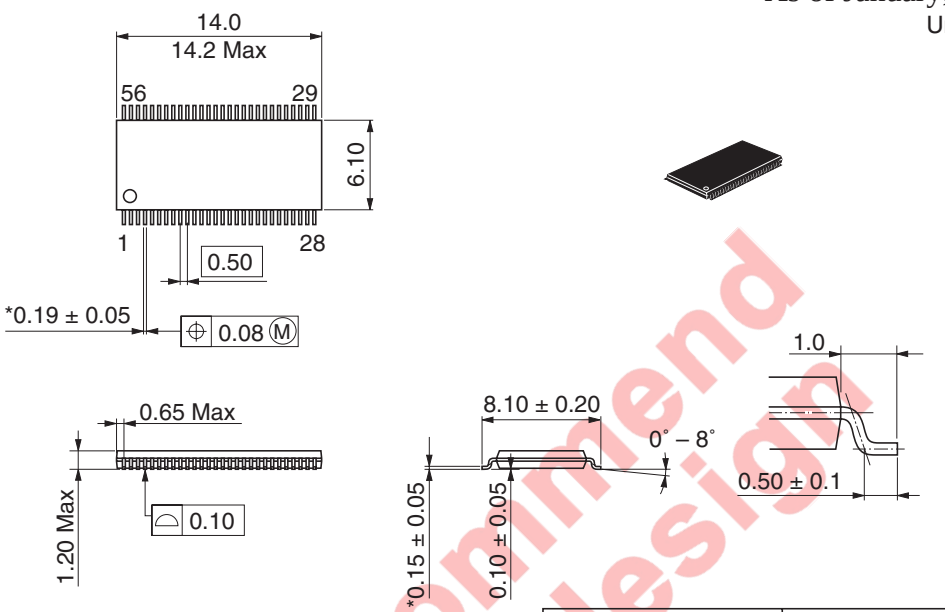
TEST	Vcc=2.5±0.2V	Vcc=2.7V, 3.3±0.3V
V_{IH}	2.3 V	2.7 V
V_{ref}	1.2 V	1.5 V
V_{OH1}	2.3 V	3.0 V
V_{OL1}	GND	GND

Notes: 1. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Zo = 50 Ω, tr ≤ 2.5 ns, tf ≤ 2.5 ns.
2. Waveform - A is for an output with internal conditions such that the output is low except when disabled by the output control.
3. Waveform - B is for an output with internal conditions such that the output is high except when disabled by the output control.
4. The output are measured one at a time with one transition per measurement.

Package Dimensions

As of January, 2003

Unit: mm



*Ni/Pd/Au plating

Package Code	TTP-56DAV
JEDEC	—
JEITA	—
Mass (reference value)	0.23 g

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