R8A66174SP
PARALLEL-IN SERIAL-OUT DATA BUFFER WITH FIFO

DESCRIPTION

The R8A66174 is a CMOS LSI with 63-byte FIFO (First-In First-Out Memory). The commands or up to 63-bytes data can be stored from 8-bit data bus. The data stored in FIFO can be outputted as serial data by executing command, and when the stored data is outputted all, R8A66174 will output an interrupt request signal. R8A66174 has 2-bit output pins (/OE, LATCH) which can set/reset outside devices by the command, R8A66174 can be connected to peripheral circuits that have a serial latch structure. R8A66174 is the succession product of M66300.
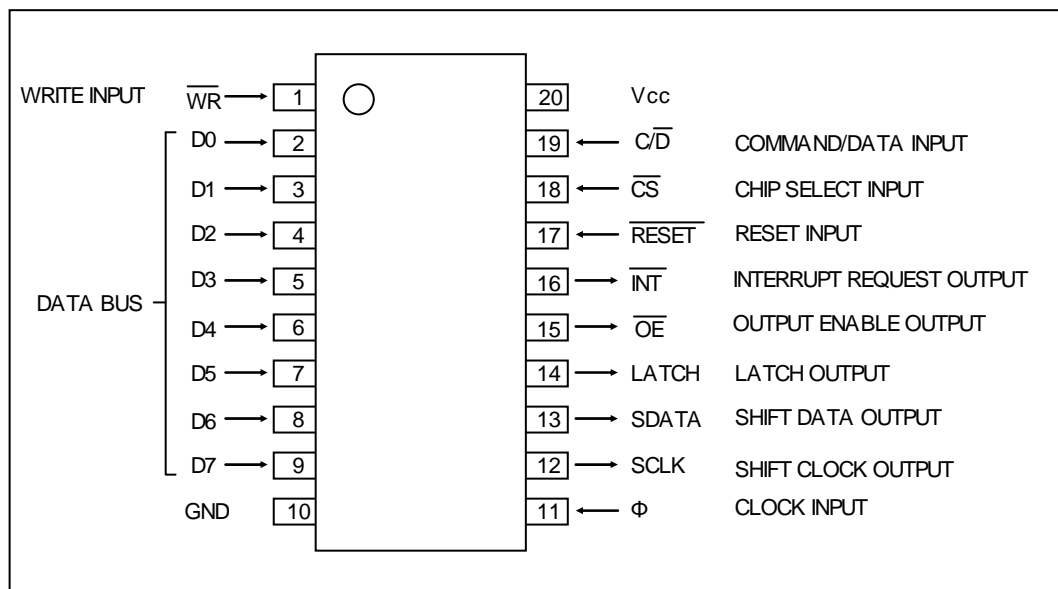
FEATURES

- General-purpose 8-bit CPU bus compatible
- Built-in 63-byte FIFO
- High-speed output (10Mbps)
- It's able to connect to LED array driver such as R8A66160 or R8A66161 directly
- Low-noise, high-output circuit
  I_{OL}=16mA, I_{OH}=-16mA (I_{OL}=4mA, I_{OH}=-4mA for /INT)
- Schmitt input (/RESET)
- Wide operating supply voltage range (Vcc=3.0~3.6V or Vcc=4.5~5.5V)
- Wide operating temperature range (Ta=-40~85°C)

APPLICATION

General digital equipment for industrial and home use, panel display controllers, and eraser unit controller for copying machine.

PIN CONFIGURATION (TOP VIEW)

BLOCK DIAGRAM

FUNCTIONAL DESCRIPTION

The information on data bus D0~D7 is loaded as command when C//D=1, and as data when C//D=0.
There are four kinds of commands.

(1) Command 1. Five kinds of division ratios of the clock input Φ are set up.

(2) Command 2. R8A66174 is set as write mode. The CPU is capable of writing 8-bit parallel data of up to 63 bytes into the internal memory (FIFO) of the R8A66174.

(3) Command 3. R8A66174 is set as serial output mode. All data written in the internal memory (FIFO) is outputted as serial data in sync with the shift clock which is set by command 1. Then, each data is outputted from LSB. When all stored data has outputted, R8A66174 will output the interrupt request /INT to CPU.

(4) Command 4. cancels the /INT and sets/resets the two control ports (LATCH, /OE).
After command4, if command3 is executed immediately, the data which is already written will be re-outputted.

FUNCTION TABLE

Command	\ Control inputs /R	/CS	C//D	/WR	D7	D6	D5	D4	D3	D2	D1	D0	SCLK	SDATA	/INT	/OE	LATCH	Remark	
—	0	×	×	×	×	×	×	×	×	×	×	×	0	0	1	1	0	Initialize	
—	1	1	×	×	×	×	×	×	×	×	×	×	*1	*1	*1	*2	*2	Memory contents not changed	
1	1	0	1	↑	1	0	0	0	×	×	×	×	0	0	1			Φ	Valid when D7 is high-level
					1	0	0	1					0	0	1			1/2 division of Φ	
					1	0	1	0					0	0	1			1/4 division of Φ	
				↓	1	0	1	1	↓	↓	↓	↓	0	0	1			1/8 division of Φ	
					1	1	0	0					0	0	1			1/16 division of Φ	
2		1		↑	0	×	×	×	0	×	×	0	0	0	1			WRITE MODE setting	WRITE MODE
		0		↑	×	×	×	×	×	×	×	×	0	0	1			WRITE operation	
3		1		↑	0	×	×	×	0	×	×	1	*3	*4	1			SERIAL OUT MODE setting	SERI. OUT MODE
		*5	×	×	×	×	×	×	×	×	×	×	*3	*4	1	↓	↓	SERIAL OUT	
		*5	×	×	×	×	×	×	×	×	×	×	0	0	0			SERIAL OUT end	
4	0	1	↑	0	×	×	×	1	D2	D1	×	0	0	1	D2	D1	set/reset the /OE and LATCH, cancel /INT	

Note1
*1 : The same operation as *3 and *4 in the SERIAL OUT mode. The output is not changed in other modes.
*2 : The output is not changed.
*3 : The Φ division pulse which is set by command 1 is outputted on /WR rise.
*4 : SDATA (n) is output on SCLK fall (n-1).
*5 : Indicates 1 when /WR is 0, don't care when /WR is 1.
X : Don't care

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BASIC OPERATION

Fig. 1 shows the basic operation flowchart. Data inputs D0~D7 are switched among four commands and 8-bit parallel data by the C//D signal. When C//D is 1, the command is stored in sync with the rise of /WR.

For initiate to work this IC, at first command 1 should be stored. Command 1 sets the division ratio for clock input Φ as 5 divisions of 1, 1/2, 1/4, 1/8 and 1/16. (The default ratio is 1.)

Then command 2 should be stored. When it is stored, 8-bit parallel data is written into the internal memory (FIFO) on the write cycle of the CPU. The maximum capacity of its FIFO is 63 bytes.

When the write operation has done, command 3 should be stored. For this action, all data in the internal memory is outputted as serial data (SDATA) in sync with the shift clock (SCLK output) which is set by command 1. Then, each data is outputted from LSB.

The SDATA changes on the fall of SCLK. When it finishes to output data, an interrupt request /INT is outputted to the CPU.

/INT is canceled by command 4 or command 2 and command 3. The command 4 sets/resets two control ports (LATCH, /OE) as well as canceling /INT. If command 3 is executed without executing command 2 after command 4, the already written-in data can be re-outputted. If it is not required to re-output the previous data, please execute command 2 before command 3 will be executed.

<Attention>

In spite of having stored write mode by command 2, when serial out mode is stored by command 3, without writing any parallel data to an internal memory (FIFO), an incorrect output appears in SDATA, SCLK, and /INT.
Please be careful.

(command 2 store ≻ data is not written ≻ command 3 store :
  Please avoid such usage.)
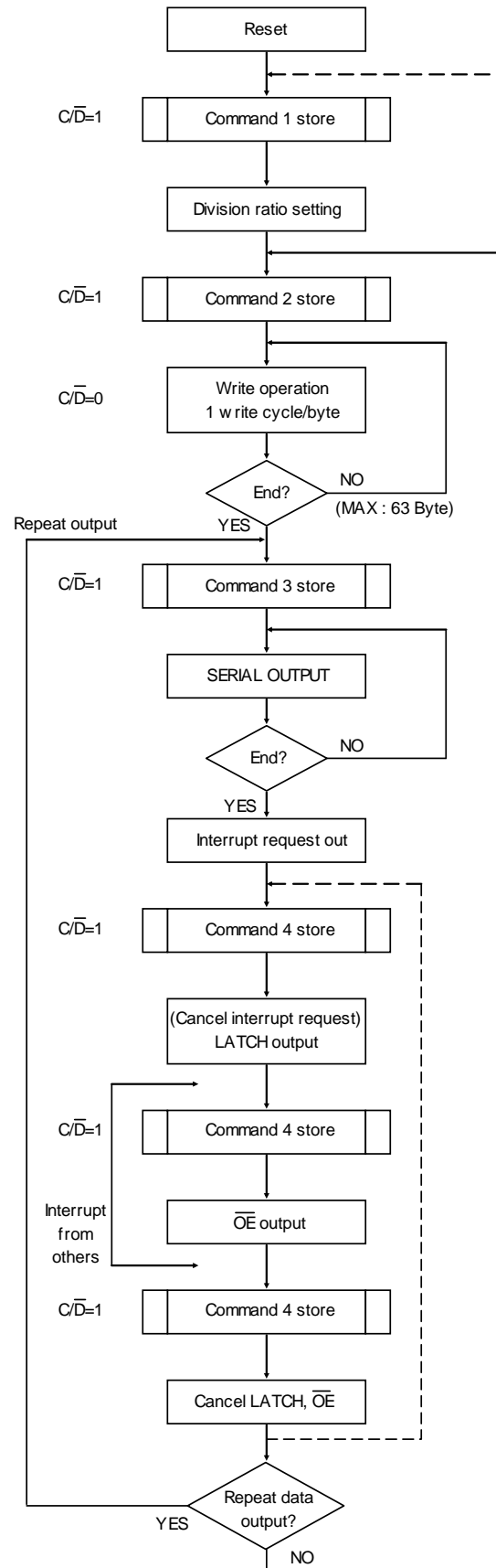
Fig. 1 Flowchart (Basic operation)

PIN DESCRIPTION

Pin name	Function
/RESET(Reset input)	When this is low-level, it clears the command and shift register and initializes the address of the internal memory (FIFO).
Φ(Clock input)	When the frequency of clock input Φ is fo,the frequency f of shift clock output SCLK is given by the following equation. $f = (1/n) \cdot fo$ (n = 1, 2, 4, 8, 16)
/CS(Chip select input)	When this is low-level, communication between the R8A66174 and the CPU becomes possible. When this is high-level, data from the CPU is ignored. However, data in the internal memory is maintained.
C//D(Command/data input)	The information on D0~D7 is regarded as commands when this is high-level and is regarded as data when this is low-level.
/WR(Write input)	On /WR rise, a command from the CPU is written into the command register and data is written into the internal memory. This input generates the serial data start signal, cancels /INT, and sets the 2-bit control ports (LATCH, /OE).
SCLK(Shift clock output)	The clock frequency is determined by D6~D4 when D7 is 1, as shown in Table 3 and Fig.2. Clock output starts on /WR rise of command 3.
SDATA(Shift data output)	All data written in the internal memory are output as serial data in sync with the SCLK.
/INT(Interrupt request output)	When output of all data in the internal memory ends, a low-level signal is output.
LATCH(Latch output)	These two outputs are set/reset by command 4 on /WR rise. The signal was named after the IC connected in the next stage, but it can be used freely for other applications.
/OE(Output enable output)	

INSTRUCTION SET
Four commands can be set by the 8-bit command words from the CPU.

Table 2 Command setting

Command	Command word	Function	Remark
1	$80_{16} \sim C0_{16}$	Division ratio setting	Note2
2	00_{16}	Write mode from the CPU to the internal memory is set.	Note3
3	01_{16}	Data output mode from the internal memory (FIFO) is set.	
4	$08_{16} \sim 0F_{16}$	Cancels the /INT and sets the two control ports (LATCH, /OE).	Note3,4

Note 2 : Lower byte can be 0~F.
   3 : Upper byte can be 1~7.
   4 : /INT can also be canceled by command 2 or command 3.

Fig. 2 shows the method for determining the command word for the instruction set. When D7 is 1, D3~D0 are masked and when D3 is 1, D0 is masked.

Table 3 Division ratio setting

D7~D4	Division
8	Φ
9	1/2 of Φ
A	1/4 of Φ
B	1/8 of Φ
C	1/16 of Φ

Table 4 /OE, LATCH setting

D3~D0	/OE	LATCH	/INT cancellation
8, 9	0	0	It is canceled
A, B	0	1	
C, D	1	0	
E, F	1	1	

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D6	D5	D4	Division ratio
0	0	0	Φ
0	0	1	1/2 of Φ
0	1	0	1/4 of Φ
0	1	1	1/8 of Φ
1	0	0	1/16 of Φ

1 Division ratio setting

When D7 = 1

Set/Reset LATCH and /OE, and cancel /INT

1

When D3 = 1

D2	D1	/OE	LATCH
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

When D7 = D3 = 0

D0	Mode setting
0	WRITE
1	SERIAL OUT

D7	D6	D5	D4	D3	D2	D1	D0
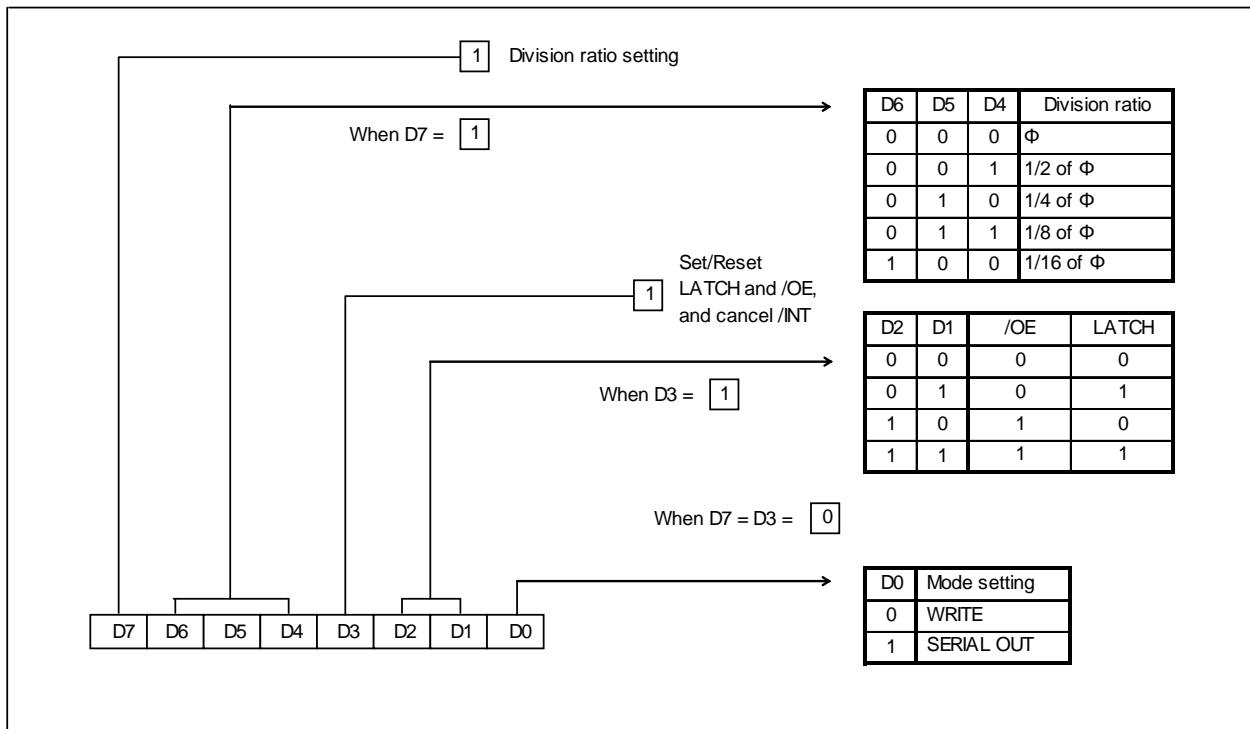
Fig. 2 Instruction set

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EXAMPLE OF TIME CHART
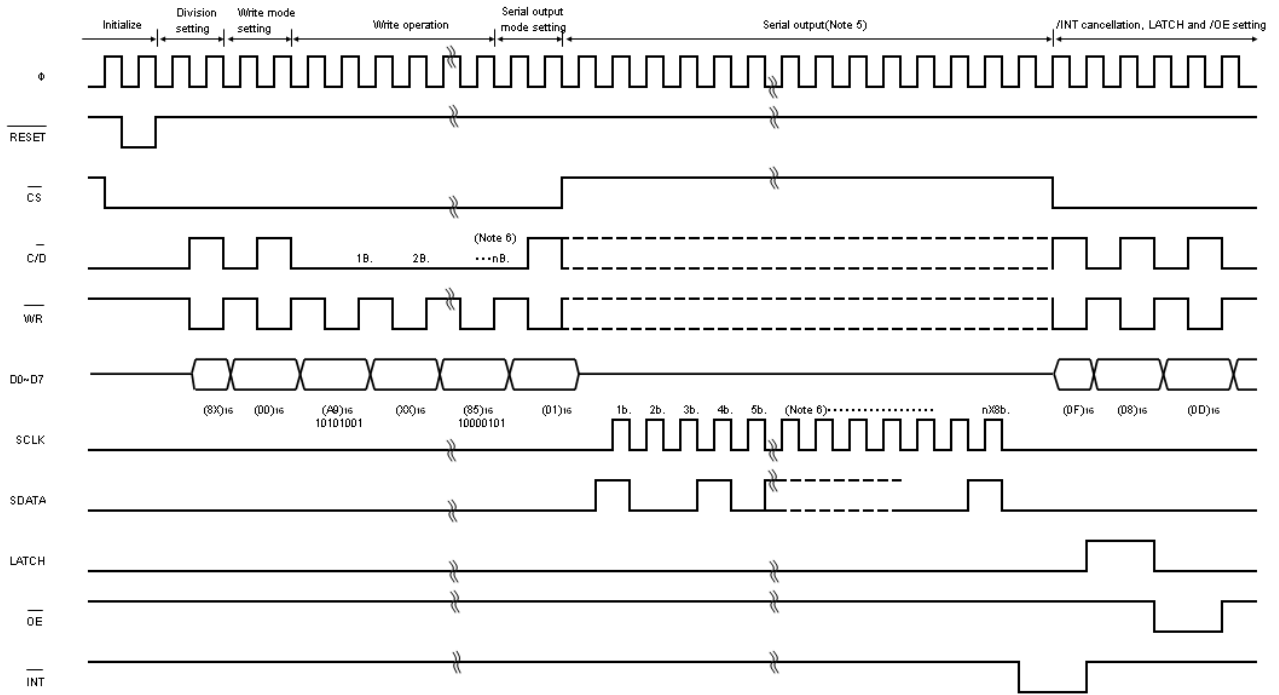
Note 5 : Always maintain /WR at high-level when /CS is low-level.
6 : B.=Byte, b.=bit
7 : Φ need not be the CPU signal. (Φ and /WR need not be synchronous.)
8 : Φ indicates the value when division ratio is set 1. If the division ratio is other than 1, a similar time chart is obtained if Φ is regarded as the waveform divided.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		-0.5~+7.0	V
V_I	Input voltage		-0.5~Vcc+0.5	V
V_O	Output voltage		-0.5~Vcc+0.5	V
Pd	Power dissipation		500	mW
Tstg	Storage temperature		-65~150	℃

RECOMMENDED OPERATING CONDITIONS（Ta=-40~85℃）

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage	5.0V	4.5	5.0	5.5	V
		3.3V	3.0	3.3	3.6	V
GND	Supply voltage			0		V
V_I	Input voltage		0		Vcc	V
V_O	Output voltage		0		Vcc	V
Topr	Operating temperature range		-40		85	℃

ELECTRICAL CHARACTERISTICS

■ 5.0V version support specifications (Ta=-40~85℃, Vcc=4.5~5.5V)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage		Inputs except /RESET	0.75XVcc			V
V_{IL}	Low-level input voltage					0.25XVcc	V
V_{T+}	Positive input threshold voltage			0.35XVcc		0.8XVcc	V
V_{T-}	Negative input threshold voltage		/RESET	0.2XVcc		0.65XVcc	V
V_H	Hysteresis width			0.4			V
V_{OH}	High-level output voltage	/INT	IOH=-4mA	Vcc-0.8			V
		Outputs except /INT	IOH=-16mA	Vcc-0.8			V
V_{OL}	Low-level output voltage	/INT	IOL=4mA			0.53	V
		Outputs except /INT	IOL=16mA			0.53	V
Icc	Supply current		VI=Vcc or GND			50	mA
I_{IH}	High-level input current		VI=Vcc			+1	µA
I_{IL}	Low-level input current		VI=0V			-1	µA

■ 3.3V version support specifications(Ta=-40~85℃, Vcc=3.0~3.6V)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage		Inputs except /RESET	0.75XVcc			V
V_{IL}	Low-level input voltage					0.25XVcc	V
V_{T+}	Positive input threshold voltage			0.35XVcc		0.8XVcc	V
V_{T-}	Negative input threshold voltage		/RESET	0.2XVcc		0.65XVcc	V
V_H	Hysteresis width			0.4			V
V_{OH}	High-level output voltage	/INT	IOH=-2mA	Vcc-0.4			V
		Outputs except /INT	IOH=-8mA	Vcc-0.6			V
V_{OL}	Low-level output voltage	/INT	IOL=2mA			0.4	V
		Outputs except /INT	IOL=8mA			0.5	V
Icc	Supply current		VI=Vcc or GND			50	mA
I_{IH}	High-level input current		VI=Vcc			+1	µA
I_{IL}	Low-level input current		VI=0V			-1	µA

Note 9 : The current flowing into the IC is positive (no sign).

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TIMING REQUIREMENTS (Ta=-40~85ºC, Vcc=4.5~5.5V or 3.0~3.6V)

Symbol	Parameter	Test condition	Limits for 5.0V			Limits for 3.3V			Unit
			Min	Typ	Max	Min	Typ	Max	
tw(Φ)	Clock pulse width		50			60			ns
tw(/W)	Write pulse width		100			120			ns
tw(/R)	Reset pulse width		100			120			ns
t_{su}(D-/W)	Data setup time before write		50			60			ns
t_h(/W-D)	Data hold time after write		0			0			ns
t_{su}(A-/W)	Address setup time before write		0			0			ns
t_h(/W-A)	Address hold time after write		0			0			ns
trec(/W)	Write recovery time		100			120			ns
trec(/INT-/W)	Write recovery time after /INT		100			120			ns
trec(/R-/W)	Write recovery time after reset		100			120			ns

Note 10 : Increase of the input rise time (tr) and fall time (tf) of clock input Φ may cause misoperation.
　　　　tr, tf : These are recommended to be 20ns or less.

SWITCHING CHARACTERISTICS(Ta=-40~85ºC, Vcc=4.5~5.5V or 3.0~3.6V)

Symbol	Parameter	Test condition	Limits for 5.0V			Limits for 3.3V			単位
			Min	Typ	Max	Min	Typ	Max	
tc(Φ)	Clock Cycle		100			120			ns
tPLH(/W-/INT)	Propagation time between write and /INT	C$_L$=50pF			100			120	ns
tPLH(/R-/INT)	Propagation time between /RESET and /INT				100			120	ns
tPLH(/W-/OE)	Propagation time between write and /OE				100			120	ns
tPHL(/W-/OE)					100			120	ns
tPLH(/W-LA)	Propagation time between write and LATCH				100			120	ns
tPHL(/W-LA)					100			120	ns
tPLH(/W-SC)	Propagation time between write and SCLK		1×T	—	2×T+100	1×T	—	2×T+120	ns
tPLH(Φ-SC)	Propagation time between Φ and SCLK	CL=150pF			100			120	ns
tPLH(Φ-SD)	Propagation time between Φ and SDATA				100			120	ns
tPHL(Φ-SD)					100			120	ns
tPHL(Φ-/INT)	Propagation time between Φ and /INT				100			120	ns
tPLH(/R-/OE)	Propagation time between /RESET and /OE				100			120	ns
tPHL(/R-LA)	Propagation time between /RESET and LATCH				100			120	ns
tTLH	Low to high level output transition time (/INT)	C$_L$=50pF			25			30	ns
tTHL	High to low level output transition time (/INT)				25			30	ns
tTLH	Low to high level output transition time (SCLK, SDATA, /OE, LATCH)	C$_L$=150pF			25			30	ns
tTHL	High to low level output transition time (SCLK, SDATA, /OE, LATCH)				25			30	ns

Note 11 : T=(1/Φ)×(1/division ratio) [ns]
　　12 : AC test waveform
　　　　Input pulse level　　　　0~Vcc
　　　　Input pulse rise time　　6ns
　　　　Input pulse fall time　　6ns
　　　　Reference voltage
　　　　　Input voltage　　　　0.5XVcc
　　　　　Output voltage　　　　0.5XVcc

TIMING DIAGRAM

Instruction set 1~4

Note 14 : Output when command 3 is set.
Note 15 : Output when command 4 is set.

Note 13 : The timing diagram when division ratio is set (1/2, 1/4, 1/8, 1/16) is regarded as the waveform as divided by Φ.
There are specific Φ inputs for switching from each Φ state.
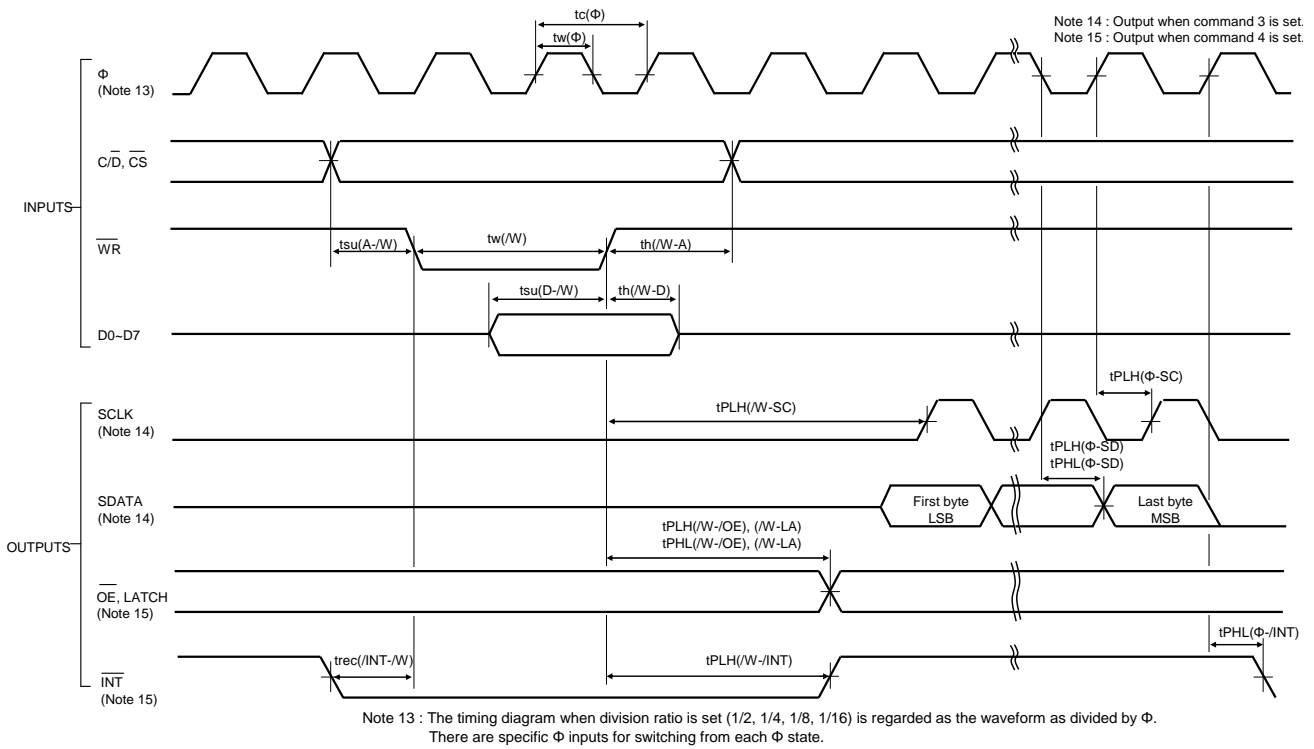
Timing diagram when RESET
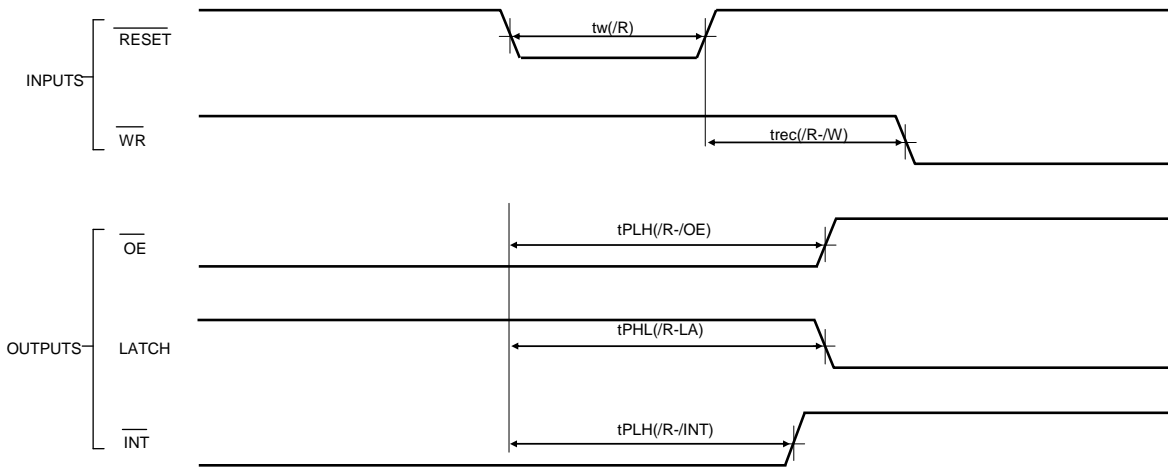
WR recovery time other than data reading
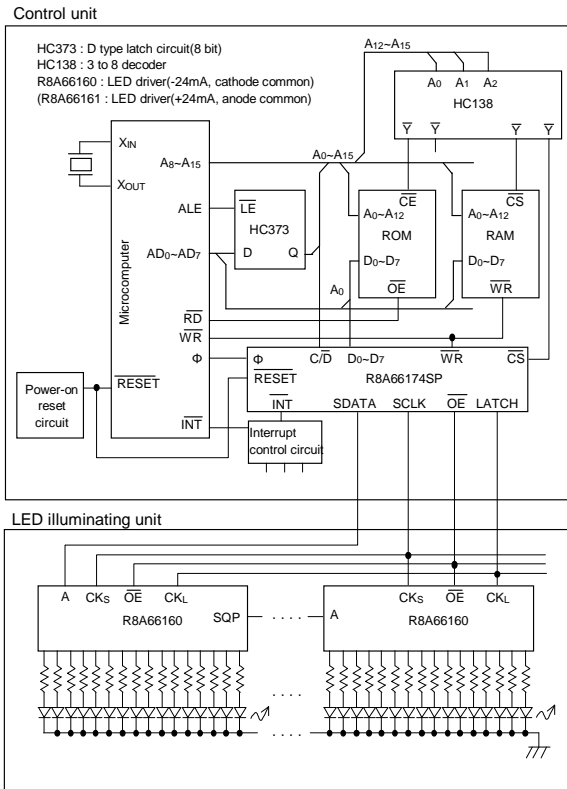
Fig. 3 Application example 1(PPC copying machine eraser circuit)
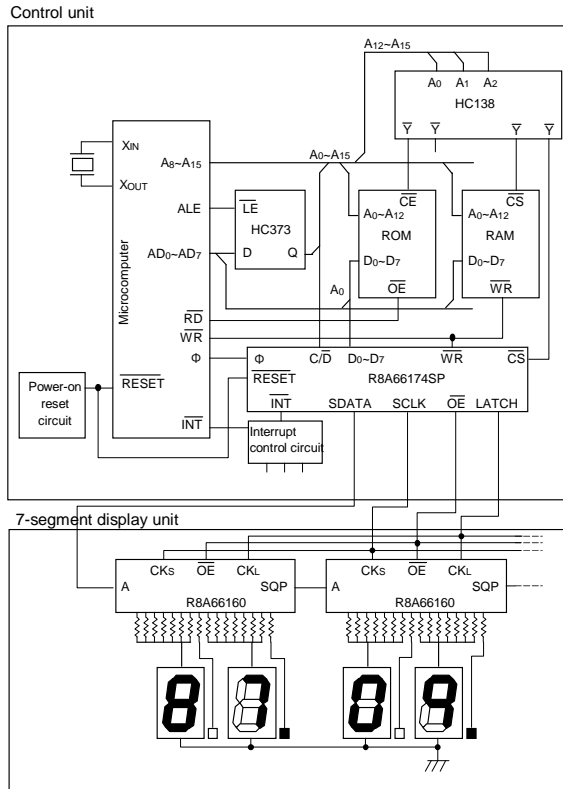
Fig. 4 Application example 2(Panel display circuit)

PACKAGE OUTLINE

Package	RENESAS Code	Previous Code
20pin SOP	PRSP0020DG-A	20P2X-C

NOTE:
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	12.60	12.80	12.90
E	7.39	7.49	7.59
A2	—	2.31	—
A1	0.10	0.20	0.30
A	—	—	2.65
bp	0.31	0.41	0.51
c	0.16	0.25	0.33
θ	0°	—	8°
HE	10.01	10.31	10.64
e	—	1.27	—
x	—	—	0.25
y	—	—	0.10
ZD	—	0.71	—
Lp	0.35	—	—
L1	—	1.41	—
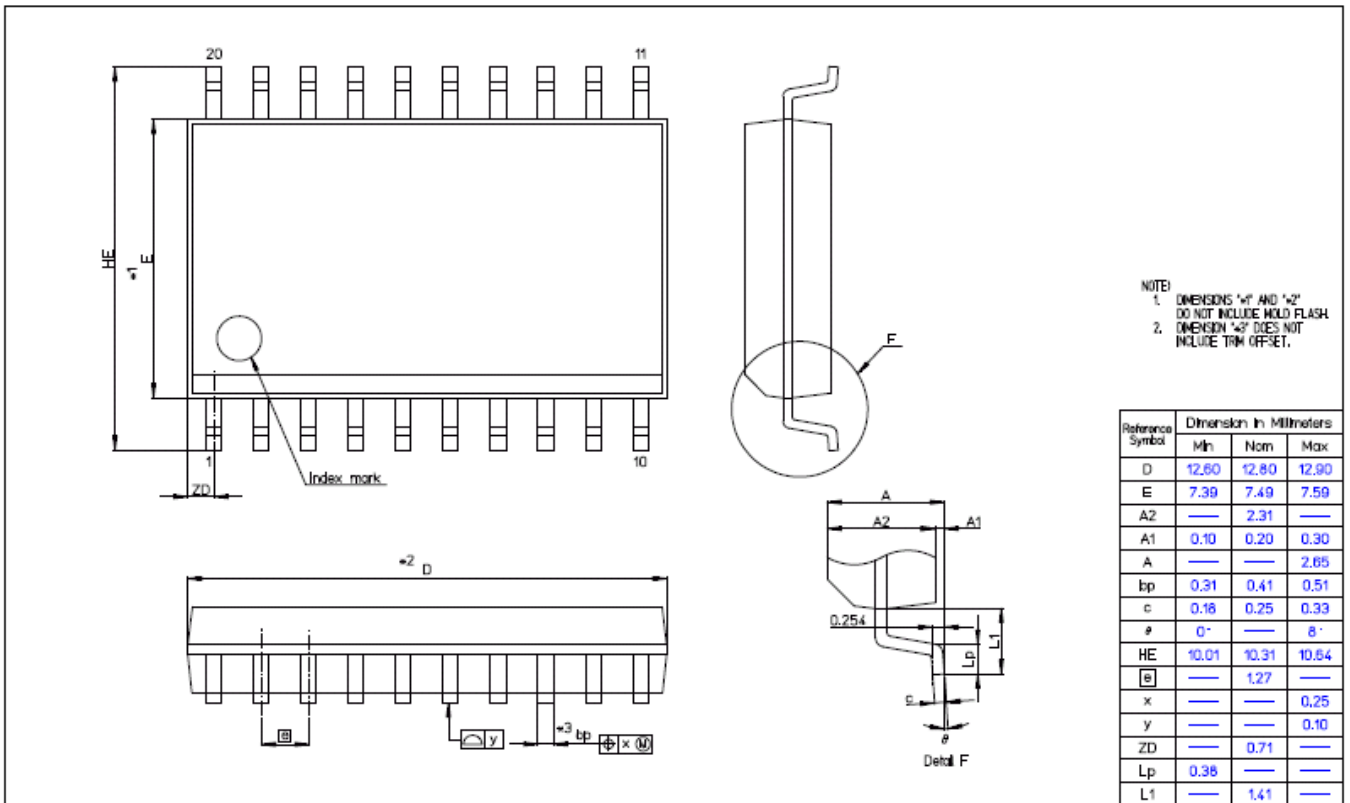
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