**KK74HC14A**

Hex Schmitt-Trigger Inverter

The KK74HC14A is identical in pinout to the LS/ALS14. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

The KK74HC14A is useful to "square up" slow input rise and fall times. Due to the hysteresis voltage of the Schmitt trigger, the KK74HC14A finds applications in noisy environments.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices

N SUFFIX
PLASTIC

14   1

D SUFFIX
SOIC

14   1
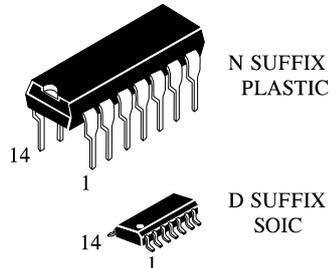
ORDERING INFORMATION

KK74HC14AN   Plastic
KK74HC14AD   SOIC

T_A = -55° to 125° C for all packages

LOGIC DIAGRAM

$Y = \bar{A}$
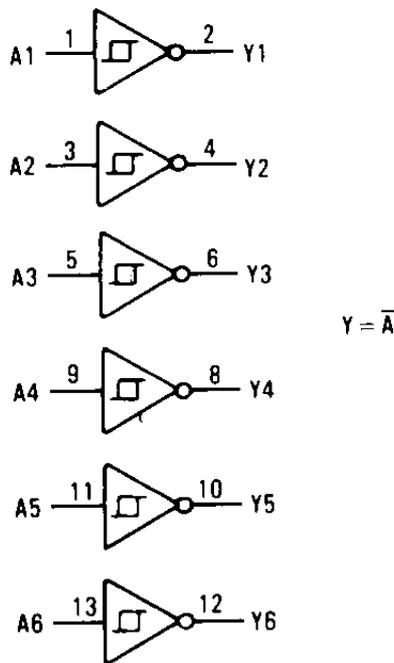
PIN 14 = V_{CC}
PIN 7 = GND

PIN ASSIGNMENT

A1	1●	14	V_{CC}
Y1	2	13	A6
A2	3	12	Y6
Y2	4	11	A5
A3	5	10	Y5
Y3	6	9	A4
GND	7	8	Y4
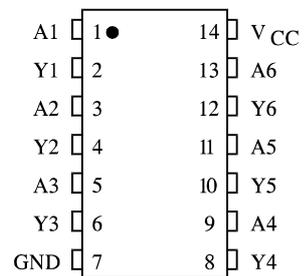
FUNCTION TABLE

Inputs	Output
A	Y
L	H
H	L

MAXIMUM RATINGS[*]

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V_{CC} +1.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, Plastic DIP** SOIC Package**	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

[*]Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
**Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
        SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	-	No Limit*	ns

* When $V_{IN} \approx 50\%$ V_{CC}, $I_{CC} > 1mA$

        This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.
        Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V_T+max	Maximum Positive-Going Input Threshold Voltage	V_{OUT}=0.1 V $\mid I_{OUT} \mid \le$ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_T+min	Minimum Positive-Going Input Threshold Voltage	V_{OUT}=0.1 V $\mid I_{OUT} \mid \le$ 20 μA	2.0 4.5 6.0	1.0 2.3 3.0	0.95 2.25 2.95	0.95 2.25 2.95	V
V_T-max	Maximum Negative-Going Input Threshold Voltage	V_{OUT}=V_{CC} -0.1 V $\mid I_{OUT} \mid \le$ 20 μA	2.0 4.5 6.0	0.9 2.0 2.6	0.95 2.05 2.65	0.95 2.05 2.65	V
V_T-min	Minimum Negative-Going Input Threshold Voltage	V_{OUT}=V_{CC}-0.1 V $\mid I_{OUT} \mid \le$ 20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
$V_H$max *	Maximum Hysteresis Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V $\mid I_{OUT} \mid \le$ 20 μA	2.0 4.5 6.0	1.2 2.25 3.0	1.2 2.25 3.0	1.2 2.25 3.0	V
$V_H$min *	Minimum Hysteresis Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V $\mid I_{OUT} \mid \le$ 20 μA	2.0 4.5 6.5	0.2 0.4 0.5	0.2 0.4 0.5	0.2 0.4 0.5	V
V_{OH}	Minimum High-Level Output Voltage	$V_{IN} \le V_T$ -min $\mid I_{OUT} \mid \le$ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{IN} \le V_T$ -min $\mid I_{OUT} \mid \le$4mA $\mid I_{OUT} \mid \le$5.2mA	4.5 6.0	3.98 5.48	3.84 5.34	3.7 5.2	
V_{OL}	Maximum Low-Level Output Voltage	$V_{IN} \ge V_T$ +max $\mid I_{OUT} \mid \le$ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{IN} \ge V_T$ +max $\mid I_{OUT} \mid \le$ 4mA $\mid I_{OUT} \mid \le$5.2mA	4.5 6.0	0.26 0.26	0.33 0.33	0.4 0.4	
I_{IN}	Maximum Input Leakage Current	V_{IN}=V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}=V_{CC} or GND I_{OUT}=0μA	6.0	1.0	10	40	μA

* $V_H$min>(V_T+min)-(V_T-max); $V_H$max=(V_T+max)-(V_T-min)

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AC ELECTRICAL CHARACTERISTICS (C$_L$=50pF, t$_r$=t$_f$=6.0 ns)

| Symbol	Parameter	V$_{CC}$ V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
t$_{PLH}$, t$_{PHL}$	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	2.0 4.5 6.0	95 19 16	120 24 20	145 29 25	ns
t$_{TLH}$, t$_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C$_{IN}$	Maximum Input Capacitance	-	10	10	10	pF
C$_{PD}$	Power Dissipation Capacitance (Per Inverter) Used to determine the no-load dynamic power consumption: P$_D$=C$_{PD}$V$_{CC}$^{2}f+I$_{CC}$V$_{CC}$	T$_A$=25°C,V$_{CC}$=5.0 V 22				pF
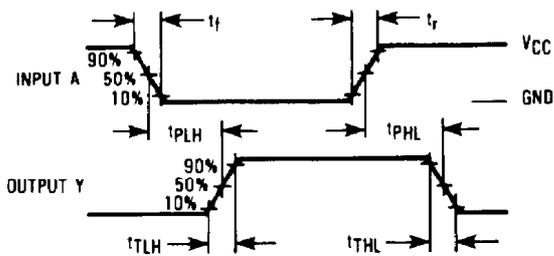
Figure 1. Switching Waveforms
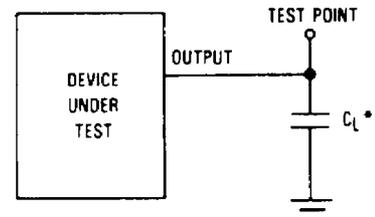
Figure 2. Test Circuit

N SUFFIX PLASTIC DIP
(MS - 001AA)

|	Dimension, mm	
Symbol	**MIN**	**MAX**
A	18.67	19.69
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	
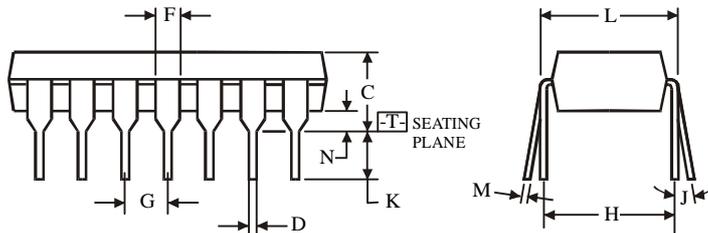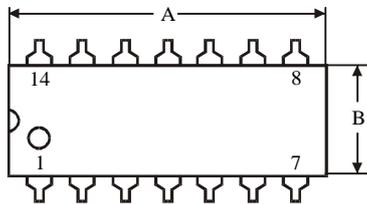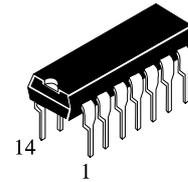
⊕ | 0.25 (0.010) Ⓜ | T

NOTES:

1. Dimensions "A", "B" do not include mold flash or protrusions.

   Maximum mold flash or protrusions 0.25 mm (0.010) per side.

D SUFFIX SOIC
(MS - 012AB)

	Dimension, mm	
Symbol	**MIN**	**MAX**
A	8.55	8.75
B	3.8	4
C	1.35	1.75
D	0.33	0.51
F	0.4	1.27
G	1.27	
H	5.27	
J	0°	8°
K	0.1	0.25
M	0.19	0.25
P	5.8	6.2
R	0.25	0.5
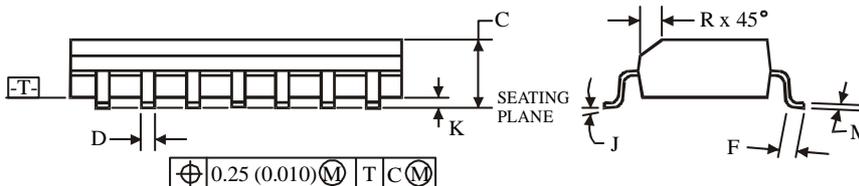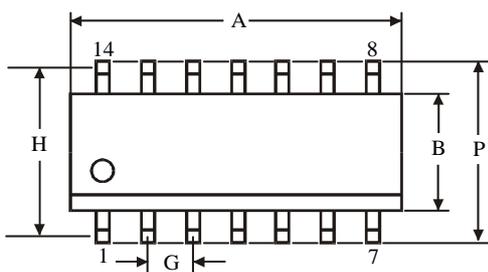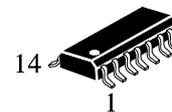
⊕ | 0.25 (0.010) Ⓜ | T | C Ⓜ

NOTES:

1. Dimensions A and B do not include mold flash or protrusion.

2. Maximum mold flash or protrusion 0.15 mm (0.006) per side
   for A; for B – 0.25 mm (0.010) per side.