

RD74VT1G125

Bus Buffer Gate with 3–state output / Dual Supply Voltage Translator

REJ03D0496–0200

Rev.2.00

Apr. 01, 2005

Description

The RD74VT1G125 has a bus buffer gate with 3–state output in a 6 pin package. Output is disabled when the associated output enable (\overline{OE}) input is high. To ensure the high impedance state during power up or power down, \overline{OE} should be connected to V_{CCIN} through a pull-up resistor, the minimum value of the resistor is determined by the current sinking capability of the driver. The input is designed to track V_{CCIN} , which accepts voltages from 1.2 V to 3.6 V, and the output is designed to track V_{CCOUT} , which operates at 1.2 V to 3.6 V. Low voltage and high-speed operation is suitable for the battery powered products (e.g., notebook computers), and the low power consumption extends the battery life.

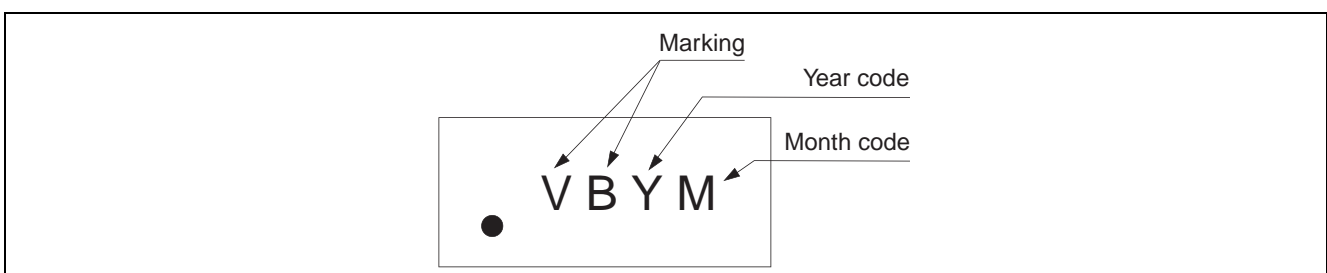
Features

- This product function as level shift that change V_{CCIN} input level to V_{CCOUT} output level by providing different supply voltage to V_{CCIN} and V_{CCOUT} .
- Supplied on emboss taping for high-speed automatic mounting.
- Supply voltage range: $V_{CCIN} = 1.2\text{ V to }3.6\text{ V}$
 $V_{CCOUT} = 1.2\text{ V to }3.6\text{ V}$
- Operating temperature range: $-40^{\circ}\text{C to }+85^{\circ}\text{C}$
- All inputs $V_{IH}(\text{Max.}) = 3.6\text{ V} (@V_{CCIN} = 0\text{ V to }3.6\text{ V})$
Outputs $V_O(\text{Max.}) = 3.6\text{ V} (@V_{CCOUT} = 0\text{ V})$
- Output current
 $\pm 2\text{ mA} (@V_{CCOUT} = 1.2\text{ V})$
 $\pm 4\text{ mA} (@V_{CCOUT} = 1.4\text{ V to }1.6\text{ V})$
 $\pm 6\text{ mA} (@V_{CCOUT} = 1.65\text{ V to }1.95\text{ V})$
 $\pm 18\text{ mA} (@V_{CCOUT} = 2.3\text{ V to }2.7\text{ V})$
 $\pm 24\text{ mA} (@V_{CCOUT} = 3.0\text{ V to }3.6\text{ V})$

Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
RD74VT1G125CLE	WCSP–6 pin	SXBG0006KB–A (TBS–6AV)	CL	E (3,000 pcs / reel)

Article Indication

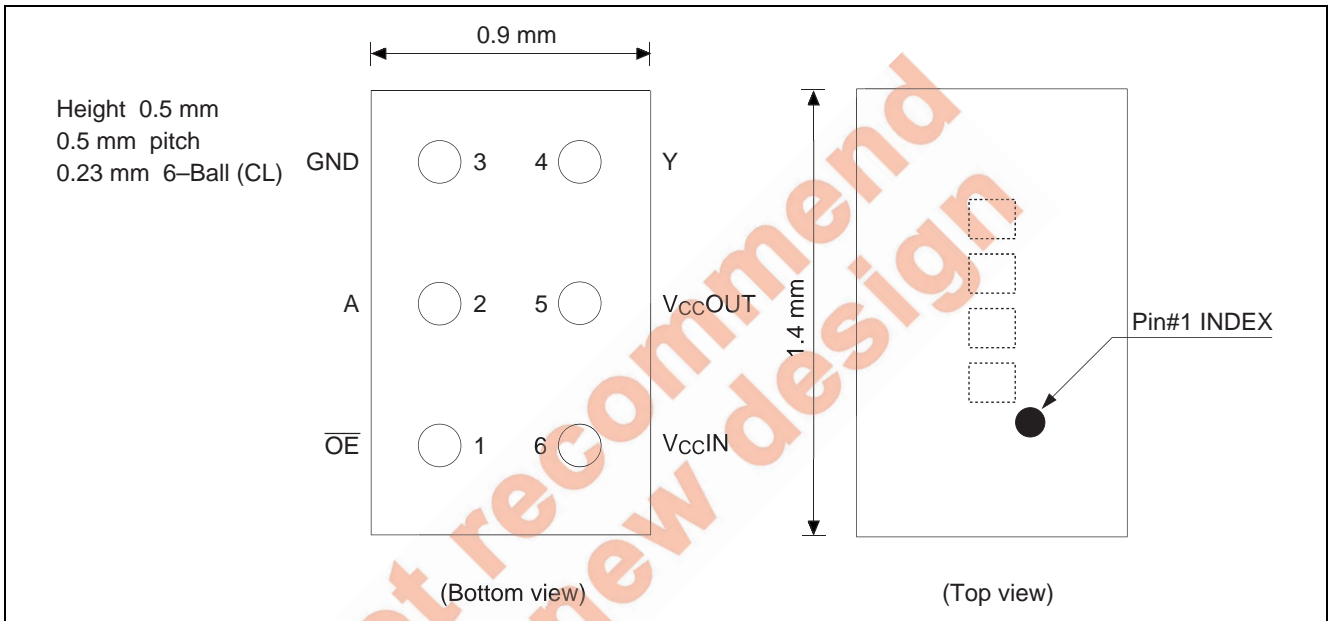


Function Table

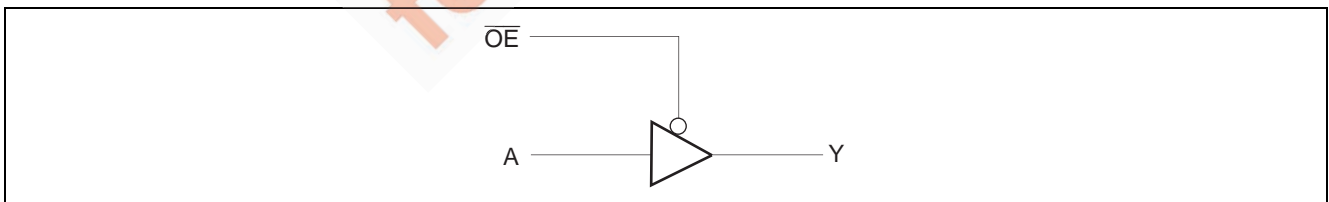
Inputs		OUTPUT Y
\overline{OE}	A	
L	H	H
L	L	L
H	X	Z

H: High level
 L: Low level
 X: Immaterial
 Z: High impedance

Pin Arrangement



Logic Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CCIN}, V_{CCOUT}	-0.5 to 4.6	V	
Input voltage range ^{*1}	V_I	-0.5 to 4.6	V	A port or \overline{OE}
Output voltage range ^{*1, 2}	V_O	-0.5 to $V_{CCOUT}+0.5$	V	Output: "H" or "L"
		-0.5 to 4.6		Output: "Z" or V_{CCOUT} : OFF
Input clamp current	I_{IK}	-50	mA	$V_I < 0$
Output clamp current	I_{OK}	-50	mA	$V_O < 0$
		50		$V_O > V_{CC}+0.5$
Continuous output current	I_O	± 50	mA	
Continuous output current V_{CC} or GND	$I_{CCIN}, I_{CCOUT}, I_{GND}$	± 100	mA	
Package Thermal impedance	θ_{ja}	123	$^{\circ}C/W$	
Storage temperature	T_{stg}	-65 to 150	$^{\circ}C$	

Notes: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

- The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- This value is limited to 4.6 V maximum.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CCIN}	1.2 to 3.6	V	
	V_{CCOUT}	1.2 to 3.6		
Input/Output voltage	V_I	0 to 3.6	V	A port or \overline{OE}
	V_O	0 to V_{CCOUT}	V	Output: "H" or "L"
0 to 3.6		Output: "Z" or V_{CCOUT} : OFF		
Output current	I_{OH}	-2	mA	$V_{CCOUT} = 1.2$ V
		-4		$V_{CCOUT} = 1.5 \pm 0.1$ V
		-6		$V_{CCOUT} = 1.8 \pm 0.15$ V
		-18		$V_{CCOUT} = 2.5 \pm 0.2$ V
		-24		$V_{CCOUT} = 3.3 \pm 0.3$ V
	I_{OL}	2	mA	$V_{CCOUT} = 1.2$ V
		4		$V_{CCOUT} = 1.5 \pm 0.1$ V
		6		$V_{CCOUT} = 1.8 \pm 0.15$ V
		18		$V_{CCOUT} = 2.5 \pm 0.2$ V
		24		$V_{CCOUT} = 3.3 \pm 0.3$ V
Input transition rise or fall time	$\Delta t / \Delta v$	10	ns / V	
Operation free-air temperature	T_a	-40 to 85	$^{\circ}C$	

Electrical Characteristics

(Ta = -40 to 85°C)

Item	Symbol	V _{CCIN} (V)*	V _{CCOUT} (V)*	Min	Typ	Max	Unit	Test conditions
Input voltage	V _{IH}	1.2	1.2 to 3.6	V _{CCIN} ×0.75	—	—	V	A port Control input
		1.5±0.1		V _{CCIN} ×0.70	—	—		
		1.8±0.15		V _{CCIN} ×0.65	—	—		
		2.5±0.2		1.6	—	—		
		3.3±0.3		2.0	—	—		
	V _{IL}	1.2	1.2 to 3.6	—	—	V _{CCIN} ×0.25	V	A port Control input
		1.5±0.1		—	—	V _{CCIN} ×0.30		
		1.8±0.15		—	—	V _{CCIN} ×0.35		
		2.5±0.2		—	—	0.7		
		3.3±0.3		—	—	0.8		
Output voltage	V _{OH}	1.2 to 3.6	1.2 to 3.6	V _{CCOUT} -0.2	—	—	V	I _{OH} = -100 μA
			1.2	0.9	—	—		I _{OH} = -2 mA
			1.5±0.1	1.1	—	—		I _{OH} = -4 mA
			1.8±0.15	1.25	—	—		I _{OH} = -6 mA
			2.5±0.2	1.7	—	—		I _{OH} = -18 mA
			3.3±0.3	2.2	—	—		I _{OH} = -24 mA
	V _{OL}	1.2 to 3.6	1.2 to 3.6	—	—	0.2	V	I _{OL} = 100 μA
			1.2	—	—	0.3		I _{OL} = 2 mA
			1.5±0.1	—	—	0.3		I _{OL} = 4 mA
			1.8±0.15	—	—	0.3		I _{OL} = 6 mA
			2.5±0.2	—	—	0.6		I _{OL} = 18 mA
			3.3±0.3	—	—	0.55		I _{OL} = 24 mA
			—	—	—	—		—
Input current	I _{IN}	3.6	3.6	-1.0	—	1.0	μA	V _{IN} = GND or V _{CCIN} control input
Off state output current	I _{OZ}	3.6	3.6	-1.5	—	1.5	μA	V _{IN} = V _{IH} or V _{IL}
Output leakage current	I _{OFF}	0	0	—	—	1.5	μA	V _{IN} , V _{OUT} = 0 to 3.6 V
Quiescent supply current	I _{CCIN}	1.2 to 3.6	1.2 to 3.6	-3.0	—	3.0	μA	I _{O(Y port)} = 0 V _{IN} = V _{CCIN} or GND
	I _{CCOUT}	1.2 to 3.6	1.2 to 3.6	-3.0	—	3.0		I _{O(Y port)} = 0 V _{IN} = V _{CCIN} or GND
Increase in I _{CC} per input	ΔI _{CC}	3.6	3.6	—	—	250	μA	A port or control V _{CCIN} -0.6 (1 input)
Input capacitance	C _{IN}	3.3	3.3	—	3.5	—	pF	V _{IN} = V _{CC} or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

 $V_{CCIN} = 3.3 \pm 0.3 \text{ V}$

Item	Symbol	From (input)	To (output)	Ta = -40 to 85°C										Unit	Test conditions
				V _{CC} OUT= 1.2 V		V _{CC} OUT= 1.5±0.1 V		V _{CC} OUT= 1.8±0.15 V		V _{CC} OUT= 2.5±0.2 V		V _{CC} OUT= 3.3±0.3 V			
				Typ	Min	Max	Min	Max	Min	Max	Min	Max	Min		
Propagation delay time	t _{PLH}	A	Y	9.2	2.0	8.8	1.5	5.8	1.0	4.2	1.0	3.5	ns	C _L = 15pF R _L = 2.0kΩ	
	t _{PHL}			9.2	2.0	8.8	1.5	5.8	1.0	4.2	1.0	3.5			
Output enable time	t _{ZH}	\overline{OE}	Y	10.2	2.0	9.6	1.5	6.4	1.0	4.2	1.0	3.7	ns	C _L = 15pF R _L = 2.0kΩ	
	t _{ZL}			10.2	2.0	9.6	1.5	6.4	1.0	4.2	1.0	3.7			
Output disable time	t _{HZ}	\overline{OE}	Y	5.2	2.0	5.6	1.5	5.2	1.0	4.6	1.0	4.5	ns	C _L = 15pF R _L = 2.0kΩ	
	t _{LZ}			5.2	2.0	5.6	1.5	5.2	1.0	4.6	1.0	4.5			

 $V_{CCIN} = 2.5 \pm 0.2 \text{ V}$

Item	Symbol	From (input)	To (output)	Ta = -40 to 85°C										Unit	Test conditions
				V _{CC} OUT= 1.2 V		V _{CC} OUT= 1.5±0.1 V		V _{CC} OUT= 1.8±0.15 V		V _{CC} OUT= 2.5±0.2 V		V _{CC} OUT= 3.3±0.3 V			
				Typ	Min	Max	Min	Max	Min	Max	Min	Max	Min		
Propagation delay time	t _{PLH}	A	Y	9.5	2.0	9.0	1.5	6.0	1.0	4.4	1.0	3.7	ns	C _L = 15pF R _L = 2.0kΩ	
	t _{PHL}			9.5	2.0	9.0	1.5	6.0	1.0	4.4	1.0	3.7			
Output enable time	t _{ZH}	\overline{OE}	Y	10.6	2.0	10.2	1.5	6.6	1.0	4.5	1.0	3.8	ns	C _L = 15pF R _L = 2.0kΩ	
	t _{ZL}			10.6	2.0	10.2	1.5	6.6	1.0	4.5	1.0	3.8			
Output disable time	t _{HZ}	\overline{OE}	Y	5.4	2.0	5.7	1.5	5.3	1.0	4.5	1.0	4.4	ns	C _L = 15pF R _L = 2.0kΩ	
	t _{LZ}			5.4	2.0	5.7	1.5	5.3	1.0	4.5	1.0	4.4			

 $V_{CCIN} = 1.8 \pm 0.15 \text{ V}$

Item	Symbol	From (input)	To (output)	Ta = -40 to 85°C										Unit	Test conditions
				V _{CC} OUT= 1.2 V		V _{CC} OUT= 1.5±0.1 V		V _{CC} OUT= 1.8±0.15 V		V _{CC} OUT= 2.5±0.2 V		V _{CC} OUT= 3.3±0.3 V			
				Typ	Min	Max	Min	Max	Min	Max	Min	Max	Min		
Propagation delay time	t _{PLH}	A	Y	9.6	2.0	9.2	1.5	6.5	1.0	4.7	1.0	4.0	ns	C _L = 15pF R _L = 2.0kΩ	
	t _{PHL}			9.6	2.0	9.2	1.5	6.5	1.0	4.7	1.0	4.0			
Output enable time	t _{ZH}	\overline{OE}	Y	10.8	2.0	10.8	1.5	7.0	1.0	5.2	1.0	4.5	ns	C _L = 15pF R _L = 2.0kΩ	
	t _{ZL}			10.8	2.0	10.8	1.5	7.0	1.0	5.2	1.0	4.5			
Output disable time	t _{HZ}	\overline{OE}	Y	5.8	2.0	6.0	1.5	5.8	1.0	5.4	1.0	5.2	ns	C _L = 15pF R _L = 2.0kΩ	
	t _{LZ}			5.8	2.0	6.0	1.5	5.8	1.0	5.4	1.0	5.2			

 $V_{CCIN} = 1.5 \pm 0.1 \text{ V}$

Item	Symbol	From (input)	To (output)	Ta = -40 to 85°C										Unit	Test conditions
				V _{CC} OUT= 1.2 V		V _{CC} OUT= 1.5±0.1 V		V _{CC} OUT= 1.8±0.15 V		V _{CC} OUT= 2.5±0.2 V		V _{CC} OUT= 3.3±0.3 V			
				Typ	Min	Max	Min	Max	Min	Max	Min	Max	Min		
Propagation delay time	t _{PLH}	A	Y	9.8	2.0	10.0	1.5	6.9	1.0	5.1	1.0	4.5	ns	C _L = 15pF R _L = 2.0kΩ	
	t _{PHL}			9.8	2.0	10.0	1.5	6.9	1.0	5.1	1.0	4.5			
Output enable time	t _{ZH}	\overline{OE}	Y	11.2	2.0	11.2	1.5	7.8	1.0	5.4	1.0	4.8	ns	C _L = 15pF R _L = 2.0kΩ	
	t _{ZL}			11.2	2.0	11.2	1.5	7.8	1.0	5.4	1.0	4.8			
Output disable time	t _{HZ}	\overline{OE}	Y	6.4	2.0	7.2	1.5	6.4	1.0	5.8	1.0	5.6	ns	C _L = 15pF R _L = 2.0kΩ	
	t _{LZ}			6.4	2.0	7.2	1.5	6.4	1.0	5.8	1.0	5.6			

Switching Characteristics (Cont.)

 $V_{CCIN} = 1.2\text{ V}$

Item	Symbol	From (input)	To (output)	$T_a = -40\text{ to }85^\circ\text{C}$					Unit	Test conditions
				$V_{CCOUT} =$ 1.2 V	$V_{CCOUT} =$ 1.5±0.1 V	$V_{CCOUT} =$ 1.8±0.15 V	$V_{CCOUT} =$ 2.5±0.2 V	$V_{CCOUT} =$ 3.3±0.3 V		
				Typ	Typ	Typ	Typ	Typ		
Propagation delay time	t_{PLH}	A	Y	10.5	7.5	6.0	4.5	4.0	ns	$C_L = 15\text{pF}$ $R_L = 2.0\text{k}\Omega$
	t_{PHL}			10.5	7.5	6.0	4.5	4.0		
Output enable time	t_{ZH}	\overline{OE}	Y	11.6	8.5	6.5	5.0	4.2	ns	$C_L = 15\text{pF}$ $R_L = 2.0\text{k}\Omega$
	t_{ZL}			11.6	8.5	6.5	5.0	4.2		
Output disable time	t_{HZ}	\overline{OE}	Y	7.0	6.2	6.0	5.7	5.5	ns	$C_L = 15\text{pF}$ $R_L = 2.0\text{k}\Omega$
	t_{LZ}			7.0	6.2	6.0	5.7	5.5		

Operating Characteristics

 $T_a = 25^\circ\text{C}$

Item	Symbol	V_{CCIN} (V)	V_{CCOUT} (V)	Min	Typ	Max	Unit	Test conditions
Power dissipation capacitance	C_{PD}	3.3	3.3	—	12	—	pF	$f = 10\text{ MHz}$ $C_L = 0$

Power-up considerations

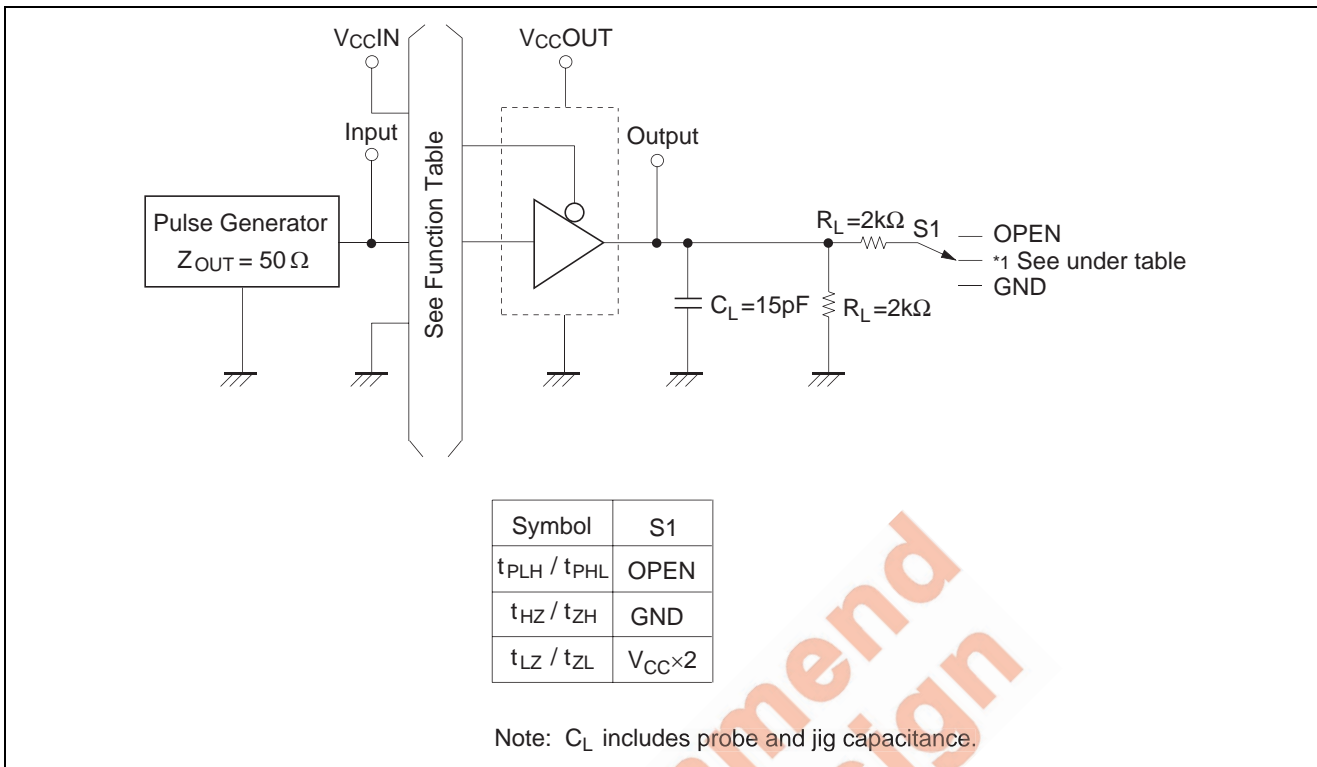
Level-translation devices offer an opportunity for successful mixed-voltage signal design.

A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device pins.

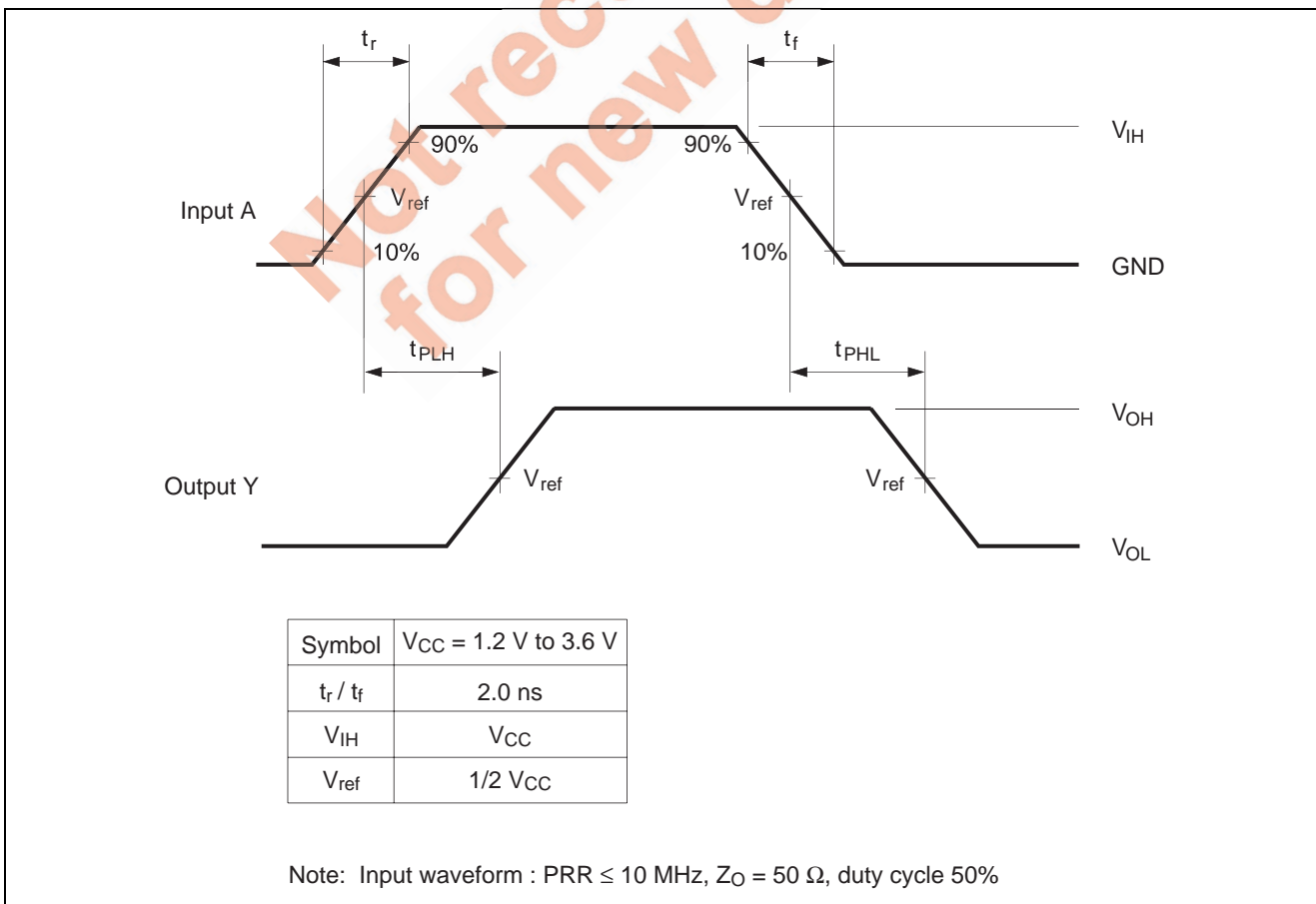
Take these precautions to guard against such power-up problems.

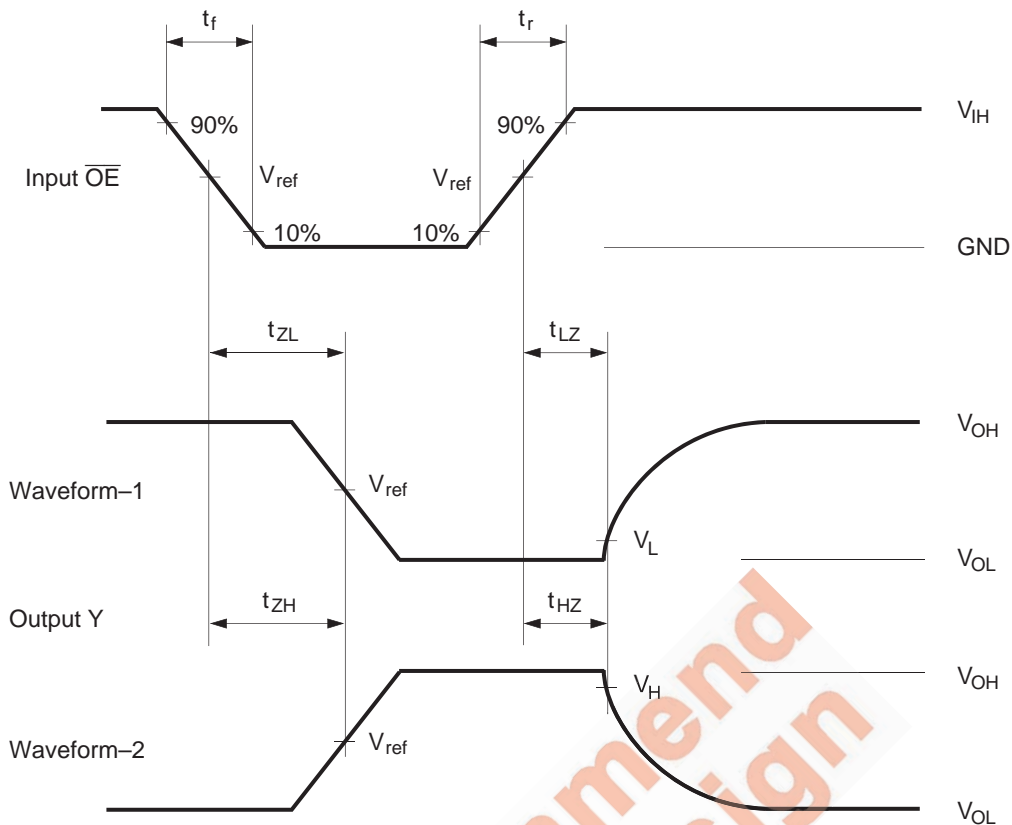
1. Connect ground before any supply voltage is applied.
2. Next, power up the control side of the device.
(Power up of V_{CCIN} is first. Next power up is V_{CCOUT})
3. Tie \overline{OE} to V_{CCIN} with a pull-up resistor so that it ramps with V_{CCIN} .

Test Circuit



Waveforms

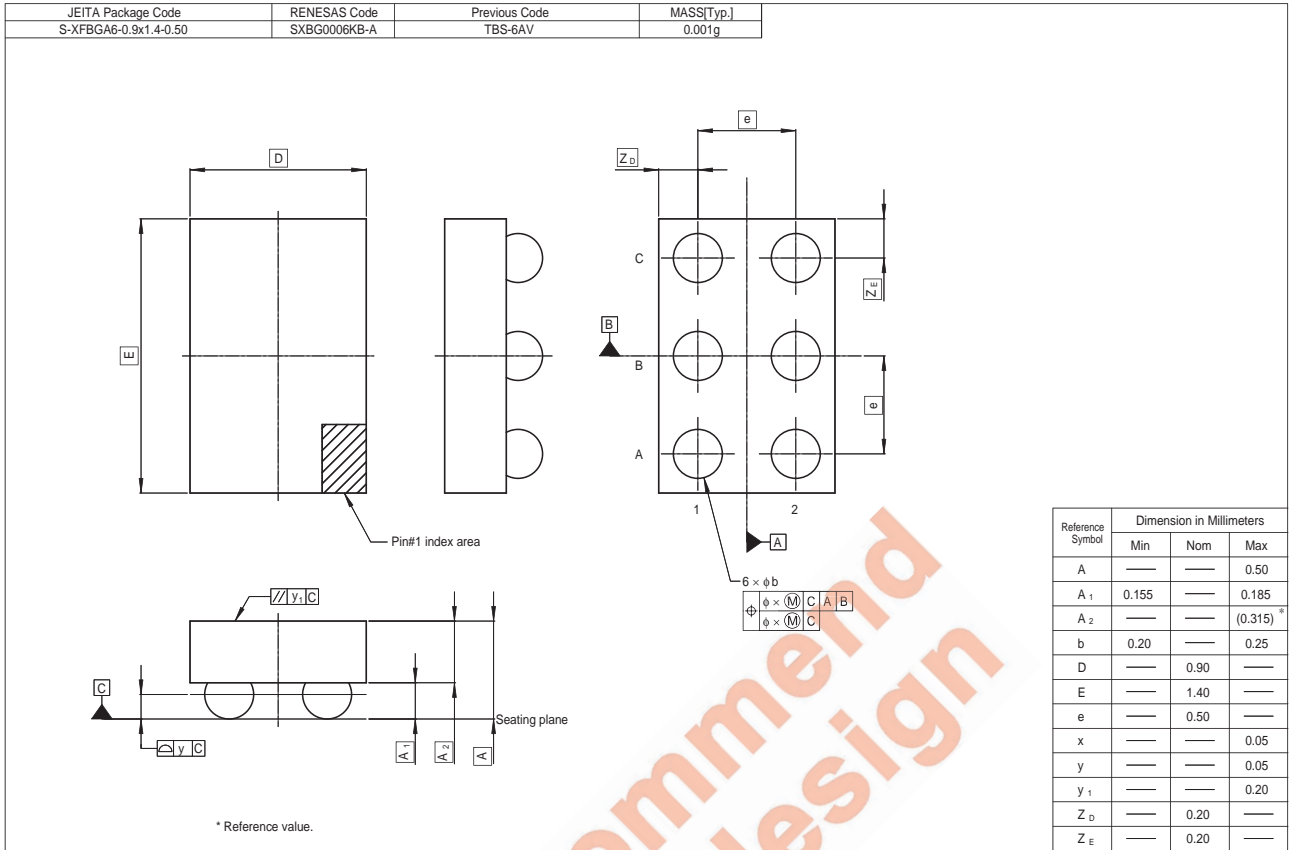




Symbol	$V_{CC} = 1.2\text{ V},$ $1.5 \pm 0.1\text{ V}$	$V_{CC} = 1.8 \pm 0.15\text{ V}$	$V_{CC} = 2.5 \pm 0.2\text{ V}$	$V_{CC} = 3.3 \pm 0.3\text{ V}$
t_r / t_f	2.0 ns	2.0 ns	2.0 ns	2.0 ns
V_{IH}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_{ref}	$1/2 V_{CC}$	$1/2 V_{CC}$	$1/2 V_{CC}$	$1/2 V_{CC}$
V_H / V_L	$V_H = V_{OH} - 0.1\text{ V}$ $V_L = V_{OL} + 0.1\text{ V}$	$V_H = V_{OH} - 0.15\text{ V}$ $V_L = V_{OL} + 0.15\text{ V}$	$V_H = V_{OH} - 0.15\text{ V}$ $V_L = V_{OL} + 0.15\text{ V}$	$V_H = V_{OH} - 0.3\text{ V}$ $V_L = V_{OL} + 0.3\text{ V}$

- Notes:
1. Input waveform : $PRR \leq 10\text{ MHz}$, $Z_o = 50\ \Omega$, duty cycle 50%.
 2. Waveform – 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 3. Waveform – 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 4. The output are measured one at a time with one transition per measurement.

Package Dimensions



Not recommended for new design

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