SPEAR-09-H042

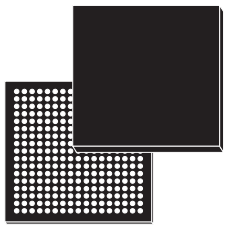
SPEAr™ Head200

ARM 926, 200 K customizable eASIC™ gates, large IP portfolio SoC

Data Brief

Features

- ARM926EJ-S - f_{MAX} 266 MHz, 32 KI - 16 KD cache, 8 KI - KD TCM, ETM9 and JTAG interfaces
- 200K customizable equivalent ASIC gates (16K LUT equivalent) with 8 channels internal DMA high speed accelerator function and 87 dedicated general purpose I/Os
- Multilayer AMBA 2.0 compliant bus with f_{MAX} 133 MHz
- Programmable internal clock generator with enhanced PLL function, specially optimized for E.M.I. reduction
- 16 KB single port SRAM embedded
- Dynamic RAM interface: 8/16 bit DDR, 8/16 bit SDRAM
- SPI interface connecting serial ROM and Flash devices
- 2 USB 2.0 Host independent ports with integrated PHYs
- USB 2.0 device with integrated PHY
- Ethernet MAC 10/100 with MII management interface
- 1 independent UART up to 115 Kbps (software flow control mode)
- I^2C master mode, fast and slow speed
- 6 general purpose I/Os



LFBGA289

- Real time clock
- WatchDog
- 4 general purpose timers
- Operating temperature: - 40 to 85 °C
- Package: LFBGA289 (15x15x1.7mm pitch 0.8mm)

Description

SPEAr Head200 is a powerful digital engine belonging to SPEAr family, the innovative customizable system-on-chip.

The device integrates an ARM core with a large set of proven IPs (Intellectual Properties) and a configurable logic block that allows very fast customization of unique and/or proprietary solutions, with low effort and low investment.

Optimized for embedded applications.

Table 1. Device summary

Order code	Package	Packing
SPEAR-09-H042	LFBGA289 (15x15x1.7mm)	Tray

Contents

1 Introduction

This data brief describes the differences between SPEAr Head200 (SPEAR-09-H022) and the one packaged in LFBGA289 balls 0.8mm pitch (SPEAR-09-H042).

In this document the main package characteristics are described as well as the chip features modifications.

The reference specifications, for the SPEAR-09-H022 are available on the web at: www.st.com.

2 Features modification

To fit the new small package a number of features has been reduced or limited:

- Analog to digital converter (ADC)
- eASIC GPIOs
- External FPGA emulation mode
- Dynamic RAM data path
- UARTs

2.1 Analog to digital converter (ADC)

ADC feature has been completely deleted so the 16 analog channels, the related test output, the power balls and the reference voltages have been removed.

2.2 eASIC GPIOs

SPEAR-09-H022 features 112 GPIOs in the eASIC customizable part, some of these I/Os have been removed, but 87 are still available on SPEAR-09-H042.

Unusable hidden eASIC GPIOs (74, 76, 78, 80, 82, 84, 86, 88, 90, 92, 94, 96, 98, 100-111) must be configured as inputs.

2.3 External FPGA emulation mode

SPEAR-09-H022 has the capability to emulate the internal eASIC behavior with an external FPGA through the component GPIOs. This feature has been completely removed on SPEAR-09-H042 hence the developement boards must use the 420 PBGA components.

2.4 Dynamic RAM data path

The SPEAr component features a multi purpose memory controller to interface SDRAM or DDR memories able to work with different data path widths.

While SPEAR-09-H022 handles 8 and 16-bit DDRs or 8, 16 and 32-bit SDRAMs, on SPEAR-09-H042 to save 16 data balls and the related "data mask" balls, the SDRAM data path has been limited to 16-bit like the DDR one.

2.5 UARTs

Two of the original UART interfaces have been removed, SPEAR-09-H042 features just the UART1 interface.

3 Pin description

Table 2 shows the component signals, grouped by function, and the relative ballout diagram.

3.1 Interface signals

Table 2. Interface signals

Group	Signal Name	Ball	Direction	Function
Debug	TEST0	A14	Input	Test configuration port. For the functional mode they have to be set to 0
	TEST1	H14		
	TEST2	H13		
	TEST3	H12		
	PLL_BYPASS	G1	Input	Enable / disable PLL bypass
eASIC	eASICGP_IO[00]	G4	I/O	eASIC general purpose I/O
	eASICGP_IO[01]	H7		
	eASICGP_IO[02]	H6		
	eASICGP_IO[03]	H5		
	eASICGP_IO[04]	F3		
	eASICGP_IO[05]	E4		
	eASICGP_IO[06]	F5		
	eASICGP_IO[07]	D2		
	eASICGP_IO[08]	E3		
	eASICGP_IO[09]	D3		
	eASICGP_IO[10]	D1		
	eASICGP_IO[11]	G6		
	eASICGP_IO[12]	G7		
	eASICGP_IO[13]	D4		
	eASICGP_IO[14]	C1		
	eASICGP_IO[15]	E5		
	eASICGP_IO[16]	F6		
	eASICGP_IO[17]	B1		
	eASICGP_IO[18]	E6		
	eASICGP_IO[19]	B4		
	eASICGP_IO[20]	F7		
	eASICGP_IO[21]	A1		

Table 2. Interface signals (continued)

Group	Signal Name	Ball	Direction	Function
	eASICGP_IO[22]	A3		
	eASICGP_IO[23]	A4		
	eASICGP_IO[24]	C2		
	eASICGP_IO[25]	F4		
	eASICGP_IO[26]	C3		
	eASICGP_IO[27]	C5		
	eASICGP_IO[28]	B5		
	eASICGP_IO[29]	H8		
	eASICGP_IO[30]	B2		
	eASICGP_IO[31]	G5		
	eASICGP_IO[32]	B3		
	eASICGP_IO[33]	A2		
	eASICGP_IO[34]	C4		
	eASICGP_IO[35]	A5		
	eASICGP_IO[36]	H9		
	eASICGP_IO[37]	C6		
	eASICGP_IO[38]	G9		
	eASICGP_IO[39]	C7		
	eASICGP_IO[40]	D5		
	eASICGP_IO[41]	B6		
	eASICGP_IO[42]	A6		
	eASICGP_IO[43]	G8		
	eASICGP_IO[44]	E8		
	eASICGP_IO[45]	E9		
	eASICGP_IO[46]	D8		
	eASICGP_IO[47]	B7		
	eASICGP_IO[48]	E7		
	eASICGP_IO[49]	F8		
	eASICGP_IO[50]	A7		
	eASICGP_IO[51]	B8		
	eASICGP_IO[52]	A8		
	eASICGP_IO[53]	D9		
	eASICGP_IO[54]	D6		
	eASICGP_IO[55]	F9		
	eASICGP_IO[56]	D7		

Table 2. Interface signals (continued)

Group	Signal Name	Ball	Direction	Function
	eASICGP_IO[57]	F10		
	eASICGP_IO[58]	C9		
	eASICGP_IO[59]	B9		
	eASICGP_IO[60]	A9		
	eASICGP_IO[61]	G10		
	eASICGP_IO[62]	C8		
	eASICGP_IO[63]	E10		
	eASICGP_IO[64]	D10		
	eASICGP_IO[65]	C10		
	eASICGP_IO[66]	B10		
	eASICGP_IO[67]	A10		
	eASICGP_IO[68]	G11		
	eASICGP_IO[69]	F11		
	eASICGP_IO[70]	E11		
	eASICGP_IO[71]	D11		
	eASICGP_IO[72]	C11		
	eASICGP_IO[73-74]	B11		
	eASICGP_IO[75-76]	A11		
	eASICGP_IO[77-78]	A12		
	eASICGP_IO[79-80]	B12		
	eASICGP_IO[81-82]	C12		
	eASICGP_IO[83-84]	D12		
	eASICGP_IO[85-86]	E12		
	eASICGP_IO[87-88]	A13		
	eASICGP_IO[89-90]	B13		
	eASICGP_IO[91-92]	C13		
	eASICGP_IO[93-94]	D13		
	eASICGP_IO[95-96]	E13		
	eASICGP_IO[97-98]	C14		
	eASICGP_IO[99]	D14		
	eASIC_EXT_CLOCK	E14		
	eASIC_PI_CLOCK	K15		eASIC program interface out clock
Ethernet	TX_CLK	C15	Input	Ethernet input TX clock
	TXD[0]	C16		Ethernet TX output data
	TXD[1]	C17		Ethernet TX output data

Table 2. Interface signals (continued)

Group	Signal Name	Ball	Direction	Function
	TXD[2]	D15	Output	Ethernet TX output data
	TXD[3]	D16		Ethernet TX output data
	TX_EN	D17		Ethernet TX enable
	CRS	E15	Input	Carrier sense input
	COL	E16		Collision detection input
	RX_CLK	E17	Input	Ethernet input RX clock
	RXD[0]	F15	Input	Ethernet RX input data
	RXD[1]	F16		
	RXD[2]	F17		
	RXD[3]	G15		
	RX_DV	G16	Input	Data valid on RX
	RX_ER	G17	Input	Data error detected
	MDC	H15	Output	Output timing reference for MDIO
	MDIO	H16	I/O	I/O data to PHY
GPI/Os	GP_IO[0]	M15	I/O	General purpose I/O
	GP_IO[1]	L17		
	GP_IO[2]	L16		
	GP_IO[3]	L15		
	GP_IO[4]	K17		
	GP_IO[5]	K16		
I2C	SDA	H17	I/O	I2C serial data
	SCL	J15	Output	I2C clock
JTAG	TDO	F12	Output	JTAG TDO
	TDI	F13	Input	JTAG TDI
	TMS	F14	Input	JTAG TMS
	RTCK	G12	Output	JTAG output clock
	TCK	G13	Input	JTAG clock
	nTRST	G14	Output	JTAG reset
Master clock	MCLK_in	N1	Input	12MHz input crystal
	MCLK_out	N2	Output	12MHz output crystal
Master reset	MRESET	G3	Input	Master reset
MPMC	MPMCDATA[00]	T12		
	MPMCDATA[01]	R12		
	MPMCDATA[02]	T13		
	MPMCDATA[03]	R13		

Table 2. Interface signals (continued)

Group	Signal Name	Ball	Direction	Function
	MPMCDATA[04]	T14	I/O	DDR / SDRAM data
	MPMCDATA[05]	R14		
	MPMCDATA[06]	T15		
	MPMCDATA[07]	R15		
	MPMCDATA[08]	T17		
	MPMCDATA[09]	P16		
	MPMCDATA[10]	P17		
	MPMCDATA[11]	N15		
	MPMCDATA[12]	N16		
	MPMCDATA[13]	N17		
	MPMCDATA[14]	M16		
	MPMCDATA[15]	M17		
	MPMCADDROUT[00]	R6	Output	DDR / SDRAM address
	MPMCADDROUT[01]	U7		
	MPMCADDROUT[02]	T7		
	MPMCADDROUT[03]	R7		
	MPMCADDROUT[04]	U8		
	MPMCADDROUT[05]	T8		
	MPMCADDROUT[06]	R8		
	MPMCADDROUT[07]	U9		
	MPMCADDROUT[08]	T9		
	MPMCADDROUT[09]	R9		
	MPMCADDROUT[10]	U10		
	MPMCADDROUT[11]	T10		
	MPMCADDROUT[12]	R10		
	MPMCADDROUT[13]	T11		
	MPMCADDROUT[14]	R11		
	nMPMCDYCSOUT[0]	U4	Output	DDR / SDRAM chip select
	nMPMCDYCSOUT[1]	T4		
	nMPMCDYCSOUT[2]	T5		
	nMPMCDYCSOUT[3]	R5		
	MPMCCKEOUT[0]	U11	Output	DDR / SDRAM clock enable
	MPMCCKEOUT[1]	U12		
	MPMCCLKOUT[0]	U16	Output	DDR / SDRAM clock 1
	nMPMCCLKOUT[0]	U15		DDR / SDRAM clock 1 neg.

Table 2. Interface signals (continued)

Group	Signal Name	Ball	Direction	Function
	MPMCCLKOUT[1]	U14		DDR / SDRAM clock 2
	nMPMCCLKOUT[1]	U13		DDR / SDRAM clock 2 neg.
	MPMCDQMOUT[0]	T16	Output	DDR / SDRAM data mask
	MPMCDQMOUT[1]	U17		
	MPMCDQS[0]	R16	Output	DDR data strobe
	MPMCDQS[1]	R17		
	nMPMCCASOUT	T6	Output	DDR / SDRAM strobes
	nMPMCRASOUT	U6		
	nMPMCWEOUT	U5	Output	DDR / SDRAM write enable
RTC	RTCXO	U2	Output	32.768KHx output crystal
	RTCXI	U1	Input	32.768KHz input crystal
SMI	SMINCS[0]	B15	Output	Serial flash chip select
	SMINCS[1]	A17		
	SMINCS[2]	A16		
	SMINCS[3]	A15		
	SMICLK	B16	Output	Serial flash output clock
	SMIDATAIN	B17	Input	Serial flash data in
	SMIDATAOUT	B14	Output	Serial flash data out
UART	UART1_RXD	J17	Input	UART1 RX data
	UART1_TXD	J16	Output	UART1 TX data
USBs	DMNS	R2	I/O	D- port of USB device
	DPLS	R1	I/O	D+ port of USB device
	HOST1_DP	L1	I/O	D+ port of USB host1
	HOST1_DM	L2	I/O	D- port of USB host1
	HOST2_DP	J1	I/O	D+ port of USB host2
	HOST2_DM	J2	I/O	D- port of USB host2
	HOST1_VBUS	F1	Output	USB host1 VBUS signal
	HOST2_VBUS	F2	Output	USB host2 VBUS signal
	OVERCURH1	E1	I/O	USB host1overcurrent
	OVERCURH2	E2	I/O	USB host2 overcurrent
	VBUS	G2	I/O	USB device VBUS signal
	RREF	J6	Input	USB reference resistor

3.2 Power connections

Table 3. Power connections

Group	Signal Name	Ball	Function
Power	vdd3v3	(1)	Digital 3.3V power
	vdd	(2)	Digital 1.2V power
	gnd	(3)	Digital ground
	vdd_dith	P6	DDR / SDR dedicated digital PLL 3.3V power
	vss_dith	P7	DDR / SDR dedicated digital PLL ground
	SSTL_VREF	P15	Voltage reference SSTL / CMOS mode. This pin is used both as logic state and as power supply
	vdd2v5_DDR	(4)	DDR / SDR digital 2.5V / 3.3V power
	vdd1v2_date_osci	T1	1.2V dedicated power for RTC
	vdd_date_osci	U3	1.2V dedicated power for RTC
	gnd_date_osci	T3	Dedicated digital ground for RTC
	gnde_date_osci	T2	Dedicated digital ground for RTC
	anavdd_3v3_pll1600	M3	Dedicated USB PLL analog 3.3V power
	anagnd_3v3_pll1600	M4	Dedicated USB PLL analog ground
	digvdd_1v2_pll1600	N3	Dedicated USB PLL analog 1.2V power
	diggnd_1v2_pll1600	N4	Dedicated USB PLL analog ground
	vddl_1v2_d	P5	Dedicated USB 1.2V power
	vddb_1v2_d	P2	Dedicated USB 1.2V power
	vddc_1v2_d	P1	Dedicated USB 1.2V power
	vdd_usb	M5	Dedicated USB 1.2V power
	vddc_1v2_h1	L4	Dedicated USB 1.2V power
	vddb_1v2_h1	L3	Dedicated USB 1.2V power
	vddl_1v2_h1	K3	Dedicated USB 1.2V power
	vddc_1v2_h0	J5	Dedicated USB 1.2V power
	vddb_1v2_h0	J4	Dedicated USB 1.2V power
	vddl_1v2_h0	H3	Dedicated USB 1.2V power
	vdd3_3v3_d	R3	Dedicated USB 3.3V power
	vdde3v3_usb	M2	Dedicated USB 3.3V power
	vdd3_3v3_h1	K2	Dedicated USB 3.3V power
	vdd3_3v3_h0	H2	Dedicated USB 3.3V power
	vssl_3v3_d	R4	Dedicated USB ground
	vssb_1v2_d	P4	Dedicated USB ground
	vssc_1v2_d	P3	Dedicated USB ground

Table 3. Power connections (continued)

Group	Signal Name	Ball	Function
	gnde_usb	M1	Dedicated USB ground
	gnd_usb	L5	Dedicated USB ground
	vssc_1v2_h1	K5	Dedicated USB ground
	vssb_1v2_h1	K4	Dedicated USB ground
	vssb_1v2_h0	H4	Dedicated USB ground
	vssc_1v2_h0	J3	Dedicated USB ground
	vssl_3v3_h0	H1	Dedicated USB ground
	vssl_3v3_h1	K1	Dedicated USB ground

1. Signal spread on the following balls: H11, J08, J09, J13, J14, K14, M14, N14, P14.
2. Signal spread on the following balls: H10, J07, J12, L14, N05, P09, P13.
3. Signal spread on the following balls: J10, J11, K06 to K13, L06 to L13, M06 to M13, N08 to N13.
4. Signal spread on the following balls: N06, N07, P08, P10 to P12.

3.3 Ballout top view

Figure 1. Ballout top view

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	eASICGP_IO[21]	eASICGP_IO[33]	eASICGP_IO[22]	eASICGP_IO[23]	eASICGP_IO[35]	eASICGP_IO[42]	eASICGP_IO[50]	eASICGP_IO[52]	eASICGP_IO[60]	eASICGP_IO[67]	eASICGP_IO[75]	eASICGP_IO[77]	eASICGP_IO[87]	TEST0	SMINCS[3]	SMINCS[2]	SMINCS[1]	A
B	eASICGP_IO[17]	eASICGP_IO[30]	eASICGP_IO[32]	eASICGP_IO[19]	eASICGP_IO[28]	eASICGP_IO[41]	eASICGP_IO[47]	eASICGP_IO[51]	eASICGP_IO[59]	eASICGP_IO[66]	eASICGP_IO[73]	eASICGP_IO[79]	eASICGP_IO[89]	SMIDATAOUT	SMINCS[0]	SMICLK	SMIDATAIN	B
C	eASICGP_IO[14]	eASICGP_IO[24]	eASICGP_IO[26]	eASICGP_IO[34]	eASICGP_IO[27]	eASICGP_IO[37]	eASICGP_IO[39]	eASICGP_IO[62]	eASICGP_IO[58]	eASICGP_IO[65]	eASICGP_IO[72]	eASICGP_IO[81]	eASICGP_IO[91]	eASICGP_IO[97]	TX_CLK	TXD[0]	TXD[1]	C
D	eASICGP_IO[10]	eASICGP_IO[7]	eASICGP_IO[9]	eASICGP_IO[13]	eASICGP_IO[40]	eASICGP_IO[54]	eASICGP_IO[56]	eASICGP_IO[46]	eASICGP_IO[53]	eASICGP_IO[64]	eASICGP_IO[71]	eASICGP_IO[83]	eASICGP_IO[93]	eASICGP_IO[99]	TXD[2]	TXD[3]	TX_EN	D
E	OVERCURH1	OVERCURH2	eASICGP_IO[8]	eASICGP_IO[5]	eASICGP_IO[15]	eASICGP_IO[18]	eASICGP_IO[48]	eASICGP_IO[44]	eASICGP_IO[45]	eASICGP_IO[63]	eASICGP_IO[70]	eASICGP_IO[85]	eASICGP_IO[95]	eASIC_EXT_CLOCK	CRS	COL	RX_CLK	E
F	HOST1_VBUS	HOST2_VBUS	eASICGP_IO[4]	eASICGP_IO[25]	eASICGP_IO[6]	eASICGP_IO[16]	eASICGP_IO[20]	eASICGP_IO[49]	eASICGP_IO[55]	eASICGP_IO[57]	eASICGP_IO[69]	TDO	TDI	TMS	RXD[0]	RXD[1]	RXD[2]	F
G	PLL_BYPASS	VBUS	MRESET	eASICGP_IO[0]	eASICGP_IO[31]	eASICGP_IO[11]	eASICGP_IO[12]	eASICGP_IO[43]	eASICGP_IO[38]	eASICGP_IO[61]	eASICGP_IO[68]	RTCK	TCK	nTRST	RXD[3]	RX_DV	RX_ER	G
H	vssl_3v3_h0	vdd3_3v3_h0	vddl_1v2_h0	vssb_1v2_h0	eASICGP_IO[3]	eASICGP_IO[2]	eASICGP_IO[1]	eASICGP_IO[29]	eASICGP_IO[36]	vdd	vdd3v3	TEST3	TEST2	TEST1	MDC	MDIO	SDA	H
J	HOST2_DP	HOST2_DM	vssc_1v2_h0	vddb_1v2_h0	vddc_1v2_h0	RREF	vdd	vdd3v3	vdd3v3	gnd	gnd	vdd	vdd3v3	vdd3v3	SCL	UART1_TXD	UART1_RXD	J
K	vssl_3v3_h1	vdd3_3v3_h1	vddl_1v2_h1	vssb_1v2_h1	vssc_1v2_h1	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	vdd3v3	eASIC_PI_CLOCK	GP_IO[5]	GP_IO[4]	K
L	HOST1_DP	HOST1_DM	vddb_1v2_h1	vddc_1v2_h1	gnd_usb	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	vdd	GP_IO[3]	GP_IO[2]	GP_IO[ ]	L
M	gnde_usb	vdde3v3_usb	anavdd_3v3_pll1600	anagnd_3v3_pll1600	vdd_usb	gnd	gnd	gnd	gnd	gnd	gnd	gnd	gnd	vdd3v3	GP_IO[0]	MPMCDATA[14]	MPMCDATA[15]	M
N	MCLK_in	MCLK_out	digvdd_1v2_pll1600	diggnd_1v2_pll1600	vdd	vdd2v5	vdd2v5	gnd	gnd	gnd	gnd	gnd	gnd	vdd3v3	MPMCDATA[11]	MPMCDATA[12]	MPMCDATA[13]	N
P	vddc_1v2_d	vddb_1v2_d	vssc_1v2_d	vssb_1v2_d	vddl_1v2_d	vdd_dith	vss_dith	vdd2v5	vdd	vdd2v5	vdd2v5	vdd2v5	vdd	vdd3v3	SSTL_VREF	MPMCDATA[9]	MPMCDATA[10]	P
R	DPLS	DMNS	vdd3_3v3_d	vssl_3v3_d	nMPMCDYCSOUT[3]	MPMCADDROUT[0]	MPMCADDROUT[3]	MPMCADDROUT[6]	MPMCADDROUT[9]	MPMCADDROUT[12]	MPMCADDROUT[14]	MPMCDATA[1]	MPMCDATA[3]	MPMCDATA[5]	MPMCDATA[7]	MPMCDQS[0]	MPMCDQS[1]	R
T	vdd1v2_date_osci	gnde_date_osci	gnd_date_osci	nMPMCDYCSOUT[1]	nMPMCDYCSOUT[2]	nMPMCCASOUT	MPMCADDROUT[2]	MPMCADDROUT[5]	MPMCADDROUT[8]	MPMCADDROUT[11]	MPMCADDROUT[13]	MPMCDATA[0]	MPMCDATA[2]	MPMCDATA[4]	MPMCDATA[6]	MPMCDQMOUT[0]	MPMCDATA[8]	T
U	RTCXI	RTCXO	vdd_date_osci	nMPMCDYCSOUT[0]	nMPMCWEOUT	nMPMCRASOUT	MPMCADDROUT[1]	MPMCADDROUT[4]	MPMCADDROUT[7]	MPMCADDROUT[10]	MPMCCKEOUT[0]	MPMCCKEOUT[1]	nMPMCCLKOUT[1]	MPMCCLKOUT[1]	nMPMCCLKOUT[0]	MPMCCLKOUT[0]	MPMCDQMOUT[1]	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

4 Package information

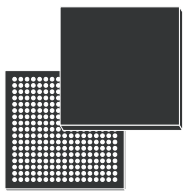
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 2. LFBGA289 mechanical data and package dimensions

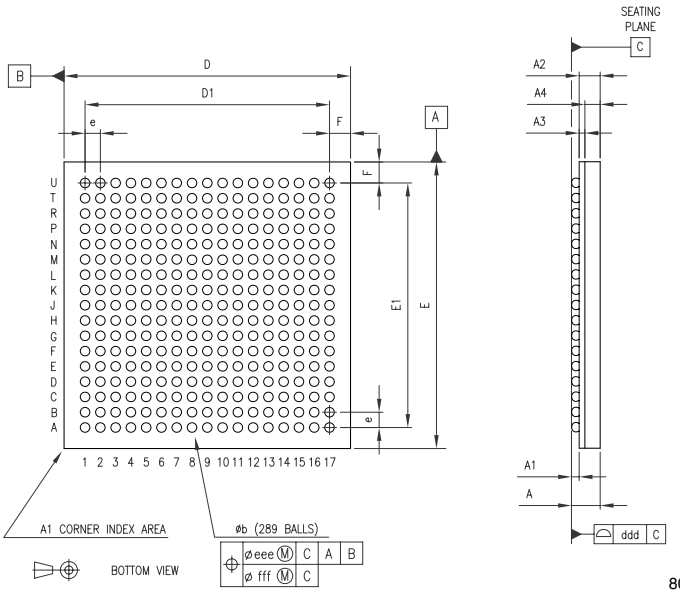
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.700			0.0669
A1	0.270			0.0106		
A2		0.985			0.0387	
A3		0.200			0.0078	
A4			0.800			0.0315
b	0.350	0.400	0.450	0.0137	0.0157	0.0177
D	14.850	15.000	15.150	0.5846	0.5906	0.5965
D1		12.800			0.5039	
E	14.850	15.000	15.150	0.5846	0.5906	0.5965
E1		12.800			0.5039	
e		0.800			0.0315	
F		1.100			0.0433	
ddd			0.120			0.0047
eee			0.150			0.0059
fff			0.080			0.0031

OUTLINE AND MECHANICAL DATA



Body: 15 x 15 x 1.7mm

LFBGA289
Low profile **F**ine Pitch **B**all **G**rid **A**rray



5 Revision history

Table 4. Document revision history

Date	Revision	Changes
31-Jan-2008	1	Initial release.

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