W83627UHG

WINBOND LPC I/O

Date: May/25/2007 Revision: 1.0

W83627UHG Data Sheet Revision History

	PAGES	DATES	VERSION	WEB VERSION	MAIN CONTENTS
1	NA	9/14/2006	0.5	NA	For Customer reference. **(PRELIMINARY)**
2	NA	11/29/2006	0.6	NA	1. Remove the section of AT Interface in Chapter 9 Floppy Disk Controller. 2. Remove sections 8.4 and 8.5 (EXTFDD and EXT2FDD). 3. Remove section 9.6 (OnNow / Security Keyboard and Mouse Wake-Up). 4. Update "$S5_{COLD}$ State" to "S5 State". 5. Update "V_{DD}" to "5VCC" in DC Characteristic. 6. Update the description of CRF0.
3	NA	05/25/2007	1.0	NA	1. Substitute "TControl" with "TBase" 2. Modify the pin descriptions of INDEX#, SOUTF, TRAK0#, WP#, RDATA#, DSKCHG#, HEFRAS, PENKBC, VIN0 ~ VIN2, CPUVCORE, VREF, PLED and PSOUT# 3. Revise the pin name of Pin 52 to PFDCUART 4. Modify the IO type of Pin 90, 92 and 77. 5. Update Figure 7-4 and 7-8 6. Modify section 7.3.1, 7.5, 7.7.2, 7.7.3, 7.7.4 and 18.2 7. Modify Chapter 13 Power Management Event 8. Add section 13.4 PWROK Generation 9. Remove Configuration Register CR[24h], bit 0; CR[26h], bit 7 and Logical Device A, CR[E4h], bit 4 10. Modify Logical Device A, CR[E6h], bit 3 and bit 5; Logical Device C, CR[E5h], bit 0 11. Re-define the strapping function of pin 122.

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1. GENERAL DESCRIPTION

The W83627UHG is a member of Winbond's Super I/O product line. This family features the LPC (Low Pin Count) interface. This interface is more economical than its ISA counterpart because it has approximately forty pins fewer, yet still provides as great performance. In addition, the improvement allows even more efficient operation of software, BIOS and device drivers.

In addition to providing an LPC interface for I/O, the W83627UHG monitors several critical parameters in PC hardware, including power supply voltages, fan speeds, and temperatures. In terms of temperature monitoring, the W83627UHG adopts the Current Mode (dual current source) approach. The W83627UHG also supports the Smart Fan control system, including "SMART FAN™ I and SMART FAN™ III, which makes the system more stable and user-friendly.

The W83627UHG supports four -- 360K, 720K, 1.2M, 1.44M, or 2.88M -- disk drives and data transfer rates of 250 Kb/s, 300 Kb/s, 500 Kb/s, 1 Mb/s, and 2 Mb/s. The disk drive adapter supports the functions of floppy disk drive controller (compatible with the industry standard 82077/ 765), data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, and interrupt and DMA logic. Such a wide range of functions integrated into one W83627UHG greatly reduces the number of required components to interface with floppy disk drives.

The W83627UHG provides six high-speed serial communication ports (UARTs), one of which provides IR functions IrDA 1.0 (SIR for 1.152K bps). Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem-control capability, and a processor interrupt system. All of the UARTs support legacy speeds up to 115.2K bps as well as higher baud rates of 230K, 460K, or 921K bps to support higher speed modems.

The W83627UHG supports the PC-compatible printer port (SPP), the bi-directional printer port (BPP), the enhanced parallel port (EPP) and the extended capabilities port (ECP).

The W83627UHG provides flexible I/O control functions through a set of 45 general purpose I/O (GPIO) ports. These GPIO ports may serve as simple I/O ports or may be individually configured to provide alternative functions.

The W83627UHG supports the SST (Simple Serial Transport) interface and Intel® PECI (Platform Environment Control Interface).

The W83627UHG fully complies with the Microsoft© PC98 and PC99 Hardware Design Guide and meets the requirements of ACPI.

The configuration registers inside the W83627UHG support mode selection, function enable and disable, and power-down selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature in Windows 95/98/2000/XP™, making the allocation of the system resources more efficient than ever.

One special characteristic of the Super I/O product line is the separation of the power supply in normal operation from that in standby operation. Please pay attention to the layout of these two power supplies to avoid short circuits. Otherwise, the feature will not function.

2. FEATURES

General

- Meet LPC Spec. 1.01
- Support LDRQ# (LPC DMA), SERIRQ (Serialized IRQ)
- Integrated hardware monitor functions
- Compliant with Microsoft PC2000/PC2001 Hardware Design Guide
- Support DPM (Device Power Management), ACPI (Advanced Configuration and Power Interface)
- Programmable configuration settings
- Single 24- or 48-MHz clock input

FDC

- Variable write pre-compensation with track-selection capability
- Support vertical recording format
- DMA-enable logic
- 16-byte data FIFOs
- Support floppy disk drives and tape drives
- Detect all overrun and underrun conditions
- Built-in address mark detection circuit to simplify the read electronics
- FDD anti-virus functions with software write protect and FDD-write enable signal (write data signal forced to be inactive)
- Support 3.5-inch or 5.25-inch floppy disk drives
- Compatible with industry standard 82077
- 360K / 720K / 1.2M / 1.44M / 2.88M formats
- 250K, 300K, 500K, 1M, 2M bps data transfer rate
- Support 3-mode FDD and its Windows driver

UART

- Six high-speed, 16550-compatible UARTs with 16-byte send / receive FIFOs
- Fully programmable serial-interface characteristics:
  --- 5, 6, 7 or 8-bit characters
  --- Even, odd or no parity bit generation/detection
  --- 1, 1.5 or 2 stop-bit generation
- Internal diagnostic capabilities:
  --- Loop-back controls for communications link fault isolation
  --- Break, parity, overrun, framing error simulation
- Programmable baud rate generator allows division of clock source by any value from 1 to $(2^{16}-1)$
- Maximum baud rate for clock source 14.769 MHz is up to 921K bps. The baud rate at 24 MHz is 1.5M bps.

Parallel Port

- Compatible with IBM parallel port
- Support PS/2-compatible bi-directional parallel port
- Support Enhanced Parallel Port (EPP) - Compatible with IEEE 1284 specification
- Support Extended Capabilities Port (ECP) - Compatible with IEEE 1284 specification
- Enhanced printer port back-drive current protection

Keyboard Controller

- 8042-based keyboard controller
- Support Phoenix MultiKey/42™ firmware
- Asynchronous Access to two data registers and one status register
- Software-compatible with 8042
- Support PS/2 mouse
- Support port 92
- Support both interrupt and polling modes
- Fast Gate A20 and Hardware Keyboard Reset
- 8-bit timer / counter
- Support binary and BCD arithmetic
- 6, 8, 12, or 16 MHz operating frequency

Hardware Monitor Functions

- Smart Fan control system, supporting the functions of SMART FAN™ I - "Thermal Cruise™" and "Fan Speed Cruise™" modes and SMART FAN™ III functions
- Programmable threshold temperature to speed fan fully while current temperature exceeds this temperature during Thermal Cruise™ mode
- Two thermal inputs from optionally-remote thermistors or thermal diode output
- Support Current Mode (dual current source) temperature sensing method
- Eight voltage inputs (CPUVCORE, VIN[0..2] and 5VCC, AVCC , 5VSB, VBAT)
- Two fan-speed monitoring inputs
- Two fan-speed controls
- Dual mode for fan control (PWM and DC)
- Built-in case open detection circuit
- Programmable hysteresis and setting points for all monitored items
- Over-temperature indicator output
- Issue SMI#, OVT# to activate system protection

- Winbond Hardware Doctor™ Support
- Provide I^2C interface to read / write registers

Infrared

- Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps
- Support SHARP ASK-IR protocol with maximum baud rate up to 57,600 bps

General Purpose I/O Ports

- 45 programmable general purpose I/O ports
- GP25, GP26 and GP27 can distinguish whether the input pins have any transitions by reading the registers and all of the 3 GPIOs also can assert PSOUT# or PME# to wake up the system if each them has any transition.

OnNow Functions

- Keyboard Wake-Up by programmable keys
- Mouse Wake-Up by programmable buttons
- On Now Wake-Up from all of the ACPI sleeping states (S1-S5)

Simple Serial Transport™ Interface

- SST temperature and voltage Combination Sensor command support
- Support SST 0.9 Specification

PECI Interface

- PECI Host
- Support PECI 1.0 Specification
- Support 4 CPU addresses and 2 domains per CPU address

Package

- 128-pin QFP
- Pb-free / RoHS

3. BLOCK DIAGRAM

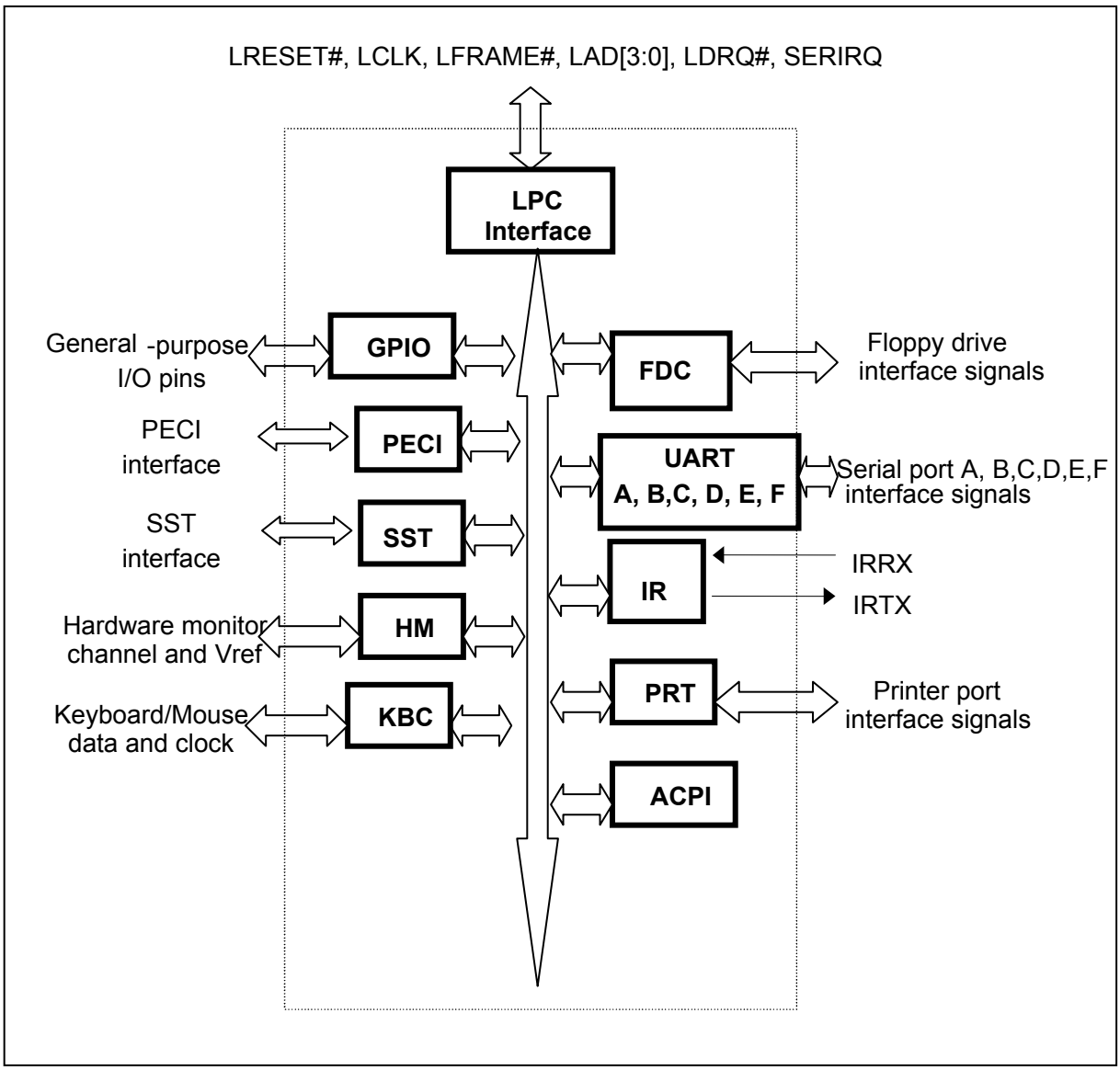


Figure 3-1 W83627UHG Block Diagram

4. PIN LAYOUT

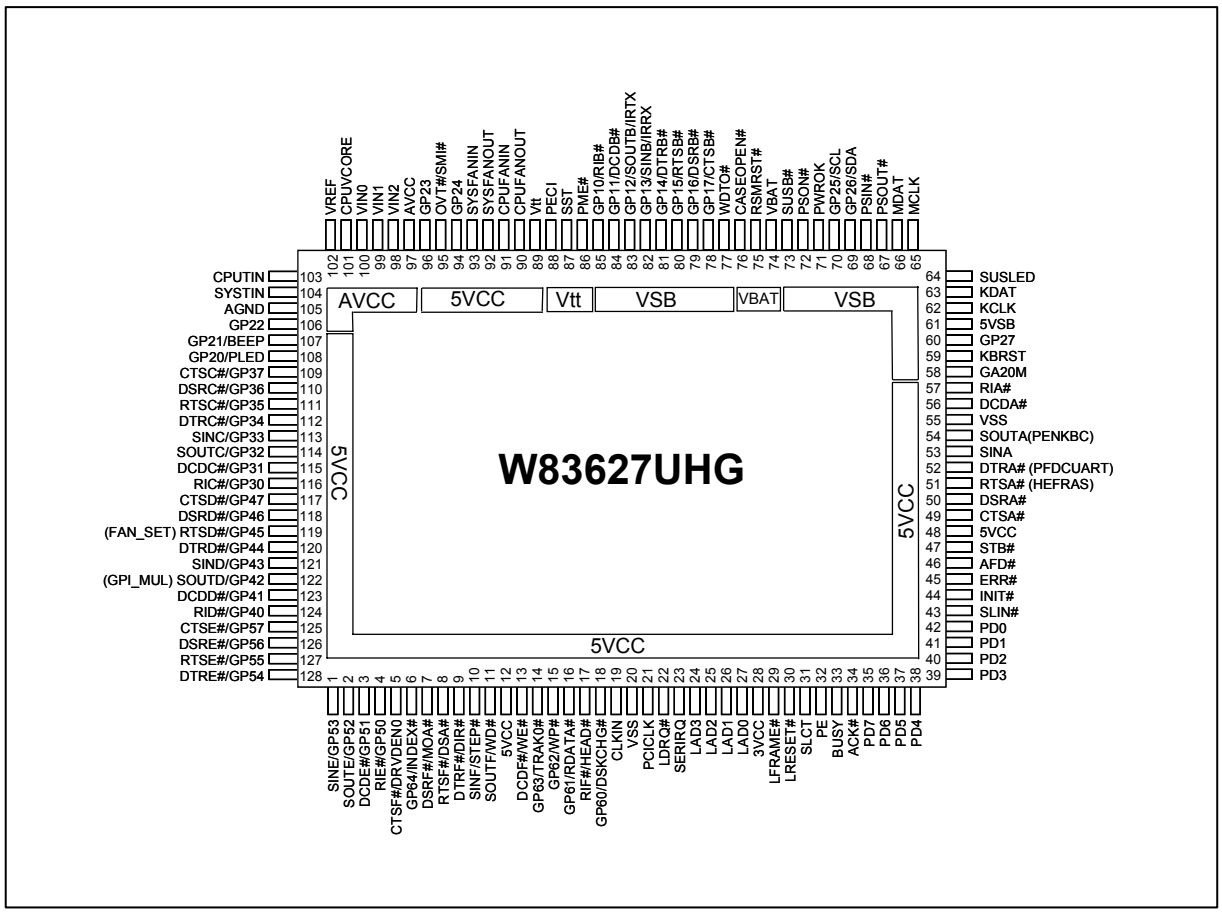


Figure 4-1 W83627UHG Pin Layout

5. PIN DESCRIPTION

Note: Please refer to Section 18.2 DC CHARACTERISTICS for details.

AOUT - Analog output pin
AIN - Analog input pin
I/O_{12tp3} - 3.3-V, TTL-level, bi-directional pin with 12mA source-sink capability
I/O_{12ts} - TTL-level Schmitt-trigger bi-directional pin with 12mA source-sink capability
I/OD_{12t} - TTL-level, bi-directional pin and open-drain output with 12mA sink capability
I/OD_{16ts} - TTL-level Schmitt-trigger bi-directional pin and open-drain output with 16mA sink capability
I/OD_{12ts} - TTL-level Schmitt-trigger bi-directional pin and open-drain output with 12mA sink capability
I/OD_{12tsu} - TTL-level, bi-directional, Schmitt-trigger pin with internal pull-up resistor
. Open-drain output with 12-mA sink capability.
I/O_{v3} - Bi-direction pin with source capability of 6 mA and sink capability of 1 mA
I/O_{v4} - Bi-direction pin with source capability of 6 mA and sink capability of 1 mA
IN_{ts} - TTL-level Schmitt-trigger input pin
IN_{tsu} - TTL-level Schmitt-trigger input pin with internal pull-up resistor
IN_{tsp3} - 3.3-V, TTL-level Schmitt-trigger input pin
IN_{t} - TTL-level input pin
IN_{tu} - TTL-level input pin with internal pull-up resistor
IN_{cd} - CMOS-level input pin with internal pull-down resistor
O_{12p3} - 3.3-V, output pin with 12mA source-sink capability
OD_{12} - Open-drain output pin with 12mA sink capability
OD_{24} - Open-drain output pin with 24mA sink capability
O_{8} - Output pin with 8mA source-sink capability
O_{12} - Output pin with 12mA source-sink capability
O_{24} - Output pin with 24mA source-sink capability

5.1 LPC Interface

SYMBOL	PIN	I/O	DESCRIPTION
CLKIN	19	IN_t	System clock input, either 24MHz or 48MHz. The actual frequency must be specified in register. The default value is 48MHz.
PME#	86	OD_{12}	Generated PME event.
PCICLK	21	IN_{tsp3}	PCI-clock 33-MHz input.
LDRQ#	22	O_{12p3}	Encoded DMA Request signal.
SERIRQ	23	I/O_{12tp3}	Serialized IRQ input / output.
LAD[3:0]	24-27	I/O_{12tp3}	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
LFRAME#	29	IN_{tsp3}	Indicates the start of a new cycle or the termination of a broken cycle.
LRESET#	30	IN_{tsp3}	Reset signal. It can be connected to the PCIRST# signal on the host.

5.2 FDC Interface

SYMBOL	PIN	I/O	DESCRIPTION
DRVDEN0	5	OD_{24}	Drive Density Select bit 0.
CTSF#		IN_t	Clear To Send. It is the modem control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
INDEX#	6	IN_{tsu}	This Schmitt-trigger input from the disk drive is active-low when the head is positioned over the beginning of a track marked by an index hole. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility.
GP64		I/OD_{12ts}	General purpose I/O port 6 bit 4.
MOA#	7	OD_{24}	Motor A On. When set to 0, this pin enables disk drive A. This is an open-drain output.
DSRF#		IN_t	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
DSA#	8	OD_{24}	Drive Select A. When set to 0, this pin enables disk drive A. This is an open-drain output.
RTSF#		O_{24}	UART F Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.

FDC Interface, continued

SYMBOL	PIN	I/O	DESCRIPTION
DIR#	9	OD_{24}	Direction of the head step motor. An open-drain output. Logic 1 = outward motion Logic 0 = inward motion
DTRF#		O_{24}	UART F Data Terminal Ready. An active low signal informs the modem or data set that the controller is ready to communicate.
STEP#	10	OD_{24}	Step output pulses. This active-low open-drain output produces a pulse to move the head to another track.
SINF		IN_t	Serial Input. This pin is used to receive serial data through the communication link.
WD#	11	OD_{24}	Write data. This logic-low open-drain writes pre-compensation serial data to the selected FDD. An open-drain output.
SOUTF		O_{24}	UART F Serial Output. This pin is used to transmit serial data out to the communication link.
WE#	13	OD_{24}	Write enable. An open-drain output.
DCDF#		IN_t	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
TRAK0#	14	IN_{tsu}	Track 0. This Schmitt-trigger input from the disk drive is active-low when the head is positioned over the outermost track. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility.
GP63		I/OD_{12ts}	General purpose I/O port 6 bit 3.
WP#	15	IN_{tsu}	Write Protected. This active-low Schmitt input from the disk drive indicates that the diskette is write-protected. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility.
GP62		I/OD_{12ts}	General purpose I/O port 6 bit 2.
RDATA#	16	IN_{tsu}	The read-data input signal from the FDD. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility.
GP61		I/OD_{12ts}	General purpose I/O port 6 bit 1.

FDC Interface, continued

SYMBOL	PIN	I/O	DESCRIPTION
HEAD#	17	OD_{24}	Head Select. This open-drain output determines which disk drive head is active. Logic 1 = side 0 Logic 0 = side 1
RIF#		IN_t	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
DSKCHG#	18	IN_{tsu}	Diskette Change. This signal is active-low at power-on and whenever the diskette is removed. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility.
GP60		I/OD_{12ts}	General purpose I/O port 6 bit 0.

5.3 Multi-Mode Parallel Port

SYMBOL	PIN	I/O	DESCRIPTION
SLCT	31	IN_{ts}	PRINTER MODE: An active-high input on this pin indicates that the printer is selected. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
PE	32	IN_{ts}	PRINTER MODE: An active-high input on this pin indicates that the printer has detected the end of the paper. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
BUSY	33	IN_{ts}	PRINTER MODE: An active-high input indicates that the printer is not ready to receive data. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
ACK#	34	IN_{ts}	PRINTER MODE: ACK# An active-low input on this pin indicates that the printer has received data and is ready to accept more data. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
ERR#	45	IN_{ts}	PRINTER MODE: ERR# An active-low input on this pin indicates that the printer has encountered an error. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
SLIN#	43	OD_{12}	PRINTER MODE: SLIN# Output line for detection of printer selection. See the description of the parallel port for the definition of this pin in ECP and EPP modes.

Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	DESCRIPTION
INIT#	44	OD_{12}	PRINTER MODE: INIT# Output line for the printer initialization. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
AFD#	46	OD_{12}	PRINTER MODE: AFD# An active-low output from this pin causes the printer to auto feed a line after a line is printed. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
STB#	47	OD_{12}	PRINTER MODE: STB# An active-low output is used to latch the parallel data into the printer. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
PD0	42	I/O_{12ts}	PRINTER MODE: PD0 Parallel port data bus bit 0. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
PD1	41	I/O_{12ts}	PRINTER MODE: PD1 Parallel port data bus bit 1. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
PD2	40	I/O_{12ts}	PRINTER MODE: PD2 Parallel port data bus bit 2. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
PD3	39	I/O_{12ts}	PRINTER MODE: PD3 Parallel port data bus bit 3. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
PD4	38	I/O_{12ts}	PRINTER MODE: PD4 Parallel port data bus bit 4. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
PD5	37	I/O_{12ts}	PRINTER MODE: PD5 Parallel port data bus bit 5. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
PD6	36	I/O_{12ts}	PRINTER MODE: PD6 Parallel port data bus bit 6. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
PD7	35	I/O_{12ts}	PRINTER MODE: PD7 Parallel port data bus bit 7. See the description of the parallel port for the definition of this pin in ECP and EPP modes.

5.4 Serial Port & Infrared Port Interface

SYMBOL	PIN	I/O	DESCRIPTION
CTSA#	49	IN_t	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
CTSB#	78	IN_t	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
GP17		I/OD_{12t}	General-purpose I/O port 1 bit 7.
CTSC#	109	IN_t	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
GP37		I/OD_{12t}	General-purpose I/O port 3 bit 7.
CTSD#	117	IN_t	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
GP47		I/OD_{12t}	General-purpose I/O port 4 bit 7.
CTSE#	125	IN_t	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
GP57		I/OD_{12t}	General-purpose I/O port 5 bit 7.
CTSF#	5	IN_t	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
DRVDEN0		OD_{24}	Drive Density Select bit 0.
DSRA#	50	IN_t	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
DSRB#	79	IN_t	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
GP16		I/OD_{12t}	General-purpose I/O port 1 bit 6.
DSRC#	110	IN_t	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
GP36		I/OD_{12t}	General-purpose I/O port 3 bit 6.
DSRD#	118	IN_t	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
GP46		I/OD_{12t}	General-purpose I/O port 4 bit 6.

Serial Port & Infrared Port Interface, continued

SYMBOL	PIN	I/O	DESCRIPTION
DSRE#	126	IN_t	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
GP56		I/OD_{12t}	General-purpose I/O port 5 bit 6.
DSRF#	7	IN_t	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
MOA#		OD_{24}	Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output.
RTSA#	51	O_8	UART A Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
HEFRAS		IN_{cd}	During power-on reset, this pin is pulled down internally and is defined as HEFRAS, which provides the power-on value for CR26 bit 6 (HEFRAS). The PCB layout should reserve space for a 1-kΩ resistor to pull down this pin so as to ensure the selection of I/O port's configuration address to 2EH, and a 1-kΩ resistor is recommended to pull it up if 4EH is selected as I/O port's configuration address.
RTSB#	80	O_8	UART B Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
GP15		I/OD_8	General-purpose I/O port 1 bit 5.
RTSC#	111	O_8	UART C Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
GP35		I/OD_8	General-purpose I/O port 3 bit 5.
RTSD#	119	O_8	UART D Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
FAN_SET		IN_{cd}	Determines the initial FAN speed. Power-on configuration for 2 fan speeds, 50% or 100%. During power-on reset, this pin needs a pulled-up or a pull-down resistor to decide whether the fan speed is 50% or 100%.
GP45		I/OD_8	General-purpose I/O port 4 bit 5.
RTSE#	127	O_{12}	UART E Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
GP55		I/OD_{12t}	General-purpose I/O port 5 bit 5.
RTSF	8	O_{24}	UART F Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
DSA#		OD_{24}	Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output.

Serial Port & Infrared Port Interface, continued

SYMBOL	PIN	I/O	DESCRIPTION
DTRA#	52	O_8	UART A Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
PFDCUART		IN_{cd}	During power-on reset, this pin is pulled down internally and is defined as FDC enable, which provides the power-on value for CR24 bit 1. A 1 kΩ is reserved to pull down and a 1 kΩ resistor is recommended if intends to pull-up to enable UART F.
DTRB#	81	O_8	UART B Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
GP14		I/OD_{12t}	General-purpose I/O port 1 bit 4.
DTRC#	112	O_8	UART C Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
GP34		I/OD_{12t}	General-purpose I/O port 3 bit 4.
DTRD#	120	O_8	UART D Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
GP44		I/OD_{8t}	General-purpose I/O port 4 bit 4.
DTRE#	128	O_8	UART E Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
GP54		I/OD_{12t}	General-purpose I/O port 5 bit 4.
DTRF#	9	O_{24}	UART F Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
DIR#		OD_{24}	Direction of the head step motor. An open drain output. Logic 1 = outward motion Logic 0 = inward motion
SINA	53	IN_t	Serial Input. This pin is used to receive serial data through the communication link.
SINB	82	IN_t	Serial Input. This pin is used to receive serial data through the communication link.
IRRX			IR Receiver input.
GP13		I/OD_{12t}	General-purpose I/O port 1 bit 3.
SINC	113	IN_t	Serial Input. This pin is used to receive serial data through the communication link.
GP33		I/OD_{12t}	General-purpose I/O port 3 bit 3.
SIND	121	IN_t	Serial Input. This pin is used to receive serial data through the communication link.
GP43		I/OD_{12t}	General-purpose I/O port 4 bit 3.

Serial Port & Infrared Port Interface, continued

SYMBOL	PIN	I/O	DESCRIPTION
SINE	1	IN_t	Serial Input. This pin is used to receive serial data through the communication link.
GP53		I/OD_{12t}	General-purpose I/O port 5 bit 3.
SINF	10	IN_t	Serial Input. This pin is used to receive serial data through the communication link.
STEP#		OD_{24}	Step output pulses. This active low open drain output produces a pulse to move the head to another track.
SOUTA	54	O_8	UART A Serial Output. This pin is used to transmit serial data out to the communication link.
PENKBC		IN_{cd}	During power on reset, this pin is pulled down internally and is defined as PENKBC, and the power-on values are shown at CR24 bit 2. The PCB layout should reserve space for a 1-kΩ resistor to pull down this pin to ensure the disabling of KBC, and a 1-kΩ resistor is recommended to pull the pin up If wish to enable KBC.
SOUTB	83	O_8	UART B Serial Output. This pin is used to transmit serial data out to the communication link.
IRTX			IR Transmitter output.
GP12		I/OD_8	General-purpose I/O port 1 bit 2.
SOUTC	114	O_8	UART C Serial Output. This pin is used to transmit serial data out to the communication link.
GP32		I/OD_8	General-purpose I/O port 3 bit 2.
SOUTD	122	O_8	UART D Serial Output. This pin is used to transmit serial data out to the communication link.
GPI_MUL		IN_{cd}	Determines PIN 107 and 108 multi-function select. During power-on reset, this pin is pulled down internally and is defined as BEEP function and power LED enable. A 1 kΩ is reserved to pull down and a 1 kΩ resistor is recommended if intending to pull up to enable GPIO output.
GP42		I/OD_8	General-purpose I/O port 4 bit 2.
SOUTE	2	O_8	UART E Serial Output. This pin is used to transmit serial data out to the communication link.
GP52		I/OD_8	General-purpose I/O port 5 bit 2.
SOUTF	11	O_{24}	UART F Serial Output. This pin is used to transmit serial data out to the communication link.
WD#		OD_{24}	Write data. This logic low open drain writes pre-compensation serial data to the selected FDD. An open drain output.

Serial Port & Infrared Port Interface, continued

SYMBOL	PIN	I/O	DESCRIPTION
DCDA#	56	IN_t	Data Carrier Detect. An active-low signal indicates the modem or data set has detected a data carrier.
DCDB#	84	IN_t	Data Carrier Detect. An active-low signal indicates the modem or data set has detected a data carrier.
GP11		I/OD_{12t}	General-purpose I/O port 1 bit 1.
DCDC#	115	IN_t	Data Carrier Detect. An active-low signal indicates the modem or data set has detected a data carrier.
GP31		I/OD_{12t}	General-purpose I/O port 3 bit 1.
DCDD#	123	IN_t	Data Carrier Detect. An active-low signal indicates the modem or data set has detected a data carrier.
GP41		I/OD_{12t}	General-purpose I/O port 4 bit 1.
DCDE#	3	IN_t	Data Carrier Detect. An active-low signal indicates the modem or data set has detected a data carrier.
GP51		I/OD_{12t}	General-purpose I/O port 5 bit 1.
DCDF#	13	IN_t	Data Carrier Detect. An active-low signal indicates the modem or data set has detected a data carrier.
WE#		OD_{24}	Write enable. An open drain output.
RIA#	57	IN_t	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or data set.
RIB#	85	IN_t	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or data set.
GP10		I/OD_{12t}	General-purpose I/O port 1 bit 0.
RIC#	116	IN_t	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or data set.
GP30		I/OD_{12t}	General-purpose I/O port 3 bit 0.
RID#	124	IN_t	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or data set.
GP40		I/OD_{12t}	General-purpose I/O port 4 bit 0.
RIE#	4	IN_t	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or data set.
GP50		I/OD_{12t}	General-purpose I/O port 5 bit 0.
RIF#	17	IN_t	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or data set.
HEAD#		OD_{24}	Head select. This open drain output determines which disk drive head is active. Logic 1 = side 0 Logic 0 = side 1

5.5 KBC Interface

SYMBOL	PIN	I/O	DESCRIPTION
GA20M	58	O_{12}	Gate A20 output. This pin is high after system reset. (KBC P21)
KBRST	59	O_{12}	Keyboard reset. This pin is high after system reset. (KBC P20)
KCLK	62	I/OD_{16ts}	Keyboard Clock.
KDAT	63	I/OD_{16ts}	Keyboard Data.
MCLK	65	I/OD_{16ts}	PS2 Mouse Clock.
MDAT	66	I/OD_{16ts}	PS2 Mouse Data.

5.6 Hardware Monitor Interface

SYMBOL	PIN	I/O	DESCRIPTION
BEEP	107	OD_{12}	Beep function for hardware monitor. This pin is low after system reset.
GP21		I/OD_{12t}	General-purpose I/O port 2 bit 1.
CASEOPEN#	76	IN_t	CASE OPEN Detection. An active-low input from an external device when the case is open. This signal can be latched if pin VBAT is connected to the battery, even if the W83627UHG is turned off. Pull up a 2-MΩ resistor to VBAT is recommended if useless.
VIN2	98	AIN	Analog Inputs for voltage measurement (Range: 0 to 2.048 V)
VIN1	99	AIN	Analog Inputs for voltage measurement (Range: 0 to 2.048 V).
VIN0	100	AIN	Analog Inputs for voltage measurement (Range: 0 to 2.048 V)
CPUVCORE	101	AIN	Analog Inputs for voltage measurement (Range: 0 to 2.048 V)
VREF	102	AOUT	Reference Voltage (2.048 V)
CPUTIN	103	AIN	Temperature sensor 2 input. It is used for CPU temperature sensing.
SYSTIN	104	AIN	Temperature sensor 1 input. It is used for system temperature sensing.
OVT#	95	OD_{12}	Over temperature Shutdown Output. This pin indicates the temperature is over the temperature limit. (Default after LRESET#)
SMI#			System Management Interrupt channel output.
CPUFANIN SYSFANIN	91 93	I/O_{12ts}	0 to +5 V amplitude fan tachometer input.

Hardware Monitor Interface, continued

SYMBOL	PIN	I/O	DESCRIPTION
CPUFANOUT SYSFANOUT	90 92	O_{12} OD_{12} AOUT	DC/PWM fan output control. CPUFANOUT and SYSFANOUT are default PWM mode.
PLED	108	OD_{12}	Power LED output. This pin is tri-stated as default.
GP20		I/OD_{12t}	General-purpose I/O port 2 bit 0.

5.7 PECI Interface

SYMBOL	PIN	I/O	DESCRIPTION
PECI	88	I/O_{V3}	INTEL® CPU PECI interface. Connect to CPU.
Vtt	89	Power	INTEL® CPU Vtt Power.

5.8 SST Interface

SYMBOL	PIN	I/O	DESCRIPTION
SST	87	I/O_{V4}	Simple Serial Transport (SST) Interface.

5.9 Advanced Configuration and Power Interface

SYMBOL	PIN	I/O	DESCRIPTION
PSIN#	68	IN_{tu}	Panel Switch Input. This pin is active-low.
PSOUT#	67	OD_{12}	Panel Switch Output. This signal is used to wake-up the system from S3/S5 state.
RSMRST#	75	OD_{12}	Resume reset signal output.
SUSB#	73	IN_t	System S3 state input.
PSON#	72	OD_{12}	Power Supply on-off Output.
PWROK	71	OD_{12}	This pin generates the PWROK signal while 5VCC comes in.
SCL	70	IN_{ts}	Serial Bus clock.
GP25		I/OD_{12ts}	General-purpose I/O port 2 bit 5.
SDA	69	I/OD_{12t}	Serial bus bi-directional Data.
GP26		I/OD_{12t}	General-purpose I/O port 2 bit 6.

5.10 General Purpose I/O Port

5.10.1 GPIO Power Source

SYMBOL	POWER SOURCE
GPIO port 1	5VSB
GPIO port 2	5VSB
GPIO port 3	5VCC
GPIO port 4	5VCC
GPIO port 5	5VCC
GPIO port 6 (Bit 0-4)	5VCC

5.10.2 GPIO-1 Interface

See 5.4 Serial Port & Infrared Port Interface

5.10.3 GPIO-2 Interface

SYMBOL	PIN	I/O	DESCRIPTION
GP20	108	I/OD_{12t}	General-purpose I/O port 2 bit 0.
PLED		OD_{12}	Power LED output. This pin is tri-stated as default..
GP21	107	I/OD_{12t}	General-purpose I/O port 2 bit 1.
BEEP		OD_{12}	Beep function for hardware monitor. This pin is low after system reset.
GP22	106	I/OD_{12t}	General-purpose I/O port 2 bit 2.
GP23	96	I/OD_{12t}	General-purpose I/O port 2 bit 3.
GP24	94	I/OD_{12t}	General-purpose I/O port 2 bit 4.
GP25	70	I/OD_{12ts}	General-purpose I/O port 2 bit 5.
SCL		IN_{ts}	Serial Bus clock.
GP26	69	I/OD_{12t}	General-purpose I/O port 2 bit 6.
SDA		I/OD_{12t}	Serial bus bi-directional data.
GP27	58	I/OD_{12t}	General-purpose I/O port 2 bit 7.

5.10.4 GPIO-3 Interface

See 5.4 Serial Port & Infrared Port Interface

5.10.5 GPIO-4 Interface

See 5.4 Serial Port & Infrared Port Interface

5.10.6 GPIO-5 Interface

See 5.4 Serial Port & Infrared Port Interface

5.10.7 GPIO-6 Interface

See 5.2 FDC Interface

5.10.8 WDTO# and SUSLED Pins

SYMBOL	PIN	I/O	DESCRIPTION
WDTO#	77	OD_{12}	Watchdog timer output signal.
SUSLED	64	OD_{12}	Suspend-LED output signal. This pin is low as default.

5.11 POWER PINS

SYMBOL	PIN	DESCRIPTION
5VSB	61	+5 V stand-by power supply for the digital circuit.
VBAT	74	+3 V on-board battery for the digital circuit.
5VCC	12,48	+5 V power supply for the digital circuit.
3VCC	28	+3.3V power supply for driving 3V on the host interface.
AVCC	97	Analog +5 V power input. Internally supply to all analog circuits.
AGND	105	Analog ground. The ground reference for all analog input. Internally connected to all analog circuits.
VSS	20,55	Ground.
Vtt	89	INTEL® CPU Vtt power.

6. CONFIGURATION REGISTER ACCESS PROTOCOL

The W83627UHG uses Super I/O protocol to access configuration registers to set up different types of configurations. The W83627UHG has totally fifteen Logical Devices (from Logical Device 0 to Logical Device F with the exception of Logical Device 4 for backward compatibility) corresponding to fifteen individual functions: FDC (Logical Device 0), Parallel Port (Logical Device 1), UARTA (Logical Device 2), UARTB (Logical Device 3), Keyboard Controller (Logical Device 5), UARTC (Logical Device 6), GPIO3, 4 (Logical Device 7), WDTO# & PLED and GPIO5, 6 (Logical Device 8), GPIO1, 2 and SUSLED (Logical Device 9), ACPI (Logical Device A), Hardware Monitor (Logical Device B), PECI & SST (Logical Device C), UARTD (Logical Device D), UARTE(Logical Device E), and UARTF (Logical Device F). Each Logical Device has its own configuration registers (above CR30). The host can access those registers by writing an appropriate Logical Device Number into the Logical Device select register at CR7.

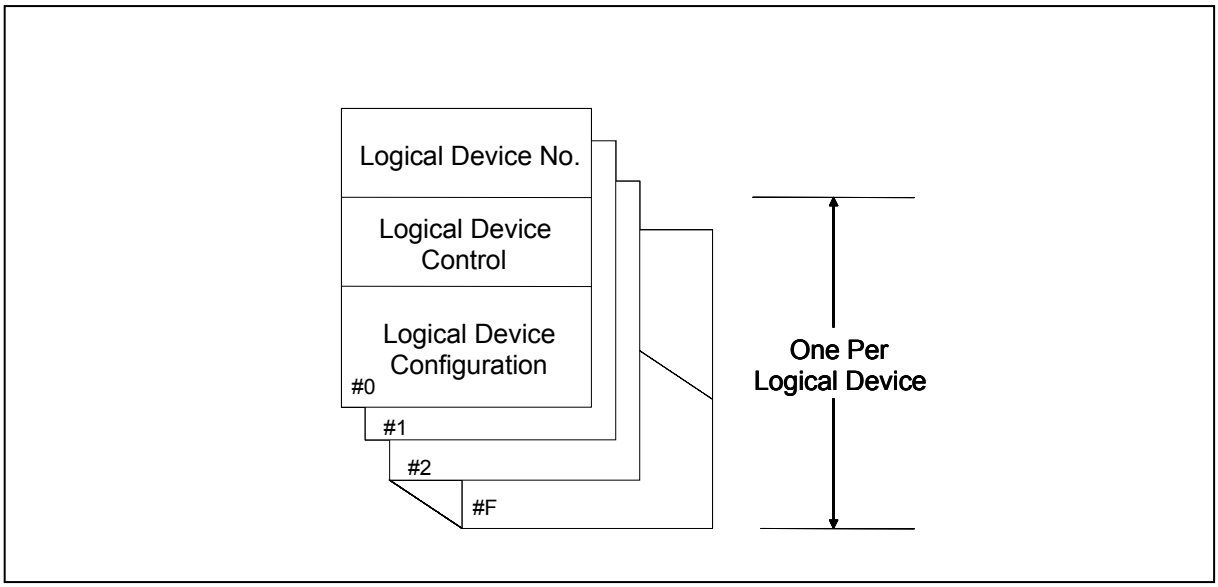


Figure 6-1 Structure of the Configuration Register

Table 6-1 Devices of I/O Base Address

LOGICAL DEVICE NUMBER	FUNCTION	I/O BASE ADDRESS	DEFAULT VALUE
0	FDC	100h ~ FF8h	3F0h
1	Parallel Port	100h ~ FF8h	378h
2	UART A	100h ~ FF8h	3F8h
3	UART B	100h ~ FF8h	2F8h
4	Reserved		
5	Keyboard Controller	100h ~ FF8h	60h/64h
6	UART C	100h ~ FF8h	3E0h
7	GPIO 3, 4	100h ~ FF8h	-
8	WDTO# & PLED, and GPIO 5, 6	Reserved	-
9	GPIO 1, 2	Reserved	-
A	ACPI	Reserved	-
B	Hardware Monitor	100h ~ FF8h	-
C	PECI & SST	Reserved	-
D	UART C	100h ~ FF8h	2E0h
E	UART D	100h ~ FF8h	3E8h
F	UART E	100h ~ FF8h	2E8h

6.1 Configuration Sequence

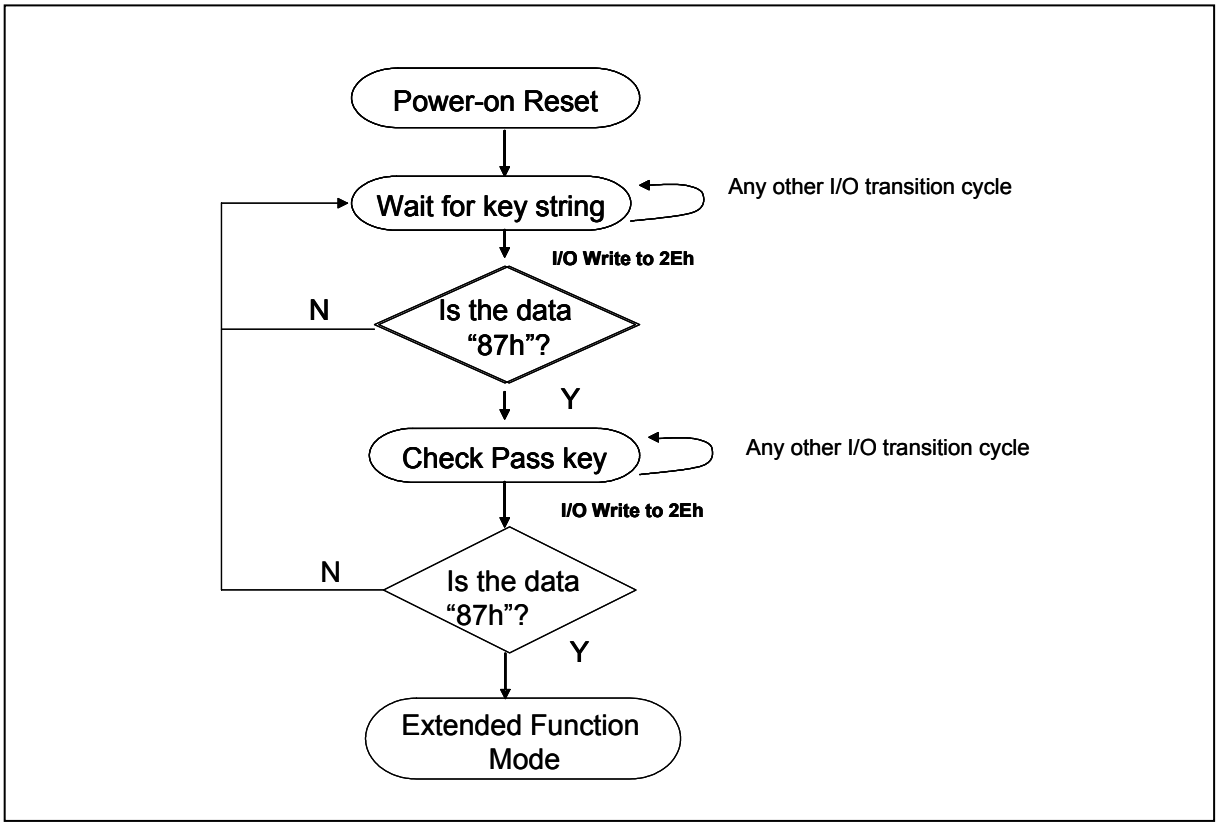


Figure 6-2 Configuration Register

To program the W83627UHG configuration registers, the following configuration procedures must be followed in sequence:

(1). Enter the Extended Function Mode.

(2). Configure the configuration registers.

(3). Exit the Extended Function Mode.

6.1.1 Enter the Extended Function Mode

To place the chip into the Extended Function Mode, two successive writes of 0x87 must be applied to Extended Function Enable Registers (EFERs, i.e. 2Eh or 4Eh).

6.1.2 Configure the Configuration Registers

The chip selects the Logical Device and activates the desired Logical Devices through Extended Function Index Register (EFIR) and Extended Function Data Register (EFDR). The EFIR is located at the same address as the EFER, and the EFDR is located at address (EFIR+1).

First, write the Logical Device Number (i.e. 0x07) to the EFIR and then write the number of the desired Logical Device to the EFDR. If accessing the Chip (Global) Control Registers, this step is not required.

Secondly, write the address of the desired configuration register within the Logical Device to the EFIR and then write (or read) the desired configuration register through the EFDR.

6.1.3 Exit the Extended Function Mode

To exit the Extended Function Mode, writing 0xAA to the EFER is required. Once the chip exits the Extended Function Mode, it is in the normal running mode and is ready to enter the configuration mode.

6.1.4 Software Programming Example

The following example is written in Intel 8086 assembly language. It assumes that the EFER is located at 2Eh, so the EFIR is located at 2Eh and the EFDR is located at 2Fh. If the HEFRAS (CR26 bit 6) is set, 2Eh can be directly replaced by 4Eh and 2Fh replaced by 4Fh.

```
;-----------------------------------------------------
; Enter the Extended Function Mode
;-----------------------------------------------------
MOV     DX, 2EH
MOV     AL, 87H
OUT     DX, AL
OUT     DX, AL
;--------------------------------------------------------------------------
; Configure Logical Device 1, Configuration Register CRF0
;--------------------------------------------------------------------------
MOV     DX, 2EH
MOV     AL, 07H
OUT     DX, AL          ; point to Logical Device Number Reg.
MOV     DX, 2FH
MOV     AL, 01H
OUT     DX, AL          ; select Logical Device 1
;
MOV     DX, 2EH
MOV     AL, F0H
OUT     DX, AL          ; select CRF0
MOV     DX, 2FH
MOV     AL, 3CH
OUT     DX, AL          ; update CRF0 with value 3CH
```

```
;----------------------------------------
; Exit the Extended Function Mode
;----------------------------------------
MOV     DX, 2EH
MOV     AL, AAH
OUT     DX, AL
```

Table 6-2 Chip (Global) Control Registers

INDEX	R/W	DEFAULT VALUE	DESCRIPTION
02h	Write Only		Software Reset
07h	R/W	00h	Logical Device
20h	Read Only	A2h	Chip ID, MSB
21h	Read Only	3xh	Chip ID, LSB
22h	R/W	FFh	Device Power Down
23h	R/W	F0h	Device Power Down
24h	R/W	0100_0ss0b	Global Option
25h	R/W	00h	Interface Tri-state Enable
26h	R/W	0s000000b	Global Option
27h	Reserved		
28h	R/W	00h	Global Option
29h	R/W	00h	Multi-function Pin Selection
2Ah	R/W	00h	I^2C Pin Select
2Bh	Reserved		
2Ch	R/W	02h	Multi-function Pin Selection
2Dh	R/W	00h	GPIO2 Input Detected Type
2Eh	R/W	00h	Reserved
2Fh	R/W	00h	Reserved

S: Strapping; x: chip version.

7. HARDWARE MONITOR

7.1 General Description

The W83627UHG monitors several critical parameters in PC hardware, including power supply voltages, fan speeds, and temperatures, all of which are very important for a high-end computer system to work stably and properly. In addition, proprietary hardware reduces the amount of programming and processor intervention to control cooling fan speeds, minimizing ambient noise and maximizing system temperature and reliability.

The W83627UHG can simultaneously monitor all of the following inputs:

- Eight analog voltage inputs (four internal voltages VBAT, 5VSB, 5VCC and AVCC power; four external voltage inputs)
- Two fan tachometer inputs
- Two remote temperatures, using either a thermistor or the CPU thermal diode (voltage or current mode measurement method)
- One case-open detection signal.

These inputs are converted to digital values using the integrated, eight-bit analog-to-digital converter (ADC).

In response to these inputs, the W83627UHG can generate the following outputs:

- Two PWM (pulse width modulation) or DC fan outputs for the fan speed control
- Beep tone output for warnings
- SMI#
- OVT# signals for system protection events

The W83627UHG provides hardware access to all monitored parameters through the LPC or I^2C interface and software access through application software, such as Winbond's Hardware Doctor™, or BIOS. In addition, the W83627UHG can generate pop-up warnings or beep tones when a parameter goes outside of a user-specified range.

The rest of this section introduces the various features of the W83627UHG hardware-monitor capability. These features are divided into the following sections:

- Access Interfaces
- Analog Inputs
- Fan Speed Measurement and Control
- Smart Fan Control
- SMI# Interrupt Mode
- OVT# Interrupt Mode
- Registers and Value RAM

7.2 Access Interfaces

The W83627UHG provides two interfaces, LPC and I^2C, for the microprocessor to read or write the internal registers of the hardware monitor.

7.2.1 LPC Interface

The internal registers of the hardware monitor block are accessible through two separate methods on the LPC bus. The first set of registers, which primarily enables the block and sets its address in the CPU I/O address space are accessed by the Super I/O protocol described in Chapter 6 at address 2Eh/2Fh or 4Eh/4Fh. The bulk of the functionality and internal registers of this block are accessed from an index/data pair of CPU I/O addresses. The standard locations are usually 295h/296h and are set by CR60 and CR61 accessed using the Super I/O protocol as described in Chapter 6.

Due to the number of internal registers, it is necessary to separate the register sets into “banks” specified by register 4Eh. The structure of the internal registers is shown in the following figure.

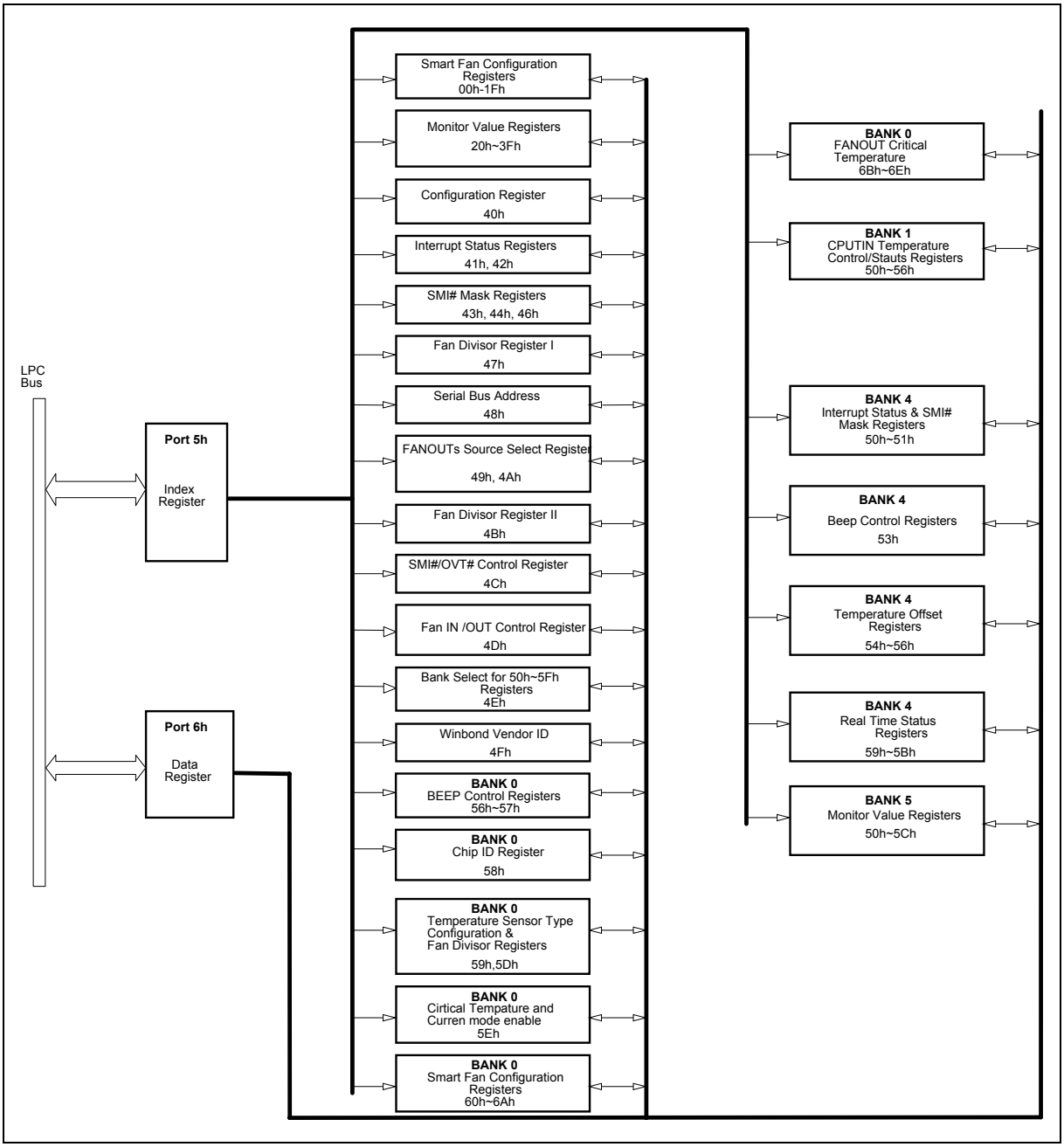


Figure 7-1 LPC Bus' Reads from / Writes to Internal Registers

7.2.2 I²C Interface

The I²C interface is a second, parallel port into the internal registers of the hardware monitor function block. The interface is totally compatible with the industry-standard I²C specification, allowing external components that are also compatible to read the internal registers of the W83627UHG hardware monitor and control fan speeds. The address of the I²C peripheral is set by the register located at index 48h (which is accessed by the index/data pair at I/O address typically at 295h/296h).

The two timing diagrams below illustrate how to use the I²C interface to write to an internal register and how to read the value in an internal register, respectively.

(a) Serial bus write to internal address register followed by the data byte

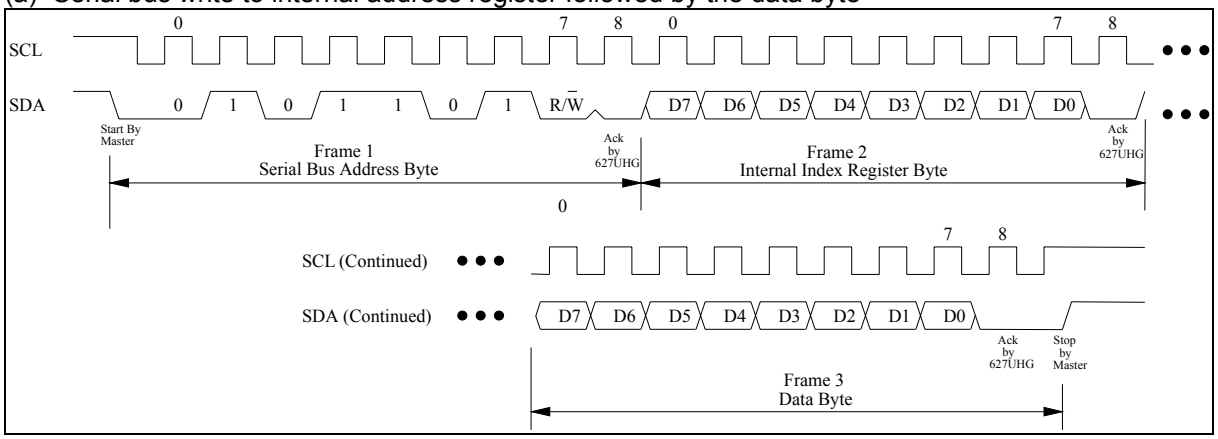


Figure 7-2 Serial Bus Write to Internal Address Register Followed by the Data Byte

(b) Serial bus read from a register

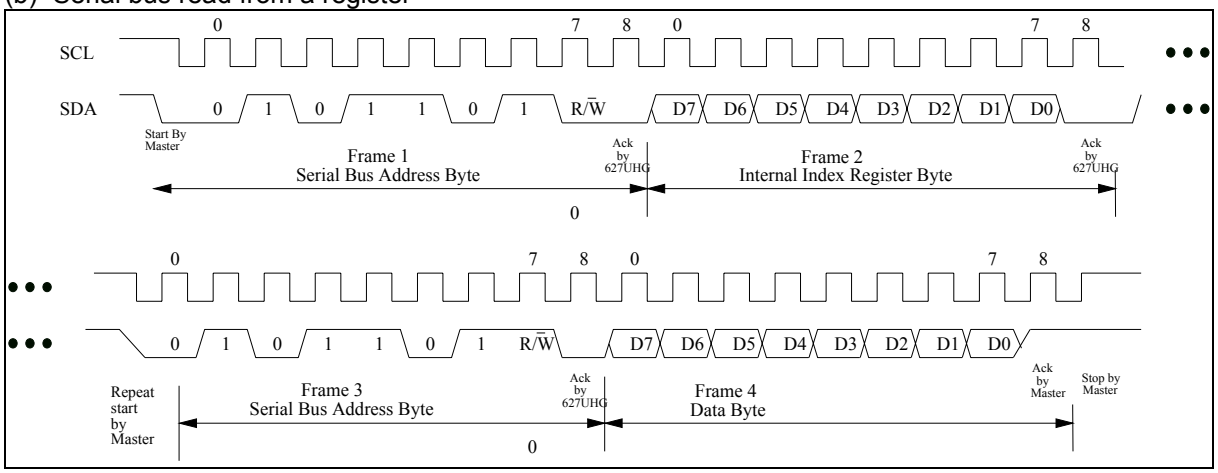


Figure 7-3 Serial Bus Read from Internal Address Register

7.3 Analog Inputs

The eight analog inputs of the hardware monitor block connect to an 8-bit Analog to Digital Converter (ADC) and consist of four general-purpose inputs connected to external device pins (CPUVCORE, VIN0 – VIN2) and four internal signals connected to the power supplies (AVCC, VBAT, 5VSB and 5VCC). All inputs are limited to a maximum voltage of 2.048V due to an internal setting of 8mV LSB (256 steps x 8mV = 2.048V). All inputs to the ADC must limit the maximum voltage by using a voltage divider. The power supplies have internal resistors, while the external pins require outside limiting resistors as described below.

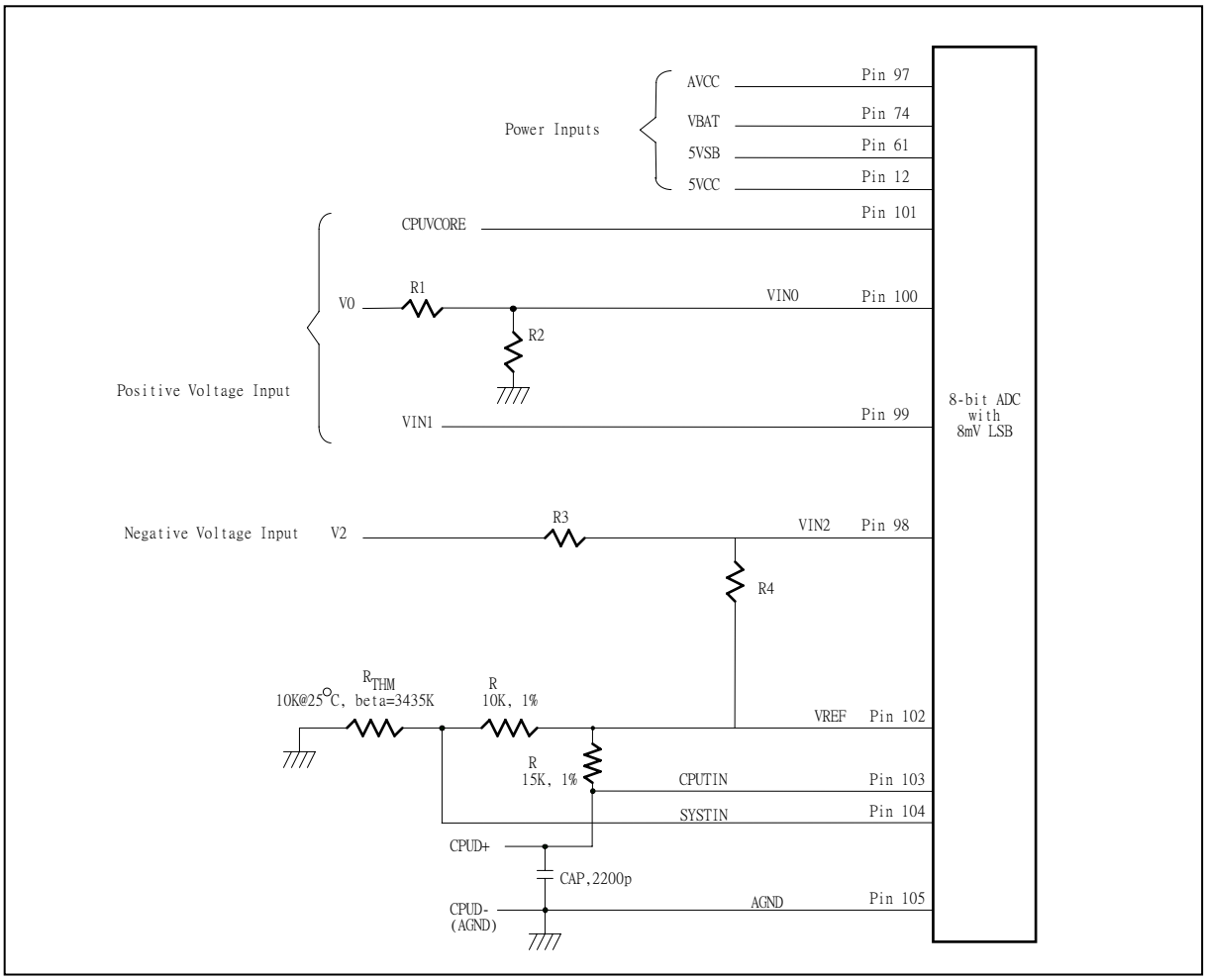


Figure 7-4 Analog Inputs and Application Circuit of the W83627UHG

As illustrated in the figure above, other connections may require some external circuits. The rest of this section provides more information about voltages outside the range of the 8-bit ADC, CPU Vcore voltage detection, and temperature measurement

7.3.1 Voltages Over 2.048 V or Less Than 0 V

Input voltages greater than 2.048 V should be reduced by an external resistor divider to keep the input voltages in the proper range. For example, input voltage V_0 (+12 V) should be reduced before it is connected to VIN0 according to the following equation:

$$VIN0 = V_0 \times \frac{R_2}{R_1 + R_2}$$

R1 and R2 can be set to 150 KΩ and 10 KΩ, respectively, to reduce V_0 from +12 V to less than 2.048 V.

The W83627UHG uses the same approach. Pins 12 and 97 provide two functions. One, these pins are connected to 5VCC at +5 V to supply internal (digital / analog) power to the W83627UHG. Two, these pins monitor 5VCC. The W83627UHG has two internal, 80-KΩ and 20-KΩ, serial resistors that reduce the ADC-input voltage to 1 V.

$$V_{in} = 5VCC \times \frac{20K\Omega}{80K\Omega + 20K\Omega} \cong 1V$$, where 5VCC is set to 5V

Pin 61 is implemented likewise to monitor its +5 V stand-by power supply.

Pin 74 also has two internal, 20-KΩ serial resistors that reduce the ADC-input voltage to 1.65 V.

$$V_{in} = VBAT \times \frac{20K\Omega}{20K\Omega + 20K\Omega} \cong 1.65V$$, where VBAT is set to 3.3V

The CPUVCORE pin feeds directly into the ADC with no voltage divider since the nominal voltage on this pin is only 1.2V.

Negative voltages are handled similarly, though the equation looks a little more complicated. For example, negative voltage V2 (-5V) can be reduced according to the following equation:

$$VIN2 = (V2 - 2.048) \times \frac{R_4}{R_3 + R_4} + 2.048, where V2 = -5$$

R3 and R4 can be set to 120 KΩ and 10 KΩ, respectively, to reduce negative input voltage V_2 from – 5 V to less than 2.048 V. Note that R4 is referenced to VREF, or 2.048V instead of 0V to allow for more dynamic range. This is simply good analog practice to yield the most precise measurements.

Both of these solutions are illustrated in the figure above.

7.3.2 Voltage Detection

The data format for voltage detection is an eight-bit value, and each unit represents an interval of 8 mV.

Detected Voltage = Reading * 0.008 V

If the source voltage was reduced by a voltage divider, the detected voltage value must be scaled up accordingly.

The voltage values can be read at Hardware Monitor Register Bank 0, Index 20h to 25h.

7.3.3 Temperature Sensing

The data format for sensor SYSTIN is 8-bit, two's-complement, and the data format for sensors CPUTIN is 9-bit, two's-complement. This is illustrated in the table below.

Table 7-1 Temperature Data Format

TEMPERATURE	8-BIT DIGITAL OUTPUT		9-BIT DIGITAL OUTPUT	
	8-BIT BINARY	8-BIT HEX	9-BIT BINARY	9-BIT HEX
+125°C	0111,1101	7Dh	0,1111,1010	0FAh
+25°C	0001,1001	19h	0,0011,0010	032h
+1°C	0000,0001	01h	0,0000,0010	002h
+0.5°C	-	-	0,0000,0001	001h
+0°C	0000,0000	00h	0,0000,0000	000h
-0.5°C	-	-	1,1111,1111	1FFh
-1°C	1111,1111	FFh	1,1111,1110	1FFh
-25°C	1110,0111	E7h	1,1100,1110	1CEh
-55°C	1100,1001	C9h	1,1001,0010	192h

Eight-bit temperature data is read from Index 27h. For nine-bit temperature data, the 8 MSB are read from Bank1 Index 50h,and the LSB is read from Bank1 Index 51h, bit 7.
There are two sources of temperature data: external thermistors or thermal diodes.

7.3.3.1 Monitor Temperature from Thermistor

External thermistors should have a β value of 3435K and a resistance of 10 KΩ at 25°C. As illustrated in the schematic below, the thermistor is connected in series with a 10-KΩ resistor and then connects to VREF (pin 102). The configuration registers to select a themistor temperature sensor and the measurement method are found at Bank 0, Index 59h, 5Dh, and 5Eh.

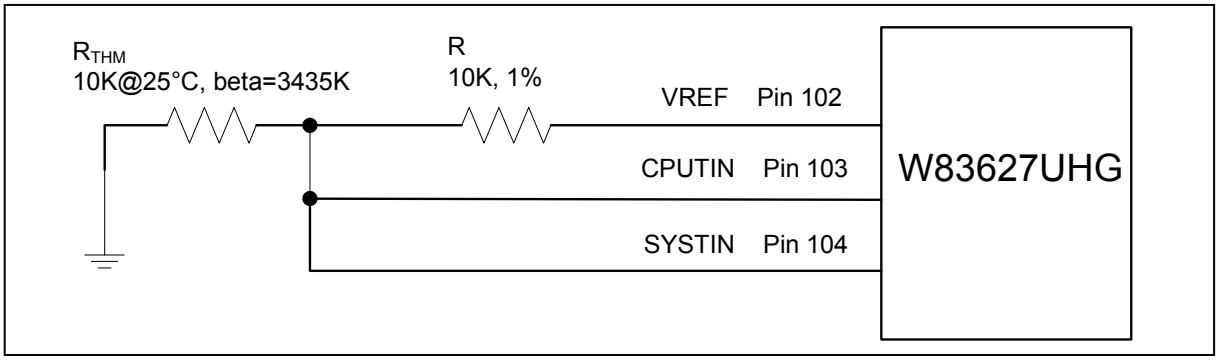


Figure 7-5 Monitoring Temperature from Thermistor

7.3.3.2 Monitor Temperature from Thermal Diode (Voltage Mode)

The thermal diode D- pin is connected to AGND (pin 105), and the D+ pin is connected to the temperature sensor pin in the W83627UHG. A 15-KΩ resistor is connected to VREF to supply the bias current for the diode, and the 2200-pF, bypass capacitor is added to filter high-frequency noise. The configuration registers to select a thermal diode temperature sensor and the measurement method are found at Bank 0, Index 59h, 5Dh, and 5Eh.

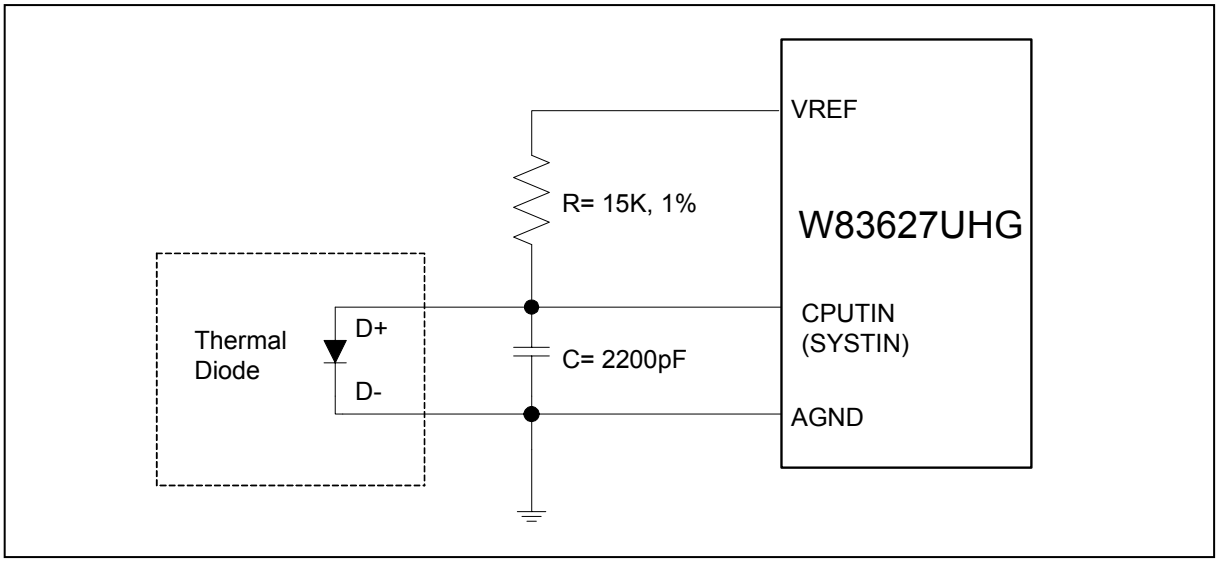


Figure 7-6 Monitoring Temperature from Thermal Diode (Voltage Mode)

7.3.3.3 Monitor Temperature from Thermal Diode (Current Mode)

The W83627UHG also can measure diode temperature by current mode and the circuit is shown in the following figure.

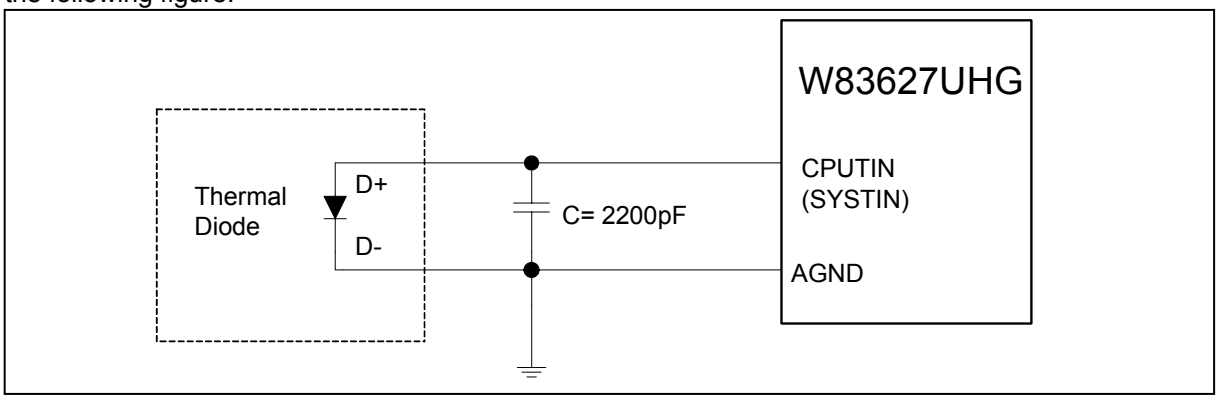


Figure 7-7 Monitoring Temperature from Thermal Diode

The pin of processor D- is connected to AGND (pin 105) and the pin D+ is connected to temperature sensor pin in W83627UHG. A bypass capacitor C=2200pF should be added to filter the high frequency noise. The configuration registers to select a thermal diode temperature sensor and the measurement method are found at Bank 0, Index 59h, 5Dh, and 5Eh.

7.4 SST Command Summary

The W83627UHG can act as an SST peripheral or slave and output the results of the Analog to Digital Converter onto the SST bus. SST is a new, popular standard to communicate temperature and voltage information from around the PC motherboard to report on the status of the system and control cooling fans and other safety mechanisms.

SST is a self-clocked, one-wire bus for data transfer. The bus requires no additional control lines. In addition, SST also includes variable data transfer rate established with every message. Therefore, it is comparatively flexible. The W83627UHG has a programmable SST address defined at Logical Device C CR[F1h]. The default address is 0x48h which is within the range of 0x48h-0x4ah defined in the SST specification.

Since the same, integrated Analog to Digital Converter is used, all the features and restrictions of use remain the same. The reference voltage is integrated and fixed with the 8-bit ADC, yielding a maximum voltage on each of 2.048V and an LSB of 8mV. As discussed in the previous section 7.3, voltage scaling using resistive dividers may be necessary to keep external voltages within the maximum input voltage range. The power supply pins have integrated resistive dividers.

7.4.1 Command Summary

The W83627UHG supports SST commands as shown in the following table:

Table 7-2 SST Command Summary

COMMAND	DESCRIPTION
ResetDevice()	This command is used to recover from serious hardware or bus error.
GetDIB()	Support 8-byte and 16-byte read length
GetIntTemp()	Returns the 20byte temperature data values for pin SYSTIN (Pin 104)
GetExtTemp()	Returns the 2-byte temperature data values for pin CPUTIN (Pin 103)
GetAllTemps()	Returns the 4-byte temperature data values for both SYSTIN and CPUTIN
GetVolt12V()	Returns the 2-byte voltage data values for pin VIN0 (Pin 100). This pin should be connected to +12V power through scaling resistors. Please refer to section 7.4.2.2
GetVolt5V()	Returns the 2-byte voltage data values for pin 5VCC (Pin 12, 48). This pin should be connected to +5V power directly. Please refer to section 7.4.2.2
GetVolt3p3V()	Returns the 2-byte voltage data values for pin VIN1 (Pin 99). This pin should be connected to +3.3V power through scaling resistors. Please refer to section 7.4.2.2
GetVolt2p5V()	Returns the 2-byte voltage data values for pin VIN2 (Pin 98). This pin should be connected to +2.5V power through scaling resistors. Please refer to section 7.4.2.2
GetVoltVccp()	Returns the 2-byte voltage data values of CPUVCORE (Pin 101). This pin should be connected to CPU power supply directly. The CPU power supply voltage must not be higher than **2.048** volt
GetAllVoltages()	Returns a 10-byte voltage data value containing all the above listed five (5) voltages

7.4.2 Combination Sensor Data Format

7.4.2.1 Temperature Data Format

The W83627UHG temperature data format of both CPUTIN and SYSTIN is 16-bit two's-complement binary value. It represents multiple of 1/64°C in the temperature reading.

Table 1 shows some typical temperature values in 16-bit two's complement format.

Table 7-3 Typical Temperature Values

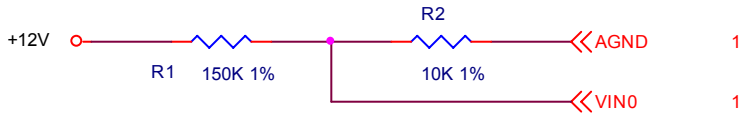
TEMPERATURE	16-BIT DIGITAL OUTPUT (2'S COMPLEMENT)	
	16-BIT BINARY	16-BIT HEX
+80°C	0001 0100 0000 0000	1400h
+79.5°C	0001 0011 1110 0000	13E0h
+1°C	0000 0000 0100 0000	0010h
+0°C	0000 0000 0000 0000	0000h
-1°C	1111 1111 1100 0000	FFC0h
-5°C	1111 1110 1100 0000	FEC0h

7.4.2.2 Voltage Data Format

The W83627UHG can return five (5) voltage values through the SST interface. The voltage data format is 16-bit two's-complement binary. The relation between the 2-byte data and the monitored voltage is listed below:

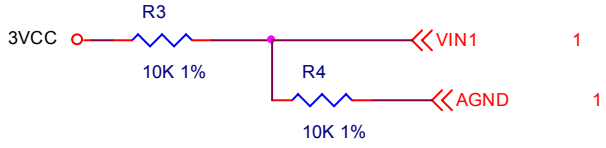
1) CPUVCORE (pin 101) = Decimal[2-byte data by GetVoltVccp()] / 1024 volts
2) 5VCC (pin 12) = Decimal[2-byte data by GetVolt5V()] / 1024 volts
3) "+12V" = Decimal[2-byte data by GetVolt12V()] / 1024 / ((R1+R2) / R2) volts

   VIN0 (pin 100) is connected as shown below:



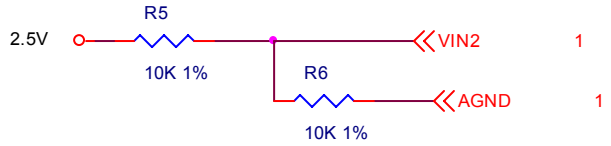
4) "+3VCC" = Decimal[2-byte data by GetVolt3p3V()] / 1024 / ((R3+R4) / R4) volts

VIN1 (pin 99) is connected as shown below:



5) "+2.5V" = Decimal[2-byte data by GetVolt2p5V()] / 1024 / ((R5+R6) / R6) volts

VIN2 (pin 98) is connected as shown below:



7.5 PECI

PECI (Platform Environment Control Interface) is a proprietary derivation of SST. It is one of the temperature sensing methods that the W83627UHG supports. With a bandwidth ranging from 2 kbps to 2 Mbps, PECI uses a single wire – no additional control lines needed – for self-clocking and data transfer. By interfacing to Digital Thermal Sensor on the Intel® CPU, PECI reports a negative temperature value relative to the processor's temperature at which the thermal control circuit (TCC) is activated.

To enable the PECI functionalities of the W83627UHG, BIOS/software should follow the steps below:

1. Program Logical Device C, CR[E8h] bit (1..0) for PECI speed selection to meet the bit timing limits of CPU with PECI. "11b" is recommended to be set to the bit for better stability.

2. Program Logical Device C, CR[E5h] bit (7..4) for each PECI Agent to match the number of domains in the processors. Setting to "1" enables the W83627UHG to issue GetTemp(0) and GetTemp(1) commands to access the PECI temperatures of domains 0 and domain 1. Setting to "0" enables the W83627UHG to issue GetTemp(0) command for domain 0.

3. Program Logical Device C, CR[E0h] bit (3..0) for each PECI Agent. Setting to "1" returns the PECI temperature of domain 1 to the temperature reading register. Setting to "0" returns the PECI temperature of domain 0 to the temperature reading register. If CR[E5h] bit 1 is set to "1", the higher PECI temperature of domain 0 and domain 1 is returned to the temperature reading register. See the example below for more details about the temperature reading register(s)

4. Program Logical Device C, CR[E0h] bit (7..4) for each PECI Agent. Setting to "1" enables the W83627UHG to access the agent. The power-on default is disabled. After an agent is enabled, the W83627UHG issues PING and GetTemp commands to obtain the PECI temperature.

5. Since the PECI temperature is a relative value, the W83627UHG provides registers for each PECI Agent to convert the relative value to a more traditional "absolute" format. The *TBase registers* (Logical Device C, CR[E1h]~CR[E4h]) store the "base" temperature. By means of BIOS/software, the desired base temperature can be written to these registers. Important: the value must be positive. Otherwise abnormal temperature responses will take place. Here is an example on how to obtain TBase value:

(1). Use a digital thermometer on the surface of the PECI processor to measure the processor body temperature.

(2). Power up the system with the PECI processor. Run the processor to 100% loading.

(3). After the system is stable, read the PECI reading from Logical Device C, CR[E0h] ~ CR[E7h] of selected Agents and record the value of the digital thermometer.

(4). Calculate TBase. For example, if PECI = -10 and the digital thermometer is 50'C, then TBase could be set to 60'C. (60 – 10 = 50).

6. There are two temperature reading registers in the W83627UHG: Bank1, Index 50h & 51h, and Bank2, Index 50h & 51h. The source of the Bank 1, Index 50h & 51h value is determined by the value programmed into the *CPUFANOUT monitor Temperature source select register* (Hardware Monitor Device, Bank 0, Index 49h, bits (2..0)). The source of Bank 2, Index 50h & 51h value is determined by the value programmed into the *SYSFANOUT monitor Temperature source select register* (Hardware Monitor Device, Bank 0, Index 4Ah, bits(7..5)).

7. The temperature values in Bank 1 and Bank 2 Index 50h & 51h are:

Bank 1, Index 50h & 51h = (TBase) + (PECI Agent relative temperature)

Bank 2, Index 50h & 51h = (TBase) + (PECI Agent relative temperature)

Example:

If the PECI relative temperature of agent 1 is -10; TBase is set to 72°C, and Bank0 Index 49h selects PECI Agent 1 as the temperature source, the reported temperature will be 62°C (-10 + 72).

Please be noted that when the temperature source is selected as PECI temperature source, the Bank 1 Index 50h & 51h or Bank 2 Index 50h & 51h reading does not reflect the actual temperature of the processor.

8. In addition, each PECI Agent relative temperature can be read in Logical Device C, CR[E0h] ~ CR[E7h], as long as Logical Device C, CR[E8h] bit 3 is set to "1". When this bit is "1", Logical Device C, CR[E0h] ~ CR[E7h] become "Read Only" registers.

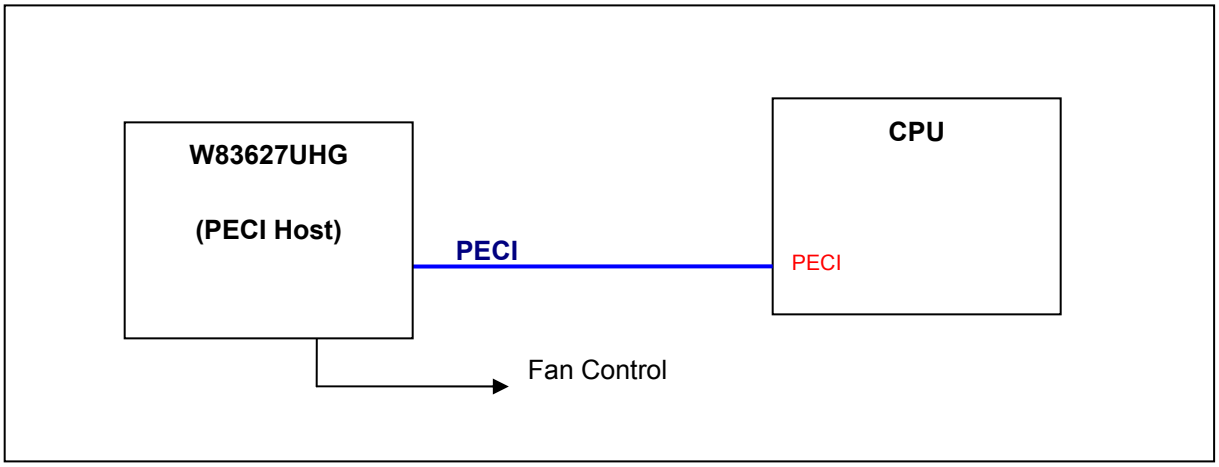


Figure 7-8 PECI Illustration

9. A warning flag register at Logical Device C, CR[E8h] bit (7..4) is designed for each PECI Agent to report whether the W83627UHG (PECI host) detects the PECI client or not and whether the PECI client returns invalid FCS values from the polling for three successive times.

7.6 Fan Speed Measurement and Control

This section is divided into two parts, one to measure the speed and the other to control the speed.

7.6.1 Fan Speed Measurement

The W83627UHG can measure fan speed for fans equipped with tachometer outputs. The tachometer signals should be set to TTL-level, and the maximum input voltage cannot exceed +5 V. If the tachometer signal exceeds +5 V, an external trimming circuit should be added to reduce the voltage accordingly.

The fan speed counter is read from Bank0 Index 28h, and 29h. The fan speed can then be evaluated by the following equation:

$$RPM = \frac{1.35 \times 10^6}{Count \times Divisor}$$

The default divisor is 2 and is specified at Bank0 Index 47h, bits 7 ~ 4; and Index 5Dh, bits 6 ~ 5. There are three bits for each divisor, and the corresponding divisor is listed in the table below.

Table 7-4 Fan Divisor Definition

BIT 2	BIT 1	BIT 0	FAN DIVISOR	BIT 2	BIT 1	BIT 0	FAN DIVISOR
0	0	0	**1**	1	0	0	**16**
0	0	1	**2**	1	0	1	**32**
0	1	0	**4**	1	1	0	**64**
0	1	1	**8**	1	1	1	**128**

The following table provides some examples of the relationship between divisor, RPM, and count.

Table 7-5 Divisor, RPM, and Count Relation

DIVISOR	NOMINAL RPM	TIME PER REVOLUTION	COUNTS	70% RPM	TIME FOR 70%
1	8800	6.82 ms	*153*	6160	9.84 ms
2 (default)	4400	13.64 ms	*153*	3080	19.48 ms
4	2200	27.27 ms	*153*	1540	38.96 ms
8	1100	54.54 ms	*153*	770	77.92 ms
16	550	109.08 ms	*153*	385	155.84 ms
32	275	218.16 ms	*153*	192	311.68 ms
64	137	436.32 ms	*153*	96	623.36 ms
128	68	872.64 ms	*153*	48	1246.72 ms

7.6.2 Fan Speed Control

The W83627UHG has two output pins for fan control, each of which offers PWM duty cycle and DC voltage to control the fan speed. The output type (PWM or DC) of each pin is configured by Bank0 Index 04h, bits 1 ~ 0.

For PWM, the duty cycle is programmed by eight-bit registers at Bank0 Index 01h and Index 03h. The duty cycle can be calculated using the following equation:

$$\text{Dutycycle}(\%) = \frac{\text{Programmed 8 - bit Register Value}}{255} \times 100\%$$

The default duty cycle is FFh, or 100%. The PWM clock frequency is programmed at Bank0 Index 00h and Index 02h.

For DC, the W83627UHG has a six bit digital-to-analog converter (DAC) that produces 0 to 5 Volts DC. The analog output is programmed at Bank0 Index 01h and Index 03h. The analog output can be calculated using the following equation:

$$\text{OUTPUT Voltage (V)} = AVCC \times \frac{\text{Programmed 6 - bit Register Value}}{64}$$

The default value is 111111YY, or nearly 5 V, and Y is a reserved bit.

7.6.3 SMART FAN™ Control

The W83627UHG supports two SMART FAN™ I features—Thermal Cruise™ mode and Fan Speed Cruise™ mode—and SMART FAN™ III. Each of these is discussed in the following sections. When SMART FAN™ I features are enabled, fan output starts from the previous setting in Bank0 Index 01h and Index 03h.

There are two pairs of temperature sensors and fan outputs in SMART FAN™ I, as illustrated in the figure below.

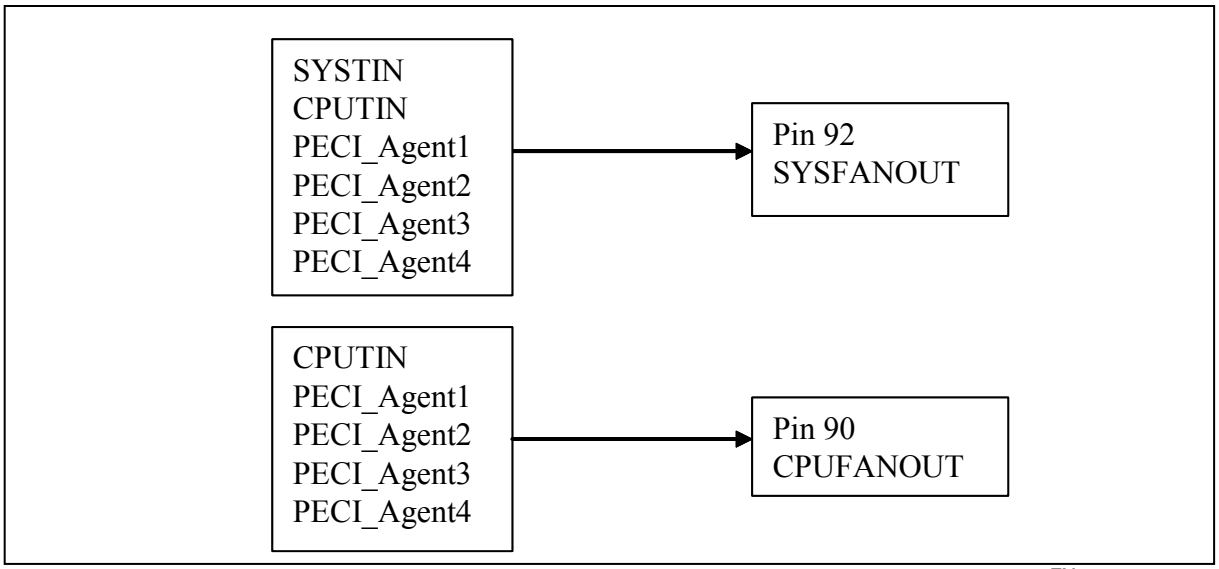


Figure 7-9 FANOUT and Corresponding Temperature Sensors in SMART FAN™I

7.6.3.1 Thermal Cruise™ Mode

Two pairs of temperature sensors and fan outputs in Thermal Cruise™ mode:

- SYSTIN and the temperature sensor selected by Bank0 Index 4Ah, bits 7 ~ 5
- CPUTIN and the temperature sensor selected by Bank0 Index 49h, bits 2 ~ 0

Thermal Cruise™ mode controls the fan speed to keep the temperature in a specified range. First, this range is defined in BIOS by a temperature and the interval (e.g., 55 °C ± 3 °C). As long as the current temperature remains below the low end of this range (i.e., 52 °C), the fan is off. Once the temperature exceeds the low end, the fan turns on at a speed defined in BIOS (e.g., 20% output). Thermal Cruise™ mode then controls the fan output according to the current temperature. Three conditions may occur:

(1) If the temperature still exceeds the high end, fan output increases slowly. If the fan is operating at full speed but the temperature still exceeds the high end, a warning message is issued to protect the system.

(2) If the temperature falls below the high end (e.g., 58 °C) but remains above the low end (e.g., 52 °C), fan output remains the same.

(3) If the temperature falls below the low end (e.g., 52 °C), fan output decreases slowly to zero or to a specified “stop value”. This stop value is enabled by Bank0 Index12h, bits 5 ~ 4, and the value itself is specified in Bank0 Index 08h and Index 09h. The fan remains at the stop value for the period of time defined in Bank0 Index 0Ch and Index 0Dh.

In general, Thermal Cruise™ mode means

- if the current temperature is higher than the high end, increase the fan speed;
- if the current temperature is lower than the low end, decrease the fan speed;
- otherwise, keep the fan speed the same.

The following figures illustrate two examples of Thermal Cruise™ mode.

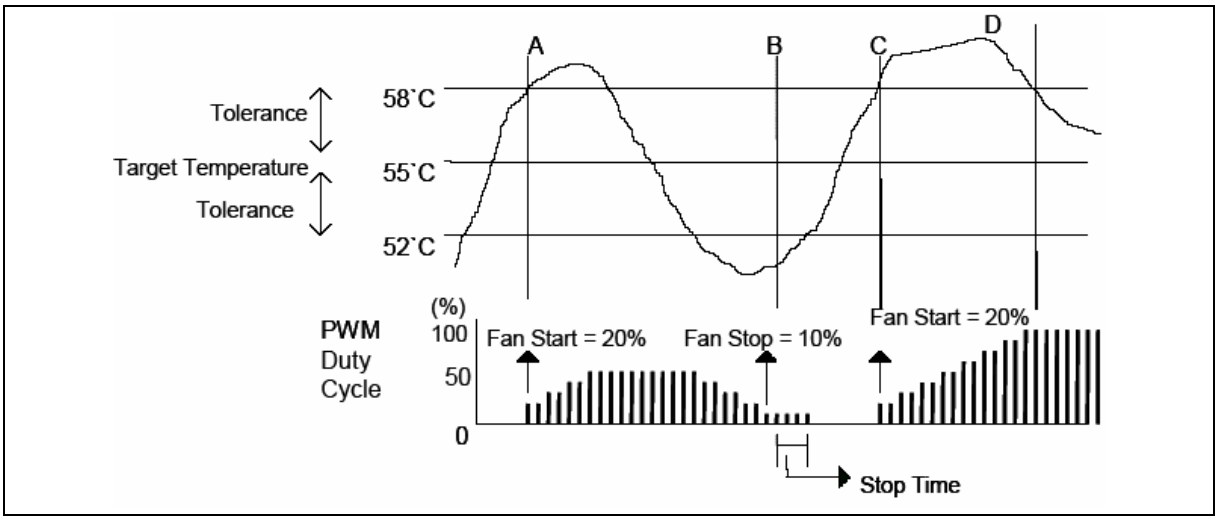


Figure 7-10 Mechanism of Thermal Cruise™ Mode (PWM Duty Cycle)

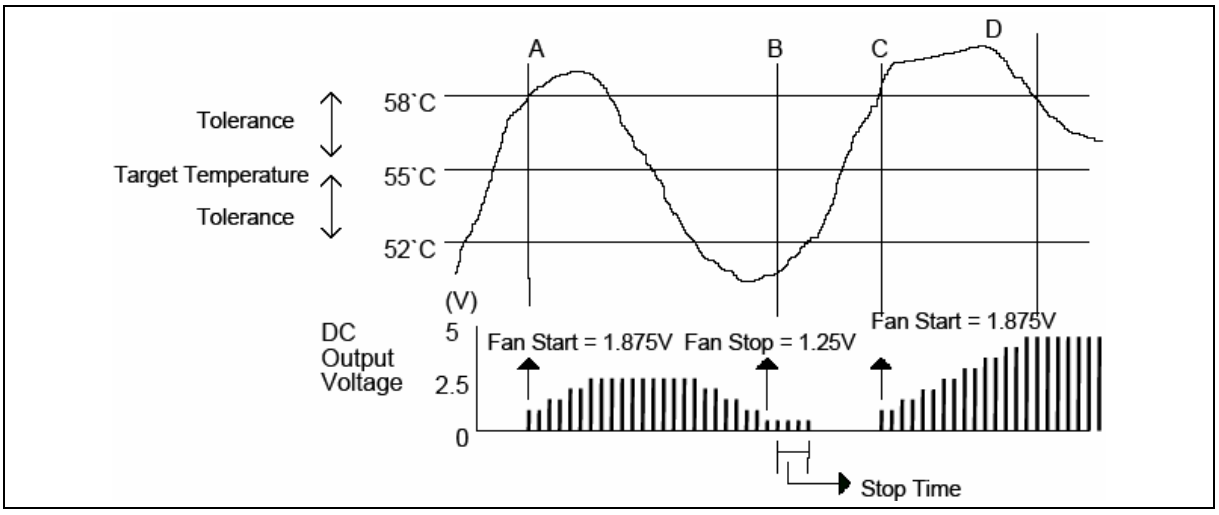


Figure 7-11 Mechanism of Thermal Cruise™ Mode (DC Output Voltage)

7.6.3.2 Fan Speed Cruise™ Mode

Two pairs of fan input sensors and fan outputs in Fan Speed Cruise™ mode.

- SYSFANIN and SYSFANOUT
- CPUFANIN and CPUFANOUT

Fan Speed Cruise™ mode keeps the fan speed in a specified range. First, this range is defined in BIOS by a fan speed count (the amount of time between clock input signals, not the number of clock input signals in a period of time) and an interval (e.g., 160 ± 10). As long as the fan speed count is in the specified range, fan output remains the same. If the fan speed count is higher than the high end (e.g., 170), fan output increases to make the count lower. If the fan speed count is lower than the low end (e.g., 150), fan output decreases to make the count higher. One example is illustrated in this figure.

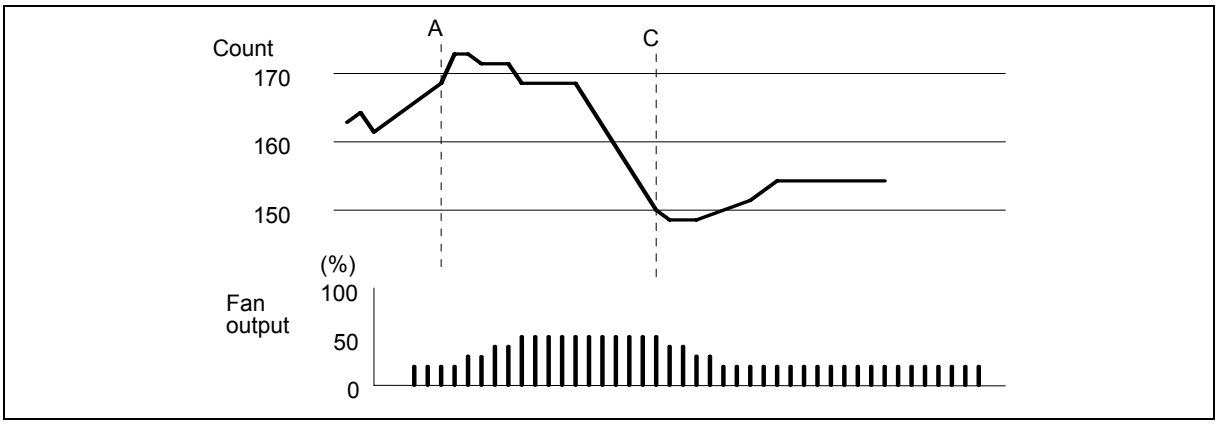


Figure 7-12 Mechanism of Fan Speed Cruise™ Mode

The following tables show current temperature, fan output value and the relative control registers at Thermal Cruise™ and Fan Speed Cruise™ mode.

Table 7-6 Display Registers – at SMART FAN™ I Mode

DESCRIPTION	REGISTER ADDRESS	REGISTER NAME	ATTRIBUTE	BIT DATA
Current CPU Temperature	Bank1, Index 50h ,51h	CPUTIN Temperature Sensor	Read only	8 MSB, 1°C bit 7, 0.5 °C
Current SYS Temperature	Bank0, Index 27h	SYSTIN Temperature Sensor	Read only	8 MSB, 1°C
Current CPUFANOUT Output Value	Bank0, Index 03h	CPUFANOUT Output Value Select	80h / FFh by strapping	Bits 7-0 CPUFANOUT Value
Current SYSFANOUT Output Value	Bank0 Index 01h	SYSFANOUT Output Value Select	80h / FFh by strapping	Bits 7-0 SYSFANOUT Value

Table 7-7 Relative Registers – at Thermal Cruise™ Mode

SPEED CRUISE™ MODE	TARGET TEMPERATURE	TOLERANCE	START-UP VALUE	STOP VALUE	KEEP MIN. FAN OUTPUT VALUE	STOP TIME	STEP-DOWN TIME	STEP-UP TIME
SYSFANOUT	Bank0, 05h	Bank0, 07h Bits0-3	Bank0, 0Ah	Bank0, 08h	Bank0, 12h, Bit5	Bank0, 0Ch	Bank0, 0Eh	Bank0, 0Fh
CPUFANOUT	Bank0, 06h	Bank0, 07h Bits 4-7	Bank0, 0Bh	Bank0, 09h	Bank0, 12h, Bit4	Bank0, 0Dh		

Table 7-8 Relative Registers – at Speed Cruise™ Mode

THERMAL-CRUISE™ MODE	TARGET-SPEED COUNT	TOLERANCE	KEEP MIN. FAN OUTPUT VALUE	STEP-DOWN TIME	STEP-UP TIME
SYSFANOUT	Bank0, Index 05h	Bank0, Index 07h Bits 0-3	Bank0, Index 12h Bit5	Bank0, Index 0Eh	Bank0, Index 0Fh
CPUFANOUT	Bank0, Index 06h	Bank0, Index 07h Bits 4-7	Bank0, Index 12h Bit4		

7.6.3.3 SMART FAN™ III

SMART FAN™ III controls the fan speed so that the temperature meets the target temperature set in BIOS or application software. There is only one pair of fan outputs and temperature sensors in SMART FAN™ III mode.

- CPUFANOUT and the temperature sensor selected by Bank0 Index 49h, bits 2 ~ 0

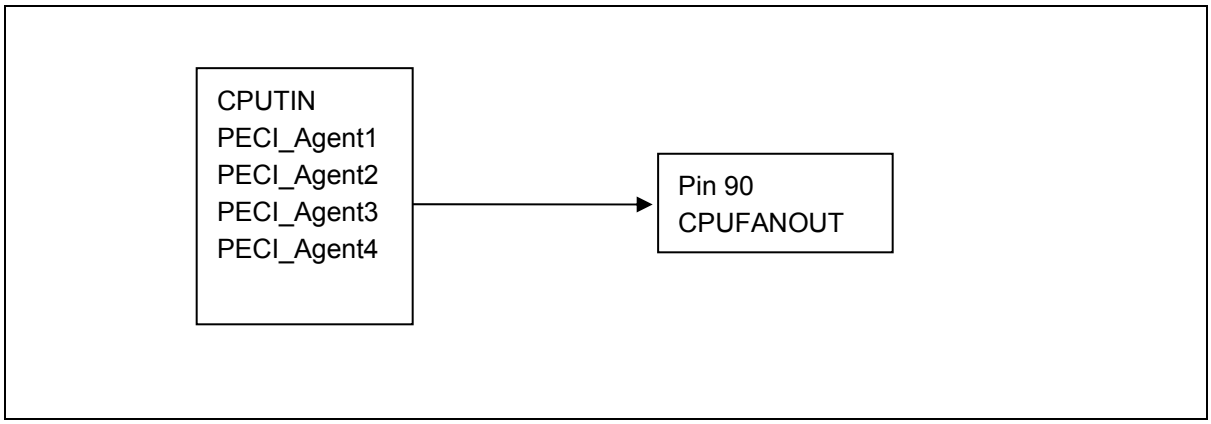


Figure 7-13 FANOUT and Corresponding Temperature Sensor in SMART FAN™ III

The algorithm is as follows:

(1) The target temperature, temperature tolerance, maximum and minimum fan outputs and step are set.
(2) The following figure shows the initial conditions. If the current temperature is within (Target Temperature ± Temperature Tolerance), the fan speed remains constant.

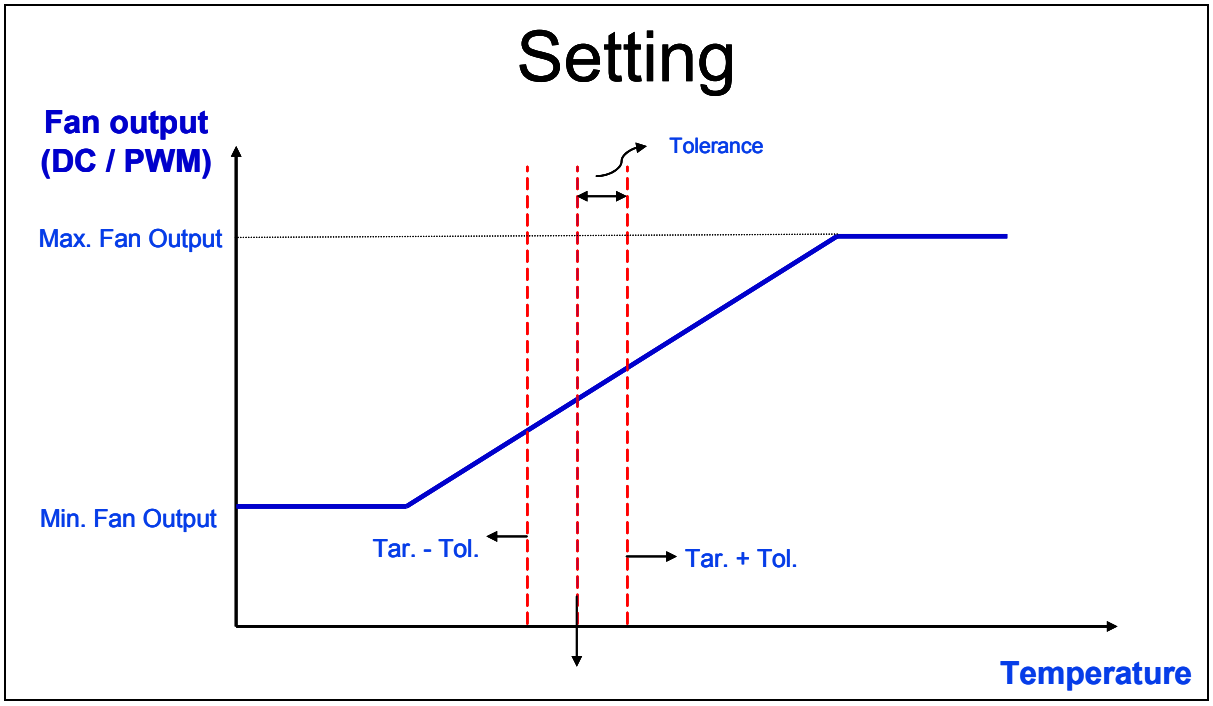


Figure 7-14 Setting of SMART FAN™ III

(3) If the current temperature is higher than (Target Temperature + Temperature Tolerance), fan speed rises one step. The step is the value in the CPUFANOUT Output Value Select Register, Bank0, Index 03h. In addition, the target temperature shifts to (Target Temperature + Temperature Tolerance), creating a new target temperature, named Target Temperature 1 in this figure.

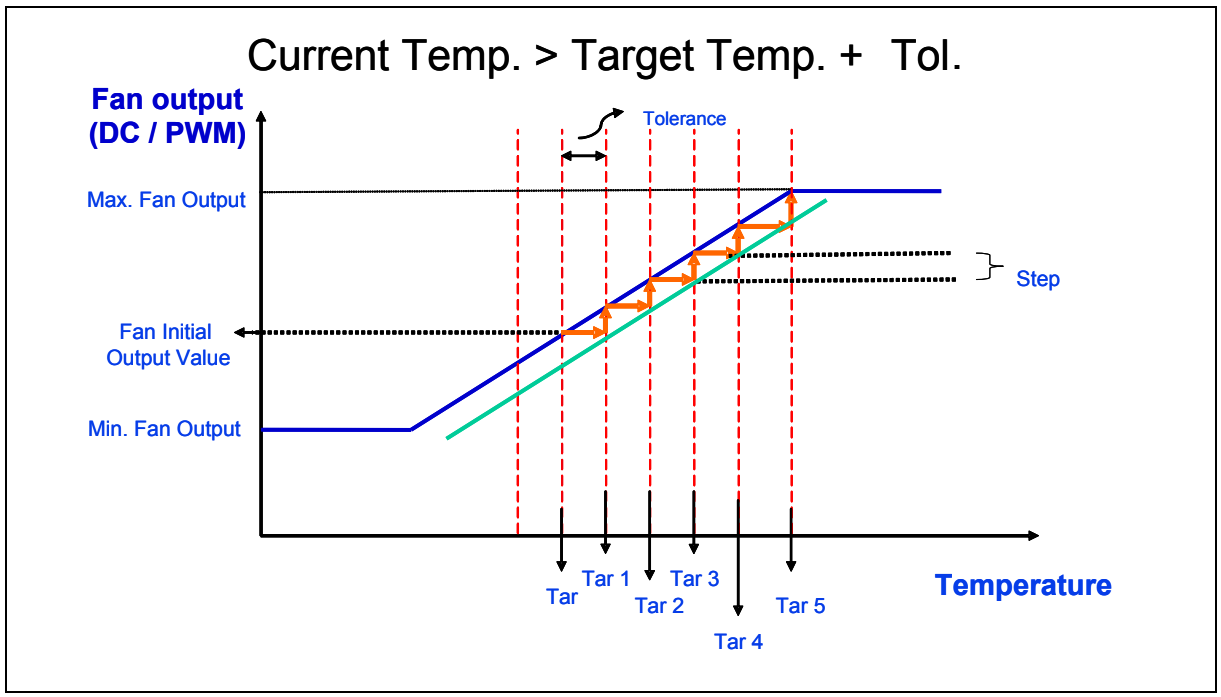


Figure 7-15 SMART FAN™ III Mechanism (Current Temp. > Target Temp. + Tol.)

If the current temperature rises higher than (Target Temperature 1 + Temperature Tolerance), the fan speed rises one step again, and the target temperature shifts to (Target Temperature 1 + Temperature Tolerance), or Target Temperature 2. This process repeats whenever the current temperature is higher than (Target Temperature X ± Temperature Tolerance) or until the fan speed reaches its maximum speed.

(4) If the current temperature falls below (Target Temperature — Temperature Tolerance), the fan speed falls one step. The step is the value in the CPUFANOUT Output Value Select Register, Bank0, Index 03h. In addition, the target temperature shifts to (Target Temperature — Temperature Tolerance), creating a new target temperature named Target Temperature 1.This is illustrated in the figure below.

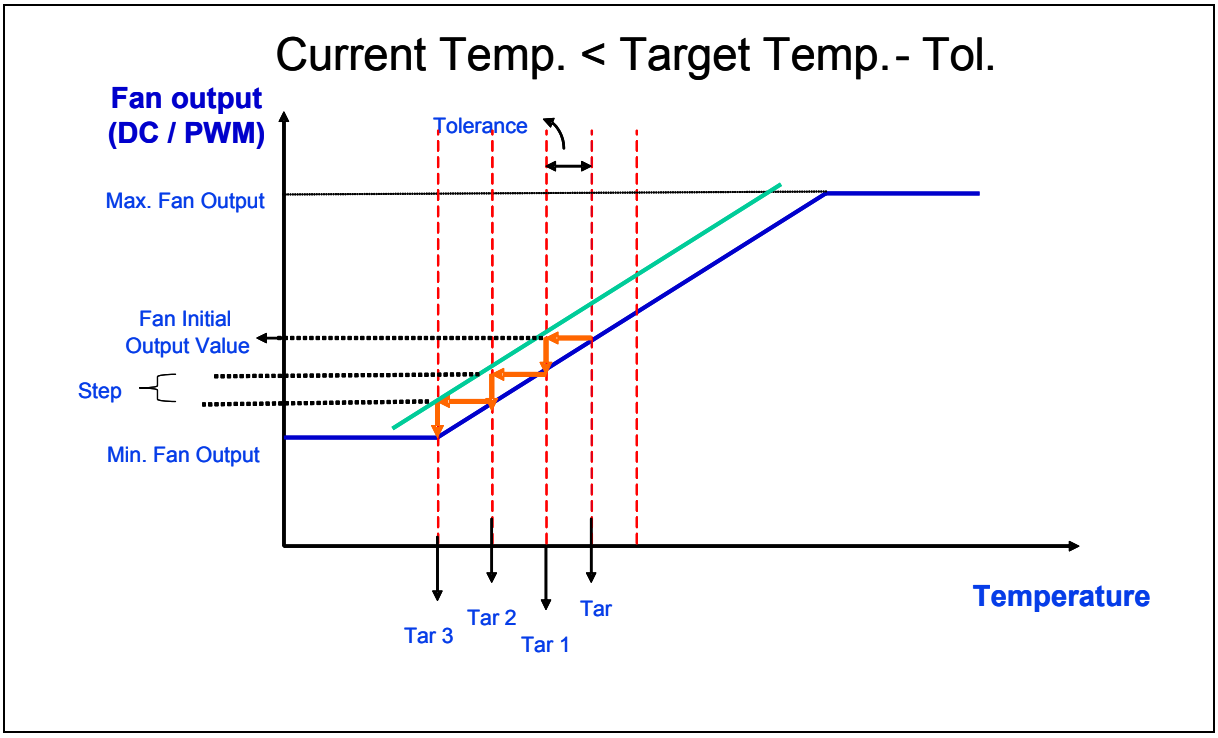


Figure 7-16 SMART FAN™ III Mechanism (Current Temp. < Target Temp. – Tol.)

If the current temperature falls lower than (Target Temperature 1 — Temperature Tolerance), the fan speed is reduced one step again, and the target temperature shifts to (Target Temperature 1 — Temperature Tolerance), or Target Temperature 2. This process repeats whenever the current temperature is lower than (Target Temperature X — Temperature Tolerance) or until the fan speed reaches its minimum speed.

(5) If the current temperature is always lower than (Target Temperature X — Temperature Tolerance), the fan speed decreases slowly to zero or to a specified stop value. The stop value is enabled by register Bank0, 12h, bit 4 and the stop value is specified in Bank0, Index 09h. The fan remains at the stop value for the period of time defined in Bank0, Index 0Dh.

The following tables show the current temperature, fan output value and the relative control registers at SMART FAN™ III mode.

Table 7-9 Display Register – at SMART FAN™III Mode

DESCRIPTION	REGISTER ADDRESS	REGISTER NAME	ATTRIBUTE	BIT DATA
Current CPU Temperature	Bank1, Index 50h ,51h	CPUTIN Temperature Sensor	Read only	8 MSB, 1°C bit 7, 0.5 °C
Current CPUFANOUT Output Value	Bank0, Index 03h	CPUFANOUT Output Value Select	80h / FFh by strapping	Bits 7-0 CPUFANOUT Value

Table 7-10 Relative Register – at SMART FAN™ III Control Mode

SMART FAN™ III MODE	TARGET TEMPERATURE	TOLERANCE	STOP VALUE (MIN. FAN OUTPUT)	MAX. FAN OUTPUT	STOP TIME
CPUFANOUT	Bank0, Index 06h	Bank0, Index 07h, bit 4-7	Bank0, Index 09h	Bank0, Index 67h	Bank0, Index 0Dh
SMART FAN™ III MODE	**OUTPUT STEP**	**STEP DOWN TIME**	**STEP UP TIME**	**KEEP MIN. FAN OUTPUT VALUE**	
CPUFANOUT	Bank0, Index 68h	Bank0, Index 0Fh	Bank0, Index 0Eh	Bank0, Index 12h, bit 4	

7.7 Interrupt Detection

7.7.1 SMI# Interrupt Mode

The SMI#/OVT# pin (pin 95) is a multi-function pin. It can be in SMI# mode or in OVT# mode by setting Configuration Register CR[29h], bit 6 to one or zero, respectively. In SMI# mode, it can monitor voltages, fan counts, or temperatures.

7.7.1.1 Voltage SMI# Mode

The SMI# pin can create an interrupt if a voltage exceeds a specified high limit or falls below a specified low limit. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This mode is illustrated in the following figure.

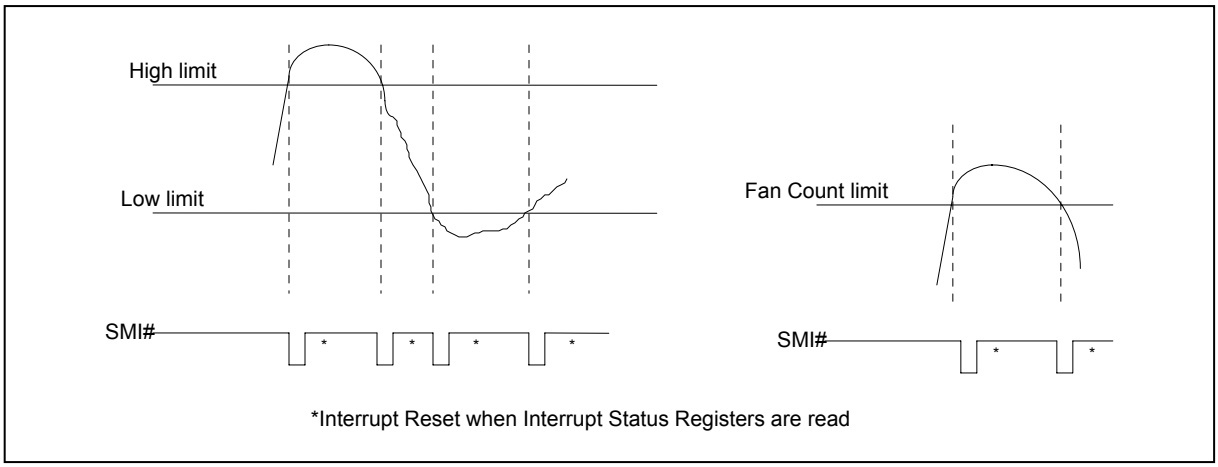


Figure 7-17 SMI Mode of Voltage and Fan Inputs

7.7.1.2 Fan SMI# Mode

The SMI# pin can create an interrupt if a fan count crosses a specified fan limit (rises above it or falls below it). This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This mode is illustrated in the figure above.

7.7.1.3 Temperature SMI# Mode

The SMI# pin can create interrupts that depend on the temperatures measured by SYSTIN and CPUTIN. These interrupts are divided into two parts, one for SYSTIN and the other for CPUTIN.

7.7.1.3.1 Temperature Sensor 1(SYSTIN) SMI# Interrupt

The SMI# pin has three interrupt modes with SYSTIN.

(1) Comparator Interrupt Mode

This mode is enabled by setting T_{HYST} (Temperature Hysteresis) to 127°C.

In this mode, the SMI# pin can create an interrupt as long as the current temperature exceeds T_O (Over Temperature). This interrupt can be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. If the interrupt is reset, the SMI# pin continues to create interrupts until the temperature goes below T_O. This is illustrated in the figure below.

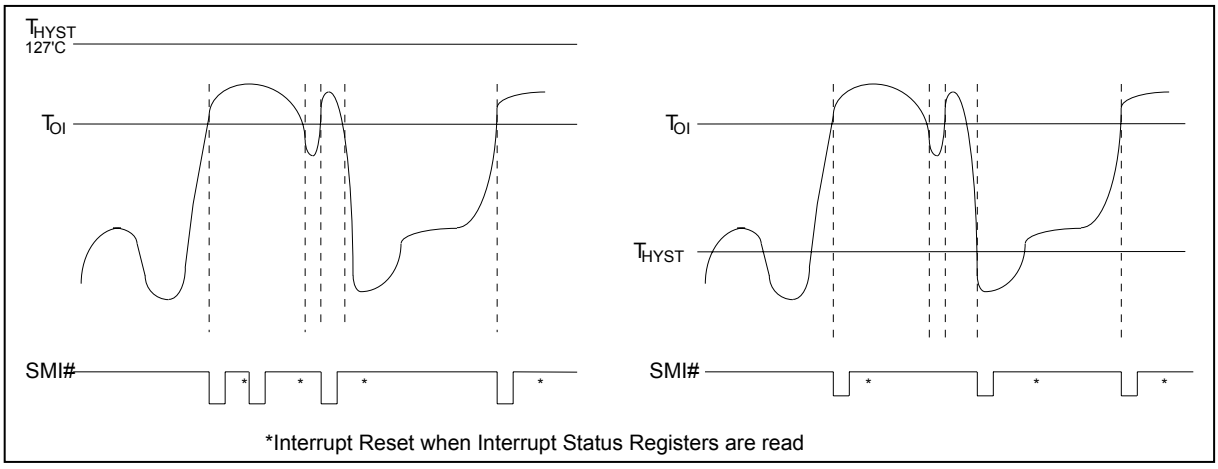


Figure 7-18 SMI Mode of SYSTIN I

(2) Two-Times Interrupt Mode

This mode is enabled by setting T_{HYST} (Temperature Hysteresis) lower than T_O and setting Bank0 Index 4Ch, bit 5 to zero.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_O or when the current temperature falls below T_{HYST}. Once the temperature rises above T_O, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the figure above.

(3) One-Time Interrupt Mode

This mode is enabled by setting T_{HYST} (Temperature Hysteresis) lower than T_O and setting Bank0 Index 4Ch, bit 5 to one.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_O. Once the temperature rises above T_O, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the following figure.

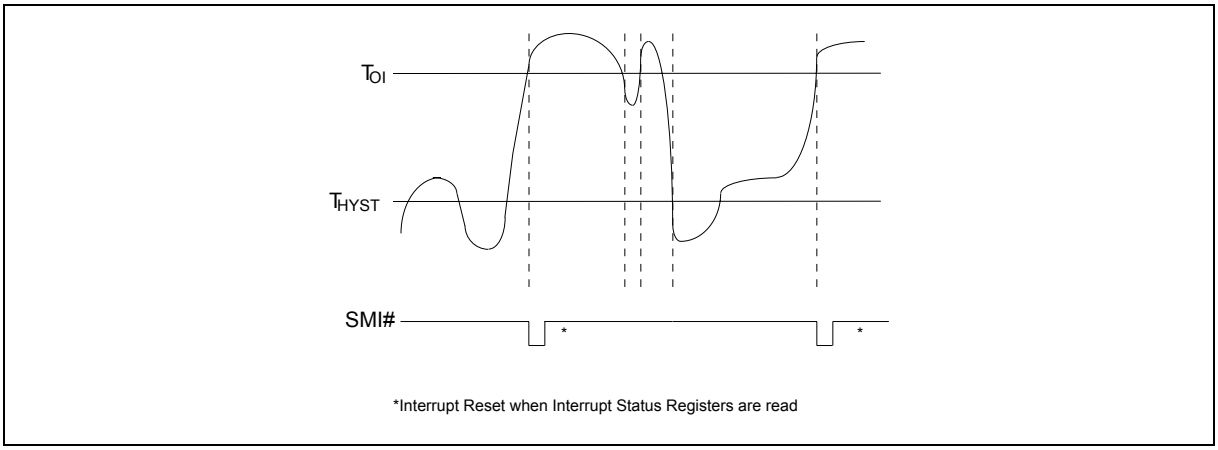


Figure 7-19 SMI Mode of SYSTIN II

7.7.1.3.2 Temperature Sensor 2(CPUTIN) SMI# Interrupt

The SMI# pin has two interrupt modes with CPUTIN.

(1) Comparator Interrupt Mode

This mode is enabled by setting Bank0 Index 4Ch, bit 6, to one.

In this mode, the SMI# pin can create an interrupt when the current temperature exceeds T_O (Over Temperature) and continues to create interrupts until the temperature falls below T_{HYST}. This interrupt can be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the figure below.

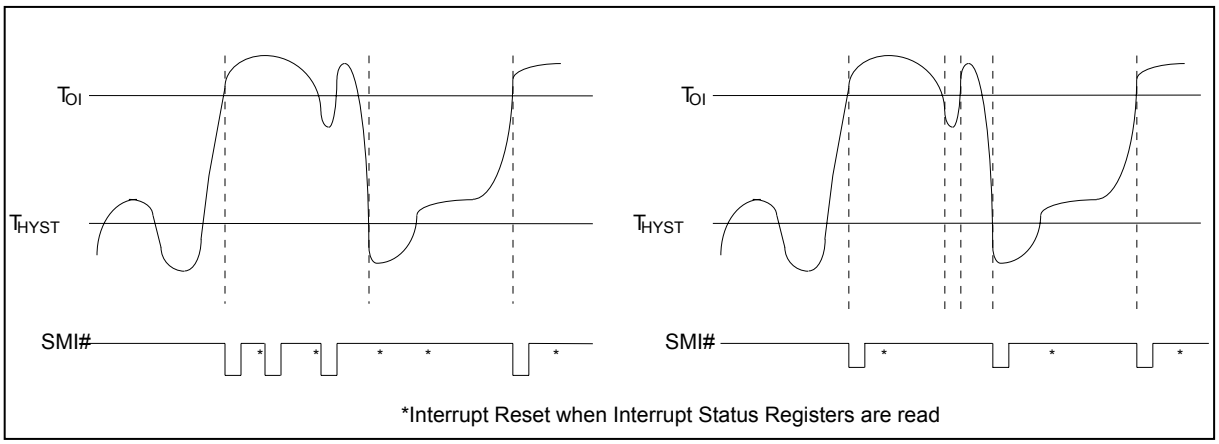


Figure 7-20 SMI Mode of CPUTIN

(2) Two-Times Interrupt Mode

This mode is enabled by setting Bank0 Index 4Ch, bit 6, to zero.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_O or when the current temperature falls below T_{HYST}. Once the temperature rises above T_O, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the figure above.

7.7.2 OVT# Interrupt Mode

The SMI#/OVT# pin is a multi-function pin. It can be in SMI# mode or in OVT# mode by setting Configuration Register CR[29h], bit 6 to one or zero, respectively. In OVT# mode, it can monitor temperatures, and it is enabled or disabled for SYSTIN and CPUTIN by Bank0 Index 18h, bit 6; and Bank0, Index 4Ch, bit 3.

The OVT# pin has two interrupt modes, comparator and interrupt. The modes are illustrated in this figure.

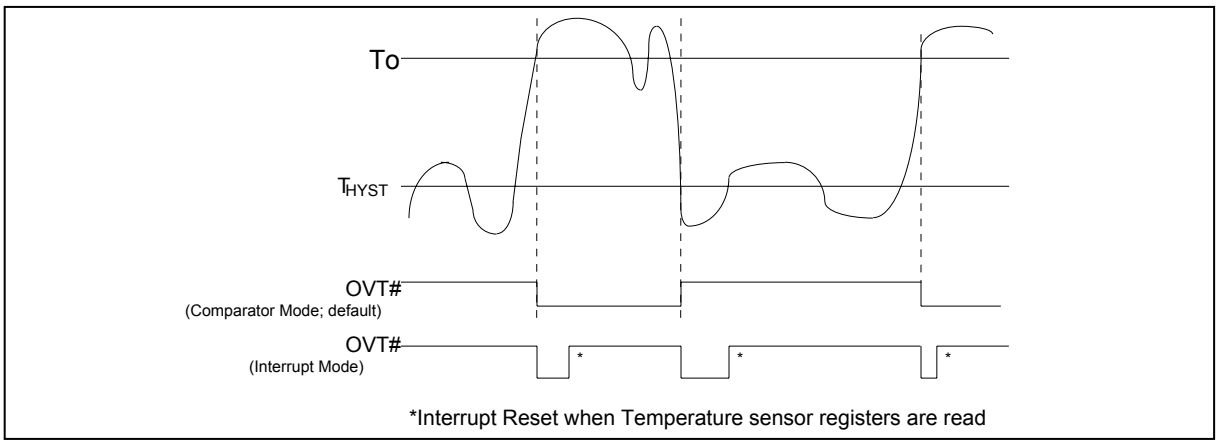


Figure 7-21 OVT# Modes of Temperature Inputs

If Bank0, Index 18h, bit 6, and Bank2 Index 52h, bit1 are set to zero, the OVT# pin is in comparator mode. In comparator mode, the OVT# pin can create an interrupt once the current temperature exceeds T_O and continues to create interrupts until the temperature falls below T_{HYST}. The OVT# pin is asserted once the temperature has exceeded T_O and has not yet fallen below T_{HYST}.

If Bank0, Index 18h, bit 6, and Bank2 Index 52h, bit1 are set to one, the OVT# pin is in interrupt mode. In interrupt mode, the OVT# pin can create an interrupt once the current temperature rises above T_O or when the temperature falls below T_{HYST}. Once the temperature rises above T_O, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers. The OVT# pin is asserted when an interrupt is generated and remains asserted until the interrupt is reset.

7.7.3 Caseopen Detection

The purpose of Caseopen function is used to detect whether the computer case has been opened and possibly tampered with. This feature must function even when there is no 5VSB power. Consequently, the power source for the circuit is from either Pin 74 (VBAT) or Pin 61 (5VSB). 5VSB is the default power source. If there is no 5VSB power, the power source is VBAT. This is designed to save power consumption of the battery.

When the case is closed, CASEOPEN# (Pin 76) must be pulled high by an external 2MΩ resistor that is connected to VBAT (Pin 74). When the case is opened, CASEOPEN# will be switched from high to low. Meanwhile, the detection circuit inside the IC latches the signal. As a result, the interrupt status and the real-time status can be read at the registers next time when the computer is powered. The status will not be cleared unless Bank 0, Index 46h, bit 7, or CR[E6h] bit 5 at Logical Device A is set to "1" first and this bit is self-cleared to "0".

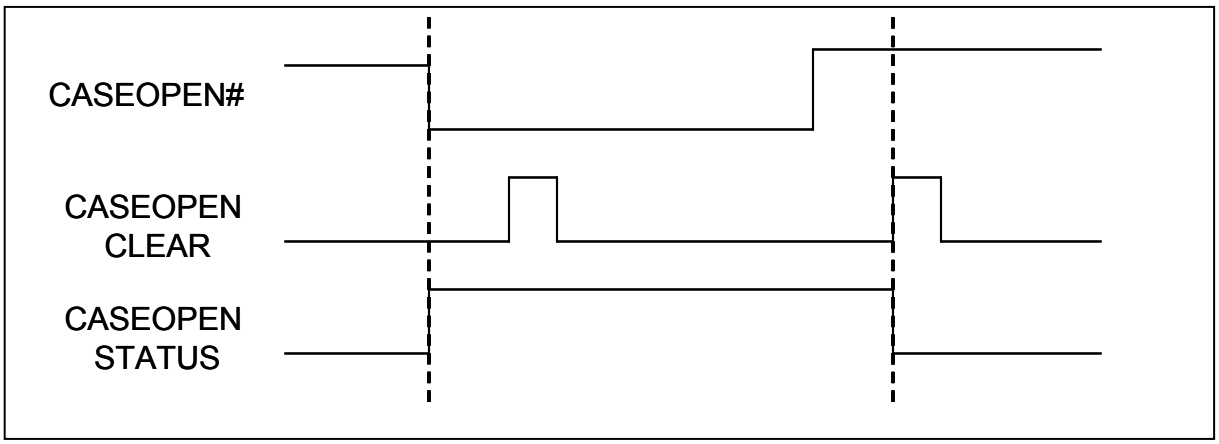


Figure 7-22 Caseopen Mechanism

7.7.4 BEEP Alarm Function

The W83627UHG provides an alarm output function at the BEEP/GP21 pin. The BEEP/GP21 pin is a multi-function pin and can be configured as BEEP output, if Logical Device B, CR[F2h], bit 1 is set to zero.

The BEEP outputs a warning tone when one of the monitored parameters in the following events is out of the preset range.

- Any voltage input of the eight pins (CPUVCORE, VIN[0..2], 5VCC, AVCC , 5VSB and VBAT) is out of the allowed range;
- Any temperature input of the three pins (SYSTIN and CPUTIN) exceeds the limit;
- Any fan input of the two pins (SYSFANIN and CPUFANIN) exceeds the limit;
- CASEOPEN# input pin is sampled low;
- User-defined bit (Bank 4, Index 53h, bit 5) is written to 1.

The BEEP alarm function is enabled or disabled by the control bit at Hardware Monitor Device, Bank 0, Index 57h, bit 7. Also, each event has their individual enable bit at Hardware Monitor Device, Bank 0, Index 56h bit[7:0], Index 57h bit[6:0] and Bank 4, Index 53h, bit[1:0].

BEEP/GP21 is an open-drain output pin and its default state is low. When the BEEP alarm function is activated, this pin repeatedly outputs 600 Hz square wave for 0.5 second and 1.2 KHz square wave for 0.5 second in turn until the enable bit or the abnormal event is cleared.

8. HARDWARE MONITOR REGISTER SET

The base address of the Address Port and Data Port is specified in registers CR[60h] and CR[61h] of Logical Device B, the hardware monitor device. CR[60h] is the high byte, and CR[61h] is the low byte. The Address Port and Data Port are located at the base address, plus 5h and 6h, respectively. For example, if CR[60h] is 02h and CR[61h] is 90h, the Address Port is at 0x295h, and the Data Port is at 0x296h.

Remember that this access is from the host CPU I/O address range. To conserve space in the crowded CPU I/O addresses, many of the hardware monitor registers are “banked” with the bank number located at Index 4Eh. Indexes from 000h to 04Fh are “global” or accessible from all banks, while indexes 050h to 0FFh are specific to each bank.

8.1 Address Port (Port x5h)

Attribute: Bit 6:0 Read/Write , Bit 7: Reserved

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	DATA							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**RESERVED.**
6-0	**READ/WRITE.**

BIT	7	6	5	4	3	2	1	0
ADDRESS	Reserved	A6	A5	A4	A3	A2	A1	A0
DEFAULT	0	00h (Address Pointer)						

8.2 Data Port (Port x6h)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	DATA							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	Data to be read from or to be written to Value RAM and Register.

8.3 SYSFANOUT PWM Output Frequency Configuration Register - Index 00h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL1	PWM_SCALE1						
DEFAULT	0	0	0	0	0	1	0	0

The register is meaningful only when SYSFANOUT is programmed for PWM output (i.e., Bank0 Index 04h, bit 0 is 0).

BIT	DESCRIPTION
7	**PWM_CLK_SEL1 (SYSFANOUT PWM Input Clock Source Select).** This bit selects clock source for PWM output frequency. 0: The clock source is 24 MHz. 1: The clock source is 180 KHz.
6-0	**PWM_SCALE1 (SYSFANOUT PWM Pre-Scale Divider).** The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. $\text{PWM output frequency} = \frac{\text{Input Clock}}{\text{Pre\_Scale Divider}} * \frac{1}{256}$ The maximum value of the divider is 127 (7Fh), and it should not be set to 0.

8.4 SYSFANOUT Output Value Select Register - Index 01h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Value							
DEFAULT	Strap by FAN_SET (Pin 119)							

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output (Bank 0, Index 04h, bit 0 is 0)	DESCRIPTION	The PWM duty cycle is equal to this 8-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
	DEFAULT	Strap by FAN_SET (Pin 119)							
DC Voltage Output (Bank 0, Index 04h, bit 0 is 1)	DESCRIPTION	SYSFANOUT voltage control. The output voltage is calculated according to this equation: **OUTPUT Voltage =** $AVCC * \frac{FANOUT}{64}$						Reserved	
	DEFAULT	Strap by FAN_SET (Pin 119)							

8.5 CPUFANOUT PWM Output Frequency Configuration Register - Index 02h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL2	PWM_SCALE2						
DEFAULT	0	0	0	0	0	1	0	0

The register is meaningful only when CPUFANOUT is programmed for PWM output.

BIT	DESCRIPTION
7	**PWM_CLK_SEL2 (CPUFANOUT PWM Input Clock Source Select).** This bit selects the clock source for PWM output. 0: The clock source is 24 MHz. 1: The clock source is 180 KHz.
6-0	**PWM_SCALE2 (CPUFANOUT PWM Pre-Scale Divider).** The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. **PWM output frequency =** $\frac{\text{Input Clock}}{\text{Pre\_Scale Divider}} * \frac{1}{256}$ The maximum value of the divider is 127 (7Fh), and it should not be set to 0.

8.6 CPUFANOUT Output Value Select Register - Index 03h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT0 Value							
DEFAULT	Strap by FAN_SET (Pin 119)							

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output (Bank 0, Index 04h, bit 1 is 0)	DESCRIPTION	CPUFANOUT PWM Duty. The PWM duty cycle is equal to this 8-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and creates a duty cycle of 0%.							
	DEFAULT	Strap by FAN_SET (Pin 119)							
DC Voltage Output (Bank 0, Index 04h, bit 1 is 1)	DESCRIPTION	CPUFANOUT Voltage Control. The output voltage is calculated according to this equation: **OUTPUT Voltage =** $AVCC * \frac{FANOUT}{64}$						Reserved	
	DEFAULT	Strap by FAN_SET (Pin 119)							

8.7 FAN Configuration Register I - Index 04h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		CPUFANOUT_MODE		SYSFAMOUT_MODE		CPUFANOUT_SEL	SYSFANOUT_SEL
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-6	**RESERVED.**
5-4	**CPUFANOUT_MODE.** CPUFANOUT mode control. **Bits** **5 4** 0 0: CPUFANOUT is in Manual Mode. (Default) 0 1: CPUFANOUT is in Thermal Cruise™ Mode. 1 0: CPUFANOUT is in Fan Speed Cruise™ Mode. 1 1: CPUFANOUT is in SMARTFAN™ III Mode.
3-2	**SYSFANOUT_MODE.** SYSFANOUT mode control. **Bits** **3 2** 0 0: SYSFANOUT is as Manual Mode. (Default) 0 1: SYSFANOUT is as Thermal Cruise™ Mode. 1 0: SYSFANOUT is as Fan Speed Cruise™ Mode. 1 1: Reserved and no function.
1	**CPUFANOUT_SEL.** CPUFANOUT output selection. 0: CPUFANOUT pin produces a PWM output duty cycle. (Default) 1: CPUFANOUT pin produces DC output.
0	**SYSFANOUT_SEL.** SYSFANOUT output mode selection. 0: SYSFANOUT pin produces a PWM duty cycle output. 1: SYSFANOUT pin produces a DC output. (Default)

8.8 SYSTIN Target Temperature Register/ SYSFANIN Target Speed Register - Index 05h (Bank 0)

Attribute: Read/Write
Size: 8 bits

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™	DESCRIPTION	Reserved	SYSTIN Target Temperature						
	DEFAULT	0	0	0	0	0	0	0	0
Fan Speed Cruise™	DESCRIPTION	SYSFANIN Target Speed							
	DEFAULT	0	0	0	0	0	0	0	0

8.9 CPUTIN Target Temperature Register/ CPUFANIN Target Speed Register - Index 06h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUTIN Target Temperature / CPUFANIN Target Speed							
DEFAULT	0	0	0	0	0	0	0	0

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™ or SMART FAN™ III	DESCRIPTION	Reserved	CPUTIN Target Temperature						
	DEFAULT	0	0	0	0	0	0	0	0
Fan Speed Cruise™	DESCRIPTION	CPUFANIN Target Speed							
	DEFAULT	0	0	0	0	0	0	0	0

8.10 Tolerance of Target Temperature or Target Speed Register - Index 07h (Bank 0)

Attribute: Read/Write
Size: 8 bits

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™ or SMART FAN™ III	DESCRIPTION	Tolerance of CPUTIN Target Temperature				Tolerance of SYSTIN Target Temperature			
	DEFAULT	0	0	0	0	0	0	0	0
Fan Speed Cruise™	DESCRIPTION	Tolerance of CPUFANIN Target Speed				Tolerance of SYSFANIN Target Speed			
	DEFAULT	0	0	0	0	0	0	0	0

8.11 SYSFANOUT Stop Value Register - Index 08h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Stop Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise™ mode, the SYSFANOUT value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

8.12 CPUFANOUT Stop Value Register - Index 09h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Stop Value							
DEFAULT	0	0	0	0	0	0	0	1

InThermal Cruise™ mode or SMART FAN™ III mode, the CPUFANOUT value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

8.13 SYSFANOUT Start-up Value Register - Index 0Ah (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Start-up Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise™ mode, SYSFANOUT value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan.

8.14 CPUFANOUT Start-up Value Register - Index 0Bh (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Start-up Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise ™ mode, CPUFANOUT value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan.

8.15 SYSFANOUT Stop Time Register - Index 0Ch (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Stop Time							
DEFAULT	0	0	1	1	1	1	0	0

In Thermal Cruise™ mode, if the stop value is enabled, this register determines the amount of time it takes the SYSFANOUT value to fall from the stop value to zero.

(1)For PWM output:

The units are intervals of 0.1 seconds. The default time is 6 seconds.

(2)For DC output:

The units are intervals of 0.4 seconds. The default time is 24 seconds.

8.16 CPUFANOUT Stop Time Register - Index 0Dh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Stop Time							
DEFAULT	0	0	1	1	1	1	0	0

In Thermal Cruise™ mode or SMART FAN™ III mode, this register determines the amount of time it takes the CPUFANOUT value to fall from the stop value to zero.

(1)For PWM output:

The units are intervals of 0.1 seconds. The default time is 6 seconds.

(2)For DC output:

The units are intervals of 0.4 seconds. The default time is 24 seconds.

8.17 Fan Output Step Down Time Register - Index 0Eh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANOUT Value Step Down Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time it takes FANOUT to decrease its value by one step.
(1)For PWM output:
The units are intervals of 0.1 seconds. The default time is 1 seconds.
(2)For DC output:
The units are intervals of 0.4 seconds. The default time is 4 seconds.

8.18 Fan Output Step Up Time Register - Index 0Fh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANOUT Value Step Up Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time it takes FANOUT to increase its value by one step.
(1)For PWM output:
The units are intervals of 0.1 second. The default time is 1 seconds.
(2)For DC output:
The units are intervals of 0.4 second. The default time is 4 seconds.

8.19 Reserved Registers - Index 10h (Bank 0)

8.20 Reserved Registers - Index 11h (Bank 0)

8.21 FAN Configuration Register II - Index 12h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED.		SYSFANOUT_MIN_VALUE	CPUFANOUT_MIN_VALUE	RESERVED			
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-6	**RESERVED.**
5	**SYSFANOUT_MIN_VALUE.** 0: SYSFANOUT value decreases to zero when the temperature goes below the target range. 1: SYSFANOUT value decreases to the value specified in Index 08h when the temperature goes below the target range.

Continued

BIT	DESCRIPTION
4	**CPUFANOUT_MIN_VALUE.** 0: CPUFANOUT value decreases to zero when the temperature goes below the target range. 1: CPUFANOUT value decreases to the value specified in Index 09h when the temperature goes below the target range.
3-0	**RESERVED.**

8.22 Reserved Registers - Index 13h (Bank 0)

8.23 Reserved Registers - Index 14h (Bank 0)

8.24 Reserved Registers - Index 15h (Bank 0)

8.25 Reserved Registers - Index 16h (Bank 0)

8.26 Reserved Registers - Index 17h (Bank 0)

8.27 OVT# Configuration Register - Index 18h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	DIS_OVT1	RESERVED	OVT1_MODE	RESERVED			
DEFAULT	0	1	0	0	0	0	1	1

BIT	DESCRIPTION
7	**RESERVED.**
6	**DIS_OVT1.** 0: Enable SYSTIN OVT# output. 1: Disable temperature sensor SYSTIN over-temperature (OVT#) output.
5	**RESERVED.**
4	**OVT1_MODE.** 0: Compare Mode. (Default) 1: Interrupt Mode.
3-0	**RESERVED.**

8.28 Reserved Registers - Index 19h ~ 1Fh (Bank 0)

8.29 Value RAM — Index 20h ~ 3Fh (Bank 0)

ADDRESS A6-A0	DESCRIPTION
20h	CPUVCORE reading
21h	VIN0 reading
22h	AVCC reading
23h	5VCC reading
24h	VIN1 reading
25h	VIN2 reading
26h	Reserved
27h	SYSTIN temperature sensor reading
28h	SYSFANIN reading Note: This location stores the number of counts of the internal clock per revolution.
29h	CPUFANIN reading Note: This location stores the number of counts of the internal clock per revolution.
2Ah	Reserved
2Bh	CPUVCORE High Limit
2Ch	CPUVCORE Low Limit
2Dh	VIN0 High Limit
2Eh	VIN0 Low Limit
2Fh	AVCC High Limit
30h	AVCC Low Limit
31h	5VCC High Limit
32h	5VCC Low Limit
33h	VIN1 High Limit
34h	VIN1 Low Limit
35h	VIN2 High Limit
36h	VIN2 Low Limit
37h	Reserved
38h	Reserved
39h	SYSTIN temperature sensor High Limit

Value RAM — Index 20h ~ 3Fh (Bank 0), continued

ADDRESS A6-A0	DESCRIPTION
3Ah	SYSTIN temperature sensor Hysteresis Limit
3Bh	SYSFANIN Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.
3Ch	CPUFANIN Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.
3Dh	Reserved
3Eh	Reserved
3Fh	Reserved

8.30 Configuration Register - Index 40h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	INITIALIZATION	RESERVED			INT_CLEAR	RESERVED	SMI#ENABLE	START
DEFAULT	0	0	0	0	0	0	1	1

BIT	DESCRIPTION
7	**INITIALIZATION.** A one restores the power-on default values to some registers. This bit clears itself since the power-on default value of this bit is zero.
6-4	**RESERVED.**
3	**INT_CLEAR.** A one disables the SMI# output without affecting the contents of Interrupt Status Registers. The device will stop monitoring. It will resume upon clearing of this bit.
2	**RESERVED.**
1	**SMI#ENABLE.** A one enables the SMI# Interrupt output.
0	**START.** A one enables startup of monitoring operations. A zero puts the part in standby mode.

Note: The outputs of Interrupt pins will not be cleared if the user writes a zero to this location after an interrupt has occurred unlike "INT_Clear" bit.

8.31 Interrupt Status Register 1 - Index 41h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN	SYSFANIN	CPUTIN	SYSTIN	5VCC	AVCC	VIN0	CPUVCORE
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**CPUFANIN.** A one indicates that the fan count limit of CPUFANIN has been exceeded.
6	**SYSFANIN.** A one indicates the fan count limit of SYSFANIN has been exceeded.
5	**CPUTIN.** A one indicates the high limit of CPUTIN temperature has been exceeded.
4	**SYSTIN.** A one indicates the high limit of SYSTIN temperature has been exceeded.
3	**5VCC.** A one indicates the high or low limit of 5VCC has been exceeded.
2	**AVCC (PIN 97).** A one indicates the high or low limit of AVCC has been exceeded.
1	**VIN0.** A one indicates the high or low limit of VIN0 has been exceeded.
0	**CPUVCORE.** A one indicates the high or low limit of CPUVCORE has been exceeded.

8.32 Interrupt Status Register 2 - Index 42h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TAR2	TAR1	RESERVED	CASEOPEN	RESERVED	VIN2	RESERVED	VIN1
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**TAR2.** A one indicates that the CPUTIN temperature has been over the target temperature for three minutes at full fan speed in the Thermal Cruise™ mode.
6	**TAR1.** A one indicates that the SYSTIN temperature has been over the target temperature for three minutes at full fan speed in the Thermal Cruise™ mode.
5	**RESERVED.**
4	**CASEOPEN.** A one indicates that the case has been opened.
3	**RESERVED.**
2	**VIN2.** A one indicates the high or low limit of VIN2 has been exceeded.
1	**RESERVED.**
0	**VIN1.** A one indicates the high or low limit of VIN1 has been exceeded.

8.33 SMI# Mask Register 1 - Index 43h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN	SYSFANIN	CPUTIN	SYSTIN	5VCC	AVCC (PIN 97)	VIN0	CPUVCORE
DEFAULT	1	1	0	1	1	1	1	0

BIT	DESCRIPTION	
7	**CPUFANIN.**	A one disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt. (See Interrupt Status Register 1 – Index 41h (Bank 0)).
6	**SYSFANIN.**	
5	**CPUTIN.**	
4	**SYSTIN.**	
3	**5VCC.**	
2	**AVCC (PIN 97).**	
1	**VIN0.**	
0	**CPUVCORE.**	

8.34 SMI# Mask Register 2 - Index 44h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TAR1	TAR2	RESERVED	CASEOPEN	RESERVED		VIN2	VIN1
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION	
7	TAR2	A one disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt. (Please see Interrupt Status Register 2 – Index 42h (Bank 0)).
6	TAR1	
5	RESERVED	
4	CASEOPEN	
3-2	RESERVED	
1	VIN2	
0	VIN1	

8.35 Reserved Register - Index 45h (Bank 0)

8.36 SMI# Mask Register 3 - Index 46h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CASEOPEN CLEAR	RESERVED						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**CASEOPEN CLEAR.** Caseopen Clear Control. Write 1 to this bit will clear CASEOPEN status. This bit will be self-cleared after an event is cleared. The function is the same as LDA, CR[E6h] bit 5.
6-0	**RESERVED.**

8.37 Fan Divisor Register I - Index 47h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN DIV_B1	CPUFANIN DIV_B0	SYFANIN DIV_B1	SYSFANIN DIV_B0	RESERVED			
DEFAULT	0	1	0	1	0	1	0	1

BIT	DESCRIPTION	
7	**CPUFANIN DIV_B1 (CPUFANIN Divisor).**	Please see VBAT Monitor Control Register – Index 5Dh (Bank 0).
6	**CPUFANIN CIV_B0 (CPUFANIN Divisor).**	
5	**SYSFANIN DIV_B1 (SYSFANIN Divisor).**	
4	**SYSFANIN DIV_B0 (SYSFANIN Divisor).**	
3-0	**RESERVED.**	

8.38 Serial Bus Address Register - Index 48h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	SERIAL BUS ADDRESS						
DEFAULT	0	0	1	0	1	1	0	1

BIT	DESCRIPTION
7	**RESERVED (Read Only).**
6-0	**Serial Bus Address <7:1>.**

8.39 CPUFANOUT monitor Temperature source select register - Index 49h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED					CPUFANOUT TEMP_SEL[2]	CPUFANOUT TEMP_SEL[1]	CPUFANOUT TEMP_SEL[0]
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION	
7-3	**RESERVED.**	
2	**CPUFANOUT TEMP_SEL[2].**	CPUFANOUT Temperature Source Select. **Bits** **2 1 0** 0 0 0: Select CPUTIN as CPUFANOUT Monitor Source. (Default) 0 0 1: Reserved. 0 1 0: Select PECI Agent 1 as CPUFANOUT monitor source. 0 1 1: Select PECI Agent 2 as CPUFANOUT monitor source. 1 0 0: Select PECI Agent 3 as CPUFANOUT monitor source. 1 0 1: Select PECI Agent 4 as CPUFANOUT monitor source.
1	**CPUFANOUT TEMP_SEL[1].**	
0	**CPUFANOUT TEMP_SEL[0].**	

8.40 SYSFANOUT monitor Temperature source select register - Index 4Ah (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT TEMP_SEL[2]	SYSFANOUT TEMP_SEL[1]	SYSFANOUT TEMP_SEL[0]	RESERVED				
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION	
7	**SYSFANOUT TEMP_SEL[2].**	SYSFANOUT Temperature Source Select. **Bits** **7 6 5** 0 0 0: Select SYSTIN as SYSFANOUT monitor source. (Default) 0 0 1: Select CPUTIN as SYSFANOUT monitor source. 0 1 0: Reserved. 0 1 1: Reserved. 1 0 0: Select PECI Agent 1 as SYSFANOUT monitor source. 1 0 1: Select PECI Agent 2 as SYSFANOUT monitor source. 1 1 0: Select PECI Agent 3 as SYSFANOUT monitor source. 1 1 1: Select PECI Agent 4 as SYSFANOUT monitor source.
6	**SYSFANOUT TEMP_SEL[1].**	
5	**SYSFANOUT TEMP_SEL[0[.**	
4-0	**RESERVED.**	

8.41 Fan Divisor Register II - Index 4Bh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		ADCOVSEL		RESERVED			
DEFAULT	0	1	0	0	0	1	0	0

BIT	DESCRIPTION
7-6	**RESERVED.**
5-4	**ADCOVSEL (A/D Converter Clock Input Select).** **Bits** **5 4** 0 0: ADC clock select 22.5 KHz. (Default) 0 1: ADC clock select 5.6 KHz. (22.5K/4) 1 0: ADC clock select 1.4 KHz. (22.5K/16) 1 1: ADC clock select 0.35 KHz. (22.5K/64)
3-2	**RESERVED.** These two bits should be set to the default value 01h.
1-0	**RESERVED.**

8.42 SMI#/OVT# Control Register - Index 4Ch (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	T2T3_INT MODE	EN_T1_ONE	RESERVED	DIS_OVT2	OVTPOL	RESERVED	
DEFAULT	0	0	0	1	0	0	0	0

BIT	DESCRIPTION
7	**RESERVED.**
6	**T2T3_INT MODE.** 1: SMI# output type of Temperature CPUTIN is in Comparator Interrupt mode. 0: SMI# output type is in Two-time Interrupt mode. (Default)
5	**EN_T1_ONE.** 1: SMI# output type of temperature SYSTIN is One-time Interrupt mode. 0: SMI# output type is Two-time Interrupt mode.
4	**RESERVED.**
3	**DIS_OVT2**. 1: Disable temperature sensor CPUTIN over-temperature (OVT) output. 0: Enable CPUTIN OVT output through pin OVT#. (Default)
2	**OVTPOL (Over-temperature polarity).** 1: OVT# is active high. 0: OVT# is active low. (Default)
1-0	**RESERVED.**

8.43 FAN IN/OUT Control Register - Index 4Dh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED				FANOPV2	FANINC2	FANOPV1	FANNC1
DEFAULT	1	0	0	1	0	1	0	1

BIT	DESCRIPTION
7-4	**RESERVED.**
3	**FANOPV2 (CPUFANIN output value, only if bit 2 is set to zero).** 1: Pin 112 (CPUFANIN) generates a logic-high signal. 0: Pin 112 generates a logic-low signal. (Default)
2	**FANINC2 (CPUFANIN Input Control).** 1: Pin 112 (CPUFANIN) acts as a FAN tachometer input. (Default) 0: Pin 112 acts as a FAN control signal, and the output value is set by bit 3.
1	**FANOPV1 (SYSFANIN output value, only if bit 0 is set to zero).** 1: Pin 113 (SYSFANIN) generates a logic-high signal. 0: Pin 113 generates a logic-low signal. (Default)
0	**FANINC1 (SYSFANIN Input Control).** 1: Pin 113 (SYSFANIN) acts as a FAN tachometer input. (Default) 0: Pin 113 acts as a FAN control signal, and the output value is set by bit 1.

8.44 Register 50h ~ 5Fh Bank Select Register - Index 4Eh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	HBACS	RESERVED				BANKSEL2	BANKSEL1	BANKSEL0
DEFAULT	1	0	0	0	0	0	0	0

BIT	DESCRIPTION	
7	**HBACS (High Byte Access).** 1: Access Index 4Fh high-byte register. (Default) 0: Access Index 4Fh low-byte register.	
6	**RESERVED.** This bit should not be set to zero.	
5-4	**RESERVED.**	
3	**RESERVED.** This bit should not be set to zero.	
2	**BANKSEL2.**	Bank Select for Index Ports 0x50h~0x5Fh. The three-bit binary value corresponds to the bank number. For example, “010” selects bank 2.
1	**BANKSEL1.**	
0	**BANKSEL0.**	

8.45 Winbond Vendor ID Register - Index 4Fh (Bank 0)

Power on Default Value: <15:0> = 5CA3h
Attribute: Read Only
Size: 16 bits

BIT	15	14	13	12	11	10	9	8
NAME	VIDL							
DEFAULT	0	1	0	1	1	1	0	0

BIT	7	6	5	4	3	2	1	0
NAME	VIDH							
DEFAULT	1	0	1	0	0	0	1	1

BIT	DESCRIPTION
15-8	Vendor ID High-Byte, if Index 4Eh, bit7 is 1. Default 5Ch.
7-0	Vendor ID Low Byte, if Index 4Eh, bit 7 is 0. Default A3h.

8.46 Reserved Register - Index 50h ~ 55h (Bank 0)

8.47 BEEP Control Register 1 - Index 56h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	EN_ CPUFANIN _BP	EN_ SYSFANIN _BP	EN_ CPUTIN _BP	EN_ SYSTIN _BP	EN_ 5VCC _BP	EN_ AVCC _BP	EN_ VIN0 _BP	EN_ CPUVCORE _BP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION	
7	**EN_CPUFANIN_BP.** BEEP output control for CPUFANIN if the monitored value exceeds the limit.	1: Enable BEEP output. 0: Disable BEEP output. (Default)
6	**EN_SYSFANIN_BP.** BEEP output control fro SYSFANIN if the monitored value exceeds the limit.	
5	**EN_CPUTIN_BP.** BEEP output control for temperature CPUTIN if the monitored value exceeds the limit.	

Continued

BIT	DESCRIPTION
4	**EN_SYSTIN_BP.** BEEP output control for temperature SYSTIN if the monitored value exceeds the limit.
3	**EN_5VCC_BP.** BEEP output control for 5VCC if the monitored value exceeds the limit.
2	**EN_AVCC_BP.** BEEP output control for AVCC if the monitored value exceeds the limit.
1	**EN_VIN0_BP.** BEEP output control for VIN0 if the monitored value exceeds the limit.
0	**EN_CPUVCORE_BP.** BEEP output control for CPUVCORE if the monitored value exceeds the limit.

8.48 BEEP Control Register 2 - Index 57h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	EN_GBP	RESERVED		EN_CASEOPEN_BP	RESERVED		EN_VIN2_BP	EN_VIN1_BP
DEFAULT	1	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**EN_GBP.** Global BEEP Control. 1: Enable global BEEP output. (Default) 0: Disable all BEEP output.
6-5	**RESERVED.**
4	**EN_CASEOPEN_BP.** BEEP output control for CASEOPEN if the case has been opened. 1: Enable BEEP output. 0: Disable BEEP output. (Default)
3-2	**RESERVED.**
1	**EN_VIN2_BP.** BEEP output control for VIN2 if the monitored value exceeds the limit. 1: Enable BEEP output. 0: Disable BEEP output. (Default)
0	**EN_VIN1_BP.** BEEP output control for VIN1 if the monitored value exceeds the limit. 1: Enable BEEP output. 0: Disable BEEP output. (Default)

8.49 Chip ID - Index 58h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CHIPID							
DEFAULT	1	1	0	0	0	0	0	1

BIT	DESCRIPTION
7-0	Winbond Chip ID Number. Default C1h.

8.50 Diode Selection Register - Index 59h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		SELPIIV2	SELPIIV1	RESERVED			
DEFAULT	0	1	1	1	0	0	0	0

BIT	DESCRIPTION
7-6	**RESERVED.**
5	**SELPIIV2.** Diode mode selection for temperature CPUTIN, if Index 5Dh, bit 2 is set to 1. 1: CPU-compatible thermal diode. 0: Reserved.
4	**SELPIIV1.** Diode mode selection for temperature SYSTIN, if Index 5Dh, bit 1 is set to 1. 1: CPU-compatible thermal diode. 0: Reserved.
3-0	**RESERVED.**

8.51 Reserved Register - Index 5Ah ~ 5Ch (Bank 0)

8.52 VBAT Monitor Control Register - Index 5Dh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	CPUFANIN DIV_B2	SYSFANIN DIV_B2	RESERVED		DIODES2	DIODES1	EN_ VBAT_MNT
DEFAULT	0	0	0	0	0	1	0	0

BIT	DESCRIPTION
7	**RESERVED.**
6	**CPUFANIN DIV_B2.** CPUFANIN Divisor, bit 2.
5	**SYSFANIN DIV_B2.** SYSFANIN Divisor, bit 2.
4-3	**RESERVED.**
2	**DIODES2.** Sensor type selection for CPUTIN. 1: Diode sensor. 0: Thermistor sensor.
1	**DIODES1.** Sensor type selection for SYSTIN. 1: Diode sensor. 0: Thermistor sensor.
0	**EN_VBAT_MINT.** 1: Enable battery voltage monitor. When this bit changes from zero to one, it takes one monitor cycle time to update the VBAT reading value register. 0: Disable battery voltage monitor.

Fan divisor table:

BIT 2	BIT 1	BIT 0	FAN DIVISOR	BIT 2	BIT 1	BIT 0	FAN DIVISOR
0	0	0	**1**	1	0	0	**16**
0	0	1	**2**	1	0	1	**32**
0	1	0	**4**	1	1	0	**64**
0	1	1	**8**	1	1	1	**128**

8.53 Critical Temperature enable register - Index 5Eh (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		EN_CPUFAN OUT CRITICAL TEMP	EN_SYSFANOUT CRITICAL TEMP	RESERVED	EN_CPUTIN CURRENT MODE	EN_SYSTIN CURRENT MODE	RESERVED
DEFAULT	0	0	0	0	0	1	0	0

BIT	DESCRIPTION
7-6	**RESERVED.**
5	**EN_CPUFANOUT CRITICAL TEMP.** 1: Enable CPUFANOUT critical temperature protection. 0: Disable CPUFANOUT critical temperature protection. (Default)
4	**EN_SYSFANOUT CRITICAL TEMP.** 1: Enable SYSFANOUT critical temperature protection. 0: Disable SYSFANOUT critical temperature protection. (Default)
3	**RESERVED.**
2	**EN_CPUTIN CURRENT MODE.** Enable CPUTIN Current Mode. 1: Temperature sensing of CPUTIN by Current Mode. (Default) 0: Temperature sensing of CPUTIN depends on setting of Index 5Dh and 59h. (Default)
1	**EN_SYSTIN CURRENT MODE.** Enable SYSTIN Current Mode. 1: Temperature sensing of SYSTIN by Current Mode. 0: Temperature sensing of SYSTIN depends on setting of Index 5Dh and 59h. (Default)
0	**RESERVED.**

8.54 Reserved Register - Index 5Fh (Bank 0)

8.55 Reserved Registers - Index 60h (Bank 0)

8.56 Reserved Registers - Index 61h (Bank 0)

8.57 Reserved Registers - Index 62h (Bank 0)

8.58 Reserved Registers - Index 63h (Bank 0)

8.59 Reserved Registers - Index 64h (Bank 0)

8.60 Reserved Registers - Index 65h (Bank 0)

8.61 Reserved Registers - Index 66h (Bank 0)

8.62 CPUFANOUT Maximum Output Value Register - Index 67h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Max. Value							
DEFAULT	1	1	1	1	1	1	1	1

In SMART FAN™ III mode, the CPUFANOUT value increases to this value. This value cannot be zero, and it cannot be lower than the CPUFANOUT Stop value.

8.63 CPUFANOUT Output Step Value Register - Index 68h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT STEP							
DEFAULT	0	0	0	0	0	0	0	1

In SMART FAN™ III mode, the CPUFANOUT value decreases or increases by this eight-bit value, when needed.

8.64 Reserved Registers - Index 69h (Bank 0)

8.65 Reserved Registers - Index 6Ah (Bank 0)

8.66 SYSFANOUT Critical Temperature register - Index 6Bh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT CRITICAL TEMPERATURE							
DEFAULT	1	1	1	1	1	1	1	1

In Thermal Cruise™ mode, when SYSFANOUT critical temperature is enabled and monitor temperature over the critical temperature then SYSFANOUT will full drive.

8.67 CPUFANOUT Critical Temperature register - Index 6Ch (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT CRITICAL TEMPERATURE							
DEFAULT	1	1	1	1	1	1	1	1

In Thermal Cruise™ mode, when CPUFANOUT critical temperature is enabled and monitor temperature over the critical temperature then CPUFANOUT will full drive.

8.68 Reserved Registers - Index 6Dh (Bank 0)

8.69 Reserved Registers - Index 6Eh (Bank 0)

8.70 CPUTIN/PECI Temperature (High Byte) Register - Index 50h (Bank 1)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<8:1>							

BIT	DESCRIPTION
7-0	**TEMP<8:1>.**Temperature <8:1> of the CPUTIN/PECI sensor. The nine-bit value is in units of 0.5°C.

(See CPUFANOUT monitor Temperature source select register – Index 49h(Bank 0))

8.71 CPUTIN/PECI Temperature (Low Byte) Register - Index 51h (Bank 1)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<0>	RESERVED						

BIT	DESCRIPTION
7	**TEMP<0>.** Temperature <0> of the CPUTIN/PECI sensor. The nine-bit value is in units of 0.5°C.
6-0	**RESERVED.**

(See CPUFANOUT monitor Temperature source select register – Index 49h(Bank 0))

8.72 CPUTIN Configuration Register - Index 52h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FAULT		RESERVED	OVTMOD	STOP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**RESERVED.** These bits should be set to 0.
4-3	**FAULT.** Number of faults to detect before setting OVT# output. This avoids false tripping due to noise.
2	**RESERVED.** This bit should be set to 0.
1	**OVTMOD.** OVT# mode select. 0: Compared mode. (Default) 1: Interrupt mode.
0	**STOP.** 0: Monitor CPUTIN. 1: Stop monitoring CPUTIN.

8.73 CPUTIN Hysteresis (High Byte) Register - Index 53h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST<8:1>							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION
7-0	**THYST<8:1>.** Hysteresis temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 75°C.

8.74 CPUTIN Hysteresis (Low Byte) Register - Index 54h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST<0>	RESERVED						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**THYST<0>.** Hysteresis temperature bit 0. The nine-bit value is in units of 0.5°C.
6-0	**RESERVED.**

8.75 CPUTIN Over-temperature (High Byte) Register - Index 55h (Bank1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<8:1>							
DEFAULT	0	1	0	1	0	0	0	0

BIT	DESCRIPTION
7-0	**TOVF<8:1>.** Over-temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 80°C.

8.76 CPUTIN Over-temperature (Low Byte) Register - Index 56h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<0>	RESERVED						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**TOVF<0>.** Over-temperature bit 0. The nine-bit value is in units of 0.5°C.
6-0	**RESERVED.**

8.77 SYSTIN/CPUTIN/PECI Temperature (High Byte) Register - Index 50h (Bank 2)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<8:1>							

BIT	DESCRIPTION
7-0	**TEMP<8:1>.** Temperature <8:1> of the SYSTIN/CPUTIN/PECI sensor. The nine-bit value is in units of 0.5°C.

(See SYSFANOUT monitor Temperature source select register – Index 4Ah(Bank 0))

8.78 SYSTIN/CPUTIN/PECI Temperature (Low Byte) Register – Index 51h (Bank 2)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<0>	RESERVED						

BIT	DESCRIPTION
7	**TEMP<0>.** Temperature <0> of the SYSTIN/CPUTIN/PECI sensor. The nine-bit value is in units of 0.5°C.
6-0	**RESERVED.**

(See SYSFANOUT monitor Temperature source select register – Index 4Ah(Bank 0))

8.79 Reserved Registers – Index 52h (Bank 2)

8.80 Reserved Registers – Index 53h (Bank 2)

8.81 Reserved Registers – Index 54h (Bank 2)

8.82 Reserved Registers – Index 55h (Bank 2)

8.83 Reserved Registers – Index 56h (Bank 2)

8.84 Interrupt Status Register 3 – Index 50h (Bank 4)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED						VBAT	5VSB
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-2	**RESERVED.**
1	**VBAT.** A one indicates the high or low limit of VBAT has been exceeded.
0	**5VSB.** A one indicates the high or low limit of 5VSB has been exceeded.

8.85 SMI# Mask Register 4 – Index 51h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED						VBAT	5VSB
DEFAULT	0	0	0	1	0	0	1	1

BIT	DESCRIPTION	
7-2	**RESERVED.**	
1	**VBAT.**	A one disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt. (Please see Interrupt Status Register 3 – Index 50h (Bank 4)).
0	**5VSB.**	

8.86 Reserved Register - Index 52h (Bank 4)

8.87 BEEP Control Register 3 - Index 53h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		EN_ USER_BP	RESERVED			EN_ VBAT_BP	EN_ 5VSB_BP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-6	**RESERVED.**
5	**EN_USER_BP.** User-defined BEEP output function. 0: Make BEEP inactive. (Default) 1: Make BEEP active.
4-2	**RESERVED.**
1	**EN_VBAT_BP.** BEEP output control for VBAT if the monitored value exceeds the limit. 1: Enable BEEP output. 0: Disable BEEP output. (Default)
0	**EN_5VSB_BP.** BEEP output control for 5VSB if the monitored value exceeds the limit. 1: Enable BEEP output. 0: Disable BEEP output. (Default)

8.88 SYSTIN Temperature Sensor Offset Register - Index 54h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SYSTIN temperature offset value.** The value in this register is added to the monitored value so that the read value will be the sum of the monitored value and this offset value.

8.89 CPUTIN Temperature Sensor Offset Register - Index 55h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**CPUTIN Temperature Offset Value.** The value in this register will be added to the monitored value so that the read value is the sum of the monitored value and this offset value.

8.90 Reserved Registers - Index 56h (Bank 4)

8.91 Reserved Register - Index 57h-58h (Bank 4)

8.92 Real Time Hardware Status Register I - Index 59h (Bank 4)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN _STS	SYSFANIN _STS	CPUTIN _STS	SYSTIN _STS	5VCC _STS	AVCC _STS	VIN0 _STS	CPUVCORE _STS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**CPUFANIN_STS.** CPUFANIN status. 1: Fan speed count is over the limit value. 0: Fan speed count is in the allowed range.
6	**SYSFANIN_STS.** 1: Fan speed count is over the limit value. 0: Fan speed count is in the allowed range.
5	**CPUTIN_STS.** 1: Temperature exceeds the over-temperature value. 0: Temperature is under the hysteresis value.
4	**SYSTIN_STS.** 1: Temperature exceeds the over-temperature value. 0: Temperature is under the hysteresis value.
3	**5VCC_STS.** 1: 5VCC voltage is over or under the allowed range. 0: 5VCC voltage is in the allowed range.
2	**AVCC_STS.** 1: AVCC voltage is over or under the allowed range. 0: AVCC voltage is in the allowed range.
1	**VIN0_STS.** 1: VIN0 voltage is over or under the allowed range. 0: VIN0 voltage is in the allowed range.
0	**CPUVCORE_STS.** 1: CPUVCORE voltage is over or under the allowed range. 0: CPUVCORE voltage is in the allowed range.

8.93 Real Time Hardware Status Register II - Index 5Ah (Bank 4)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TAR2_STS	TAR1_STS	RESERVED	CASEOPEN_STS	RESERVED			VIN1_STS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**TAR2_STS. Smart Fan of CPUFANIN Warning Status.** 1: Selected temperature has been over the target temperature for three minutes at full speed in Thermal Cruise™ mode. 0: Selected temperature has not reached the warning range.
6	**TAR1_STS. Smart Fan of SYSFANIN Warning Status.** 1: SYSTIN temperature has been over the target temperature for three minutes at full speed in Thermal Cruise™ mode. 0: SYSTIN temperature has not reached the warning range.
5	**RESERVED.**
4	**CASEOPEN_STS. Caseopen Status.** 1: Caseopen is detected and latched. 0: Caseopen is not latched.
3-1	**RESERVED.**
0	**VIN1_STS. VIN1 Voltage Status.** 1: VIN1 voltage is over or under the allowed range. 0: VIN1 voltage is in the allowed range.

8.94 Real Time Hardware Status Register III - Index 5Bh (Bank 4)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		VIN2_STS	RESERVED			VBAT_STS	5VSB_STS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-6	**RESERVED.**
5	**VIN2_STS. VIN2 Voltage Status.** 1: VIN2 voltage is over or under the allowed range. 0: VIN2 voltage is in the allowed range.
4-2	**RESERVED.**
1	**VBAT_STS. VBAT Voltage Status.** 1: VBAT voltage is over or under the allowed range. 0: VBAT voltage is in the allowed range.
0	**5VSB_STS. 5VSB Voltage Status.** 1: 5VSB voltage is over or under the allowed range. 0: 5VSB voltage is in the allowed range.

8.95 Reserved Register - Index 5Ch - 5Fh (Bank 4)

8.96 Value RAM 2 — Index 50h-59h (Bank 5)

ADDRESS A6-A0	DESCRIPTION
50h	5VSB reading
51h	VBAT reading. The reading is meaningless unless EN_VBAT_MN (Bank0 Index 5Dh, bit0) is set.
52h	Reserved
53h	Reserved
54h	5VSB High Limit
55h	5VSB Low Limit
56h	VBAT High Limit
57h	VBAT Low Limit
58h	Reserved
59h	Reserved
5Ah	Reserved
5Bh	Reserved
5Ch	Reserved

8.97 Reserved Register - Index 50h - 57h (Bank 6)

9. FLOPPY DISK CONTROLLER

9.1 FDC Functional Description

The floppy disk controller (FDC) of the W83627UHG integrates all of the logic required for floppy disk control. The FDC implements a FIFO, which provides better system performance in multi-master systems, and the digital data separator supports data rates up to 2 M bits/sec.

The FDC includes the following blocks: Precompensation, Data Rate Selection, Digital Data Separator, FIFO, and FDC Core. The rest of this section discusses these blocks through the following topics: FIFO, Data Separator, Write Precompensation, Perpendicular Recording mode, FDC core, FDC commands, and FDC registers.

9.1.1 FIFO (Data)

The FIFO is 16 bytes in size and has programmable threshold values. All command parameter information and disk data transfers go through the FIFO. Data transfers are governed by the RQM (Request for Master) and DIO (Data Input/Output) bits in the Main Status Register.

The FIFO is defaulted to disabled mode after any form of reset, which maintains PC/AT hardware compatibility. The default values can be changed through the configure command. The advantage of the FIFO is that it allows a larger DMA latency in the system without causing disk errors. The following tables give several examples of the delays with the FIFO. The data are based upon the following formula:

DELAY = THRESHOLD # $\times$ (1 / DATA RATE) * 8 - 1.5 μs

Table 9-1 The Delays of the FIFO

FIFO THRESHOLD	MAXIMUM DELAY UNTIL SERVICING AT 500K BPS
	Data Rate
1 Byte	1 $\times$ 16 μs - 1.5 μs = 14.5 μs
2 Byte	2 $\times$ 16 μs - 1.5 μs = 30.5 μs
8 Byte	8 $\times$ 16 μs - 1.5 μs = 6.5 μs
15 Byte	15 $\times$ 16 μs - 1.5 μs = 238.5 μs
FIFO THRESHOLD	**MAXIMUM DELAY UNTIL SERVICING AT 1M BPS**
	Data Rate
1 Byte	1 $\times$ 8 μs - 1.5 μs = 6.5 μs
2 Byte	2 $\times$ 8 μs - 1.5 μs = 14.5 μs
8 Byte	8 $\times$ 8 μs - 1.5 μs = 62.5 μs
15 Byte	15 $\times$ 8 μs - 1.5 μs = 118.5 μs

At the start of a command, the FIFO is always disabled, and command parameters must be sent based upon the RQM and DIO bit settings in the Main Status Register. When the FDC enters the command execution phase, it clears the FIFO off any data to ensure that invalid data are not transferred.

An overrun or underrun terminates the current command and data transfer. Disk writes complete the current sector by generating a 00 pattern and valid CRC. Reads require the host to remove the remaining data so that the result phase may be entered.

DMA transfers are enabled by the specify command and are initiated by the FDC when the LDRQ pin is activated during a data transfer command.

9.2 Data Separator

The function of the data separator is to lock onto incoming serial read data. When a lock is achieved, the serial front-end logic in the chip is provided with a clock that is synchronized with the read data. The synchronized clock, called the Data Window, is used to internally sample the serial data portion of the bit cell, and the alternate state samples the clock portion. Serial-to-parallel conversion logic separates the read data into clock and data bytes.

The Digital Data Separator (DDS) has three parts: control logic, error adjustment, and speed tracking. The control logic generates RDD and RWD for every pulse input, and any data pulse input is synchronized and then adjusted immediately by error adjustment. A digital integrator keeps track of the speed changes in the input data stream.

9.2.1 Write Precompensation

The write precompensation logic minimizes bit shifts in the RDDATA stream from the disk drive. Shifting of bits is a known phenomenon in magnetic media and depends on the disk media and the floppy drive.

The FDC monitors the bit stream that is being sent to the drive. The data patterns that require precompensation are well known, so, depending on the pattern, the bit is shifted either early or late, relative to the surrounding bits.

9.2.2 Perpendicular Recording Mode

The FDC is also capable of interfacing directly to perpendicular recording floppy drives. Perpendicular recording differs from the traditional longitudinal method in that the magnetic bits are oriented vertically. This scheme packs more data bits into the same area.

FDCs with perpendicular recording drives can read standard 3.5" floppy disks and can read and write perpendicular media. Some manufacturers offer drives that can read and write standard and perpendicular media in a perpendicular media drive.

A single command puts the FDC into perpendicular mode. All other commands operate as they normally do. Perpendicular mode requires a 1 Mbps data rate for the FDC, and, at this data rate, the FIFO manages the host interface bottleneck due to the high speed of data transfer to and from the disk.

9.2.3 FDC Core

The W83627UHG FDC is capable of performing twenty commands. Each command is initiated by a multi-byte transfer from the microprocessor, and the result may be a multi-byte transfer back to the microprocessor. Each command consists of three phases: command, execution, and result.

Command

The microprocessor issues all required information to the controller to perform a specific operation.

Execution

The controller performs the specified operation.

Result

After the operation is completed, status information and other housekeeping information are provided to the microprocessor.

The next section introduces each of the commands.

9.2.4 FDC Commands

Command Symbol Descriptions:

C:	Cylinder Number 0 - 256
D:	Data Pattern
DIR:	Step Direction DIR = 0: step out DIR = 1: step in
DS0:	Disk Drive Select 0
DS1:	Disk Drive Select 1
DTL:	Data Length
EC:	Enable Count
EFIFO:	Enable FIFO
EIS:	Enable Implied Seek
EOT:	End of Track
FIFOTHR:	FIFO Threshold
GAP:	Gap Length Selection
GPL:	Gap Length
H:	Head Number
HDS:	Head Number Select
HLT:	Head Load Time
HUT:	Head Unload Time
LOCK:	Lock EFIFO, FIFOTHR, and PTRTRK bits to prevent being affected by software reset
MFM:	MFM or FM Mode
MT:	Multitrack
N:	The number of data bytes written in a sector
NCN:	New Cylinder Number

ND: Non-DMA Mode
OW: Overwritten
PCN: Present Cylinder Number
POLL: Polling Disable
PRETRK: Precompensation Start Track Number
R: Record
RCN: Relative Cylinder Number
R/W: Read/Write
SC: Sectors per Cylinder
SK: Skip deleted data address mark
SRT: Step Rate Time
ST0: Status Register 0
ST1: Status Register 1
ST2: Status Register 2
ST3: Status Register 3
WG: Write gate alters timing of WE

(1) Read Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	0	1	1	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(2) Read Deleted Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	1	1	0	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(3) Read A Track

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	0	0	1	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system; FDD reads contents of all cylinders from index hole to EOT

Read A Track, continued

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(4) Read ID

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	0	1	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution										The first correct ID information on the cylinder is stored in the Data Register
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Disk status after the command has been completed
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(5) Verify

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	1	0	1	1	0	Command codes
	W	EC	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
		---------- DTL/SC ----------								
Execution										No data transfer takes place

Verify, continued

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(6) Version

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	0	0	Command code
Result	R	1	0	0	1	0	0	0	0	Enhanced controller

(7) Write Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	0	0	0	1	0	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to Command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system
Result	R	---------- ST0 ----------								Status information after Command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after Command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(8) Write Deleted Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	0	0	1	0	0	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(9) Format A Track

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	1	0	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- N ----------								Bytes per Sector
	W	---------- SC ----------								Sectors per Cylinder
	W	---------- GPL ----------								Gap 3
	W	---------- D ----------								Filler Byte
Execution for Each Sector: (Repeat)	W	---------- C ----------								Input Sector Parameters
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								

Format A Track, continued

PHASE	R/W	D7 D6 D5 D4 D3 D2 D1 D0	REMARKS
Result	R	---------- ST0 ----------	Status information after command execution
	R	---------- ST1 ----------	
	R	---------- ST2 ----------	
	R	---------- Undefined ----------	
	R	---------- Undefined ----------	
	R	---------- Undefined ----------	
	R	---------- Undefined ----------	

(10) Recalibrate

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	1	1	Command codes
	W	0	0	0	0	0	0	DS1	DS0	
Execution										Head retracted to Track 0 Interrupt

(11) Sense Interrupt Status

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	0	0	0	Command code
Result	R	---------- ST0 ----------								Status information at the end of each seek operation
	R	---------- PCN ----------								

(12) Specify

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	0	1	1	Command codes
	W	| ---------SRT ---------- | --------- HUT ---------- |								
	W	|---------- HLT ----------| ND								

(13) Seek

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- NCN ----------								
Execution	R									Head positioned over proper cylinder on diskette

(14) Configure

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	1	Configure information
	W	0	0	0	0	0	0	0	0	
	W	0	EIS	EFIFO	POLL	------ FIFOTHR ----				
	W		----------PRETRK ----------							
Execution										Internal registers written

(15) Relative Seek

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	1	DIR	0	0	1	1	1	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W		---------- RCN ----------							

(16) Dumpreg

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	0	Registers placed in FIFO
Result	R	---------- PCN-Drive 0----------								
	R	---------- PCN-Drive 1 ----------								
	R	---------- PCN-Drive 2----------								
	R	---------- PCN-Drive 3 ----------								
	R	--------SRT ---------- | --------- HUT --------								
	R	---------- HLT ----------| ND								
	R	---------- SC/EOT ----------								
	R	LOCK	0	D3	D2	D1	D0	GAP	WG	
	R	0	EIS	EFIFO	POLL	------ FIFOTHR --------				
	R	----------PRETRK ----------								

(17) Perpendicular Mode

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	0	Command Code
	W	OW	0	D3	D2	D1	D0	GAP	WG	

(18) Lock

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	LOCK	0	0	1	0	1	0	0	Command Code
Result	R	0	0	0	LOCK	0	0	0	0	

(19) Sense Drive Status

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	0	0	Command Code
	W	0	0	0	0	0	HDS	DS1	DS0	
Result	R	---------- ST3 ----------								Status information about disk drive

(20) Invalid

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	---------- Invalid Codes ----------								Invalid codes (no operation-FDC goes to standby state)
Result	R	---------- ST0 ----------								ST0 = 80H

9.3 Register Descriptions

There are several status, data, and control registers in the W83627UHG. These registers are defined below, and the rest of this section provides more detail about each one of them.

Table 9-2 FDC Registers

ADDRESS OFFSET	REGISTER	
	READ	WRITE
base address + 0	SA REGISTER	
base address + 1	SB REGISTER	
base address + 2		DO REGISTER
base address + 3	TD REGISTER	TD REGISTER
base address + 4	MS REGISTER	DR REGISTER
base address + 5	DT (FIFO) REGISTER	DT (FIFO) REGISTER
base address + 7	DI REGISTER	CC REGISTER

9.3.1 Status Register A (SA Register) (Read base address + 0)

Along with the SB register, the SA register is used to monitor several disk-interface pins in PS/2 and Model 30 modes. In PS/2 mode, the bit definitions for this register are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	INIT PENDING	DRV 2#	STEP	TRAK0#	HEAD	INDEX#	WP#	DIR
DEFAULT	0	0	NA	1	NA	1	1	NA

BIT	DESCRIPTION

BIT	DESCRIPTION
7	**INIT PENDING**. Indicates the value of the floppy disk interrupt output.
6	**DRV2#.** 0: A second drive has been installed. 1: No second drive is installed.
5	**STEP.** Indicates the complement of the STEP# output.
4	**TRAK0#.** Indicates the value of the TRAK# input.
3	**HEAD.** Indicates the complement of the HEAD# output. 0: Side 0. 1: Side 1.
2	**INDEX#.** Indicates the value of the INDEX# output.
1	**WP#.** 0: The disk is write-protected. 1: The disk is not write-protected.
0	**DIR.** Indicates the direction of head movement. 0: Outward direction. 1: Inward direction.

In PS/2 Model 30 mode, the bit definitions for this register are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	INIT PENDING	DRQ	STEP F/F	TRAK0	HEAD#	INDEX	WP	DIR#
DEFAULT	0	0	NA	0	NA	0	0	NA

BIT	DESCRIPTION
7	**INIT PENDING.** Indicates the value of the floppy disk interrupt output.
6	**DRQ.** Indicates the value of the DRQ output pin.
5	**SETP F/F.** indicates the complement of latched STEP# output.
4	**TRAK0.** Indicates the complement of the TRAK0# input.
3	**HEAD#.** Indicates the value of the HEAD# output. 0: Side 1. 1: Side 0.
2	**INDEX.** Indicates the complement of the INDEX# output.
1	**WP.** 0: The disk is not write-protected. 1: The disk is write-protected.
0	**DIR#.** Indicates the direction of the head movement. 0: Inward direction. 1: Outward direction.

9.3.2 Status Register B (SB Register) (Read base address + 1)

Along with the SA register, the SB register is used to monitor several disk interface pins in PS/2 and Model 30 modes. In PS/2 mode, the bit definitions for this register are as follows:

BIT	7	6	5	4	3	2	1	0
NAME			Drive SEL0	WDTA Toggle	RDTA Toggle	WE	MOT EN B	MOT EN A
DEFAULT	1	1	0	0	0	0	0	0

BIT	DESCRIPTION
7	1
6	1
5	**Drive SEL0.** Indicates the status of the DO Register, bit 0 (drive-select bit 0).
4	**WDATA Toggle.** Changes state on every rising edge of the WD# output pin.
3	**RDATA Toggle.** Changes state on every rising edge of the RDATA# output pin.
2	**WE.** Indicates the complement of the WE# output pin.
1	**MOT EN B.** Indicates the complement of the MOB# output pin.
0	**MOT EN A.** Indicates the complement of the MOA# output pin.

In PS/2 Model 30 mode, the bit definitions for this register are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	DRV 2#	RESERVED.	DSA#	WD F/F	RDATA F/F	WE F/F	DSD#	DSC#
DEFAULT	0	1	1	0	0	0	1	1

BIT	DESCRIPTION
7	**DRV 2#.** 0: A second drive has been installed. 1: No second drive is installed.
6	**Reserved.**
5	**DSA#.** Indicates the status of the DSA# output pin.
4	**WD F/F.** Indicates the complement of the WD# output pin, which is latched on every rising edge of the WD# output pin.
3	**RDATA F/F.** Indicates the complement of the latched RDATA# output pin.
2	**WE F/F.** Indicates the complement of the latched WE# output pin.
1-0	**Reserved.**

9.3.3 Digital Output Register (DO Register) (Write base address + 2)

The Digital Output Register is a write-only register that controls drive motors, drive selection, DRQ/IRQ enable, and FDC reset. All the bits in this register are cleared by the MR pin. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			MOTOR ENABLE A	DMA&INT ENABLE	FDC RESET	DRIVE SELECT	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**Reserved.**
4	**MOTOR ENABLE A.** A logical 1 enables Motor A.
3	**DMA & INT ENABLE.** A logical 1 enables DRQ/IRQ.
2	**FDC RESET.** Floppy Disk Controller Reset. A logical 0 resets the FDC.
1-0	**DRIVE SELECT.** **Bits** **1 0** 0 0: Select Drive A. 0 1: Select Drive B. 1 0: Select Drive C. 1 1: Select Drive D.

9.3.4 Tape Drive Register (TD Register) (Read base address + 3)

This register is used to assign a particular drive number to the tape drive support mode of the data separator. This register also holds the media ID, drive type, and floppy boot drive information for the floppy disk drive.

In normal floppy mode, this register only has bits 0 and 1, and the bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED						Tape sel 1	Tape sel 0
DEFAULT	NA	NA	NA	NA	NA	NA	0	0

BIT	DESCRIPTION
7-2	**RESERVED.**
1	Tape sel 1.
0	Tape sel 0.

If the three-mode FDD function is enabled (EN3MODE = 1 in LD0 CRF0, Bit 0), the bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	Media ID1	Media ID0	Drive Type ID1	Drive Type ID0	Floppy Boot Drive 1	Floppy Boot Drive 0	Tape Sel 1	Tape Sel 0
DEFAULT	0	0	1	1	0	0	0	0

BIT	DESCRIPTION	
7	**Media ID1.** Read only. Reflects the value of LD0, CRF1, bit 5.	
6	**Media ID0.** Read only. Reflects the value of LD0, CRF1, bit 4.	
5	**Drive Type ID1.**	Reflect the bit in LD0, CRF2. Which bit is reflected depends on the last drive selected in the PO register.
4	**Drive Type ID0.**	
3	**Floppy Boot Drive 1.** Reflects the value of LD0, CRF1, bit 7.	
2	**Floppy Boot Drive 0.** Reflects the value of LD0, CRF1, bit 6.	
1	**Tape Sel 1.**	Assign a logical drive number to the tape drive. Drive 0 is not available as a tape drive and is reserved for the floppy disk boot drive.
0	**Tape Sel 0.**	

TAPE SEL 1	TAPE SEL 0	DRIVE SELECTED
0	0	None
0	1	1
1	0	2
1	1	3

9.3.5 Main Status Register (MS Register) (Read base address + 4)

The Main Status Register is used to control the flow of data between the microprocessor and the controller. The bit definitions for this register are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RQM	DIO	Non-DMA mode	FDC Busy	FDD 3 Busy	FDD 2 Busy	FDD 1 Busy	FDD 0 Busy
DEFAULT	0	NA	NA	NA	NA	NA	NA	NA

BIT	DESCRIPTION
7	**Request for Master (RQM).** A high on this bit indicates Data Register is ready to send or receive data to or from the processor.
6	**DATA INPUT/OUTPUT (DIO).** If DIO = HIGH, then the transfer is from Data Register to the processor. If DIO = LOW, the transfer is from processor to Data Register.
5	**Non-DMA mode.** The FDC is in the non-DMA mode, this bit is set only during the execution phase in non-DMA mode.
4	**FDC Busy** (CB). A read or write command is in the process when CB = HIGH.
3	**FDD 3 Busy.** (D3B = 1) FDD number 3 is in the SEEK mode.
2	**FDD 2 Busy.** (D2B = 1) FDD number 2 is in the SEEK mode.
1	**FDD 1 Busy.** (D1B = 1) FDD number 1 is in the SEEK mode.
0	**FDD 0 Busy.** (D0B = 1) FDD number 0 is in the SEEK mode.

9.3.6 Data Rate Register (DR Register) (Write base address + 4)

The Data Rate Register is used to set the transfer rate and write precompensation. However, in PC-AT and PS/2 Model 30 and PS/2 modes, the data rate is controlled by the CC register, not by the DR register. As a result, the real data rate is determined by the most recent write to either the DR or CC register. The bit definitions for this register are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	S/W RESET	POWER DOWN		PRECOMP2	PRECOMP1	PRECOMP0	DRATE1	DRATE0
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION	
7	**S/W RESET.** The software reset bit.	
6	**POWER DOWN.** 0: FDC in normal mode. 1: FDC in power-down mode.	
5	0	
4	**PRECOMP 2.**	Selects the value of write precompensation. The following tables show the precompensation values for every combination of these bits. Please see the tables below.
3	**PRECOMP 1.**	
2	**PRECOMP 0.**	

Continued

BIT	DESCRIPTION	
1	**DRATE 1.**	Select the data rate of the FDC and reduced write-current control. **Bits** **1 0** 0 0: 500 KB/S (MFM), 250 KB/S (FM), RWC# = 1 0 1: 300 KB/S (MFM), 150 KB/S (FM), RWC# = 0 1 0: 250 KB/S (MFM), 125 KB/S (FM), RWC# = 0 1 1: 1 MB/S (MFM), Illegal (FM), RWC# = 1
0	**DRATE 0.**	

The 2 MB/S data rate for the tape drive is only supported by setting DRATE1 and DRATE0 to 01, as well as setting DRT1 and DRT0 (CRF4 and CRF5 for logical device 0) to 10. Please see the functional description of CRF4 or CRF5 and the data rate table for individual data-rate settings.

PRECOMP	PRECOMPENSATION DELAY	
2 1 0	250K - 1 Mbps	2 Mbps Tape drive
0 0 0	Default Delays	Default Delays
0 0 1	41.67 ns	20.8 ns
0 1 0	83.34 ns	41.17 ns
0 1 1	125.00 ns	62.5ns
1 0 0	166.67 ns	83.3 ns
1 0 1	208.33 ns	104.2 ns
1 1 0	250.00 ns	125.00 ns
1 1 1	0.00 ns (disabled)	0.00 ns (disabled)

DATA RATE	DEFAULT PRECOMPENSATION DELAYS
250 KB/S	125 ns
300 KB/S	125 ns
500 KB/S	125 ns
1 MB/S	41.67ns
2 MB/S	20.8 ns

9.3.7 FIFO Register (R/W base address + 5)

The FIFO register consists of four status registers in a stack, and only one register is presented to the data bus at a time. The FIFO register stores data, commands, and parameters, and it provides disk-drive status information. In addition, data bytes pass through the data register to program or obtain results after a command. In the W83627UHG, this register is disabled after reset. The FIFO can enable it and change its values through the configure command.

BIT	7	6	5	4	3	2	1	0
NAME	IC Interrupt Code		SE Seek End	EC Equipment Check	NR Not Ready	HD Head Address	US1, US0 Drive Select	

Status Register 0 (ST0)

BIT	DESCRIPTION
7-6	**IC Interrupt Code.** **Bits** **7 6** 0 0: Normal termination of the command. 0 1: Abnormal termination of the command. 1 0: Invalid command issue. 1 1: Abnormal termination because the ready signal from FDD changed state during command execution.
5	**SE (Seek End).** 1: Seek end. 0: Seek error.
4	**EC (Equipment Check).** 1: When a fault signal is received from the FDD or the track. 0: Signal fails to occur after 77 step pulses. 0: No error.
3	**NR (Not Ready).** 1: Drive is not ready. 0: Drive is ready.
2	**HD Head Address. (The current head address)** 1: Head selected. 0: Head selected.
1-0	**US 1, US0 Drive Select.** **Bits** **1 0** 0 0: Drive A selected. 0 1: Drive B selected. 1 0: Drive C selected. 1 1: Drive D selected.

Status Register 1 (ST1)

BIT	7	6	5	4	3	2	1	0
NAME	EN	Not Used	OE	OR	Not Used	ND	NW	MAM

BIT	DESCRIPTION
7	**EN (End of Track).** 1 will be written to this bit if the FDC tries to access a sector beyond the final sector or a cylinder.
6	Not Used. This bit is always 0.
5	**DE (Data Error).** 1 will be written to this bit if the FDC detects a CRC error in either the ID field or the data field.
4	**OR (Over Run).** 1 will be written to this bit if the FDC is not served by the host system within a certain time interval during data transfer.
3	Not Used. This bit is always 0.
2	**ND (No Data).** 1 will be written to this bit if the specified sector cannot be found during execution of a read, write or verity data.
1	**NW (Not Writable).** 1 will be written to this bit if a write protect signal is detected from the diskette drive during execution of write data.
0	**MAM (Missing Address Mark).** 1 will be written to this bit if the FDC cannot detect the data address mark or the data address mark has been deleted.

Status Register 2 (ST2)

BIT	7	6	5	4	3	2	1	0
NAME		CM	DD	WC	SH	SN	BC	MD

BIT	DESCRIPTION
7	Not used. This bit is always 0.
6	**CM (Control Mark).** 1: During execution of the read data or scan command. 0: No error.
5	**DD (Data error in the Data field).** 1: If the FDC detects a CRC error in the data field. 0: No error.
4	**WC (Wrong Cylinder).** 1: Indicates wrong cylinder.
3	**SH (Scan Equal Hit).** 1: During execution of the Scan command, if the equal condition is satisfied. 0: No error.
2	**SN (Scan Not Satisfied).** 1: During execution of the Scan command. 0: No error.

BIT	DESCRIPTION
1	**BC (Bad Cylinder).** 1: Bad Cylinder. 0: No error.
0	**MD (Missing Address Mark in Data Field).** 1: If FDC cannot find a data address mark (or the address mark has been deleted) when reading data from the media. 0: No error.

Status Register 3 (ST3)

BIT	7	6	5	4	3	2	1	0
NAME	FT	WP	RY	T0	TS	HD	US1	US0

BIT	DESCRIPTION
7	**FT.** Fault.
6	**WP.** Write protected.
5	**RY.** Ready.
4	**T0.** Track 0.
3	**TS.** Two-side.
2	**HD.** Head Address.
1	**US1.** Unit Select 1.
0	**US0.** Unit Select 0.

9.3.8 Digital Input Register (DI Register) (Read base address + 7)

The Digital Input Register is an 8-bit, read-only register used for diagnostic purposes. In PC/XT or PC/AT mode, only bit 7 is checked by the BIOS. When the register is read, bit 7 shows the complement of DSKCHG#, while the other bits remain in tri-state. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	DSKCHG	RESERVED						
DEFAULT	0	NA	NA	NA	NA	NA	NA	NA

BIT	DESCRIPTION
7	**DSKCHG.**
6-0	**RESERVED.** Reserved for the hard disk controller. During a read of this register, these bits are in tri-state.

In PS/2 mode, the bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	DSKCHG					DRATE1	DRATE0	HIGH DENS#
DEFAULT	0	1	1	1	1	1	0	1

BIT	DESCRIPTION	
7	**DSKCHG.** Indicates the complement of the DSKCHG# input.	
6-3	Always 1 during a read.	
2	**DRATE 1.**	Select the data rate of the FDC. See DR register bits 1 and 0 (Data Rate Register (DR Register) (Write base address + 4)) for how the settings correspond to individual data rates.
1	**DRATE 0.**	
0	**HIGHDENS#.** 0: 500 KB/S or 1 MB/S data rate (high-density FDD). 1: 250 KB/S or 300 KB/S data rate.	

In PS/2 Model 30 mode, the bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	DSKCHG#				DMAEN	NOPREC	DRATE1	DRATE0
DEFAULT	1	0	0	0	0	0	1	0

BIT	DESCRIPTION	
7	**DSKCHG.** Indicates the status of the DSKCHG# input.	
6-4	Always 0 during a read.	
3	**DMAEN.** Indicates the value of DO register, bit 3.	
2	**NOPREC.** Indicates the value of the NOPREC bit in the CC REGISTER.	
1	**DRATE 1.**	Select the data rate of the FDC. See DR register bits 1 and 0 (Data Rate Register (DR Register) (Write base address +4)) for how the settings correspond to individual data rates.
0	**DRATE 0.**	

9.3.9 Configuration Control Register (CC Register) (Write base address + 7)

This register is used to control the data rate. In PC/AT and PS/2 mode, the bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED						DRATE1	DRATE0
DEFAULT	NA	NA	NA	NAN	NA	NA	1	0

BIT	DESCRIPTION	
7-2	**RESERVED.** Should be set to 0.	
1	**DRATE 1.**	Select the data rate of the FDC. See DR register bits 1 and 0 (Data Rate Register (DR Register) (Write base address + 4) for how the settings correspond to individual data rates.
0	**DRATE 0.**	

In the PS/2 Model 30 mode, the bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED					NOPREC	DRATE1	DRATE0
DEFAULT	NA	NA	NA	NA	NA	0	1	0

BIT	DESCRIPTION	
7-3	**RESERVED.** Should be set to 0.	
2	**NOPREC.** Disables the precompensation function. This bit can be set by the software.	
1	**DRATE1.**	Select the data rate of the FDC. See DR register bits 1 and 0 (Data Rate Register (DR Register) (Write base address + 4)) for how the settings correspond to individual data rates.
0	**DRATE0.**	

10. UART PORT

10.1 Universal Asynchronous Receiver/Transmitter (UART A, B, C, D, E, F)

The UARTs are used to convert parallel data into serial format for transmission and to convert serial data into parallel format during reception. The serial data format is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one-and-a-half (five-bit format only) or two stop bits. The UARTs are capable of handling divisors of 1 to 65535 and producing a 16x clock for driving the internal transmitter logic. Provisions are also included to use this 16x clock to drive the receiver logic. The UARTs also support the MIDI data rate. Furthermore, the UARTs also include a complete modem control capability and 16-byte FIFOs for reception and transmission to reduce the number of interrupts presented to the CPU.

10.2 Register Address

10.2.1 UART Control Register (UCR) (Read/Write)

The UART Control Register defines and controls the protocol for asynchronous data communications, including data length, stop bit, parity, and baud rate selection.

BIT	7	6	5	4	3	2	1	0
NAME	BDLAB	SSE	PBFE	EPE	PBE	MSBE	DLS1	DLS0
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**BDLAB (Baud Rate Divisor Latch Access Bit).** When this bit is set to logic 1, designers can access the divisor (in 16-bit binary format) from the divisor latches of the baud-rate generator during a read or write operation. When this bit is set to logic 0, the Receiver Buffer Register, the Transmitter Buffer Register, and the Interrupt Control Register can be accessed.
6	**SSE (Set Silence Enable).** A logic 1 forces the Serial Output (SOUT) to a silent state (a logical 0). Only IRTX is affected by this bit; the transmitter is not affected.
5	**PBFE (Parity Bit Fixed Enable).** When PBE and PBFE of UCR are both set to logic 1, (1) if EPE is logic 1, the parity bit is logical 0 when transmitting and checking; (2) if EPE is logic 0, the parity bit is logical 1 when transmitting and checking.
4	**EPE (Even Parity Enable).** When PBE is set to logic 1, this bit counts the number of logic 1's in the data word bits and determines the parity bit. When this bit is set to logic 1, the parity bit is set to logic 1 if an even number of logic 1's are sent or checked. When the bit is set to logic 0, the parity bit is logic 1, if an odd number of logic 1's are sent or checked.
3	**PBE (Parity Bit Enable).** When this bit is set to logic 1, the transmitter inserts a stop bit between the last data bit and the stop bit of the SOUT, and the receiver checks the parity bit in the same position.

Continued

BIT	DESCRIPTION
2	**MSBE (Multiple Stop Bit Enable).** Defines the number of stop bits in each serial character that is transmitted or received. (1) If MSBE is set to logic 0, one stop bit is sent and checked. (2) If MSBE is set to logic 1 and the data length is 5 bits, one-and-a-half stop bits are sent and checked. (3) If MSBE is set to logic 1 and the data length is 6, 7, or 8 bits, two stop bits are sent and checked.
1	**DLS1 (Data Length Select Bit 1).** Defines the number of data bits that are sent or checked in each serial character.
0	**DLS0 (Data Length Select Bit 0).** Defines the number of data bits that are sent or checked in each serial character.

DLS1	DLS0	DATA LENGTH
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

The following table identifies the remaining UART registers. Each one is described separately in the following sections.

Table 10-1 Register Summary for UART

Register Address Base			Bit Number							
			0	1	2	3	4	5	6	7
+ 0 BDLAB = 0	Receiver Buffer Register (Read Only)	RBR	RX Data Bit 0	RX Data Bit 1	RX Data Bit 2	RX Data Bit 3	RX Data Bit 4	RX Data Bit 5	RX Data Bit 6	RX Data Bit 7
+ 0 BDLAB = 0	Transmitter Buffer Register (Write Only)	TBR	TX Data Bit 0	TX Data Bit 1	TX Data Bit 2	TX Data Bit 3	TX Data Bit 4	TX Data Bit 5	TX Data Bit 6	TX Data Bit 7
+ 1 BDLAB = 0	Interrupt Control Register	ICR	RBR Data Ready Interrupt Enable (ERDRI)	TBR Empty Interrupt Enable (ETBREI)	USR Interrupt Enable (EUSRI)	HSR Interrupt Enable (EHSRI)	0	0	0	0
+ 2	Interrupt Status Register (Read Only)	ISR	"0" if Interrupt Pending	Interrupt Status Bit (0)	Interrupt Status Bit (1)	Interrupt Status Bit (2)**	0	0	FIFOs Enabled **	FIFOs Enabled **
+ 2	UART FIFO Control Register (Write Only)	UFR	FIFO Enable	RCVR FIFO Reset	XMIT FIFO Reset	DMA Mode Select	Reserved	Reversed	RX Interrupt Active Level (LSB)	RX Interrupt Active Level (MSB)
+ 3	UART Control Register	UCR	Data Length Select Bit 0 (DLS0)	Data Length Select Bit 1 (DLS1)	Multiple Stop Bits Enable (MSBE)	Parity Bit Enable (PBE)	Even Parity Enable (EPE)	Parity Bit Fixed Enable PBFE)	Set Silence Enable (SSE)	Baudrate Divisor Latch Access Bit (BDLAB)
+ 4	Handshake Control Register	HCR	Data Terminal Ready (DTR)	Request to Send (RTS)	Loopback RI Input	IRQ Enable	Internal Loopback Enable	0	0	0
+ 5	UART Status Register	USR	RBR Data Ready (RDR)	Overrun Error (OER)	Parity Bit Error (PBER)	No Stop Bit Error (NSER)	Silent Byte Detected (SBD)	TBR Empty (TBRE)	TSR Empty (TSRE)	RX FIFO Error Indication (RFEI) **
+ 6	Handshake Status Register	HSR	CTS Toggling (TCTS)	DSR Toggling (TDSR)	RI Falling Edge (FERI)	DCD Toggling (TDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)
+ 7	User Defined Register	UDR	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+ 0 BDLAB = 1	Baudrate Divisor Latch Low	BLL	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+ 1 BDLAB = 1	Baudrate Divisor Latch High	BHL	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

*: Bit 0 is the least significant bit. The least significant bit is the first bit serially transmitted or received.
**: These bits are always 0 in 16450 Mode.

10.2.2 UART Status Register (USR) (Read/Write)

This 8-bit register provides information about the status of data transfer during communication.

BIT	7	6	5	4	3	2	1	0
NAME	RF EI	TSRE	TBRE	SBD	NSER	PBER	OER	PDR
DEFAULT	0	1	1	0	0	0	0	0

BIT	DESCRIPTION
7	**RF EI (RX FIFO Error Indication).** In 16450 mode, this bit is always set to logical 0. in 16550 mode, this bit is set to logical 1 when there is at least one parity-bit error and no stop0bit error or silent-byte detected in the FIFO. In 16550 mode, this bit is cleared to logical 0 by reading from the USR if there are no remaining errors left in the FIFO.
6	**TSRE (Transmitter Shift Register Empty).** In 16450 mode, this bit is set to logical 1 when TBR and TSR are both empty. In 16550 mode, it is set to logical 1 when the transmit FIFO and TSR are both empty. Otherwise, this bit is set to logical 0.
5	**TBRE (Transmitter Buffer Register Empty).** In 16450 mode, when a data character is transferred from TBR to TSR, this bit is set to logical 1. If ETREI of ICR is high, and interrupt is generated to notify the CPU to write next data. In 16550 mode, this bit is set to logical 1 when the transmit FIFO is empty. It is set to logical 0 when the CPU writes data into TBR or the FIFO.
4	**SBD (Silent Byte Detected).** This bit is set to logical 1 to indicate that received data are kept in silent state for the time it takes to receive a full word, which includes the start bit, data bits, parity bit, and stop bits. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
3	**NSER (No Stop Bit Error).** This bit is set to logical 1 to indicate that the received data have no stop bit. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
2	**PBER (Parity Bit Error).** This bit is set to logical 1 to indicate that the received data has the wrong parity bit. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
1	**OER (Overrun Error).** This bit is set to logical 1 to indicate that the received data have been overwritten by the next received data before they were read by the CPU. In 16550 mode, it indicates the same condition, instead of FIFO full. When the CPU reads USR, it sets this bit to logical 0.
0	**RDR (RBR Data Ready).** This bit is set to logical 1 to indicate that the received data are ready to be read by the CPU in the RBR or FIFO. When no data are left in the RBR or FIFO, the bit is set to logical 0.

10.2.3 Handshake Control Register (HCR) (Read/Write)

This register controls pins used with handshaking peripherals such as modems and also controls the diagnostic mode of the UART.

BIT	7	6	5	4	3	2	1	0
NAME				INTERNAL LOOPBACK ENABLE	IRQ ENABLE	LOOPBACK RI INPUT	RTS	DTR
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	0
6	0
5	0
4	**Internal Loopback Enable.** When this bit is set to logic 1, the UART enters diagnostic mode, as follows: (1) SOUT is forced to logic 1, and SIN is isolated from the communication link. (2) The modem output pins are set to their inactive state. (3) The modem input pins are isolated from the communication link and connect internally as DTR (bit 0 of HCR) →DSR#, RTS (bit 1 of HCR) →CTS#, Loopback RI input (bit 2 of HCR) → RI# and IRQ enable (bit 3 of HCR) →DCD#. Aside from the above connections, the UART operates normally. This method allows the CPU to test the UART in a convenient way.
3	**IRQ Enable.** The UART interrupt output is enabled by setting this bit to logic 1. In diagnostic mode, this bit is internally connected to the modem control input DCD#.
2	**Loopback RI Input.** This bit is only used in the diagnostic mode. In diagnostic mode, this bit is internally connected to the modem control input RI#.
1	**RTS (Request to Send).** This bit controls the RTS# output. The value of this bit is inverted and output to RTS#.
0	**DTR (Data Terminal Ready).** This bit controls the DTR# output. The value of this bit is inverted and output to DTR#.

10.2.4 Handshake Status Register (HSR) (Read/Write)

This register reflects the current state of four input pins used with handshake peripherals such as modems and records changes on these pins.

BIT	7	6	5	4	3	2	1	0
NAME	DCD	RI	DSR	CTS	TDCD	FERI	TDSR	TCTS
DEFAULT	NA	NA	NA	NA	NA	NA	NA	NA

BIT	DESCRIPTION
7	**DCD (Data Carrier Detect).** This bit is the inverse of the DCD# input and is equivalent to bit 3 of HCR in Loopback mode.
6	**RI (Ring Indicator).** This bit is the inverse of the RI# input and is equivalent to bit 2 of HCR in Loopback mode.
5	**DSR (Data Set Ready).** This bit is the inverse of the DSR# input and is equivalent to bit 0 of HCR in Loopback mode.
4	**CTS (Clear to Send).** This bit is the inverse of the CTS# input and is equivalent to bit 1 of HCR in Loopback mode.
3	**TDCD (DCD# Toggling).** This bit indicates that the state of the DCD# pin has changed after HSR is read by the CPU.
2	**FERI (RI Falling Edge).** This bit indicates that the RI# pin has changed from low to high after HSR is read by the CPU.
1	**TDSR (DSR# Toggling).** This bit indicates that the state of the DSR# pin has changed after HSR is read by the CPU.
0	**TCTS (CTS# Toggling).** This bit indicates that the state of the CTS# pin has changed after HSR is read by the CPU.

10.2.5 This register is used to control the FIFO functions of the UART

BIT	7	6	5	4	3	2	1	0
NAME	MSB	LSB	RESERVED		DMA MODE SELECT	TRANSMITTER FIFO RESET	RECEIVER FIFO RESET	FIFO ENABLE
DEFAULT	0	0	NA	NA	0	0	0	0

BIT	DESCRIPTION	
7	**MSB (RX Interrupt Active Level).**	These two bits are used to set the active level of the receiver FIFO interrupt. The active level is the number of bytes that must be in the receiver FIFO to generate an interrupt.
6	**LSB (RX Interrupt Active Level).**	
5-4	**RESERVED.**	
3	**DMS MODE SELECT.** When this bit is set to logic 1, DMA mode changes from mode 0 to mode 1 if UFR bit 0 = 1.	
2	**TRANSMITTER FIFO RESET.** Setting this bit to logic 1 resets the TX FIFO counter logic to its initial state. This bit is automatically cleared afterwards.	
1	**RECEIVER FIFO RESET.** Setting this bit to logic 1 resets the RX FIFO counter logic to its initial state. This bit is automatically cleared afterwards.	
0	**FIFO ENABLE.** This bit enables 16550 (FIFO) mode. This bit should be set to logic 1 before other UFR bits are programmed.	

BIT 7	BIT 6	RX FIFO INTERRUPT ACTIVE LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14

10.2.6 Interrupt Status Register (ISR) (Read only)

This register reflects the UART interrupt status.

BIT	7	6	5	4	3	2	1	0
NAME	FIFOS ENABLED				INTERRUPT STATUS BIT 2	INTERRUPT STATUS BIT 1	INTERRUPT STATUS BIT 0	0 IF INTERRUPT PENDING
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION	
7-6	**FIFOS ENABLED.** Set to logical 1 when UFR, bit 0 = 1.	
5	0	
4	0	
3	**INTERRUPT STATUS BIT 2.** In 16450 mode, this bit is logical 0. In 16550 mode, bits 3 and 2 are set to logical 1 when a time-out interrupt is pending. Please see the table below.	
2	**INTERRUPT STATUS BIT 1.**	These two bits identify the priority level of the pending interrupt, as shown in the table below.
1	**INTERRUPT STATUS BIT 0.**	
0	**0 IF INTERRUPT PENDING.** This bit is logic 1 if there is no interrupt pending. If one of the interrupt sources has occurred, this bit is set to logical 0.	

ISR				INTERRUPT SET AND FUNCTION			
Bit 3	Bit 2	Bit 1	Bit 0	Interrupt priority	Interrupt Type	Interrupt Source	Clear Interrupt
0	0	0	1	-	-	No Interrupt pending	-
0	1	1	0	First	UART Receive Status	1. OER = 1 2. PBER =1 3. NSER = 1 4. SBD = 1	Read USR
0	1	0	0	Second	RBR Data Ready	1. RBR data ready 2. FIFO interrupt active level reached	1. Read RBR 2. Read RBR until FIFO data under active level

Continued

ISR				INTERRUPT SET AND FUNCTION			
Bit 3	Bit 2	Bit 1	Bit 0	Interrupt priority	Interrupt Type	Interrupt Source	Clear Interrupt
1	1	0	0	Second	FIFO Data Timeout	Data present in RX FIFO for 4 characters period of time since last access of RX FIFO.	Read RBR
0	0	1	0	Third	TBR Empty	TBR empty	1. Write data into TBR 2. Read ISR (if priority is third)
0	0	0	0	Fourth	Handshake status	1. TCTS = 1 2. TDSR = 1 3. FERI = 1 4. TDCD = 1	Read HSR

** Bit 3 of ISR is enabled when bit 0 of UFR is logical 1.

10.2.7 Interrupt Control Register (ICR) (Read/Write)

This 8-bit register enables and disables the five types of controller interrupts separately. A selected interrupt can be enabled by setting the appropriate bit to logical 1. The interrupt system can be totally disabled by setting bits 0 through 3 to logical 0.

BIT	7	6	5	4	3	2	1	0
NAME					EHSRI	EUSRI	ETBREI	ERDRI
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	0
6	0
5	0
4	0
3	**EHSRI (Handshake Status Interrupt Enable).** Set this bit to logical 1 to enable the handshake status register interrupt.
2	**EUSRI (UART Receive Status Interrupt Enable).** Set this bit to logical 1 to enable the UART status register interrupt.
1	**ETBREI (TBR Empty Interrupt Enable).** Set this bit to logical 1 to enable the TBR empty interrupt.
0	**ERDRI (RBR Data Ready Interrupt Enable).** Set this bit to logical 1 to enable the RBR data ready interrupt.

11. PARALLEL PORT

11.1 Printer Interface Logic

The W83627UHG parallel port can be attached to devices that accept eight bits of parallel data at standard TTL level. The W83627UHG supports the IBM XT/AT compatible parallel port (SPP), the bi-directional parallel port (BPP), the Enhanced Parallel Port (EPP), and the Extended Capabilities Parallel Port (ECP).

The following tables show the pin definitions for different modes of the parallel port.

Table 11-1 Pin Descriptions for SPP, EPP, and ECP Modes

HOST CONNECTOR	PIN NUMBER OF W83627UHG	PIN ATTRIBUTE	SPP	EPP	ECP
1	36	O	Nstb	nWrite	nSTB, HostClk[2]
2-9	31-26, 24-23	I/O	PD<7:0>	PD<7:0>	PD<7:0>
10	22	I	nACK	Intr	nACK, PeriphClk[2]
11	21	I	BUSY	nWait	BUSY, PeriphAck[2]
12	19	I	PE	PE	PEerror, nAckReverse[2]
13	18	I	SLCT	Select	SLCT, Xflag[2]
14	35	O	Nafd	nDStrb	nAFD, HostAck[2]
15	34	I	nERR	nError	nFault[1], nPeriphRequest[2]
16	33	O	Ninit	nInit	nINIT[1], nReverseRqst[2]
17	32	O	nSLIN	nAStrb	nSLIN[1], ECPMode[2]

Notes:

n<name > : Active Low

1. Compatible Mode
2. High Speed Mode
3. For more information, refer to the IEEE 1284 standard.

11.2 Enhanced Parallel Port (EPP)

The following table lists the registers used in the EPP mode, and identifies the bit map of the parallel port and EPP registers. Some registers are also used in other modes.

Table 11-2 EPP Register Addresses

A2	A1	A0	REGISTER	NOTE
0	0	0	Data pot (R/W)	1
0	0	1	Printer status buffer (Read)	1
0	1	0	Printer control latch (Write)	1
0	1	0	Printer control swapper (Read)	1
0	1	1	EPP address port (R/W)	2

EPP Register Addresses, continued

1	0	0	EPP data port 0 (R/W)	2
1	0	1	EPP data port 1 (R/W)	2
1	1	0	EPP data port 2 (R/W)	2
1	1	1	EPP data port 2 (R/W)	2

Notes:

1. These registers are available in all modes.
2. These registers are available only in EPP mode.

Table 11-3 Address and Bit Map for SPP and EPP Modes

REGISTER	7	6	5	4	3	2	1	0
Data Port (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Status Buffer (Read)	BUSY#	ACK#	PE	SLCT	ERROR#	1	1	TMOUT
Control Swapper (Read)	1	1	1	IRQEN	SLIN	INIT#	AUTOFD#	STROBE#
Control Latch (Write)	1	1	DIR	IRQ	SLIN	INIT#	AUTOFD#	STROBE#
EPP Address Port (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 0 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 1 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 2 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 3 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Each register (or pair of registers, in some cases) is discussed below.

11.2.1 Data Port (Data Swapper)

The CPU reads the contents of the printer's data latch by reading the data port.

11.2.2 Printer Status Buffer

The CPU reads the printer status by reading the printer status buffer. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	BUSY#	ACK#	PE	SLCT	ERROR#			TMOUT
DEFAULT	NA	NA	NA	NA	NA	1	1	0

BIT	DESCRIPTION
7	**BUSY#.** This signal is active during data entry, when the printer is off-line during printing, when the print head is changing position, or during an error state. When this signal is active, the printer is busy and cannot accept data.
6	**ACK#.** This bit represents the current state of the printer's ACK# signal. A logical 0 means the printer has received a character and is ready to accept another. Normally, this signal is active for approximately 5 μs before BUSY# stops.
5	**PE.** A logical 1 means the printer has detected the end of paper.
4	**SLCT.** A logical 1 means the printer is selected.
3	**ERROR#.** A logical 0 means the printer has encountered an error condition.
2	1
1	1
0	**TMOUT.** This bit is only valid in EPP mode. A logical 1 indicates that a 10-μs time-out has occurred on the EPP bus; a logical 0 means hat no time-out error has occurred. Writing a logical 1 to this bit clears the time-out status bit; writing a logical 0 has no effect.

11.2.3 Printer Control Latch and Printer Control Swapper

The CPU reads the contents of the printer control latch by reading the printer control swapper. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME			DIR	IRQ ENABLE	SLCT IN	INIT#	AUTO FD	STROBE
DEFAULT	1	1	NA	0	NA	NA	NA	NA

BIT	DESCRIPTION
7-6	These two bits are always read as logical 1 and can be written.
5	**DIR** (Direction Control Bit). When this bit is logical 1, the parallel port is in the input mode (read). When it is logical 0, the parallel port is in the output mode (write). This bit can be read and written. In SPP mode, this bit is invalid and fixed at zero.
4	**IRQ ENABLE.** A logical 1 allows an interrupt to occur when ACK# changes from low to high.
3	**SLCT IN.** a logical 1 selects the printer.
2	**INIT#.** A logical 0 starts the printer (50 microsecond pulse, minimum).
1	**AUTO FD.** A logical 1 causes the printer to line-feed after a line is printed.
0	**STROBE.** A logical 1 generates an active-high pulse for a minimum of 0.5 μs to clock data into the printer. Valid data must be presented for a minimum of 0.5 μs before and after the strobe pulse.

11.2.4 EPP Address Port

The address port is available only in EPP mode. Bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

The contents of DB0-DB7 are buffered (non-inverting) and output to ports PD0-PD7 during a write operation. The leading edge of IOW# causes an EPP address write cycle to be performed, and the trailing edge of IOW# latches the data for the duration of the EPP write cycle.

PD0-PD7 ports are read during a read operation. The leading edge of IOR# causes an EPP address read cycle to be performed and the data to be output to the host CPU.

11.2.5 EPP Data Port 0-3

These four registers are available only in EPP mode. The bit definitions for each data port are the same and as follows:

BIT	7	6	5	4	3	2	1	0
NAME	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

When any EPP data port is accessed, the contents of DB0-DB7 are buffered (non-inverting) and output to ports PD0-PD7 during a write operation. The leading edge of IOW# causes an EPP data write cycle to be performed and the trailing edge of IOW# latches the data for the duration of the EPP write cycle.

During a read operation, ports PD0-PD7 are read, and the leading edge of IOR# causes an EPP read cycle to be performed and the data to be output to the host CPU.

11.2.6 EPP Pin Descriptions

EPP NAME	TYPE	EPP DESCRIPTION
NWrite	O	Denotes read or write operation for address or data.
PD<7:0>	I/O	Bi-directional EPP address and data bus.
Intr	I	Used by peripheral devices to interrupt the host.
NWait	I	Inactivated to acknowledge that data transfer is complete. Activated to indicate that the device is ready for the next transfer.
PE	I	Paper end; same as SPP mode.
Select	I	Printer-select status; same as SPP mode.
NDStrb	O	This signal is active low. It denotes a data read or write operation.
Nerror	I	Error; same as SPP mode.
Ninits	O	This signal is active low. When it is active, the EPP device is reset to its initial operating mode.
NAStrb	O	This signal is active low. It denotes an address read or write operation.

11.2.7 EPP Operation

When EPP mode is selected, the PDx bus is in standard or bi-directional mode when no EPP read, write, or address cycle is being executed. In this situation, all output signals are set by the SPP Control Port and the direction is controlled by DIR of the Control Port.

A watchdog timer is required to prevent system lockup. The timer indicates that more than 10 μS have elapsed from the start of the EPP cycle to the time WAIT# is deasserted. The current EPP cycle is aborted when a time-out occurs. The time-out condition is indicated in status bit 0.

The EPP operates on a two-phase cycle. First, the host selects the register within the device for subsequent operations. Second, the host performs a series of read and/or write byte operations to the selected register. Four operations are supported on the EPP: Address Write, Data Write, Address Read, and Data Read. All operations on the EPP device are performed asynchronously.

11.2.7.1 EPP Version 1.9 Operation

The EPP read/write operation can be completed under the following conditions:

a. If nWait is active low, the read cycle (nWrite inactive high, nDStrb/nAStrb active low) or write cycle (nWrite active low, nDStrb/nAStrb active low) starts, proceeds normally, and is completed when nWait goes inactive high.

b. If nWait is inactive high, the read/write cycle cannot start. It must wait until nWait changes to active low, at which time it starts is as described above.

11.2.7.2 EPP Version 1.7 Operation

The EPP read/write cycle can start without checking whether nWait is active or inactive. Once the read/write cycle starts, however, it does not finish until nWait changes from active low to inactive high.

11.3 Extended Capabilities Parallel (ECP) Port

This port is software- and hardware-compatible with existing parallel ports, so the W83627UHG parallel port may be used in standard printer mode if ECP is not required. It provides an automatic high burst-bandwidth channel that supports DMA for ECP in both the forward (host-to-peripheral) and reverse (peripheral-to-host) directions.

Small FIFOs are used in both forward and reverse directions to improve the maximum bandwidth requirement. The size of the FIFO is 16 bytes. The ECP port supports an automatic handshake for the standard parallel port to improve compatibility mode transfer speed.

The ECP port hardware supports run-length-encoded (RLE) decompression.

Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. RLE compression is required; the hardware support is optional.

For more information about the ECP Protocol, refer to the Extended Capabilities Port Protocol and ISA Interface Standard.

The W83627UHG ECP supports the following modes.

Table 11-4 ECP Mode Description

MODE	DESCRIPTION
000	SPP mode
001	PS/2 Parallel Port mode
010	Parallel Port Data FIFO mode
011	ECP Parallel Port mode
100	EPP mode (If this option is enabled in the CRF0h to select ECP/EPP mode)
101	Reserved
110	Test mode
111	Configuration mode

The mode selection bits are bits 7-5 of the Extended Control Register.

11.3.1 ECP Register and Bit Map

The next two tables list the registers used in ECP mode and provide a bit map of the parallel port and ECP registers.

Table 11-5 ECP Register Addresses

NAME	ADDRESS	I/O	ECP MODES	FUNCTION
data	Base+000h	R/W	000-001	Data Register
ecpAFifo	Base+000h	R/W	011	ECP FIFO (Address)
dsr	Base+001h	R	All	Status Register
dcr	Base+002h	R/W	All	Control Register
cFifo	Base+400h	R/W	010	Parallel Port Data FIFO
ecpDFifo	Base+400h	R/W	011	ECP FIFO (DATA)
tFifo	Base+400h	R/W	110	Test FIFO
cnfgA	Base+400h	R	111	Configuration Register A
cnfgB	Base+401h	R/W	111	Configuration Register B
ecr	Base+402h	R/W	All	Extended Control Register

Note: The base addresses are specified by CR60 and 61, which are determined by configuration register or hardware setting.

Table 11-6 Bit Map of the ECP Registers

	D7	D6	D5	D4	D3	D2	D1	D0	NOTE
Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	
ecpAFifo	Addr/RLE	Address or RLE field							2
Dsr	nBusy	nAck	PError	Select	nFault	1	1	1	1
Dcr	1	1	Directio	ackIntEn	SelectIn	nInit	Autofd	strobe	1
cFifo	Parallel Port Data FIFO								2
ecpFifo	ECP Data FIFO								2
tFifo	Test FIFO								2
cnfgA	0	0	0	1	0	0	0	0	
cnfgB	compress	intrValue	1	1	1	1	1	1	
Ecr	MODE			nErrIntrEn	dmaEn	serviceIntr	full	empty	

Notes:

1. These registers are available in all modes.
2. All FIFOs use one common 16-byte FIFO.

Each register (or pair of registers, in some cases) is discussed below.

11.3.2 Data and ecpAFifo Port

Modes 000 (SPP) and 001 (PS/2) (Data Port)

During a write operation, the Data Register latches the contents of the data bus on the rising edge of the input, and the contents of this register are output to PD0-PD7. During a read operation, ports PD0-PD7 are read and output to the host. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Mode 011 (ECP FIFO-Address/RLE)

A data byte written to this address is placed in the FIFO and tagged as an ECP Address/RLE. The hardware at the ECP port transmits this byte to the peripheral automatically. This operation is defined only for the forward direction. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	Address/RLE	Address or RLE						

11.3.3 Device Status Register (DSR)

These bits are logical 0 during a read of the Printer Status Register. The bits of this status register are defined as follows:

BIT	7	6	5	4	3	2	1	0
NAME	nBusy	nAck	PError	Select	nFault	1	1	1

BIT	DESCRIPTION
7	nBusy. This bit reflects the complement of the Busy input.
6	nAck. This bit reflects the nAck input.
5	PError. This bit reflects the PError input.
4	Select. This bit reflects the Select input.
3	nFault. This bit reflects the nFault input.
2-0	These three bits are not implemented and are always logical 1 during a read.

11.3.4 Device Control Register (DCR)

The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME			Director	ackInEn	SelectIn	nInit	Autofd	Strobe
DEFAULT	1	1	NA	NA	NA	NA	NA	NA

BIT	DESCRIPTION
7-6	These two bits are always read as logical 1 and cannot be written.
5	**Director.** If the mode is 000 or 010, this bit has no effect and the direction is always out. In other modes, 0: The parallel port is in the output mode. 1: The parallel port is in the input mode.
4	**ackInEn** (Interrupt Request Enable). When this bit is set to logical 1, it enables interrupt requests from the parallel port to the CPU on the low-to-high transition on ACK#.
3	**SelectIn.** This bit is inverted and output to the SLIN# output. 0: The printer is not selected. 1: The printer is selected.
2	**nInit.** This bit is output to the INIT# output.
1	**Autofd.** This bit is inverted and output to the AFD# output.
0	**Strobe.** This bit is inverted and output to the STB# output.

11.3.5 CFIFO (Parallel Port Data FIFO) Mode = 010

This mode is defined only for the forward direction. Bytes written or DMAed to this FIFO are transmitted by a hardware handshake to the peripheral using the standard parallel port protocol. Transfers to the FIFO are byte-aligned.

11.3.6 ECPDFIFO (ECP Data FIFO) Mode = 011

When the direction bit is 0, bytes written or DMAed to this FIFO are transmitted by a hardware handshake to the peripheral using the ECP parallel port protocol. Transfers to the FIFO are byte-aligned.

When the direction bit is 1, data bytes from the peripheral are read via automatic hardware handshake from ECP into this FIFO. Reads or DMAs from the FIFO return bytes of ECP data to the system.

11.3.7 TFIFO (Test FIFO Mode) Mode = 110

Data bytes may be read, written, or DMAed to or from the system to this FIFO in any direction. Data in the tFIFO is not transmitted to the parallel port lines. However, data in the tFIFO may be displayed on the parallel port data lines.

11.3.8 CNFGA (Configuration Register A) Mode = 111

This register is a read-only register. When it is read, 10H is returned. This indicates that this is an 8-bit implementation.

11.3.9 CNFGB (Configuration Register B) Mode = 111

The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	COMPRESS	intrVALUE	IRQx2	IRQx1	IRQx0			
DEFAULT	0	0	0	0	0	1	1	1

BIT	DESCRIPTION
7	**Compress.** This bit is read-only. It is logical 0 during a read, which means that this chip does not support hardware RLE compression.
6	**intrValue.** Returns the value on the ISA IRQ line to determine possible conflicts.
5	**IRQx2.**
4	**IRQx1.**
3	**IRQx0.**

Reflects the IRQ resource assigned for ECP port.

cnfgB[5:3]	IRQ resource
000	Reflects other IRQ resources selected by PnP register (default)
001	IRQ7
010	IRQ9
011	IRQ10
100	IRQ11
101	IRQ14
110	IRQ15
111	IRQ5

2-0	These three bits are logical 1 during a read and can be written.

11.3.10 ECR (Extended Control Register) Mode = all

This register controls the extended ECP parallel port functions. The bit definitions are follows:

BIT	7	6	5	4	3	2	1	0
NAME	MODE	MODE	MODE	nErrIntrEn	dmaEn	ServiceIntr	Full	Empty
DEFAULT	0	0	0	1	0	1	0	1

<table>
<tr><th>BIT</th><th>DESCRIPTION</th></tr>
<tr><td>7-5</td><td>Mode. Read/Write. These bits select the mode.

<table>
<tr><td>000</td><td>Standard Parallel Port (SPP) mode. The FIFO is reset in this mode.</td></tr>
<tr><td>001</td><td>PS/2 Parallel Port mode. This is the same as SPP mode except that direction may be used to tri-state the data lines. Furthermore, reading the data register returns the value on the data lines, not the value in the data register.</td></tr>
<tr><td>010</td><td>Parallel Port FIFO mode. This is the same as SPP mode except that bytes are written or DMAed to the FIFO. FIFO data are automatically transmitted using the standard parallel port protocol. This mode is useful only when direction is 0.</td></tr>
<tr><td>011</td><td>ECP Parallel Port Mode. When the direction is 0 (forward direction), bytes placed into the ecpDFifo and bytes written to the ecpAFifo are placed in a single FIFO and automatically transmitted to the peripheral using the ECP Protocol. When the direction is 1 (reverse direction), bytes are moved from the ECP parallel port and packed into bytes in the ecpDFifo.</td></tr>
<tr><td>100</td><td>EPP Mode. EPP mode is activated if the EPP mode is selected.</td></tr>
<tr><td>101</td><td>Reserved.</td></tr>
<tr><td>110</td><td>Test Mode. The FIFO may be written and read in this mode, but the data is not transmitted on the parallel port.</td></tr>
<tr><td>111</td><td>Configuration Mode. The confgA and confgB registers are accessible at 0x400 and 0x401 in this mode.</td></tr>
</table></td></tr>
<tr><td>4</td><td>nErrIntrEn. Read/Write (Valid only in ECP Mode)
0: Enables the interrupt generated on the falling edge of nFault. This prevents interrupts from being lost in the time between the read of the ECR and the write of the ECR.
1: Disables the interrupt generated on the asserting edge of nFault.</td></tr>
<tr><td>3</td><td>dmaEn. Read/Write.
0: Disable DMA unconditionally.
1: Enable DMA.</td></tr>
<tr><td>2</td><td>serviceIntr. Read/Write.
0: Enable one of the following cases of interrupts. When one of the serviced interrupts occurs, this bit is set to logical 1 by the hardware. This bit must be reset to logical 0 to re-enable the interrupts.
(a) dmaEn = 1: During DMA, this bit is set to logical 1 when terminal count is reached.
(b) dmaEn = 0, direction = 0: This bit is set to logical 1 whenever there are writeIntr threshold or more bytes free in the FIFO.
(c) dmaEn = 0, direction = 1: This bit is set to logical 1 whenever there are readIntr threshold or more valid bytes to be read from the FIFO.
1: Disable DMA and all of the service interrupts. Writing a logical 1 to this bit does not cause an interrupt.</td></tr>
</table>

Continued

BIT	DESCRIPTION
1	**Full.** Read Only. 0: The FIFO has at least one free byte. 1: The FIFO is completely full; it cannot accept another byte.
0	**Empty.** Read Only. 0: The FIFO contains at least one byte of data. 1: The FIFO is completely empty.

11.3.11 ECP Pin Descriptions

NAME	TYPE	DESCRIPTION
NStrobe (HostClk)	O	This pin loads data or address into the slave on its asserting edge during write operations. This signal handshakes with Busy.
PD<7:0>	I/O	These signals contain address, data or RLE data.
nAck (PeriphClk)	I	This signal indicates valid data driven by the peripheral when asserted. This signal handshakes with nAutoFd in reverse.
Busy (PeriphAck)	I	This signal deasserts to indicate that the peripheral can accept data. In the reverse direction, it indicates whether the data lines contain ECP command information or data. Normal data are transferred when Busy (PeriphAck) is high, and an 8-bit command is transferred when it is low.
PError (nAckReverse)	I	This signal is used to acknowledge a change in the direction of the transfer (asserted = forward). The peripheral drives this signal low to acknowledge nReverseRequest. The host relies upon nAckReverse to determine when it is permitted to drive the data bus.
Select (Xflag)	I	Indicates printer on-line.
NautoFd (HostAck)	O	Requests a byte of data from the peripheral when it is asserted. In the forward direction, this signal indicates whether the data lines contain ECP address or data. Normal data are transferred when nAutoFd (HostAck) is high, and an 8-bit command is transferred when it is low.
nFault (nPeriphReuqest)	I	Generates an error interrupt when it is asserted. This signal is valid only in the forward direction. The peripheral is permitted (but not required) to drive this pin low to request a reverse transfer during ECP mode.
nInit (nReverseRequest)	O	This signal sets the transfer direction (asserted = reverse, deasserted = forward). This pin is driven low to place the channel in the reverse direction.
nSelectIn (ECPMode)	O	This signal is always deasserted in ECP mode.

11.3.12 ECP Operation

The host must negotiate on the parallel port to determine if the peripheral supports the ECP protocol before ECP operation. After negotiation, it is necessary to initialize some of the port bits.

(a) Set direction = 0, enabling the drivers.

(b) Set strobe = 0, causing the nStrobe signal to default to the deasserted state.

(c) Set autoFd = 0, causing the nAutoFd signal to default to the deasserted state.

(d) Set mode = 011 (ECP Mode)

ECP address/RLE bytes or data bytes may be sent automatically by writing the ecpAFifo or ecpDFifo, respectively.

11.3.12.1 Mode Switching

The software must handle P1284 negotiation and all operations prior to a data transfer in SPP or PS/2 modes (000 or 001). The hardware provides an automatic control line handshake, moving data between the FIFO and the ECP port, only in the data transfer phase (mode 011 or 010).

If the port is in mode 000 or 001, it may switch to any other mode. If the port is not in mode 000 or 001, it can only be switched into mode 000 or 001. The direction can only be changed in mode 001.

In extended forward mode, the software should wait for the FIFO to be empty before switching back to mode 000 or 001. In ECP reverse mode, the software should wait for all the data to be read from the FIFO before changing back to mode 000 or 001.

11.3.12.2 Command/Data

ECP mode allows the transfer of normal 8-bit data or 8-bit commands. In the forward direction, normal data are transferred when HostAck is high, and an 8-bit command is transferred when HostAck is low. The most significant bits of the command indicate whether it is a run-length count (for compression) or a channel address.

In the reverse direction, normal data are transferred when PeriphAck is high, and an 8-bit command is transferred when PeriphAck is low. The most significant bit of the command is always zero.

11.3.12.3 Data Compression

The W83627UHG hardware supports RLE decompression and can transfer compressed data to a peripheral. Odd (RLE) compression is not supported in the hardware, however. In order to transfer data in ECP mode, the compression count is written to ecpAFifo and the data byte is written to ecpDFifo.

11.3.12.4 FIFO Operation

The FIFO threshold is set in CR5. All data transferred to or from the parallel port can proceed in DMA or Programmed I/O (non-DMA) mode, as indicated by the selected mode. The FIFO is used in Parallel Port FIFO mode or ECP Parallel Port Mode. After a reset, the FIFO is disabled.

11.3.13 DMA Transfers

DMA transfers are always to or from the ecpDFifo, tFifo, or CFifo. DMA uses the standard PC DMA services. The ECP requests DMA transfers from the host by activating the PDRQ pin. The DMA empties or fills the FIFO using the appropriate direction and mode. When the terminal count in the DMA controller is reached, an interrupt is generated, and serviceIntr is asserted, which will disable the DMA.

11.3.14 Programmed I/O (NON-DMA) Mode

The ECP and parallel port FIFOs can also be operated using interrupt-driven, programmed I/O. Programmed I/O transfers are

1. To the ecpDFifo at 400H and ecpAFifo at 000H
2. From the ecpDFifo located at 400H
3. To / from the tFifo at 400H.

The host must set dmaEn and serviceIntr to 0 and also must set the direction and state accordingly in the programmed I/O transfers.

The ECP requests programmed I/O transfers from the host by activating the IRQ pin. The programmed I/O empties or fills the FIFO using the appropriate direction and mode.

12. KEYBOARD CONTROLLER

The W83627UHG KBC (8042 with licensed KB BIOS) circuit is designed to provide the functions needed to interface a CPU with a keyboard and/or a PS/2 mouse and can be used with IBM®-compatible personal computers or PS/2-based systems. The controller receives serial data from the keyboard or PS/2 mouse, checks the parity of the data, and presents the data to the system as a byte of data in its output buffer. Then, the controller asserts an interrupt to the system when data are placed in its output buffer. The keyboard and PS/2 mouse are required to acknowledge all data transmissions. No transmission should be sent to the keyboard or PS/2 mouse until an acknowledgement is received for the previous data byte.

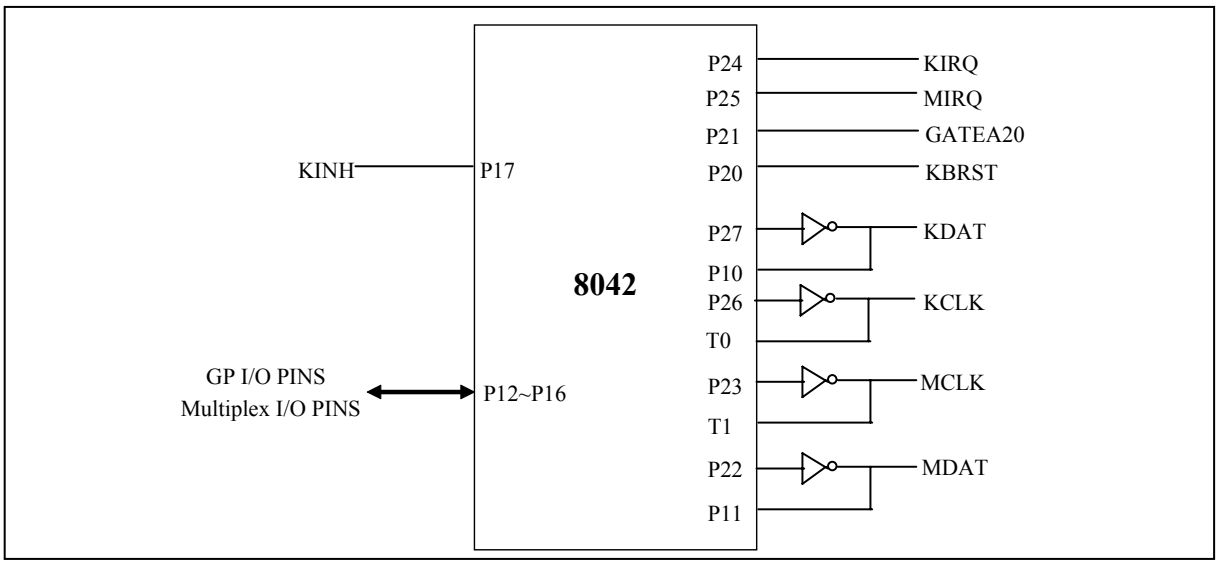


Figure 12-1 Keyboard and Mouse Interface

12.1 Output Buffer

The output buffer is an 8-bit, read-only register at I/O address 60H (Default, PnP programmable I/O address LD5-CR60 and LD5-CR61). The keyboard controller uses the output buffer to send the scan code (from the keyboard) and required command bytes to the system. The output buffer can only be read when the output buffer full bit in the register (in the status register) is logical 1.

12.2 Input Buffer

The input buffer is an 8-bit, write-only register at I/O address 60h or 64h (Default, PnP programmable I/O address LD5-CR60, LD5-CR61, LD5-CR62, and LD5-CR63). Writing to address 60h sets a flag to indicate a data write; writing to address 64h sets a flag to indicate a command write. Data written to I/O address 60h is sent to the keyboard (unless the keyboard controller is expecting a data byte) through the controller's input buffer only if the input buffer full bit (in the status register) is logical 0.

12.3 Status Register

The status register is an 8-bit, read-only register at I/O address 64H (Default, PnP programmable I/O address LD5-CR62 and LD5-CR63) that holds information about the status of the keyboard controller and interface. It may be read at any time.

Table 12-1 Bit Map of Status Register

BIT	BIT FUNCTION	DESCRIPTION
0	Output Buffer Full	0: Output buffer empty 1: Output buffer full
1	Input Buffer Full	0: Input buffer empty 1: Input buffer full
2	System Flag	This bit may be set to 0 or 1 by writing to the system flag bit in the command byte of the keyboard controller. It defaults to 0 after a power-on reset.
3	Command/Data	0: Data byte 1: Command byte
4	Inhibit Switch	0: Keyboard is inhibited 1: Keyboard is not inhibited
5	Auxiliary Device Output Buffer	0: Auxiliary device output buffer empty 1: Auxiliary device output buffer full
6	General Purpose Time-out	0: No time-out error 1: Time-out error
7	Parity Error	0: Odd parity 1: Even parity (error)

12.4 Commands

Table 12-2 KBC Command Sets

<table>
<tr><th>COMMAND</th><th>FUNCTION</th></tr>
<tr><td>20h</td><td>Read Command Byte of Keyboard Controller</td></tr>
<tr><td>60h</td><td>Write Command Byte of Keyboard Controller
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>7</td><td>Reserved</td></tr>
<tr><td>6</td><td>IBM Keyboard Translate Mode</td></tr>
<tr><td>5</td><td>Disable Auxiliary Device</td></tr>
<tr><td>4</td><td>Disable Keyboard</td></tr>
<tr><td>3</td><td>Reserve</td></tr>
<tr><td>2</td><td>System Flag</td></tr>
<tr><td>1</td><td>Enable Auxiliary Interrupt</td></tr>
<tr><td>0</td><td>Enable Keyboard Interrupt</td></tr>
</table></td></tr>
<tr><td>A4h</td><td>Test Password
Returns 0Fah if Password is loaded
Returns 0F1h if Password is not loaded</td></tr>
<tr><td>A5h</td><td>Load Password
Load Password until a logical 0 is received from the system</td></tr>
<tr><td>A6h</td><td>Enable Password
Enable the checking of keystrokes for a match with the password</td></tr>
<tr><td>A7h</td><td>Disable Auxiliary Device Interface</td></tr>
<tr><td>A8h</td><td>Enable Auxiliary Device Interface</td></tr>
<tr><td>A9h</td><td>Interface Test
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>00</td><td>No Error Detected</td></tr>
<tr><td>01</td><td>Auxiliary Device "Clock" line is stuck low</td></tr>
<tr><td>02</td><td>Auxiliary Device "Clock" line is stuck high</td></tr>
<tr><td>03</td><td>Auxiliary Device "Data" line is stuck low</td></tr>
<tr><td>04</td><td>Auxiliary Device "Data" line is stuck low</td></tr>
</table></td></tr>
<tr><td>AAh</td><td>Self-test
Returns 055h if self-test succeeds</td></tr>
</table>

KBC Command Sets, continued

COMMAND	FUNCTION
ABh	Interface Test BIT / BIT DEFINITION 00 — No Error Detected 01 — Keyboard "Clock" line is stuck low 02 — Keyboard "Clock" line is stuck high 03 — Keyboard "Data" line is stuck low 04 — Keyboard "Data" line is stuck high
ADh	Disable Keyboard Interface
AEh	Enable Keyboard Interface
C0h	Read Input Port (P1) and send data to the system
C1h	Continuously puts the lower four bits of Port1 into the STATUS register
C2h	Continuously puts the upper four bits of Port1 into the STATUS register
D0h	Send Port 2 value to the system
D1h	Only set / reset GateA20 line based on system data bit 1
D2h	Send data back to the system as if it came from the Keyboard
D3h	Send data back to the system as if it came from Auxiliary Device
D4h	Output next received byte of data from system to Auxiliary Device
E0h	Reports the status of the test inputs
FXh	Pulse only RC (the reset line) low for 6μs if the Command byte is even

12.5 Hardware GATEA20/Keyboard Reset Control Logic

The KBC includes hardware control logic to speed-up GATEA20 and KBRESET. This control logic is controlled by LD5-CRF0 as follows:

12.5.1 KB Control Register (Logic Device 5, CR-F0)

BIT	7	6	5	4	3	2	1	0
NAME	KCLKS1	KCLKS0	RESERVED			P92EN	HGA20	HKBRST
DEFAULT	1	0	0	0	0	0	0	0

BIT	DESCRIPTION	
7	**KCLKS1**.	Select the KBC clock rate. **Bits** **7 6** 0 0: KBC clock input is 6 MHz. 0 1: KBC clock input is 8 MHz. 1 0: KBC clock input is 12 MHz. 1 1: KBC clock input is 16 MHz.
6	**KCLKS0**.	
5-3	**RESERVED**.	
2	**P92EN** (Port 92 Enable). 1: Enables Port 92 to control GATEA20 and KBRESET. 0: Disables Port 92 functions.	
1	**HGA20** (Hardware GATEA 20). 1: Selects hardware GATE A20 control logic to control GATE A20 signal. 0: Disables GATEA20 control logic functions.	
0	**HKBRST** (Hardware Keyboard Reset). 1: Selects hardware KB RESET control logic to control KBRESET signal. 0: Disables hardware KB RESET control logic function.	

When the KBC receives data that follows a "D1" command, the hardware control logic sets or clears GATE A20 according to received data bit 1. Similarly, the hardware control logic sets or clears KBRESET depending on received data bit 0. When the KBC receives an "FE" command, the KBRESET is pulse low for 6 μs (Min.) with a 14 μs (Min.) delay.

GATE A20 and KBRESET are controlled by either software or hardware logic, and they are mutually exclusive. Then, GATE A20 and KBRESET are merged with Port92 when the P92EN bit is set.

12.5.2 Port 92 Control Register (Default Value = 0x24)

BIT	7	6	5	4	3	2	1	0
NAME	RES. (0)		RES. (1)	RES. (0)		RES. (1)	SGA20	PLKBRST
DEFAULT	0	0	1	0	0	1	0	0

BIT	DESCRIPTION
7-6	RES. (0)
5	RES. (1)
4-3	RES. (0)
2	RES. (1)
1	**SGA20** (Special GATE A20 Control) 1: Drives GATE A20 signal to high. 0: Drives GATE A20 signal to low.
0	**PLKBRST** (Pulled-low KBRESET). A logical 1 on this bit causes KBRESET to drive low for 6 µS(Min.) with a 14 µS(Min.) delay. Before issuing another keyboard-reset command, the bit must be cleared.

13. POWER MANAGEMENT EVENT

The PME# (pin 86) signal is connected to the South Bridge and is used to wake up the system from S1 ~ S5 sleeping states.

One control bit and four registers in the W83627UHG are associated with the PME function. The control bit is at Logical Device A, CR[F2h], bit[0] and is for enabling or disabling the PME function. If this bit is set to "0", the W83627UHG won't output any PME signal when any of the wake-up events has occurred and is enabled. The four registers are divided into PME status registers and PME interrupt registers of wake-up events [Note.1].

1) The PME status registers of wake-up event:
   - At Logical Device A, CR[F3h] and CR[F4h]
   - Each wake-up event has its own status
   - The PME status should be cleared by writing a "1" before enabling its corresponding bit in the PME interrupt registers
2) The PME interrupt registers of wake-up event:
   - At Logical Device A, CR[F6h] and CR[F7h]
   - Each wake-up event can be enabled / disabled individually to generate a PME# signal

Note.1 PME wake-up events that the W83627UHG supports include:

- Mouse IRQ event
- Keyboard IRQ event
- Printer IRQ event
- Floppy IRQ event
- UART A IRQ event
- UART B IRQ event
- UART C IRQ event
- UART D IRQ event
- UART E IRQ event
- UART F IRQ event
- Hardware Monitor IRQ event
- WDTO# event
- RIB (UARTB Ring Indicator) event

13.1 Power Control Logic

This chapter describes how the W83627UHG implements its ACPI function via these power control pins: PSIN# (Pin 68), PSOUT# (Pin 67), SUSB# (i.e. SLP_S3#; Pin 73) and PSON# (Pin 72). The following figure illustrates the relationships.

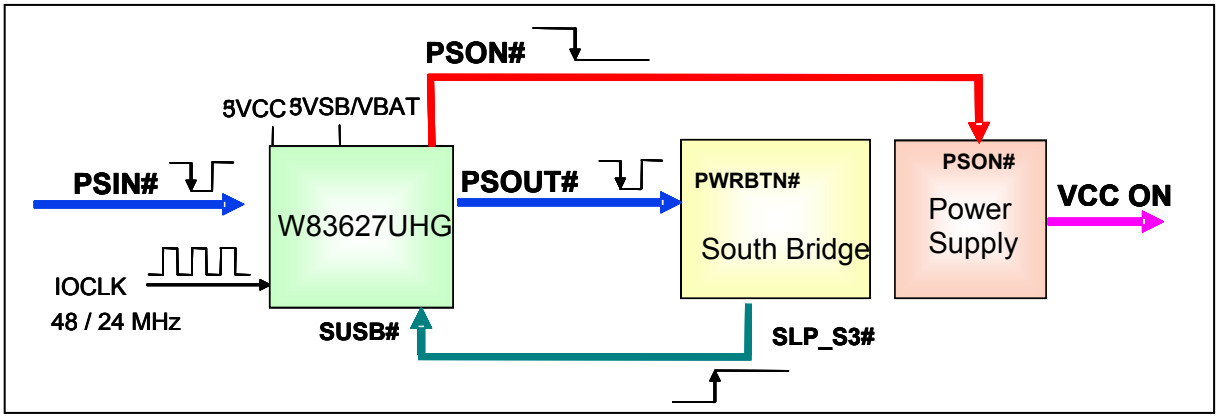


Figure 13-1 Power Control Mechanism

13.1.1 PSON# Logic

13.1.1.1 Normal Operation

The PSOUT# signal will be asserted low if the PSIN# signal is asserted low. The PSOUT# signal is held low for as long as the PSIN# is held low. The South Bridge controls the SUSB# signal through the PSOUT# signal. The PSON# is directly connected to the power supply to turn on or off the power.

Figure 13-2 shows the power on and off sequences.

The ACPI state changes from S5 to S0, then to S5

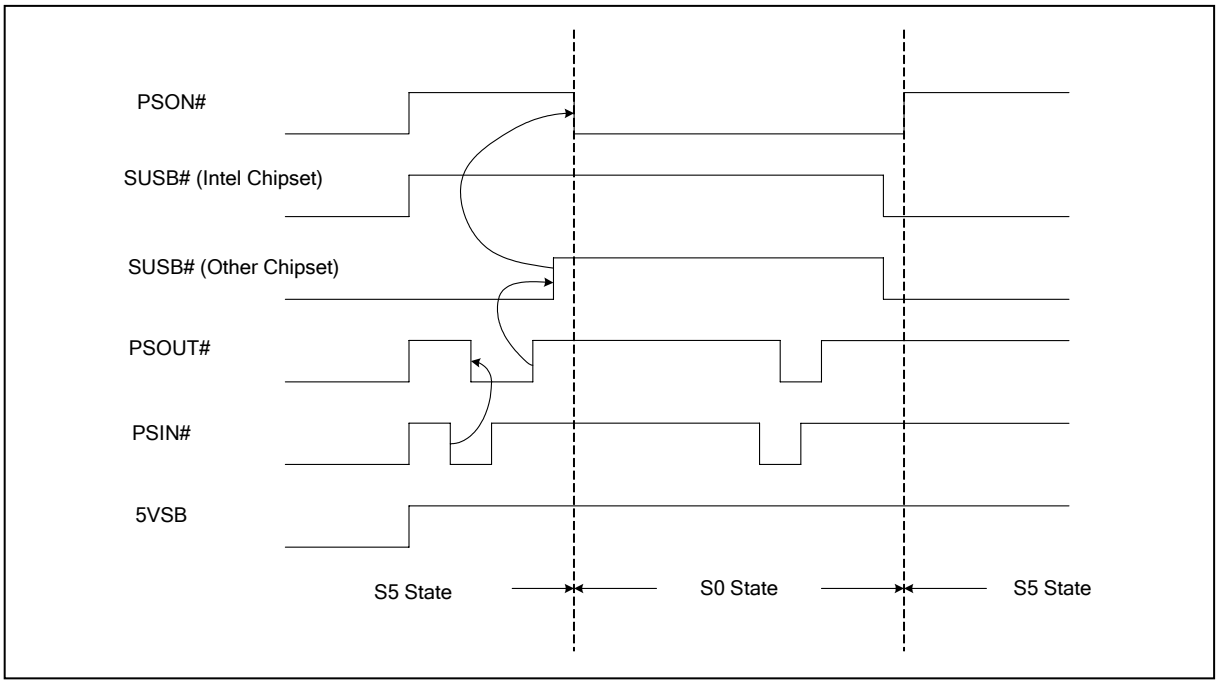


Figure 13-2 Power Sequence from S5 to S0, then back to S5.

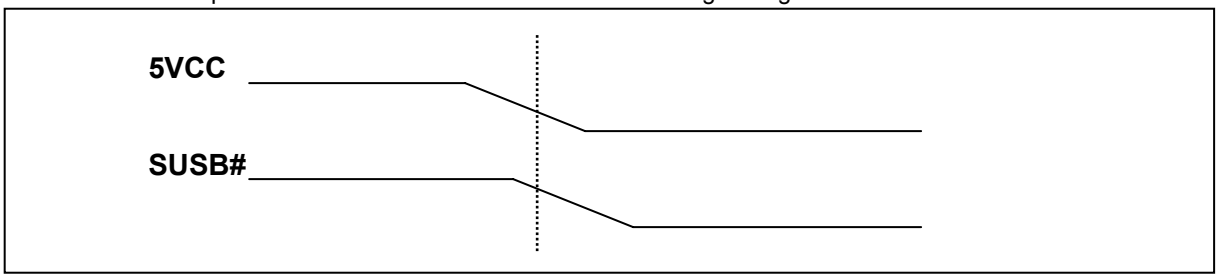
13.1.2 AC Power Failure Resume

By definition, AC power failure means that the standby power is removed. The power failure resume control logic of the W83627UHG is used to recover the system to a pre-defined state after AC power failure. Two control bits at Logical Device A, CR[E4h], bits[6:5] indicate the pre-defined state. The definition of these two bits is listed in the following table:

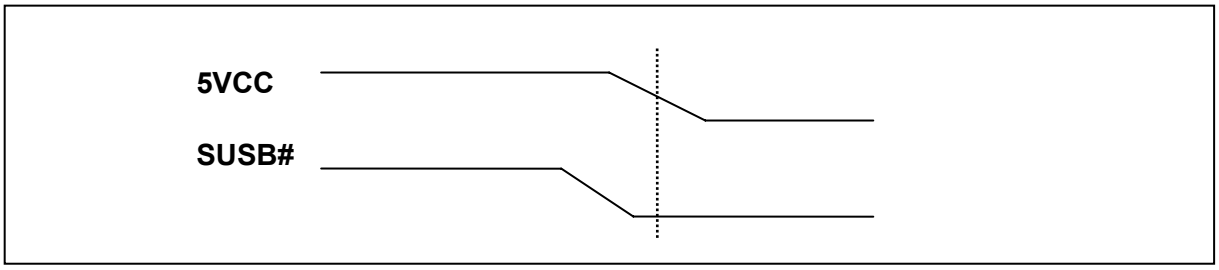
Table 13-1 Bit Map of Logical Device A, CR[E4h], bits [6:5]

LOGICAL DEVICE A, CR[E4H], BITS[6:5]	DEFINITION
00	System always turns off when it returns from AC power failure
01	System always turns on when it returns from AC power failure
10	System turns off / on when it returns from power failure depending on the state before the power failure. (Please see Note 1)
11	User defines the state before the power failure. (The previous state is set at CRE6[4]. Please see Note 2)

Note1. The W83627UHG detects the state before power failure (on or off) through the SUSB# signal and the 5VCC power. The relation is illustrated in the following two figures.



The previous state is “on”, if 5VCC falls to 3.75V and SUSB# keeps at 2.0V.



The previous state is “off”, if 5VCC falls to 3.75V and SUSB# keeps at 0.8V.

Note 2.

Logical Device A, CR[E6h] bit [4]	Definition
0	User defines the state to be “on”
1	User defines the state to be “off”

To ensure that VCC does not fall faster than VSB in various ATX Power Supplies, the W83627UHG adds the option of "user define mode" for the pre-defined state before AC power failure. BIOS can set the pre-defined state to be "On" or "Off". According to this setting, the system is returned to the pre-defined state after the AC power recovery.

13.2 Wake Up the System by Keyboard and Mouse

The W83627UHG generates a low pulse through the PSOUT# pin to wake up the system when it detects a key code pressed or mouse button clicked. The following sections describe how the W83627UHG works.

13.2.1 Waken up by Keyboard events

The keyboard Wake-Up function is enabled by setting Logical Device A, CR[E0h], bit 6 to "1".

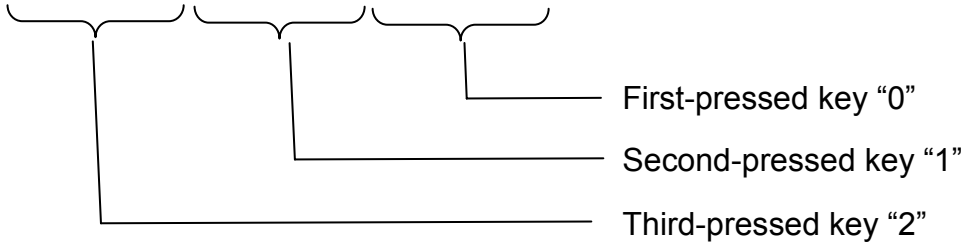
There are two keyboard events that can be used for the wake-up

1) Any key – Set bit 0 at Logical Device A, CR[E0h] to "1" (Default).
2) Specific keys (Password) - Set bit 0 at Logical Device A, CR[E0h] to "0".

Three sets of specific key combinations are stored at Logical Device A. CR[E1h] is an index register to indicate which byte of key code storage (0x00h ~ 0x0Eh, 0x30h ~ 0x3Eh, 0x40h ~ 0x4Eh) is going to be read or written through CR[E2h]. According to IBM 101/102 keyboard specification, a complete key code contains a 1-byte make code and a 2-byte break code. For example, the make code of "0" is 0x45h, and the corresponding break code is 0xF0h, 0x45h.

The approach to implement Keyboard Password Wake-Up Function is to fill key codes into the password storage. Assume that we want to set "012" as the password. The storage should be filled as below. Please note that index 0x09h ~ 0x0Eh must be filled as 0x00h since the password has only three numbers.

Index(CRE1)→	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
Data(CRE2)→	1E	F0	1E	16	F0	16	45	F0	45	00	00	00	00	00	00



13.2.2 Waken up by Mouse events

The mouse Wake-Up function is enabled by setting Logical Device A, CR[E0h], bit 5 to "1".

The following specific mouse events can be used for the wake-up:

- Any button clicked or any movement
- One click of the left or the right button
- One click of the left button
- One click of the right button
- Two clicks of the left button
- Two clicks of the right button.

Three control bits (ENMDAT_UP, MSRKEY, MSXKEY) define the combinations of the mouse wake-up events. Please see the following table for the details.

Table 13-2 Definitions of Mouse Wake-Up Events

ENMDAT_UP (LOGICAL DEVICE A, CR[E6H], BIT 7)	MSRKEY (LOGICAL DEVICE A, CR[E0H], BIT 4)	MSXKEY (LOGICAL DEVICE A, CR[E0H], BIT 1)	WAKE-UP EVENT
1	x	1	Any button clicked or any movement.
1	x	0	One click of the left or right button.
0	0	1	One click of the left button.
0	1	1	One click of the right button.
0	0	0	Two clicks of the left button.
0	1	0	Two clicks of the right button.

13.3 Resume Reset Logic

The RSMRST# (Pin 75) signal is a reset output and is used as the 5VSB power on reset signal for the South Bridge.

When the W83627UHG detects the 5VSB voltage rises to "V1", it then starts a delay – "t1" before the rising edge of RSMRST# asserting. If the 5VSB voltage falls below "V2", the RSMRST# de-asserts immediately.

Timing and voltage parameters are shown in Figure 13-3 and Table 13-3.

Figure 13-3 Mechanism of Resume Reset Logic

Table 13-3 Timing and Voltage Parameters of RSMRST#

NAME	PARAMETER	MIN.	MAX.	UNIT
V1	5VSB Valid Voltage	-	4.3	V
V2	5VSB Ineffective Voltage	2.6	-	V
t1	Valid 5VSB to RSMRST# inactive	100	200	mS

13.4 PWROK Generation

The PWROK (Pin 71) signal is an output and is used as both the 5VCC and 3VCC power-on reset signal.

When the W83627UHG detects both of the 5VCC and 3VCC voltages rise to “V3” and “V5”, it then starts a delay – “t2” before the rising edge of PWROK assertion. If both of the 5VCC and 3VCC voltages fall below “V4” and “V6”, the PWROK de-asserts immediately.

Timing and the voltage parameters are shown in Figure 13-4 and Table 13-4.

Figure 13-4 PWROK Generation Mechanism

Table 13-4 Timing and the Voltage Parameters of PWROK

NAME	PARAMETER	MIN.	MAX.	UNIT
V3	5VCC Valid Voltage	-	4.3	V
V4	5VCC Ineffective Voltage	2.6	-	V
V5	3VCC Valid Voltage	-	2.9	V
V6	3VCC Ineffective Voltage	2.1		V
t2	Valid 5VCC and 3VCC to PWROK active	300	500	mS

Originally, the t2 timing is between 300 mS to 500 mS, but it can be changed to 200 mS to 300 mS by programming Logical Device A, CR[E6h], bit 3 to "1". Furthermore, the W83627UHG provides four different extra delay time of PWROK for various demands. The four extra delay time are designed at Logical Device A, CR[E6h], bits 2~1. The following table shows the definitions of Logical Device A, CR[E6h] bits 3 ~1.

LOGICAL DEVICE A, CR[E6H] BIT	DEFINITION
3	PWROK_DEL (first stage) **(VSB)** Set the delay time when rising from PWROK_LP to PWROK_ST. 0: 300 ~ 500 mS. 1: 200 ~ 300 mS.
2~1	PWROK_DEL **(VSB)** Set the delay time when rising from PWROK_ST to PWROK. 00: No delay time. 01: Delay 32 ms 10: 96 ms 11: Delay 250 ms

For example, if Logical Device A, CR[E6h] bit 2 is set to "0" and bits 2~1 are set to "10", the range of t2 timing is from 396(300 + 96) mS to 596(500 + 96) mS.

14. SERIALIZED IRQ

The W83627UHG supports a serialized IRQ scheme. This allows a signal line to be used to report the parallel interrupt requests. Since more than one device may need to share the signal serial SERIRQ signal, an open drain signal scheme is employed. The clock source is the PCI clock. The serialized interrupt is transferred on the SERIRQ signal, one cycle consisting of three frames types: the Start Frame, the IRQ/Data Frame, and the Stop Frame.

14.1 Start Frame

There are two modes of operation for the SERIRQ Start Frame: the Quiet mode and the Continuous mode.

In the Quiet mode, the W83627UHG drives the SERIRQ signal active low for one clock, and then tri-states it. This brings all the state machines of the W83627UHG from idle to active states. The host controller (the South Bridge) then takes over driving SERIRQ signal low in the next clock and continues driving the SERIRQ low for programmable 3 to 7 clock periods. This makes the total number of clocks low 4 to 8 clock periods. After these clocks, the host controller drives the SERIRQ high for one clock and then tri-states it.

In the Continuous mode, the START Frame can only be initiated by the host controller to update the information of the IRQ/Data Frame. The host controller drives the SERIRQ signal low for 4 to 8 clock periods. Upon a reset, the SERIRQ signal is defaulted to the Continuous mode for the host controller to initiate the first Start Frame.

Please see the diagram below for more details.

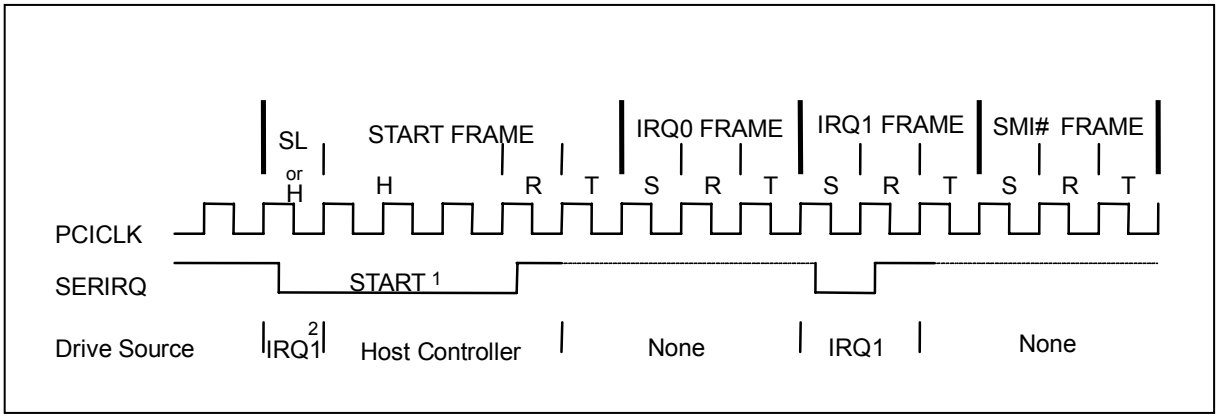


Figure 14-1 Start Frame Timing with Source Sampled A Low Pulse on IRQ1

H=Host Control SL=Slave Control R=Recovery T=Turn-around S=Sample

Note:

1. The Start Frame pulse can be 4-8 clocks wide.
2. The first clock of Start Frame is driven low by the W83627UHG because IRQ1 of the W83627UHG needs an interrupt request. Then the host takes over and continues to pull the SERIRQ low.

14.2 IRQ/Data Frame

Once the Start Frame has been initiated, the W83627UHG must start counting frames based on the rising edge of the start pulse. Each IRQ/Data Frame has three clocks: the Sample phase, the Recovery phase, and the Turn-around phase.

During the Sample phase, the W83627UHG drives SERIRQ low if the corresponding IRQ is active. If the corresponding IRQ is inactive, then SERIRQ must be left tri-stated. During the Recovery phase, the W83627UHG device drives the SERIRQ high. During the Turn-around phase, the W83627UHG device leaves the SERIRQ tri-stated. The W83627UHG starts to drive the SERIRQ line from the beginning of "IRQ0 FRAME" based on the rising edge of PCICLK.

The IRQ/Data Frame has a specific numeral order, as shown in Table 14-1.

Table 14-1 SERIRQ Sampling Periods

SERIRQ SAMPLING PERIODS			
IRQ/DATA FRAME	**SIGNAL SAMPLED**	**# OF CLOCKS PAST START**	**EMPLOYED BY**
1	IRQ0	2	-
2	IRQ1	5	Keyboard
3	SMI#	8	-
4	IRQ3	11	UART B
5	IRQ4	14	UART A
6	IRQ5	17	-
7	IRQ6	20	FDC
8	IRQ7	23	LPT
9	IRQ8	26	-
10	IRQ9	29	-
11	IRQ10	32	-
12	IRQ11	35	-
13	IRQ12	38	Mouse
14	IRQ13	41	-
15	IRQ14	44	-
16	IRQ15	47	-
17	IOCHCK#	50	-
18	INTA#	53	-
19	INTB#	56	-
20	INTC#	59	-
21	INTD#	62	-
32:22	Unassigned	95	-

14.3 Stop Frame

After all IRQ/Data Frames have completed, the host controller will terminates SERIRQ with a Stop frame. Only the host controller can initiate the Stop Frame by driving SERIRQ low for 2 or 3 clocks. If the Stop Frame is low for 2 clocks, the Sample mode of next SERIRQ cycle's Sample mode is the Quiet mode. If the Stop Frame is low for 3 clocks, the Sample mode of next SERIRQ cycle is the Continuous mode.

Please see the diagram below for more details.

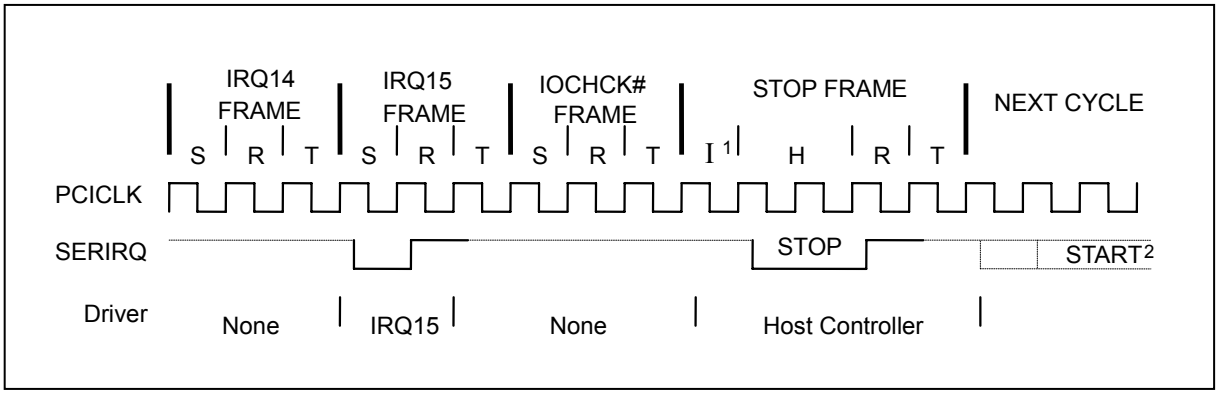


Figure 14-2 Stop Frame Timing with Host Using 17 SERIRQ Sampling Period

H=Host Control R=Recovery T=Turn-around S=Sample I= Idle.

Note:

1. There may be none, one or more Idle states during the Stop Frame.
2. The Start Frame pulse of next SERIRQ cycle may or may not start immediately after the turn-around clock of the Stop Frame.

15. WATCHDOG TIMER

Pin 77 is the WDTO# pin in the W83627UHG.

The Watchdog Timer of the W83627UHG consists of an 8-bit programmable time-out counter and a control and status register. The time-out counter ranges from 1 to 255 minutes in the minute mode, or 1 to 255 seconds in the second mode. The units of Watchdog Timer counter are selected at Logical Device 8, CR[F5h], bit[3]. The time-out value is set at Logical Device 8, CR[F6h]. Writing zero disables the Watchdog Timer function. Writing any non-zero value to this register causes the counter to load this value into the Watchdog Timer counter and start counting down.

The W83627UHG outputs a low signal to the WDTO# pin (pin 77) when a time-out event occurs. In other words, when the value is counted down to zero, the timer stops, and the W83627UHG sets the WDTO# status bit in Logical Device 8, CR[F7h], bit[4], outputting a low signal to the WDTO# pin(pin 77). Writing a zero will clear the status bit and the WDTO# pin returns to high. Writing a zero will clear the status bit. This bit will also be cleared if LRESET# or PWROK# signal is asserted.

Please note that the output type of WDTO# (pin 77) is open-drain.

16. GENERAL PURPOSE I/O

16.1 GPIO Architecture

The W83627UHG provides 45 input/output ports that can be individually configured to perform a simple basic I/O function or an alternative, pre-defined function. GPIO ports 1 ~2 are configured through control registers in Logical Device 9, GPIO ports 3~4 in Logical Device 7, and GPIO ports 5~6 in Logic Device 8. Users can configure each individual port to be an input or output port by programming respective bit in the selection register (0 = output, 1 = input). Invert port value by setting inversion register (0 = non -inverse, 1 = inverse). The port value is read / written through data registers.

In addition, only GP25, GP26 and GP27 are designed to be able to assert PSOUT# or PME# signal to wake up the system if any of them has any transitions. The rising or falling edge can be set to perform the wake-up function. The following table gives a more detailed register map on GP25, GP26 and GP27.

Table 16-1 Relative Control Registers of GPIO 25, 26 and 27 that Support Wake-Up Function

	EVENTROUTE I (PSOUT#) **0: DISABLE** **1: ENABLE**	**EVENTROUTE II (PME#)** **0: DISABLE** **1: ENABLE**	**EVENT POLARITY** **0 : RISING** **1 : FALLING**	**EVENT STATUS**
GP25	LDA, CR[FEh] bit4	LDA, CR[FEh] bit0	LD9, CR[E6h] bit5	LD9, CR[E7h] bit5
GP26	LDA, CR[FEh] bit5	LDA, CR[FEh] bit1	LD9, CR[E6h] bit6	LD9, CR[E7h] bit6
GP27	LDA, CR[FEh] bit6	LDA, CR[FEh] bit2	LD9, CR[E6h] bit7	LD9, CR[E7h] bit7

16.2 Access Channels

There are two different channels to set up/access the GPIO ports. The first one is the indirect access via register 2E/2F (4E/4F, it depends by HEFRAS trapping). The registers can be read / written only when the respective logical device ID and port number are selected.

The other is the direct access through GPIO register table that can be configured by {CR61, CR60} of logic device 8. The mapped 5 registers are defined in table 11.2. Since the base address is set, the GPIO number can be selected by writing the group number to GSR [INDEX] (GPIO Select Register, #1~#6 for GPIO1 ~ GPIO6 respectively; #0 and #7 is invalid for GSR [INDEX]). Then the I/O register, the Data register and the Inversion register are mapped to addresses Base+0, Base+1 and Base+2 respectively. Only one GPIO can be accessed at one time. The chip will ignore more than one “1” written in GSR. The most significant bit (MSB) is with higher priority.

Table 16-2 GPIO Register Addresses

ADDRESS	ABBR	BIT NUMBER							
		7	6	5	4	3	2	1	0
Base + 0	GSR	Reserved					INDEX		
Base + 1	IOR	GPIO I/O Register							
Base + 2	DAT	GPIO Data Register							
Base + 3	INV	GPIO Inversion Register							
Base + 4	DST	GPIO Status Register							

17. CONFIGURATION REGISTER

17.1 Chip (Global) Control Register

CR 02h. (Software Reset; Write Only)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	Write "1" Only	Software RESET.

CR 07h. (Logical Device; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Logical Device Number.

CR 20h. (Chip ID, MSB; Read Only)

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only	Chip ID number = A2h (high byte).

CR 21h. (Chip ID, LSB; Read Only)

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only	Chip ID number = 3xh (low byte). x is the IC version

CR 22h. (Device Power Down; Default FFh)

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	HM Power Down. 0: Powered down 1: Not powered down
5	R / W	UARTB Power Down. 0: Powered down 1: Not powered down
4	R / W	UARTA Power Down. 0: Powered down 1: Not powered down
3	R / W	PRT Power Down. 0: Powered down 1: Not powered down
2~1	Reserved.	
0	R / W	FDC Power Down. 0: Powered down 1: Not powered down

CR 23h. (IPD&Device Power Down; Default F0h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	UARTF Power Down 0: Powered down 1: Not powered down
6	R / W	UARTE Power Down 0: Powered down 1: Not powered down
5	R / W	UARTD Power Down. 0: Powered down 1: Not powered down

CR 23h. (IPD&Device Power Down; Default F0h), continued

BIT	READ / WRITE	DESCRIPTION
4	R / W	UARTC Power Down. 0: Powered down 1: Not powered down
3~1	Reserved.	
0	R / W	IPD (Immediate Power Down). When set to 1, the whole chip is put into power-down mode immediately.

CR 24h. (Global Option; Default 0100_0ss0b) s: value by strapping

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	CLKSEL => Input clock rate selection = 0 The clock input on pin 18 is 24 MHz. = 1 The clock input on pin 18 is 48 MHz. (Default)
5	Reserved.	
4	R / W	Select output type of SYSFANOUT =0 SYSFANOUT is Open-drain. (Default) =1 SYSFANOUT is Push-pull.
3	R / W	Select output type of CPUFANOUT0 =0 CPUFANOUT is Open-drain. (Default) =1 CPUFANOUT is Push-pull.
2	Read Only	ENKBC => Enable keyboard controller = 0 KBC is disabled after hardware reset. = 1 KBC is enabled after hardware reset. This bit is read-only, and it is set or reset by a power-on strapping pin (Pin 54, SOUTA).
1	R / W	ENFDC => Enable FDC interface = 0 FDC is enabled after hardware reset. = 1 FDC is disabled after hardware reset. This bit is set or reset by a power-on strapping pin (Pin 52, DTRA#). **Note 1**
0	Reserved.	

Note1:

Disable FDC interface

Pin 5 → CTSF#

Pin 6 → GP64

Pin 7 → DSRF#

Pin 8 → RTSF#

Enable FDC interface

Pin 5 → DRVDEN0

Pin 6 → INDEX#

Pin 7 → MOA#

Pin 8 → DSA#

Disable FDC interface	Enable FDC interface
Pin 9 → DTRF#	Pin 9 → DIR#
Pin 10 → SINF	Pin 10 → STEP#
Pin 11→ SOUTF	Pin 11→ WD#
Pin 13 → DCDF#	Pin 13 → WE#
Pin 14 → GP63	Pin 14 → TRAK0#
Pin 15 → GP62	Pin 15 → WP#
Pin 16 → GP61	Pin 16 → RDATA#
Pin 17→ RIF#	Pin 17→ HEAD#
Pin 18→ GP60	Pin 18→ DSKCHG#

CR 25h. (Interface Tri-state Enable; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~6	Reserved.	
5	R / W	UARTBTRI => =0 Tri-state disabled =1 Tri-state enabled
4	R / W	UARTATRI => =0 Tri-state disabled =1 Tri-state enabled
3	R / W	PRTTRI => =0 Tri-state disabled =1 Tri-state enabled
2~1	Reserved.	
0	R / W	FDCTRI. => =0 Tri-state disabled =1 Tri-state enabled

CR 26h. (Global Option; Default 0s000000b) s: value by strapping

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	HEFRAS => = 0 Write 87h to location 2E twice. = 1 Write 87h to location 4E twice. The corresponding power-on strapping pin is RTSA# (Pin 51).
5	R / W	LOCKREG => = 0 Enable R/W configuration registers. = 1 Disable R/W configuration registers.

CR 26h. (Global Option; Default 0s000000b), continued

BIT	READ / WRITE	DESCRIPTION
4	Reserved.	
3	R / W	DSFDLGRQ => = 0 Enable FDC legacy mode for IRQ and DRQ selection. Then DO register (base address + 2) bit 3 is effective when selecting IRQ. = 1 Disable FDC legacy mode for IRQ and DRQ selection. Then DO register (base address + 2) bit 3 is not effective when selecting IRQ.
2	R / W	DSPRLGRQ => = 0 Enable PRT legacy mode for IRQ and DRQ selection. Then DCR register (base address + 2) bit 4 is effective when selecting IRQ. = 1 Disable PRT legacy mode for IRQ and DRQ selection. Then DCR register (base address + 2) bit 4 is not effective when selecting IRQ.
1	R / W	DSUALGRQ => = 0 Enable UART A legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ. = 1 Disable UART A legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.
0	R / W	DSUBLGRQ => = 0 Enable UART B legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ. = 1 Disable UART B legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.

CR 27h. (Reserved)

CR 28h. (Global Option; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R/W	DSUFLGRQ => = 0 Enable UART F legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ. = 1 Disable UART F legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.
6	R/W	DSUELGRQ => = 0 Enable UART E legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ. = 1 Disable UART E legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.

CR 28h. (Global Option; Default 00h), continued

BIT	READ / WRITE	DESCRIPTION
5	R/W	DSUDLGRQ => = 0 Enable UART D legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ. = 1 Disable UART D legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.
4	R/W	DSUCLGRQ => = 0 Enable UART C legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ. = 1 Disable UART C legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.
3	Reserved.	
2~0	R / W	PRTMODS2 ~ 0 => = 0xx Parallel Port Mode. = 1xx Reserved.

CR 29h. (OVT#/HM_SMI#, PLED & GPIO3, 4, 5, 6 Output Type Select; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R/W	Select output type of GPIO 6 =0 GPIO6 (pins 6, 14, 15, 16 & 18) are open-drain. (Default) =1 GPIO6 are push-pull.
6	R / W	Pin 95 function select = 0 OVT# = 1 SMI#
5	R/W	Select output type of GPIO 5 = 0 GPIO 5 (pins 125 ~ 4) are open-drain. (Default) = 1 GPIO 5 are push-pull.
4	R/W	Select output type of GPIO 4 = 0 GPIO 4 (pins 117 ~ 124) are open-drain. (Default) = 1 GPIO 4 are push-pull.
3	R/W	Select output type of GPIO 3 = 0 GPIO 3 (pins 109 ~ 116) are open-drain. (Default) = 1 GPIO 3 are push-pull.
2~1	R / W	Select Power LED mode. 00: Power LED pin is tri-stated. 01: Power LED pin is driven low. 10: Power LED pin outputs 1Hz pulse with 50% duty cycle. 11: Power LED pin outputs $^1/_4$Hz pulse with 50% duty cycle.
0	Reserved.	

CR 2Ah. (I^2C Pin Select; Default 00h) (VSB Power)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3	R/W	SDA_filter_EN: 0: Enable SDA input to a filter 1: Disable SDA input to a filter
2	R / W	SCL_filter_EN: 0: Enable SCL input to a filter 1: Disable SCL input to a filter
1	R / W	Pin 69, Pin 70 function select (I^2C interface) = 0 Pin 69, 70 → GP25, GP26 (Default) = 1 Pin 69, 70 → SDA, SCL
0	Reserved.	

CR 2Bh. (Reserved)

CR 2Ch. (GPIO1 Multi-function and GPIO1, 2 Output Type Select; Default 02h) (VSB Power)

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>Select output type of GPIO 2
= 0 GPIO 2 (pins 108, 107, 106, 96, 94, 70, 69, 58) are open-drain. (Default)
= 1 GPIO 2 are push-pull.</td></tr>
<tr><td>6</td><td>R / W</td><td>Select output type of GPIO 1
= 0 GPIO 1 (pins 78 ~ 85) are open-drain. (Default)
= 1 GPIO 1 are push-pull.</td></tr>
<tr><td>5~3</td><td colspan="2">Reserved.</td></tr>
<tr><td>2</td><td>R / W</td><td>EN_PWRDN. (VBAT)
= 0 Disable thermal shutdown function.
= 1 Enable thermal shutdown function.</td></tr>
<tr><td>1~0</td><td>R / W</td><td>Pins 78 ~ 85 function select
<table>
<tr><th>Bit-1</th><th>Bit-0</th><th>Pins 78 ~ 85 function</th></tr>
<tr><td>0</td><td>0</td><td>Pin 82 → Reserved (tri-state)
Pin 83 → Reserved (always low)
Others → GPIO1</td></tr>
<tr><td>0</td><td>1</td><td>Pin 82 → IRRX
Pin 83 → IRTX
Others → GPIO1</td></tr>
<tr><td>1</td><td>0</td><td>Pins 78 ~ 85 → GPIO1</td></tr>
<tr><td>1</td><td>1</td><td>Pins 78 ~ 85 → UART B</td></tr>
</table></td></tr>
</table>

CR 2Dh. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	0: Enable GP27 input de-bouncer. 1: Disable GP27 input de-bouncer.
5	R / W	0: Enable GP26 input de-bouncer. 1: Disable GP26 input de-bouncer.
4	R / W	0: Enable GP25 input de-bouncer. 1: Disable GP25 input de-bouncer.
3	Reserved.	
2	R / W	0: GP27 trigger type :edge 1: GP27 trigger type :level
1	R / W	0: GP26 trigger type :edge 1: GP26 trigger type :level
0	R / W	0: GP25 trigger type :edge 1: GP25 trigger type :level

CR 2Eh. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Test Mode Bits: Reserved.

CR 2Fh. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Test Mode Bits: Reserved.

17.2 Logical Device 0 (FDC)

CR 30h. (Default 01h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: Logical device is inactive. 1: Logical device is active.

CR 60h, 61h. (Default 03h,F0h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select FDC I/O base address <100h : FF8h> on 8-byte boundary.

CR 70h. (Default 06h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for FDC.

CR 74h. (Default 02h)

BIT	READ / WRITE	DESCRIPTION
7~3	Reserved.	
2~0	R / W	These bits select DRQ resource for FDC. 000: DMA0. 001: DMA1. 010: DMA2. 011: DMA3. 1xx: No DMA active.

CR F0h. (Default 8Eh)

BIT	READ / WRITE	DESCRIPTION
7	R / W	FIPURDWN This bit controls the internal pulled-up resistors of the FDC input pins RDATA#, INDEX#, TRAK0#, DSKCHG# and WP#. 0: The internal pulled-up resistors of FDC are turned on. 1: The internal pulled-up resistors of FDC are turned off. (Default)
6	R / W	This bit determines the polarity of all FDD interface signals. 0: FDD interface signals are active low. 1: FDD interface signals are active high.
5	R / W	When this bit is logic 0, it indicates a second drive is installed and is reflected in status register A. (PS2 mode only)
4	R / W	Swap Drive 0, 1 Mode => 0: No Swap. 1: Drive and Motor select 0 and 1 are swapped.
3~2	R / W	Interface Mode. 00: Model 30. 01: PS/2. 10: Reserved. 11: AT Mode
1	R / W	FDC DMA Mode. 0: Burst Mode is enabled 1: Non-Burst Mode.
0	R / W	Floppy Mode. 0: Normal Floppy Mode. 1: Enhanced 3-mode FDD.

CR F1h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~6	R / W	Boot Floppy. 00: FDD A. 01: FDD B. 10: FDD C. 11: FDD D.
5~4	R / W	Media ID1, Media ID0. These bits will be reflected on FDC's Tape Drive Register bit 7, 6.
3~2	R / W	Density Select. 00: Normal. 01 Normal. 10: 1 (Forced to logic 1). 11: 0 (Forced to logic 0).
1	R / W	DISFDDWR => 0: Enable FDD write. 1: Disable FDD write (forces pins WE, WD stay high).
0	R / W	SWWP => 0: Normal, use WP to determine whether the FDD is write protected or not. 1: FDD is always write-protected.

CR F2h. (Default FFh)

BIT	READ / WRITE	DESCRIPTION
7~6	R / W	FDD D Drive Type.
5~4	R / W	FDD C Drive Type.
3~2	R / W	FDD B Drive Type.
1~0	R / W	FDD A Drive Type.

CR F4h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	0: Enable FDC Pre-compensation. 1: Disable FDC Pre-compensation.
5	Reserved.	
4~3	R / W	Data Rate Table selection (Refer to TABLE A). 00: Select regular drives and 2.88 format. 01: 3-mode drive. 10: 2 Meg Tape. 11: Reserved.
2	Reserved.	
1~0	R / W	Drive Type selection (Refer to TABLE B).

CR F5h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Same as FDD0 of CR F5h.

TABLE A

DRIVE RATE TABLE SELECT		DATA RATE		SELECTED DATA RATE		SELDEN
DRTS1	DRTS0	DRATE1	DRATE0	MFM	FM	
0	0	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	300K	150K	0
		1	0	250K	125K	0
0	1	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	500K	250K	0
		1	0	250K	125K	0
1	0	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	2Meg	---	0
		1	0	250K	125K	0

TABLE B

DTYPE0	DTYPE1	DRVDEN0 (pin 2)	DRVDEN1 (pin 3)	DRIVE TYPE
0	0	SELDEN	DRATE0	4/2/1 MB 3.5”“ 2/1 MB 5.25” 2/1.6/1 MB 3.5” (3-MODE)
0	1	DRATE1	DRATE0	
1	0	$\overline{\text{SELDEN}}$	DRATE0	
1	1	DRATE0	DRATE1	

17.3 Logical Device 1 (Parallel Port)

CR 30h. (Default 01h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: Logical device is inactive. 1: Logical device is active.

CR 60h, 61h. (Default 03h, 78h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select PRT I/O base address. <100h : FFCh> on 4-byte boundary (EPP not supported) or <100h : FF8h> on 8-byte boundary (all modes supported, EPP is only available when the base address is on 8-byte boundary).

CR 70h. (Default 07h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for PRT.

CR 74h. (Default 04h)

BIT	READ / WRITE	DESCRIPTION
7~3	Reserved.	
2~0	R / W	These bits select DRQ resource for PRT. 000: DMA0. 001: DMA1. 010: DMA2. 011: DMA3. 1xx: No DMA active.

CR F0h. (Default 3Fh)

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6~3	R / W	ECP FIFO Threshold.
2~0	R / W	Parallel Port Mode selection (CR28 bit2 PRTMODS2 = 0). 000: Standard and Bi-direction (SPP) mode. 001: EPP – 1.9 and SPP mode. 010: ECP mode. 011: ECP and EPP – 1.9 mode. 100: Printer Mode. 101: EPP – 1.7 and SPP mode. 110: Reserved. 111: ECP and EPP – 1.7 mode.

17.4 Logical Device 2 (UART A)

CR 30h. (Default 01h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: Logical device is inactive. 1: Logical device is active.

CR 60h, 61h. (Default 03h, F8h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select Serial Port 1 I/O base address <100h: FF8h> on 8-byte boundary.

CR 70h. (Default 04h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for Serial Port A.

CR F0h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Delay RXCLK for 5 ns for LG issue. 1: No delay of 5 ns for RXCLK.
6	R / W	0: IRQ is the level mode. 1: IRQ is the pulse mode.
5	R / W	0: Using the original RX FIFO Error Indication signal (USR bit 7). 1: Using new RX FIFO Error Indication signal to solve some issues.
4~2	Reserved.	
1~0	R / W	00: UART A clock source is 1.8462 MHz (24 MHz / 13). 01: UART A clock source is 2 MHz (24 MHz / 12). 00: UART A clock source is 24 MHz (24 MHz / 1). 00: UART A clock source is 14.769 MHz (24 MHz / 1.625).

17.5 Logical Device 3 (UART B)

CR 30h. (Default 01h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: Logical device is inactive. 1: Logical device is active.

CR 60h, 61h. (Default 02h, F8h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select Serial Port 2 I/O base address <100h: FF8h> on 8-byte boundary.

CR 70h. (Default 03h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for Serial Port B.

CR F0h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Delay RXCLK for 5 ns for LG issue. 1: No delay of 5 ns for RXCLK.
6	R / W	0: IRQ is the level mode. 1: IRQ is the pulse mode.
5	R / W	0: Using the original RX FIFO Error Indication signal (USR bit 7). 1: Using new RX FIFO Error Indication signal to solve some issues.
4	Reserved.	
3	R / W	0: No reception delay when SIR is changed from TX mode to RX mode. 1: Reception delay 4 characters' time (40 bit-time) when SIR is changed from TX mode to RX mode.
2	R / W	0: No transmission delay when SIR is changed from RX mode to TX mode. 1: Transmission delay 4 characters' time (40 bit-time) when SIR is changed from RX mode to TX mode.
1~0	R / W	00: UART B clock source is 1.8462 MHz (24 MHz / 13). 01: UART B clock source is 2 MHz (24 MHz / 12). 00: UART B clock source is 24 MHz (24 MHz / 1). 00: UART B clock source is 14.769 MHz (24 MHz / 1.625).

CR F1h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	Reserved.
6	R / W	IRLOCSEL => IR I/O pins' location selection. 0: Through SINB / SOUTB. 1: Through IRRX / IRTX.
5~3	R / W	IRMODE => IR function mode selection. See the table below.
2	R / W	IR half / full duplex function selection. 0: IR function is Full Duplex. 1: IR function is Half Duplex.
1	R / W	0: SOUTB pin of UART B function or IRTX pin of IR function is in normal condition. 1: Inverse SOUTB pin of UART B function or IRTX pin of IR function.
0	R / W	0: SINB pin of UART B function or IRRX pin of IR function is in normal condition. 1: Inverse SINB pin of UART B function or IRRX pin of IR function.

IR MODE	IR FUNCTION	IRTX	IRRX
00X	Disable	Tri-state	High
010*	IrDA	Active pulse 1.6 μS	Demodulation into SINB/IRRX
011*	IrDA	Active pulse 3/16 bit time	Demodulation into SINB/IRRX
100	ASK-IR	Inverting IRTX/SOUTB pin	Routed to SINB/IRRX
101	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	Routed to SINB/IRRX
110	ASK-IR	Inverting IRTX/SOUTB	Demodulation into SINB/IRRX
111*	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	Demodulation into SINB/IRRX

Note: The notation is normal mode in the IR function.

17.6 Logical Device 5 (Keyboard Controller)

CR 30h. (Default 01h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: Logical device is inactive. 1: Logical device is active.

CR 60h, 61h. (Default 00h,60h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select the first KBC I/O base address <100h: FFFh> on 1-byte boundary.

CR 62h, 63h. (Default 00h,64h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select the second KBC I/O base address <100h: FFFh> on 1-byte boundary.

CR 70h. (Default 01h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for KINT. (Keyboard interrupt)

CR 72h. (Default 0Ch)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for MINT. (PS/2 Mouse interrupt)

CR F0h. (Default 83h)

BIT	READ / WRITE	DESCRIPTION
7~6	R / W	KBC clock rate selection 00: 6MHz 01: 8MHz 10: 12MHz 11: 16MHz
5~3	Reserved.	

CR F0h. (Default 83h), continued

BIT	READ / WRITE	DESCRIPTION
2	R / W	0: Port 92 disabled. 1: Port 92 enabled.
1	R / W	0: Gate A20 software control. 1: Gate A20 hardware speed up.
0	R / W	0: KBRST software control. 1: KBRST hardware speeds up.

17.7 Logical Device 6 (UART C)

CR 30h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: Logical device is inactive. 1: Logical device is active.

CR 60h, 61h. (Default 03h, E0h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select Serial Port 1 I/O base address <100h : FF8h> on 8-byte boundary.

CR 70h. (Default 04h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for Serial Port C.

CR F0h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Delay RXCLK for 5 ns for LG issue. 1: No delay of 5 ns for RXCLK.
6	R / W	0: IRQ is the level mode. 1: IRQ is the pulse mode.
5	R / W	0: Using the original RX FIFO Error Indication signal (USR bit 7). 1: Using new RX FIFO Error Indication signal to solve some issues.
4~2	Reserved.	
1~0	R / W	00: UART C clock source is 1.8462 MHz (24 MHz / 13). 01: UART C clock source is 2 MHz (24 MHz / 12). 00: UART C clock source is 24 MHz (24 MHz / 1). 00: UART C clock source is 14.769 MHz (24 MHz / 1.625).

17.8 Logical Device 7 (GPIO3, GPIO4)

CR 30h. (Default 03h)

BIT	READ / WRITE	DESCRIPTION
7~2	Reserved.	
1	R / W	0: GPIO4 is inactive. 1: GPIO4 is active.
0	R / W	0: GPIO3 is inactive. 1: GPIO3 is active.

CR E0h. (GPIO3 I/O Register; Default FFh)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO3 I/O register 0: The respective GPIO3 PIN is programmed as an Output port 1: The respective GPIO3 PIN is programmed as an Input port.

CR E1h. (GPIO3 Data Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO3 Data register For Output ports, the respective bits can be read and written by the pins.
	Read Only	For Input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR E2h. (GPIO3 Inversion Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO3 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR E3h. (Status Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only Read-Clear	GPIO3 Event Status Bit 7-0 corresponds to GP37-GP30, respectively. 0 : No active edge(rising/falling) has been detected 1 : An active edge(rising/falling) has been detected Reading the status bit clears it to 0.

CR E4h. (GPIO4 I/O Register; Default FFh)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO4 I/O register 0: The respective GPIO4 PIN is programmed as an Output port 1: The respective GPIO4 PIN is programmed as an Input port.

CR E5h. (GPIO4 Data Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO4 Data register For Output ports, the respective bits can be read and written by the pins.
	Read Only	For Input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR E6h. (GPIO4 Inversion Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO4 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR E7h. (Status Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only Read-Clear	GPIO4 Event Status Bits 7-0 correspond to GP47-GP40, respectively. 0 : No active edge(rising/falling) has been detected 1 : An active edge(rising/falling) has been detected Reading the status bit clears it to 0.

17.9 Logical Device 8 (WDTO#, PLED, GPIO5, 6 & GPIO Base Address)

CR 30h. (Default 02h)

BIT	READ / WRITE	DESCRIPTION
7~3	Reserved.	
2	R / W	0: GPIO6 is inactive. 1: GPIO6 is active.
1	R / W	0: GPIO5 is inactive. 1: GPIO5 is active.
0	R / W	0: WDTO# and PLED are inactive. 1: WDTO# and PLED are active.

CR 60h 61h. (Default 00h, 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select GPIO base address <100h: FF8h> on 4-byte boundary.

CR E0h. (GPIO5 I/O Register; Default FFh)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO5 I/O register 0: The respective GPIO5 PIN is programmed as an Output port 1: The respective GPIO5 PIN is programmed as an Input port.

CR E1h. (GPIO5 Data Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO5 Data register For Output ports, the respective bits can be read and written by the pins.
	Read Only	For Input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR E2h. (GPIO5 Inversion Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO5 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR E3h. (Status Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only Read-Clear	GPIO5 Event Status Bits 7-0 correspond to GP57-GP50, respectively. 0 : No active edge(rising/falling) has been detected 1 : An active edge(rising/falling) has been detected Reading the status bit clears it to 0.

CR E4h. (GPIO6 I/O Register; Default FFh)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO6 I/O register 0: The respective GPIO6 PIN is programmed as an Output port 1: The respective GPIO6 PIN is programmed as an Input port.

CR E5h. (GPIO6 Data Register; Default 1Fh)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO6 Data register For Output ports, the respective bits can be read and written by the pins.
	Read Only	For Input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR E6h. (GPIO6 Inversion Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO6 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR E7h. (Status Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only Read-Clear	GPIO6 Event Status Bits 7-0 correspond to GP67-GP60, respectively. 0 : No active edge(rising/falling) has been detected 1 : An active edge(rising/falling) has been detected Reading the status bit clears it to 0.

CR F5h. (WDTO# and KBC P20 Control Mode Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~5	Reserved.	
4	R / W	1000 times faster in WDTO# count mode. 0: Disable. 1: Enable. (If bit-3 is Second Mode, the count mode is 1/1000 Sec.) (If bit-3 is Minute Mode, the count mode is 1/1000 Min.)
3	R / W	Select WDTO# count mode. 0: Second Mode. 1: Minute Mode.
2	R / W	Enable the rising edge of KBC reset (P20) to issue time-out event. 0: Disable. 1: Enable.
1	R / W	Disable / Enable the WDTO# output low pulse to the KBRST# pin (PIN60) 0: Disable. 1: Enable.
0	Reserved.	

CR F6h. (WDTO# Counter Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Watch Dog Timer Time-out value. Writing a non-zero value to this register causes the counter to load the value to Watch Dog Counter and start counting down. If bits 7 and 6 of CR F7h are set, any Mouse Interrupt or Keyboard Interrupt event will also cause the reload of previously-loaded non-zero value to Watch Dog Counter and start counting down. Reading this register returns current value in Watch Dog Counter instead of Watch Dog Timer Time-out value. 00h: Time-out Disable 01h: Time-out occurs after 1 second/minute 02h: Time-out occurs after 2 second/minutes 03h: Time-out occurs after 3 second/minutes ……..... FFh: Time-out occurs after 255 second/minutes

CR F7h. (WDTO# Control & Status Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	Mouse interrupt reset watch-dog timer enable 0: Watchdog timer is not affected by mouse interrupt. 1: Watchdog timer is reset by mouse interrupt.
6	R / W	Keyboard interrupt reset watch-dog timer enable 0: Watchdog timer is not affected by keyboard interrupt. 1: Watchdog timer is reset by keyboard interrupt.
5	Write “1” Only	Trigger WDTO# event. This bit is self-clearing.
4	R / W Write “0” Clear	WDTO# status bit 0: Watchdog timer is running. 1: Watchdog timer issues time-out event.
3~0	R / W	These bits select IRQ resource for WDTO#. (02h for SMI# event.)

17.10 Logical Device 9 (GPIO1, GPIO2 and SUSLED)

CR 30h. (Default 03h)

BIT	READ / WRITE	DESCRIPTION
7~2	Reserved.	
1	R / W	0: GPIO2 is inactive. 1: GPIO2 is active.
0	R / W	0: GPIO1 is inactive. 1: GPIO1 is active.

CR E0h. (GPIO1 I/O Register; Default FFh)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO1 I/O register 0: The respective GPIO1 PIN is programmed as an Output port 1: The respective GPIO1 PIN is programmed as an Input port.

CR E1h. (GPIO1 Data Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO1 Data register For Output ports, the respective bits can be read and written by the pins.
	Read Only	For Input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR E2h. (GPIO1 Inversion Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO1 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR E3h. (Status Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only Read-Clear	GPIO1 Event Status Bits 7-0 correspond to GP17-GP10, respectively. 0 : No active edge(rising/falling) has been detected 1 : An active edge(rising/falling) has been detected Reading the status bit clears it to 0.

CR E4h. (GPIO2 I/O Register; Default FFh)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO2 I/O register 0: The respective GPIO2 PIN is programmed as an Output port 1: The respective GPIO2 PIN is programmed as an Input port.

CR E5h. (GPIO2 Data Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO2 Data register For Output ports, the respective bits can be read and written by the pins.
	Read Only	For Input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR E6h. (GPIO2 Inversion Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO2 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR E7h. (Status Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only Read-Clear	GPIO2 Event Status Bit 4-0 corresponds to GP24-GP20, respectively. 0 : No active edge(rising/falling) has been detected 1 : An active edge(rising/falling) has been detected Reading the status bit clears it to 0.

CR F3h. (Suspend LED Mode Register; Default 00h) (VBAT power)

BIT	READ / WRITE	DESCRIPTION
7~6	R / W	Select Suspend LED mode. 00: Suspend LED pin is driven low. 01: Suspend LED pin is tri-stated. 10: Suspend LED pin outputs 1Hz pulse with 50% duty cycle. 11: Suspend LED pin outputs $^1/_4$Hz pulse with 50% duty cycle.
5~0	Reserved.	

17.11 Logical Device A (ACPI)

(CR30, CR70 are VCC powered; CRE0~F7 and CRFE are VRTC powered)

CR 30h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: Logical device is inactive. 1: Logical device is active.

CR 70h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for PME#.

CR E0h. (Default 01h) (VBAT Power)

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>DIS_PSIN => Disable panel switch input to turn system power supply on.
0: PSIN# is wire-AND and connected to PSOUT#.
1: PSIN# is blocked and cannot affect PSOUT#.</td></tr>
<tr><td>6</td><td>R / W</td><td>Enable KBC wake-up
0: Disable keyboard wake-up function via PSOUT#.
1: Enable keyboard wake-up function via PSOUT#.</td></tr>
<tr><td>5</td><td>R / W</td><td>Enable Mouse wake-up
0: Disable mouse wake-up function via PSOUT#.
1: Enable mouse wake-up function via PSOUT#.</td></tr>
<tr><td>4</td><td>R / W</td><td>MSRKEY =>
3 keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please refer to the following table for the details.
<table>
<tr><th>ENMDAT_UP</th><th>MSRKEY</th><th>MSXKEY</th><th>Wake-up event</th></tr>
<tr><td>1</td><td>x</td><td>1</td><td>Any button clicked or movement.</td></tr>
<tr><td>1</td><td>x</td><td>0</td><td>One click of either left or right MS button.</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>One click of the MS left button.</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>One click of the MS right button.</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Two clicks of the MS left button.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Two clicks of the MS right button.</td></tr>
</table>
</td></tr>
</table>

CR E0h. (Default 01h) (VBAT Power), continued

BIT	READ / WRITE	DESCRIPTION
3	Reserved.	
2	R / W	Keyboard / Mouse swap enable 0: Normal mode. 1: Keyboard / Mouse ports are swapped.
1	R / W	MSXKEY => 3 keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please refer to the table in CRE0[4] for the details.
0	R / W	KBXKEY => 0: Only the pre-determined key combination in sequence can wake up the system. 1: Any character received from the keyboard can wake up the system.

CR E1h. (KBC Wake-Up Index Register; Default 00h) (VSB Power)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Keyboard wake-up index register. It is the index register of CRE2, which is the access window of keyboard pre-determined key combination characters. The first set of wake up key combination is in the range of 0x00 - 0x0E, the second set 0x30 – 0x3E, and the third set 0x40 – 0x4E. Incoming key combination can be read through 0x10 – 0x1E.

CR E2h. (KBC Wake-Up Data Register; Default FFh) (VSB Power)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Keyboard wake-up data register. It is the data register of the keyboard pre-determined key combination characters, which is indexed by CRE1.

CR E3h. (Event Status Register; Default 08h)

BIT	READ / WRITE	DESCRIPTION
7~6	Reserved.	
5	Read Only Read-Clear	This event status is caused by VSB power off/on.

CR E3h. (Event Status Register; Default 08h), continued

BIT	READ / WRITE	DESCRIPTION
4	Read Only Read-Clear	If E4[7] is 1 => This bit is 0: When power loss occurs and VSB power is on, it indicates that the system power is turned on. This bit is 1: When power loss occurs and VSB power is on, it indicates that the system power is turned off. If E4[7] is 0 => This bit is always 0.
3	Read Only Read-Clear	Thermal shutdown status. 0: No thermal shutdown event is issued. 1: The thermal shutdown event is issued.
2	Read Only Read-Clear	PSIN_STS 0: No PSIN event is issued. 1: The PSIN event is issued.
1	Read Only Read-Clear	MSWAKEUP_STS => The bit is latched by the mouse wake-up event. 0: No mouse wake-up event is issued. 1: The mouse wake-up event is issued.
0	Read Only Read-Clear	KBWAKEUP_STS => The bit is latched by the keyboard wake-up event. 0: No keyboard wake-up event is issued. 1: The keyboard wake-up event is issued.

CR E4h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	Disable / Enable power loss control function (LDA: CRE4[6:5]) for Intel chipset. (**VBAT**) 0: Disable. 1: Enable.
6~5	R / W	Power-loss control bits => (**VBAT**) 00: System always turns off when it returns from the power-loss state. 01: System always turns on when it returns from the power-loss state. 10: System turns off / on when it returns from the power-loss state depending on the state before the power loss. 11: User defines the state before power loss.(i.e. the last state set of CRE6[4])
4	Reserved.	
3	R / W	Keyboard wake-up options. **(LRESET#)** 0: Password or sequence hot keys programmed in the registers. 1: Any key.
2	R / W	Enable the hunting mode for all wake-up events set in CRE0. This bit is cleared when any wake-up events is captured. **(LRESET#)** 0: Disable. 1: Enable.
1~0	Reserved.	

CR E5h. (GPIOs Reset Source Register; Default 00))

BIT	READ / WRITE	DESCRIPTION
7	R / W	GPIO 6 reset source control bit. =0 Enable GPIO 6 reset source by LRESET# =1 Disable GPIO 6 reset source by LRESET#
6	R / W	GPIO 5 reset source control bit. =0 Enable GPIO 5 reset source by LRESET# =1 Disable GPIO 5 reset source by LRESET#
5	R / W	GPIO 4 reset source control bit. =0 Enable GPIO 4 reset source by LRESET# =1 Disable GPIO 4 reset source by LRESET#
4	R / W	GPIO 3 reset source control bit. =0 Enable GPIO 3 reset source by LRESET# =1 Disable GPIO 3 reset source by LRESET#
3	R / W	GPIO 2 reset source control bit. =0 Enable GPIO 2 reset source by LRESET# =1 Disable GPIO 2 reset source by LRESET#
2	R / W	GP25~27 reset source control bit. =0 LRESET# =1 RSMRST#
1-0	Reserved.	

CR E6h. (Default 1Ch)

BIT	READ / WRITE	DESCRIPTION
7	R / W	ENMDAT => **(VSB)** 3 keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please refer to the table in CRE0[4] for the details.
6	Reserved.	
5	R / W	CASEOPEN Clear Control. **(VSB)** Write 1 to this bit will clear CASEOPEN status. This bit will clear the status itself. The function is the same as Index 46h bit 7 of H/W Monitor part.
4	R / W	Power-loss Last State Flag. **(VBAT)** 0: ON 1: OFF.

CR E6h. (Default 1Ch), continued

BIT	READ / WRITE	DESCRIPTION
3	R / W	PWROK_DEL (first stage) **(VSB)** Set the delay time when rising from PWROK_LP to PWROK_ST. 0: 300 ~ 500 ms. 1: 200 ~ 300 ms.
2~1	R / W	PWROK_DEL **(VSB)** Set the delay time when rising from PWROK_ST to PWROK. 00: No delay time. 01: Delay 32 ms 10: 96 ms 11: Delay 250 ms
0	R / W-Clear	PWROK_TRIG => Write 1 to re-trigger the PWROK signal from low to high.

CR E7h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	ENKD3 => **(VSB)** Enable the third set of keyboard wake-up key combination. Its values are accessed through keyboard wake-up index register (CRE1) and keyboard wake-up data register (CRE2) at the index from 40h to 4eh. 0: Disable the third set of the key combinations. 1: Enable the third set of the key combinations.
6	R / W	ENKD2 => **(VSB)** Enable the second set of keyboard wake-up key combination. Its values are accessed through keyboard wake-up index register (CRE1) and keyboard wake-up data register (CRE2) at the index from 30h to 3eh. 0: Disable the second set of the key combinations. 1: Enable the second set of the key combinations.
5	R / W	ENWIN98KEY => **(VSB)** Enable Win98 keyboard dedicated key to wake-up the system via PSOUT# when keyboard wake-up function is enabled. 0: Disable Win98 keyboard wake-up. 1: Enable Win98 keyboard wake-up.
4	R / W	EN_ONPSOUT **(VBAT)** Disable/Enable to issue a 0.5s long PSOUT# pulse when the system returns from the power-loss state and is supposed to be on as described in CRE4[6:5], logic device A. (for SiS & VIA chipsets) 0: Disable. 1: Enable.
3	R / W	Select WDTO# reset source **(VSB)** 0: Watchdog timer is reset by LRESET#. 1: Watchdog timer is reset by PWROK.
2~1	Reserved.	
0	R / W	Hardware Monitor RESET source select **(VBAT)** 0: PWROK. 1: LRESET#.

CR E8h. (Reserved)

CR E9h. (Reserved.)

CR F2h. (Default 3Eh) (VSB Power)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	EN_PME => 0: Disable PME. 1: Enable PME.

CR F3h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R /W-Clear	PME status of the URC IRQ event. Write 1 to clear this status.
5	R / W-Clear	PME status of the Mouse IRQ event. Write 1 to clear this status.
4	R / W-Clear	PME status of the KBC IRQ event. Write 1 to clear this status.
3	R / W-Clear	PME status of the PRT IRQ event. Write 1 to clear this status.
2	R / W-Clear	PME status of the FDC IRQ event. Write 1 to clear this status.
1	R / W-Clear	PME status of the URA IRQ event. Write 1 to clear this status.
0	R / W-Clear	PME status of the URB IRQ event. Write 1 to clear this status.

CR F4h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~6	Reserved.	
5	R / W-Clear	PME status of the URF IRQ event. Write 1 to clear this status.
4	R / W-Clear	PME status of the URE IRQ event. Write 1 to clear this status.
3	R / W-Clear	PME status of the HM IRQ event. Write 1 to clear this status.

CR F4h. (Default 00h), continued

BIT	READ / WRITE	DESCRIPTION
2	R / W-Clear	PME status of the WDTO# event. Write 1 to clear this status.
1	R / W-Clear	PME status of the URD IRQ event. Write 1 to clear this status.
0	R / W-Clear	PME status of the RIB event. Write 1 to clear this status.

CR F6h. (Default 00h) (VSB Power)

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	0: Disable PME interrupt of the URC IRQ event. 1: Enable PME interrupt of the URC IRQ event.
5	R / W	0: Disable PME interrupt of the Mouse IRQ event. 1: Enable PME interrupt of the Mouse IRQ event.
4	R / W	0: Disable PME interrupt of the KBC IRQ event. 1: Enable PME interrupt of the KBC IRQ event.
3	R / W	0: Disable PME interrupt of the PRT IRQ event. 1: Enable PME interrupt of the PRT IRQ event.
2	R / W	0: Disable PME interrupt of the FDC IRQ event. 1: Enable PME interrupt of the FDC IRQ event.
1	R / W	0: Disable PME interrupt of the URA IRQ event. 1: Enable PME interrupt of the URA IRQ event.
0	R / W	0: Disable PME interrupt of the URB IRQ event. 1: Enable PME interrupt of the URB IRQ event.

CR F7h. (Default 00h) (VSB Power)

BIT	READ / WRITE	DESCRIPTION
7~6	Reserved.	
5	R / W	0: Disable PME interrupt of the URF IRQ event. 1: Enable PME interrupt of the URF IRQ event.
4	R / W	0: Disable PME interrupt of the URE IRQ event. 1: Enable PME interrupt of the URE IRQ event.
3	R / W	0: Disable PME interrupt of the HM IRQ event. 1: Enable PME interrupt of the HM IRQ event.

CR F7h. (Default 00h) (VSB Power), continued

BIT	READ / WRITE	DESCRIPTION
2	R / W	0: Disable PME interrupt of the WDTO# event. 1: Enable PME interrupt of the WDTO# event.
1	R / W	0: Disable PME interrupt of the URD IRQ event. 1: Enable PME interrupt of the URD IRQ event.
0	R / W	0: Disable PME interrupt of the RIB event. 1: Enable PME interrupt of the RIB event.

CR FEh. (GPIO2 Event Route Selection Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	Reserved.
6	R / W	0: Disable GP27 event route to PSOUT#. 1: Enable GP27 event route to PSOUT#.
5	R / W	0: Disable GP26 event route to PSOUT#. 1: Enable GP26 event route to PSOUT#.
4	R / W	0: Disable GP25 event route to PSOUT#. 1: Enable GP25 event route to PSOUT#.
3	Reserved.	
2	R / W	0: Disable GP27 event route to PME#. 1: Enable GP27 event route to PME#.
1	R / W	0: Disable GP26 event route to PME#. 1: Enable GP26 event route to PME#.
0	R / W	0: Disable GP25 event route to PME#. 1: Enable GP25 event route to PME#.

17.12 Logical Device B (Hardware Monitor)

CR 30h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: Logical device is inactive. 1: Logical device is active.

CR 60h, 61h. (Default 00h, 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select HM base address <100h : FFEh> on 2-byte boundary.

CR 70h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for HM.

CR F0h. (Reserved.)

CR F1h. (Reserved.)

CR F2h. (Multi-function Select & FAN Strapping Status Register; Default 00h) (VCC Power)

BIT	READ / WRITE	DESCRIPTION
7~2	Reserved.	
1	Read Only	GPI_MUL strapping status. This bit is strapped by pin 122 (SOUTD / GP42). 0: PIN 107,108 → BEEP, PLED 1: PIN 107,108 → GP20, GP21
0	Read Only	FAN_SET strapping status. This bit is strapped by pin 119 (RTSD# / GP45). 0: The initial speed is 100%. 1: The initial speed is 50%.

17.13 Logical Device C (PECI, SST)

CR E0h. (Agent Configuration Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	**Agt4EN** (Agent 4 Enable Bit) 0: Agent 4 is disabled. 1: Agent 4 is enabled.
6	R / W	**Agt3EN** (Agent 3 Enable Bit) 0: Agent 3 is disabled. 1: Agent 3 is enabled.
5	R / W	**Agt2EN** (Agent 2 Enable Bit) 0: Agent 2 is disabled. 1: Agent 2 is enabled.
4	R / W	**Agt1EN** (Agent 1 Enable Bit) 0: Agent 1 is disabled. 1: Agent 1 is enabled.
3	R / W	**RTD4** (Agent 4 Return Domain 1 Enable Bit, Functions only when CR E5h bit 7 is set to 1) 0: Agent 4 always returns the relative temperature from domain 0. 1: Agent 4 always returns the relative temperature from domain 1.
2	R / W	**RTD3** (Agent 3 Return Domain 1 Enable Bit, Functions only when CR E5h bit 6 is set to 1) 0: Agent 3 always returns the relative temperature from domain 0. 1: Agent 3 always returns the relative temperature from domain 1.
1	R / W	**RTD2** (Agent 2 Return Domain 1 Enable Bit, Functions only when CR E5h bit 5 is set to 1) 0: Agent 2 always returns the relative temperature from domain 0. 1: Agent 2 always returns the relative temperature from domain 1.
0	R / W	**RTD1** (Agent 1 Return Domain 1 Enable Bit, Functions only when CR E5h bit 4 is set to 1) 0: Agent 1 always returns the relative temperature from domain 0. 1: Agent 1 always returns the relative temperature from domain 1.

(When CR E8 [3] is set to 1, this register is used to read the relative temperature of Agent 1 (Low Byte)).

Note. Agent 1 ~ Agent 4 represent the addresses of PECI devices from 0x30h to 0x33h respectively.

CR E1h. (Agent 1 TControl Register; Default 48h)

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6~0	R / W	Agent 1 TBase must always be a positive value; a negative value will introduce abnormal temperature response. (Note1)

(When CR E8 [3] is set to 1, this register is used to read the relative temperature of Agent 1 (High Byte))

CR E2h. (Agent 2 TControl Register; Default 48h)

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6~0	R / W	Agent 2 TBase must always be a positive value; a negative value will introduce abnormal temperature response. (Note1)

(When CR E8 [3] is set to 1, this register is used to read the relative temperature of Agent 2 (Low Byte))

CR E3h. (Agent 3 TControl Register; Default 48h)

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6~0	R / W	Agent 3 TBase must always be a positive value; a negative value will introduce abnormal temperature response. (Note1)

(When CR E8 [3] is set to 1, this register is used to read the relative temperature of Agent 2 (High Byte))

CR E4h. (Agent 4 TControl Register; Default 48h)

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6~0	R / W	Agent 4 TBase must always be a positive value; a negative value will introduce abnormal temperature response. (Note1)

(When CR E8 [3] is set to 1, this register is used to read the relative temperature of Agent 3 (Low Byte))

Note1: TBase is a temperature reference based on the experiment of the processor actual temperature. For more details, please refer to section 7.5.

CR E5h. (PECI Domain Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	**Agt4D1** (Agent 4 Domain 1 Enable Bit) 0: Agent 4 does not have domain 1. 1: Agent 4 has domain 1.
6	R / W	**Agt3D1** (Agent 3 Domain 1 Enable Bit) 0: Agent 3 does not have domain 1. 1: Agent 3 has domain 1.
5	R / W	**Agt2D1** (Agent 2 Domain 1 Enable Bit) 0: Agent 2 does not have domain 1. 1: Agent 2has domain 1.
4	R / W	**Agt1D1** (Agent 1 Domain 1 Enable Bit) 0: Agent 1 does not have domain 1. 1: Agent 1 has domain 1.
3~2	Reserved.	
1	R / W	**Return High Temperature** 0: The temperature of each Agent is returned from domain 0 or domain 1, which is controlled by CRE0 bit 0~3. 1: Return the highest temperature in domain 0 and domain 1 of each individual Agent.
0	Reserved.	

(When CR E8 [3] is set to 1, this register is used to read the relative temperature of Agent 3 (High Byte))

CR E6h. (Agent 4 Relative Temperature (Low Byte))

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only	**Agent 4 Relative Temperature** (Low Byte) Before reading this register, this must be set to 1 in CR E8[3]

CR E7h. (Agent 4 Relative Temperature (High Byte))

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only	**Agent 4 Relative Temperature** (High Byte) Before reading this register, this must be set to 1 in CR E8[3]

CR E8h. (PECI Warning Flag Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	**Agent 4 Alert Bit** (When CR E8[3] is 0) 0: Agent 4 has valid FCS. 1: Agent 4 has invalid FCS in the previous 3 transactions.
		Agent 4 Absent Bit (When CR E8[3] is 1) 0: Agent 4 is detected. 1: Agent 4 cannot be detected.
6	R / W	**Agent 3 Alert Bit** (When CR E8[3] is 0) 0: Agent 3 has valid FCS. 1: Agent 3 has invalid FCS in the previous 3 transactions.
		Agent 3 Absent Bit (When CR E8[3] is 1) 0: Agent 3 is detected. 1: Agent 3 cannot be detected.
5	R / W	**Agent 2 Alert Bit** (When CR E8[3] is 0) 0: Agent 2 has valid FCS. 1: Agent 2 has invalid FCS in the previous 3 transactions.
		Agent 2 Absent Bit (When CR E8[3] is 1) 0: Agent 2 is detected. 1: Agent 2 cannot be detected.
4	R / W	**Agent 1 Alert Bit** (When CR E8[3] is 0) 0: Agent 1 has valid FCS. 1: Agent 1 has invalid FCS in the previous 3 transactions.
		Agent 1 Absent Bit (When CR E8[3]) 0: Agent 1 is detected. 1: Agent 1 cannot be detected.
3	R / W	**Bank Select.** This bit is used in Bank index selection. The relative data delivered over PECI interface and PECI Agent Absent Bit can be read from the registers below by setting Bank selection. Agt1RelTemp: CR E0 (Low Byte), CR E1 (High Byte) Agt2RelTemp: CR E2 (Low Byte), CR E3 (High Byte) Agt3RelTemp: CR E4 (Low Byte), CR E5 (High Byte) Agt4RelTemp: CR E6 (Low Byte), CR E7 (High Byte) Agent 4 Absent Bit: CR E8 bit 7 Agent 3 Absent Bit: CR E8 bit 6 Agent 2 Absent Bit: CR E8 bit 5 Agent 1 Absent Bit: CR E8 bit 4
2	Reserved.	

CR E8h. (PECI Warning Flag Register; Default 00h), continued

BIT	READ / WRITE	DESCRIPTION
1~0	R / W	**PECI Speed Select.** 00: The PECI speed is 1.5 MHz 01: The PECI speed is 750 KHz 10: The PECI speed is 375 KHz 11: The PECI speed is 187 KHz

BANK SELECT	CR E8 BIT 3 = 0	CR E8 BIT 3 = 1
CR E0	Agent Configuration Register	Agt1RelTemp (Low Byte)
CR E1	Agent 1 TBase Register	Agt1RelTemp (High Byte)
CR E2	Agent 2 TBase Register	Agt2RelTemp (Low Byte)
CR E3	Agent 3 TBase Register	Agt2RelTemp (High Byte)
CR E4	Agent 4 TBase Register	Agt3RelTemp (Low Byte)
CR E5	PECI Domain Register	Agt3RelTemp (High Byte)
CR E6	Reserved	Agt4RelTemp (Low Byte)
CR E7	Reserved	Agt4RelTemp (High Byte)
CR E8 (bit 4 ~ 7)	Agent Alert Bit	Agent Absent Bit

CR F1h. (SST Address Register; Default 48h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	SST address

CR F2h. (SST Vendor ID Low Byte; Default 50h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	SST Vendor ID Low Byte. (Note 2)

CR F3h. (SST Vendor ID High Byte; Default 10h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	SST Vendor ID High Byte. (Note 2)

CR FEh. (SST Device ID Low Byte; Default 23h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	SST Device ID Low Byte. (Note 3)

CR FFh. (SST Device ID High Byte; Default 5Ah)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	SST Device ID High Byte. (Note 3)

Note 2: Vendor ID identifies the device from a specific vendor. The PCI SIG or TBA assigns the contents of this value.

Note 3: This value is assigned by vendor and must be exclusive to that vendor and to the device. It will be used in conjunction with the Vendor ID to associate the correct software driver with the sensor.

17.14 Logical Device D (UART D)

CR 30h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: Logical device is inactive. 1: Logical device is active.

CR 60h, 61h. (Default 02h, E0h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select Serial Port 1 I/O base address <100h : FF8h> on 8-byte boundary.

CR 70h. (Default 03h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for Serial Port D.

CR F0h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Delay RXCLK for 5 ns for LG issue. 1: No delay of 5 ns for RXCLK.
6	R / W	0: IRQ is the level mode. 1: IRQ is the pulse mode.
5	R / W	0: Using the original RX FIFO Error Indication signal (USR bit 7). 1: Using new RX FIFO Error Indication signal to solve some issues.
4~2	Reserved.	
1~0	R / W	00: UART D clock source is 1.8462 MHz (24 MHz / 13). 01: UART D clock source is 2 MHz (24 MHz / 12). 00: UART D clock source is 24 MHz (24 MHz / 1). 00: UART D clock source is 14.769 MHz (24 MHz / 1.625).

17.15 Logical Device E (UART E)

CR 30h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: Logical device is inactive. 1: Logical device is active.

CR 60h, 61h. (Default 03h, E8h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select Serial Port 1 I/O base address <100h : FF8h> on 8-byte boundary.

CR 70h. (Default 04h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for Serial Port E.

CR F0h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6	R / W	0: IRQ is the level mode. 1: IRQ is the pulse mode.
5	R / W	0: Using the original RX FIFO Error Indication signal (USR bit 7). 1: Using new RX FIFO Error Indication signal to solve some issues.
4~2	Reserved.	
1~0	R / W	00: UART E clock source is 1.8462 MHz (24 MHz / 13). 01: UART E clock source is 2 MHz (24 MHz / 12). 00: UART E clock source is 24 MHz (24 MHz / 1). 00: UART E clock source is 14.769 MHz (24 MHz / 1.625).

17.16 Logical Device F (UART F)

CR 30h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: Logical device is inactive. 1: Logical device is active.

CR 60h, 61h. (Default 02h, E8h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select Serial Port 1 I/O base address <100h : FF8h> on 8-byte boundary.

CR 70h. (Default 03h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for Serial Port F.

CR F0h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Delay RXCLK for 5 ns for LG issue. 1: No delay of 5 ns for RXCLK.
6	R / W	0: IRQ is the level mode. 1: IRQ is the pulse mode.
5	R / W	0: Using the original RX FIFO Error Indication signal (USR bit 7). 1: Using new RX FIFO Error Indication signal to solve some issues.
4~2	Reserved.	
1~0	R / W	00: UART F clock source is 1.8462 MHz (24 MHz / 13). 01: UART F clock source is 2 MHz (24 MHz / 12). 00: UART F clock source is 24 MHz (24 MHz / 1). 00: UART F clock source is 14.769 MHz (24 MHz / 1.625).

18. SPECIFICATIONS

18.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage (5V)	4.5 to 5.5	V
Input Voltage	-0.5 to 5VCC+0.5	V
RTC Battery Voltage VBAT	3.0 to 3.6	V
Operating Temperature	0 to +70	°C
Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

18.2 DC CHARACTERISTICS

(T_a = 0°C to 70°C, $5V_{CC}$ = 5V ± 10%, V_{SS} = 0V)

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
RTC Battery Quiescent Current	IBAT			2.4	µA	VBAT = 2.5 V
ACPI Stand-by Power Supply Quiescent Current	ISB			2.0	mA	VSB = 5V, All ACPI pins are not connected.
I/O_{12tp3} – 5V TTL level bi-directional pin with 12mA source-sink capability						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	2.4			V	IOH = -12 mA
Input High Leakage	ILIH			+10	µA	VIN = 5V
Input Low Leakage	ILIL			-10	µA	VIN = 0V
I/O_{12ts} - TTL level Schmitt-trigger bi-directional pin with 12mA source-sink capability						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	
Hysteresis	VTH	0.5	1.2		V	5VCC= 5V
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	2.4			V	IOH = -12 mA
Input High Leakage	ILIH			+10	µA	VIN = 5V
Input Low Leakage	ILIL			-10	µA	VIN = 0V

DC CHARACTERISTICS, continued

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
I/OD_{12t} - TTL level bi-directional pin and open-drain output with 12mA sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/OD_{12ts} - TTL level Schmitt-trigger bi-directional pin and open drain output with 12mA sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	
Hysteresis	V_{TH}	0.5	1.2		V	$5V_{CC}$= 5V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/OD_{12tsu} - TTL level Schmitt-trigger bi-directional pin with internal pull-up resistor and open drain output with 12mA sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	
Hysteresis	V_{TH}	0.5	1.2		V	$5V_{CC}$= 5V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/OD_{16ts} - TTL level Schmitt-trigger bi-directional pin and open drain output with 16mA sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	
Hysteresis	V_{TH}	0.5	1.2		V	$5V_{CC}$= 5V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 16 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V

DC CHARACTERISTICS, continued

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
O_8 - Output pin with 8mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -8 mA
O_{12} - Output pin with 12mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
O_{24} - Output pin with 24mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
O_{12p3} - 5V output pin with 12mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
OD_{12} - Open drain output pin with 12mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
OD_{24} - Open drain output pin with 24mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
IN_t - TTL level input pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{tu} - TTL level input pin with internal pull-up resistor						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{ts} - TTL level Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}	0.8	0.9	1.0	V	5V_{CC} = 5V
Input High Threshold Voltage	V_{t+}	1.8	1.9	2.0	V	5V_{CC} = 5V
Hysteresis	V_{TH}	0.8	1.0		V	5V_{CC} = 5V

DC CHARACTERISTICS, continued

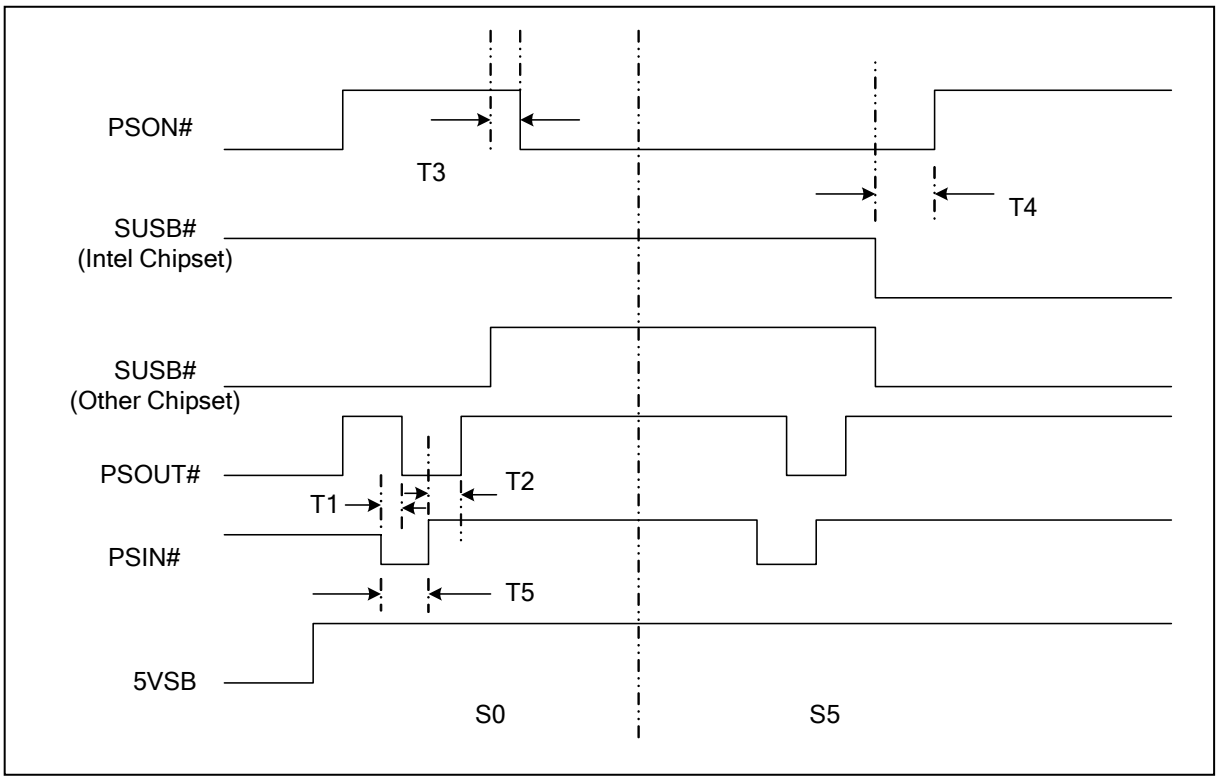
PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{tsu} - TTL level Schmitt-trigger input pin with internal pull-up resistor						
Input Low Threshold Voltage	V_{t-}	0.8	0.9	1.0	V	5V_{CC} = 5V
Input High Threshold Voltage	V_{t+}	1.8	1.9	2.0	V	5V_{CC} = 5V
Hystersis	V_{TH}	0.8	1.0		V	5V_{CC} = 5V
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{tsp3} - 3.3V TTL level Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	$5V_{CC}$ = 5 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	$5V_{CC}$ = 5 V
Hysteresis	V_{TH}	0.5	1.2		V	$5V_{CC}$ = 5 V
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{cd} - CMOS level input pin with internal pull-down resistor						
Input Low Voltage	V_{IL}			0.3 5V_{CC}	V	
Input High Voltage	V_{IH}	0.7 5V_{CC}			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
I/O_{V3} – Bi-direction pin with source capability of 6 mA and sink capability of 1 mA for INTEL® PECI						
Input Low Voltage	V_{IL}	0.275V_{tt}		0.5V_{tt}	V	
Input High Voltage	V_{IH}	0.55V_{tt}		0.725V_{tt}	V	
Output Low Voltage	V_{OL}			0.25V_{tt}	V	
Output High Voltage	V_{OH}	0.75V_{tt}			V	
Hysteresis	V_{Hys}	0.1V_{tt}			V	

DC CHARACTERISTICS, continued

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
I/O_{V4} – Bi-direction pin with source capability of 6 mA and sink capability of 1 mA for INTEL® SST						
Input Low Threshold Voltage	V_{t-}	0.4		0.65	V	
Input High Threshold Voltage	V_{t+}	0.75		1.1	V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 1.5 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
Hysteresis	V_{TH}	0.15			V	

18.3 AC CHARACTERISTICS

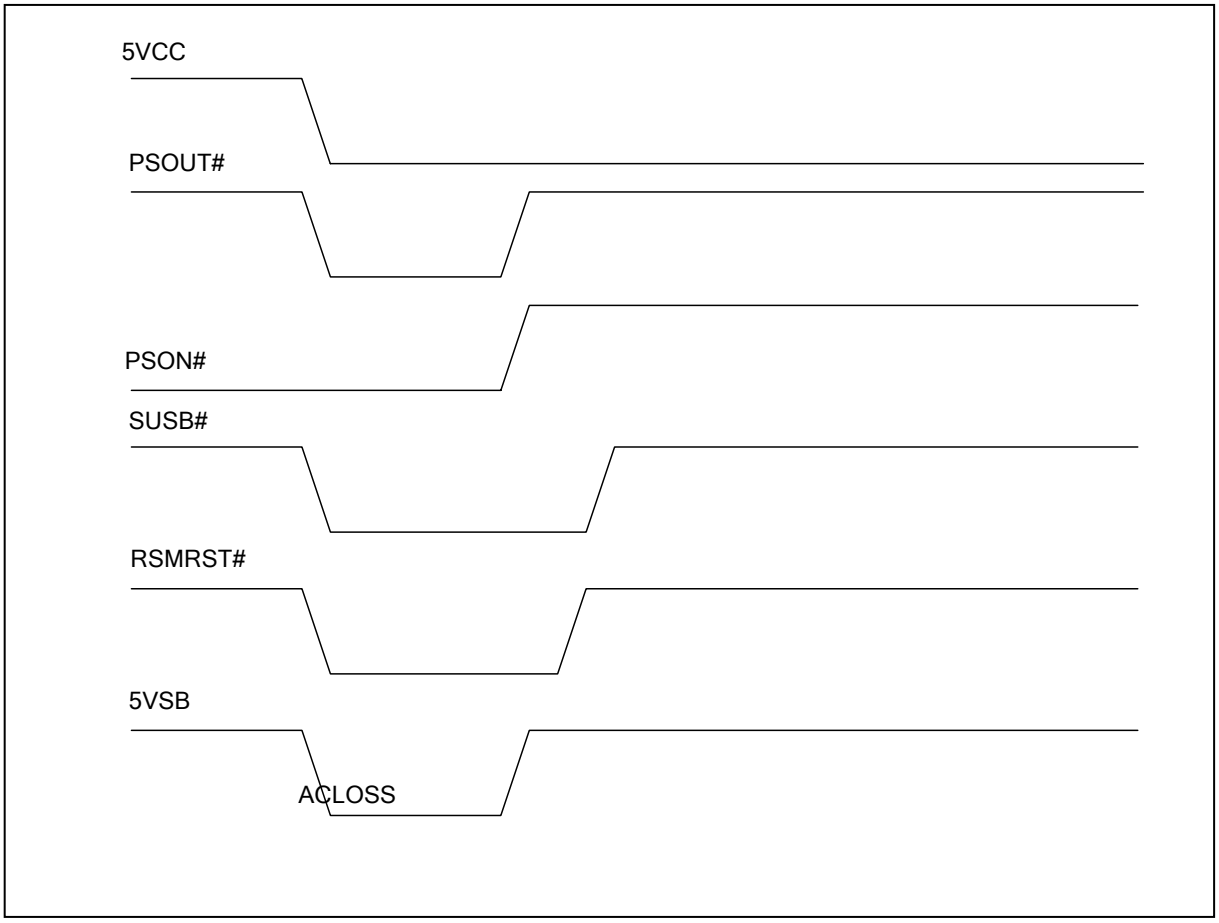
18.3.1 Power On / Off Timing



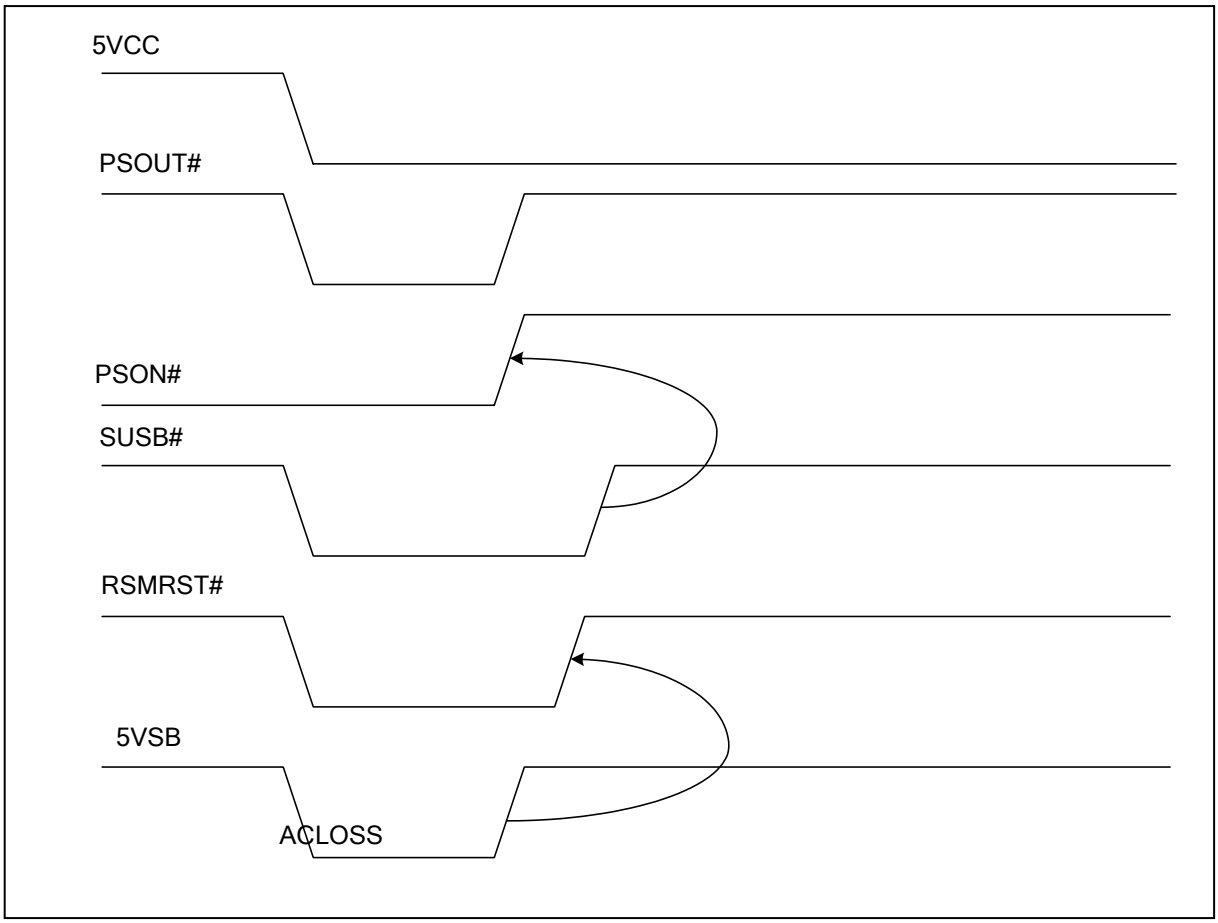
	T1	T2	T3	T4	T5
IDEAL TIMING (SEC)	64m	16m	32m	282m	Over 64m at least

18.3.2 AC Power Failure Resume Timing

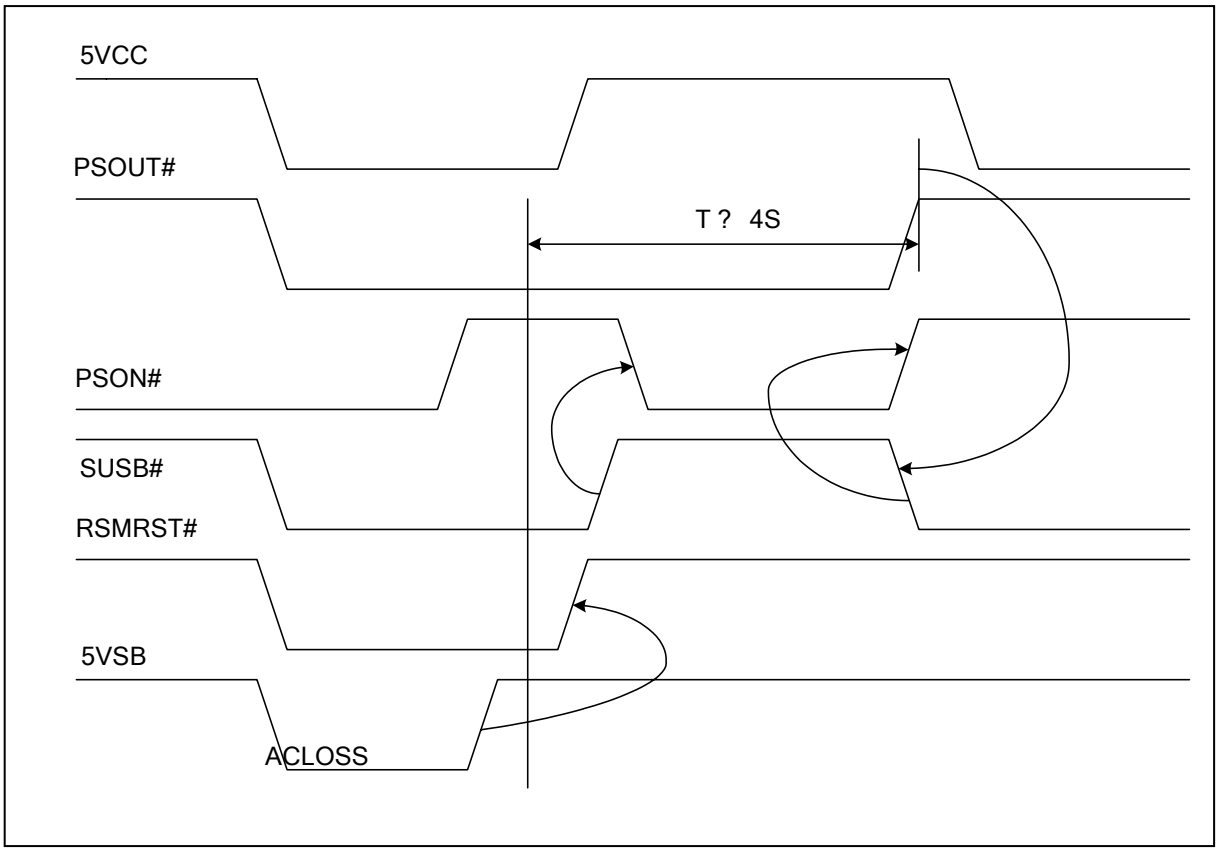
1. Logic device A CRE4 bit7 = “0” and CRE4 bits[6:5] are selected to “OFF” state (“OFF” means always turn off or last state is off)



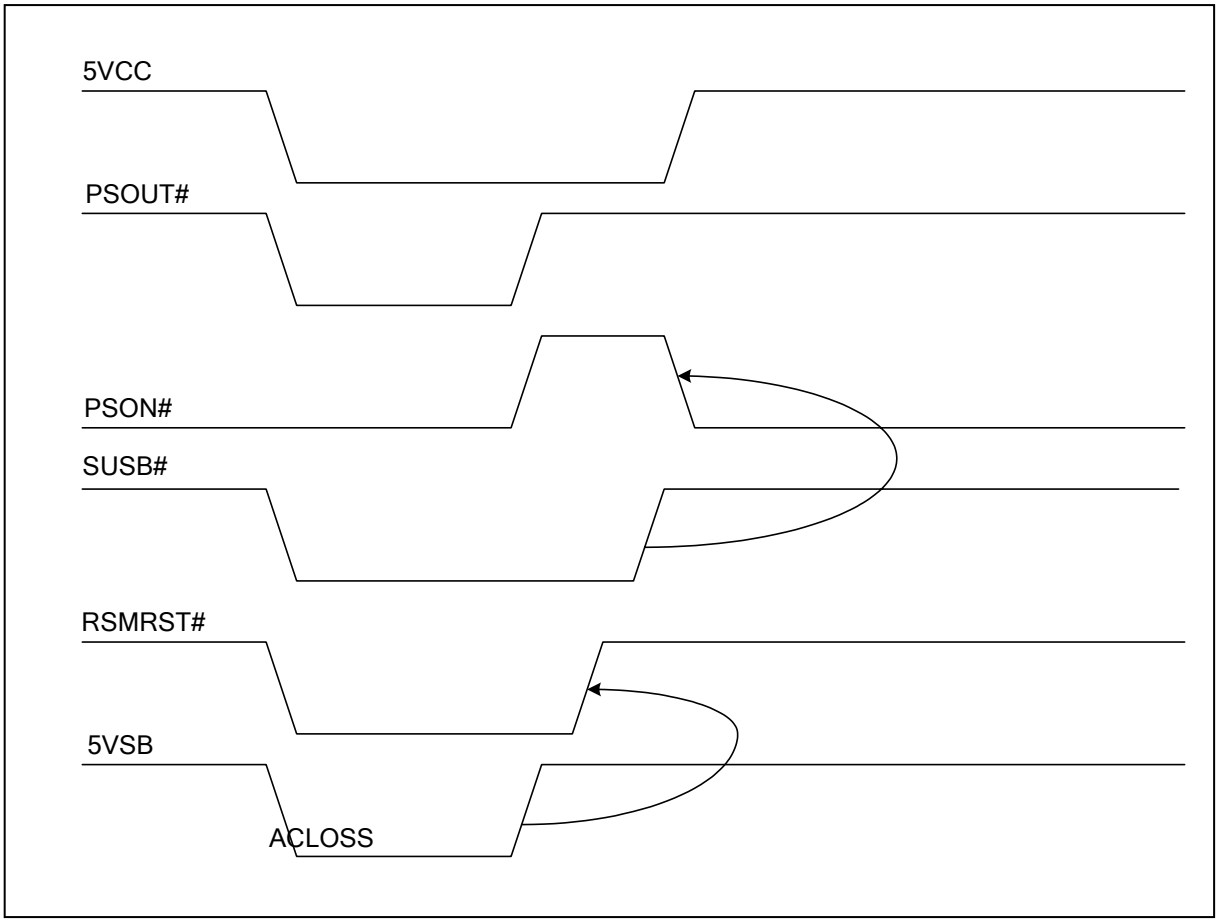
2. Logic device A CRE4 bit7 = “0” and CRE4 bits[6:5] are selected to “ON” state
(“ON” means always turn on or last state is on)



3. Logic device A CRE4 bit7 = “1” and CRE4 bits[6:5] are selected to “OFF” state
(“OFF” means always turn off or last state is off)



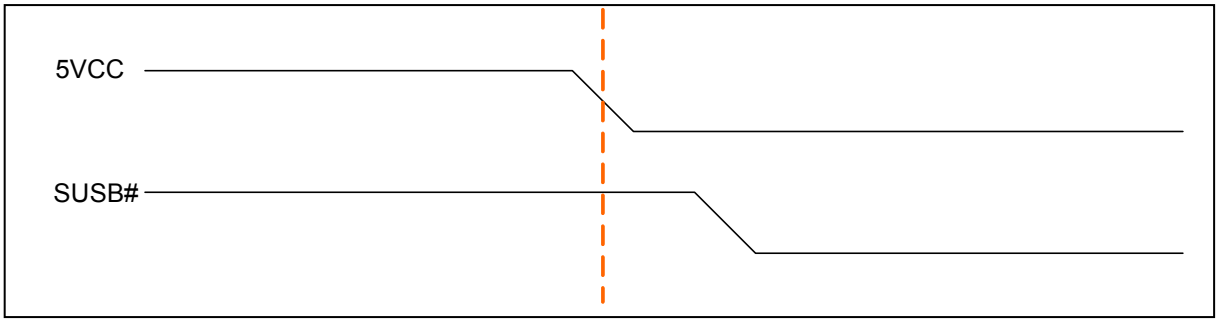
4. Logic device A CRE4 bit7 = “1” and CRE4 bits[6:5] are selected to “ON” state
(“ON” means always turn on or last state is on)



**** What's the definition of last state when AC power failure?**

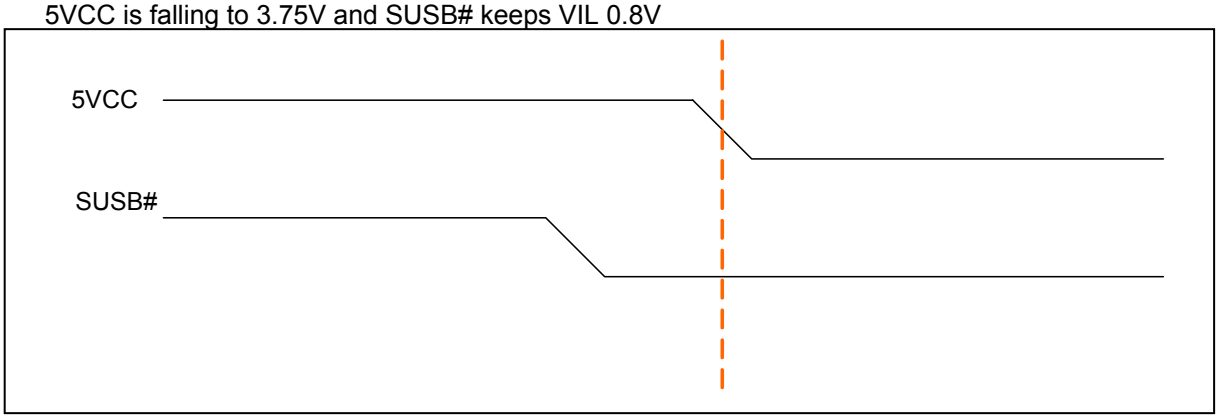
1) Last state is "ON"

5VCC is falling to 3.75V and SUSB# keeps VIH 2.0V



2) Last state is "OFF"

5VCC is falling to 3.75V and SUSB# keeps VIL 0.8V



To prevent that VCC goes down faster than VSB in various ATX Power Supplies. W83627UHG add the "user define mode" option for AC power loss pre-state. BIOS can set the pre-state that is "On" or "Off" state, because the status of AC power resume depends on it.

Logical Device A, CR E4h

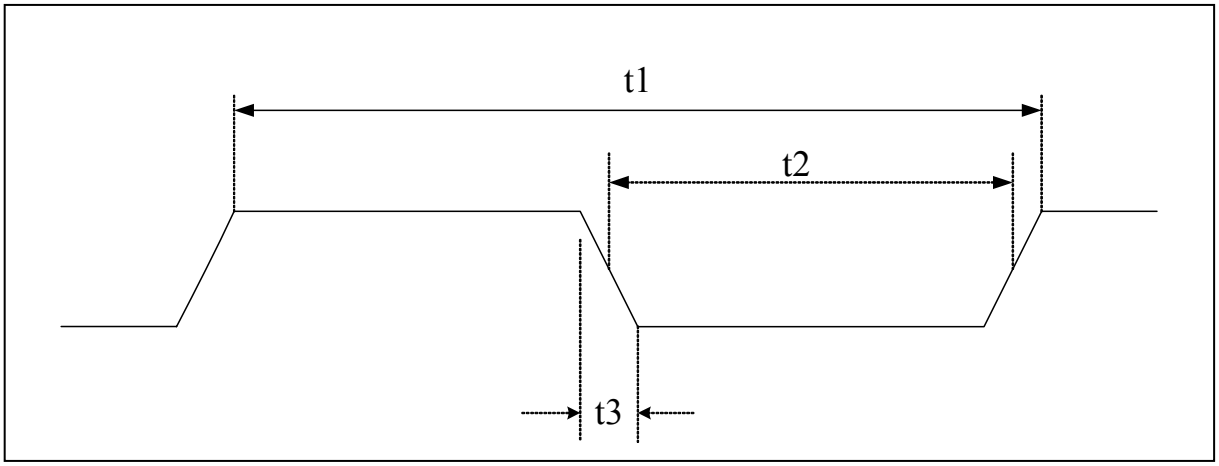
6~5	R / W	Power loss control bits => (**VBAT**) 00: System always turns off when come back from power loss state. 01: System always turns on when come back from power loss state. 10: System turns off / on when come back from power loss state depend on the state before power loss. 11: User define the state before power loss.(The last state set at CRE6[4])

Logical Device A, CR E6h

4	R / W	Power loss Last State Flag. **(VBAT)** 0: ON 1: OFF

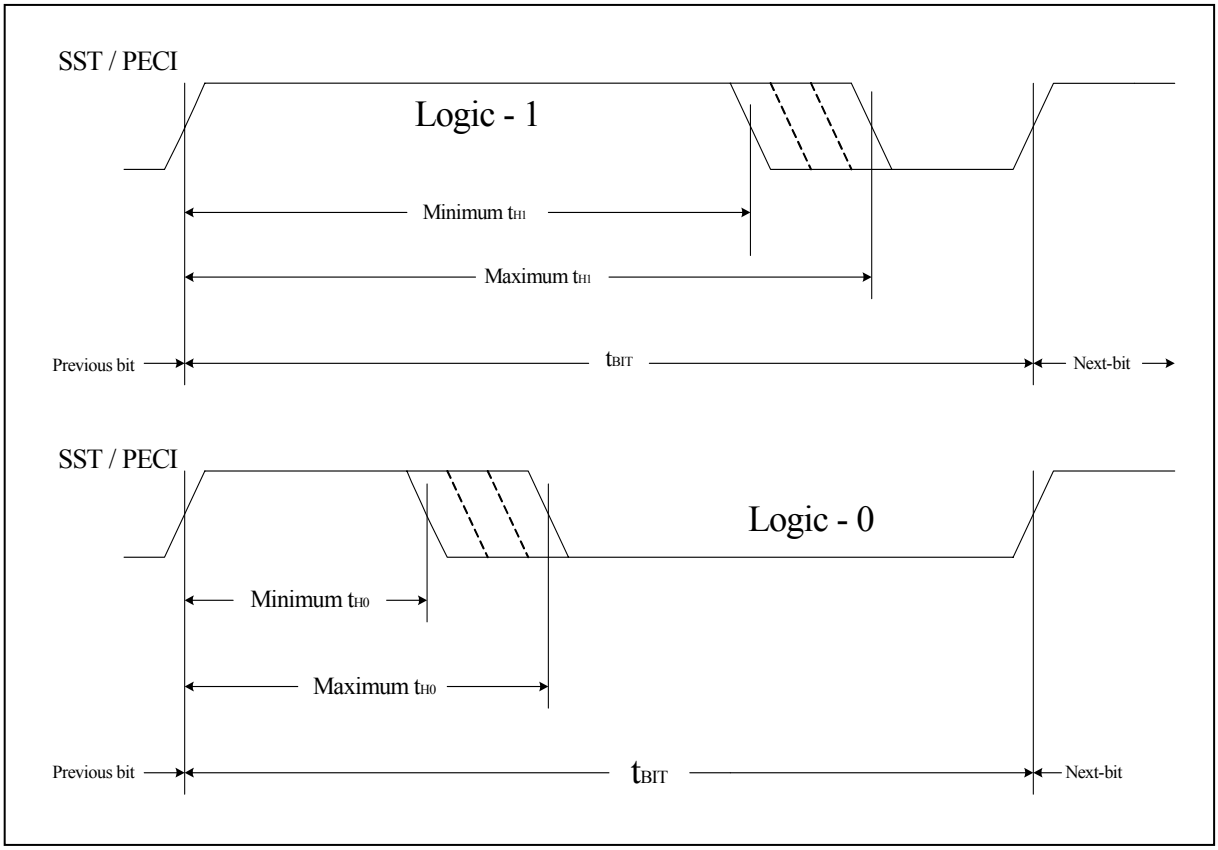
18.3.3 Clock Input Timing

PARAMETER	48MHZ / 24MHZ		UNIT
	MIN	MAX	
Cycle to cycle jitter		300/500	ps
Duty cycle	45	55	%



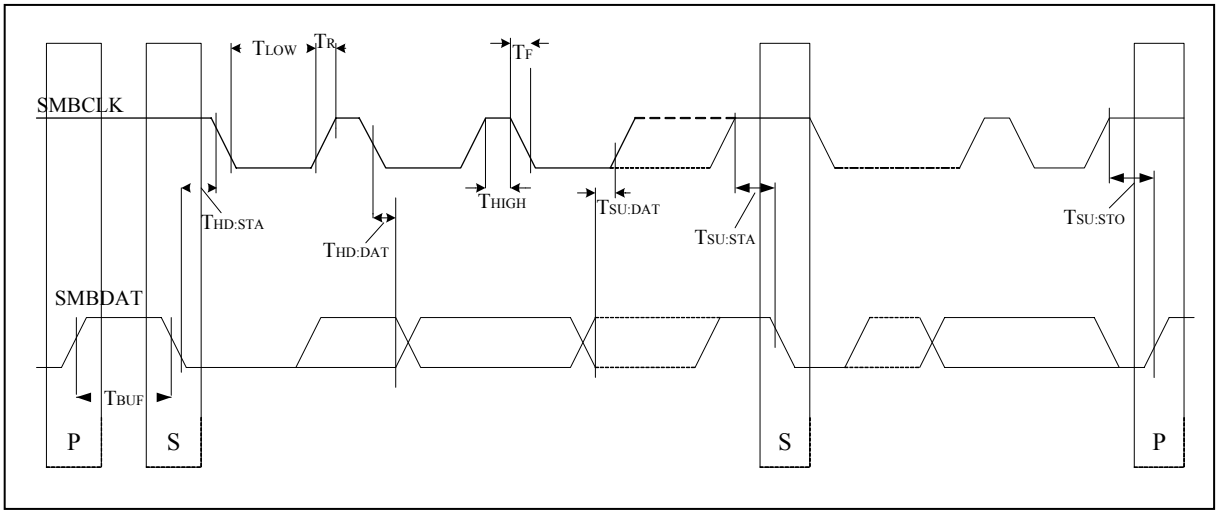
PARAMETER	DESCRIPTION	48MHZ / 24MHZ			UNIT
		MIN	TYP	MAX	
t1	Clock cycle time		20.8 / 41.7		ns
t2	Clock high time/low time	9 / 19	10 / 21		ns
t3	Clock rising time/falling time (0.4V~2.4V)			3	ns

18.3.4 PECI and SST Timing



SYMBOL		MIN	TYP	MAX	UNITS
t_{BIT}	Client	0.495		500	µs
	Originator	0.495		250	
t_{H1}		0.6	3/4	0.8	× t_{BIT}
t_{H0}		0.2	1/4	0.4	× t_{BIT}

18.3.5 SMBus Timing



18.3.6 Floppy Disk Drive Timing

FDC: Data rate = 1MB, 500KB, 300KB, 250KB/sec.

PARAMETER	SYM.	MIN.	TYP. (NOTE 1)	MAX.	UNIT
DIR# setup time to STEP#	TDST	1.0/1.6 /2.0/4.0			µS
DIR# hold time from STEP#	TSTD	24/40 /48/96			µS
STEP# pulse width	TSTP	6.8/11.5 /13.8/27.8	7/11.7 /14/28	7.2/11.9 /14.2/28.2	µS
STEP# cycle width	TSC	NOTE 2	NOTE 2	NOTE 2	mS
INDEX# pulse width	TIDX	125/250 /417/500			nS
RDATA# pulse width	TRD	40			nS
WD# pulse width	TWD	100/185 /225/475	125/210 /250/500	150/235 /275/525	nS

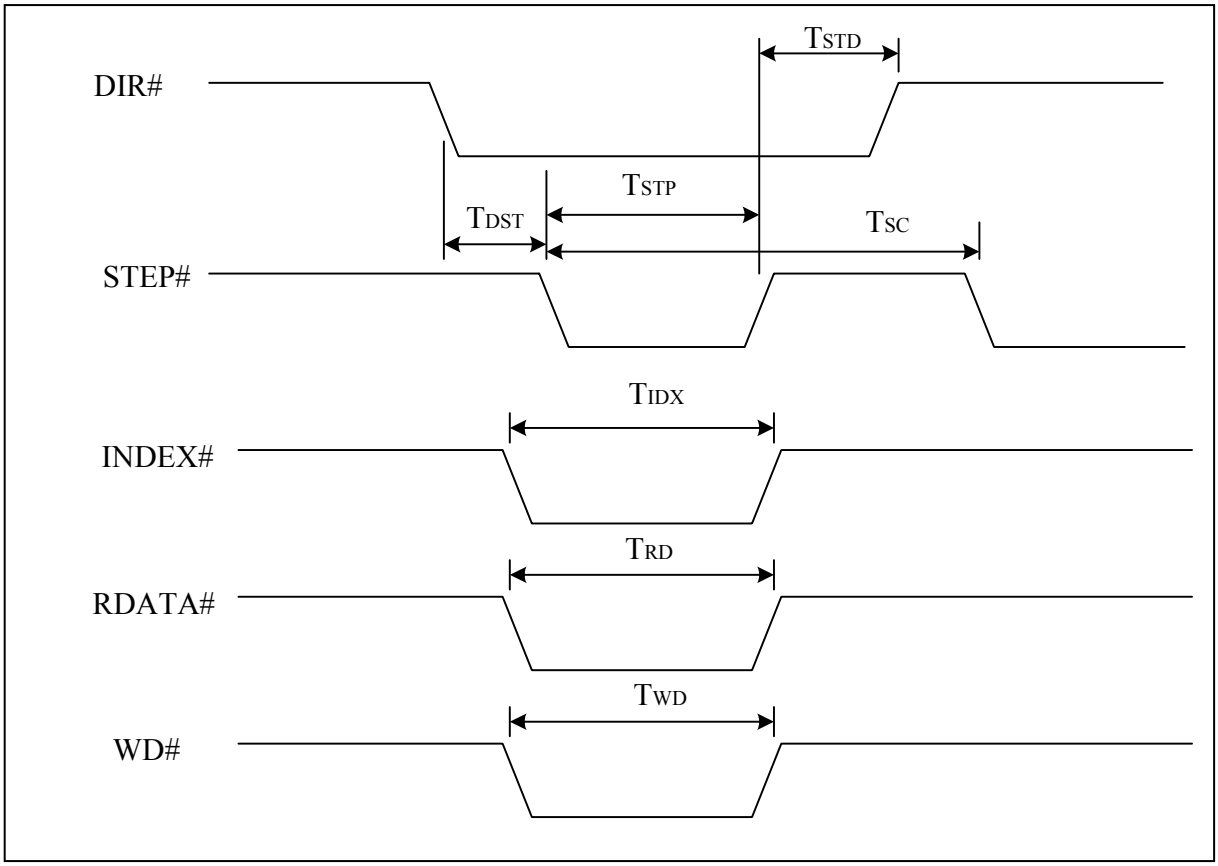
Notes:

1. Typical values for T = 25°C and normal supply voltage.
2. Programmable from 0.5 mS through 32 mS as described in step rate table. (Please refer to the description of the SPECIFY command set.)

Step Rate Table

DATA RATE SRT	1MB/S	500KB/S	300KB/S	250KB/S
0	8	16	26.7	32
1	7.5	15	25	30
…	…	…	…	…
E	1.0	2	3.33	4
F	0.5	1	1.67	2

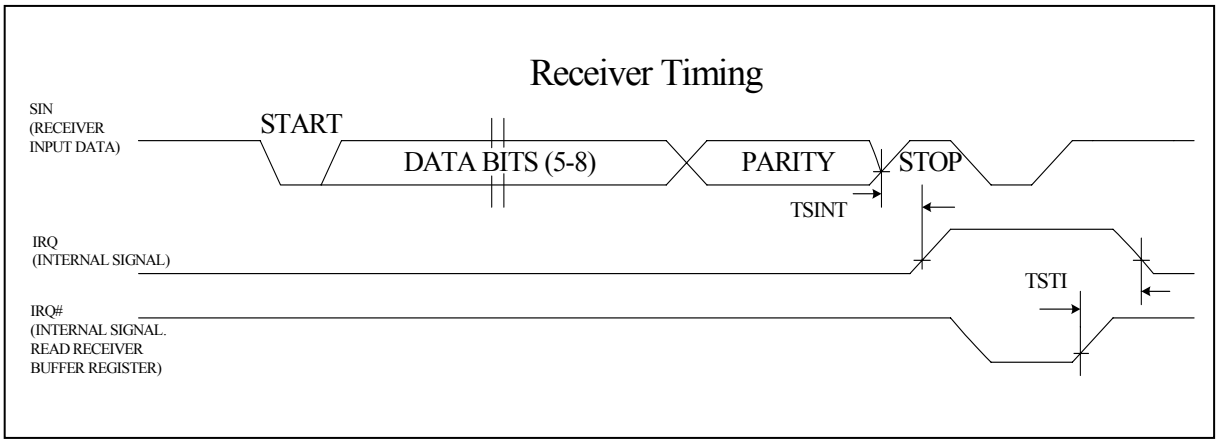
Floppy Disk Driving Timing



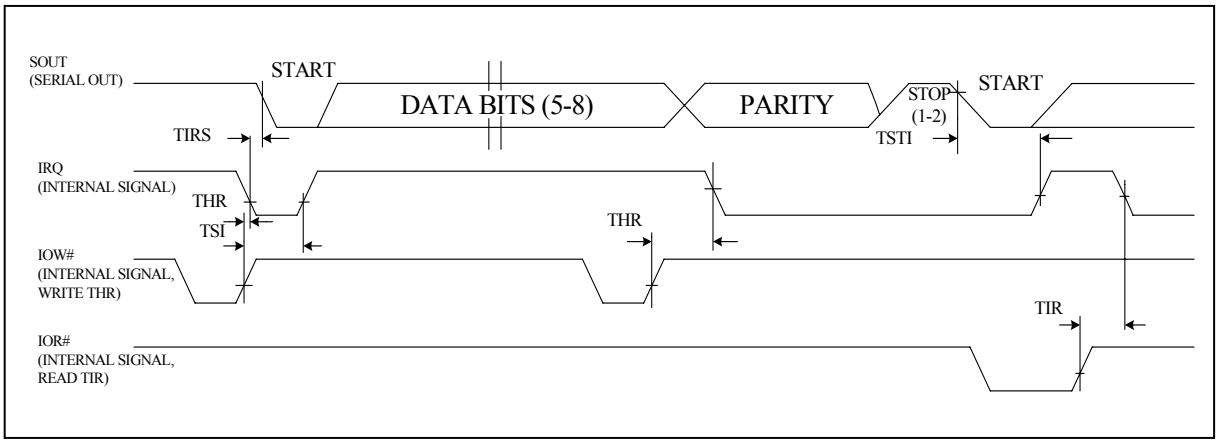
18.3.7 UART/Parallel Port

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Delay from Stop to Set Interrupt	TSINT		9/16		Baud Rate
Delay from $\overline{IOR}$ Reset Interrupt	TRINT		9	1000	nS
Delay from Initial IRQ Reset to Transmit Start	TIRS		1/16	8/16	Baud Rate
Delay from to Reset interrupt	THR			175	nS
Delay from Initial $\overline{IOW}$ to interrupt	TSI		9/16	16/16	Baud Rate
Delay from Stop to Set Interrupt	TSTI			8/16	Baud Rate
Delay from $\overline{IOR}$ to Reset Interrupt	TIR		8	250	nS
Delay from $\overline{IOR}$ to Output	TMWO		6	200	nS
Set Interrupt Delay from Modem Input	TSIM		18	250	nS
Reset Interrupt Delay from $\overline{IOR}$	TRIM		9	250	nS
Baud Divisor	N	100 pF Loading		2^{16}-1	

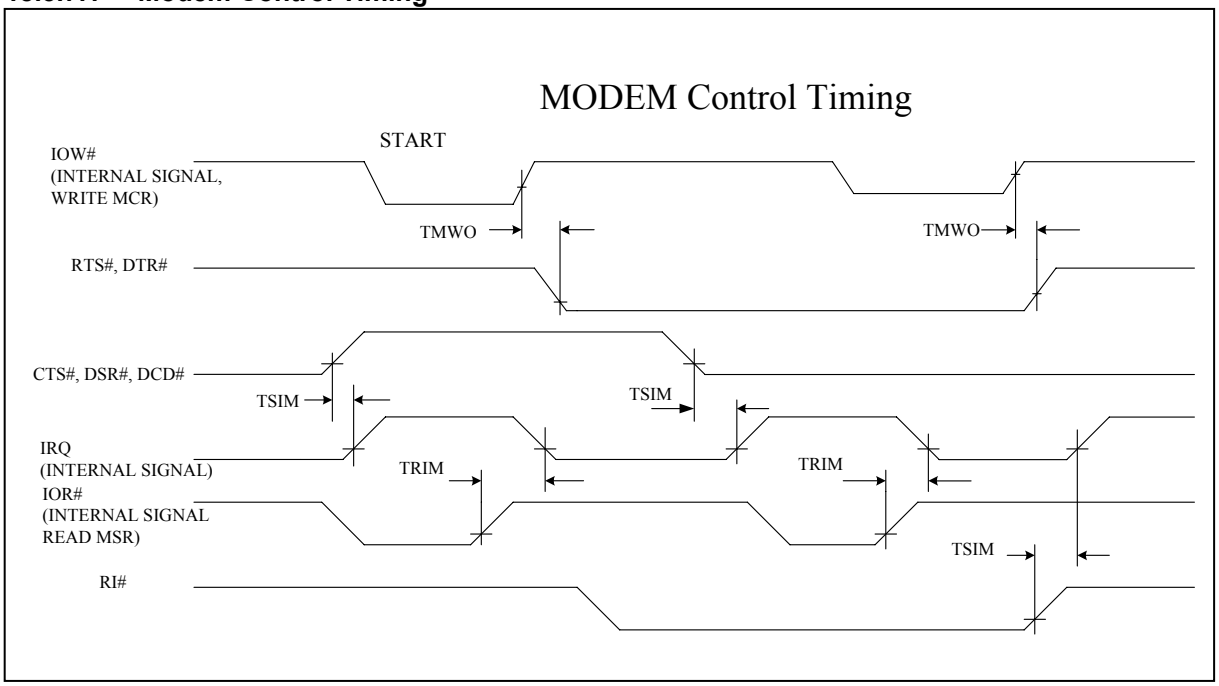
UART Receiver Timing



UART Transmitter Timing



18.3.7.1 Modem Control Timing

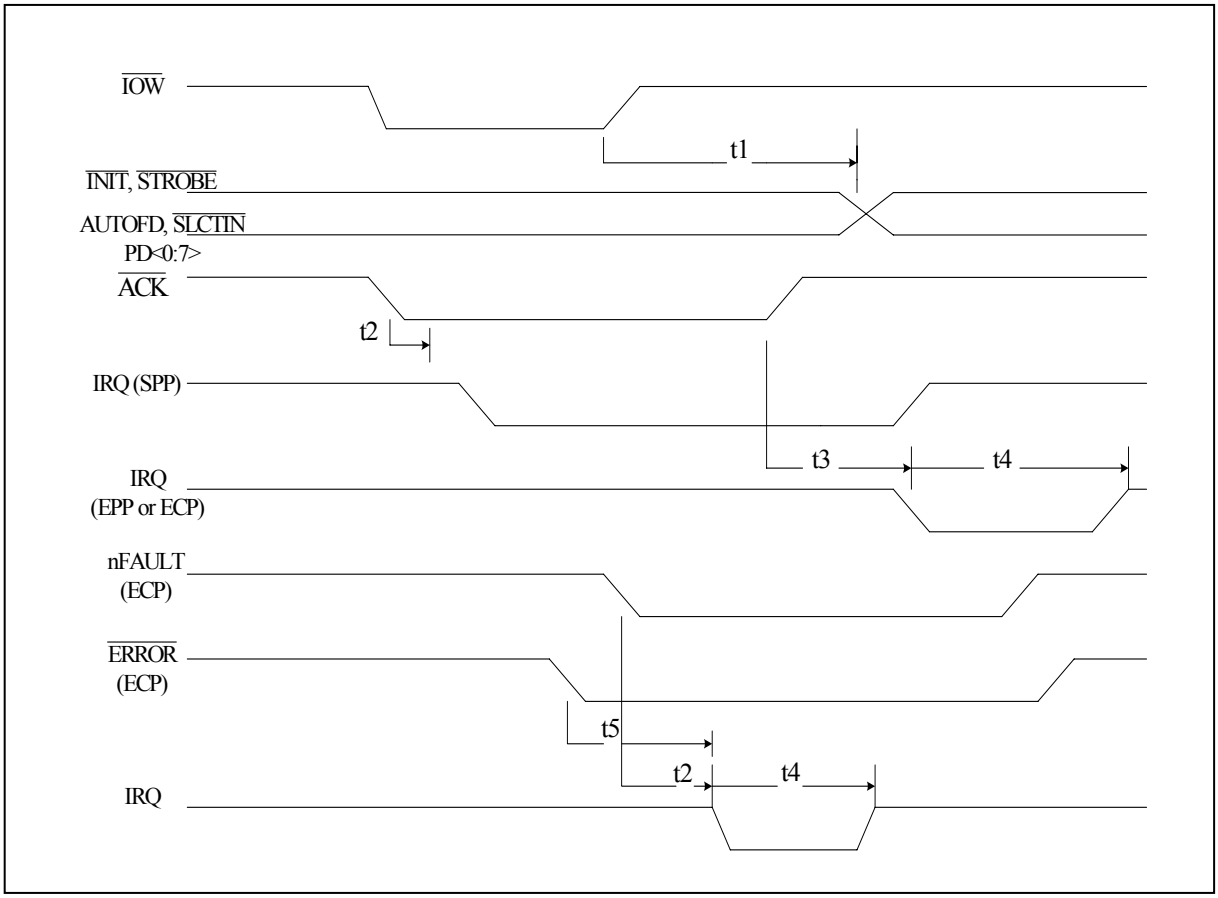


18.3.8 Parallel Port Mode Parameters

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT
PD0-7, $\overline{\text{INDEX}}$, $\overline{\text{STROBE}}$, $\overline{\text{AUTOFD}}$ Delay from $\overline{\text{IOW}}$	t1			100	nS
IRQ Delay from $\overline{\text{ACK}}$, nFAULT	t2			60	nS
IRQ Delay from $\overline{\text{IOW}}$	t3			105	nS
IRQ Active Low in ECP and EPP Modes	t4	200		300	nS
$\overline{\text{ERROR}}$ Active to IRQ Active	t5			105	nS
PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT
PD0-7, $\overline{\text{INDEX}}$, $\overline{\text{STROBE}}$, $\overline{\text{AUTOFD}}$ Delay from $\overline{\text{IOW}}$	t1			100	nS
IRQ Delay from $\overline{\text{ACK}}$, nFAULT	t2			60	nS
IRQ Delay from $\overline{\text{IOW}}$	t3			105	nS
IRQ Active Low in ECP and EPP Modes	t4	200		300	nS
$\overline{\text{ERROR}}$ Active to IRQ Active	t5			105	nS

18.3.9 Parallel Port

18.3.9.1 Parallel Port Timing



18.3.9.2 EPP Data or Address Read Cycle Timing Parameters

PARAMETER	SYM.	MIN.	MAX.	UNIT
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Deasserted	t14	0	185	nS
Deasserted to $\overline{\text{WRITE}}$ Modified	t15	60	190	nS
$\overline{\text{WAIT}}$ Asserted to PD Hi-Z	t17	60	180	nS
Command Asserted to PD Valid	t18	0		nS
Command Deasserted to PD Hi-Z	t19	0		nS
$\overline{\text{WAIT}}$ Deasserted to PD Drive	t20	60	190	nS
$\overline{\text{WRITE}}$ Deasserted to Command	t21	1		nS

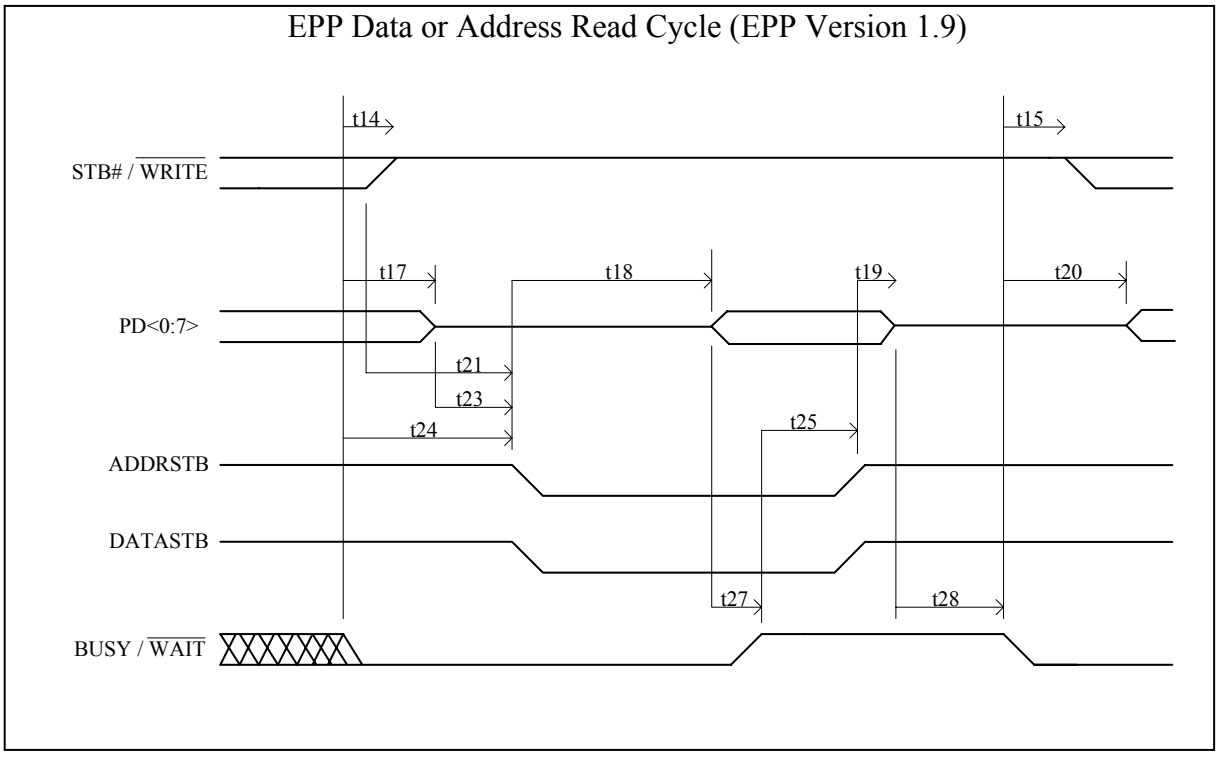
EPP Data or Address Read Cycle Timing Parameters, continued

PARAMETER	SYM.	MIN.	MAX.	UNIT
PBDIR Set to Command	t22	0	20	nS
PD Hi-Z to Command Asserted	t23	0	30	nS
Asserted to Command Asserted	t24	0	195	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t25	60	180	nS
Time out	t26	10	12	nS
PD Valid to $\overline{\text{WAIT}}$ Deasserted	t27	0		nS
PD Hi-Z to $\overline{\text{WAIT}}$ Deasserted	t28	0		μS
PARAMETER	SYM.	MIN.	MAX.	UNIT
Ax Valid to $\overline{\text{IOR}}$ Asserted	t1	40		nS
IOCHRDY Deasserted to $\overline{\text{IOR}}$ Deasserted	t2	0		nS
$\overline{\text{IOR}}$ Deasserted to Ax Valid	t3	10	10	nS
$\overline{\text{IOR}}$ Deasserted to $\overline{\text{IOW}}$ or $\overline{\text{IOR}}$ Asserted	t4	40		
$\overline{\text{IOR}}$ Asserted to IOCHRDY Asserted	t5	0	24	nS
PD Valid to SD Valid	t6	0	75	nS
$\overline{\text{IOR}}$ Deasserted to SD Hi-Z (Hold Time)	t7	0	40	μS
SD Valid to IOCHRDY Deasserted	t8	0	85	nS
$\overline{\text{WAIT}}$ Deasserted to IOCHRDY Deasserted	t9	60	160	nS
PD Hi-Z to PDBIR Set	t10	0		nS
$\overline{\text{WRITE}}$ Deasserted to $\overline{\text{IOR}}$ Asserted	t13	0		nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Deasserted	t14	0	185	nS
Deasserted to $\overline{\text{WRITE}}$ Modified	t15	60	190	nS
$\overline{\text{IOR}}$ Asserted to PD Hi-Z	t16	0	50	nS
$\overline{\text{WAIT}}$ Asserted to PD Hi-Z	t17	60	180	nS
Command Asserted to PD Valid	t18	0		nS
Command Deasserted to PD Hi-Z	t19	0		nS
$\overline{\text{WAIT}}$ Deasserted to PD Drive	t20	60	190	nS
$\overline{\text{WRITE}}$ Deasserted to Command	t21	1		nS
PBDIR Set to Command	t22	0	20	nS
PD Hi-Z to Command Asserted	t23	0	30	nS
Asserted to Command Asserted	t24	0	195	nS

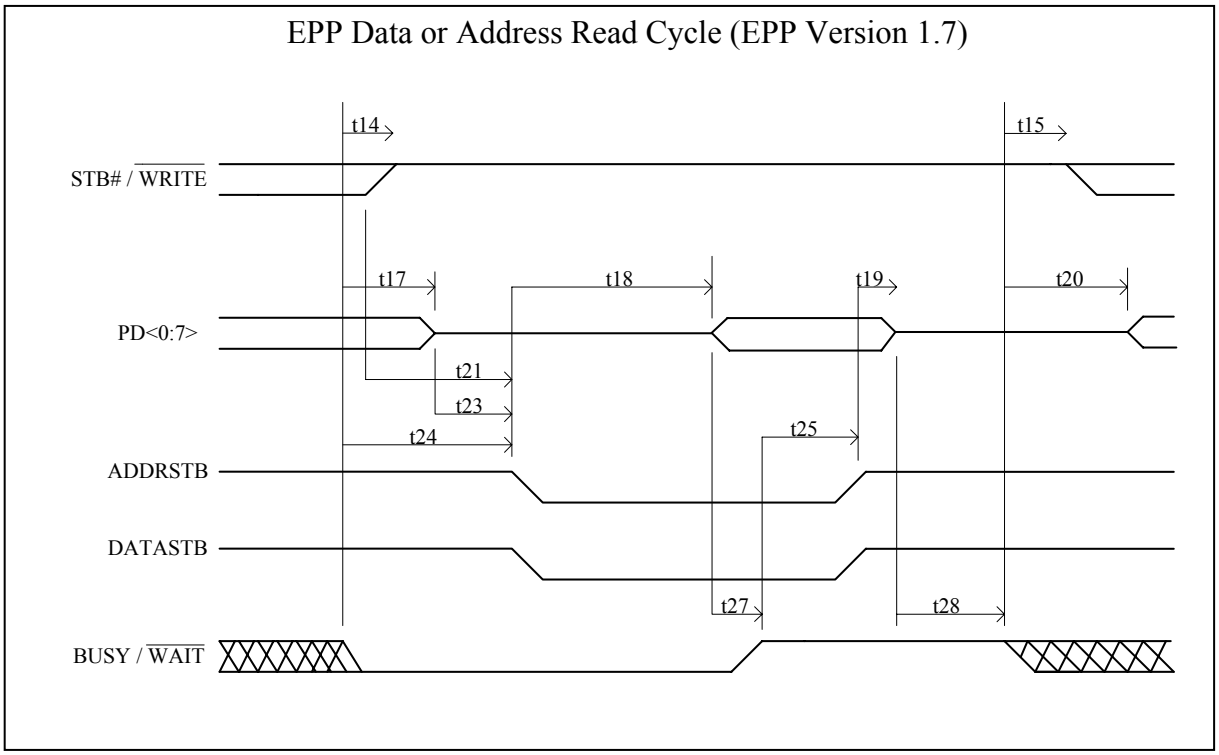
EPP Data or Address Read Cycle Timing Parameters, continued

PARAMETER	SYM.	MIN.	MAX.	UNIT
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t25	60	180	nS
Time out	t26	10	12	nS
PD Valid to $\overline{\text{WAIT}}$ Deasserted	t27	0		nS
PD Hi-Z to $\overline{\text{WAIT}}$ Deasserted	t28	0		µS

18.3.9.3 EPP Data or Address Read Cycle (EPP Version 1.9)



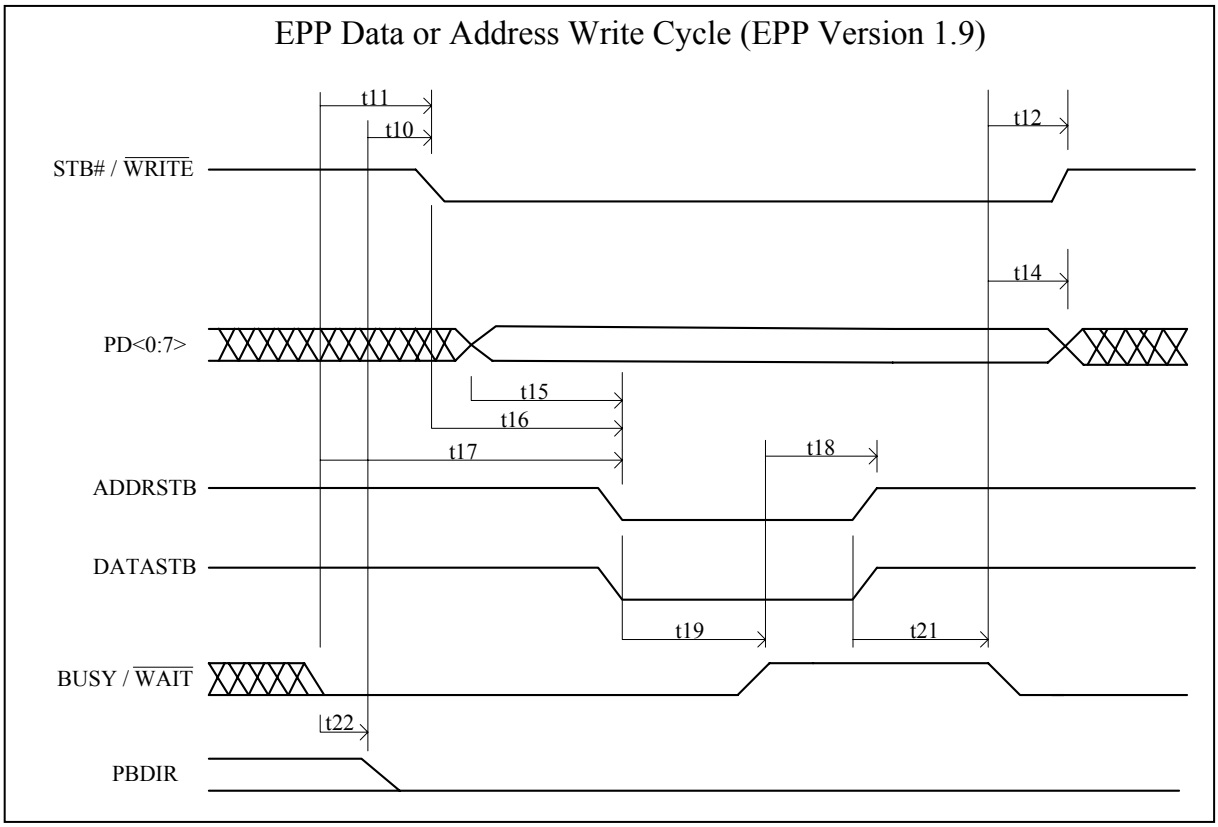
18.3.9.4 EPP Data or Address Read Cycle (EPP Version 1.7)



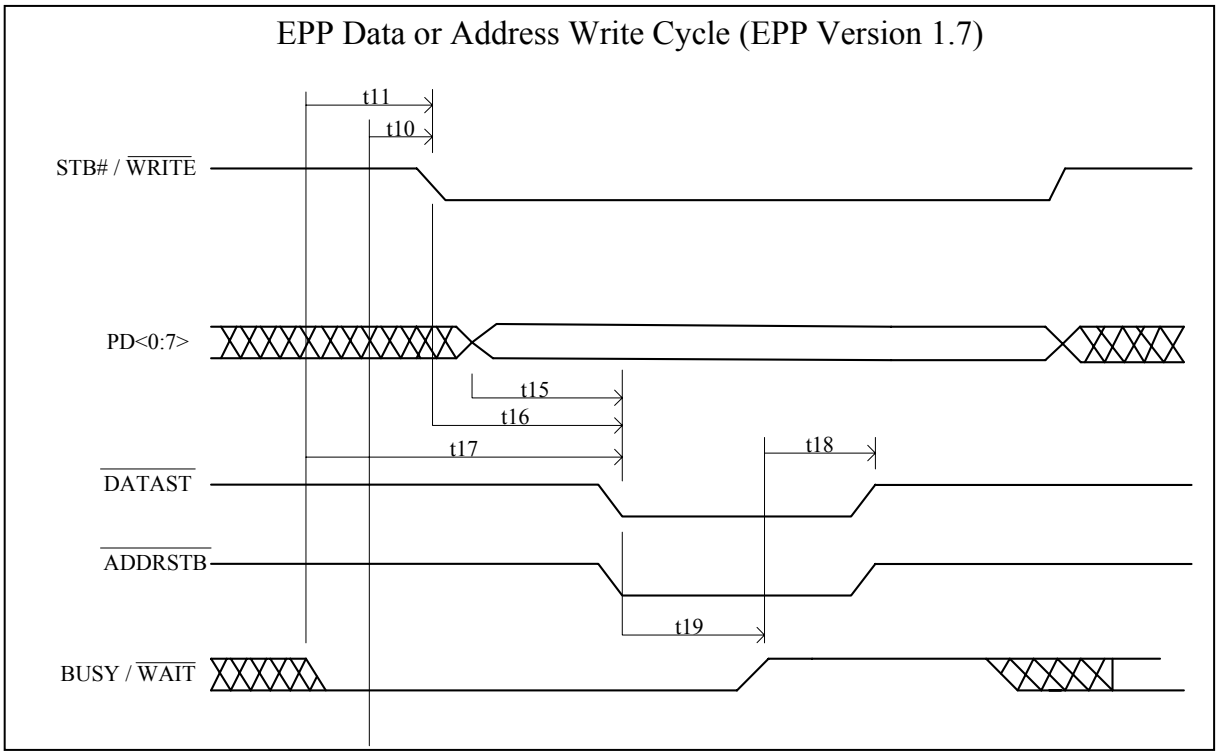
18.3.9.5 EPP Data or Address Write Cycle Timing Parameters

PARAMETER	SYM.	MIN.	MAX.	UNIT
PBDIR Low to $\overline{\text{WRITE}}$ Asserted	t10	0	-	nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Asserted	t11	60	185	nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Change	t12	60	185	nS
$\overline{\text{WAIT}}$ Asserted to PD Invalid	t14	0	-	nS
PD Invalid to Command Asserted	t15	10	-	nS
$\overline{\text{WAIT}}$ Asserted to Command Asserted	t17	60	210	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t18	60	190	nS
Command Asserted to $\overline{\text{WAIT}}$ Deasserted	t19	0	10	μS
Time out	t20	10	12	μS
Command Deasserted to $\overline{\text{WAIT}}$ Asserted	t21	0	-	nS
Ax Valid to $\overline{\text{IOW}}$ Asserted	t1	40	-	nS
SD Valid to Asserted	t2	10	-	nS
$\overline{\text{IOW}}$ Deasserted to Ax Invalid	t3	10	-	nS
$\overline{\text{WAIT}}$ Deasserted to IOCHRDY Deasserted	t4	0	-	nS
Command Asserted to $\overline{\text{WAIT}}$ Deasserted	t5	10	-	nS
$\overline{\text{IOW}}$ Deasserted to $\overline{\text{IOW}}$ or $\overline{\text{IOR}}$ Asserted	t6	40	-	nS
IOCHRDY Deasserted to $\overline{\text{IOW}}$ Deasserted	t7	0	24	nS
$\overline{\text{WAIT}}$ Asserted to Command Asserted	t8	60	160	nS
$\overline{\text{IOW}}$ Asserted to $\overline{\text{WAIT}}$ Asserted	t9	0	70	nS
PBDIR Low to $\overline{\text{WRITE}}$ Asserted	t10	0	-	nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Asserted	t11	60	185	nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Change	t12	60	185	nS
$\overline{\text{IOW}}$ Asserted to PD Valid	t13	0	50	nS
$\overline{\text{WAIT}}$ Asserted to PD Invalid	t14	0	-	nS
PD Invalid to Command Asserted	t15	10	-	nS
$\overline{\text{IOW}}$ to Command Asserted	t16	5	35	nS
$\overline{\text{WAIT}}$ Asserted to Command Asserted	t17	60	210	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t18	60	190	nS
Command Asserted to $\overline{\text{WAIT}}$ Deasserted	t19	0	10	μS
Time out	t20	10	12	μS
Command Deasserted to $\overline{\text{WAIT}}$ Asserted	t21	0	-	nS
$\overline{\text{IOW}}$ Deasserted to $\overline{\text{WRITE}}$ Deasserted and PD invalid	t22	0	-	nS
$\overline{\text{WRITE}}$ to Command Asserted	t16	5	35	nS

18.3.9.6 EPP Data or Address Write Cycle (EPP Version 1.9)



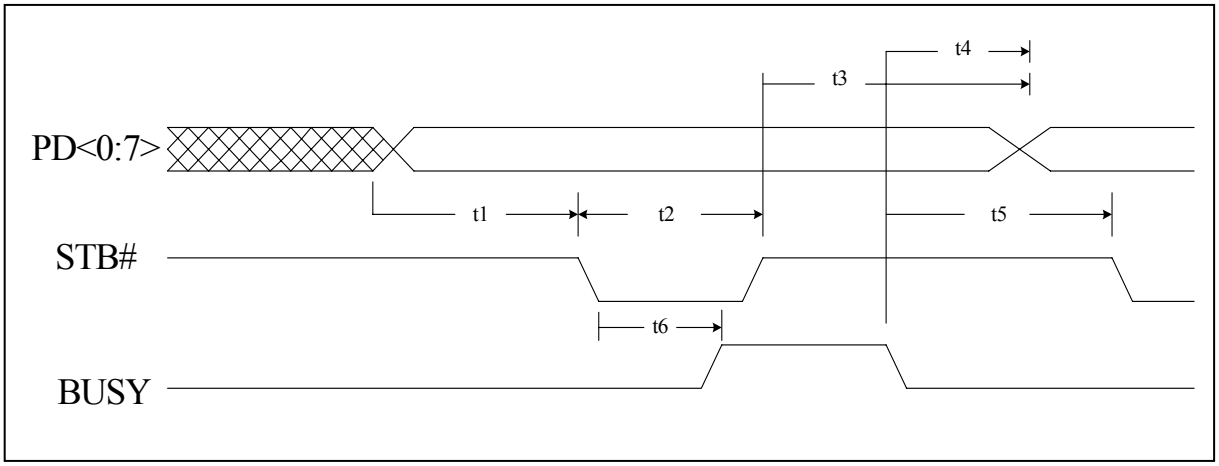
18.3.9.7 EPP Data or Address Write Cycle (EPP Version 1.7)



18.3.9.8 Parallel Port FIFO Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DATA Valid to nSTROBE Active	t1	600	-	nS
nSTROBE Active Pulse Width	t2	600	-	nS
DATA Hold from nSTROBE Inactive	t3	450	-	nS
BUSY Inactive to PD Inactive	t4	80	-	nS
BUSY Inactive to nSTROBE Active	t5	680	-	nS
nSTROBE Active to BUSY Active	t6	-	500	nS

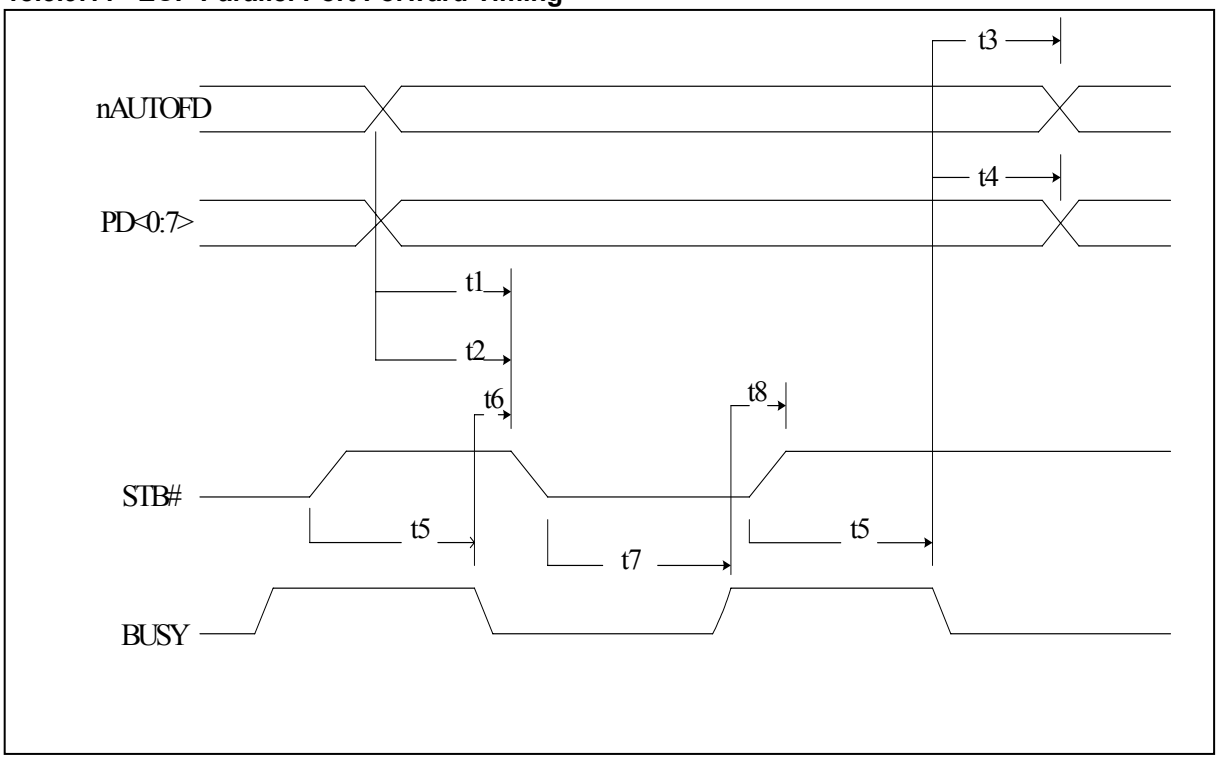
18.3.9.9 Parallel FIFO Timing



18.3.9.10 ECP Parallel Port Forward Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
nAUTOFD Valid to nSTROBE Asserted	t1	0	60	nS
PD Valid to nSTROBE Asserted	t2	0	60	nS
BUSY Deasserted to nAUTOFD Changed	t3	80	180	nS
BUSY Deasserted to PD Changed	t4	80	180	nS
nSTROBE Deasserted to BUSY Deasserted	t5	0	-	nS
BUSY Deasserted to nSTROBE Asserted	t6	80	200	nS
nSTROBE Asserted to BUSY Asserted	t7	0	-	nS
BUSY Asserted to nSTROBE Deasserted	t8	80	180	nS

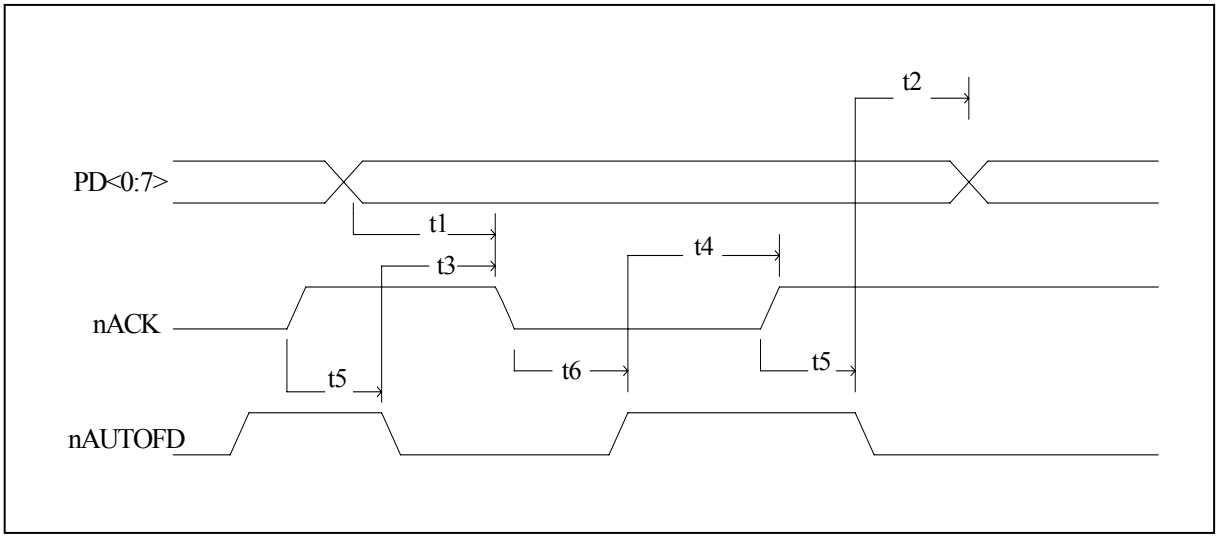
18.3.9.11 ECP Parallel Port Forward Timing



18.3.9.12 ECP Parallel Port Reverse Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
PD Valid to nACK Asserted	t1	0	-	nS
nAUTOFD Deasserted to PD Changed	t2	0	-	nS
nAUTOFD Asserted to nACK Asserted	t3	0	-	nS
nAUTOFD Deasserted to nACK Deasserted	t4	0	-	nS
nACK Deasserted to nAUTOFD Asserted	t5	80	200	nS
PD Changed to nAUTOFD Deasserted	t6	80	200	nS

18.3.9.13 ECP Parallel Port Reverse Timing



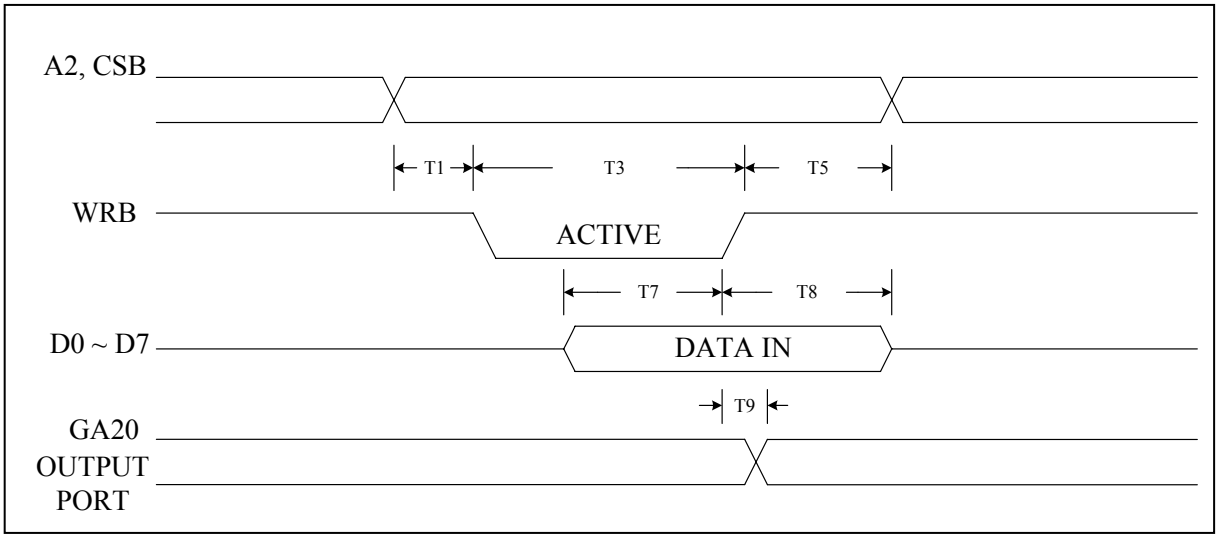
18.3.10 KBC Timing Parameters

NO.	DESCRIPTION	MIN.	MAX.	UNIT
T1	Address Setup Time from WRB	0	-	nS
T2	Address Setup Time from RDB	0	-	nS
T3	WRB Strobe Width	20	-	nS
T4	RDB Strobe Width	20	-	nS
T5	Address Hold Time from WRB	0	-	nS
T6	Address Hold Time from RDB	0	-	nS
T7	Data Setup Time	50	-	nS
T8	Data Hold Time	0	-	nS
T9	Gate Delay Time from WRB	10	30	nS
T10	RDB to Drive Data Delay	-	40	nS
T11	RDB to Floating Data Delay	0	20	nS
T12	Data Valid After Clock Falling (SEND)	-	4	µS
T13	K/B Clock Period	20	-	µS
T14	K/B Clock Pulse Width	10	-	µS
T15	Data Valid Before Clock Falling (RECEIVE)	4	-	µS
T16	K/B ACK After Finish Receiving	20	-	µS

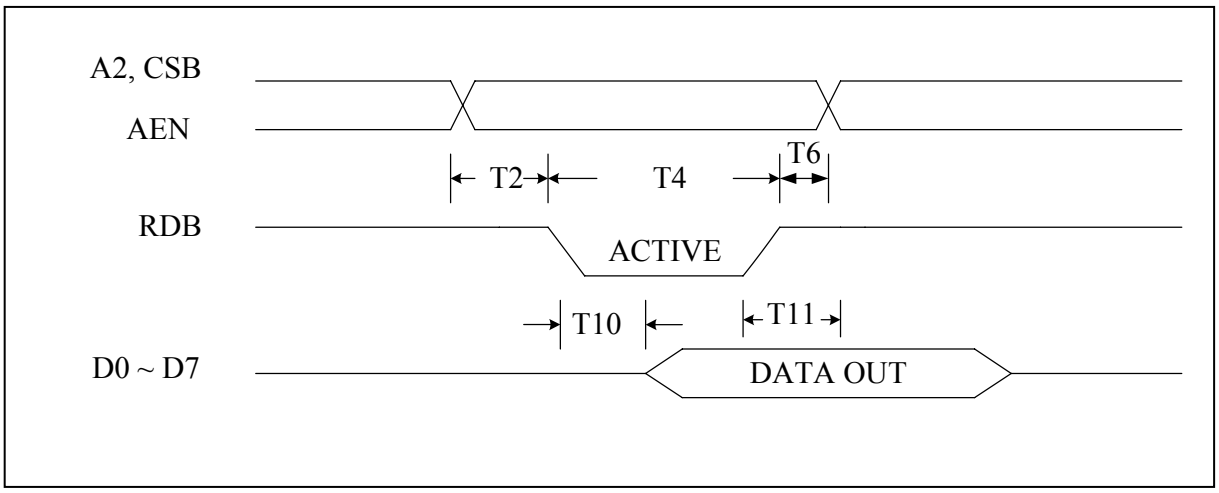
KBC Timing Parameters, continued

NO.	DESCRIPTION	MIN.	MAX.	UNIT
T19	Transmit Timeout	-	2	mS
T20	Data Valid Hold Time	0	-	µS
T21	Input Clock Period (6–16 Mhz)	63	167	nS
T22	Duration of CLK inactive	30	50	µS
T23	Duration of CLK active	30	50	µS
T24	Time from inactive CLK transition, used to time when the auxiliary device sample DATA	5	25	µS
T25	Time of inhibit mode	100	300	µS
T26	Time from rising edge of CLK to DATA transition	5	T28-5	µS
T27	Duration of CLK inactive	30	50	µS
T28	Duration of CLK active	30	50	µS
T29	Time from DATA transition to falling edge of CLK	5	25	µS

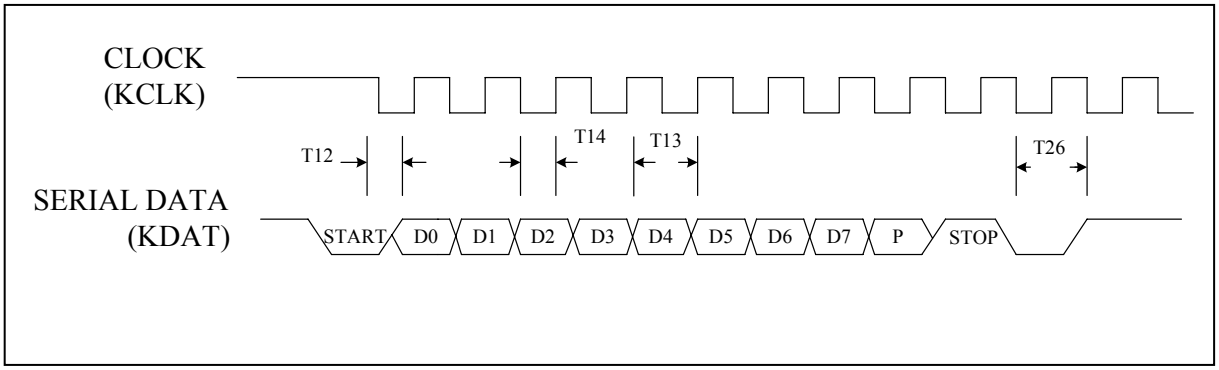
18.3.10.1 Writing Cycle Timing



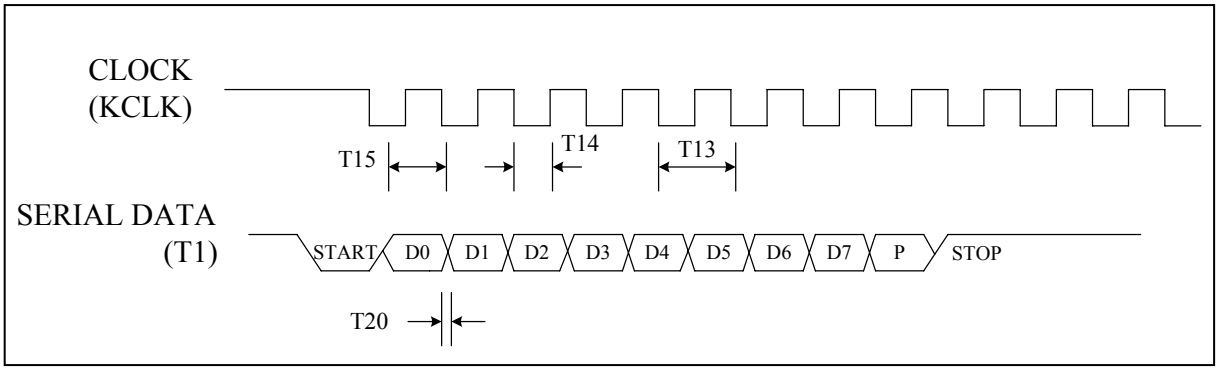
18.3.10.2 Read Cycle Timing



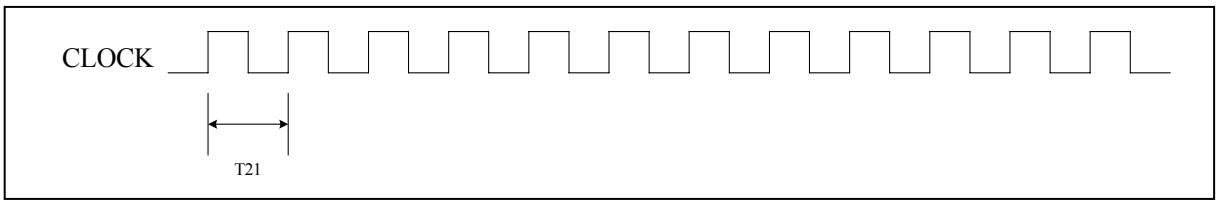
18.3.10.3 Send Data to K/B



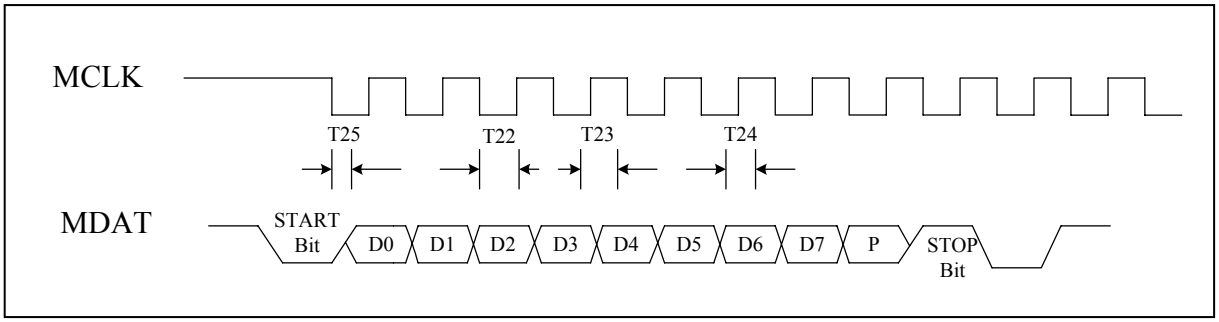
18.3.10.4 Receive Data from K/B



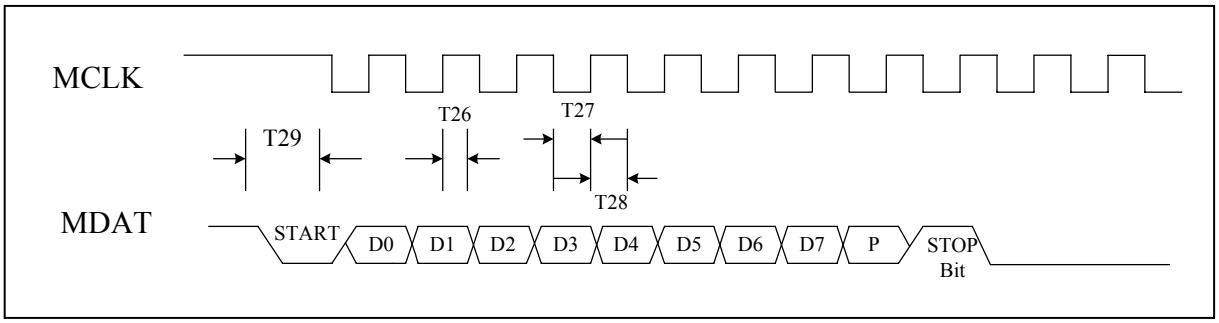
18.3.10.5 Input Clock



18.3.10.6 Send Data to Mouse



18.3.10.7 Receive Data from Mouse

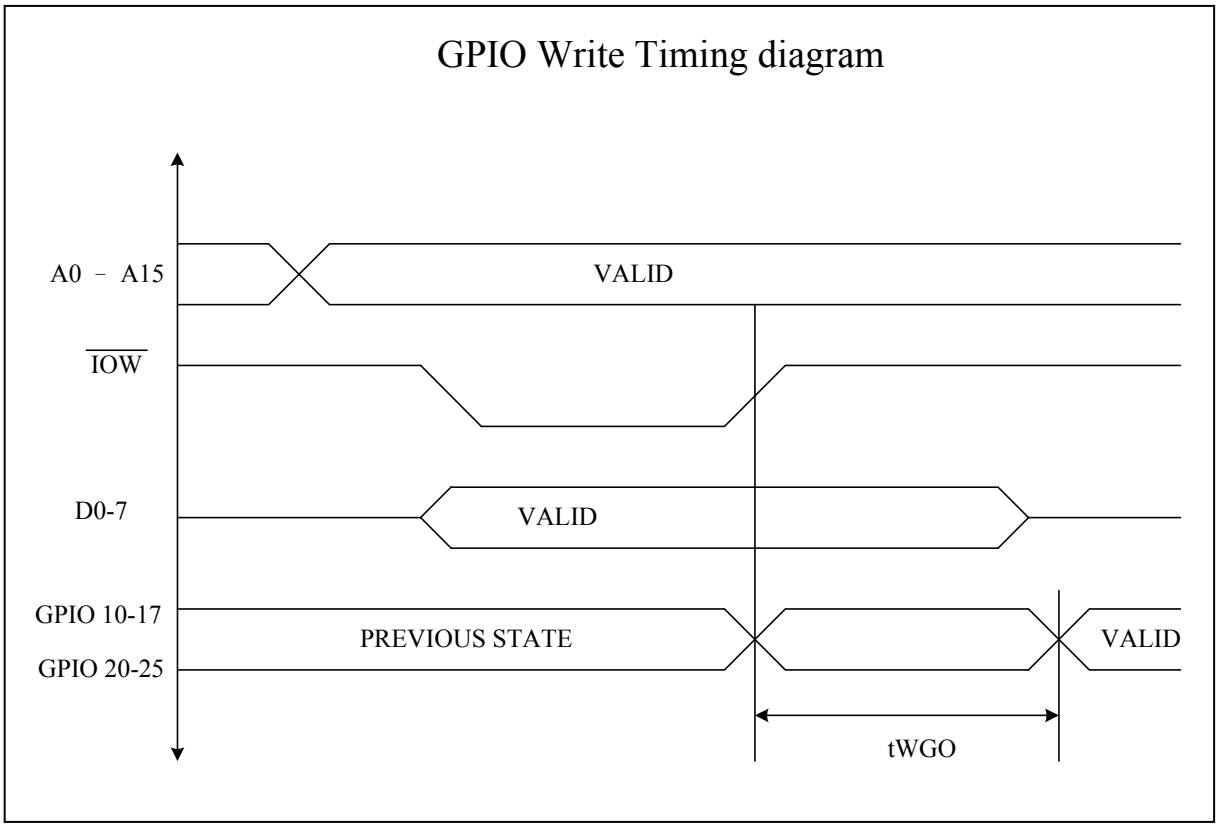


18.3.11 GPIO Timing Parameters

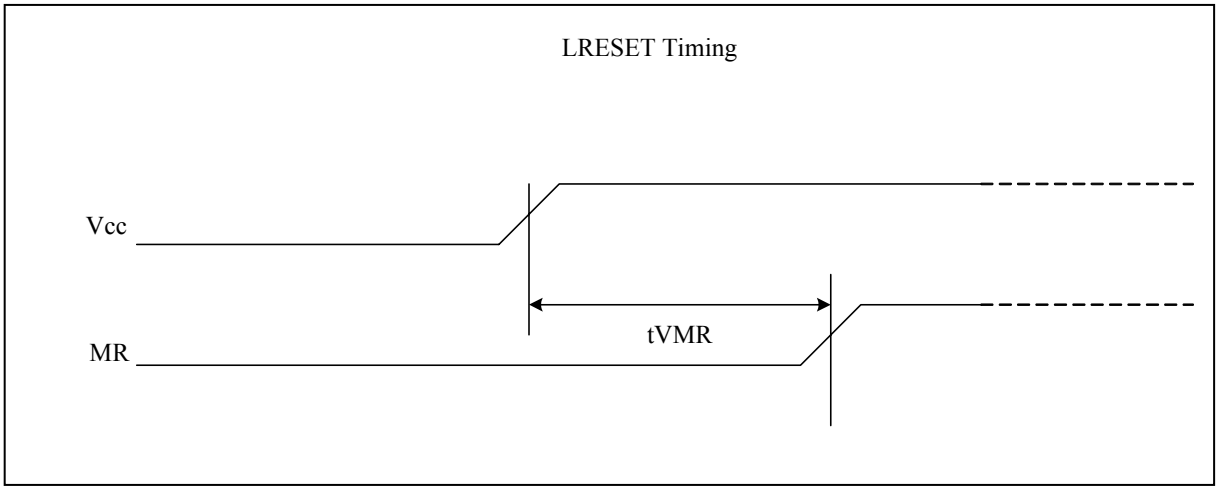
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{WGO}	Write data to GPIO update	-	300(Note 1)	ns
t_{SWP}	SWITCH pulse width	16	-	msec

Note: Refer to Microprocessor Interface Timing for Read Timing.

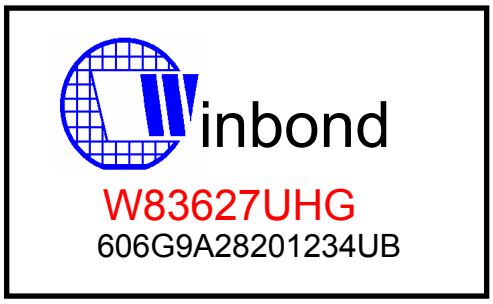
18.3.11.1 GPIO Write Timing



18.4 LRESET Timing



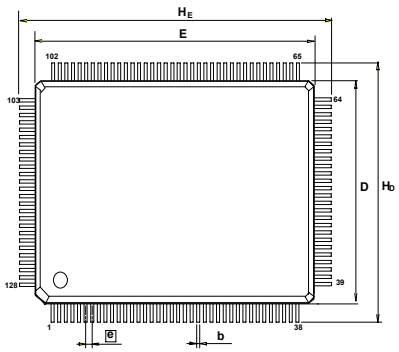
19. TOP MARKING SPECIFICATION

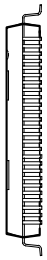


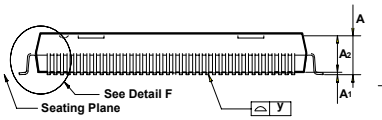
1st line: Winbond logo
2nd line: part number: W83627UHG (Pb-free package)
3rd line: tracking code 606G9A28201234UB

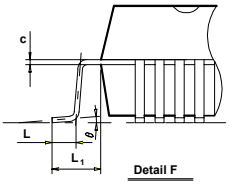
606: packages made in '06, week 06
G: assembly house ID; G means GR, A means ASE ... etc.
9: code version; 9 means code 009
A: IC revision; A means version A, B means version B
28201234: wafer production series lot number
UB: Winbond internal use.

20. PACKAGE SPECIFICATION









Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A_1	0.25	0.35	0.45	0.010	0.014	0.018
A_2	2.57	2.72	2.87	0.101	0.107	0.113
b	0.10	0.20	0.30	0.004	0.008	0.012
c	0.10	0.15	0.20	0.004	0.006	0.008
D	13.90	14.00	14.10	0.547	0.551	0.555
E	19.90	20.00	20.10	0.783	0.787	0.791
e	——	0.50	——	—	0.020	—
H_D	17.00	17.20	17.40	0.669	0.677	0.685
H_E	23.00	23.20	23.40	0.905	0.913	0.921
L	0.65	0.80	0.95	0.025	0.031	0.037
L_1	——	1.60	——	—	0.063	—
y	——	——	0.08	—	—	0.003
θ	0	——	7	0	—	7

Note:
1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion .
3. Controlling dimension : Millimeter
4. General appearance spec. should be based on final visual inspection spec.
5. PCB layout please use the "mm".

(128-pin (QFP)

APPENDIX – ABBREVIATIONS

A

ACLOSS – AC power failure

ACPI – Advanced Configuration and Power Interface

ADC – Analog Digital Converter

ASK-IR – Amplitude Shift Keyed IR

ATX – Advanced Technology Extended

B

BPP – Bi-directional Parallel Port

BIOS – Basic Input/Output System

C

CRC – Cyclic Redundancy Check

CLKSEL – Clock Select

CTS – Clear to Send

D

DCD – Data Carrier Detect

DMA – Direct Memory Access

DR Register – Data Rate Register

DSR – Data Set Ready

DTR – Data Terminal Ready

E

ECP – Extended Capabilities Port

EPP – Enhanced Parallel Port

F

FCS – Frame Check Sequence

FDC – Floppy Disk Controller

FDD – Floppy Disk Drive

FIFO – First-in First-out buffer

G

GPIO – General-purpose Input and Output

H

HM – Hardware Monitor

HSR – Handshake Status Register

I

I^2C – Inter-Integrated Circuit

INIT# – Initialization (PRT Port)

IOH – High Output Leakage

IOL – Low Output Leakage

IR – Infrared

IrDA – Infrared Data Association

IRQ – Interrupt

IRRX – Infrared Receiver

IRTX – Infrared Transmitter

ISA – Industry Standard Architecture

ISR – Interrupt Service Routine

K

KBRESET – Keyboard Reset

KCLK – Keyboard Clock

KDAT – Keyboard Data

KINT – Keyboard Interrupt

L

LAD – LPC Address and Data

LCLK – PCI Clock

LD – Logical Device

LDRQ# – LPC DMA Request

LFRAME# – LPC Frame

LPC – Low Pin Count

LRESET# – LPC Reset

LSB – Least Significant Bit (Byte)

M

MCLK – Mouse Clock

MDAT – Mouse Data

MIDI – Musical Instrument Digital Interface

MINT – Mouse Interrupt

MSB – Most Significant Bit (Byte)

O

OVT# – Over Temperature

P

PANSWIN# – Panel Switch Input

PANSWOUT# – Panel Switch Output

PC – Personal Computer

PCI SIG – Peripheral Component Interconnect Special Interest Group

PD – Parallel Port Data

PDRQ – Parallel Port DMA Request

PE – Paper End

PECI – Platform Environment Control Interface

PLED – Power LED

PME – Power Management Event

PnP – Plug and Play

PRT – Printer

PS/2 – IBM Personal System/2

PSIN_STS – PSIN# Status

PWM – Pulse Width Modulation

PWROK – Power OK

Q

QFP – Quad Flat Package

R

R/W – Read / Write

RI – Ring Indicator

RLE – Run Length Encoding/ Expanding

RPM – Revolutions per Minute

RSMRST# – Resume Reset

RTC – Real Time Clock

RTS – Request to Send

S

S/W Reset – Software Reset

SCL – Serial Clock

SDA – Serial Data

SERIRQ – Serialized IRQ

SLCT – Select Status

SLIN – Select Input

SMI# - System Management Interrupt

SPP – Standard Parallel Port

SST – Simple Serial Transport

SYSFANIN – System Fan Input

SYSTIN – System Temperature Input

T

Tcontrol: a temperature spec. based on a temperature from the thermal diode

TTL – Transistor-Transistor Logic

U

UART – Universal Asynchronous Receiver/ Transmitter

V

VSB – Standby Supply Voltage

VSS – GND

W

WDTO# – Watch Dog Timer Output

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