AvnetCore: Datasheet

Version 1.0, July 2006

UTOPIA Level 3 PHY

Intended Use:

- ATM Cell Processors
- PHY Processors
- ATM Bridges & Gaskets
- DSL ASSP interfaces
- UNI/MAC
- Microprocessor interfaces

Features:

- Function compatible with ATM Forum af-phy-0136.000
- Asynchronous/synchronous FIFO using RAM
- Up to 256 PHY ports supported
- 8/16/32 bit interfaces supported
- Direct and polled status
- Simple system side FIFO interface
- Flow control and polling integrated

Targeted Devices:

- Axcelerator® Family
- ProASIC®3 Family
- ProASIC PLUS® Family

Core Deliverables:

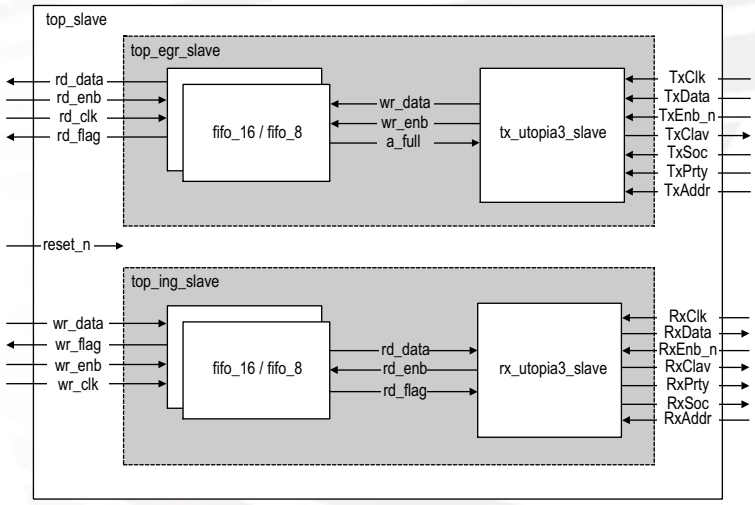
- Netlist Version
  - > Compiled RTL simulation model, compliant with the Actel Libero® environment
  - > Netlist compatible with the Actel Designer place and route tool
- RTL Version
  - > VHDL Source Code
- All
  - > User Guide
  - > Test Bench

Synthesis and Simulation Support:

- Synthesis: Synplicity®
- Simulation: Model*Sim*®
- Other tools supported upon request

Verification:

- Test Bench
- Test Vectors



Block Diagram

UTOPIA (Universal Test and Operations PHY Interface for ATM) Level 3 defines the interface between the ATM or LINK layer and a Physical Layer (PHY) device. The UTOPIA Level 3 standard defines a full duplex interface with a Master/Slave format. The Slave or LINK layer device responds to the requests from the PHY or Master device. The Master performs PHY arbitration and initiates data transfers to and from the Slave. The ATM forum has defined the UTOPIA Level 3 as either 8 or 32 bits in width, at up to 104 MHz, supporting an OC48 channel at 2.5 Gbps.

Actel CompanionCore

AVNET Memec

Functional Description

This core conforms to the appropriate standard(s). In general, standards do not define the internal user interface, only the external interfaces and protocols. Therefore, Avnet Memec has created a simple FIFO interface to this core for easy user connectivity. This document describes this Avnet Memec created interface. Please consult the appropriate standards document for all external signaling.

TOP_SLAVE

This is the top level of the core. Its only purpose is to serve as a container to instantiate the transmit & receive modules. TOP_SLAVE is also where the generics are located that configure the core. These parameters are then passed down to the TX & RX modules.

TOP_EGR_SLAVE & TOP_ING_SLAVE

These modules comprise the transmit and receive portions of the interface. They were developed so that they may be instantiated either separately in different FPGAs or together in one FPGA. They use the common sub-modules FIFO_16 & FIFO_8, for simplicity and reliability.

EGR_UTOPIA3_SLAVE

The Egress Slave is responsible for replying to polls from the master in order to receive cells from the master device.

ING_UTOPIA3_SLAVE

The Ingress Slave is responsible for responding to the master in order to send cells to the master device.

FIFO_16 / FIFO_8

The FIFO module contains one FIFO per PHY polled (i.e. this module is instantiated N = number of PHY ports times in each direction. The FIFOs are created by utilizing the available RAM resources in the FPGA. Additionally, two FIFO_16 modules (and hence 2x the RAMs) are instantiated to create a 32-bit wide FIFO for the 32-bit mode, however 2x the cells can be buffered. The FIFO may be operated in synchronous (same clock for read & write) and asynchronous (different clocks for read & write) systems.

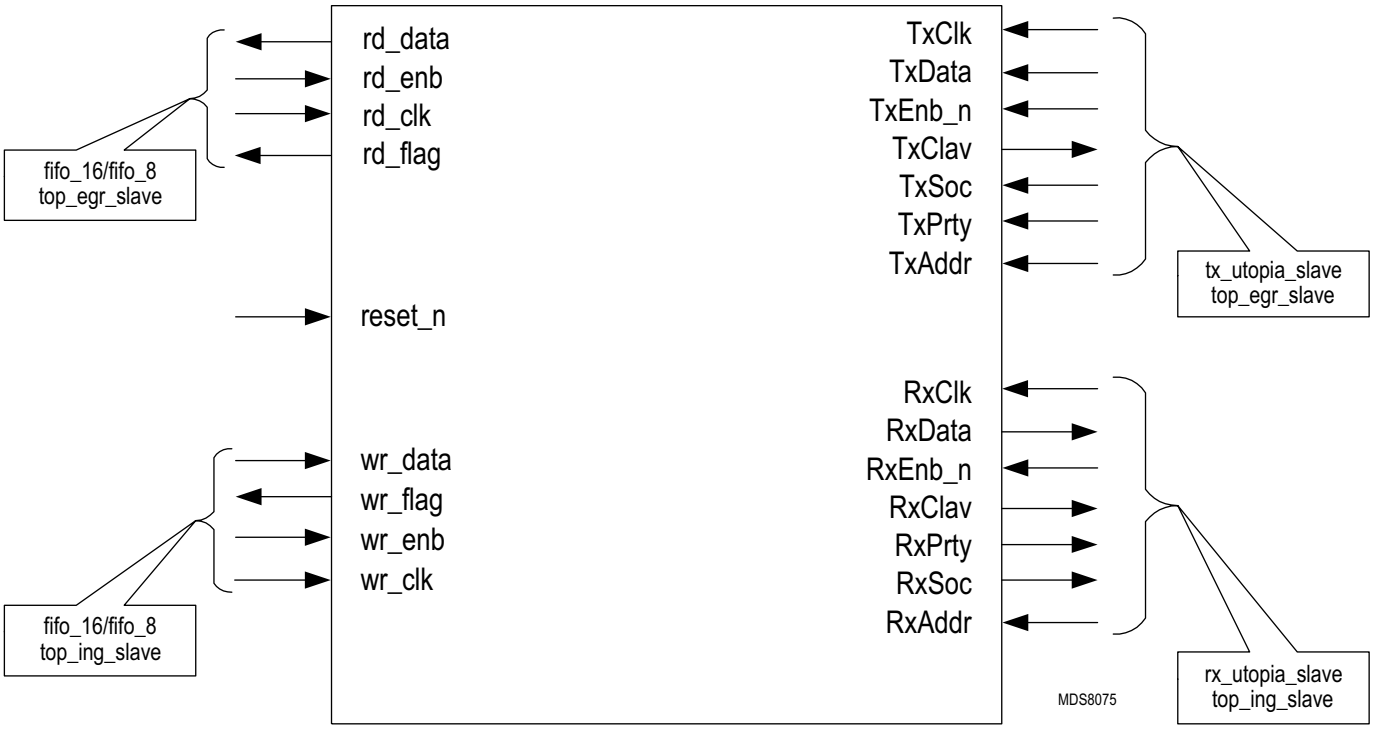


Figure 1: Logic Symbol

Device Requirements

Family	Device	Utilization			Performance
		COMB	SEQ	Tiles	
Axcelerator	AX250	38%	73%	n/a	131 MHz
ProASIC3	A3PE600	n/a	n/a	20%	81 MHz
ProASIC^{PLUS}	APA150	n/a	n/a	52%	80 MHz

Table 1: Device Utilization and Performance

Verification and Compliance

The testbench is self-checking, which means that if there is an error detected in the start word, end word, or payload the testbench will assert one or both of two error signals. The test checks for errors at two stages in the testbench: when the cells are looped back through the Slave device (SIG_LOOP_ERROR_OUT) and upon reading out of the Master device (SIG_ERROR_OUT).

Signal Descriptions

The following signal descriptions define the IO signals.

Signal	Width	Direction	Description
RD_DATA	8/16	Output	Read data bus for the FIFO
RD_ENB	1	Input	Read enable signal for the FIFO
RD_CLK	1	Input	Read clock for the FIFO
RD_FLAG	1	Output	FIFO packet available signal
RESET_N	1	Input	Reset signal from user logic
WR_DATA	8/16	Input	Write data bus for FIFO
WR_FLAG	1	Output	Write flag indicating if FIFO can accept another cell
WR_ENB	1	Input	Write enable signal for FIFO
WR_CLK	1	Input	System clock for all registers in this block
TXCLK	1	Input	100 MHz utopia clock
TXDATA	8/16/32	Input	Utopia data bus, 8, 16 or 32-bit selectable
TXENB_N	1	Input	Utopia enable signal used for throttle control
TXCLAV	$1 \leq N \leq 4$	Output	Utopia cell buffer available signal(s) used to indicate that the slave has room for a cell
TXSOC	1	Input	Utopia start of cell signal used to flag the first byte/word in the cell
TXPRTY	1	Input	Utopia parity signal used for odd parity on TXDATA
TXADDR	8	Input	Utopia address bus used for polling
RXCLK	1	Input	100 MHz utopia clock
RXDATA	8/16/32	Output	Utopia data bus, 8, 16 or 32-bit selectable
RXENB_N	1	Input	Utopia enable signal used for throttle control
RXCLAV	$1 \leq N \leq 4$	Output	Utopia cell buffer available signal(s) used to indicate that the slave has room for a cell
RXPRTY	1	Output	Utopia parity signal used for odd parity on TXDATA
RXSOC	1	Output	Utopia start of cell signal used to flag the first byte/word in the cell
RXADDR	8	Input	Utopia address bus used for polling

Table 2: Core I/O Signals

Timing

Since the ATM Forum specification fully defines the line side of the UTOPIA Level 3 interface, timing for that is not replicated here. Instead, only user (FIFO) interface timing information is presented here. The figure below shows the functional timing for FIFO reads and writes.

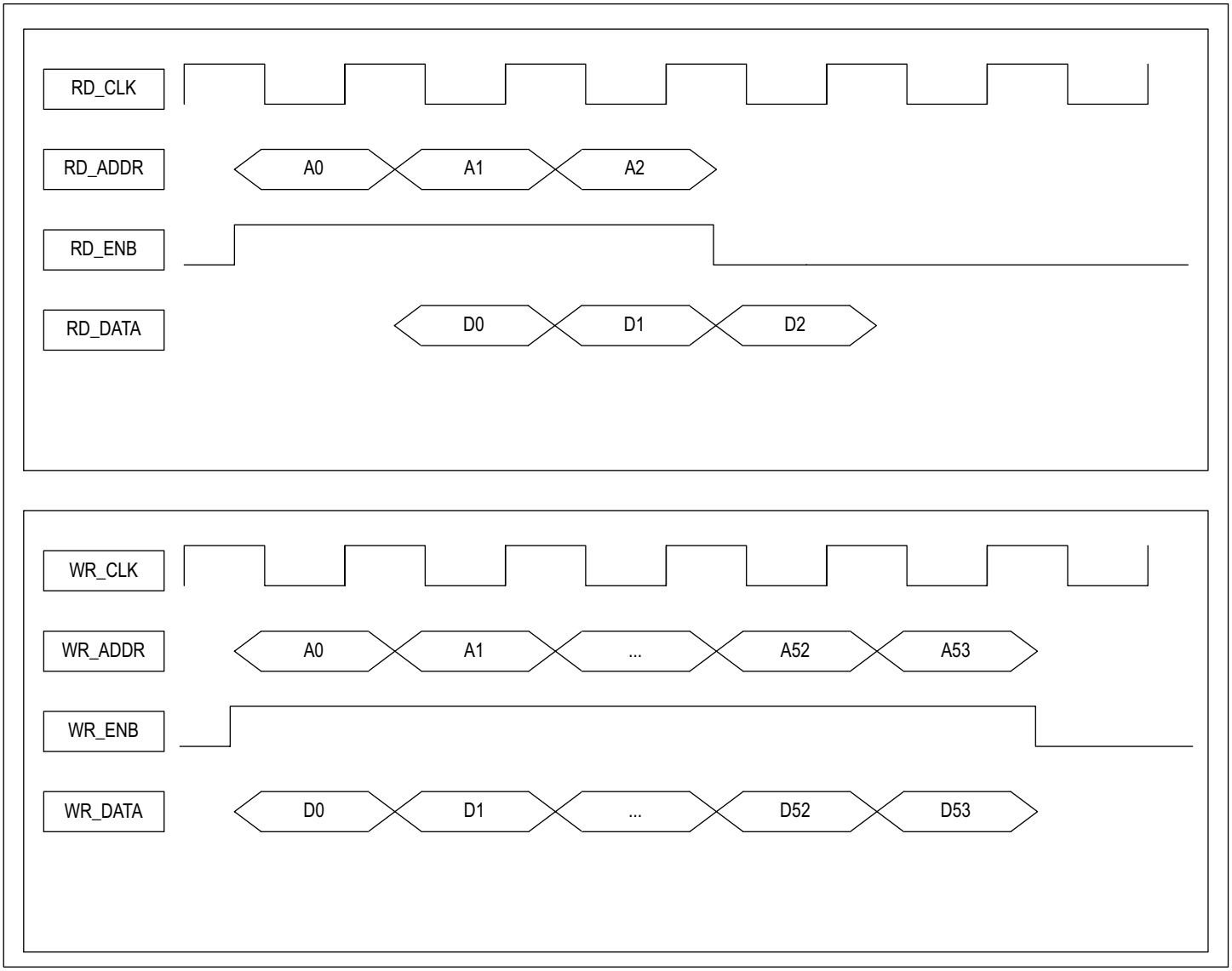


Figure 2: FIFO Timing

The top example shows where the last valid data word (LD) is clocked out relative to the deassertion of read enable. The bottom example shows read enable responding to the assertion of read empty.

Recommended Design Experience

For the source version, users should be familiar with HDL entry and Actel design flows. Users should be familiar with Actel Libero Integrated Design Environment (IDE) and preferably with Synplify and Model*Sim*.

Ordering Information

The CORE is provided under license from Avnet Memec for use in Actel programmable logic devices. Please contact Avnet Memec for pricing and more information.

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Ordering Information:

Part Number	Hardware	Resale
MC-ACT-HDLC-NET	Actel HDLC Controller Netlist	Contact for pricing
MC-ACT-HDLC-VLOG	Actel HDLC Controller Verilog	Contact for pricing
MC-ACT-HDLC-VHDL	Actel HDLC Controller VHDL	Contact for pricing

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