PDI1284P11

3.3 V parallel interface transceiver/buffer

Rev. 03 — 25 August 2008 Product data sheet

1. General description

The PDI1284P11 parallel interface chip is designed to provide an asynchronous, 8-bit, bidirectional, parallel interface for personal computers. The PDI1284P11 includes all 19 signal lines defined by the IEEE 1284 interface specification for Byte, Nibble, EPP, and ECP modes. The PDI1284P11 is designed for hosts or peripherals operating at 3.3 V to interface 3.3 V or 5.0 V devices.

The eight transceiver pairs (A/B 1 to 8) allow data transmission from the A-bus to the B-bus, or from the B-bus to the A-bus, depending on the state of the direction pin DIR.

The B-bus and the Y9 to Y13 lines have either totem pole or resistor pull-up outputs, depending on the state of the high drive enable pin HD. The A-bus has only totem pole style outputs. All inputs are TTL compatible with at least 400 mV of input hysteresis at V_{CC} = 3.3 V.

2. Features

- Asynchronous operation
- 8-bit transceivers
- Six additional buffer/driver lines peripheral to cable
- Five additional control lines from cable
- 5 V tolerant
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Latch-up current protection exceeds 500 mA per JEDEC Std 19
- Input hysteresis
- Low-noise operation
- IEEE 1284 compliant level 1 and 2
- Overvoltage protection on B/Y side for off-state
- A side 3-state option
- B side active or resistive pull-up option
- Cable side supply voltage for 5 V or 3 V operation

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
PDI1284P11DL	0 °C to 70 °C	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1
PDI1284P11DGG	0 °C to 70 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1

4. Functional diagram

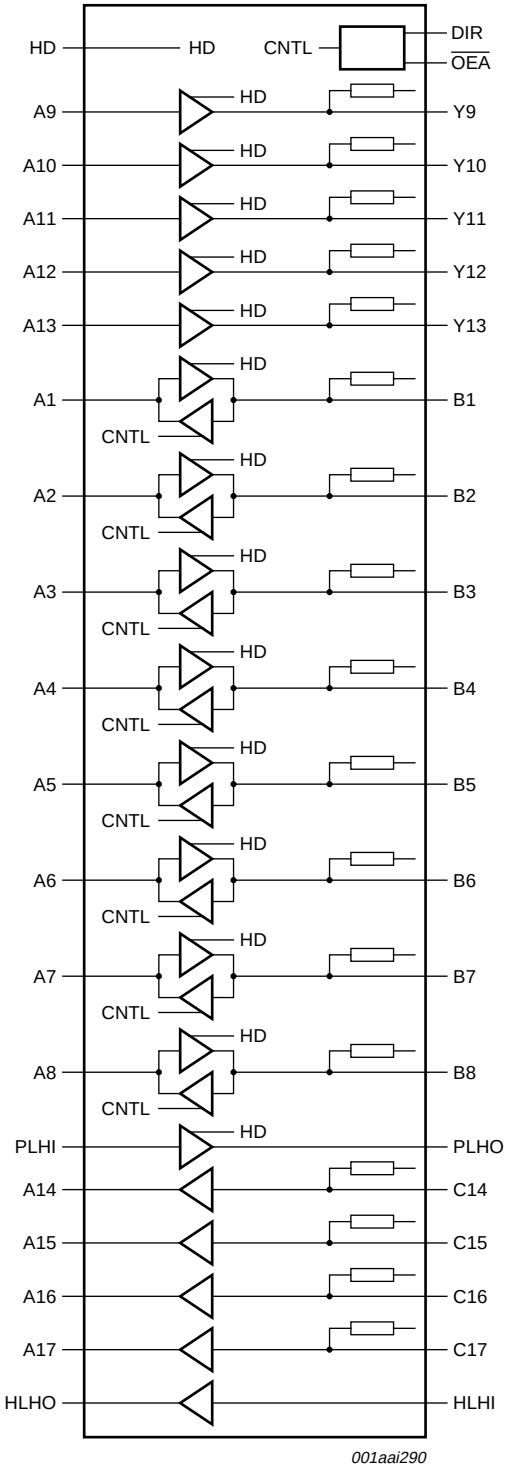


Fig 1. Logic symbol

5. Pinning information

5.1 Pinning

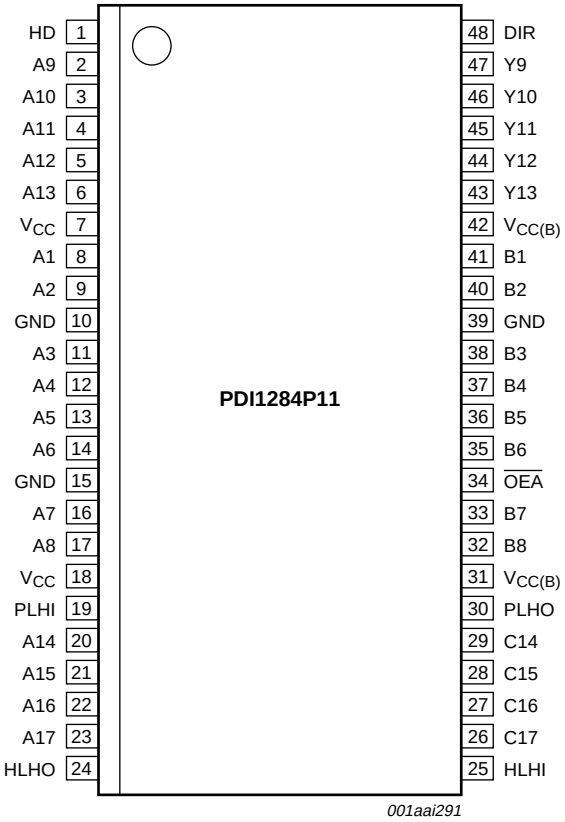


Fig 2. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
HD	1	high drive enable/disable input
A1 to A8	8, 9, 11, 12, 13, 14, 16, 17	data input/output
B1 to B8	41, 40, 38, 37, 36, 35, 33, 32	IEEE 1284 standard output/input[1]
A9 to A13	2, 3, 4, 5, 6	data input
Y9 to Y13	47, 46, 45, 44, 43	IEEE 1284 standard output[1]
C14 to C17	29, 28, 27, 26	control input (cable)[1]
A14 to A17	20, 21, 22, 23	control output (peripheral)
V_{CC}	7, 18	supply voltage
GND	10, 15, 39	ground (0 V)
PLHI	19	peripheral logic high input (peripheral)

Table 2. Pin description *...continued*

Symbol	Pin	Description
HLHO	24	host logic high output (cable)
HLHI	25	host logic high input (cable)
PLHO	30	peripheral logic high output (cable)
$V_{CC(B)}$	31, 42	supply voltage B (cable side 3 V/5 V)
$\overline{OEA}$	34	A side output enable input (active LOW)
DIR	48	direction selection input

[1] Pin with pull-up resistor to load cable.

6. Functional description

6.1 Function selection

Table 3. Function table[1]

DIR	$\overline{OEA}$	HD	Input	Output	Output type
X	X	X	C14 to C17	A14 to A17	TP
X	X	X	HLHI	HLHO	TP
X	X	L	A9 to A13	Y9 to Y13	RP
X	X	H	A9 to A13	Y9 to Y13	TP
X	X	L	PLHI	PLHO	OC
X	X	H	PLHI	PLHO	TP
H	X	L	A1 to A8	B1 to B8	RP
H	X	H	A1 to A8	B1 to B8	TP
L	L	X	B1 to B8	A1 to A8	TP
L	H	X	-	A1 to A8	Z[2]
L	H	X	B1 to B8	-	RP[2]

[1] An = side driving internal IC;
Bn = side driving external cable (bidirectional);
Cn = side receiving control signals from external cable;
H = HIGH voltage level;
L = LOW voltage level;
OC = Open Collector;
X = don't care (control signals in);
Yn = side driving external cable (unidirectional);
Z = high impedance (high-Z) or 3-state;
TP = totem pole output;
RP = resistive pull-up: 1.4 kΩ (nominal) on B/Y/C cable side and V_{CC}. However, while a B/Y side output is LOW as driven by a LOW signal on the A side, that particular B/Y side resistor is switched off to stop current drain from V_{CC} through it.

[2] When DIR = L and $\overline{OEA}$ = H, the output signal is isolated from the input signal. Signals B1 to B8 maintain a resistive pull-up of 1.4 kΩ on the input for this mode.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage	pins V_{CC}		–0.5	+4.6	V
$V_{CC(B)}$	supply voltage B	pins $V_{CC(B)}$; cable side 3 V/5 V		–0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V		-	±20	mA
I_{OK}	output clamping current	$V_O < 0$ V		-	±50	mA
V_I	input voltage		[2]	–0.5	+5.5	V
V_O	output voltage	B/Y side	[2]	–0.5	+5.5	V
		A side		–0.5	V_{CC} + 0.5	V
V_{trt}	transient voltage	B/Y side; 40 ns transient	[3]	–2	+7	V
I_{CC}	supply current			-	200	mA
I_{GND}	ground current			–200	-	mA
I_O	output current	output HIGH or LOW		-	±50	mA
T_{stg}	storage temperature			–60	+150	°C
P_{tot}	total power dissipation	T_{amb} = 0 °C to +70 °C	[4]	-	500	mW

[1] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

[2] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[3] V_{trt} guarantees only that the PDI1284P11 will not be damaged by reflections in application so long as the voltage levels remain in the specified range.

[4] Above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	pins V_{CC}	3.0	3.6	V
$V_{CC(B)}$	supply voltage B	pins $V_{CC(B)}$; cable side 3 V/5 V	3.0	5.5	V
V_{IH}	HIGH-level input voltage		2.0	-	V
V_{IL}	LOW-level input voltage		-	0.8	V
V_O	output voltage	pins Bn, Yn	–0.5	+5.5	V
		pins An	0	V_{CC}	V
I_{OH}	HIGH-level output current	pins Bn, Yn	-	–14	mA
I_{OL}	LOW-level output current	pins Bn, Yn	-	14	mA
T_{amb}	ambient temperature	free-air	0	70	°C

9. Static characteristics

Table 6. Static characteristics

T_{amb} = 0 °C to 70 °C; ground = 0 V; unless specified otherwise.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IL}	LOW-level input voltage	An, Bn, Cn and PLHI inputs; V_{CC} = 3.0 V to 3.6 V		-	-	0.8	V
		HLHI input; V_{CC} = 3.0 V		-	-	1.55	V
V_{IH}	HIGH-level input voltage	An, Bn, PLHI inputs; V_{CC} = 3.0 V to 3.6 V		2.0	-	-	V
		Cn inputs; V_{CC} = 3.0 V to 3.6 V		2.3	-	-	V
		HLHI input; V_{CC} = 3.6 V		2.6	-	-	V
V_H	hysteresis voltage	An, Bn inputs; V_{CC} = 3.3 V; V_{IL} = 0.8 V; V_{IH} = 2.0 V	[1]	0.4	0.47	-	V
		Cn inputs; V_{CC} = 3.3 V	[1]	0.8	0.47	-	V
V_{OL}	LOW-level output voltage	pins An, HLHO; I_{OL} = 50 µA; V_{CC} = 3.0 V		-	-	0.2	V
		pins An, HLHO; I_{OL} = 4 mA; V_{CC} = 3.0 V		-	-	0.4	V
		pins Bn, Yn; I_{OL} = 14 mA; V_{CC} = 3.0 V		-	-	0.77	V
		pin PLHO; I_{OL} = 500 µA; V_{CC} = 3.0 V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	pins An, HLHO; I_{OH} = –500 µA; V_{CC} = 3.0 V		2.8	-	-	V
		pins An, HLHO; I_{OH} = –4 mA; V_{CC} = 3.0 V		2.4	-	-	V
		pins Bn, Yn; I_{OH} = –14 mA; V_{CC} = 3.0 V		2.23	-	-	V
		pin PLHO; I_{OH} = 500 µA; V_{CC} = 3.15 V		3.1	-	-	V
I_{CC}	supply current	V_I = 0 V or V_{CC}; I_O = 0 A	[1]	-	5	-	µA
		pins V_{CC} and $V_{CC(B)}$; V_{CC} = 3.6 V; $V_{CC(B)}$ = 3.6 V to 5.5 V; V_I = 0 V or V_{CC}; pins Bn = $V_{CC(B)}$; pins Cn = $V_{CC(B)}$ or floating		-	0.1	100	µA
		pins $V_{CC(B)}$; V_{CC} = 3.6 V; V_I = 0 V or V_{CC}; pins Cn = 0 V	[2]				
		pin DIR = 3.6 V; $V_{CC(B)}$ = 3.6 V		-	10	15	mA
		pin DIR = 3.6 V; $V_{CC(B)}$ = 5.5 V		-	16	20	mA
		pin DIR = 0 V; $V_{CC(B)}$ = 3.6 V; pins Bn = 0 V		-	30	40	mA
		pin DIR = 0 V; $V_{CC(B)}$ = 5.5 V; pins Bn = 0 V		-	47	60	mA
I_{OFF}	power-off leakage current	pins Bn, Cn, Yn; V_O = 5.5 V; V_{CC} = 0 V					
		$V_{CC(B)}$ = 0 V		-	-	±100	µA
		$V_{CC(B)}$ = 4.5 V		-	-	±100	µA
I_I	input leakage current	V_I = 0 V to V_{CC}	[3]	-	-	±1	µA
I_{OZ}	OFF-state output current	3-state; V_O = V_{CC} or 0 V	[3]	-	-	±20	µA
R_o	output resistance	V_{CC} = 3.3 V; see Figure 9					
		V_O = 1.65 V ± 0.1 V; B/Y side	[1]	35	45	55	Ω
R_{PU}	pull-up resistance	B/Y side; V_{CC} = 3.3 V; output in high-Z with resistive pull-up	[1]	1.15	1.4	1.65	kΩ

[1] Typical values at T_{amb} = 25 °C.

[2] Includes extra $I_{CC(B)}$ current from pull-up resistors, i.e. $I_{CC(B)}$ = (total number of LOW inputs on B and C sides) × ($V_{CC(B)}$ / R_{PU}).

[3] The pull-up resistor on the B side outputs makes it impossible to test I_{OZ} on the B side. This applies to the input current on the C side inputs as well.

10. Dynamic characteristics

Table 7. Dynamic characteristics

V_{CC} = 3.0 V to 3.6 V; ground = 0 V; C_L = 50 pF; R_L = 500 Ω; T_{amb} = 0 °C to 70 °C; unless specified otherwise.

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
t_{PLH}	LOW to HIGH propagation delay	An to Bn or Yn; see Figure 3 and 8		0	12.5	20	ns
t_{PHL}	HIGH to LOW propagation delay	An to Bn or Yn; see Figure 3 and 8		0	13.9	23	ns
t_{pd}	propagation delay	see Figure 4 and 8	[1]				
		Bn to An		0	-	12	ns
		Cn to An		-	-	15	ns
		PLHI to PLHO		-	-	20	ns
		HLHI to HLHO		-	-	15	ns
SR	slew rate	Bn/Yn; R_L = 62 Ω; see Figure 5 and 8		0.05	0.2	0.4	V/ns
t_{dis}	disable time	HD to Yn or Bn; see Figure 6 and 8	[3]	-	-	20	ns
		HD to PLHO; see Figure 6 and 7	[3]	-	-	20	ns
		R_L = 250 Ω; see Figure 6 and 7	[3]				
		DIR to Bn; TP load on B/Y side		-	-	50	ns
		DIR to An		-	-	15	ns
		$\overline{OEA}$ to An		-	-	6	ns
t_{en}	enable time	HD to Yn or Bn; see Figure 6 and 7	[4]	-	-	20	ns
		HD to PLHO; see Figure 6 and 7	[4]	-	-	20	ns
		R_L = 250 Ω; see Figure 6 and 7	[4]				
		DIR to Bn; TP load on B/Y side		-	-	30	ns
		DIR to An		-	-	50	ns
		$\overline{OEA}$ to An		-	-	12	ns
Δt_{PD}	propagation delay difference	$t_{PZH} - t_{PHZ}$; HD to output		-	-	10	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] Value at T_{amb} = 25 °C and V_{CC} = 3.3 V.

[3] t_{dis} is the same as t_{PHZ} and t_{PLZ}.

[4] t_{en} is the same as t_{PZH} and t_{PZL}.

11. Waveforms

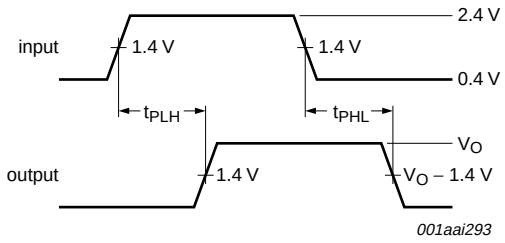
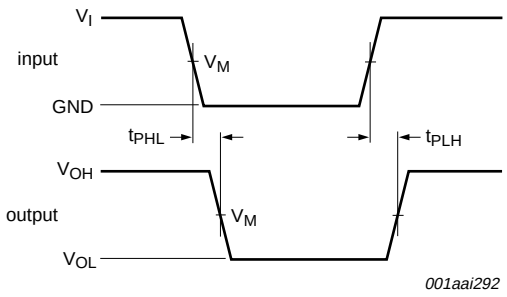


Fig 3. Input An to output Bn or Yn propagation delays

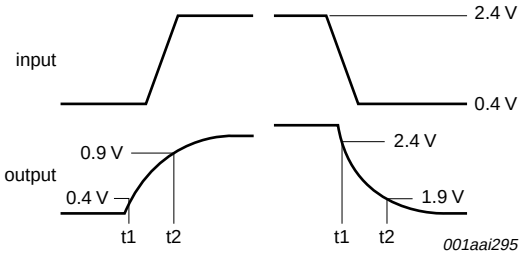


V_M = 1.5 V.

V_{CC} never goes below 3.0 V.

V_{OL} and V_{OH} are the typical voltage output levels that occur with the output load.

Fig 4. Input Bn, Cn to output An propagation delays



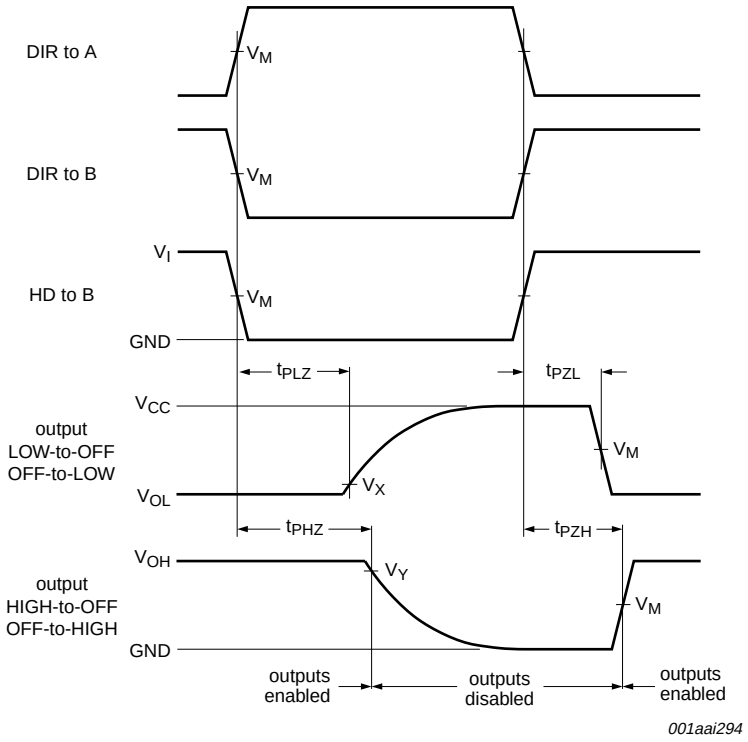
Measurement data is given in Table 8.

SR is measured for both a LOW-to-HIGH and a HIGH-to-LOW transition.

Fig 5. Slew rate on B/Y side

Table 8. Slew rate measurements

t_r	t_f	t_W	R_L	V_O transition (see Figure 8)	
				Rising	Falling
3 ns	3 ns	150 ns < t_W < 10 µs	62 Ω	from V_O = 0.4 V to V_O = 0.9 V	from V_O = 2.4 V to V_O = 1.9 V

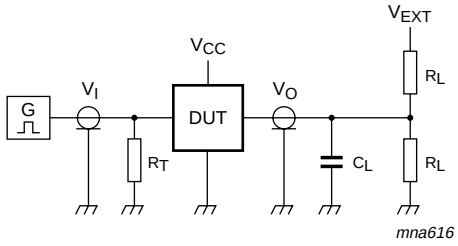


Test circuit is shown in Figure 7.

Measurement points are given in Table 9.

V_{OL} and V_{OH} are the typical voltage output levels that occur with the output load.

Fig 6. Enable and disable times

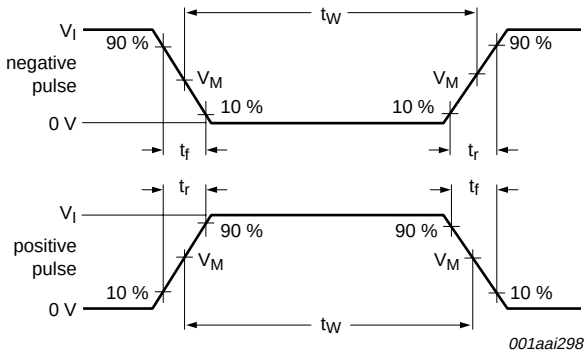


Test conditions are given in Table 9.

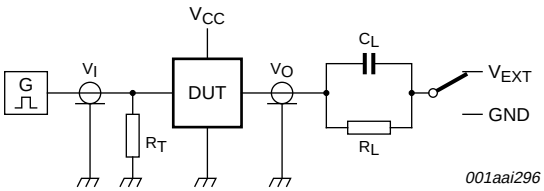
Fig 7. Test circuit for measuring enable and disable times

Table 9. Test data for test circuit measuring enable disable times Bn to An

Parameter	V_{CC}	Input		Output			V_{EXT}	
		V_I	V_M	V_M	V_X	V_Y	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
DIR to Bn, An; $\overline{OEA}$ to An	< 2.7 V	V_{CC}	1.5 V	1.5 V	V_{OL} ± 0.3 V	V_{OH} – 0.3 V	GND	$2V_{CC}$
	2.7 V to 3.6 V	2.7 V	1.5 V	1.5 V	V_{OL} ± 0.3 V	V_{OH} – 0.3 V	GND	$2V_{CC}$
HD to Yn or Bn; HD to PHLO	< 2.7 V	V_{CC}	1.5 V	1.5 V	-	V_{OH} – 0.3 V	open	-
	2.7 V to 3.6 V	2.7 V	1.5 V	1.5 V	-	V_{OH} – 0.3 V	open	-



a. Input pulse definition



b. Test circuit

C_L = load capacitance includes jig and probe capacitance.

R_L = load resistance.

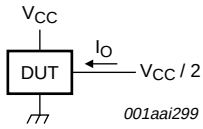
R_T = termination resistance should be equal to the output impedance of the pulse generator.

Test conditions for propagation delays are given in Table 10, test conditions for slew rate are given in Table 8

Fig 8. Test circuit for An, Bn and Yn outputs; slew rate B/Y side

Table 10. Test conditions for An, Bn and Yn outputs

Output	V_I	V_M	Repetition rate	t_W	t_r	t_f	Switch position	
							t_{PLH}, t_{PZH}	t_{PHL}, t_{PHZ}
An	3.0 V	1.5 V	1 MHz	500 ns	3 ns	3 ns	GND	GND
Bn, Yn	3.0 V	1.5 V	1 MHz	500 ns	3 ns	3 ns	GND	V_{EXT} = 2.8 V

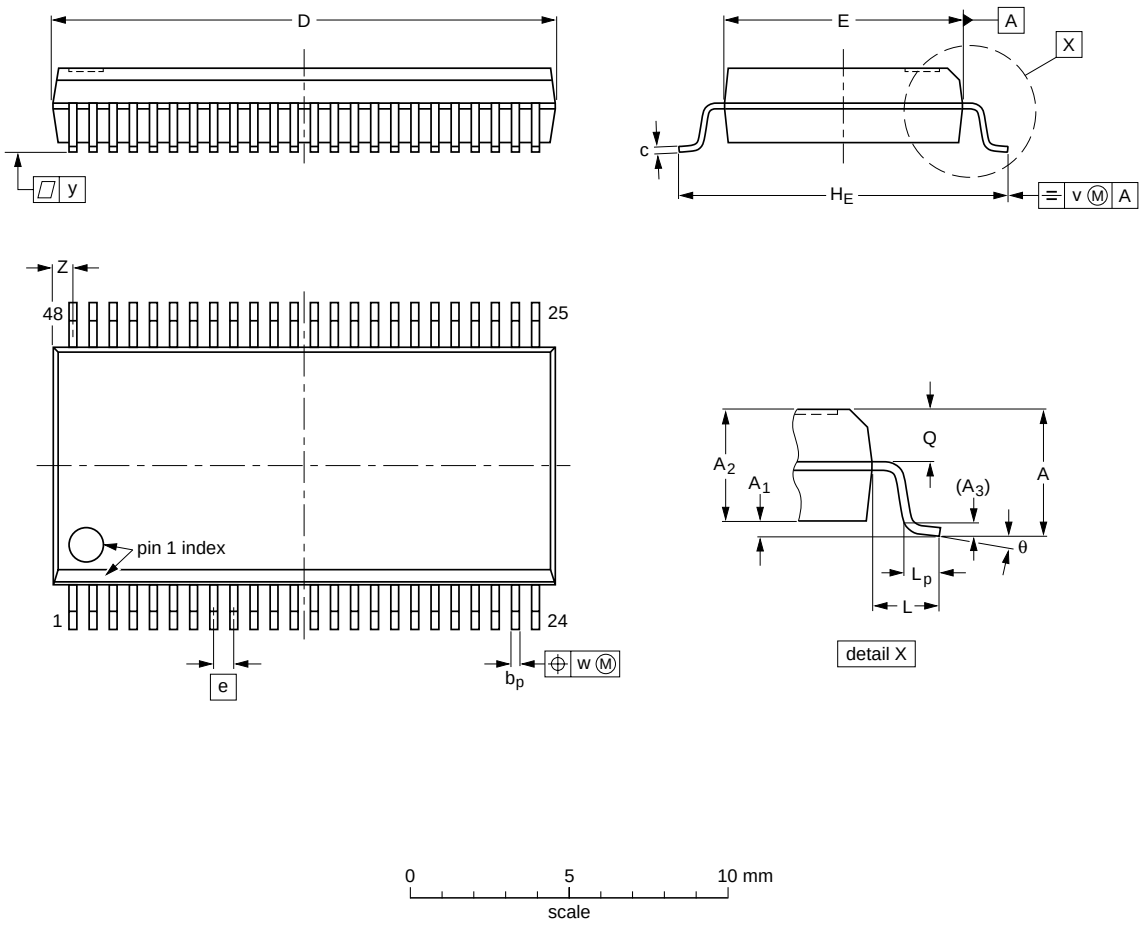


I_O is measured by forcing $0.5V_{CC}$ on the output. The output impedance can then be calculated as $R_o = 0.5V_{CC} / |I_O|$.

Fig 9. Output impedance

12. Package outline

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm **SOT370-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8^o 0^o

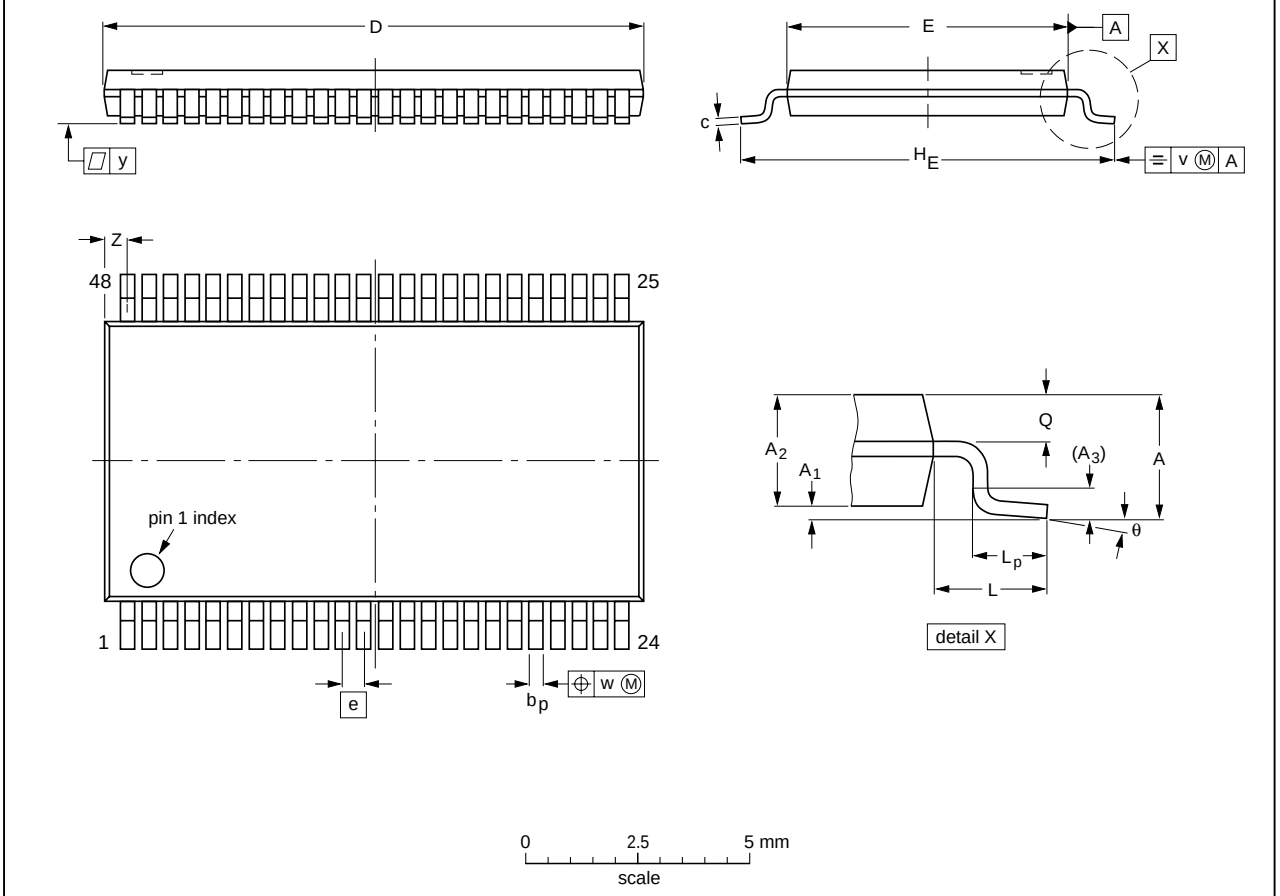
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT370-1		MO-118				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT370-1 (SSOP48)

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT362-1 (TSSOP48)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ECP	Extended Capability Port
EPP	Enhanced Parallel Port
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PDI1284P11_3	20080825	Product data sheet	-	PDI1284P11_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Quick reference table removed. • Table 7, t_{PHL}: Maximum value of 20 ns replaced by 23 ns. • Table 11: Abbreviations list added.			
PDI1284P11_2	19990917	Product specification	-	PDI1284P11_1
PDI1284P11_1	19970915	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

15.2 Definitions

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17. Contents

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Date of release: 25 August 2008
Document identifier: PDI1284P11_3