Emerging Memory & Logic Solutions Inc.

Document Title

1M x 16Bit Multiplexed Single Transistor RAM

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial Draft	Jan. 1 , 2005	Preliminary

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1M x16 Bit Multiplexed Single Transistor RAM

FEATURES

- Process Technology : 0.13μm CMOS process
- Organization :1M x16
- Power Supply Voltage : 1.7~1.9V
- Multiplexed address and data bus
- Three state outputs
- RMS and Auto TCSR for power saving

GENERAL WAFER SPECIFICATIONS

- Deep trench process
- 3 Metal layers including local inter-connection
- Typical Pad Size : 73.0um x 70.0um
- Wafer diameter : 8-inch

PAD DESCRIPTION

Name	Function	Name	Function
/CS	Chip select inputs	/LB	Lower byte ($ADQ_{0~7}$)
/OE	Output enable input	/UB	Upper byte ($ADQ_{8~15}$)
/WE	Write enable input	VCC	Power supply
/AVD	Address valid input	VCCQ	I/O Power supply
ADQ_i	Address/Data In-out	VSS(Q)	Ground
A_i	Address inputs	NC	No connection

FUNCTION BLOCK DIAGRAM

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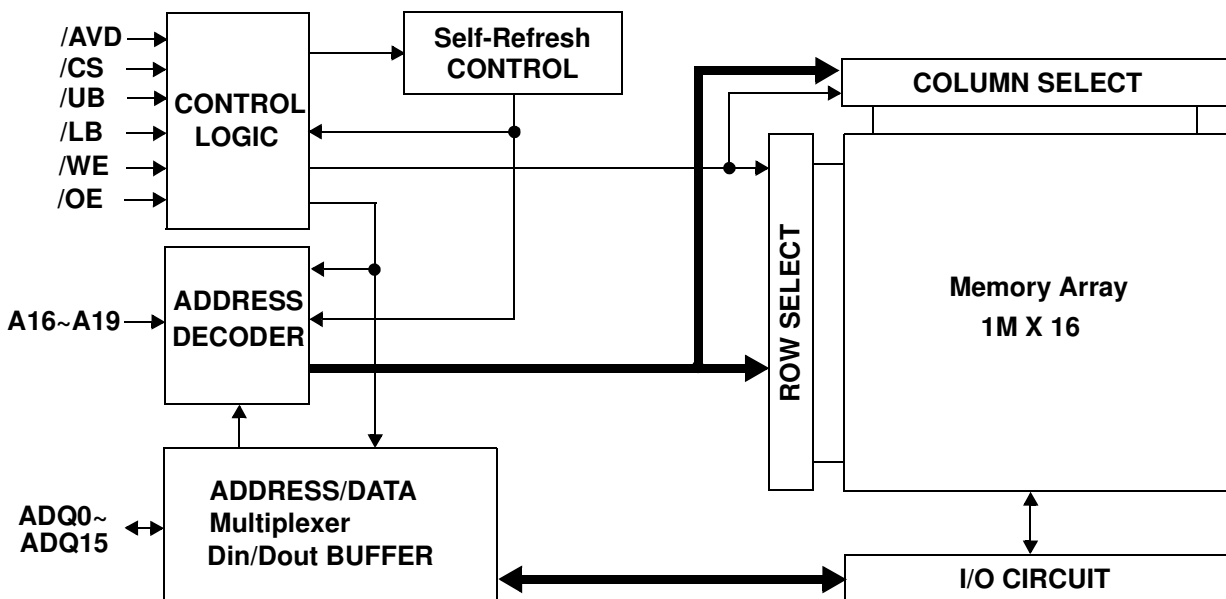
ABSOLUTE MAXIMUM RATINGS [1)]

Parameter	Symbol	Minimum	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.2 to V_{CCQ}+0.3V	V
Voltage on Vcc supply relative to Vss	V_{CC}, V_{CCQ}	-0.2[2)] to 2.5V	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_A	-25 to 85	°C

1. Stresses greater than those listed above "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Undershoot at power-off : -1.0V in case of pulse width ≤ 20ns

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	$\overline{AVD}$	$ADQ_{0\sim15}$	$A_{16}\sim A_{19}$	Mode	Power
H	X	X	X	X	X	High-Z	X	Deselected	Stand by
L	H	H	X	X	H	High-Z	X	Output Disabled	Active
L	X	X	H	H	X	High-Z	X	Output Disabled	Active
L	H	L	H	H	H	Data In	X	Configuration Register Write Access	Active
L	L	H	H	H	H	Data Out	X	Configuration Register Read Access	Active
L	H	H	H	H	L	Add. Input	Add. Input	Address Input	Active
L	L	H	L	H	H	Data Out	X	Lower Byte Read	Active
L	L	H	H	L	H	Data Out	X	Upper Byte Read	Active
L	L	H	L	L	H	Data Out	X	Word Read	Active
L	H	L	L	H	H	Data In	X	Lower Byte Write	Active
L	H	L	H	L	H	Data In	X	Upper Byte Write	Active
L	H	L	L	L	H	Data In	X	Word Write	Active

Note: X means don't care. (Must be low or high state)

RECOMMENDED DC OPERATING CONDITIONS [1]

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	1.7	1.8	1.9	V
	V_{CCQ}	1.7	1.8	1.9	V
Ground	V_{SS}, V_{SSQ}	0	0	0	V
Input high voltage	V_{IH}	V_{CCQ} - 0.4	-	V_{CCQ} + 0.2 [2]	V
Input low voltage	V_{IL}	-0.2 [3]	-	0.4	V

1. T_A= -25 to 85°C, otherwise specified
2. Overshoot: V_{CC} +1.0 V in case of pulse width $\leq$ 20ns
3. Undershoot: -1.0 V in case of pulse width $\leq$ 20ns
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE [1] (f =1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Ouput capacitance	C_{IO}	V_{IO}=0V	-	10	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

| Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input leakage current	I_{LI}	V_{IN}=V_{SS} to V_{CCQ} , V_{CC}=V_{CCmax}		-1	-	1	uA
Output leakage current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} , V_{IO}=V_{SS} to V_{CCQ} , V_{CC}=V_{CCmax}		-1	-	1	uA
Average operating current	I_{CC1}	Cycle time=1μs, 100% duty, I_{IO}=0mA, $\overline{CS}\leq$0.2V, $V_{IN}\leq$0.2V or $V_{IN}\geq V_{CCQ}$-0.2V		-	-	3	mA
	I_{CC2}	Cycle time = Min, I_{IO}=0mA, 100% duty, $\overline{CS}$=V_{IL}, V_{IN}=V_{IL} or V_{IH}		-	-	25	mA
Output low voltage	V_{OL}	I_{OL} = 0.1mA, V_{CC}=V_{CCmin}		-	-	0.1	V
Output high voltage	V_{OH}	I_{OH} = -0.1mA, V_{CC}=V_{CCmin}		V_{CCQ}-0.1	-	-	V
Standby Current (CMOS)	I_{SB1}	$\overline{CS}\geq V_{CCQ}$-0.2V, Other inputs = 0 ~ V_{CCQ} (Typ. condition : V_{CC}=1.8V @ 25°C) (Max. condition : V_{CC}=1.9V @ 85°C)	LL	-	-	60	uA

1. Maximum Icc specifications are tested with V_{CC} = V_{CCmax}.

AC OPERATING CONDITIONS

Test Conditions (Test Load and Test Input/Output Reference)

Input Pulse Level : 0.2V to V_{CCQ}-0.2V
Input Rise and Fall Time : 5ns
Input and Output reference Voltage : $V_{CCQ}/2$

Output Load (See right) : $CL^{1)}$ = 30pF

1. Including scope and Jig capacitance

Dout

$CL^{1)}$
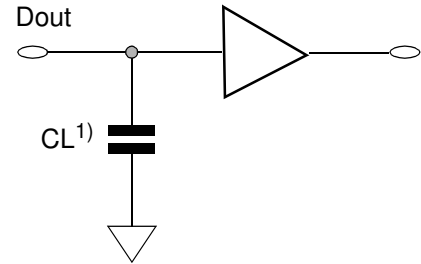
AC CHARACTERISTICS (V_{cc} = 1.7 to 1.9V, Gnd = 0V, T_A = -25C to +85°C)

Parameter List		Symbol	Speed		Unit
			Min	Max	
Common	$\overline{AVD}$ Low pulse	t_{AVD}	15	1000	ns
	Address setup to $\overline{AVD}$ rising edge	t_{AVDS}	15	-	ns
	Address hold from $\overline{AVD}$ rising edge	t_{AVDH}	5	-	ns
	Chip enable setup to $\overline{AVD}$ rising edge	t_{CSS}	7	-	ns
Read	$\overline{AVD}$ low to data valid time	t_{ACC1}	-	70	ns
	Address access time	t_{ACC2}	-	70	ns
	Chip enable to data output	t_{ACC3}	-	70	ns
	Address disable to output enable	t_{ADOE}	0	-	ns
	Output enable to valid output	t_{OE}	-	25	ns
	$\overline{UB}, \overline{LB}$ enable to data output	t_{UBLBA}	-	25	ns
	$\overline{UB}, \overline{LB}$ enable to low-Z output	t_{BLZ}	5	-	ns
	Output enable to low-Z output	t_{OLZ}	5	-	ns
	Chip disable to high-Z output	t_{HZ}	-	15	ns
	$\overline{UB}, \overline{LB}$ disable to high-Z output	t_{BHZ}	-	15	ns
	Output disable to high-Z output	t_{OHZ}	-	15	ns
Write	$\overline{AVD}$ low to end of write	t_{ACW1}	70	-	ns
	Address valid to end of write	t_{ACW2}	70	-	ns
	Chip enable to end of write	t_{ACW3}	70	-	ns
	Write pulse low	t_{WRL}	45	-	ns
	$\overline{UB}, \overline{LB}$ valid to end of write	t_{BW}	50	-	ns
	Data to write time overlap	t_{DW}	25	-	ns
	Data hold from write time	t_{DH}	0	-	ns

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Device Operaton

The access is performed in two stages. The first stage is address latching. The first stage take place between point A and B in timing diagram. At this stage, the Chip Select($\overline{CS}$) to the device is asserted. The random access is enabled either from the point the address becomes stable, the falling edge of the $\overline{AVD}$ signal or from the falling edge of the last chip select signal. The second stage is the read or write access. This takes place between points B and C in timing diagram. In case of a read access, the multiplexed address/data bus ($ADQ_0 \sim ADQ_{15}$) changes its direction. It is important to notice tOE when it is dominant that the device gets into the read cycle since the address is available long before the device output is enabled.
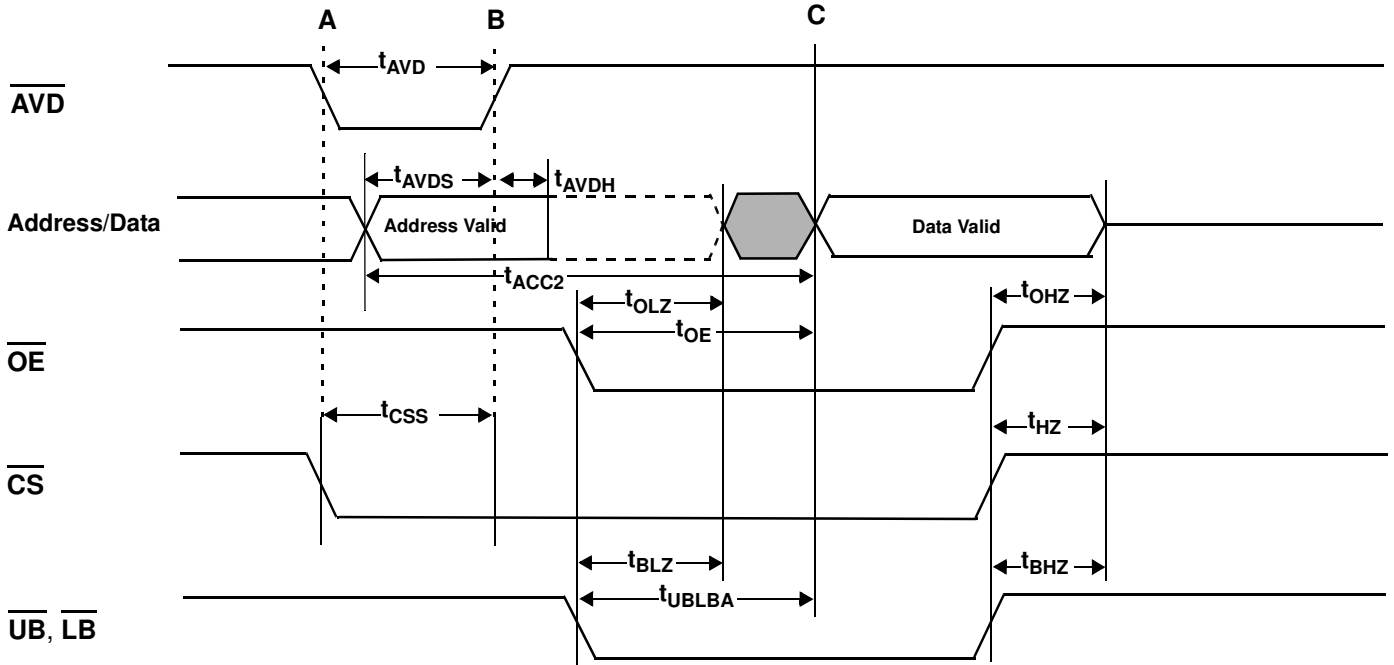
Read Access

The read access is initiated by applying the address to the multiplexed address/data bus or to the address bus over A_{15} ($A_{16} \rightarrow A_{xx}$). When the address is stable, the device chip select($\overline{CS}$) is set active low. At point A, the $\overline{AVD}$ signal is taken low and the latch becomes transparent. This allows the address to be propagated to the memory array. The address is stable at the rising edge of the $\overline{AVD}$ signal. The $\overline{AVD}$ signal goes high at point B in which the address latch is completed. At this point the read cycle is entered. The $\overline{OE}$ signal is set active low. This changes the direction of the bus. The status of control signals $\overline{UB}$ and $\overline{LB}$ are set according to the access. Data is read at point C.

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) ($\overline{WE}$ = V_{IH})
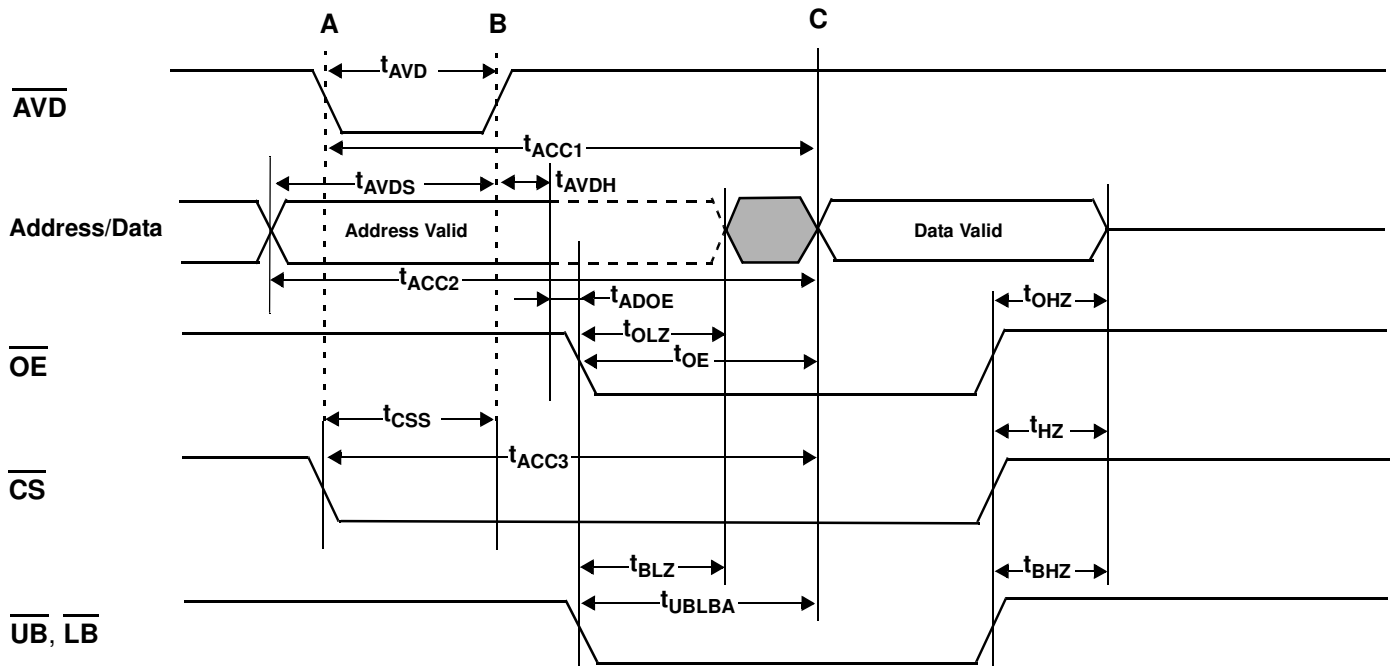
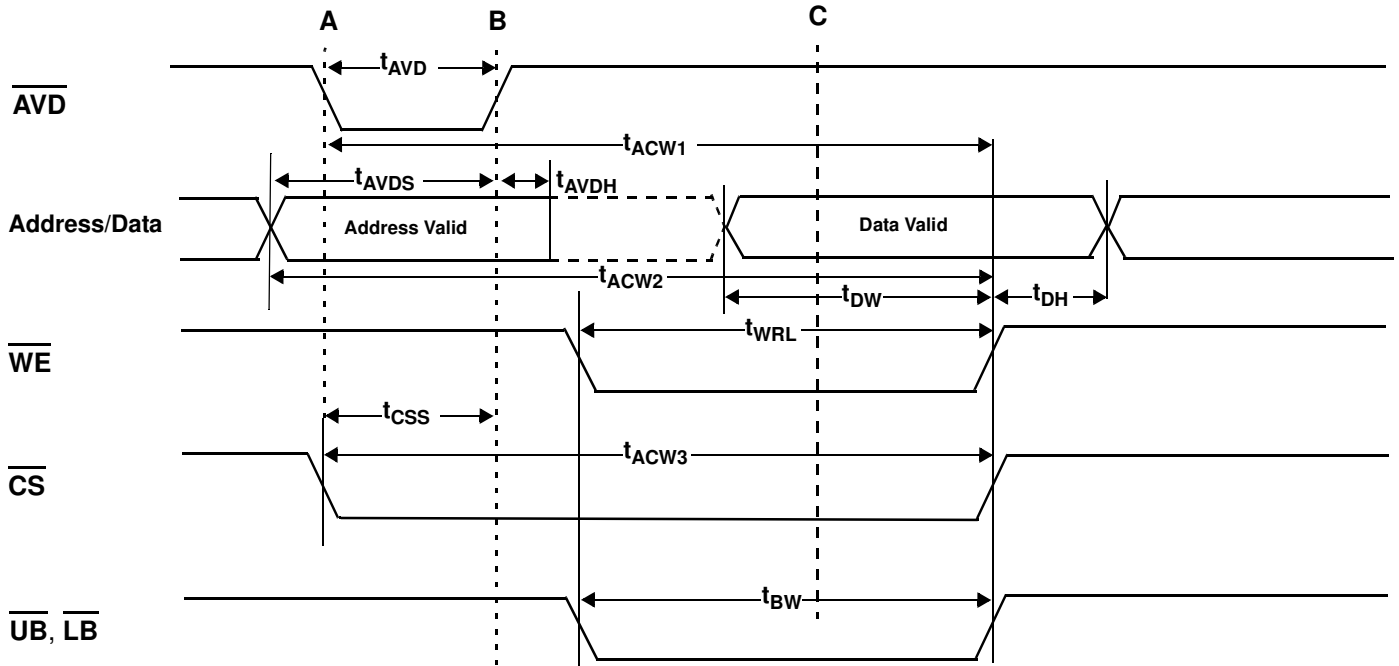## TIMING WAVEFORM OF READ CYCLE (2) ($\overline{WE} = V_{IH}$)

NOTES (READ CYCLE)

1. t_{HZ} and t_{BHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

Write Access

The write access is initiated by applying the address to the multiplexed address/data bus or to the address bus over A_{15} (A_{16} -> A_{xx}). When the address is stable, the device chip select($\overline{CS}$) is set active low. At point A, the $\overline{AVD}$ signal is taken low and the latch becomes transparent. This allows the address to be propagated to the memory array. The address is stable at the rising edge of the $\overline{AVD}$ signal. The $\overline{AVD}$ signal goes high at point B in which the address latch is completed. At this point, the second stage of the write process is entered. Data is input to the multiplexed address/data bus. The $\overline{WE}$ signal is set low and control signal $\overline{UB}$ and $\overline{LB}$ are set according to the access.

### TIMING WAVEFORM OF WRITE CYCLE (1) ($\overline{OE}$ = V_{IH})

TIMING WAVEFORM OF WRITE CYCLE (2) ($\overline{OE}$ = V_{IH})
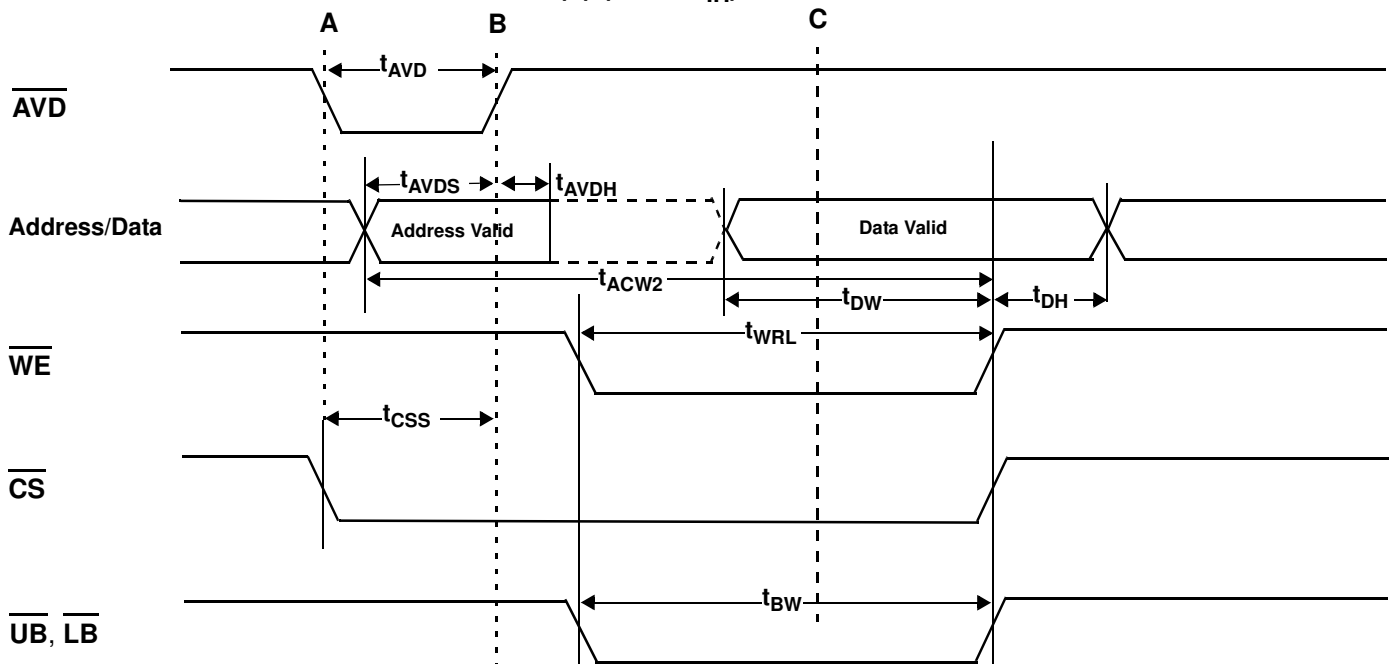
NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WRL}) of low $\overline{CS}$, low $\overline{WE}$ and low $\overline{UB}$ or $\overline{LB}$. A write begins at the last transition among low $\overline{CS}$ and low $\overline{WE}$ with asserting $\overline{UB}$ or $\overline{LB}$ low for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ low for word operation. A write ends at the earliest transition among high $\overline{CS}$ and high $\overline{WE}$. The t_{WRL} is measured from the beginning of write to the end of write.

TIMING WAVEFORM OF POWER UP
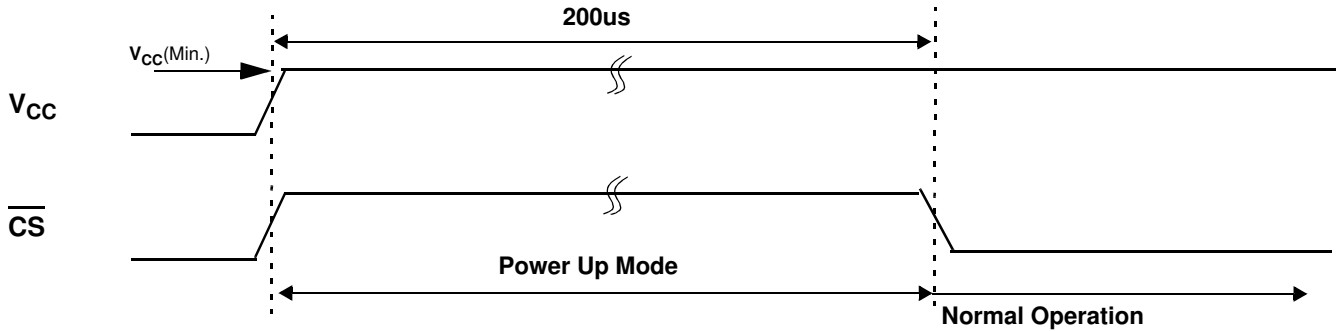
NOTE . (POWER UP)

1. After Vcc reaches Vcc(Min.) , wait 200us with $\overline{CS}$ high. Then you get into the normal operation.

RMS (Reduced Memory Size)

The 16M STRAM can be operated as a 2M, 4M, 8M or 16M device. The mode is set according to configuration register access timings, and the array size is set by configuration register bit 2 and 3. While operating in the RMS mode, the unselected memory array may not be used.
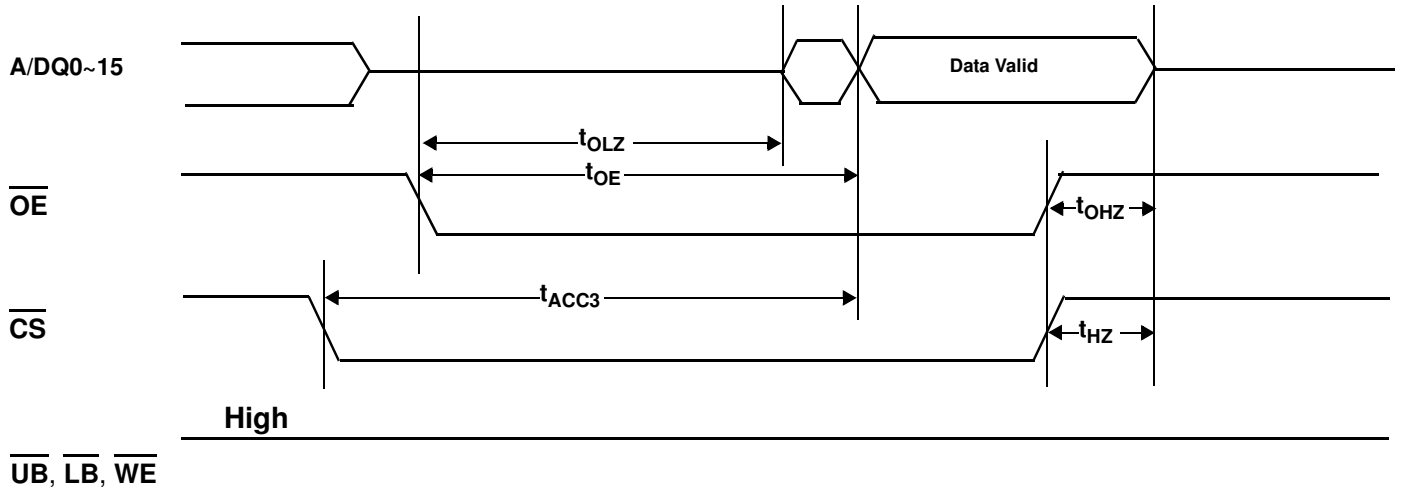
TCSR (Temperature Cotrolled Self Refresh)

The 16M STRAM can be operated with temperature controlled self-refresh. The device internal self-refresh period is controlled according as temperature change automatically.

Configuration Register Setting Table

Bit Number	Definition	Remark			
15 ~ 8	Do not use in normal mode				
7 ~ 4	Reserved for future use				
3 ~ 2	Reduced Memory Size	**Bit 3**	**Bit 2**	**Memory Size**	**Using Addresses**
		0	0	Full Array(Default)	$ADQ_{0 \sim 15}$, $A_{16} \sim A_{19}$
		0	1	1/2 Array	$ADQ_{0 \sim 15}$, $A_{16} \sim A_{18}$
		1	0	1/4 Array	$ADQ_{0 \sim 15}$, $A_{16} \sim A_{17}$
		1	1	1/8 Array	$ADQ_{0 \sim 15}$, A_{16}
1 ~ 0	Temperature	**Bit 1**	**Bit 0**	**Temperature Range**	
		0	0	Auto TCSR	

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TIMING WAVEFORM OF CONFIGURATION REGISTER ACCESS

- Read Cycle ($\overline{AVD}$ signal is fixed "High")

A/DQ0~15

t_{OLZ}

t_{OE}

$\overline{OE}$

t_{OHZ}

t_{ACC3}

$\overline{CS}$

t_{HZ}

Data Valid

High

$\overline{UB}$, $\overline{LB}$, $\overline{WE}$

- Write Cycle ($\overline{AVD}$ signal is fixed "High")

A/DQ0~15

Data Valid

t_{DW}

t_{DH}

t_{WRL}

$\overline{WE}$

t_{ACC3}

$\overline{CS}$

High

$\overline{UB}$, $\overline{LB}$, $\overline{OE}$

MEMORY FUNCTION GUIDE

EM X XX X X X XX X X - XX XX

1. EMLSI Memory
2. Device Type
3. Density
4. Option
5. Technology
6. Operating Voltage

11. Power
10. Speed
9. Packages
8. Version
7. Organization
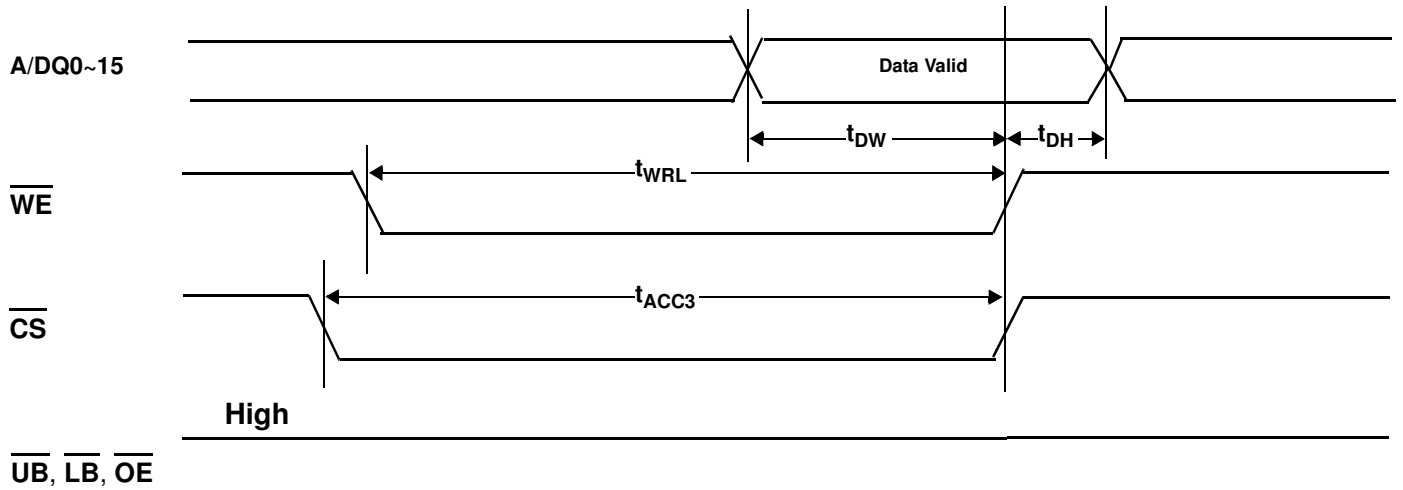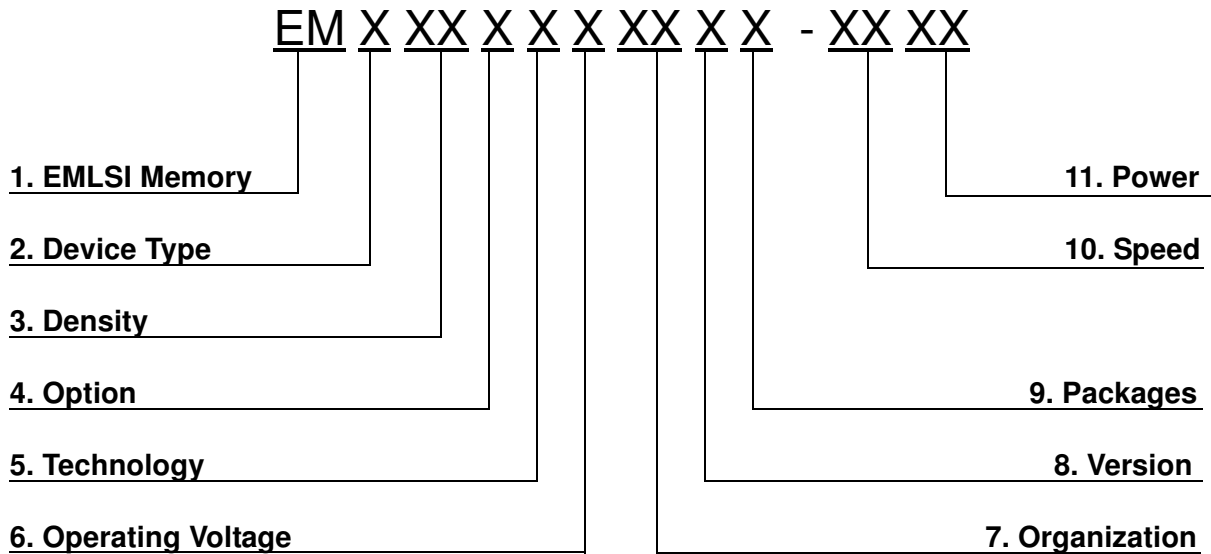
1. Memory Component

2. Device Type
6 ----------------------- Low Power SRAM
7 ----------------------- STRAM

3. Density
1 ----------------------- 1M
2 ----------------------- 2M
4 ----------------------- 4M
8 ----------------------- 8M
16 --------------------- 16M
32 --------------------- 32M
64 --------------------- 64M

4. Function
0 ---------------------- Dual CS
1 ---------------------- Single CS
2 ---------------------- Multiplexed

5. Technology
Blank ----------------- CMOS
F ----------------------- Full CMOS
S ----------------------- Single Transistor

6. Operating Voltage
Blank ------------------- 5V
V ----------------------- 3.3V
U ----------------------- 3.0V
S ----------------------- 2.5V
R ----------------------- 2.0V
P ----------------------- 1.8V
O ----------------------- 1.5V

7. Organization
8 ---------------------- x8 bit
16 --------------------- x16 bit
32 --------------------- x32 bit

8. Version
Blank ---------------- Mother die
A ----------------------- First version
B ----------------------- Second version
C ----------------------- Third version
D ----------------------- Fourth version
E ----------------------- Fifth version

9. Package
Blank ---------------------- Package
W -------------------- Wafer

10. Speed
45 ---------------------- 45ns
55 ---------------------- 55ns
70 ---------------------- 70ns
85 ---------------------- 85ns
90 ---------------------- 90ns
10 -------------------- 100ns
12 -------------------- 120ns

11. Power
LL --------------------- Low Low Power
L ---------------------- Low Power
S ---------------------- Standard Power