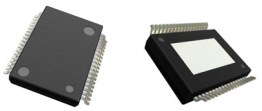
LNBH24

Dual LNB supply and control IC with step-up and I²C interface

Features

- Complete interface between LNBS and I²C bus
- Built-in DC-DC converter for single 12 V supply operation and high efficiency (typ. 93%@0.5 A)
- Selectable output current limit through external resistor
- Compliant with main satellite receivers output voltage specification
- New accurate built-in 22 kHz tone generator meets widely accepted standards (patent pending)
- Fast oscillator start-up facilitates DiSEqC™ encoding
- Built-in 22 kHz tone detector supports bi-directional DiSEqC™ 2.0
- Very low-drop post regulator and high efficiency step-up PWM with integrated power N-MOS allow low power losses
- Two output pins suitable for bypassing the output R-L filter and avoiding tone distortion (R-L filter as per DiSEqC™ 2.0 specs, see typ. application circuits)
- Overload and over-temperature internal protections with I²C diagnostic bits
- Output voltage and output current level diagnostic feedback by I²C bits
- LNB short circuit dynamic protection
- +/- 4 kV ESD tolerant on output power pins



PowerSSO-36 (ePad)

Description

Intended for analog and digital DUAL Satellite receivers/Sat-TV, sat-PC cards, the LNBH24 is a monolithic voltage regulator and interface IC, assembled in PowerSSO-36 ePad, specifically designed to provide the 13/18 V power supply and the 22 kHz tone signalling for two independent LNB down-converters in the antenna dishes and/or multi-switch box. In this application field, it offers a dual tuner STBs with extremely low component count, low power dissipation together with simple design and I²C standard interfacing.

Table 1. Device summary

Order code	Package	Packaging
LNBH24PPR	PowerSSO-36 (Exposed pad)	Tape and reel

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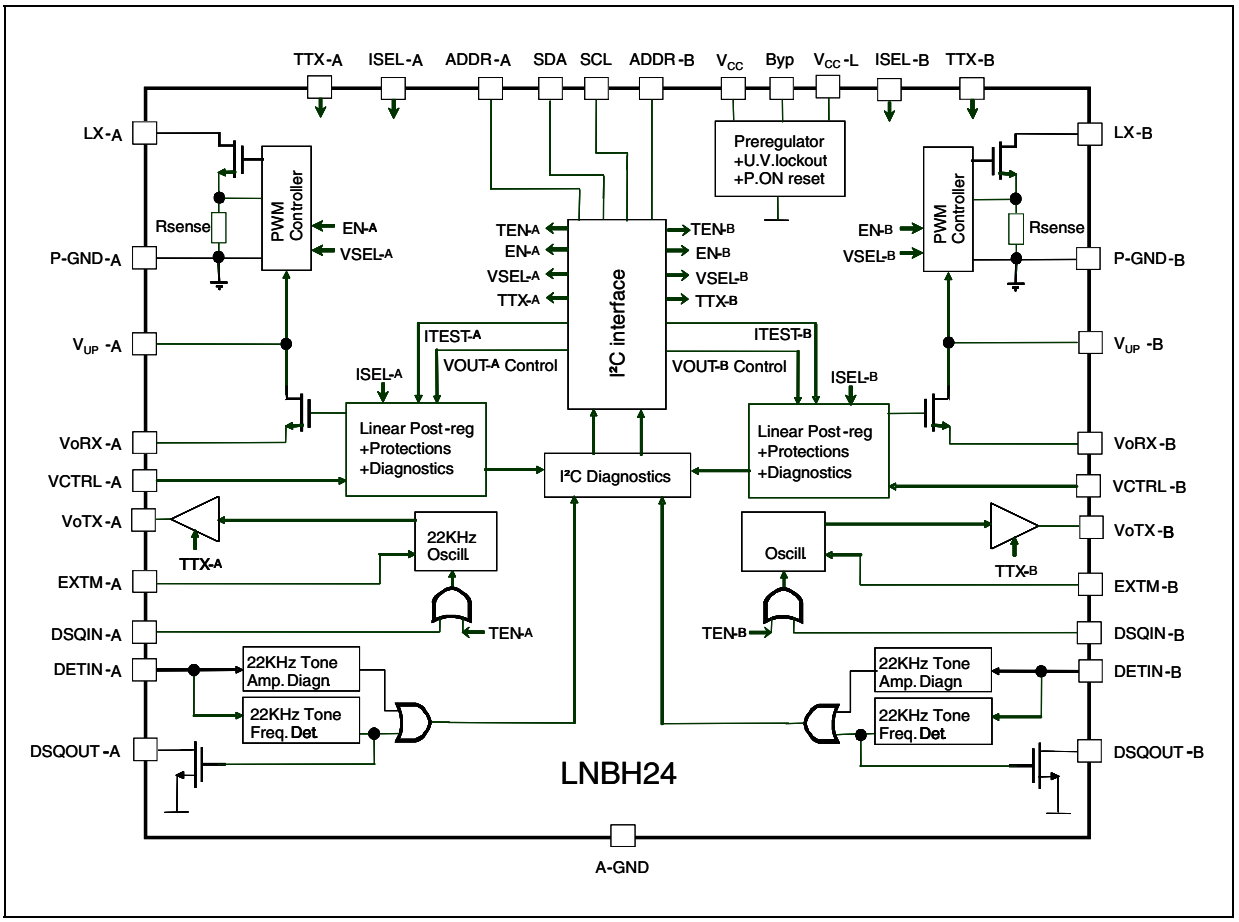
1 Block diagram

Figure 1. Block diagram



2 Introduction

The LNBH24 includes two completely independent sections. Except for the V_{CC} and I²C inputs, each circuit can be separately controlled and have independent external components. The specification that follow should be considered equally for both sections (A/B).

2.1 Application information

This IC has a built-in DC-DC step-up converter which, from a single 8 V to 15 V source, generates the voltages (V_{UP}) that allow the linear post-regulator to work at a minimum dissipated power of 0.375 W Typ. @ 500 mA load (the linear post-regulator drop voltage is internally held at V_{UP}-V_{OUT}=0.75 V typ.). An under voltage lockout circuit will disable the entire circuit when the supplied V_{CC} drops below a fixed threshold (6.7 V typically).

Note: In this document the V_{OUT} is intended as the Voltage present at the linear post-regulator output (V_{oRX} pin).

2.2 DiSEqC™ data encoding and decoding

The new internal 22 kHz tone generator (patent pending) is factory trimmed in accordance with the standards, and can be selected through I²C interface TTX bit (or TTX pin) and activated by a dedicated pin (DSQIN) which allows immediate DiSEqC™ data encoding, or through TEN I²C bit in case the 22 kHz presence is requested in continuous mode. In standby condition (EN bit LOW). The TTX function must be disabled setting TTX to LOW.

2.3 DiSEqC™ 2.0 implementation

The built-in 22 kHz Tone detector completes the fully bi-directional DiSEqC™ 2.0 (see *Note:*) interfacing. Its input pin (DETIN) must be AC coupled to the DiSEqC™ bus, and extracted PWK data are available on the DSQOUT pin. To comply with the bi-directional DiSEqC™ 2.0 bus hardware requirements an output R-L filter is needed. The LNBH24 is provided with two output pins for each section, one for the DC voltage output (V_{oRX}) and one for the 22 kHz tone transmission (V_{oTX}). The V_{oTX} must be activated only during the tone transmission while the V_{oRX} provides the 13/18 V output voltage. This allows the 22 kHz Tone to pass without any losses due to the R-L filter impedance (see *Figure 4*). During the 22 kHz transmission, in DiSEqC™ 2.0 applications, activated by DSQIN pin or by the TEN bit, the V_{oTX} pin must be preventively set ON by the TTX function. This can be controlled both through the TTX pin and the I²C bit. As soon as the tone transmission is expired, the V_{oTX} must be disabled by setting the TTX to LOW to set the device in the 22 kHz receiving mode. The 13/18 V power supply is always provided to the LNB from the V_{oRX} pin through the R-L filter.

2.4 DiSEqC™ 1.X implementation

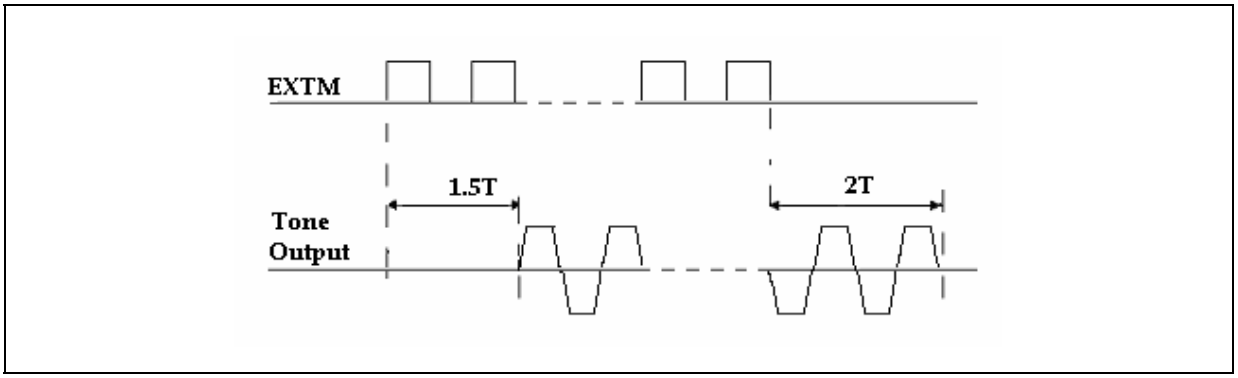
When the LNBH24 is used in DiSEqC™ 1.x applications the R-L filter is always needed for the proper operation of the 22 kHz tone generator (patent pending. See *Figure 4*). Also in this case, the TTX function must be preventively enabled before to start the 22 kHz data transmission and disabled as soon as the data transmission has been expired. The tone can

be activated both with the DSQIN pin or the TEN I²C bit. The DSQIN internal circuit activates the 22 kHz tone on the V_{oTX} output with 0.5 cycle ± 25 µs delay from the TTL signal presence on the DSQIN pin, and it stops with 1 cycle ± 25 µs delay after the TTL signal is expired.

2.5 Data encoding through external tone generator (EXTM)

In order to improve design flexibility an external tone input pin is available (EXTM). The EXTM is a Logic input pin which activates the 22 kHz tone output, on the V_{oTX} pin, by using the LNBH24 integrated tone generator (similar to the DSQIN pin function). In fact, the output tone waveform characteristics will always be internally controlled by the LNBH24 tone generator and the EXTM signal will be used as a timing control for DiSEqC tone data encoding on the V_{oTX} output. A TTL-compatible 22 kHz signal is required for the proper control of the EXTM pin function. Before sending the TTL signal on the EXTM pin, the V_{oTX} tone generator must be previously enabled through the TTX function (TTX pin or TTX bit set HIGH). As soon as the EXTM internal circuit detects the 22 kHz TTL signal code, it activates the 22 kHz tone on the V_{oTX} output with 1.5 cycles ±25 µs delay from the TTL signal presence on the EXTM pin, and it stops with 2 cycles ±25 µs delay after the TTL signal is expired (see *Figure 2*).

Figure 2. EXTM timings



2.6 I²C interface

The main functions of the IC are controlled via I²C BUS by writing 8 bits on the System Register (SR 8 bits in write mode). On the same register there are 8 bits that can be read back (SR 8 bits in read mode) to provide 8 diagnostic functions: five bits will report the diagnostic status of five internal monitoring functions (IMON, VMON, TMON, OTF, OLF), while three will report the last output voltage register status (EN, VSEL, LLC) received by the IC (see the diagnostic functions section). Each section (A/B) has two selectable I²C addresses selectable, respectively, through the ADDR-A and ADDR-B pins (see address pins characteristics *Table 10*).

2.7 Output voltage selection

When the IC sections are in standby mode (EN bit LOW), the power blocks are disabled. When the regulator blocks are active (EN bit HIGH), the output can be logic controlled to be 13 or 18 V by means of the VSEL bit (Voltage SELect) for remote controlling of non-DiSEqC LNBs. Additionally, the LNBH24 is provided with the LLC I^2C bit which increase the selected voltage value by +1 V to compensate the excess of voltage drop along the coaxial cable.

The LNBH24 is also compliant with the USA LNB power supply standards. In order to allow fast transition of the output voltage from 18 V to 13 V and vice-versa, the LNBH24 is provided with the VCTRL TTL pin which keeps the output at 13 V when it is set LOW and at 18 V when it is set HIGH or floating. VSEL and, if required, LLC bits must be set HIGH before using the VCTRL pin to switch the output voltage level. If VCTRL=1 or floating, then V_{OUT}=18.5 V (or 19.5 V if LLC=1). With VCTRL=0 V_{OUT}=13.4 V (LLC= either 0 or 1). Should be noted that the VCTRL pin controls only the linear regulator V_{OUT} stage while the step-up V_{UP} voltage is controlled only through the VSEL and LLC I²C bits. That is, even if VCTRL=0 (keeping V_{OUT}=13.4 V) you will have V_{UP}=19.25 V typ when VSEL=1 and 20.25 V with VSEL=LLC=1. This means that VCTRL=0 must be used only for short period to avoid the higher power dissipation. In standby condition (EN bit LOW) all the I²C bits and the TTX pin must be set LOW (if the TTX pin is not used it can be left floating but the TTX bit must be set LOW during the standby condition).

2.8 Diagnostic and protection functions

The LNBH24 has 5 diagnostic internal functions provided via I²C BUS by reading 5 bits on the system register (SR bits in read mode). All the diagnostic bits are, in normal operation (no failure detected), set to LOW. Two diagnostic bits are dedicated to the over-temperature and over-load protection status (OTF and OLF), while the remaining 3 bits are dedicated to the output voltage level (VMON), 22 kHz Tone (TMON) and to the Minimum Load Current diagnostic function (IMON).

2.9 Output voltage diagnostic

When VSEL=0 or 1 and LLC=0, the output voltage pin (V_{oRX}) is internally monitored and, as long as the output voltage level is below the guaranteed limits, the VMON I²C bit is set to "1". The output voltage diagnostic is valid only with LLC=0 and AUX=0. Any VMON information with LLC=1 and/or AUX=1 must be disregarded by the MCU.

2.10 22 kHz tone diagnostic

The 22 kHz tone can be internally detected and monitored If the DETIN pin is connected to the LNB output bus (see typical application circuits) through a decoupling capacitor. The Tone diagnostic function is provided with the TMON I²C bit. If the 22 kHz Tone amplitude and/or the Tone frequency is out of the guaranteed limits (see TMON limits in the electrical characteristics in *Table 13*), the TMON I²C Bit is set to "1".

2.11 Minimum output current diagnostic

In order to detect the output load absence (no LNB connected on the bus or cable not connected to the IRD) the LNBH24 is provided with a minimum output current flag by the IMON I²C bit in read mode, which is set to "1" if the output current is lower than 12 mA typically with ITEST=1, and 6 mA with ITEST=0. The minimum current diagnostic function (IMON) is always active. In order for it to function even in a multi-IRD configuration (multi-switch), where the supply current could be sunk only from the higher supply voltage connected to the multi-switch box, the LNBH24 is provided with the AUX I^2C bit. To force the LNBH24 output voltage as the highest voltage on the bus (22 V typ.) during the minimum current diagnostic phase, the AUX I^2C bit can be set HIGH before reading the IMON I^2C bit status. When the AUX bit is set to HIGH, the V_{OUT} is set to 22 V (typ.) and the V_{UP} is set to

22.75 V (V_{UP}=V_{OUT}+0.75 V typ.) independent of the VSEL/LLC bits status. If the AUX function is used to force the V_{OUT} to 22 V, it is recommended to set the AUX bit to LOW as soon as the minimum current test phase is expired, so that the V_{OUT} voltage will be controlled again as per the VSEL/LLC bits status. In order to avoid false triggering, the IMON function must be used only with the 22 kHz tone transmission deactivated (TEN=0 and DSQIN=LOW), otherwise the IMON bit could be set to 0 even if the output current is below the minimum current thresholds (6 mA or 12 mA).

2.12 Output current limit selection

The linear regulator current limit threshold can be set through an external resistor connected to ISEL pin. The resistor value defines the output current limit by the equation:
$I_{MAX(A)} = 10000/R_{SEL}$

where R_{SEL} is the resistor connected between ISEL and GND. The highest selectable current limit threshold is 1.0 A typ with R_{SEL}=10 kΩ. The above equation defines the typical threshold value for each output. However, it is suggested not to exceed for an extended period a total of current of 1 A from both sections ($I_{OUT\_A} + I_{OUT\_B} < 1$ A) in order to avoid triggering the over-temperature protection.

2.13 Over-current and short-circuit protection and diagnostic

In order to reduce the total power dissipation during an overload or a short-circuit condition, the device is provided with a dynamic short-circuit protection. It is possible to set the short-circuit current protection either statically (simple current clamp) or dynamically through the PCL bit of the I²C SR. When the PCL (pulsed current limiting) bit is set to LOW, the over-current protection circuit works dynamically: as soon as an overload is detected, the output is shut down for a time T_{OFF}, typically 900 ms. Simultaneously the diagnostic OLF I²C bit of the system register is set to "1". After this time has elapsed, the output is resumed for a time T_{ON} = (1/10) T_{OFF} = 90 ms (typ.). At the end of T_{ON}, if the overload is still detected, the protection circuit will cycle again through T_{OFF} and T_{ON}. At the end of a full T_{ON} in which no overload is detected, normal operation is resumed and the OLF diagnostic bit is reset to LOW. Typical T_{ON}+T_{OFF} time is 990 ms and an internal timer determines it. This dynamic operation can greatly reduce the power dissipation in short-circuit condition, still ensuring excellent power-on start-up in most conditions. However, there could be some cases in which a highly capacitive load on the output may cause a difficult start-up when the dynamic protection is chosen. This can be solved by initiating any power start-up in static mode (PCL=1) and then switching to the dynamic mode (PCL=0) after a chosen amount of time depending on the output capacitance. When in static mode, the diagnostic OLF bit goes to "1" when the current clamp limit is reached and returns LOW when the overload condition is cleared.

2.14 Thermal protection and diagnostic

The LNBH24 is also protected against overheating. When the junction temperature exceeds 150 °C (typ.), the step-up converter and the liner regulator are shut off, and the diagnostic OTF SR bit is set to "1". Normal operation is resumed and the OTF bit is reset to LOW when the junction is cooled down to 135 °C (typ.).

Note: External components are needed to comply to bi-directional DiSEqC™ bus hardware requirements. Full compliance of the whole application with DiSEqC™ specifications is not implied by the use of this IC. NOTICE: DiSEqC™ is a trademark of EUTELSAT.

3 Pin configuration

Figure 3. Pin connections

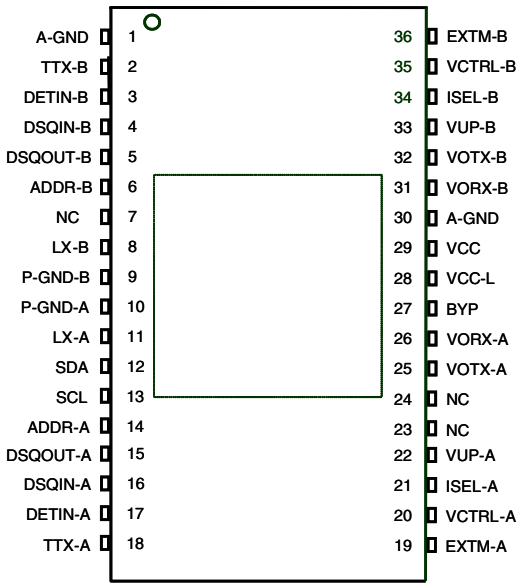


Table 2. Pin description

Pin n° (sec. A/B)	Symbol	Name	Function
29	V_{CC}	Supply input	8 to 15 V IC DC-DC power supply.
28	V_{CC}_L	Supply input	8 to 15 V analog power supply.
11	LX-A	N-MOS Drain	Integrated N-Channel power MOSFETs drain.
8	LX-B		
22	V_{UP}-A	Step-Up voltage	Input of the linear post-regulators. The voltage on these pins is monitored by the internal step-up controllers to keep a minimum dropout across the linear pass transistors.
33	V_{UP}-B		
26	V_{oRX}-A	LDO output port	Outputs of the linear post-regulators. See *Table 6* for voltage selections and description.
31	V_{oRX}-B		
25	V_{oTX}-A	Output port during 22 kHz Tone TX	TX Outputs to the LNB. See *Table 6* for selection.
32	V_{oTX}-B		
12	SDA	Serial data	Bi-directional data from / to I^2C BUS.
13	SCL	Serial clock	Clock from I^2C BUS.
16	DSQIN-A	DiSEqC inputs	These pins will accept the DiSEqC code from the main microcontroller. The LNBH24 will uses this code to modulate the internally-generated 22 kHz carrier. Set to ground if not used.
4	DSQIN-B		

Table 2. Pin description (continued)

Pin n° (sec. A/B)	Symbol	Name	Function
18	TTX-A	TTX enable	The TTX pins can be used as well as the TTX I^2C bits of the system register, to control the TTX function enable. Set floating or to GND if not used.
2	TTX-B		
17	DETIN-A	Tone decoders inputs	22 kHz tone decoders inputs must be AC coupled to the DiSEqC 2.0 BUS. Set to GND if not used.
3	DETIN-B		
15	DSQOUT- A	DiSEqC outputs	Open drain outputs of the tone detectors to the main µController for DiSEqC 2.0 data decoding. They are LOW when tone is detected on DETIN pins. Set to GND if not used.
5	DSQOUT- B		
19	EXTM-A	External modulation	External modulation logic input pins which activate the 22 kHz tone output on the V_{oTX} pins. Set to ground if not used.
36	EXTM-B		
10	P-GND-A	Power grounds	DC-DC converters power grounds.
9	P-GND-B		
ePad	ePad	Exposed Pad	To be connected with power grounds and to the ground layer through vias to dissipate the heat.
1, 30	A-GND	Analog grounds	Analog circuits grounds.
27	BYP	By-pass capacitor	Needed for internal pre-regulator filtering. The BYP pin is intended only to connect an external ceramic capacitor. Any connection of this pin to external current or voltage sources may cause permanent damage to the device.
14	ADDR-A	Address setting	Two I²C addresses available for each section by setting the Address pins voltage level. See *Table 10*
6	ADDR-B		
21	ISEL-A	Current selection	The resistors “RSEL” connected between ISEL and GND define the linear regulators current limit protection threshold by the equation: $I_{MAX}(typ)=10000/ RSEL$.
34	ISEL-B		
20	VCTRL-A	Output voltage control	13 V-18 V linear regulators V_{oRX} switch control. To be used only with VSEL=1. If V_{CTRL}=1 or floating VoRX=18.5 V (or 19.5V if LLC=1). If V_{CTRL}=0 than VoRX=13.4 V (LLC=either 0 or 1). Leave floating if not used. DO NOT connect to GND if not used.
35	VCTRL-B		
7, 23, 24	N.C.	Not connected	Not internally connected pins.

4 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC-L}, V_{CC}	DC power supply input voltage pins	-0.3 to 16	V
V_{UP}	DC input voltage	-0.3 to 24	V
I_O	Output current	Internally limited	
V_{oRX}	DC output pin voltage	-0.3 to 25	V
V_{oTX}	Tone output pin voltage	-0.3 to 25	V
V_I	Logic input voltage (TTX, SDA, SCL, DSQIN, EXTM, V_{CTRL}, Address)	-0.3 to 7	V
LX	LX input voltage	-0.3 to 24	V
V_{DETIN}	Detector input signal amplitude	2	V_{PP}
V_{OH}	Logic high output voltage (DSQOUT)	-0.3 to 7	V
V_{BYP}	Internal reference pin voltage (*Note 1*)	-0.3 to 4.6	V
ISEL	Current selection pin voltage	-0.3 to 4.6	V
T_{STG}	Storage temperature range	-50 to 150	°C
T_J	Operating junction temperature range	-25 to 125	°C
ESD	ESD rating with Human Body Model (HBM) for all pins unless 8, 11, 25, 26, 31, 32	2	KV
	ESD rating with Human Body Model (HBM) for pins 25, 26, 31, 32	4	
	ESD rating with Human Body Model (HBM) for pins 8, 11	0.6	

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to network ground terminal.

Note: 1 The BYP pin is intended only to connect an external ceramic capacitor. Any connection of this pin to external current or voltage sources may cause permanent damage to the device.

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case	2	°C/W
R_{thJA}	Thermal resistance junction-ambient (PSSO-36) with device soldered on 2s2p PC Board	30	°C/W

5 Application circuit

Figure 4. Typical application circuit

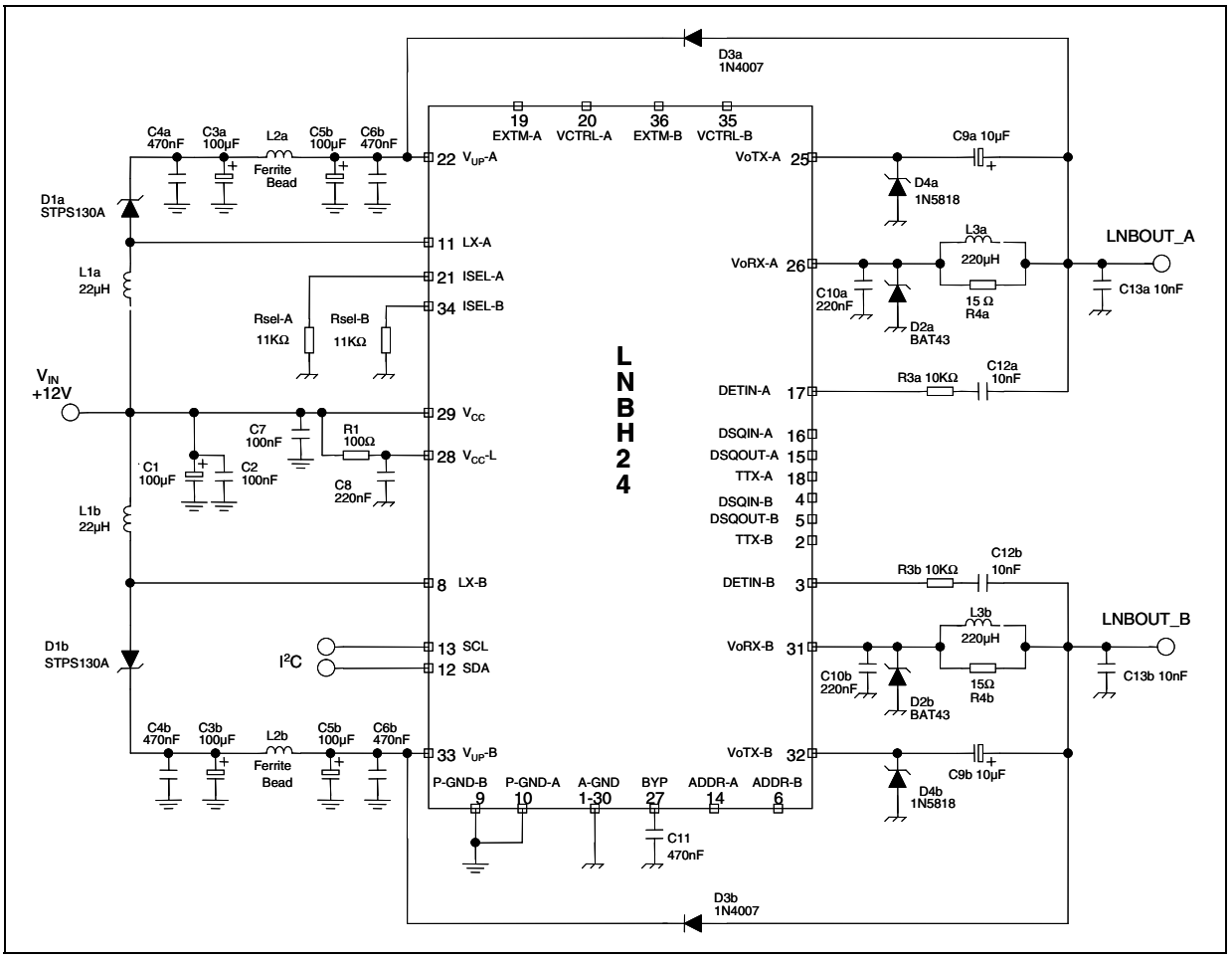


Table 5. Bill of material (valid for A and B sections except for C1, C2, C7, C8 and R1)

Component	Notes
R1, R4	1/4 W resistors. Refer to the typical application circuit for the relative values
R3, R_{SEL}	1/8 W resistors. Refer to the typical application circuit for the relative values
C1	25 V electrolytic capacitor, 100 µF or higher is suitable.
C9	10µF, > 35 V electrolytic capacitor
C3, C5	100µF, > 25 V electrolytic capacitor, ESR in the 150 mΩ to 350 mΩ range
C2, C4, C6, C7, C8, C10, C11, C12, C13	>25 V ceramic capacitors. Refer to the typ. appl. circuit for the relative values
D1	STPS130A or any similar schottky diode with V_{RRM} > 25 V and $I_{F(AV)}$ higher than: $I_{F(AV)} > I_{OUT\_MAX}$ x (V_{UP_MAX}/V_{IN_MIN})
D2	BAT43, 1N5818, or any schottky diode with $I_{F(AV)}$>0.2A, V_{RRM} > 25 V, V_F<0.5 V
D3	1N4007 or equivalent
D4	1N5818 or equivalent schottky diode
L1	22µH inductor with $I_{SAT}>I_{PEAK}$, where I_{PEAK} is the boost converter peak current: $I_{PEAK} = \frac{V_{UP\_MAX} * I_{OUT\_MAX}}{Eff * V_{IN\_MIN}} + \frac{V_{IN\_MIN}}{2LF}\left(1 - \frac{V_{IN\_MIN}}{V_{UP\_MAX}}\right)$
L2	Ferrite bead, Panasonic-EXCELS A35, Murata-BL01RN1-A62, Taiyo-Yuden-BKP1608HS600 or equivalent with similar or higher impedance and current rating higher than 2A
L3	220 µH-270 µH inductor with current rating higher than rated output current

6 I²C bus interface

Data transmission from main MCU to the LNBH24 and vice-versa takes place through the 2 wires I^2C bus Interface, consisting of the 2 SDA and SCL lines (pull-up resistors to positive supply voltage must be externally connected).

6.1 Data validity

As shown in *Figure 5* the data on the SDA line must be stable during the high semi-period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

6.2 Start and stop condition

As shown in *Figure 6* a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition.

6.3 Byte format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

6.4 Acknowledge

The master (MCU) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see *Figure 7*). The peripheral (LNBH24) that acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse. The peripheral which has been addressed has to generate acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer. The LNBH24 will not generate acknowledge if the V_{CC} supply is below the under-voltage lockout threshold (6.7 V typ.).

6.5 Transmission without acknowledge

Avoiding to detect the acknowledges of the LNBH24, the MCU can use a simpler transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data. This approach of course is less protected from malfunctions and decreases the noise immunity.

Figure 5. Data validity on the I²C bus

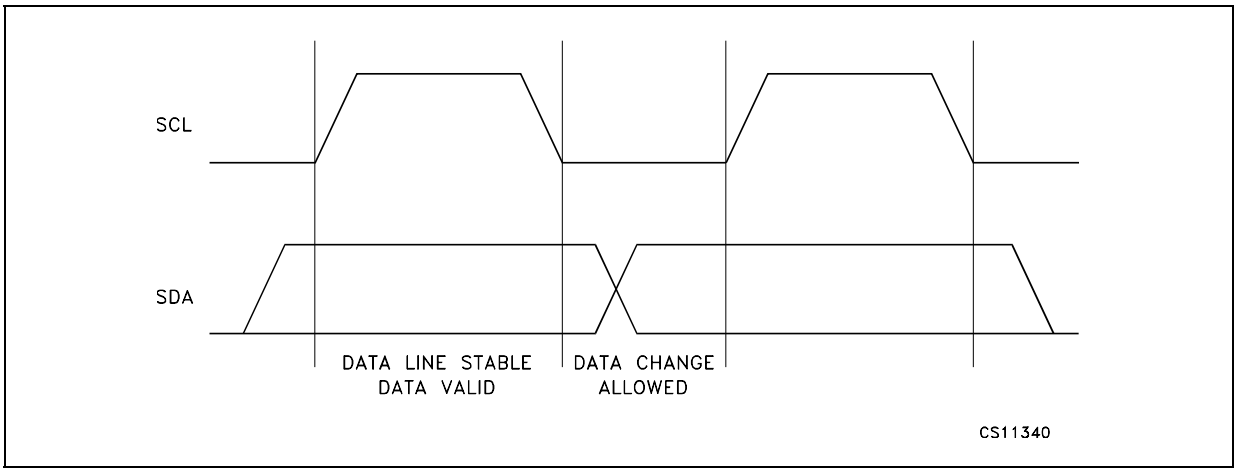


Figure 6. Timing diagram of I²C bus

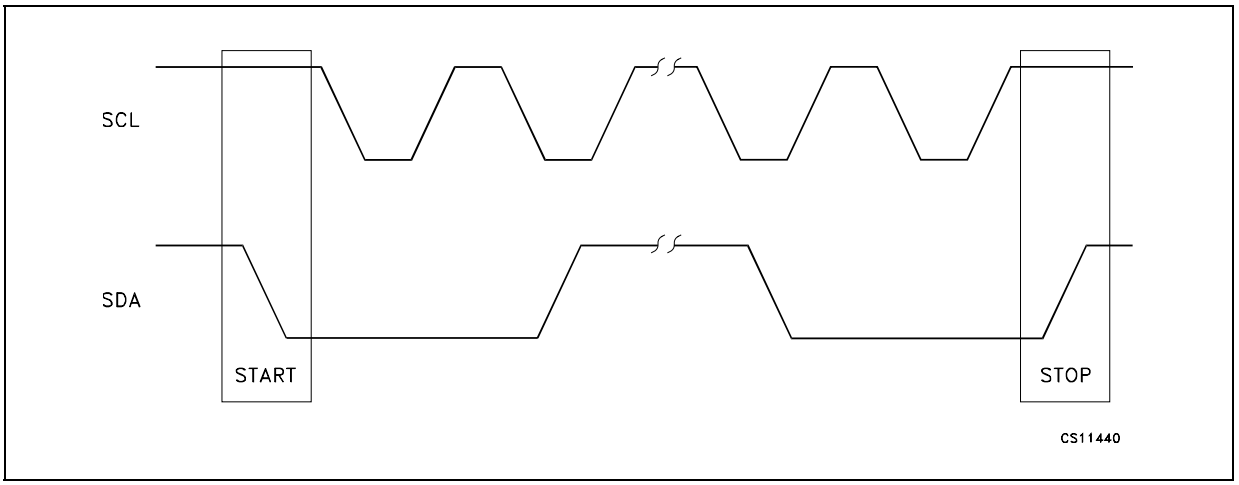
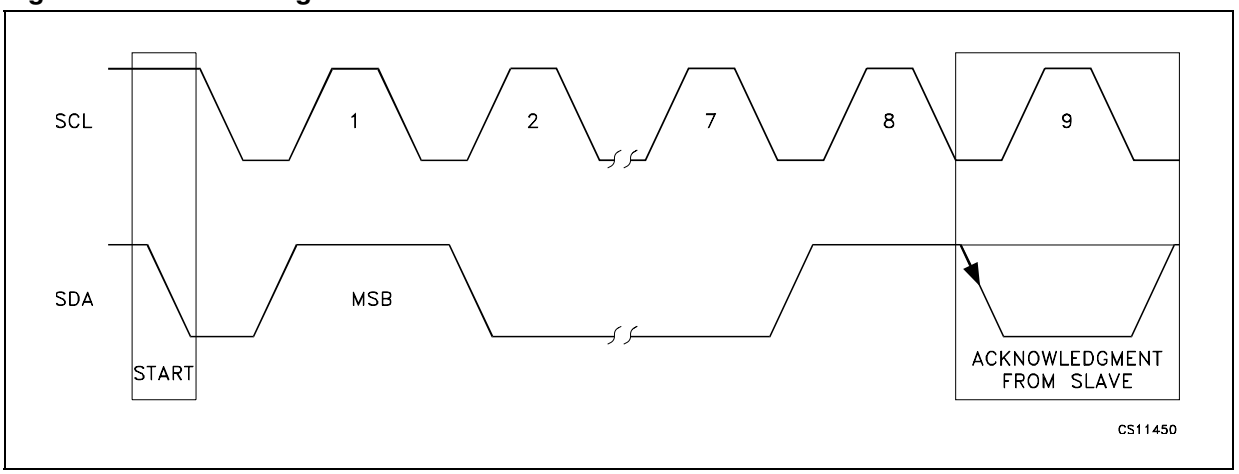


Figure 7. Acknowledge on the I²C bus



7 LNBH24 software description

The LNBH24 I^2C interface controls both the IC sections A and B depending on the address sent before the DATA byte. The description below is valid for both sections.

7.1 Interface protocol

The interface protocol comprises:

- A start condition (S)
- A chip address byte (the LSB bit determines read (=1)/write (=0) transmission)
- A sequence of data (1 byte + acknowledge)
- A stop condition (P)

	Section address (A or B)										Data									
	MSB							LSB			MSB							LSB		
S	0	0	0	1	0	X	X	R/W	ACK										ACK	P

ACK = Acknowledge

S = Start

P = Stop

R/W = 1/0, Read/Write bit

X = 0/1, two addresses for each section selectable by ADDR-A/B pins (see *Table 10*)

7.2 System register (SR, 1 Byte for each section A and B)

Mode	MSB							LSB
Write	PCL	TTX	TEN	LLC	VSEL	EN	ITEST	AUX
Read	IMON	VMON	TMON	LLC	VSEL	EN	OTF	OLF

Write = control bits functions in write mode

Read = diagnostic bits in read mode.

All bits reset to 0 at power on

7.3 Transmitted data (I^2C bus write mode) for each section A/B

When the R/W bit in the section address is set to 0, the main MCU can write on the system register (SR) of the relative section (A or B, depending on the 7 bit address value) via I^2C BUS. All and 8 bits are available and can be written by the MCU to control the device functions as per the below *Table 6*.

Table 6. Truth table

PCL	TTX	TEN	LLC	VSEL	EN	ITEST	AUX	Function
	0		0	0	1		0	V_{oRX}= 13.4 V, V_{UP}=14.15 V, (V_{UP}-V_{oRX}=0.75 V)
	0		0	1	1		0	V_{oRX}= 18.5 V, V_{UP}=19.25 V, (V_{UP}-V_{oRX}=0.75 V)
	0		1	0	1		0	V_{oRX}= 14.4 V, V_{UP}=15.15 V, (V_{UP}-V_{oRX}=0.75 V)
	0		1	1	1		0	V_{oRX}= 19.5 V, V_{UP}=20.25 V, (V_{UP}-V_{oRX}=0.75 V)
			X	X	1	X	1	V_{oRX}= 22 V, V_{UP}=22.75 V, (V_{UP}-V_{oRX}=0.75 V)
		0			1			22 KHz controlled by DSQIN pin (only if TTX=1)
	1	1			1			22 KHz tone output is always activated
	0				1			V_{oRX} output is ON, V_{oTX} Tone generator output is OFF
	1				1			V_{oRX} output is ON, V_{oTX} Tone generator output is ON
0					1			Pulsed (dynamic) current limiting is selected
1					1			Static current limiting is selected
			X	X	1	0		Minimum output current diagnostic threshold = 6mA typ.
			X	X	1	1		Minimum output current diagnostic threshold = 12mA typ.
X	X	X	X	X	0	X	X	Power block disabled

X = don't care

All values are typical unless otherwise specified

Valid with TTX pin floating or connected GND

7.4 Diagnostic received data (I²C read mode) for both sections A/B

The LNBH24 can provide to the master a copy of the diagnostic system register information via I²C bus in read mode. The read mode is master activated by sending the chip address with R/W bit set to 1. At the following master generated clock bits, the LNBH24 issues a byte on the SDA data bus line (MSB transmitted first). At the ninth clock bit the MCU master can:

- Acknowledge the reception, thus starting the transmission of another byte from the LNBH24
- No acknowledge, stopping the read mode communication

Three bits of the register are read back as a copy of the corresponding write output voltage register status (LLC, VSEL, EN), while the other five bits convey diagnostic information about the over-temperature (OTF), output voltage level (VMON), output overload (OLF), minimum output current presence (IMON) and 22 kHz tone (TMON). In normal operation the diagnostic bits are set to zero, while if a failure is occurring, the corresponding bit is set to one. At start-up all the bits are reset to zero.

Table 7. Register

IMON	VMON	TMON	LLC	VSEL	EN	OTF	OLF	Function
			These bits are read exactly the same as they were left after last write operation			0		T_J < 135°C, normal operation
						1		T_J > 150°C, power blocks disabled
							0	I_O < I_{OMAX}, normal operation
							1	I_O > I_{OMAX}, Overload Protection triggered
0/1	0/1	0/1						These bits are set to 1 if the relative parameter is out of the specification limits.

Note: Values are typical unless otherwise specified.

7.5 Power-ON I²C interface reset

The I²C interface built in the LNBH24 is automatically reset at power-ON. As long as the V_{CC} stays below the undervoltage lockout (UVL) threshold (6.7 V), the interface will not respond to any I²C command and the system registers (SR) are initialized to all zeroes, thus keeping the power blocks disabled. Once the V_{CC} rises above 7.3 V typ. The I²C interface becomes operative and the SRs can be configured by the main MCU. This is due to 500 mV hysteresis provided in the UVL threshold to avoid false re-triggering of the power-ON reset circuit.

7.6 Address pin

For each section of the LNBH24 it is possible to select two I²C interface addresses by means of the relevant ADDR pin. The ADDR pins are TTL-compatible and can be set as per address pins characteristics *Table 10*.

7.7 DiSEqC™ implementation for each section A/B

LNBH24 helps system designer to implement the bi-directional DiSEqC 2.0 protocol by allowing easy PWK modulation/demodulation of the 22 kHz carrier. Between the LNBH24 and the main MCU the PWK data is exchanged using logic levels that are compatible with both 3.3 V and 5 V MCU. This data exchange is made through two dedicated pins, DSQIN and DSQOUT, in order to maintain the timing relationships between the PWK data and the PWK modulation as accurate as possible. These two pins should be directly connected to two I/O pins of the MCU, thus leaving to the firmware the task of encoding and decoding the PWK data in accordance with the DiSEqC protocol. Full compliance of the system to the specification is thus not implied by the bare use of the LNBH24. The system designer should also take in consideration the bus hardware requirements, which can be simply accomplished by the R-L termination connected on the V_{OUT} pins of the LNBH24, as shown in the typical application circuits in *Figure 4*. To avoid any losses due to the R-L impedance during the tone transmission, LNBH24 has dedicated Tone output (V_{oTX}) that is connected after the filter and must be enabled by setting the TTX function to HIGH only during the tone transmission (see DiSEqC 2.0 implementation in sections *2.2* and *2.3*). Also unidirectional DiSEqC 1.x and non-DiSEqC system need this termination connected through a bypass capacitor and after an R-L filter with 15 Ω in parallel with a 220 µH-270 µH inductor. However, there is no need for tone decoding, so the DETIN and DSQOUT pins can be left connected to GND.

8 Electrical characteristics

Table 8. Electrical characteristics of sections A/B (refer to the typical application circuit in *Figure 4*, T_J from 0 to 85 °C, EN=1, VSEL=LLC=TEN=PCL=ITEST=TTX=AUX=0, R_{SEL} = 11 kΩ, DSQIN=LOW, V_I = 12 V, I_{OUT} = 50 mA, unless otherwise stated. Typical values are referred to T_J = 25 °C. V_{OUT}=V_{oRX} pin voltage. See software description section for I²C access to the system register)

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
V_{IN}	Supply voltage	I_{OUT}=750mA, VSEL=LLC=1		8	12	15	V
I_{IN}	Supply current	Both sections A and B enabled, I_{OUT}=0			20	30	mA
		Both sections A and B enabled, EN=TEN=TTX=1, I_{OUT}=0			50	70	
		EN=0			6		
V_{OUT}	Output voltage	AUX=1; I_{OUT}=50mA			22		V
		V_{SEL}=1, I_{OUT}=750mA	LLC=0	17.8	18.5	19.2	
			LLC=1	18.8	19.5	20.2	
		V_{SEL}=0, I_{OUT}=750mA	LLC=0	12.8	13.4	14	
			LLC=1	13.8	14.4	15	
V_{OUT}	Line regulation	V_{IN}=8 to 15V	VSEL=0		5	40	mV
			VSEL=1		5	60	
V_{OUT}	Load regulation	V_{SEL}=0 or 1, I_{OUT} from 50 to750mA				200	mV
13/18 T_R - T_F	13/18V Rise and Fall transition time by V_{CTRL} pin	V_{SEL}=LLC=1, V_{CTRL} from LOW to HIGH and vice versa, I_{OUT} from 6 to 450mA, C_O from 10 to 330nF			575		µs
I_{MAX}	Output current limiting	R_{SEL}=11KΩ		750		1000	mA
		R_{SEL}= 22KΩ		300		600	
I_{SC}	Output short circuit current	V_{SEL}=0/1, AUX=0/1			1000		mA
T_{OFF}	Dynamic overload protection OFF time	PCL=0, Output shorted			900		ms
T_{ON}	Dynamic overload protection ON time	PCL=0, Output shorted			T_{OFF}/10		
F_{TONE}	Tone frequency	DSQIN=HIGH or TEN=1, TTX=1		20	22	24	kHz
A_{TONE}	Tone amplitude	DSQIN=HIGH or TEN=1, TTX=1 I_{OUT} from 0 to750mA C_{OUT} from 0 to 750nF		0.4	0.65	0.9	V_{PP}
D_{TONE}	Tone duty cycle	DSQIN=HIGH or TEN=1, TTX=1		43	50	57	%
t_r, t_f	Tone rise or fall time	DSQIN=HIGH or TEN=1, TTX=1		5	8	15	µs
F_{EXTM}	EXTM frequency	V_{EXTM-H} =3.3V, V_{EXTM-L} =0V, (1)		20	22	24	kHz
Eff_{DC-DC}	DC-DC converter efficiency	I_{OUT}=750mA			93		%

Table 8. Electrical characteristics of sections A/B (continued) (refer to the typical application circuit in *Figure 4*, T_J from 0 to 85 °C, EN=1, VSEL=LLC=TEN=PCL=ITEST=TTX=AUX=0, R_{SEL} = 11 kΩ, DSQIN=LOW, V_I = 12 V, I_{OUT} = 50 mA, unless otherwise stated. Typical values are referred to T_J = 25 °C. V_{OUT}=V_{oRX} pin voltage. See software description section for I²C access to the system register)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
F_{SW}	DC-DC converter switching frequency			220		kHz
F_{DETIN}	Tone detector frequency capture range	0.4V_{PP} sine wave(2)	19	22	25	kHz
V_{DETIN}	Tone detector input amplitude	Sine wave signal, 22 kHz	0.3		1.5	V_{PP}
Z_{DETIN}	Tone detector input impedance			150		kΩ
V_{OL}	DSQOUT pin logic LOW	DETIN Tone present, I_{OL}=2mA		0.3	0.5	V
I_{OZ}	DSQOUT pin leakage current	DETIN Tone absent, V_{OH}=6V			10	µA
V_{IL}	DSQIN,TTX,13/18, EXTM pin logic Low				0.8	V
V_{IH}	DSQIN,TTX,13/18, EXTM pin logic High		2			V
I_{IH}	DSQIN,TTX,13/18, EXTM pin input current	V_{IH}=5V		15		µA
I_{OBK}	Output backward current	EN=0, V_{OBK}=21V		-6	-15	mA
T_{SHDN}	Thermal shut-down threshold			150		°C
ΔT_{SHDN}	Thermal shut-down hysteresis			15		°C

1. External signal frequency range in which the EXTM function is guaranteed.
2. Frequency range in which the DETIN function is guaranteed. The V_{PP} level is intended on the LNBOUT (before the C12A/B capacitor. See typical application circuit in *Figure 4*).

Table 9. I²C electrical characteristics (T_J from 0 to 85 °C, V_I = 12 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	LOW Level input voltage	SDA, SCL			0.8	V
V_{IH}	HIGH Level input voltage	SDA, SCL	2			V
I_{IN}	Input current	SDA, SCL, V_I = 0.4 to 4.5 V	-10		10	µA
V_{OL}	Low level output voltage	SDA (open drain), I_{OL} = 6 mA			0.6	V
F_{MAX}	Maximum clock frequency	SCL	400			kHz

Table 10. Address pins characteristics (T_J from 0 to 85 °C, V_I = 12 V)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Section “A” address selection						
$V_{ADDR-A1}$	"0001000(R/W)" Address pin voltage range for section A	R/W bit determines the transmission mode: read (R/W=1) write (R/W=0)	0		0.8	V
$V_{ADDR-A2}$	"0001001(RW)" Address pin voltage range for section A	R/W bit determines the transmission mode: read (R/W=1) write (R/W=0)	2		5	V
Section “B” address selection						
$V_{ADDR-B1}$	"0001010(R/W)" Address pin voltage range for section B	R/W bit determines the transmission mode: read (R/W=1) write (R/W=0)	0		0.8	V
$V_{ADDR-B2}$	"0001011(RW)" Address pin voltage range for section B	R/W bit determines the transmission mode: read (R/W=1) write (R/W=0)	2		5	V

Table 11. Output voltage diagnostic (VMON bit) characteristics of sections A/B
(refer to the typical application circuit in *Figure 4*, T_J from 0 to 85 °C, EN=1, VSEL=LLC=TEN=PCL=ITEST=TTX=AUX=0, R_{SEL} = 11 kΩ, DSQIN=LOW, V_I=12 V, I_O = 50 mA, unless otherwise stated. Typical values are referred to T_J = 25 °C. V_O=V_{oRX} pin voltage. See software description section for I²C access to the system register)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{TH-L}	Diagnostic low threshold at V_O=13.4V typ.	EN=1, VSEL=0 LLC=0	85	90	95	%
V_{TH-L}	Diagnostic low threshold at V_O=18.5V typ.	EN=VSEL=1 LLC=0	84	90	96	%

NB: if the output voltage is lower than the min. value the VMON I²C bit is set to 1.

When VSEL=0: If VMON=0 then V_O>85% of V_O typ.; If VMON=1 then V_O<95% of V_O typ.

When VSEL=1: If VMON=0 then V_O>84% of V_O typ.; If VMON=1 then V_O<96% of V_O typ.

Table 12. Minimum output current diagnostic (IMON bit) characteristics of sections A/B
(refer to the typical application circuit in *Figure 4*, T_J from 0 to 85 °C, EN=1, VSEL=LLC=TEN=PCL=TTX=0, DSQIN=LOW, R_{SEL} = 11 kΩ, V_I = 12 V, I_O = 50 mA, unless otherwise stated. Typical values are referred to T_J = 25 °C. V_O=V_{oRX} pin voltage. See software description section for I²C access to the system register)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{TH}	Minimum current diagnostic threshold	ITEST=1, AUX=0/1	5	12	20	mA
		ITEST=0, AUX=0/1	2.5	6	10	

NB: if the output current is lower than the min. threshold limit the IMON I²C bit is set to 1. If the output current is higher than the max threshold limit the IMON I²C bit is set to 0.

Table 13. 22KHz tone diagnostic (TMON bit) characteristics of sections A/B
(refer to the typical application circuit in *Figure 4*, T_J from 0 to 85 °C, EN=1, VSEL=LLC=TEN=PCL=ITEST=TTX=AUX=0, R_{SEL}=11 kΩ, DSQIN=LOW, V_I=12 V, I_O = 50 mA, unless otherwise stated. Typical values are referred to T_J = 25 °C. See software description section for I²C access to the system register)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
A_{TH-L}	Amplitude diagnostic low threshold	DETIN pin AC coupled	200	300	400	mV
A_{TH-H}	Amplitude diagnostic high threshold	DETIN pin AC coupled	900	1100	1200	mV
F_{TH-L}	Frequency diagnostic low thresholds	DETIN pin AC coupled	13	16.5	20	kHz
F_{TH-H}	Frequency diagnostic high thresholds	DETIN pin AC coupled	24	29.5	38	kHz

NB: if the 22 kHz tone parameters are lower or higher than the above limits the TMON I²C bit is set to 1.

9 Typical performance characteristics

(refer to the typical application circuit in *Figure 4*, T_J from 0 to 85 °C, EN=1, VSEL=LLC=TEN=PCL=ITEST=TTX=AUX=0, R_{SEL} = 11 kΩ, DSQIN=LOW, V_I = 12 V, I_{OUT} = 50 mA, unless otherwise stated. Typical values are referred to T_J = 25 °C, $V_{OUT}=V_{oRX}$)

Figure 8. Output voltage vs temperature

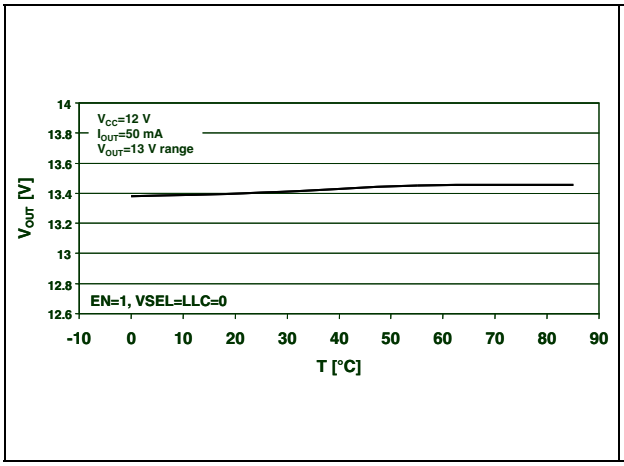


Figure 9. Output voltage vs temperature

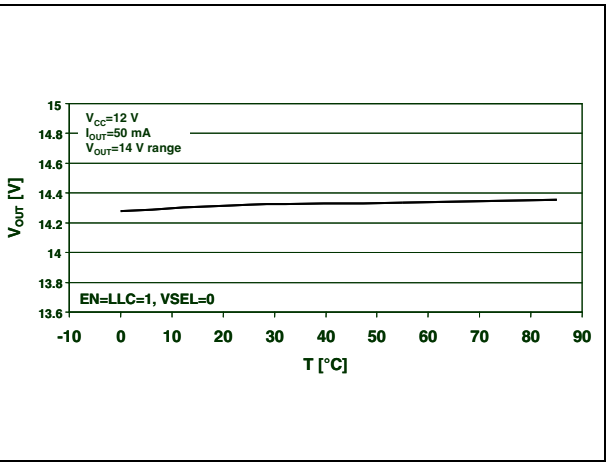


Figure 10. Output voltage vs temperature

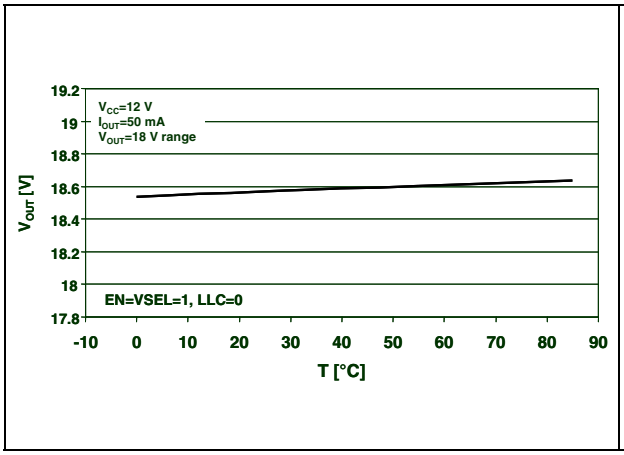


Figure 11. Output voltage vs temperature

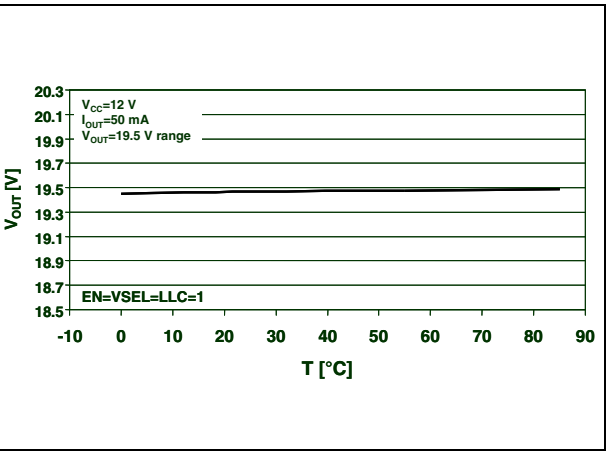


Figure 12. Load regulation vs temperature

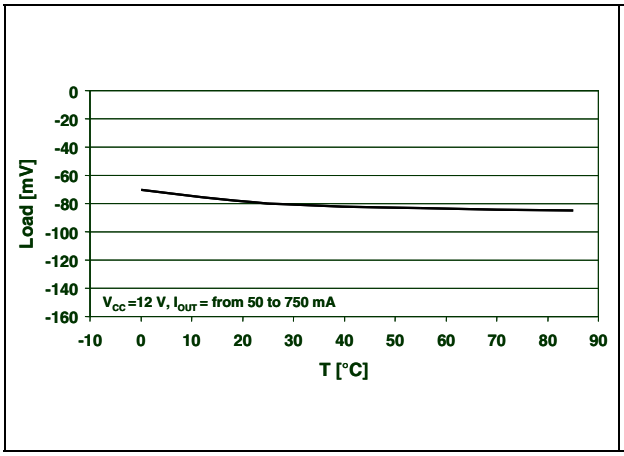


Figure 13. Supply current vs temperature

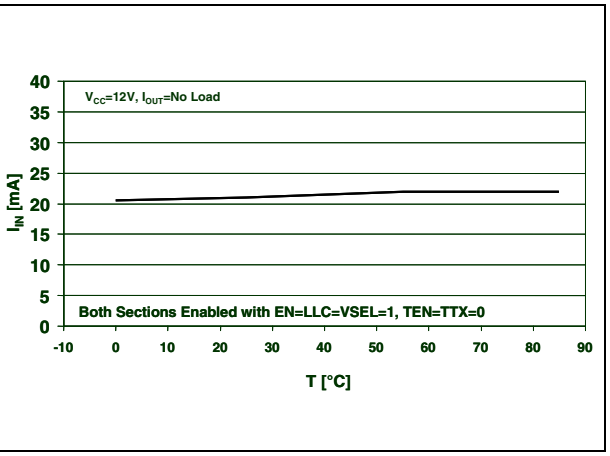


Figure 14. Supply current vs temperature

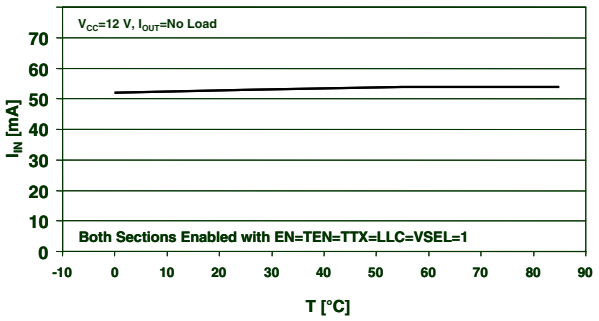


Figure 15. Supply current vs temperature ON time vs temperature

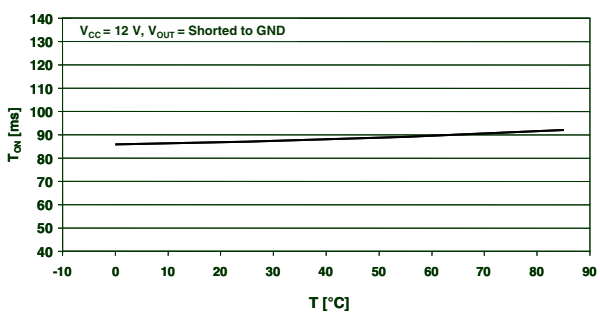


Figure 16. Dynamic overload protection OFF time vs temperature

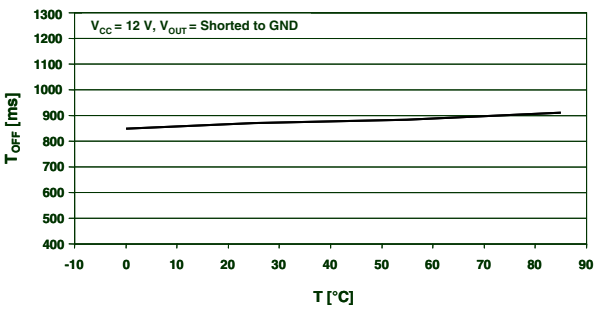


Figure 17. Output current limiting vs R_{SEL}

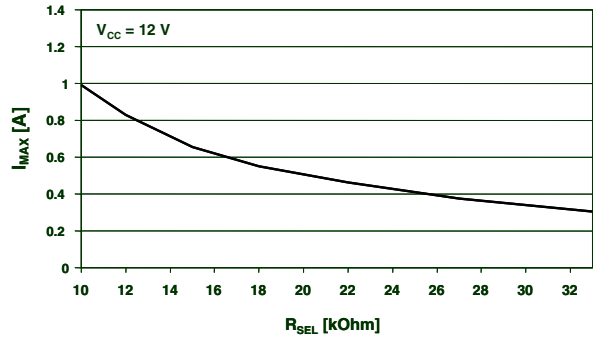


Figure 18. Output current limiting vs temperature

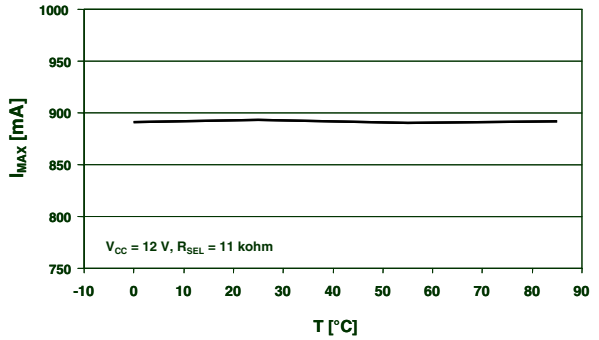


Figure 19. Output current limiting vs temperature

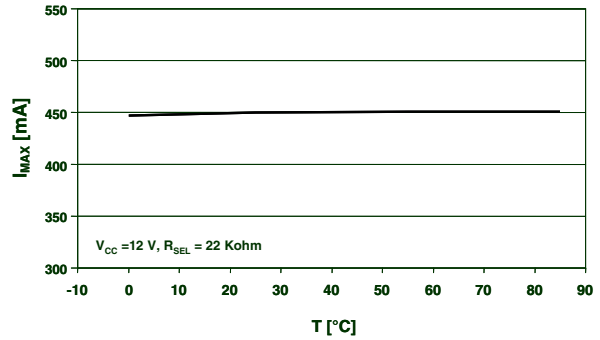


Figure 20. Tone frequency vs temperature

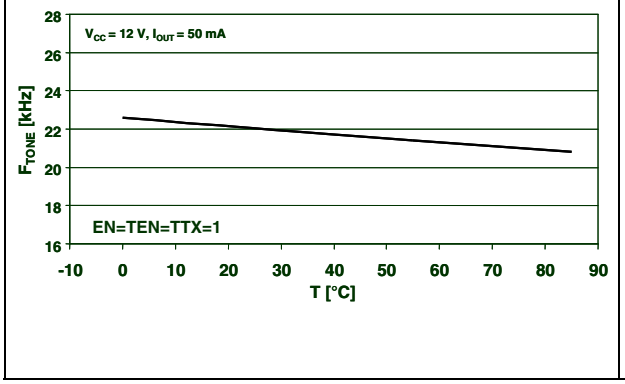


Figure 21. Tone amplitude vs temperature

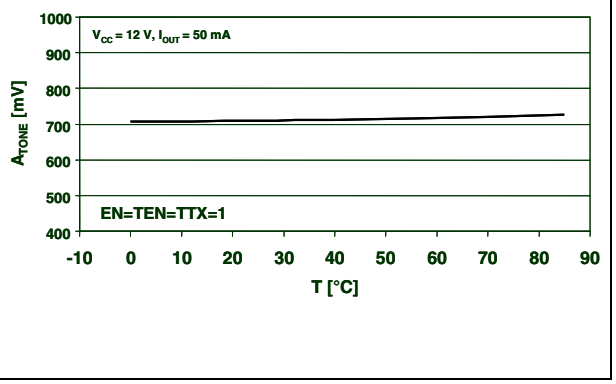


Figure 22. Tone duty cycle vs temperature

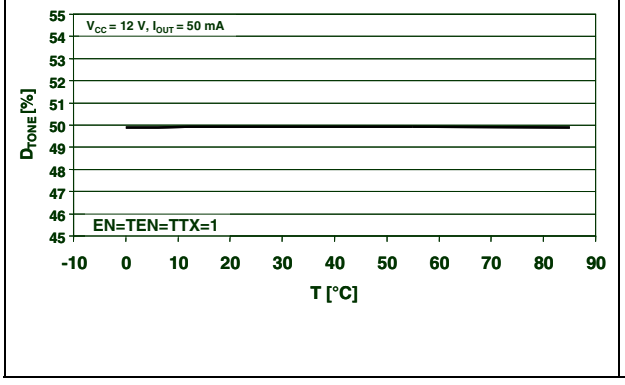


Figure 23. Tone rise time vs temperature

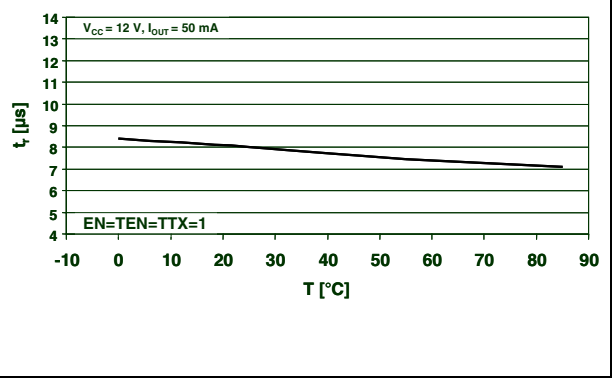


Figure 24. Tone fall time vs temperature

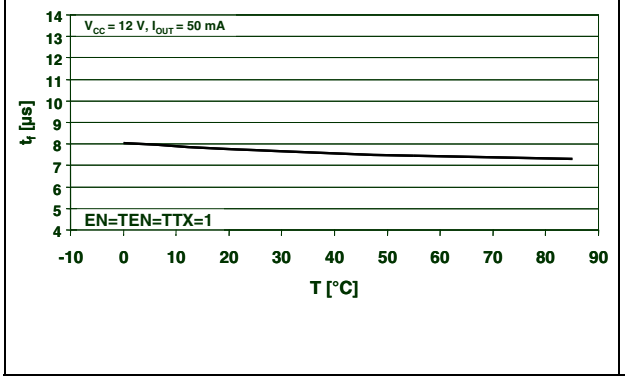


Figure 25. Output backward current vs temperature

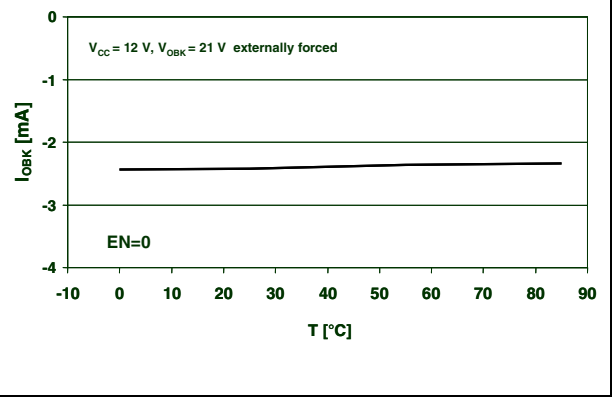


Figure 26. DC-DC converter efficiency vs temperature

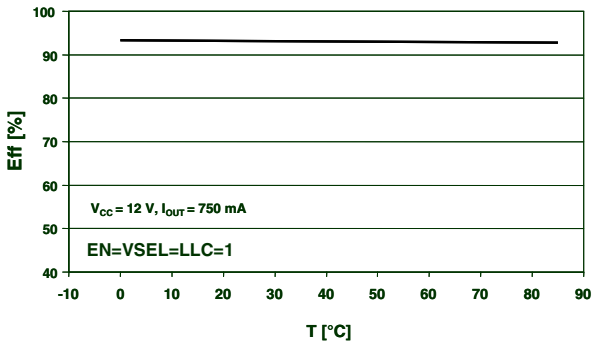


Figure 27. 22 kHz tone waveform

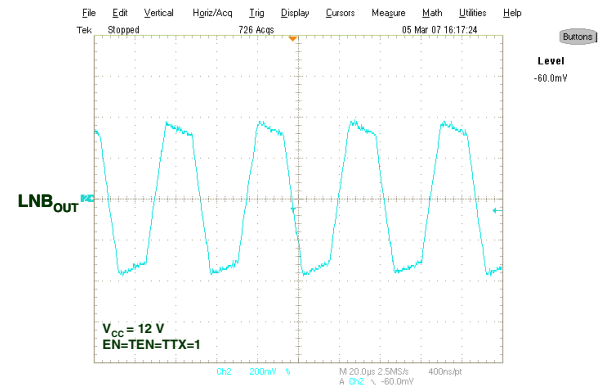


Figure 28. DSQIN tone enable transient response

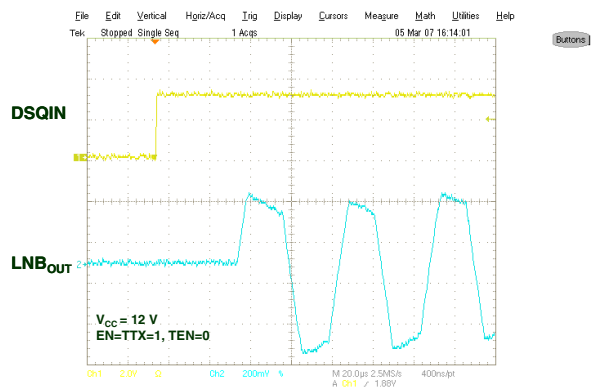
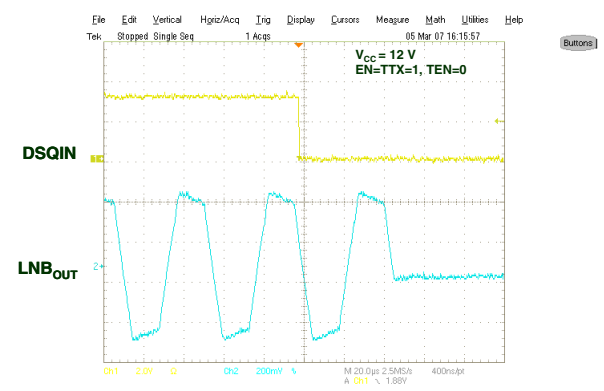


Figure 29. DSQIN tone disable transient response



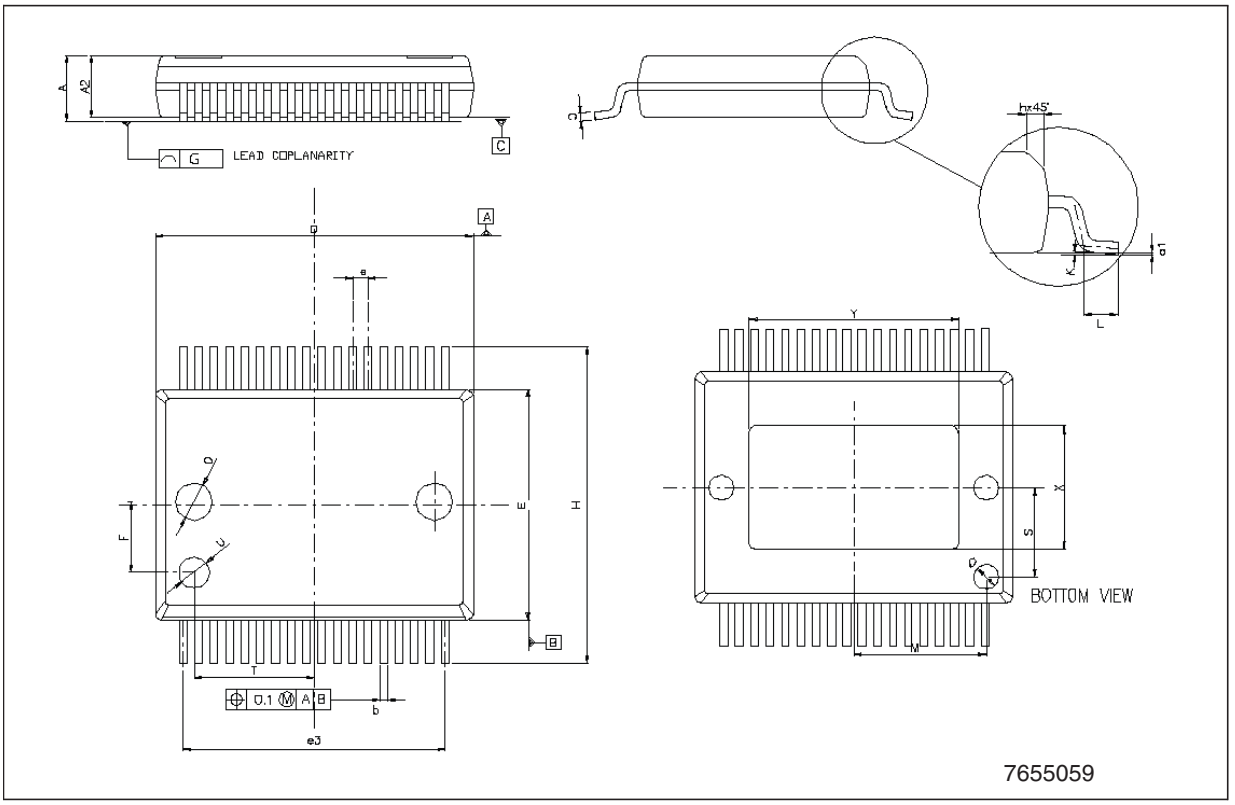
10 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

PowerSSO-36 mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.15		2.47	0.085		0.097
A2	2.15		2.40	0.085		0.094
a1	0		0.075	0		0.003
b	0.18		0.36	0.007		0.014
c	0.23		0.32	0.009		0.013
D	10.10		10.50	0.398		0.413
E	7.4		7.6	0.291		0.299
e		0.5			0.020	
e3		8.5			0.335	
F		2.3			0.091	
G			0.075			0.003
G1			0.06			0.002
H	10.1		10.5	0.398		0.413
h			0.4			0.016
L	0.55		0.85	0.022		0.033
M		4.3			0.169	
N			10°			10°
O		1.2			0.047	
Q		0.8			0.031	
S		2.9			0.114	
T		3.65			0.144	
U		1.0			0.039	
X	4.1		4.7	0.161		0.185
Y	6.5		7.3	0.256		0.287

(1) “D and E” do not include mold flash or protusions - Mold flash or protusions shall not exceed 0.15mm (0.006”)



11 Revision history

Table 14. Document revision history

Date	Revision	Changes
11-Feb-2008	1	Initial release.
27-Aug-2008	2	Modified mechanical data *on page 28*.

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