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## Description

The CXA3796N is a bipolar IC developed as a head amplifier for digital CCD cameras. This IC provides the following functions: correlated double sampling, AGC for the CCD signal, A/D sample and hold, blanking, A/D reference voltage, and an output driver.  
(Applications: CCD cameras)

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## Features

- ◆ High sensitivity made possible by a high-gain AGC amplifier
- ◆ Blanking function provided for the purpose of calibrating the CCD output signal black level
- ◆ Regulator output pin provided for A/D converter reference voltage
- ◆ Built-in sample-and-hold circuits for camera signals required by external A/D converters

### <Changes and improvements from CXA2096N>

- ◆ Selectable maximum gain of AGC amplifier (MAXGAIN mode)
- ◆ Minus gain setting of AGC amplifier (GAINSHIFT mode)
- ◆ CCDLEVEL output blanking function
- ◆ Input dynamic range expansion
- ◆ Noise characteristics improvement

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## Package

24-pin SSOP (Plastic)

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## Structure

Bipolar silicon monolithic IC

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**Absolute Maximum Ratings**

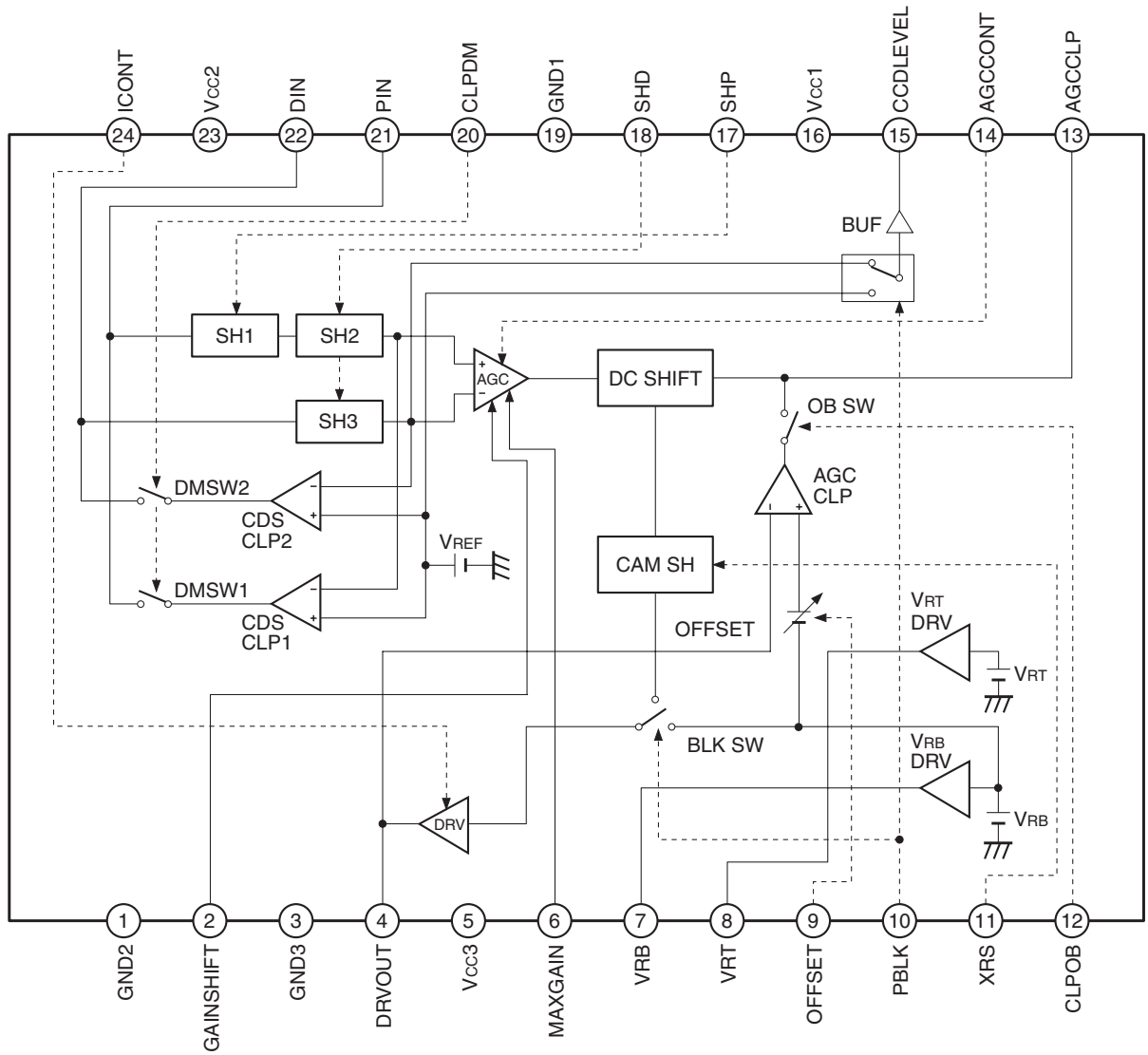
◆ Supply voltage	V <sub>CC</sub>	5.5	V
◆ Operating temperature	T <sub>opr</sub>	-20 to +75	°C
◆ Storage temperature	T <sub>stg</sub>	-65 to +150	°C
◆ Allowable power dissipation	P <sub>D</sub>	417	mW

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**Operating Conditions**

◆ Supply voltage	V <sub>CC1, 2, 3</sub>	3.0 to 3.6	V
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Block Diagram and Pin Configuration


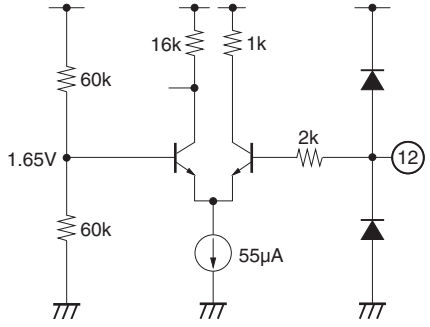
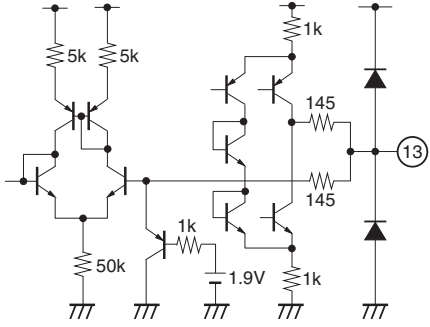
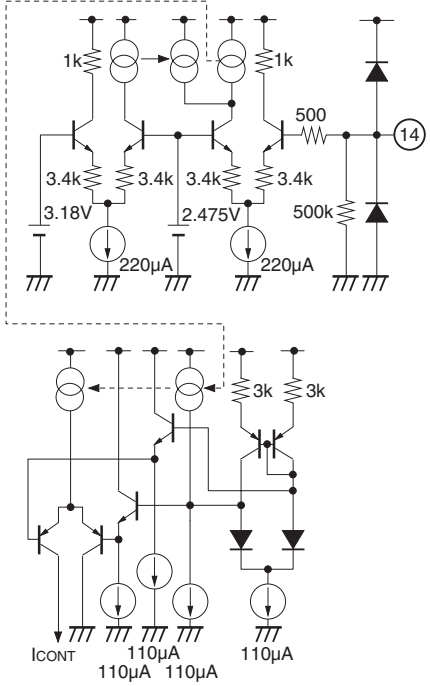


Pin Description

(Vcc1, 2, 3 = 3.3V)

Pin No.	Symbol	I/O	Pin voltage	Equivalent circuit	Description
1 3 19	GND2 GND3 GND1	—	GND		Ground.
2	GAINSHIFT	I	Gain shifted according to the following setting. Vcc to 0.7Vcc: 0dB OPEN: -3dB 0.3Vcc to GND: -6dB		Gain shift.
4	DRVOUT	O	V <sub>RB</sub> to V <sub>RB</sub> + 110mV		Driver output for A/D converter capable of direct DC coupling capacitor.  Dynamic range = 1.07Vp-p.
5 16 23	Vcc3 Vcc1 Vcc2	—	Vcc		Power supply.
6	MAXGAIN	I	Vcc to 0.7Vcc: 34dB OPEN: 26dB 0.3Vcc to GND: 30dB * AGCCONT = 3.0V		MAXGAIN.

Pin No.	Symbol	I/O	Pin voltage	Equivalent circuit	Description
7	VRB	O	1.485V (0.45V <sub>CC</sub> )		<p>1.485V regulator output.</p> <p>Be sure to decouple this pin near the IC pins to prevent the oscillation and external noise when this pin is not used. (Recommended capacitor value: 4.7µF)</p>
8	VRT	O	2.585V (0.783V <sub>CC</sub> )		<p>2.585V regulator output.</p> <p>Be sure to decouple this pin near the IC pins to prevent the oscillation and external noise when this pin is not used. (Recommended capacitor value: 4.7µF)</p>
9	OFFSET	I	1.65 to 3.3V & 0V		<p>Controls the output offset.</p> <p>When 3.3V: V<sub>RB</sub> + 0mV When 1.65V: V<sub>RB</sub> + 110mV</p> <p>When 0V (preset mode): V<sub>RB</sub> + 40mV</p>
10	PBLK	I	V <sub>TH</sub> = 1.65V Active: Low		<p>Camera signal preblanking pulse input.</p> <p>Active when Low. Calibrates the black level of the AGC output waveform. When PBLK is Low, the DRVOUT potential is forced to V<sub>RB</sub>.</p>
11	XRS	I	V <sub>TH</sub> = 0.74V Sampling		<p>Camera signal sample-and-hold pulse input.</p>

Pin No.	Symbol	I/O	Pin voltage	Equivalent circuit	Description
12	CLPOB	I	$V_{TH} = 1.65V$  Active: Low		Clamp pulse input used to clamp the optical black portion of the camera signal after it passes through the AGC amplifier.
13	AGCCLP	O	Approximately 1.4V		AGC clamp capacitor. (Recommended value: 0.1µF)
14	AGCCONT	I	1.65 to 3.3V (0.5V <sub>cc</sub> to 1.0V <sub>cc</sub> )		AGC gain control input.  When 1.65V: -1 dB (Minimum gain) When 3.3V: 31.5 dB (Maximum gain)  ♦ MAXGAIN = OPEN ♦ GAINSHIFT = V <sub>cc</sub> * Gain values can be changed by setting two pins shown above.



Electrical Characteristics

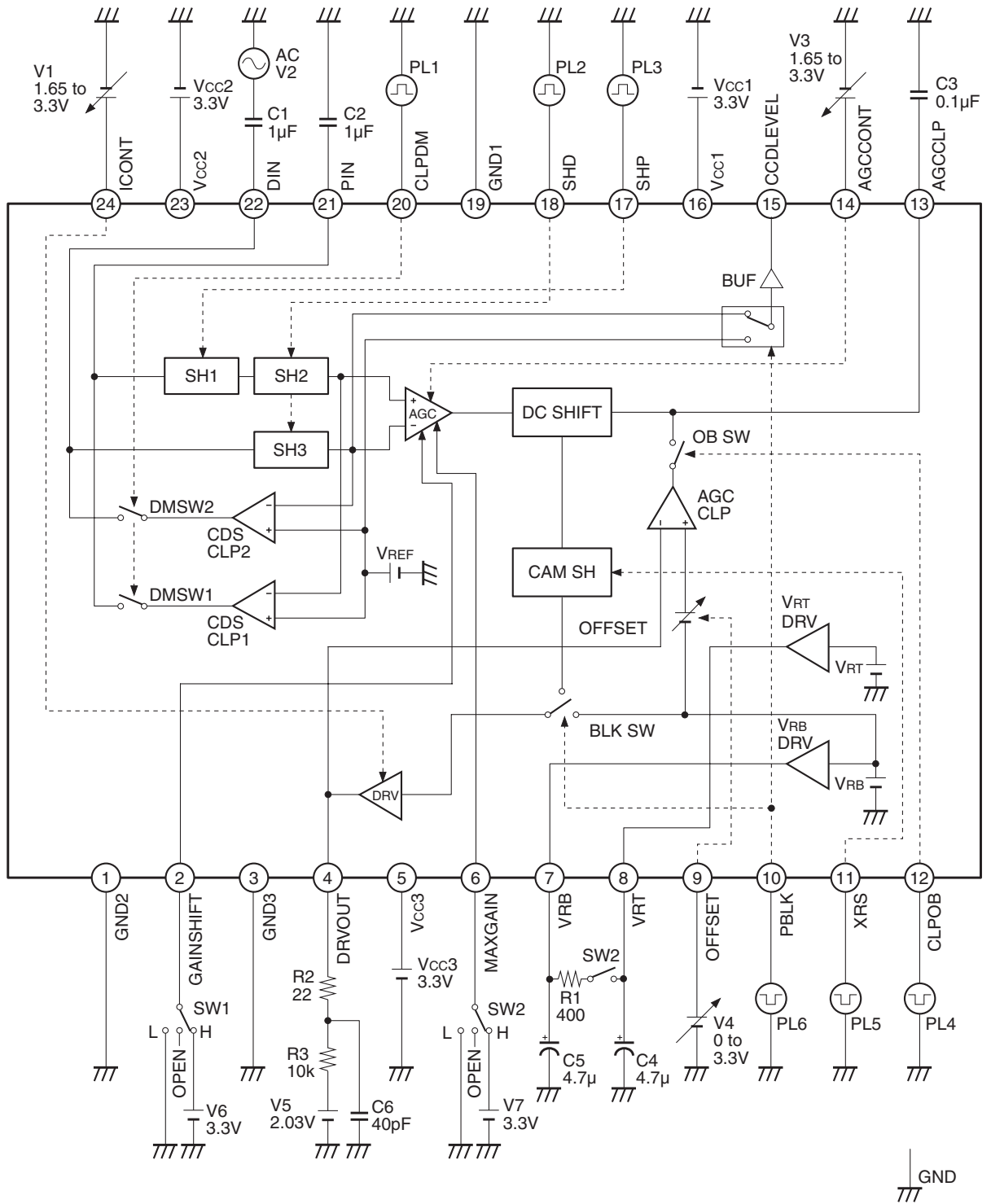
(Ta = 25°C, Vcc1, 2, 3 = 3.3V)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption	Vcc = 3.3V	I <sub>DC</sub>	V <sub>AGCCONT</sub> = 1.65V, open between V <sub>RT</sub> and V <sub>RB</sub> MAXGAIN = OPEN, GAINSHIFT = V <sub>CC</sub> I <sub>CONT</sub> = 3.3V, SHP, SHD = Duty75% (H:L = 3:1)	33	45.7	65.6	mA
	Vcc = 3.0V	I <sub>DC30</sub>	V <sub>AGCCONT</sub> = 1.5V, open between V <sub>RT</sub> and V <sub>RB</sub> MAXGAIN = OPEN, GAINSHIFT = V <sub>CC</sub> I <sub>CONT</sub> = 3.0V, SHP, SHD = Duty75% (H:L = 3:1)	29.5	41.3	59	
AGC	MAXGAIN1	A CONT max.1	DIN = 1μs, 15 mVp-p pulse V <sub>AGCCONT</sub> = 3.0V, I <sub>CONT</sub> = 3.3V MAXGAIN = V <sub>CC</sub> , GAINSHIFT = V <sub>CC</sub>	31	34	37	dB
	MAXGAIN2	A CONT max.2	DIN = 1μs, 20 mVp-p pulse V <sub>AGCCONT</sub> = 3.0V, I <sub>CONT</sub> = 3.3V MAXGAIN = GND, GAINSHIFT = V <sub>CC</sub>	27	30	33	
	MAXGAIN3	A CONT max.3	DIN = 1μs, 30 mVp-p pulse V <sub>AGCCONT</sub> = 3.0V, I <sub>CONT</sub> = 3.3V MAXGAIN = OPEN, GAINSHIFT = V <sub>CC</sub>	23	26	29	
	GAINSHIFT1	A CONT min.1	DIN = 1μs, 500 mVp-p pulse V <sub>AGCCONT</sub> = 1.65V, I <sub>CONT</sub> = 3.3V MAXGAIN = OPEN, GAINSHIFT = V <sub>CC</sub>	—	-0.8	1.4	
	GAINSHIFT2	A CONT min.2	DIN = 1μs, 500 mVp-p pulse V <sub>AGCCONT</sub> = 1.65V, I <sub>CONT</sub> = 3.3V MAXGAIN = OPEN, GAINSHIFT = OPEN	—	-3.6	-1	
	GAINSHIFT3	A CONT min.3	DIN = 1μs, 500 mVp-p pulse V <sub>AGCCONT</sub> = 1.65V, I <sub>CONT</sub> = 3.3V MAXGAIN = OPEN, GAINSHIFT = GND	—	-6.5	-3.5	
	Gain variable width 1	AGC G1	A CONT max.1 – A CONT min.1	29.6	34.8	—	
	Gain variable width 2	AGC G2	A CONT max.2 – A CONT min.1	25.6	30.8	—	
	Gain variable width 3	AGC G3	A CONT max.3 – A CONT min.1	21.6	26.8	—	
	Gain variable width 4	AGC G4	A CONT max.1 – A CONT min.2	32	37.6	—	
	Gain variable width 5	AGC G5	A CONT max.2 – A CONT min.2	28	33.6	—	
Gain variable width 6	AGC G6	A CONT max.3 – A CONT min.2	24	29.6	—		
Gain variable width 7	AGC G7	A CONT max.1 – A CONT min.3	34.5	40.5	—		
Gain variable width 8	AGC G8	A CONT max.2 – A CONT min.3	30.5	36.5	—		
Gain variable width 9	AGC G9	A CONT max.3 – A CONT min.3	26.5	32.5	—		



Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
AGC	Dynamic range Max.	AGCmax.D	V <sub>AGCCONT</sub> = 3.3V MAXGAIN = OPEN, GAINSHIFT = V <sub>CC</sub> At the level when DRVOUT output signal is saturated	0.88	1.07	—	V
	Dynamic range Typ.	AGCtyp.D	V <sub>AGCCONT</sub> = 2.2V MAXGAIN = OPEN, GAINSHIFT = V <sub>CC</sub> At the level when DRVOUT output signal is saturated	0.88	1.07	—	V
DRV	Offset High	CAOF high	OFFSET = 1.65V	88	115	—	mV
	Offset Low	CAOF low	OFFSET = 3.3V	—	3	10	
	Offset Preset	CAOF pre	OFFSET = 0V	30	41	55	
REF	V <sub>RTDC</sub> level	VRTO	400Ωload	2535	2585	2635	mV
	V <sub>RBDC</sub> level	VRBO	400Ωload	1435	1485	1535	
	V <sub>RT</sub> – V <sub>RB</sub>	ΔVR	400Ωload	1045	1087	1155	
BLK	Offset	BLKOF1	BLKOF (PBLK = 3.3V) – BLKOF (PBLK = 0V) I <sub>CONT</sub> = 3.3V	–15	2	30	mV
SH3	Dynamic range	SH3 D	DIN = 1μs, 1.1Vp-p pulse	0.9	1	—	V

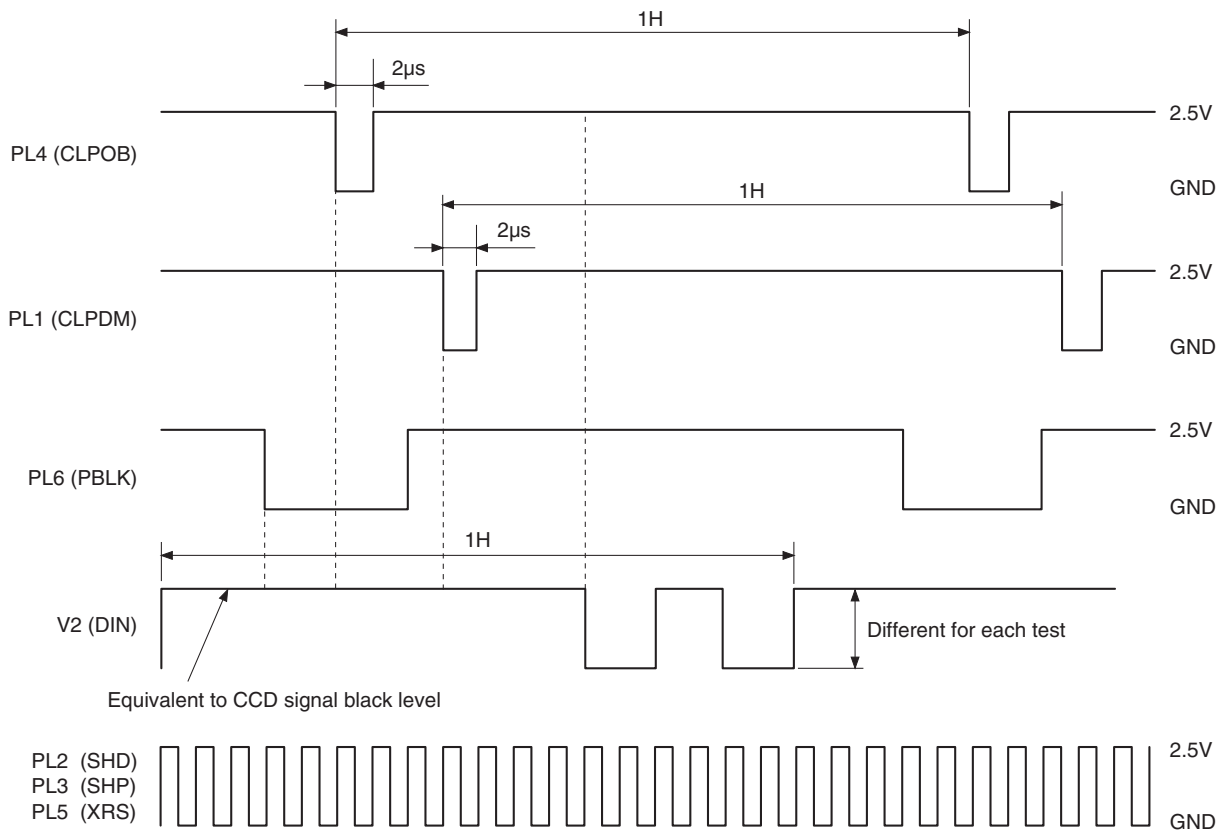
Electrical Characteristics Measurement Circuit



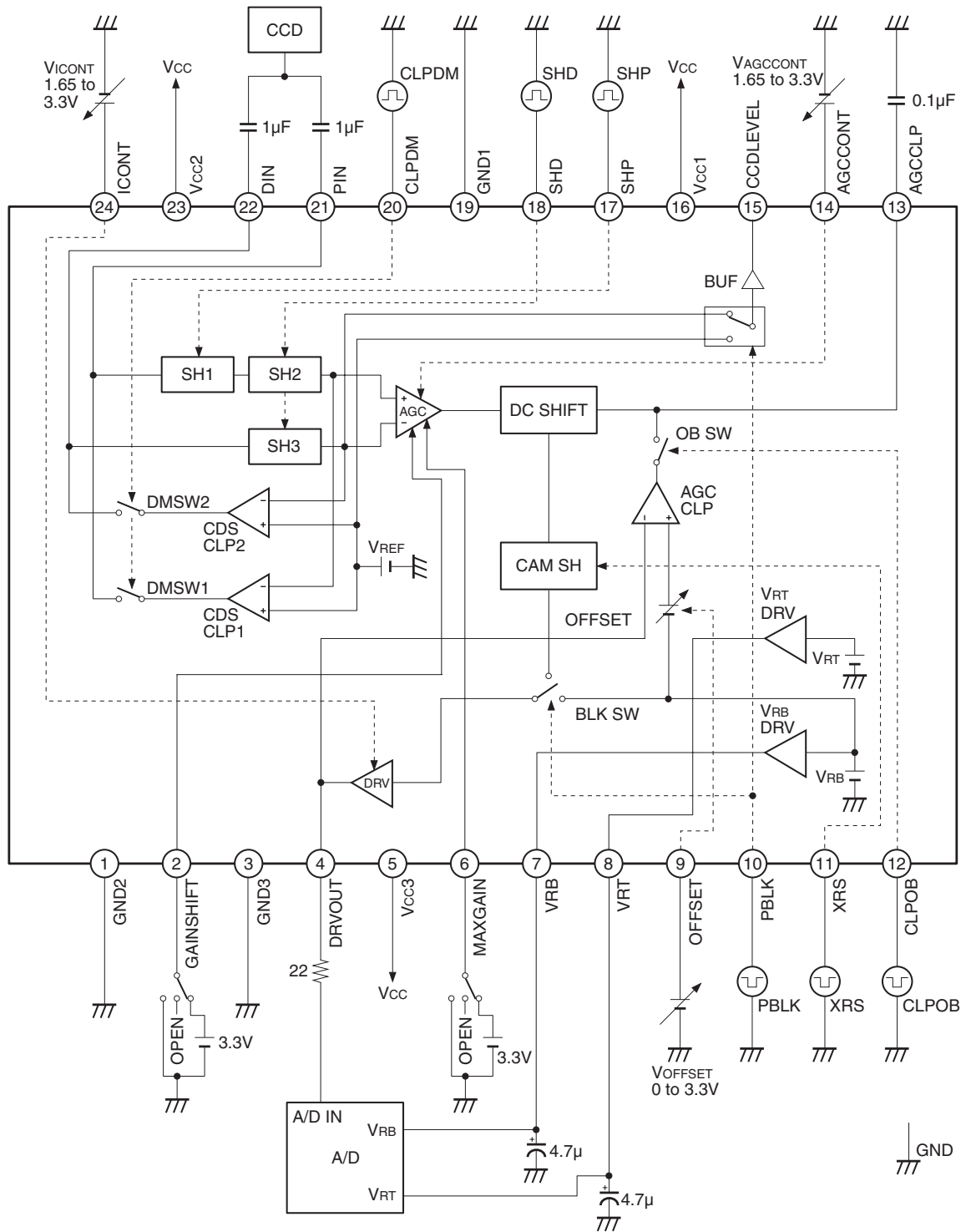
SW1	GAINSHIFT
H	0dB mode
OPEN	-3dB mode
L	-6dB mode

SW2	MAXGAIN
H	34dB (VAGCCONT = 3.0V)
OPEN	26dB (VAGCCONT = 3.0V)
L	30dB (VAGCCONT = 3.0V)

Measurement Timing Chart



Application Circuit



SW1	GAINSHIFT
H	0dB mode
OPEN	-3dB mode
L	-6dB mode

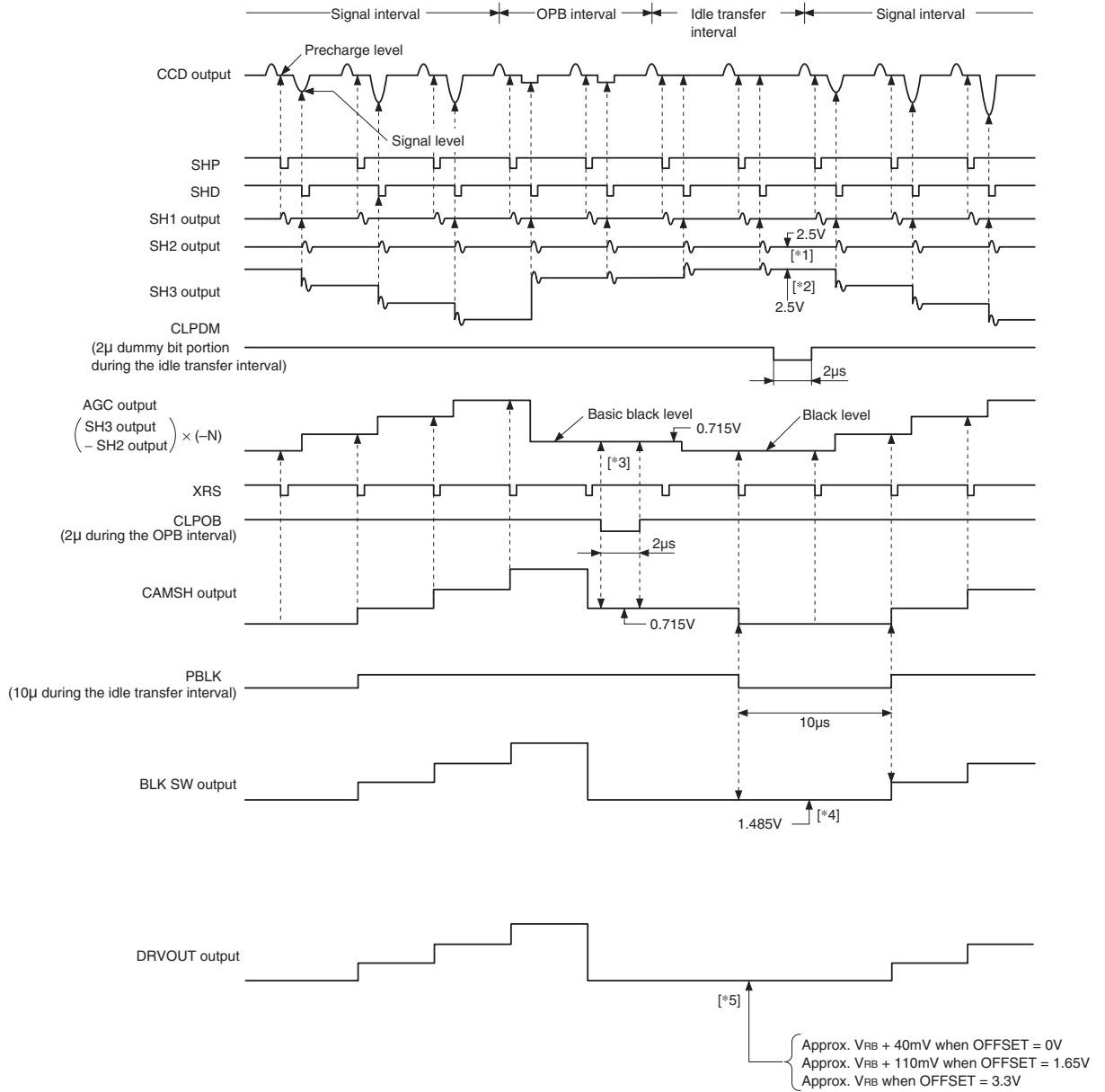
SW2	MAXGAIN
H	34dB (VAGCCONT = 3.0V)
OPEN	26dB (VAGCCONT = 3.0V)
L	30dB (VAGCCONT = 3.0V)

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Description of Operation

Refer to the Block Diagram.

Timing Chart (when Vcc = 3.3 V)



**CDS (SH1, SH2, SH3):**

The CCD signal from the CCD image sensor is input to PIN and DIN where correlated double sampling (CDS) is performed by SH1, SH2 and SH3. The precharge level of the CCD output signal is sampled, held and output by the SH2 output, and the signal level is sampled, held and output by the SH3 output. SH1 and SH2 are the sample-and-hold circuits for the precharge level; SH3 is the sample-and-hold circuit for the signal level.

**CDSCLP 1, 2:**

CDSCLP1 and 2 stabilize the input signal DC level, clamp (CLPDM) the input signal during the idle transfer interval for the purpose of eliminating the AGC input offset, and adjust the DC level ([\*1], [\*2]) of SH2 and SH3 in line with  $V_{REF}$ . CDSCLP1 is the clamp circuit for the precharge level, and CDSCLP2 is the clamp circuit for the signal level.

**AGC:**

AGC is the gain control amplifier for the camera signal.

The gain can be varied from  $-1$  to  $+31$ dB (when MAXGAIN = OPEN, GAINSHIFT =  $V_{CC}$ ) by adjusting the AGCCONT voltage control  $V_{AGCCONT}$  from 1.65 to 3.3V.

\* Gain width can be changed by MAXGAIN =  $V_{CC}/OPEN/GND$ , GAINSHIFT =  $V_{CC}/OPEN/GND$  setting.

**CAM SH:**

CAM SH is the sample-and-hold circuit for synchronizing the data read-in timing for the external A/D. Sampling is possible according to the approximately 10ns sampling pulse width input to XRS.

**AGCCLP:**

The basic black level is set ([\*3]) by clamping the AGC output waveform with the CLPOB clock during the OPB interval. When PBLK is High and CLPOB is Low, the clamping circuit operates, adjusting the AGCCLP current so that the DRVOUT potential equals the OFFSET potential (which is determined by the voltage applied to the OFFSET pin), thus setting the AGCCLP potential. The AGCCLP capacitance is connected to the AGCCLP pin.

**DC SHIFT:**

This circuit functions when AGCCLP operates, following the AGCCLP potential and forcing a DC shift of the AGC output waveform OPB interval to the basic black level. When AGCCLP is not operating, the basic black level is maintained at its previous setting.

**BLK SW:**

The black level is calibrated by blanking the black level signal of the AGC output waveform so that it does not fall below the basic black level and replacing the DC potential with  $V_{RB}$ . ([\*4])

The signal is blanked when PBLK is Low.

**OFFSET:**

OFFSET controls the DRV output waveform black level offset.

The offset of the DRVOUT camera signals can be adjusted when a voltage is applied to OFFSET. ([\*5])

The voltage controlled by OFFSET is output as the DRV output DC offset via AGCCLP, DCSHIFT, CAMSH and BLKSW.

When the OFFSET voltage is 1.65 to 3.3V, DRVOUT DC can vary in a linear fashion from  $V_{RB} + 110$ mV to  $V_{RB}$ . In addition, when the OFFSET voltage is 0V, DRVOUT DC is preset to  $V_{RB} + 40$ mV.

**DRV:**

DRV drives the external A/D. The current that flows to the last-stage amplifier in DRV is controlled by applying voltage to the ICONT pin, making it possible to adjust the rise time of the output waveform, which affects the external A/D load capacitance. The variable range is 1.65 to 3.3V, with 1.65V yielding the maximum and 3.3V yielding the minimum. The optimum rise time for the external A/D input capacitance can be selected.

**VRT DRV, VRB DRV:**

These are the external A/D reference voltage drivers. These circuits are connected to A/D V<sub>RT</sub> and V<sub>RB</sub>, supplying 2.585V and 1.485V, respectively, when V<sub>CC</sub> is 3.3V. The IC's internal primary voltage is also generated on the basis of the V<sub>RT</sub> and V<sub>RB</sub> voltage.

**GAINSHIFT:**

AGC gain curve can be shifted by setting GAINSHIFT as follows.

- ◆ When applying V<sub>CC</sub>      0dB shift
- ◆ When OPEN                -3dB shift
- ◆ When GND                 -6dB shift

**MAXGAIN:**

AGC MAX gain can be changed by setting MAXGAIN as follows.

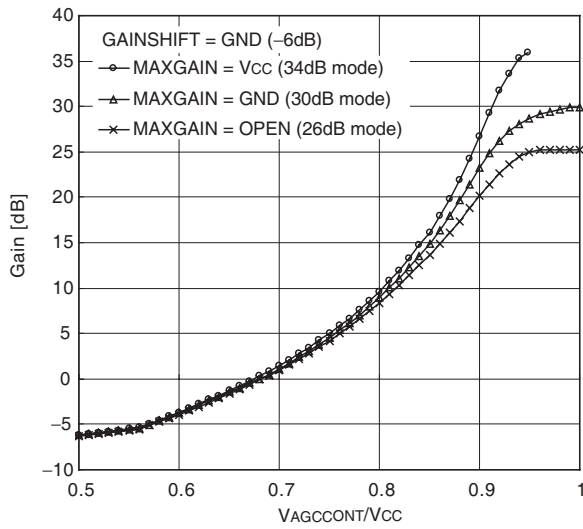
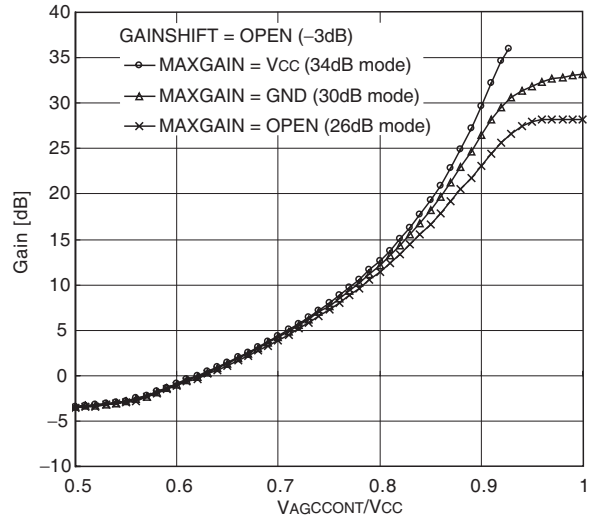
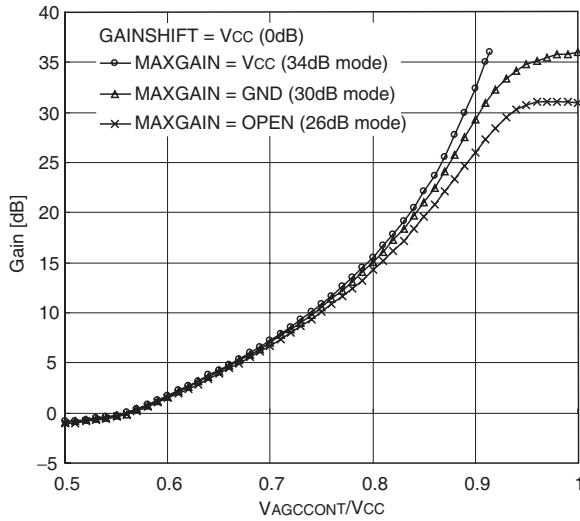
- ◆ When applying V<sub>CC</sub>      34dB \* when V<sub>AGCCOUNT</sub> = 3.0V
- ◆ When OPEN                26dB \* when V<sub>AGCCOUNT</sub> = 3.0V
- ◆ When GND                 30dB \* when V<sub>AGCCOUNT</sub> = 3.0V

**CCDLEVEL BUF:**

This is buffer to monitor SH3 output camera signal and output from CCDLEVEL. SH3 output is output to CCDLEVEL when PBLK = High and internal generation voltage (V<sub>ref</sub>) is output when PBLK = Low.

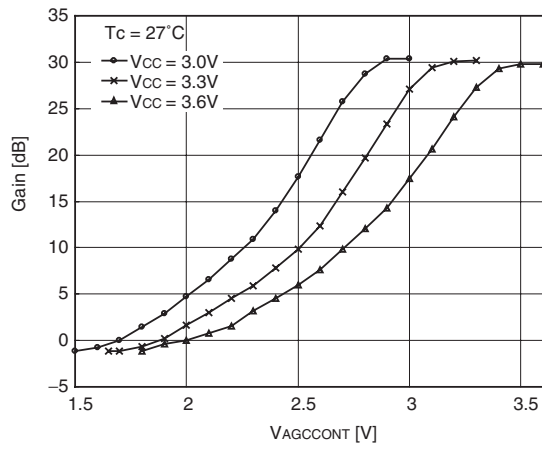
Example of Representative Characteristics

AGCCONT control supply voltage characteristics  
VAGCCONT vs. Gain

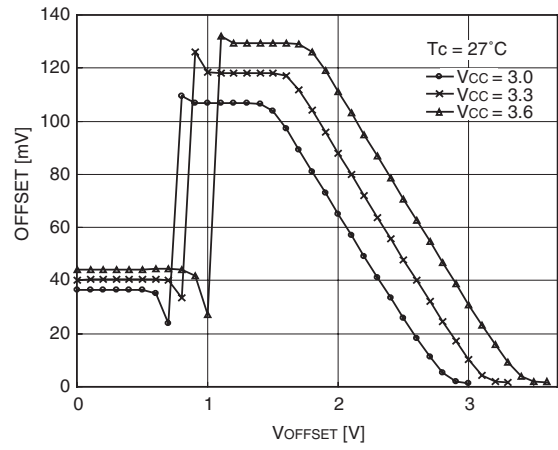




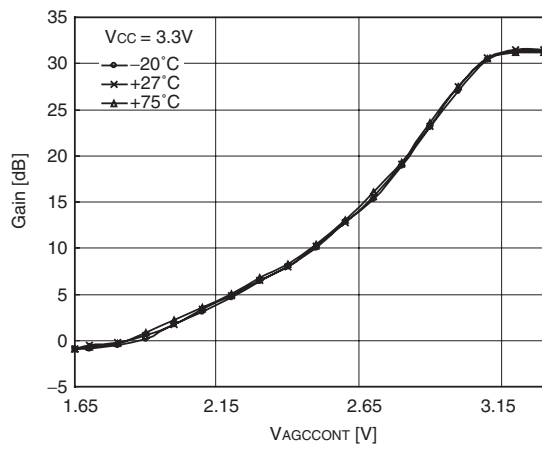
AGCCONT control supply voltage characteristics  
VAGCCONT vs. Gain



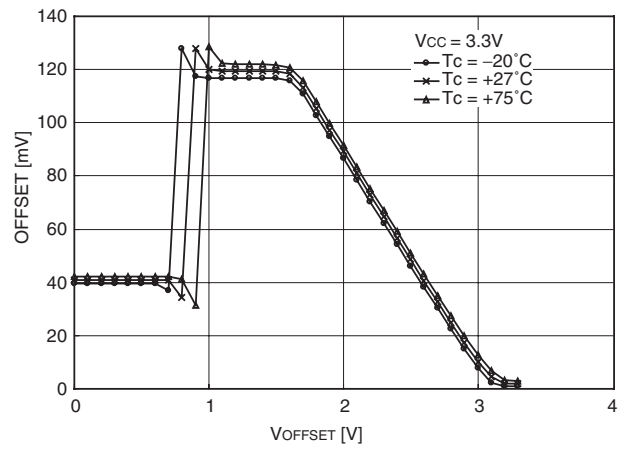
OFFSET control supply voltage characteristics  
VOFFSET vs. OFFSET



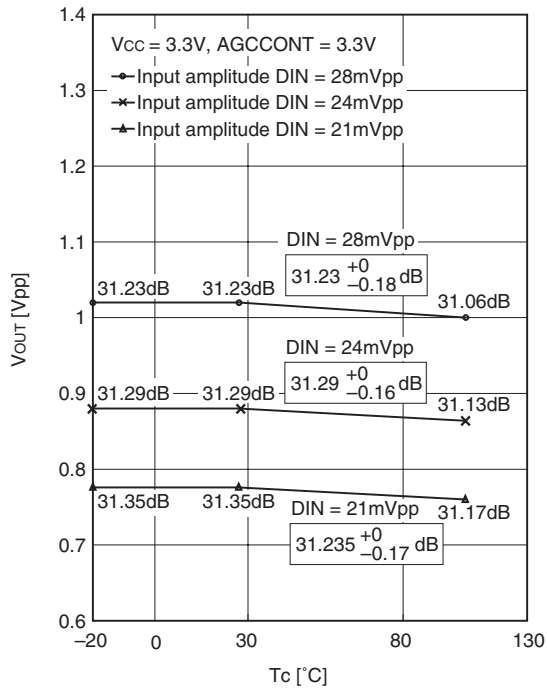
AGCCONT control temperature characteristics  
VAGCCONT vs. Gain



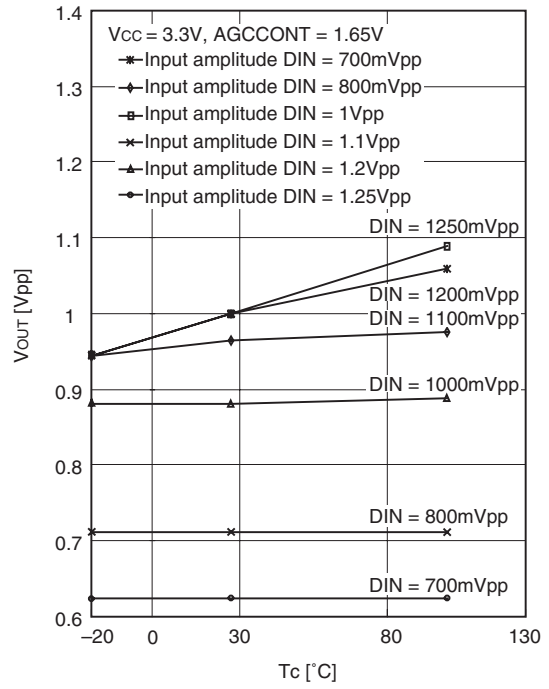
OFFSET control temperature characteristics  
VOFFSET vs. OFFSET



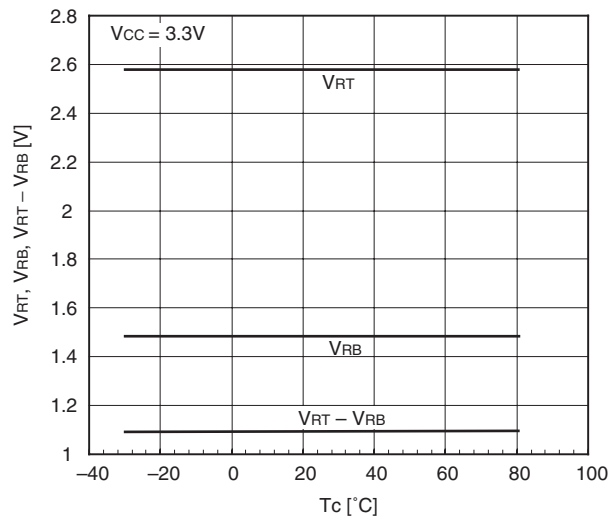
Maximum signal amplitude temperature characteristics (Max. gain)  
Tc vs. Vout



Maximum signal amplitude temperature characteristics (Min. gain)  
Tc vs. Vout



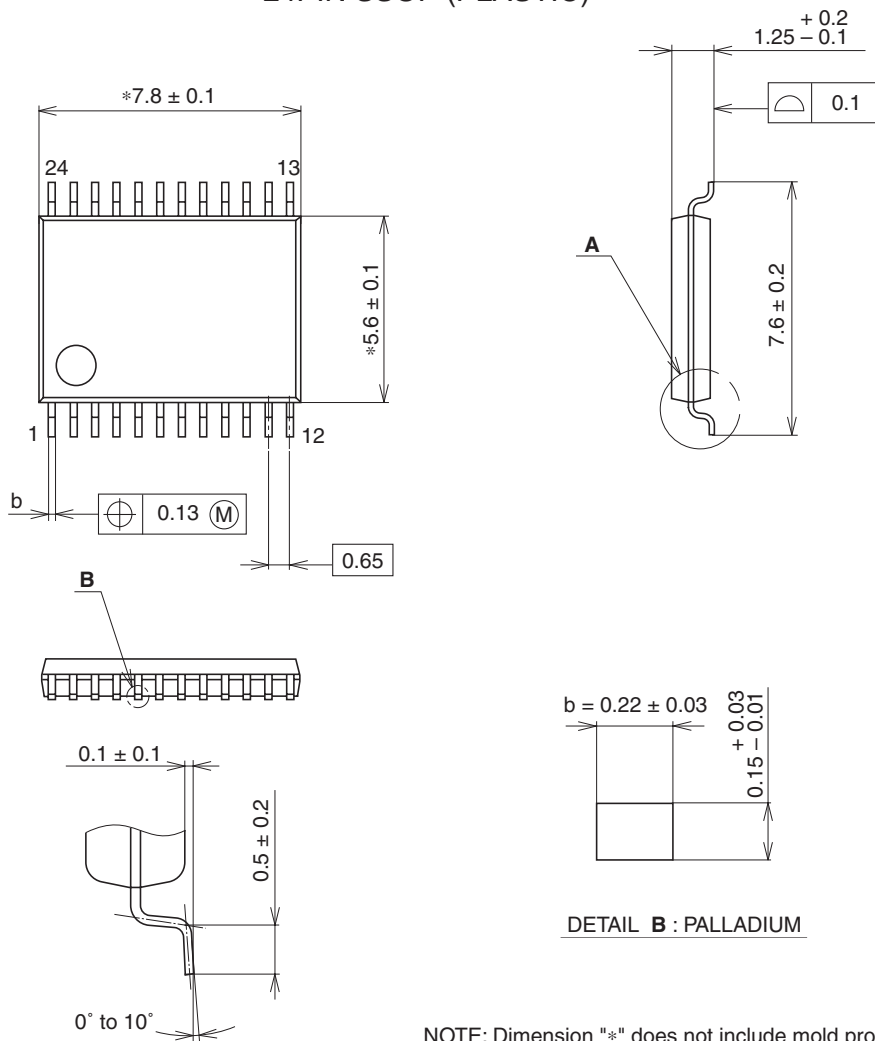
V<sub>RT</sub>, V<sub>RB</sub>, V<sub>RT</sub> - V<sub>RB</sub> temperature characteristics  
Tc vs. V<sub>RT</sub>, V<sub>RB</sub>, V<sub>RT</sub> - V<sub>RB</sub>



Package Outline

(Unit: mm)

24PIN SSOP (PLASTIC)



DETAIL A

DETAIL B : PALLADIUM

NOTE: Dimension "\*" does not include mold protrusion.

PACKAGE STRUCTURE

SONY CODE	SSOP-24P-L01
EIAJ CODE	P-SSOP24-7.8x5.6-0.65
JEDEC CODE	—

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.1g