1:4 CLOCK BUFFER

IDT5V551

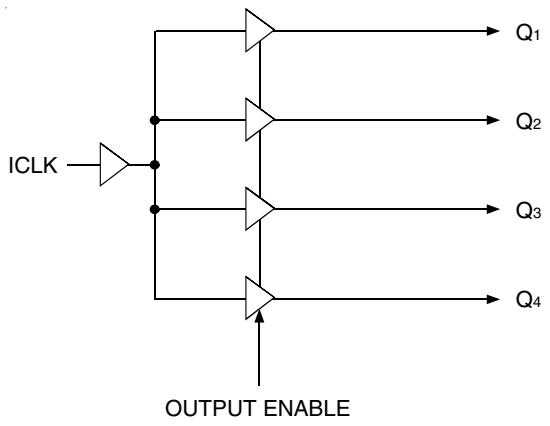
FEATURES:

- **Advanced, low power CMOS process**
- **5V tolerant inputs**
- **Low skew outputs (<250ps)**
- **Input/Output frequency up to 160MHz**
- **Non-inverting output clock**
- **Ideal for networking clocks**
- **Operating voltage of 3V**
- **Output enable mode tri-states outputs**
- **Lead-free packaging available**
- **Available in SOIC package**

DESCRIPTION:

The 5V551 clock driver is built using advanced CMOS technology. This low skew clock driver offers 1:4 fanout. The fanout from a single input reduces loading on the preceding driver and provides an efficient clock distribution network. The 5V551 offers low capacitance inputs. Typical applications are clock and signal distribution.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

SOIC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max.	Unit
V_{DD}	Supply Voltage	–0.5 to +4.6	V
V_{TERM}	All Inputs	–0.5 to +7	V
	All Outputs	–0.5 to V_{DD} + 0.5	
T_A	Ambient Operating Temp	–40 to +85	° C
T_{STG}	Storage Temperature	–65 to +150	° C
T_J	Junction Temperature	150	° C
T_{SOLDER}	Soldering Temperature	260	° C

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

PIN DESCRIPTION

Name	Type	Description
ICLK	Input	Clock Input, internal pull-up resistor
Qn	Output	Clock Outputs
GND	PWR	Connect to Ground
V_{DD}	PWR	Connect to 3.3V
OE	Input	Output Enable. Tri-states outputs when LOW. Internal pull-up resistor.

EXTERNAL COMPONENTS

A minimum number of external components are required for proper operation. A decoupling capacitor of 0.01µF should be connected between V_{DD} on pin 7 and GND on pin 6, as close to the device as possible. A 33Ω series terminating resistor may be used on each clock output if the trace is longer than one inch.

RECOMMENDED OPERATING RANGE

Symbol	Description	Min.	Typ.	Max.	Unit
T_A	Ambient Operating Temperature	–40	—	+85	° C
V_{DD}	Power Supply Voltage (measured in respect to GND)	3	—	3.6	V

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified
T_A = -40°C to +85°C, V_{DD} = 3.3V ± 5%

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage		3.15	—	3.45	V
V_{IH}	Input HIGH Voltage, ICLK(1)		$V_{DD}/2$ + 0.7	—	—	V
V_{IL}	Input LOW Voltage, ICLK(1)		—	—	$V_{DD}/2$ – 0.7	V
V_{IH}	Input HIGH Voltage, OE		2	—	—	V
V_{IL}	Input LOW Voltage, OE		—	—	0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = –25mA	2.4	—	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 25mA	—	—	0.4	V
V_{OH}	Output HIGH Voltage (CMOS)	I_{OH} = –12mA	V_{DD} – 0.4	—	—	V
I_{DD}	Operating Supply Current	No Load, 135MHz	—	18	—	mA
Z_O	Nominal Output Impedance		—	20	—	Ω
R_{PU}	Internal Pull-Up Resistor	ICLK, OE = 0V	—	350	—	kΩ
C_{IN}	Input Capacitance	OE Pin	—	5	—	pF
		ICLK	—	3	—	
I_{OS}	Short Circuit Current		—	±90	—	mA

NOTE:
1. Nominal switching threshold is $V_{DD}/2$.

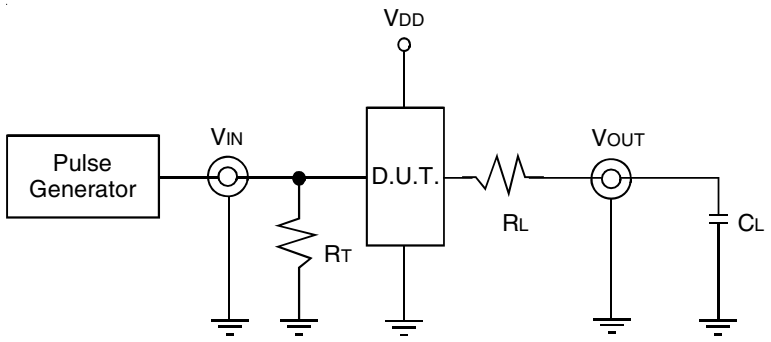
AC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified
T_A = -40°C to +85°C, V_{DD} = 3.3V ± 5%

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
F_{IN}	Input Frequency		0	—	160	MHz
F_{OUT}	Output Frequency[1]	15pF load	—	—	160	MHz
t_{OR}	Output Clock Rise Time	0.8V to 2V	—	—	1.5	ns
t_{OF}	Output Clock Fall Time	2V to 0.8V	—	—	1.5	ns
t_{PD}	Propagation Delay[2]	135MHz	2	4	8	ns
$t_{SK(O)}$	Output to Output Skew[3]	Rising edges at $V_{DD}/2$	—	—	250	ps

NOTES:
1. With external series resistor of 33Ω positioned close to each output pin.
2. With rail-to-rail input clock.
3. Between any two outputs with equal loading.
4. Duty cycle on outputs will match incoming clock duty cycle. Consult IDT for tight duty cycle clock generators.

TEST CIRCUIT

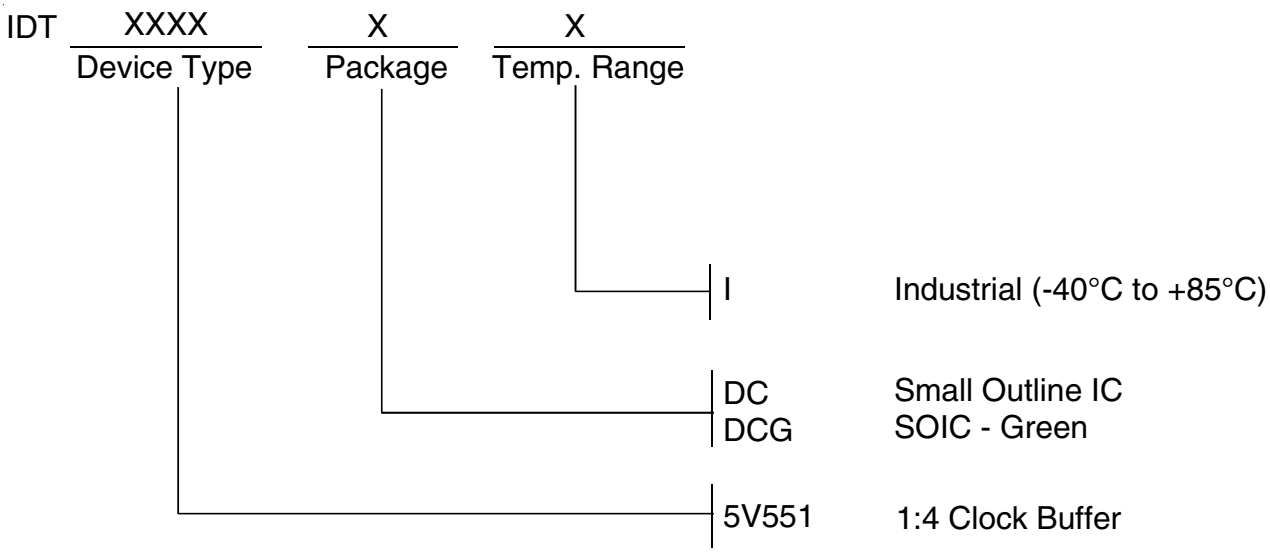


TEST CONDITIONS

Symbol	V_{DD} = 3.3V ± 5%	Unit
C_L	15	pF
R_T	Z_{OUT} of pulse generator	Ω
R_L	33	Ω
t_R/t_F	1 (0V to 3V or 3V to 0V)	ns

DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to the Z_{OUT} of the pulse generator.
t_R/t_F = Rise/Fall time of the input stimulus from the pulse generator.

ORDERING INFORMATION



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