1.8V, 500-MHz, 10-Output JEDEC-Compliant Zero Delay Buffer

Features

- **Operating frequency: 125 MHz to 500 MHz**
- **Supports DDRII SDRAM**
- **1 to 10 differential clock buffer (SSTL_18)**
- **Spread-Spectrum-compatible**
- **Low jitter (cycle-to-cycle): 40 ps**
- **Very low output-to-output skew: 40 ps**
- **Auto power-down feature when input is low**
- **1.8V operation**
- **Fully JEDEC-compliant (JESD 82-8)**
- **52-ball BGA**

Functional Description

The CY2SSTU877 is a high-performance, low-skew, low-jitter zero delay buffer designed to distribute differential clocks in high-speed applications.

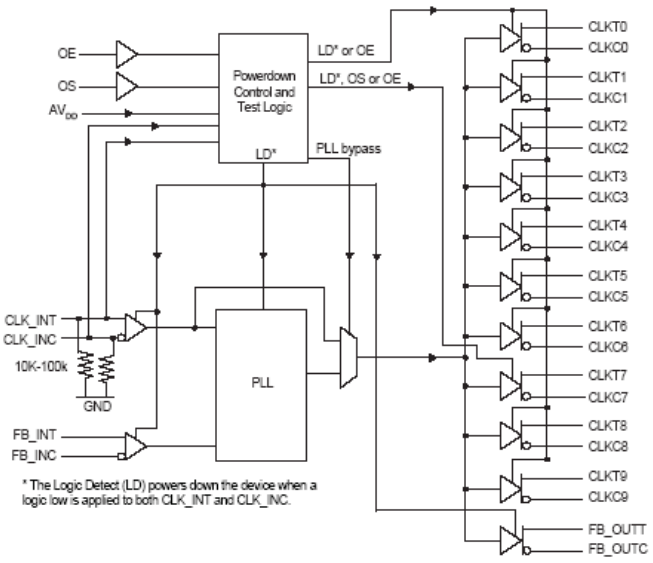
This phase-locked loop (PLL) clock buffer is designed for a V_{DD} of 1.8V, an AV_{DD} of 1.8V and SSTL18 differential data input and output levels. This device is a zero delay buffer that distributes a differential clock input pair (CK, CK#) to ten differential pair of clock outputs (Y[0:9], Y#[0:9]) and one differential pair of feedback clock outputs (FBOUT, FBOUT#).

The input clocks (CK, CK#), the feedback clocks (FBIN, FBIN#), the LVCMOS (OE, OS), and the analog power input (AVDD) control the clock outputs.

The PLL in the CY2SSTU877 clock driver uses the input clocks (CK, CK#) and the feedback clocks (FBIN, FBIN#) to provide high-performance, low-skew, low-jitter output differential clocks (Y[0:9], Y#[0:9]). The CY2SSTU877 is also able to track Spread Spectrum Clocking (SSC) for reduced EMI.

When AVDD is grounded, the PLL is turned off and bypassed for test purposes. When both clock signals (CK, CK#) are logic low, the device will enter a low-power mode. An input logic detection circuit on the differential inputs, independent from the input buffers, will detect the logic low level and perform a low-power state where all outputs, the feedback, and the PLL are OFF. When the inputs transition from both being logic low to being differential signals, the PLL will be turned back on, the inputs and outputs will be enabled and the PLL will obtain phase lock between the feedback clock pair (FBIN, FBIN#) and the input clock pair (CK, CK#) within the specified stabilization time t_L.

Block Diagram



Pin Configuration

	1	2	3	4	5	6
A	CLKT1	CLKT0	CLKC0	CLKC5	CLKT5	CLKT6
B	CLKC1	GND	GND	GND	GND	CLKC6
C	CLKC2	GND	NB	NB	GND	CLKC7
D	CLKT2	VDDQ	VDDQ	VDDQ	OS	CLKT7
E	CLK_INT	VDDQ	NB	NB	VDDQ	FB_INT
F	CLK_INC	VDDQ	NB	NB	OE	FB_INC
G	AGND	VDDQ	VDDQ	VDDQ	VDDQ	FB_OUTC
H	AVDD	GND	NB	NB	GND	FB_OUTT
J	CLKT3	GND	GND	GND	GND	CLKT8
K	CLKC3	CLKC4	CLKT4	CLKT9	CLKC9	CLKC8

52 BGA

Pin Description

Pin No.	Name	Description
G1	AGND	Ground for 1.8V analog supply
H1	AVDD	1.8V analog supply
E1, F1	CLK_INT, CLK_INC	Differential clock input with a (10K–100KΩ) pull-down resistor
E6, F6	FB_INT, FB_INC	Feedback differential clock input
H6, G6	FB_OUTT, FB_OUTC	Feedback differential clock output
B2, B3, B4, B5, C2, C5, H2, H5, J2, J3, J4, J5	GND	Ground
F5	OE	Output enable (ASYNC) for CLKT[0:9] and CLKC [0:9]
D5	OS	Output Select (Tied to GND or VDDQ)
D2, D3, D4, E2, E5, F2, G2, G3, G4, G5	VDDQ	1.8V supply
A2, A1, D1, J1, K3, A5, A6, D6, J6, K4,	CLKT [0:9]	Buffered output of input clock, CLK
A3, B1, C1, K1, K2, A4, B6, C6, K6, K5	CLKC [0:9]	Buffered output of input clock, CLK

Table 1. Function Table

Inputs					Outputs				
AVDD	OE	OS	CLK_INT	CLK_INC	CLKT	CLKC	FB_OUTT	FB_OUTC	PLL
GND	H	X	L	H	L	H	L	H	Bypassed/Off
GND	H	X	H	L	H	L	H	L	Bypassed/Off
GND	L	H	L	H	Lz	Lz	L	H	Bypassed/Off
GND	L	L	H	L	Lz,CLKT7 Active	Lz,CLKC7 Active	H	L	Bypassed/Off
VDD	L	H	L	H	Lz	Lz	L	H	On
VDD	L	L	H	L	Lz,CLKT7 Active	Lz,CLKC7 Active	H	L	On
VDD	H	X	L	H	L	H	L	H	On
VDD	H	X	H	L	H	L	H	L	On
VDD	X	X	L	L	Lz	Lz	Lz	Lz	Off
X	X	X	H	H	Reserved				

Recommended Operating Conditions

Parameter	Description	Condition	Min.	Max.	Unit
T_A (Com.)	Ambient Operating Temp		0	70	°C
V_{DD}, AV_{DD}	Operating Voltage		1.7	1.9	V

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
V_{IN}	Input Voltage Range		–0.5	V_{DDQ} + 0.5	V
V_{OUT}	Output Voltage Range		–0.5	V_{DDQ} + 0.5	V
T_S	Storage Temperature		–65	150	°C
V_{CC}, AV_{CC}	Supply Voltage Range		–0.5	2.5	V
I_{IK}	Input Clamp Current		–50	50	mA
I_{OK}	Output Clamp Current		–50	50	mA
I_O	Continuous Output Current		–50	50	mA
	Continuous Current through V_{DD}/GND		–100	100	mA

DC Electrical Specifications

Parameter	Description	Conditions	Min.	Max.	Unit
V_{IK}	Input Clamping Voltage	I_I = –18 mA		–1.2	V
V_{OD}	Output Differential Voltage		0.5		V
V_{OX}	Output Differential Crossing Voltage		V_{DDQ}/2 – 0.08	V_{DDQ}/2 + 0.08	V
V_{IX}	Input Differential Crossing Voltage		(V_{DDQ}/2) – 0.15	(V_{DDQ}/2) + 0.15	V
V_{ID} DC	Input Differential Voltage (DC Values)		0.3	V_{DDQ} + 0.4	V
V_{ID} AC	Input Differential Voltage (AC Values)		0.6	V_{DDQ} + 0.4	V
V_{IL}	Input Low Voltage	(OE, OS, CLK_INT, CLK_INC)		0.35 * V_{DDQ}	V
V_{IH}	Input High Voltage	(OE, OS, CLK_INT, CLK_INC)	0.65 * V_{DDQ}		V
V_{OL}	Output Low Voltage	I_{OL} = 100 µA		0.1	V
		I_{OL} = 9 mA		0.6	V
V_{OH}	Output High Voltage	I_{OH} = –100 µA	V_{DDQ} – 0.2		V
		I_{OH} = –9 mA	1.1		V
I_{IH}	Input High Current	V_{IN} = V_{DDQ} or GND	–250	250	µA
I_{IL}	Input Low Current	V_{IN} = V_{DDQ}or GND	–10	10	µA
I_{ODL}	Output disabled low current	V_{ODL}= 100 mV OE = GND	100		µA
I_{DDLD}	Static Supply current	I_{DDQ} + I_{ADD}, CLK_INT = CLK_INC = GND		500	µA
I_{DD}	Dynamic Supply Current	C_L = 0 @ 270 MHz		300	mA
I_{OH}	Output High Current			–9	mA
I_{OL}	Output Low Current			9	mA
C_{IN}	Input Capacitance	(Input Capacitance of CLK_INT, CLK_INC, FB_INT, FB_INC) V_I = V_{DDQ} or GND	2	3	pF
C_{OUT}					pF
$C_{IN(DELTA)}$		Ci(delta) (CLK_INT, CLK_INC, FB_INT, FB_INC) V_I = V_{DDQ} or GND	–0.25	0.25	pF

AC Timing Specifications

Parameter	Description	Conditions	Min.	Max.	Unit
F_{CLK}[1,2]	Clock Frequency (Max)	Room temp and nominal V_{DDQ}	125	500	MHz
	Clock Frequency (Application)	Room temp and nominal V_{DDQ}	250	500	MHz
T_{DC}	Input Duty Cycle		40	60	%
T_{ODC}	Output Duty Cycle		48	52	%
T_{LOCK}	PLL Lock Time		–	15	µs
T_{OENB}	Output Enable Time	OE to any CLKT/ CLKC[0:9]	–	8	ns
T_{ODIS}	Output Disable Time	OE to any CLKT/ CLKC[0:9]	–	8	ns
Tjitt (cc)	Cycle-to-cycle jitter		–40	40	ps
Tjit (Period)	Period jitter		–30	30	ps
Tjit (H-Period)	Half Period Cycle-to-cycle jitter	Above 270 MHz	–45	45	ps
		Below 270 MHz	–60	60	ps
$T_{(\phi)}$	Static Phase Offset	Average 1000 cycles	–50	50	ps
$T_{(\phi)DYN}$	Dynamic Phase Offset		–40	40	ps
T_{SKEW}	Clock Skew		–	40	ps
$S_{LR(O)}$	Output Slew Rate	CLKT/ CLKC[0:9], FB_OUTT, FB_OUTC	1.5	4	V/ns
$S_{LR(I)}$	Input Slew Rate	CLK_INT, CLK_INC, FB_INT, FB_INC	1	4	V/ns
		OE	0.5		V/ns

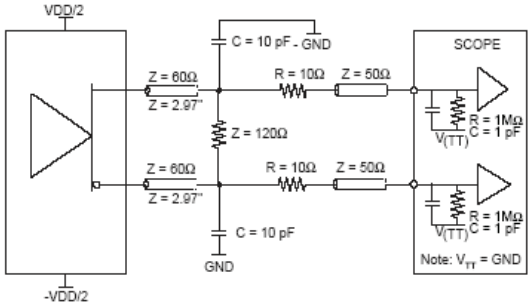


Figure 1. Test Loads for Timing Measurement

Notes:
1. Operating clock frequency indicates a range over which the PLL must be able to lock, but in which it is not required to meet the other timing parameters (used for low speed system debug).
2. Application clock frequency indicates a range over which the PLL must meet all timing requirements.

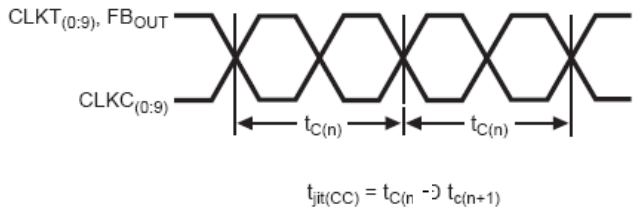


Figure 2. Cycle-to-cycle Jitter

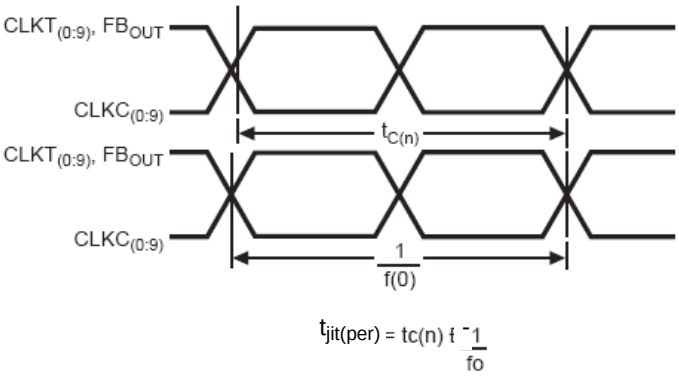


Figure 3. Period Jitter

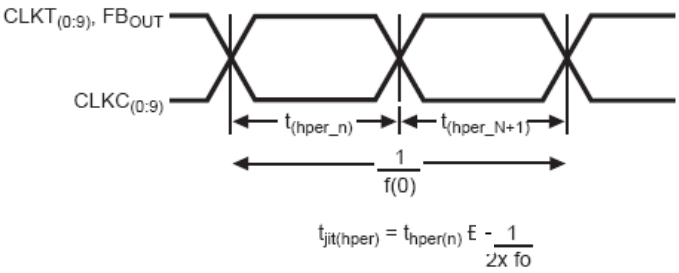


Figure 4. Half Period Jitter

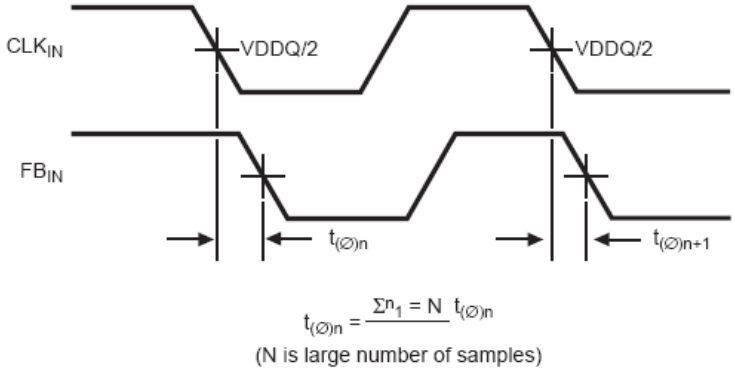


Figure 5. Static Phase Offset (Differential Probes)

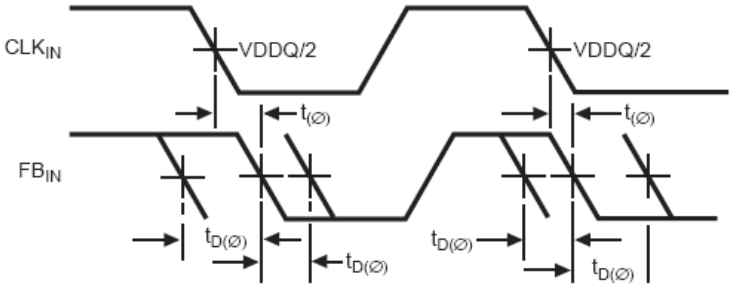


Figure 6. Dynamic Phase Offset (Differential Probes)

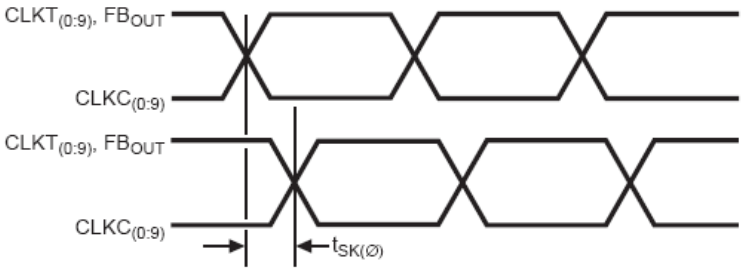


Figure 7. Output Skew

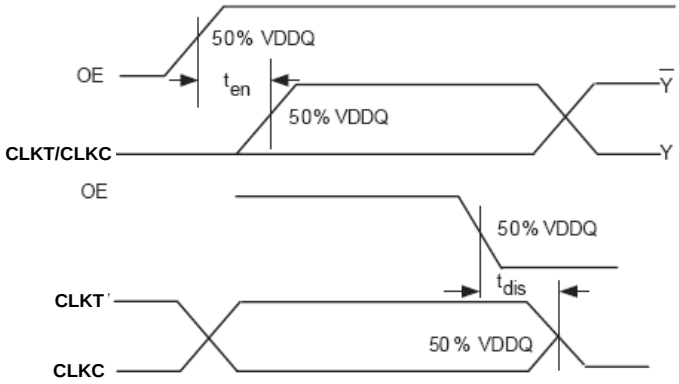


Figure 8. Output Enable and Disable Times

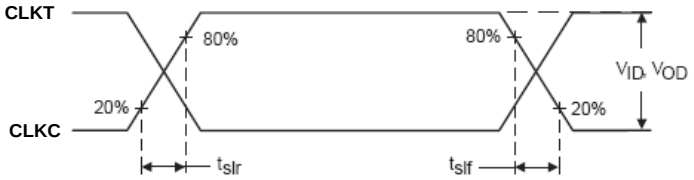


Figure 9. Input/Output Slew Rates

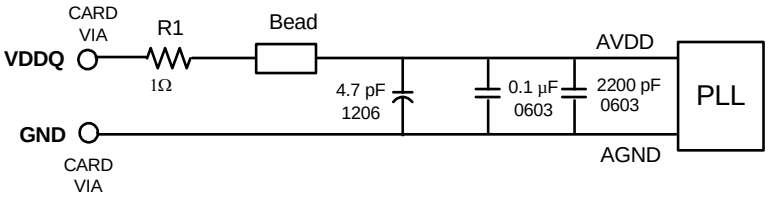


Figure 10. AV_{DD} Filtering[3,4,5]

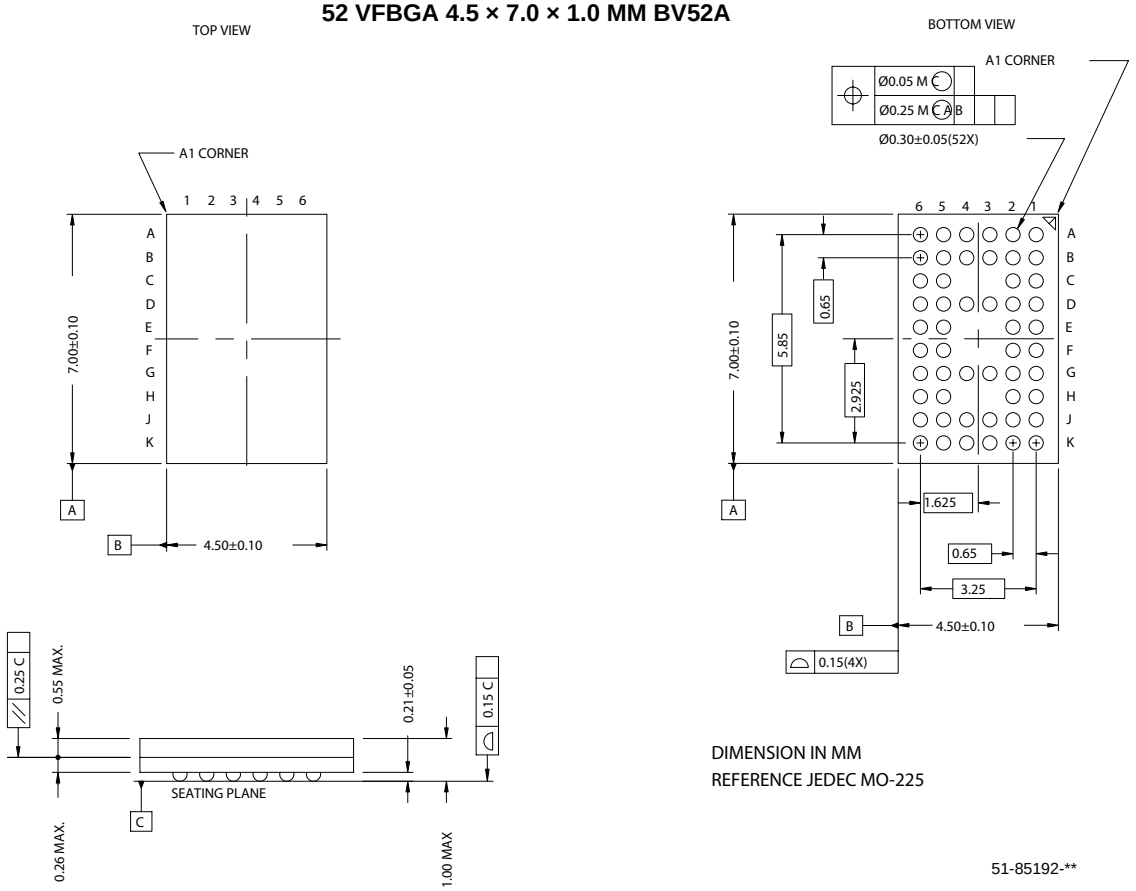
Ordering Information

Part Number	Package Type	Product Flow
Lead-free and ROHS Compliant		
CY2SSTU877BVXC-32	52-pin VFBGA for DDR400	Commercial, 0° to 70°C
CY2SSTU877BVXC-32T	52-pin VFBGA for DDR400 – Tape& Reel	Commercial, 0° to 70°C
CY2SSTU877BVXI-32	52-pin VFBGA for DDR400	Industrial, –40° to 85°C
CY2SSTU877BVXI-32T	52-pin VFBGA for DDR400 – Tape& Reel	Industrial, –40° to 85°C
CY2SSTU877BVXC-43	52-pin VFBGA for DDR533	Commercial, 0° to 70°C
CY2SSTU877BVXC-43T	52-pin VFBGA for DDR533 – Tape& Reel	Commercial, 0° to 70°C
CY2SSTU877BVXI-43	52-pin VFBGA for DDR533	Industrial, –40° to 85°C
CY2SSTU877BVXI-43T	52-pin VFBGA for DDR533 – Tape& Reel	Industrial, –40° to 85°C

Notes:
3. Place the 2200-pF capacitor close to the PLL.
4. Use a wide trace for the PLL analog power and ground. Connect PLL & Caps to AGND trace & connect trace to one GND via (farthest from PLL).
5. Recommended bead: Fair-Rite P/N 2506036017Y0 or equivalent (0.9 ohm DC max, 600 ohms@100 MHz).

Package Drawing

52 VFBGA 4.5 × 7.0 × 1.0 MM BV52A



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Document History Page

Document Title:CY2SSTU877 1.8V, 500-MHz, 10-Output JEDEC-Compliant Zero Delay Buffer Document Number: 38-07575				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	129198	08/22/03	RGL	New Data Sheet
*A	204389	See ECN	RGL	Added more Information. Deleted 4 rows from the bottom of the Pin description.
*B	310414	See ECN	RGL	Changed Advance Info. to Preliminary status Added Lead-free devices
*C	324113	See ECN	RGL	Data sheet re-write
*D	404547	See ECN	RGL	Added speed bins to part number
*E	424024	See ECN	RGL	Swap pins 6G and 6H