

## Features

- TSOP I Package Configurable as 512K x 16 or 1M x 8 SRAM
- High Speed: 45 ns
- Temperature Ranges
  - Industrial: -40°C to +85°C
  - Automotive-A: -40°C to +85°C
  - Automotive-E: -40°C to +125°C
- Wide Voltage Range: 2.20V to 3.60V
- Pin Compatible with CY62157DV30
- Ultra Low Standby Power
  - Typical standby current: 2  $\mu$ A
  - Maximum standby current: 8  $\mu$ A (Industrial)
- Ultra Low Active Power
  - Typical active current: 1.8 mA at f = 1 MHz
- Easy Memory Expansion with  $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{OE}$  Features
- Automatic Power Down when Deselected
- CMOS for Optimum Speed and Power
- Available in Pb-free and non Pb-free 48-Ball VFBGA, Pb-free 44-Pin TSOP II and 48-Pin TSOP I Packages

## Functional Description

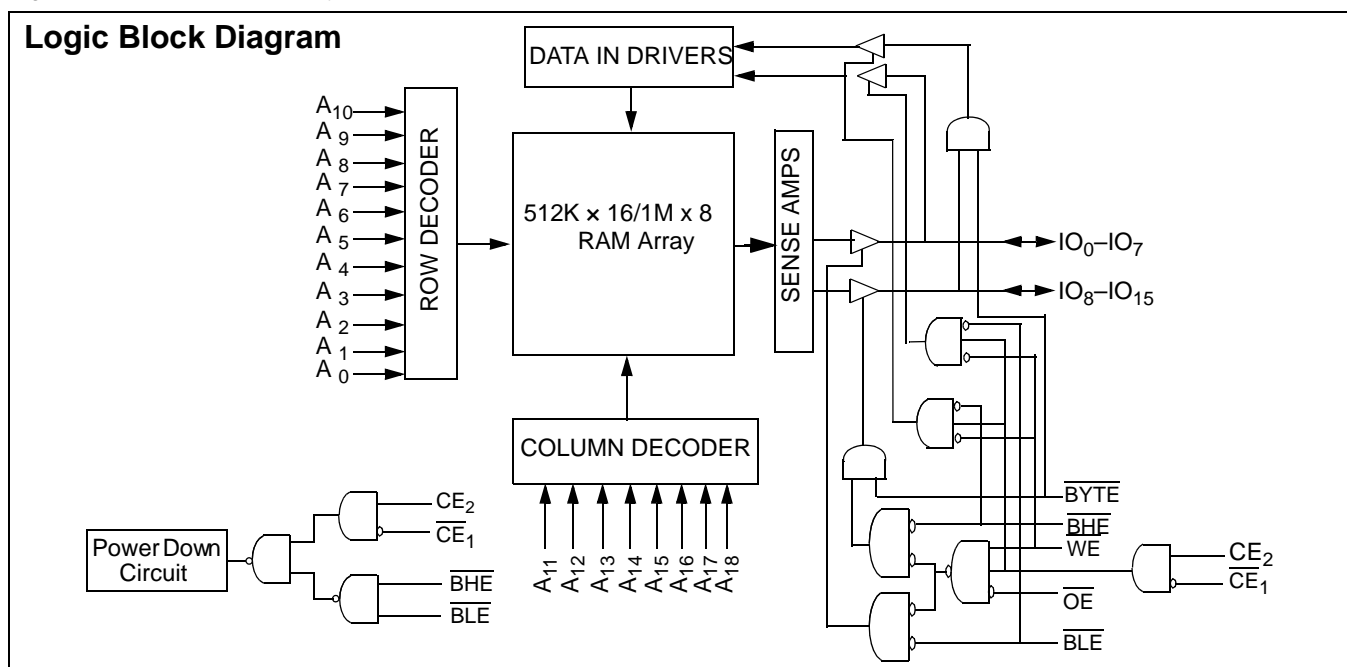
The CY62157EV30 is a high performance CMOS static RAM organized as 512K words by 16 bits. This device features

advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Place the device into standby mode when deselected ( $CE_1$  HIGH or  $CE_2$  LOW or both BHE and BLE are HIGH). The input or output pins ( $IO_0$  through  $IO_{15}$ ) are placed in a high impedance state when the device is deselected ( $CE_1$  HIGH or  $CE_2$  LOW), the outputs are disabled ( $\overline{OE}$  HIGH), Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH), or a write operation is active ( $\overline{CE}_1$  LOW,  $CE_2$  HIGH and WE LOW).

To write to the device, take Chip Enable ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from IO pins ( $IO_0$  through  $IO_7$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{18}$ ). If Byte High Enable (BHE) is LOW, then data from IO pins ( $IO_8$  through  $IO_{15}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{18}$ ).

To read from the device, take Chip Enable ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins appear on  $IO_0$  to  $IO_7$ . If Byte High Enable (BHE) is LOW, then data from memory appears on  $IO_8$  to  $IO_{15}$ . See the [Truth Table on page 10](#) for a complete description of read and write modes.

For best practice recommendations, refer to the Cypress application note [AN1064, SRAM System Guidelines](#).



## Pin Configuration

Figure 1. 48-Ball VFBGA (Top View) [2]

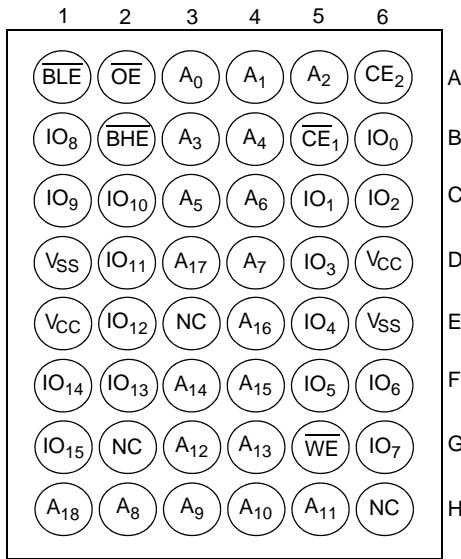


Figure 2. 44-Pin TSOP II (Top View) [3]

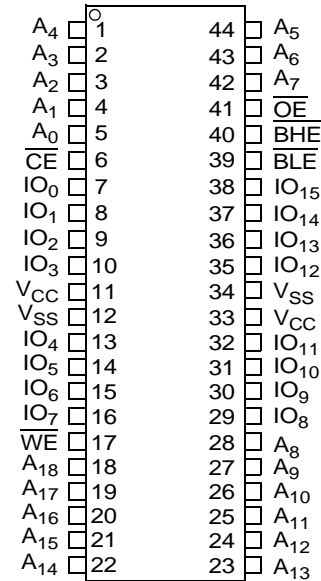
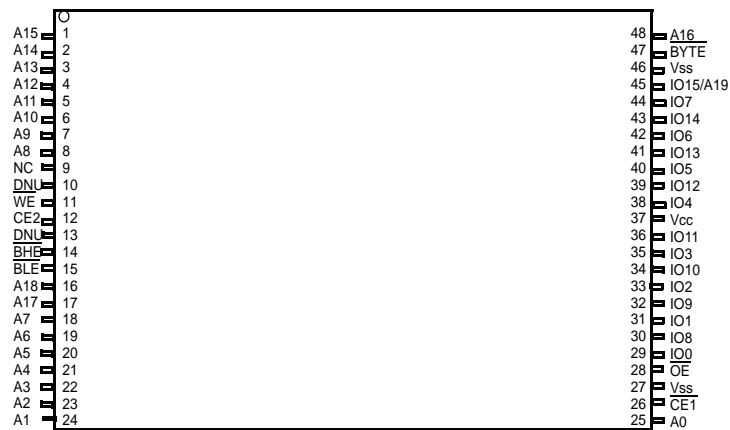


Figure 3. 48-Pin TSOP I (512K x 16/1M x 8) (Top View) [2, 4]



## Product Portfolio

Product	Range	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
						Operating I <sub>CC</sub> (mA)				Standby, I <sub>SB2</sub> (μA)	
		Min	Typ <sup>[1]</sup>	Max		Typ <sup>[1]</sup>	Max	Typ <sup>[1]</sup>	Max		
CY62157EV30LL	Ind'I/Auto-A	2.2	3.0	3.6	45	1.8	3	18	25	2	8
	Auto-E	2.2	3.0	3.6	55	1.8	4	18	35	2	30

### Notes

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25°C.
2. NC pins are not connected on the die.
3. The 44-TSOP II package has only one chip enable ( $\overline{CE}$ ) pin.
4. The BYTE pin in the 48-TSOP I package must be tied HIGH to use the device as a 512K x 16 SRAM. The 48-TSOP I package can also be used as a 1M x 8 SRAM by tying the BYTE signal LOW. In the 1M x 8 configuration, Pin 45 is A19, while BHE, BLE and IO8 to IO14 pins are not used (DNU).

## Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage Temperature ..... -65°C to + 150°C

Ambient Temperature with Power Applied ..... -55°C to + 125°C

Supply Voltage to Ground Potential ..... -0.3V to 3.9V ( $V_{CCmax} + 0.3V$ )

DC Voltage Applied to Outputs in High-Z State <sup>[5, 6]</sup> ..... -0.3V to 3.9V ( $V_{CCmax} + 0.3V$ )

DC Input Voltage <sup>[5, 6]</sup> ..... -0.3V to 3.9V ( $V_{CCmax} + 0.3V$ )

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 2001V (MIL-STD-883, Method 3015)

Latch Up Current ..... > 200 mA

## Operating Range

Device	Range	Ambient Temperature	V <sub>CC</sub> <sup>[7]</sup>
CY62157EV30LL	Ind'I/Auto-A	-40°C to +85°C	2.2V to 3.6V
	Auto-E	-40°C to +125°C	

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	45 ns (Ind'I/Auto-A)			55 ns (Auto-E)			Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Typ <sup>[1]</sup>	Max	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -0.1 mA	2.0			2.0			V
		I <sub>OH</sub> = -1.0 mA, V <sub>CC</sub> ≥ 2.70V	2.4			2.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 0.1 mA			0.4			0.4	V
		I <sub>OL</sub> = 2.1mA, V <sub>CC</sub> ≥ 2.70V			0.4			0.4	V
V <sub>IH</sub>	Input HIGH Voltage	V <sub>CC</sub> = 2.2V to 2.7V	1.8		V <sub>CC</sub> + 0.3	1.8		V <sub>CC</sub> + 0.3	V
		V <sub>CC</sub> = 2.7V to 3.6V	2.2		V <sub>CC</sub> + 0.3	2.2		V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage	V <sub>CC</sub> = 2.2V to 2.7V	-0.3		0.6	-0.3		0.6	V
		V <sub>CC</sub> = 2.7V to 3.6V	-0.3		0.8	-0.3		0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1		+1	-4		+4	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-1		+1	-4		+4	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>max</sub> = 1/t <sub>RC</sub>		18	25		18	35	mA
		f = 1 MHz		1.8	3		1.8	4	
I <sub>SB1</sub>	Automatic CE Power Down Current — CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.2V$ , CE <sub>2</sub> ≤ 0.2V V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≤ 0.2V f = f <sub>max</sub> (Address and Data Only), f = 0 (OE, BHE, BLE and WE), V <sub>CC</sub> = 3.60V		2	8		2	30	μA
I <sub>SB2</sub> <sup>[8]</sup>	Automatic CE Power Down Current — CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.2V$ or CE <sub>2</sub> ≤ 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = 0, V <sub>CC</sub> = 3.60V		2	8		2	30	μA

### Notes

- V<sub>IL(min)</sub> = -2.0V for pulse durations less than 20 ns.
- V<sub>IH(max)</sub> = V<sub>CC</sub> + 0.75V for pulse durations less than 20 ns.
- Full device AC operation assumes a 100 μs ramp time from 0 to V<sub>CC(min)</sub> and 200 μs wait time after V<sub>CC</sub> stabilization.
- Only chip enables (CE<sub>1</sub> and CE<sub>2</sub>), byte enables (BHE and BLE) and BYTE (48 TSOP I only) need to be tied to CMOS levels to meet the I<sub>SB2</sub> / I<sub>CCDR</sub> spec. Other inputs can be left floating.
- Tested initially and after any design or process changes that may affect these parameters.

### Capacitance

Tested initially and after any design or process changes that may affect these parameters.

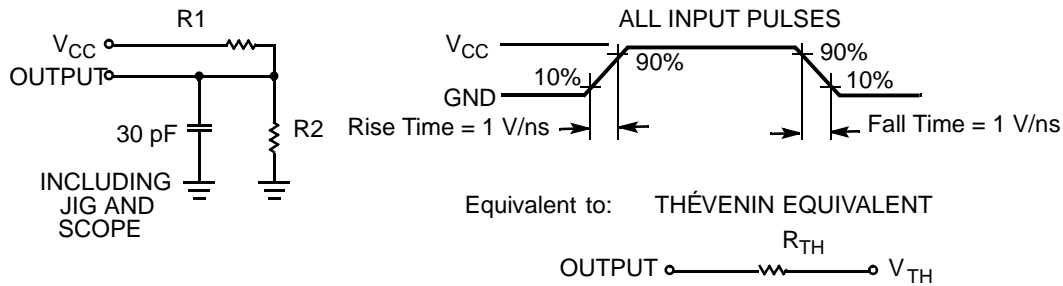
Parameter	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC</sub> (typ)	10	pF
C <sub>OUT</sub>	Output Capacitance		10	pF

### Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	BGA	TSOP I	TSOP II	Unit
Θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	72	74.88	76.88	°C/W
Θ <sub>JC</sub>	Thermal Resistance (Junction to Case)		8.86	8.6	13.52	°C/W

Figure 4. AC Test Loads and Waveforms



Parameters	2.5V	3.0V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R <sub>TH</sub>	8000	645	Ω
V <sub>TH</sub>	1.20	1.75	V

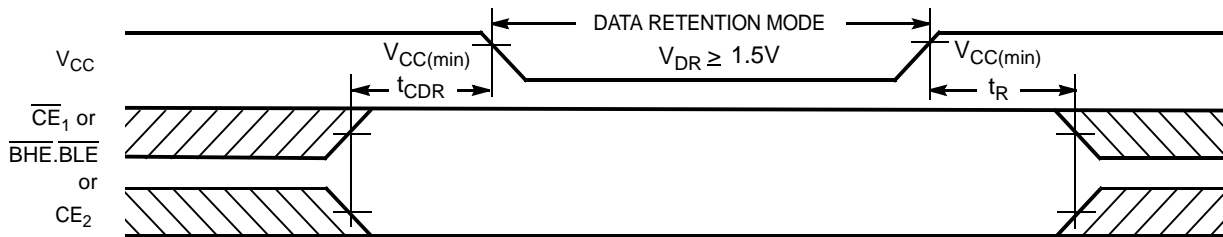
### Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention		1.5			V
I <sub>CCDR</sub> <sup>[8]</sup>	Data Retention Current	V <sub>CC</sub> = 1.5V, $\overline{CE}_1 \geq V_{CC} - 0.2V$ , CE <sub>2</sub> ≤ 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V				
		Ind'l/Auto-A		2	5	μA
		Auto-E			30	
t <sub>CDR</sub> <sup>[9]</sup>	Chip Deselect to Data Retention Time		0			ns
t <sub>R</sub> <sup>[10]</sup>	Operation Recovery Time		t <sub>RC</sub>			ns

### Data Retention Waveform

Figure 5. Data Retention Waveform <sup>[11]</sup>



**Notes**

10. Full device operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min)</sub> ≥ 100 μs or stable at V<sub>CC(min)</sub> ≥ 100 μs.

11. BHE.BLE is the AND of both BHE and BLE. Deselect the chip by either disabling chip enable signals or by disabling both  $\overline{BHE}$  and  $\overline{BLE}$ .

## Switching Characteristics

Over the Operating Range<sup>[12, 13]</sup>

Parameter	Description	45 ns (Ind'l/Auto-A)		55 ns (Auto-E)		Unit
		Min	Max	Min	Max	
<b>Read Cycle</b>						
t <sub>RC</sub>	Read Cycle Time	45		55		ns
t <sub>AA</sub>	Address to Data Valid		45		55	ns
t <sub>OHA</sub>	Data Hold from Address Change	10		10		ns
t <sub>ACE</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to Data Valid		45		55	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		22		25	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low-Z <sup>[14]</sup>	5		5		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High-Z <sup>[14, 15]</sup>		18		20	ns
t <sub>LZCE</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to Low-Z <sup>[14]</sup>	10		10		ns
t <sub>HZCE</sub>	$\overline{CE}_1$ HIGH and CE <sub>2</sub> LOW to High-Z <sup>[14, 15]</sup>		18		20	ns
t <sub>PU</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to Power Up	0		0		ns
t <sub>PD</sub>	$\overline{CE}_1$ HIGH and CE <sub>2</sub> LOW to Power Down		45		55	ns
t <sub>DBE</sub>	$\overline{BLE}/\overline{BHE}$ LOW to Data Valid		45		55	ns
t <sub>LZBE</sub>	$\overline{BLE}/\overline{BHE}$ LOW to Low-Z <sup>[14, 16]</sup>	5		10		ns
t <sub>HZBE</sub>	$\overline{BLE}/\overline{BHE}$ HIGH to HIGH-Z <sup>[14, 15]</sup>		18		20	ns
<b>Write Cycle<sup>[17]</sup></b>						
t <sub>WC</sub>	Write Cycle Time	45		55		ns
t <sub>SCE</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to Write End	35		40		ns
t <sub>AW</sub>	Address Setup to Write End	35		40		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		ns
t <sub>SA</sub>	Address Setup to Write Start	0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	35		40		ns
t <sub>BW</sub>	$\overline{BLE}/\overline{BHE}$ LOW to Write End	35		40		ns
t <sub>SD</sub>	Data Setup to Write End	25		25		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High-Z <sup>[14, 15]</sup>		18		20	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low-Z <sup>[14]</sup>	10		10		ns

### Notes

12. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the [AC Test Loads and Waveforms on page 4](#).
13. AC timing parameters are subject to byte enable signals (BHE or BLE) not switching when chip is disabled. See application note [AN13842](#) for further clarification.
14. At any temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZBE</sub> is less than t<sub>LZBE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any device.
15. t<sub>HZOE</sub>, t<sub>HZCE</sub>, t<sub>HZBE</sub>, and t<sub>HZWE</sub> transitions are measured when the outputs enter a high-impedance state.
16. If both byte enables are toggled together, this value is 10 ns.
17. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  or both =  $V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

## Switching Waveforms

Figure 6 shows Address Transition Controlled read cycle waveforms.<sup>[18, 19]</sup>

Figure 6. Read Cycle No. 1

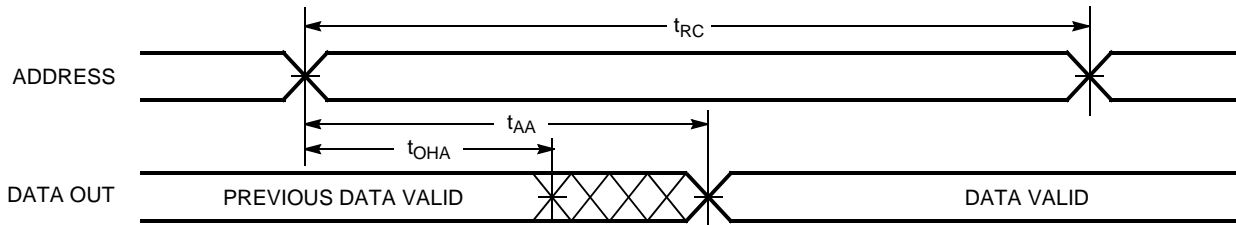
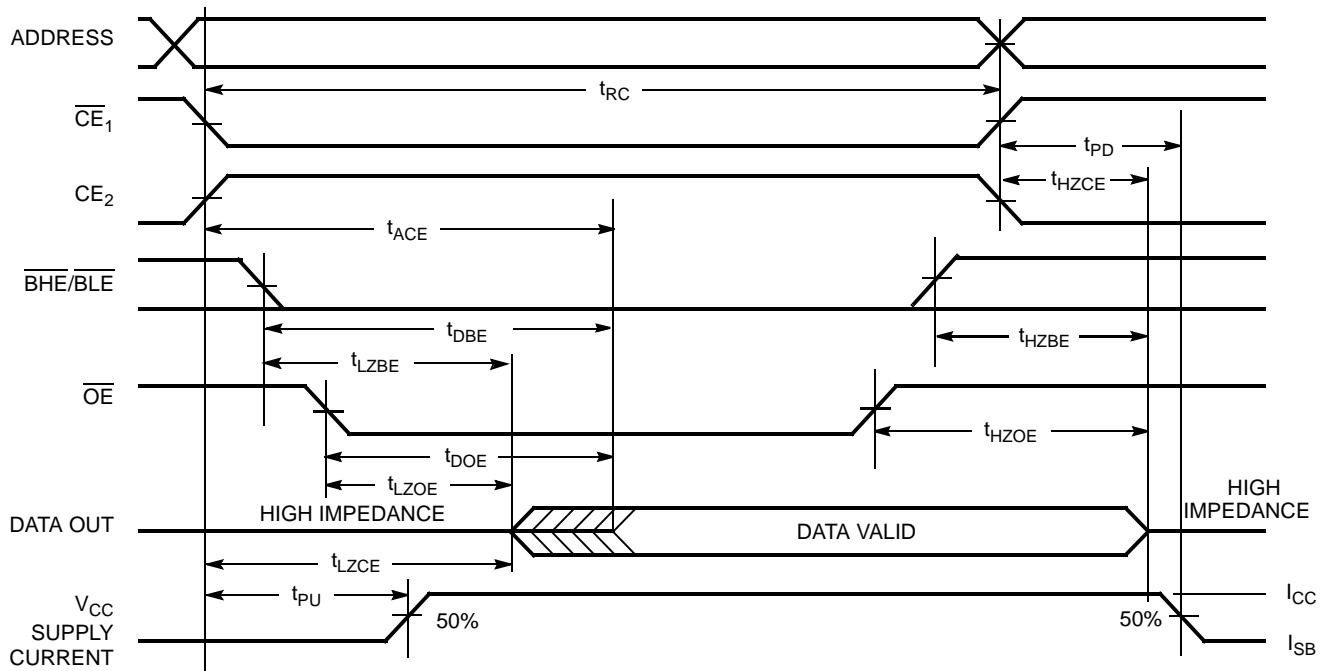


Figure 7 shows  $\overline{\text{OE}}$  Controlled read cycle waveforms.<sup>[19, 20]</sup>

Figure 7. Read Cycle No. 2



### Notes

18. The device is continuously selected.  $\overline{\text{OE}}$ ,  $\overline{\text{CE}}_1 = V_{\text{IL}}$ ,  $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$ , or both =  $V_{\text{IL}}$ , and  $\text{CE}_2 = V_{\text{IH}}$ .
19.  $\overline{\text{WE}}$  is HIGH for read cycle.
20. Address valid before or similar to  $\overline{\text{CE}}_1$ ,  $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$  transition LOW and  $\text{CE}_2$  transition HIGH.

**Switching Waveforms** (continued)

Figure 8 shows  $\overline{WE}$  Controlled write cycle waveforms.<sup>[17, 21, 22]</sup>

**Figure 8. Write Cycle No. 1**

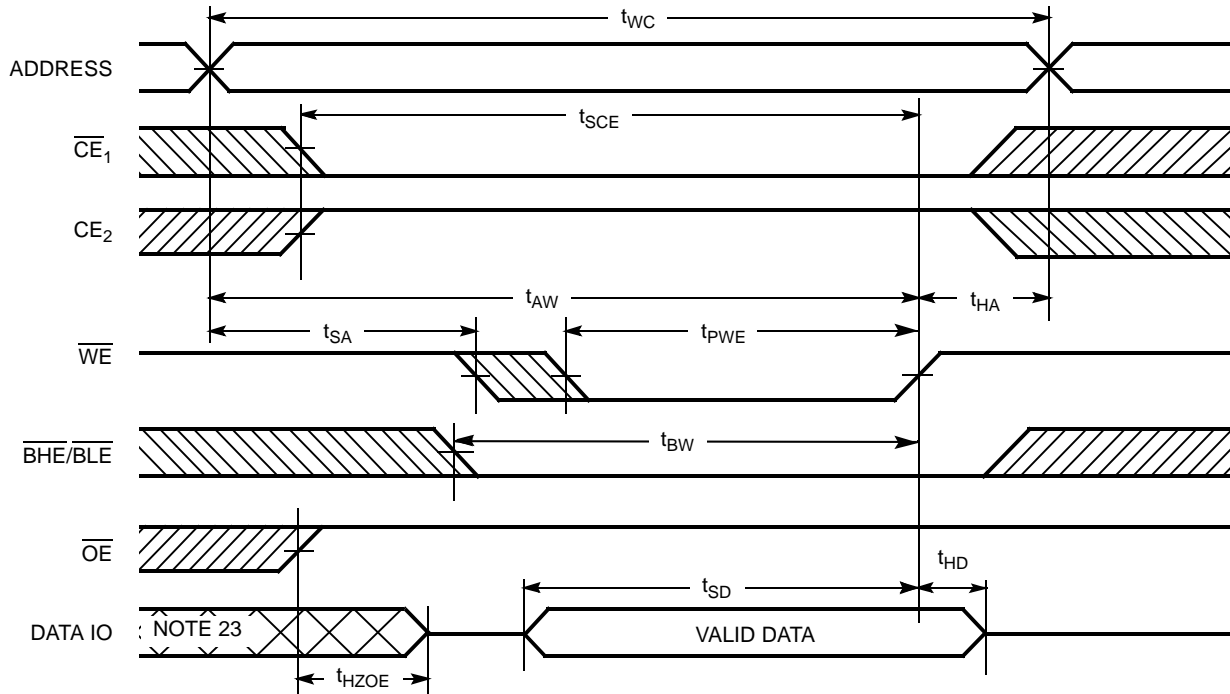
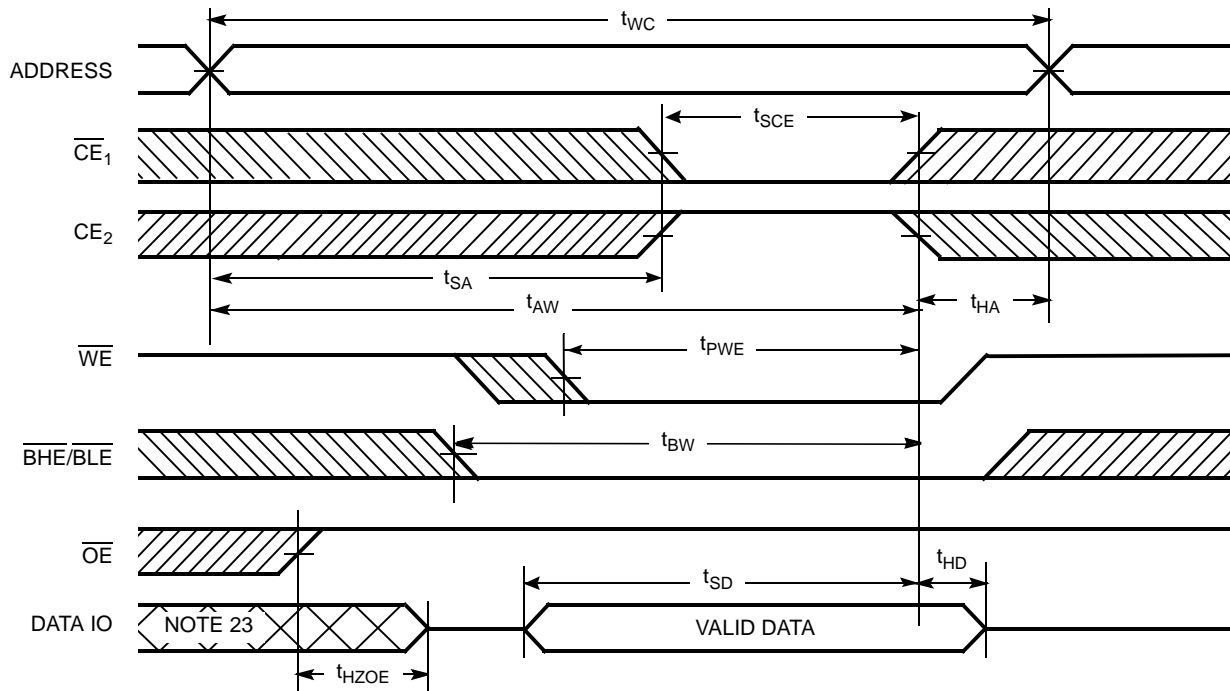


Figure 9 shows  $\overline{CE}_1$  or  $CE_2$  Controlled write cycle waveforms.<sup>[17, 21, 22]</sup>

**Figure 9. Write Cycle No. 1**



**Notes**

- 21. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
- 22. If  $\overline{CE}_1$  goes HIGH and  $CE_2$  goes LOW simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high impedance state.
- 23. During this period, the I/Os are in output state. Do not apply input signals.



**Switching Waveforms** (continued)

Figure 10 shows  $\overline{WE}$  Controlled,  $\overline{OE}$  LOW write cycle waveforms.<sup>[22]</sup>

**Figure 10. Write Cycle No. 3**

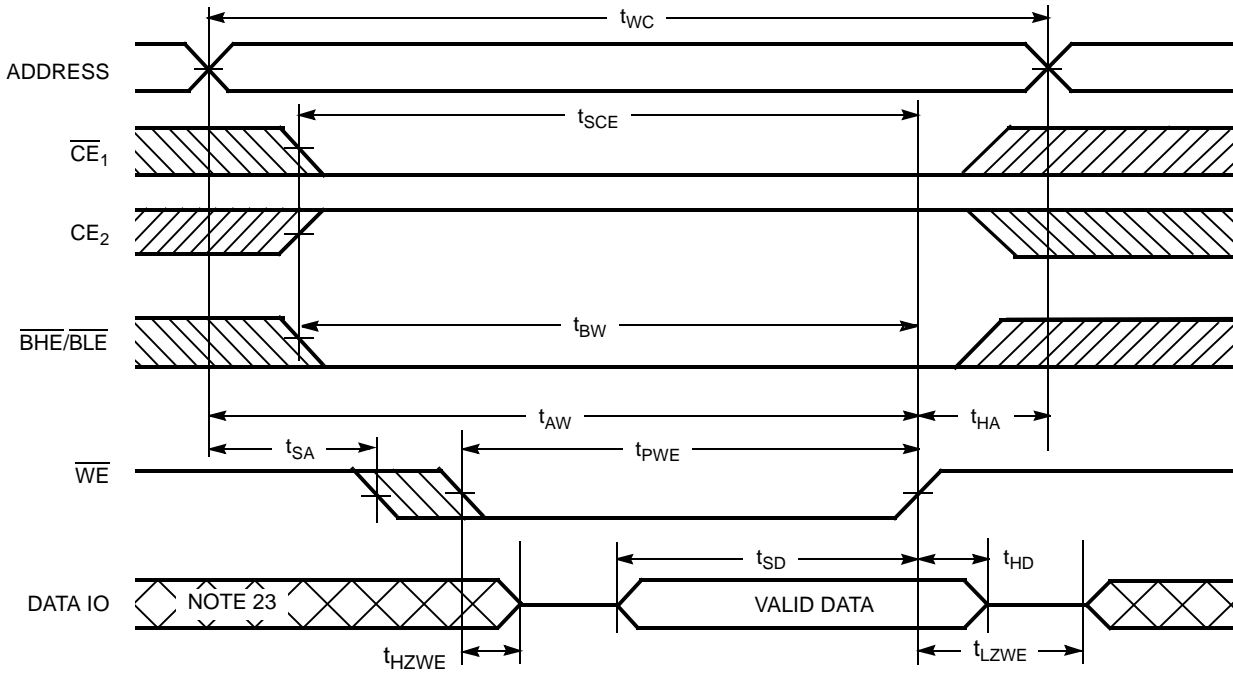
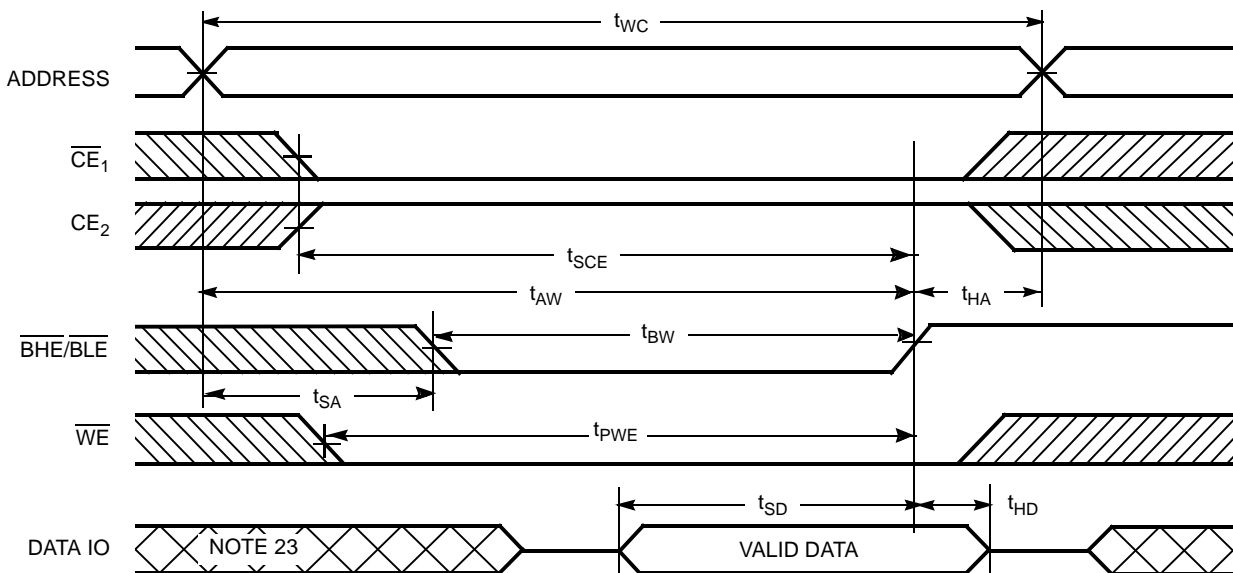


Figure 11 shows  $\overline{BHE}/\overline{BLE}$  Controlled,  $\overline{OE}$  LOW write cycle waveforms.<sup>[22]</sup>

**Figure 11. Write Cycle No. 4**



**Truth Table**

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High-Z	Deselect/Power Down	Standby ( $I_{SB}$ )
X	L	X	X	X	X	High-Z	Deselect/Power Down	Standby ( $I_{SB}$ )
X	X	X	X	H	H	High-Z	Deselect/Power Down	Standby ( $I_{SB}$ )
L	H	H	L	L	L	Data Out ( $IO_0$ - $IO_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	H	L	H	L	Data Out ( $IO_0$ - $IO_7$ ); High-Z ( $IO_8$ - $IO_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	H	L	L	H	High-Z ( $IO_0$ - $IO_7$ ); Data Out ( $IO_8$ - $IO_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	H	H	L	H	High-Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	H	L	High-Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	L	L	High-Z	Output Disabled	Active ( $I_{CC}$ )
L	H	L	X	L	L	Data In ( $IO_0$ - $IO_{15}$ )	Write	Active ( $I_{CC}$ )
L	H	L	X	H	L	Data In ( $IO_0$ - $IO_7$ ); High-Z ( $IO_8$ - $IO_{15}$ )	Write	Active ( $I_{CC}$ )
L	H	L	X	L	H	High-Z ( $IO_0$ - $IO_7$ ); Data In ( $IO_8$ - $IO_{15}$ )	Write	Active ( $I_{CC}$ )

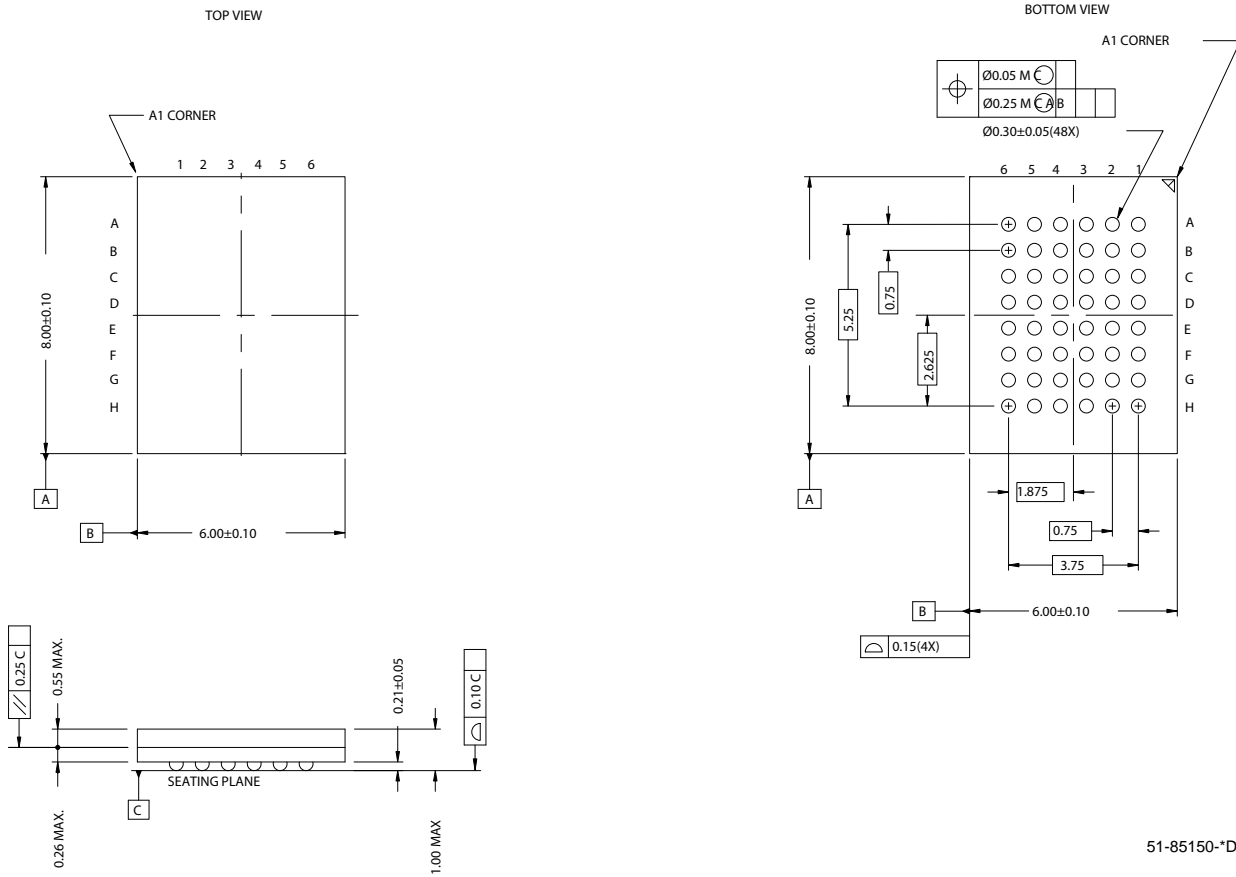
**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62157EV30LL-45BVI	51-85150	48-ball Very Fine Pitch Ball Grid Array	Industrial
	CY62157EV30LL-45BVXI	51-85150	48-ball Very Fine Pitch Ball Grid Array (Pb-free)	
	CY62157EV30LL-45ZSXI	51-85087	44-pin Thin Small Outline Package Type II (Pb-free)	
	CY62157EV30LL-45ZXI	51-85183	48-pin Thin Small Outline Package Type I (Pb-free)	
	CY62157EV30LL-45BVXA	51-85150	48-ball Very Fine Pitch Ball Grid Array (Pb-free)	Automotive-A
	CY62157EV30LL-45ZSXA	51-85087	44-pin Thin Small Outline Package Type II (Pb-free)	
	CY62157EV30LL-45ZXA	51-85183	48-pin Thin Small Outline Package Type I (Pb-free)	
55	CY62157EV30LL-55ZSXE	51-85087	44-pin Thin Small Outline Package Type II (Pb-free)	Automotive-E
	CY62157EV30LL-55ZXE	51-85183	48-pin Thin Small Outline Package Type I (Pb-free)	

Contact your local Cypress sales representative for availability of these parts.

Package Diagrams

Figure 12. 48-Pin VFBGA (6 x 8 x 1 mm), 51-85150

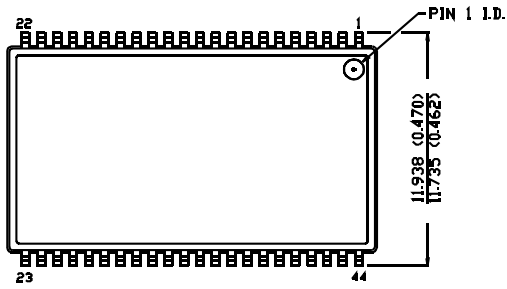


51-85150-\*D

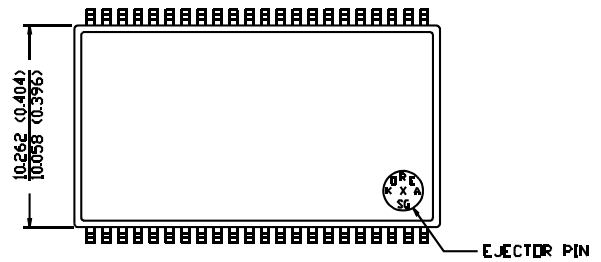
Package Diagrams (continued)

Figure 13. 44-Pin TSOP II, 51-85087

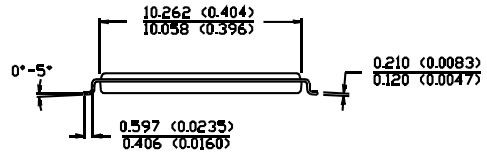
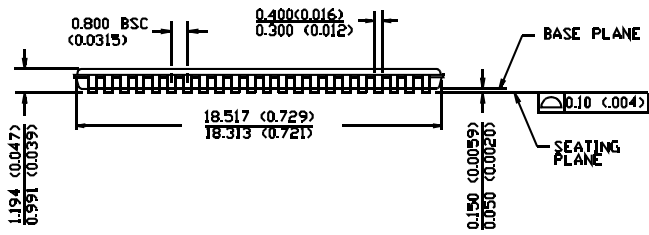
DIMENSION IN MM (INCH)  
MAX  
MIN



TOP VIEW



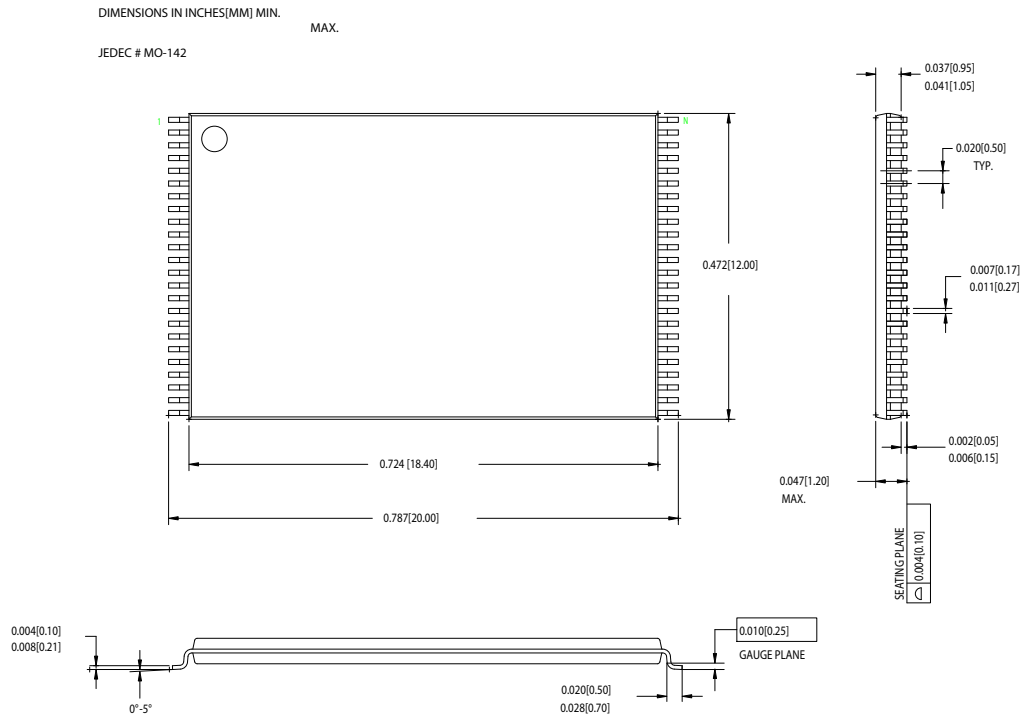
BOTTOM VIEW



51-85087-\*A

Package Diagrams (continued)

Figure 14. 48-Pin TSOP I (12 mm x 18.4 mm x 1.0 mm), 51-85183



51-85183-\*A

Document History Page

Document Title: CY62157EV30 MoBL®, 8 Mbit (512K x 16) Static RAM				
Document Number: 38-05445				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	202940	AJU	See ECN	New Data Sheet
*A	291272	SYT	See ECN	<p>Converted from Advance Information to Preliminary</p> <p>Removed 48-TSOP I Package and the associated footnote</p> <p>Added footnote stating 44 TSOP II Package has only one CE on Page # 2</p> <p>Changed V<sub>CC</sub> stabilization time in footnote #7 from 100 μs to 200 μs</p> <p>Changed I<sub>CCDR</sub> from 4 to 4.5 μA</p> <p>Changed t<sub>OHA</sub> from 6 to 10 ns for both 35 and 45 ns Speed Bins</p> <p>Changed t<sub>DOE</sub> from 15 to 18 ns for 35 ns Speed Bin</p> <p>Changed t<sub>HZOE</sub>, t<sub>HZBE</sub> and t<sub>HZWE</sub> from 12 and 15 ns to 15 and 18 ns for 35 and 45 ns Speed Bins respectively</p> <p>Changed t<sub>HZCE</sub> from 12 and 15 ns to 18 and 22 ns for 35 and 45 ns Speed Bins respectively</p> <p>Changed t<sub>SCE</sub>, t<sub>AW</sub> and t<sub>BW</sub> from 25 and 40 ns to 30 and 35 ns for 35 and 45 ns Speed Bins respectively</p> <p>Changed t<sub>SD</sub> from 15 and 20 ns to 18 and 22 ns for 35 and 45 ns Speed Bins respectively</p> <p>Added Lead-Free Package Information</p>
*B	444306	NXR	See ECN	<p>Converted from Preliminary to Final.</p> <p>Changed ball E3 from DNU to NC</p> <p>Removed redundant footnote on DNU.</p> <p>Removed 35 ns speed bin</p> <p>Removed "L" bin</p> <p>Added 48 pin TSOP I package</p> <p>Added Automotive product information.</p> <p>Changed the I<sub>CC</sub> Typ value from 16 mA to 18 mA and I<sub>CC</sub> Max value from 28 mA to 25 mA for test condition f = fax = 1/t<sub>RC</sub>.</p> <p>Changed the I<sub>CC</sub> Max value from 2.3 mA to 3 mA for test condition f = 1MHz.</p> <p>Changed the I<sub>SB1</sub> and I<sub>SB2</sub> Max value from 4.5 μA to 8 μA and Typ value from 0.9 μA to 2 μA respectively.</p> <p>Modified ISB<sub>1</sub> test condition to include <math>\overline{BHE}</math>, <math>\overline{BLE}</math></p> <p>Updated Thermal Resistance table.</p> <p>Changed Test Load Capacitance from 50 pF to 30 pF.</p> <p>Added Typ value for I<sub>CCDR</sub></p> <p>Changed the I<sub>CCDR</sub> Max value from 4.5 μA to 5 μA</p> <p>Corrected t<sub>R</sub> in Data Retention Characteristics from 100 μs to t<sub>RC</sub> ns.</p> <p>Changed t<sub>LZOE</sub> from 3 to 5</p> <p>Changed t<sub>LZCE</sub> from 6 to 10</p> <p>Changed t<sub>HZCE</sub> from 22 to 18</p> <p>Changed t<sub>LZBE</sub> from 6 to 5</p> <p>Changed t<sub>PWE</sub> from 30 to 35</p> <p>Changed t<sub>SD</sub> from 22 to 25</p> <p>Changed t<sub>LZWE</sub> from 6 to 10</p> <p>Added footnote #15</p> <p>Updated the ordering Information and replaced the Package Name column with Package Diagram.</p>
*C	467052	NXR	See ECN	<p>Modified Data sheet to include x8 configurability.</p> <p>Updated the Ordering Information table</p>
*D	925501	VKN	See ECN	<p>Removed Automotive-E information</p> <p>Added Preliminary Automotive-A information</p> <p>Added footnote #10 related to I<sub>SB2</sub> and I<sub>CCDR</sub></p> <p>Added footnote #15 related AC timing parameters</p>
*E	1045801	VKN	See ECN	<p>Converted Automotive-A specs from preliminary to final</p> <p>Updated footnote #9</p>

<b>Document Title: CY62157EV30 MoBL®, 8 Mbit (512K x 16) Static RAM</b>				
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Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*F	2724889	NXR/AESA	06/26/09	Added Automotive-E information Included -45ZXAX/-55ZSXE/-55ZXE parts in the Ordering Information table

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