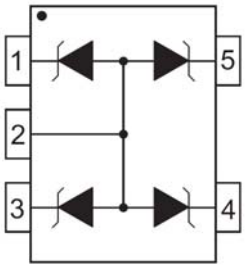
Feature

- 100W peak pulse power per line (t_P = 8/20μS)
- SOT-353 package
- Protects three bidirectional lines and four Unidirectional lines
- Monolithic structure
- Working voltage: 5V
- Low clamping voltage
- ESD protection > 40 KV
- Low leakage current
- RoHS compliant
- Transient protection for data lines to IEC 61000-4-2(ESD) ±15KV(air), ±8KV(contact); IEC 61000-4-4 (EFT) 40A (5/50ns)



Applications

- Communication systems & Cellular phones
- Printers
- Notebook and hand hold computers
- PDAs
- Video Equipment

Electrical characteristics per line@25℃(unless otherwise specified) note1

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Reverse stand-off voltage	V_{RWM}				5	V
Reverse Breakdown voltage	V_{BR}	I_t = 1mA	6			V
Reverse Leakage Current	I_R	V_{RWM} = 5V T=25℃			5	μA
Clamping Voltage	V_C	I_{PP} = 1A t_P = 8/20μS			8.8	V
Clamping Voltage	V_C	I_{PP}=10A t_P = 8/20μS			10.0	V
Junction Capacitance	C_j	V_R=0V f = 1MHz		90		pF

Absolute maximum rating @25℃ note1

Rating	Symbol	Value	Units
Peak Pulse Power (t_p=8/20μS)	P_{pp}	100	W
Forward voltage@10mA	V_F	1.5	V
Operating Temperature	T_J	-55 to +150	℃
Storage Temperature	T_{STG}	-55 to +150	℃

- Note1: Pin 1, 3, 4, 5 to Pin 2

Typical Characteristics

FIGURE 1
PEAK PULSE POWER VS PULSE TIME

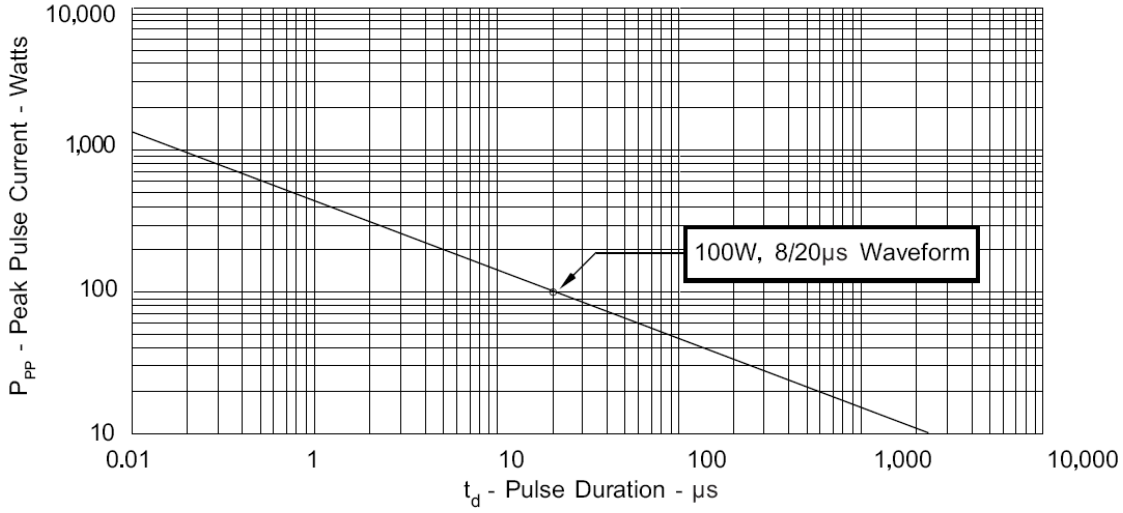


FIGURE 2
PULSE WAVE FORM

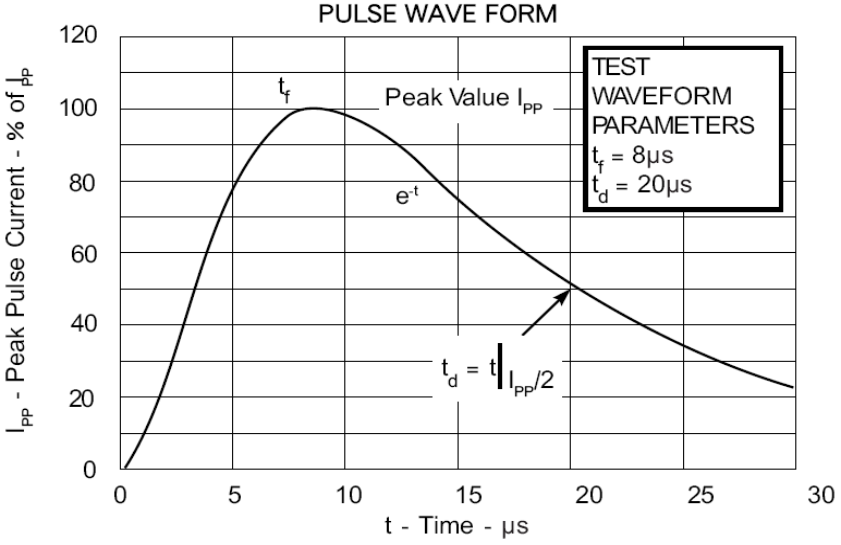
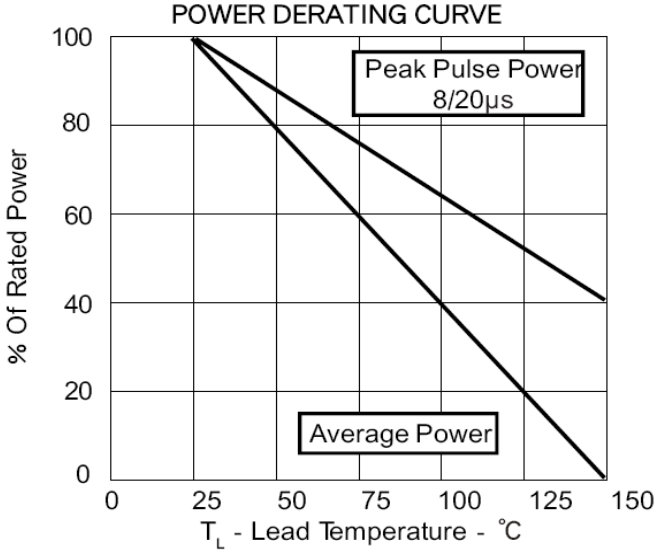


FIGURE 3
POWER DERATING CURVE



Typical Characteristics

FIGURE 4
OVERSHOOT & CLAMPING VOLTAGE FOR UMD SES5VT553-5

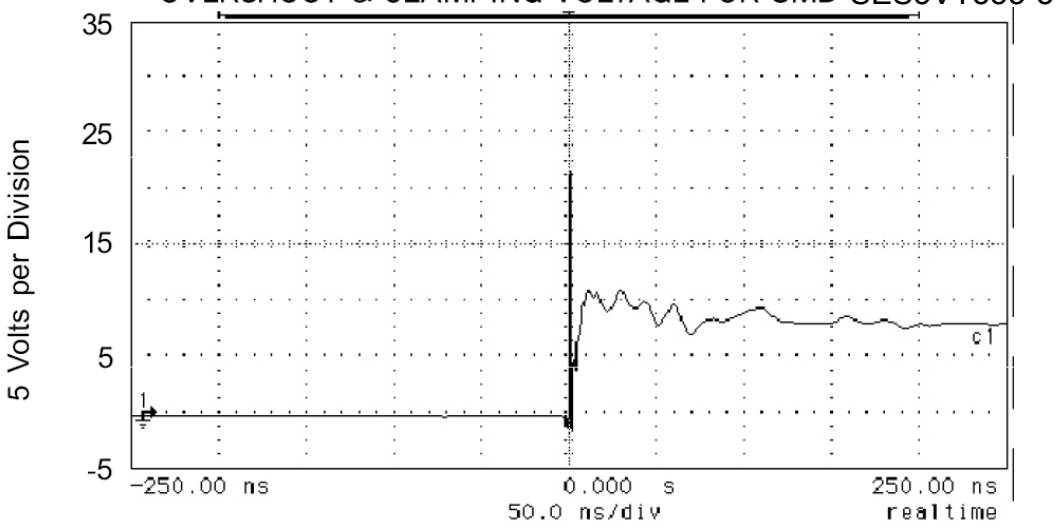
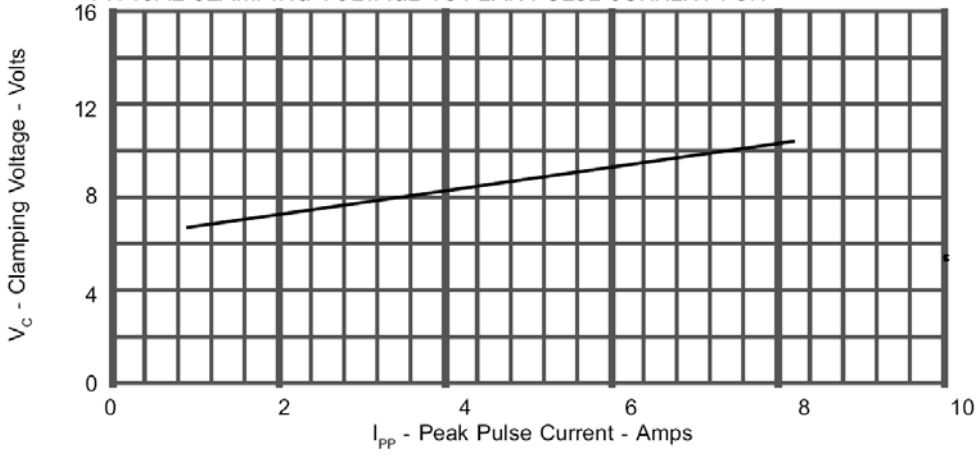
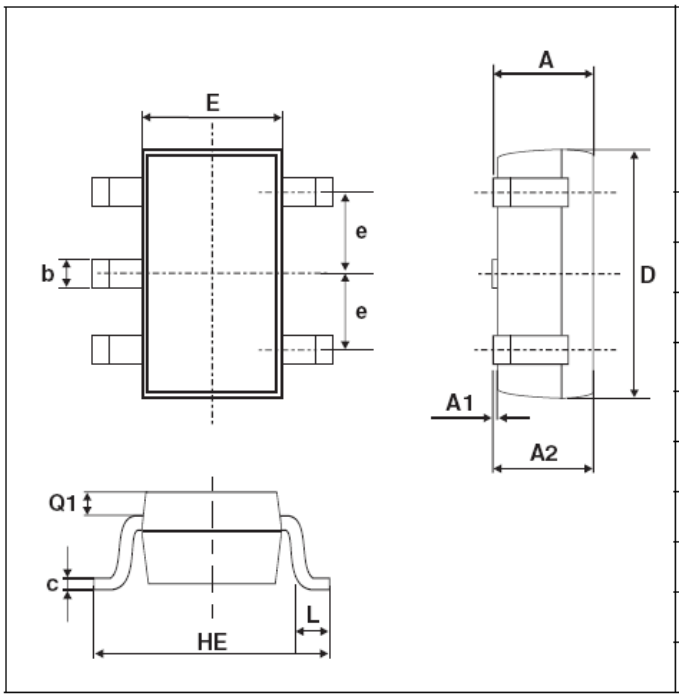


FIGURE 5
TYPICAL CLAMPING VOLTAGE VS PEAK PULSE CURRENT FOR **SES5VT353-5**



Product dimension and pad size

SOT-353 Mechanical Data



REF.	DIMENSIONS			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.8	1.1	0.031	0.043
A1	0	0.1	0	0.004
A2	0.8	1	0.031	0.039
b	0.15	0.3	0.006	0.012
c	0.1	0.18	0.004	0.007
D	1.8	2.2	0.071	0.086
E	1.15	1.35	0.045	0.053
e	0.65 Typ.		0.025 Typ.	
H	1.8	2.4	0.071	0.094
Q1	0.1	0.4	0.004	0.016

Application note

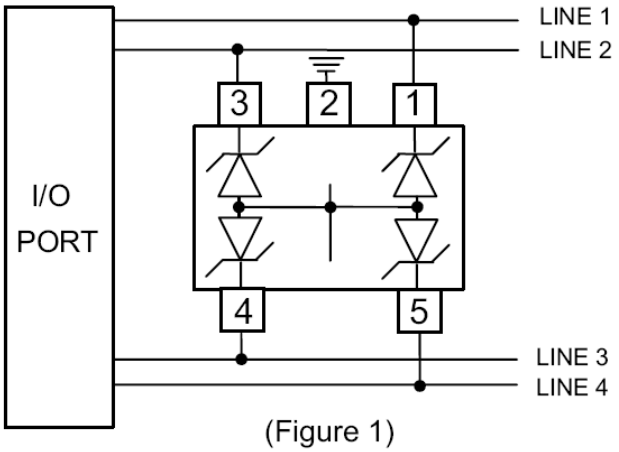
The **SES5VT353-5** Series is TVS arrays designed to protect I/O or data lines from the damaging effects of ESD or EFT. This product provides both unidirectional and bidirectional protection, with a surge capability of 100 Watts Ppp per line for an 8/20μs wave shape and ESD protection > 25 kilovolts.

COMMON-MODE UNIDIRECTIONAL CONFIGURATION (Figure 1)

The **SES5VT353-5** Series provides up to 4 lines of protection in a common-mode unidirectional configuration as depicted in Figure 1.

Circuit connectivity is as follows:

- Line 1 is connected to Pin 1.
- Line 2 is connected to Pin 3.
- Line 3 is connected to Pin 4.
- Line 4 is connected to Pin 5.
- Pin 2 is connected to ground.



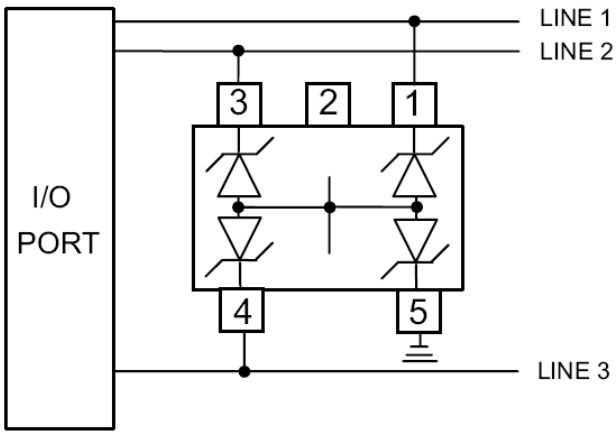
(Figure 1)

COMMON-MODE BIDIRECTIONAL CONFIGURATION (Figure 2)

The **SES5VT353-5** Series provides up to 3 lines of protection in a common-mode bidirectional configuration as depicted in Figure 2.

Circuit connectivity is as follows:

- Line 1 is connected to Pin 1.
- Line 2 is connected to Pin 3.
- Line 3 is connected to Pin 4.
- Pin 5 is connected to ground.
- Pin 2 is not connected.



(Figure 2)

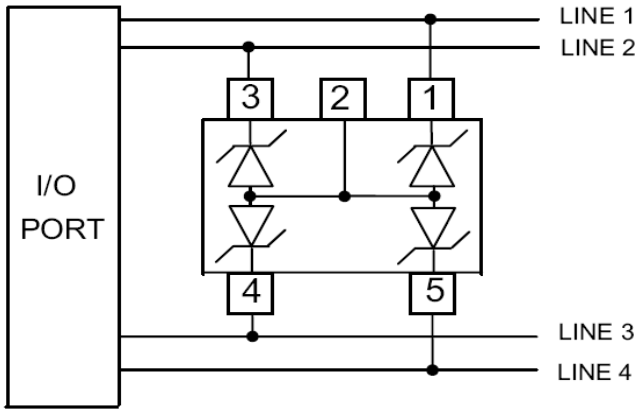
Application note

DIFFERENTIAL-MODE BIDIRECTIONAL CONFIGURATION (Figure 3)

The SES5VT353-5 Series provides up to 4 lines of protection in a differential-mode bidirectional configuration as depicted in Figure 3.

Circuit connectivity is as follows:

- Line 1 is connected to Pin 1.
- Line 2 is connected to Pin 3.
- Line 3 is connected to Pin 4.
- Line 4 is connected to Pin 5.
- Pin 2 is not connected.



(Figure 3)

Circuit board layout and protection device placement:

Circuit board layout is critical for the suppression of ESD transients.
The following guidelines are recommended:

1. Place the protection device as close to the input terminal or connector as possible.
2. The path length between the protection device and the protected line should be minimized.
3. Keep parallel signal paths to a minimum.
4. Avoid running protection conductors in parallel with unprotected conductor.
5. Minimize all printed-circuit board conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Ground planes should be used whenever possible. For multilayer printed-circuit boards, use ground vias.

Revision History

Revision	Date	Changes
1.0	2008-7-3	-