IXYS RF

IXZ4DF12N100
RF Power MOSFET & DRIVER

Driver / MOSFET Combination
DEIC-515 Driver combined with a DE375-102N12A MOSFET
Gate driver matched to MOSFET

1000 Volts
12 A
0.7 Ohms

Features

- Isolated Substrate
  - high isolation voltage (>2500V)
  - excellent thermal transfer
  - Increased temperature and power cycling capability
- IXYS advanced Z-MOS process
- Low $R_{DS(on)}$
- Very low insertion inductance (<2nH)
- No beryllium oxide (BeO) or other hazardous materials
- Built using the advantages and compatibility of CMOS and IXYS HDMOS™ processes
- Latch-Up Protected
- Low Quiescent Supply Current

Advantages

- Optimized for RF and high speed
- Easy to mount—no insulators needed
- High power density
- Single package reduces size and heat sink area

Applications

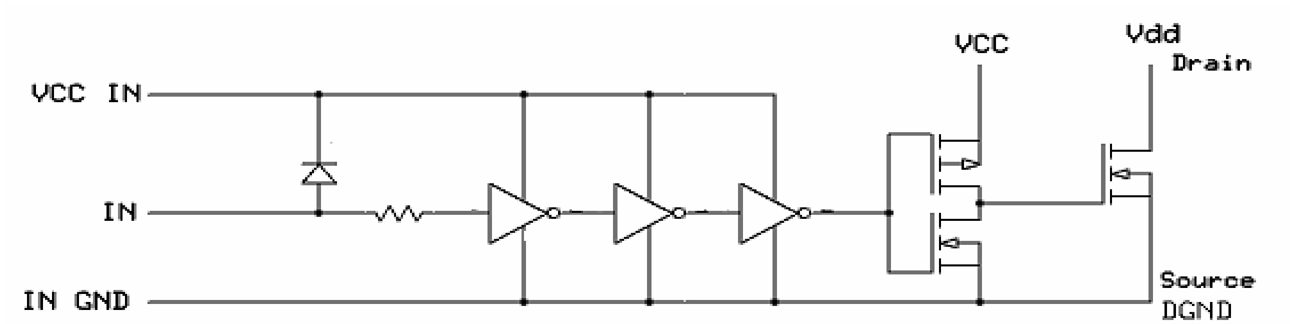
- Class D or E Switching Amplifier
- Multi MHz Switch Mode Power Supplies (SMPS)

Description

The IXZ4DF12N100 is a CMOS high speed high current gate driver and a MOSFET combination specifically designed Class D, E, HF, RF applications at up to 40MHz, as well as other applications. The IXZ4DF12N100 in pulse mode can provide 72A of peak current while producing voltage rise and fall times of less than 5ns, and minimum pulse widths of 8ns. The input of the driver is fully immune to latch up over the entire operating range. Designed with small internal delays, the IXZ4DF12N100 is suitable for higher power operation where combiners are used. Its features and wide safety margin in operating voltage and power make the IXZ4DF12N100 unmatched in performance and value.

The IXZ4DF12N100 is packaged in DEIs low inductance RF package incorporating DEI's RF layout techniques to minimize stray lead inductances for optimum switching performance. The IXZ4DF12N100 is a surface-mountable device.

Figure 1.
Functional Diagram



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Device Specifications

Parameter	Value
Maximum Junction Temperature	150°C
Operating Temperature Range	- 40°C to 85°C
Weight	5.5g

Symbol	Test Conditions	Maximum Ratings
f_{MAX}	I_D = 0.5I_{DM25}	40MHz
V_{DSS}		1000V
V_{CC}, V_{CCIN}		20V
I_{DSS}	V_{DS} = 0.8V_{DSS} T_J = 25C V_{GS} = 0V T_J = 125C	50uA 1mA
I_{DM25}	T_C = 25°C	12A
I_{DM}	T_C = 25°C, Pulse limited by T_{JM}	72A
I_{AR}	T_C = 25°C	12A
P_T (MOSFET and Driver)	T_C = 25°C	TBD 500W
R_{thJC}		0.25 °C/W
R_{thJHS}		TBD °C/W

Device Performance

Symbol	Test Condition	Minimum	Typical	Maximum
$R_{ds(ON)}$	V_{CC} = 15V, I_D = 0.5I_{DM25} Pulse Test, t ≤ 300µS, Duty Cycle ≤ 2%		0.7 Ω	
V_{CC}, V_{CCIN}		8V	15V	20V
IN (Signal Input)		- 5V		V_{CCIN}+0.3V
V_{IH} (High Input Voltage)		V_{CCIN} -2V		V_{CCIN}+0.3V
V_{IL} (Low Input Voltage)			0.8V	
Z_{IN}	f = 1MHz		7960 Ω	
C_{stray}	f = 1MHz Any one pin to the back plane metal		46pf	
C_{OSS}	V_{GS} = 0V, V_{DS} = 0.8$V_{DSS(max)}$, f =1MHz		150pf	
t_{ONDLY}	T_C = 25°C V_{CC}, V_{CCIN} , V_{IN} = 15V 1µS Pulse, V_{DS}= 50V, R_L = 2.5Ω		20nS	
t_{OFFDLY}			22.6nS	
t_R	T_C = 25°C V_{CC}, V_{CCIN}, V_{IN} = 15V 1µS Pulse, V_{DS} = 50V, R_L = 2.5Ω		3nS	
t_F			4.5nS	

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Fig. 2

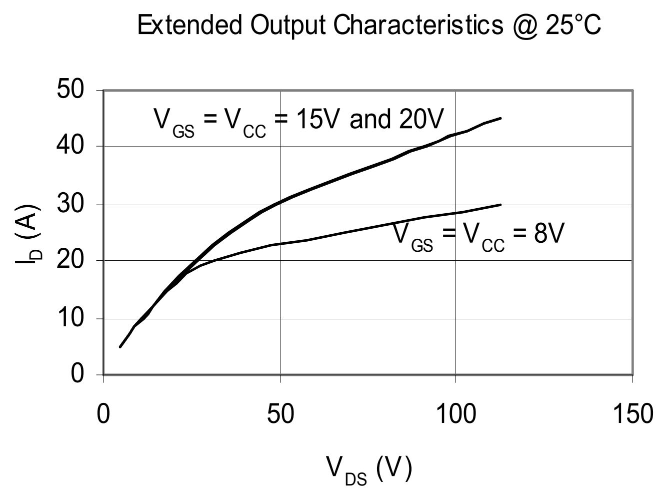


Fig. 3

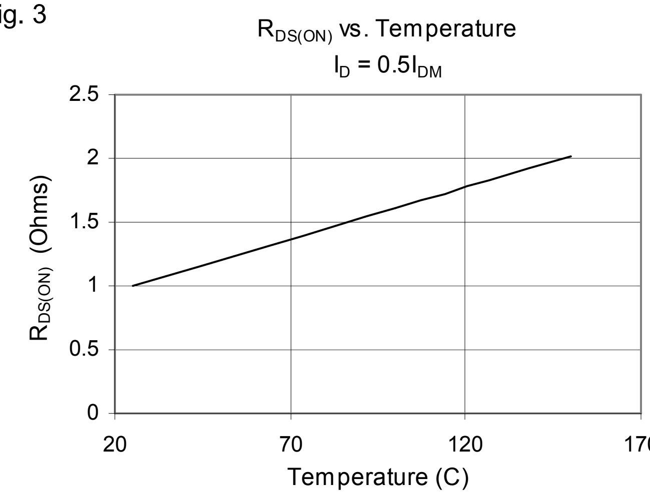


Fig. 4

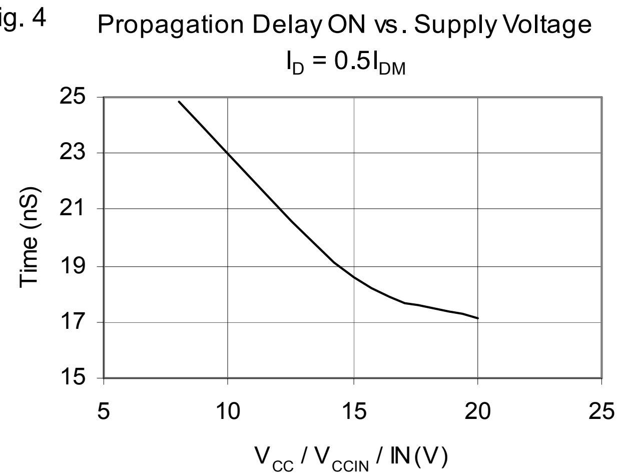
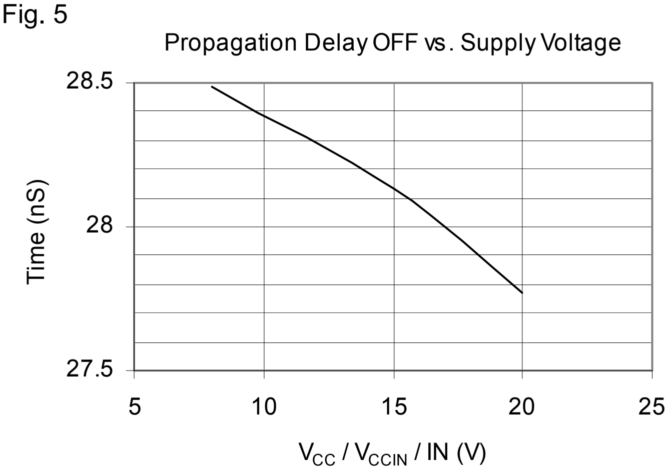


Fig. 5



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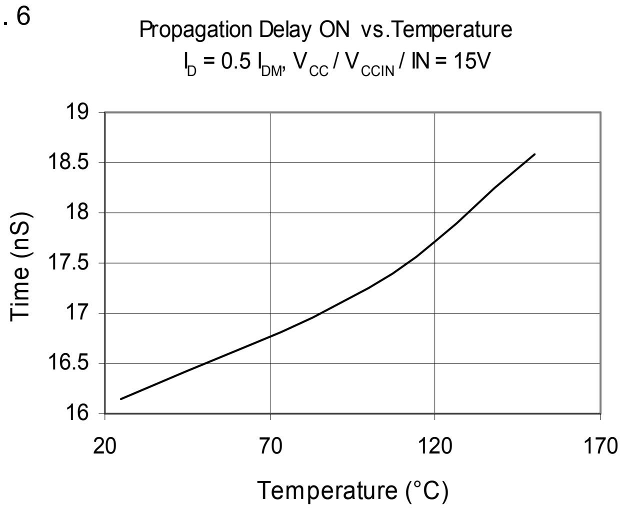

Fig. 7

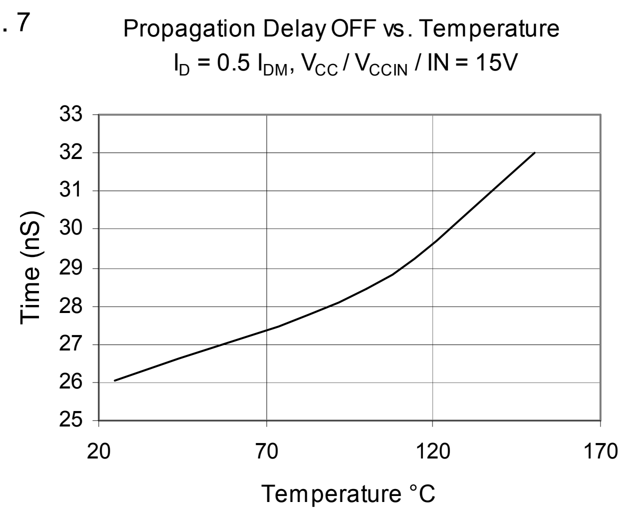

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Fig. 8

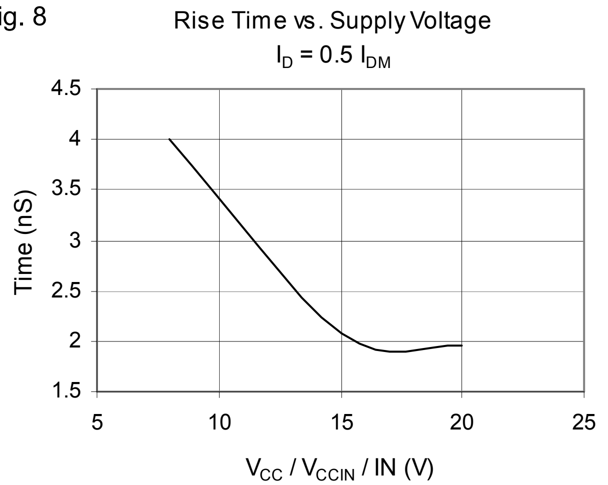

Fig. 9

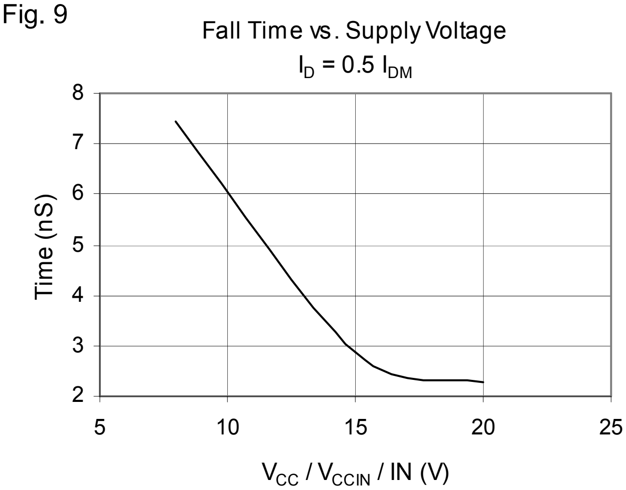

Fig. 10

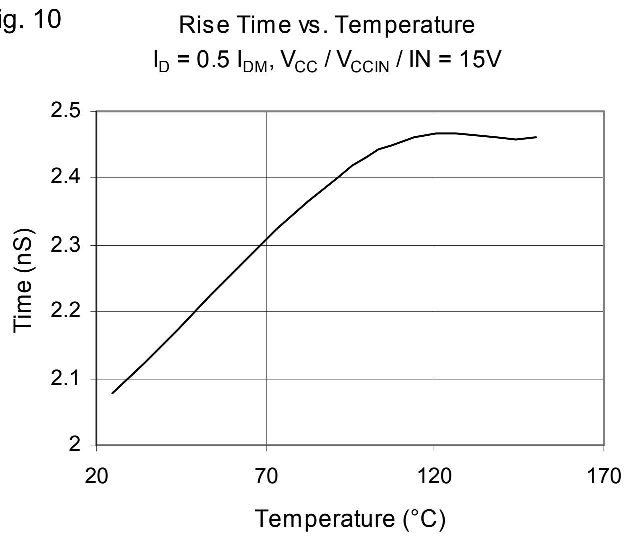

Fig. 11

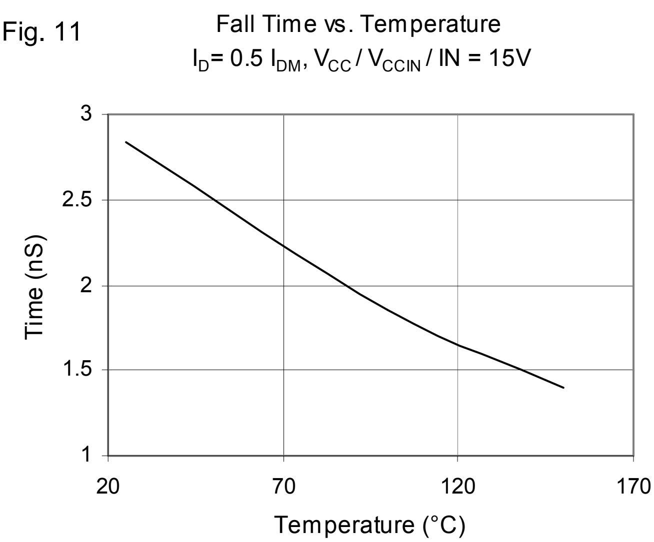

Fig. 12

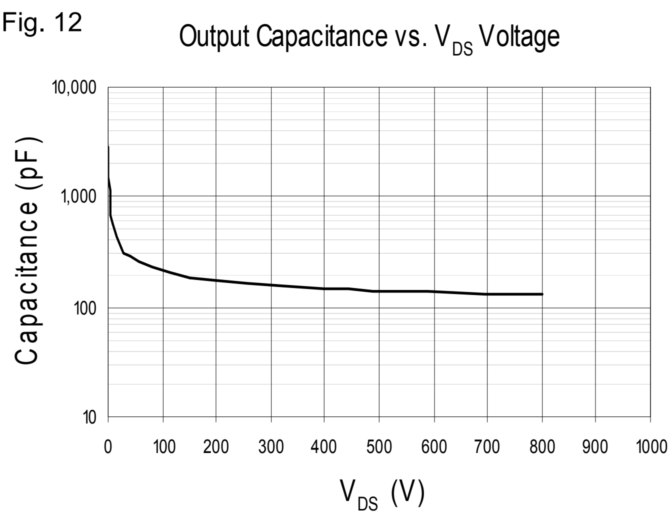

Fig. 13

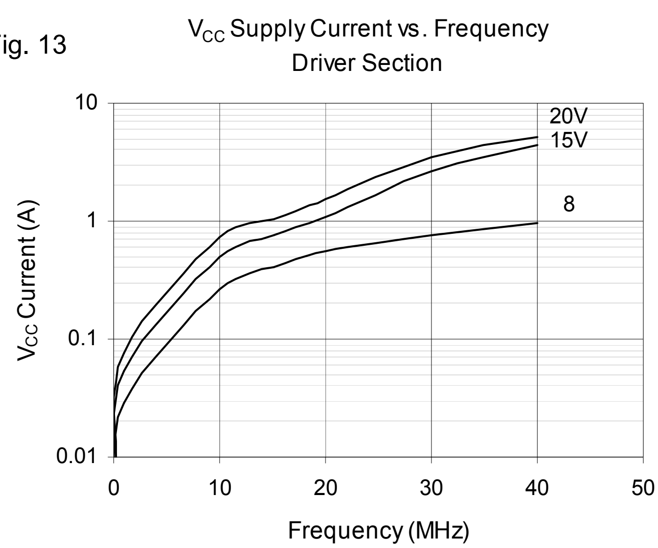

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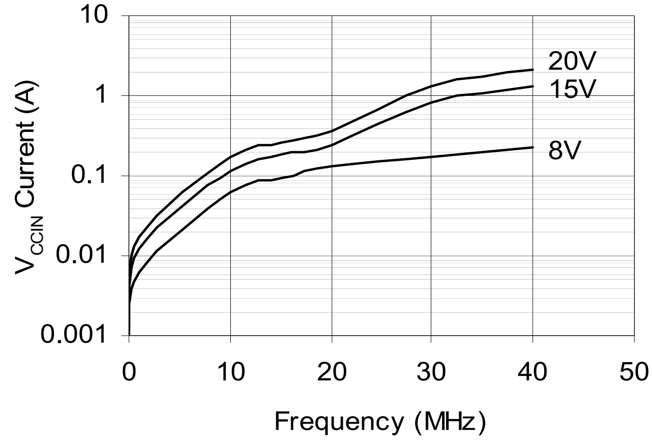
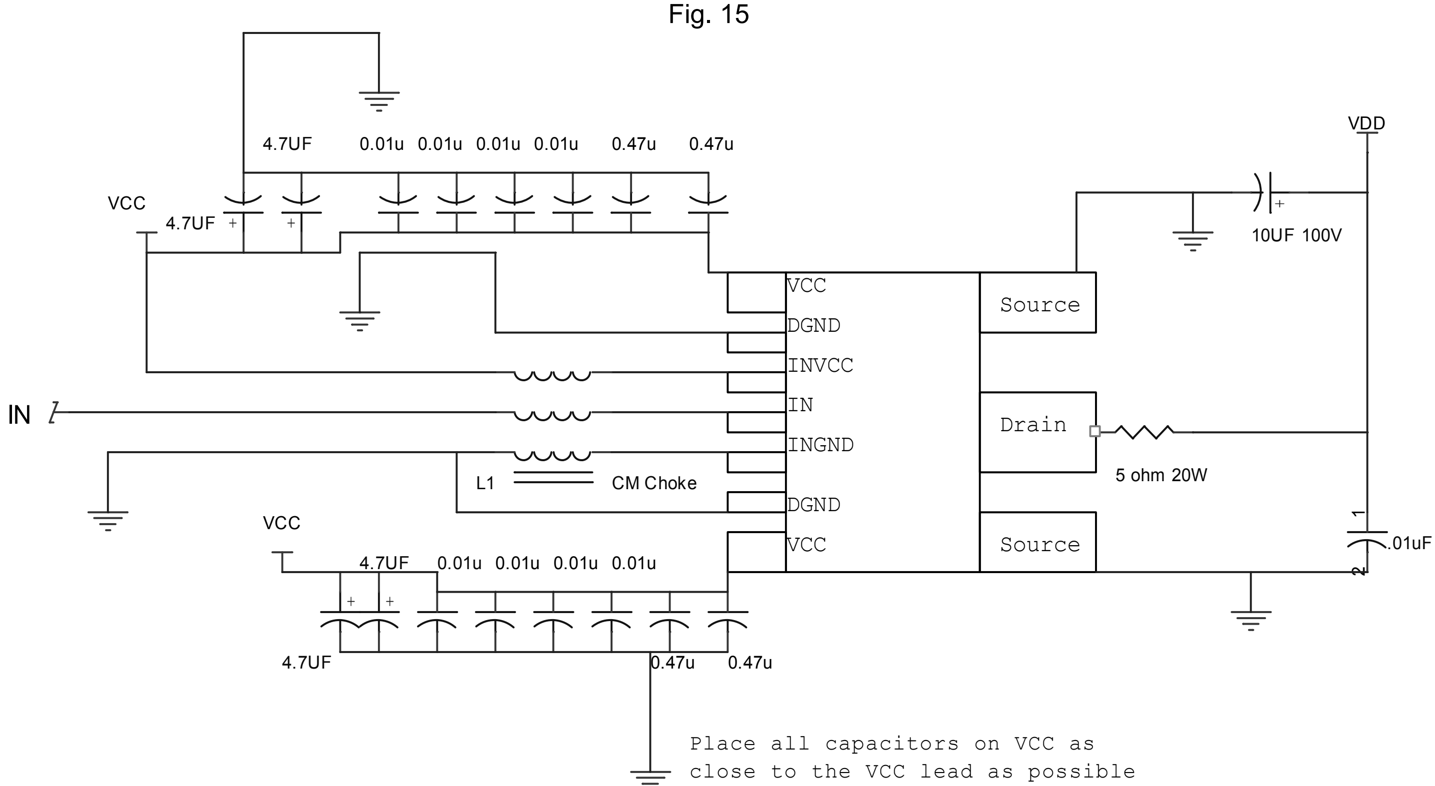
Fig. 14



Test Circuit

Fig. 15



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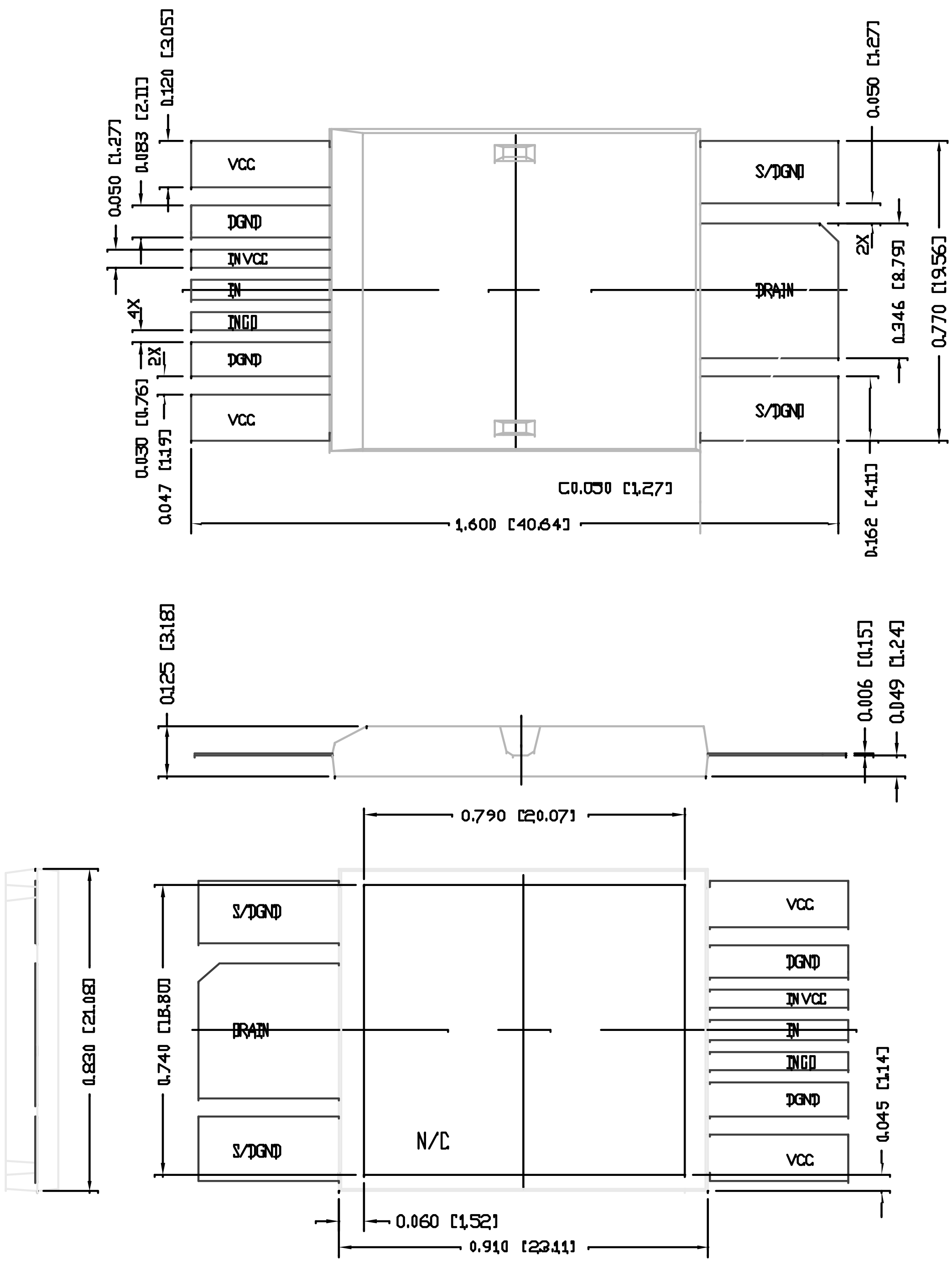
Lead Description

SYMBOL	FUNCTION	DESCRIPTION
Drain	MOSFET Drain	Drain of Power MOSFET.
Source	MOSFET Source	Source of Power MOSFET. This connection is common to DGND.
VCC	Driver Section Supply Voltage	Power supply input for the driver output section. These leads provide power to the output section of the DEIC515 driver. Both leads must be connected.
VCCIN	Input Section Supply Voltage	Input for the positive input section power-supply voltage. This lead provides power to the input section of the DEIC515 driver. This lead should not be directly connected to VCC.
IN	Input	Input signal.
DGND	Power Driver Ground	The system ground leads. Internally connected to all circuitry, these leads provide ground reference for the entire chip. These leads should be connected to a low noise analog ground plane for optimum performance.
INGND	Input Section Ground	The input section ground lead. This lead is a Kelvin connection internally connected to DGND. This lead must not be connected to DGND as excessive current can damage this lead.

Fig. 16 IXZ4DF12N100 Package Outline



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