

R2A20115SP

Power Factor Correction Controller IC

REJ03D0923-0100

Rev.1.00

Oct 06, 2009

Description

R2A20115 is a power-factor correction (PFC) controller IC, which employs continuous conduction mode as PFC control mode. Various kinds of functions such as constant power limit, overvoltage detection, overcurrent detection, soft start function, feedback-loop open detection, and the function holding its operation through momentary outage (PFC hold function) are incorporated in a single chip. These functions reduce external circuitry.

The constant power limit function significantly reduces "coil vibration", which is caused by the operation of a conventional overcurrent detection circuit when the system is overloaded.

The PFC hold function enables quick recovery by keeping PFC operation active for a certain duration (hold time) during momentary outage/power failure. The hold time can be adjusted by an external capacitor.

This IC provides the separated pin used for detecting overcurrent, so that, the preset current value range for overcurrent detection becomes wider than before.

The shutdown function with latch mode is also implemented.

A soft-start control pin is provided for the easy adjustment of soft-start operation.

And also the dynamic over voltage protection function integrated in this IC reduces overshooting of the output voltage, which might occur for the duration of startup, recovery after momentary power failure and just after a sudden variation of a load.

Features

- Maximum ratings
 - Power-supply voltage V_{cc} : 24 V
 - Operating junction temperature T_{jopr} : - 40 to 150°C
- Electrical characteristics
 - VREF output voltage V_{REF} : 5.0 V \pm 1.6%
 - UVLO operation start voltage V_H : 10.4 \pm 0.7 V
 - UVLO operation stop voltage V_L : 8.9 \pm 0.5 V
 - PFC output maximum ON duty $D_{max-out}$: 95% (typ.)
- Functions
 - Constant power limit function
 - Continuous conduction mode
 - Hold function of PFC operation on momentary outage (PFC hold function)
 - Overvoltage detection
 - Overcurrent detection
 - Soft start
 - Feedback loop disconnection detection
 - IC shutdown function
 - Dynamic OVP (Over Voltage Protection)
 - Package lineup: SOP-16

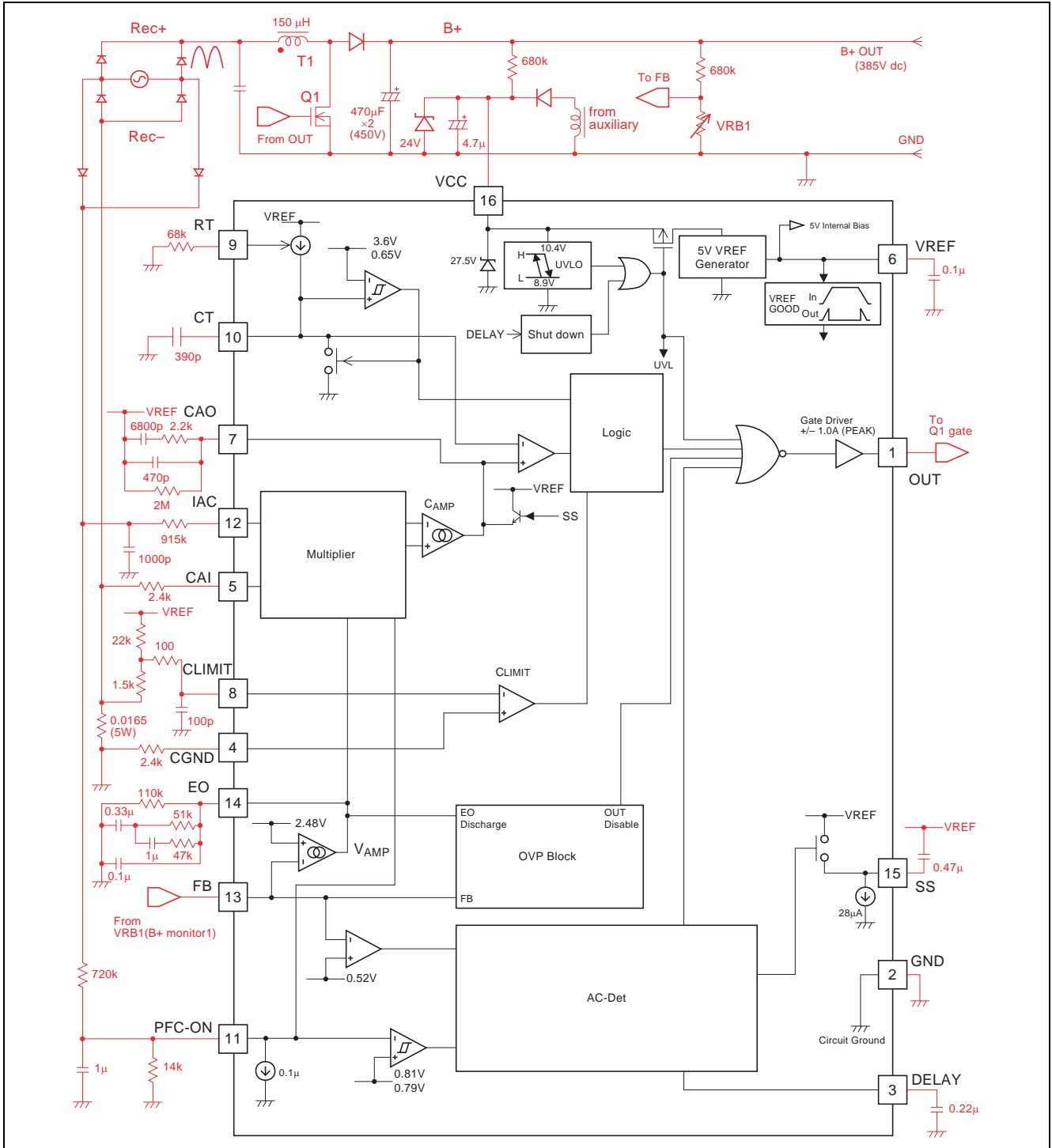
Applications

- Flat panel display
- Projector
- Desktop PC
- White goods

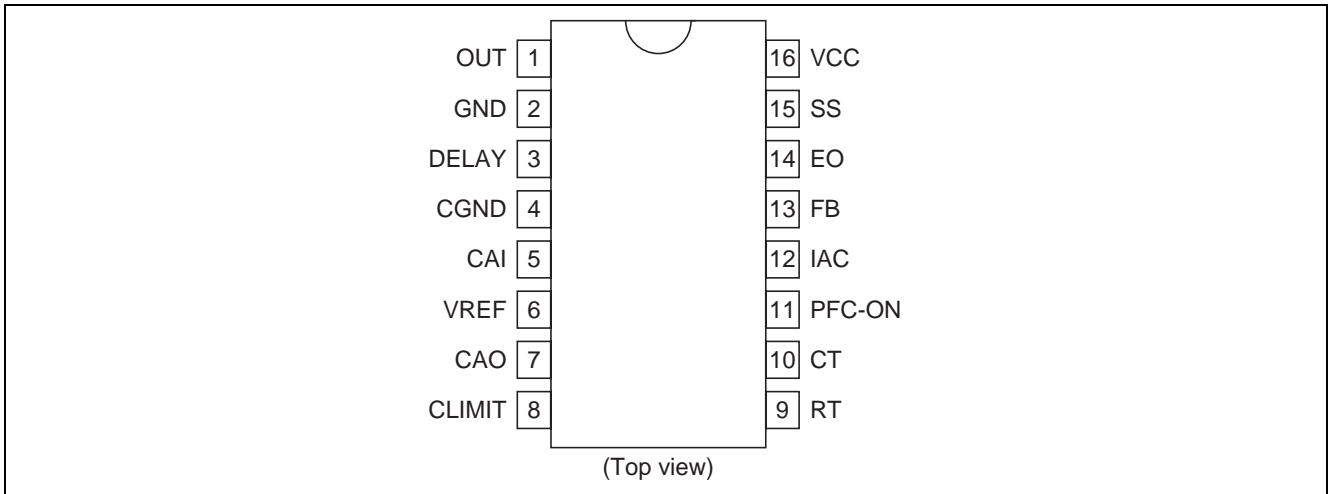
Ordering Information

Part No.	Package Name	Package Code	Taping Spec.
R2A20115SPW0	FP-16DAV	PRSP0016DH-B	2000 pcs./one taping product

System Diagram



Pin Arrangement



Pin Description

Pin No.	Pin Name	I/O	Function
1	OUT	Output	Power MOS FET gate driver output
2	GND	—	Ground
3	DELAY	Input/Output	Hold time adjust and IC shutdown
4	CGND	Input	Non-inverting input of current amplifier
5	CAI	Input/Output	Inverting input of current amplifier and Current output for PFC control
6	VREF	Output	Reference voltage output
7	CAO	Output	Current amplifier output
8	CLIMIT	Input	Overcurrent detection
9	RT	Input/Output	Timing resistor for settings of operational frequency, and the maximum CAI pin and DELAY pin current
10	CT	Output	Timing capacitor for operational frequency adjust
11	PFC-ON	Input	Detection of input AC voltage level
12	IAC	Input	Detection of input AC waveform
13	FB	Input	Voltage amplifier input
14	EO	Output	Voltage amplifier output
15	SS	Output	Timing capacitor for soft-start time adjust
16	VCC	Input	Power supply voltage input

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit	Note
Supply voltage	VCC	24	V	
OUT peak current	Ipk-out	±1.0	A	3
OUT DC current	I _{dc-out}	±0.1	A	
Terminal voltage	Vi-group1	-0.3 to V _{cc}	V	4
	Vi-group2	-0.3 to V _{ref}	V	5
CAO voltage	V _{cao}	-0.3 to V _{caoh}	V	
EO voltage	V _{eo}	-0.3 to V _{eah}	V	
DELAY voltage	V _{delay}	-0.3 to +6.5	V	
CAI voltage	Vi-cs	-1.5 to +0.3	V	
RT current	I _{rt}	-200	μA	
IAC current	I _{iac}	0.6	mA	
VREF current	I _{o-ref}	-5	mA	
Power dissipation	P _t	1	W	6
Operating junction temperature	T _{j-opr}	-40 to +150	°C	
Storage temperature	T _{stg}	-55 to +150	°C	

- Notes: 1. Rated voltages are with reference to the GND pin.
 2. For rated currents, inflow to the IC is indicated by (+), and outflow by (-).
 3. The transient current when driving capacitive load.
 4. This is the rated voltage for the following pin:
 OUT.
 5. This is the rated voltage for the following pins:
 CGND, VREF, CLIMIT, RT, CT, PFC-ON, IAC, FB, SS
 6. Thermal resistance of packages

Package	θ _{ja}	θ _{jc}	Note
SOP16	120°C/W	—	40 × 40 × 1.6 [mm], Mounted on a glass epoxy printed board with 10% wiring density
	—	35°C/W	Infinite heat sink

Electrical Characteristics

(Ta = 25°C, VCC = 12 V, RT = 27 kΩ, CT = 1000 pF)

	Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Supply	Start threshold	VH	9.7	10.4	11.1	V	
	Shutdown threshold	VL	8.4	8.9	9.4	V	
	UVLO hysteresis	dVUVL	1.0	1.5	2.0	V	
	Startup current	Is	75	100	145	μA	VCC = 9.5 V
	Is temperature stability	dIs/dTa	—	-0.3	—	%/°C	*1
	Operating current	Icc	2.4	3.4	4.4	mA	IAC = 0 A, CL = 0 F
VREF	Output voltage	Vref	4.92	5.00	5.08	V	Isource = 1 mA
	Line regulation	Vref-line	—	5	20	mV	Isource = 1 mA, VCC = 12 V to 23 V
	Load regulation	Vref-load	—	5	20	mV	Isource = 1 mA to 5 mA
	Temperature stability	dVref	—	±80	—	ppm/°C	Ta = -40 to 125°C *1
Oscillator	Initial accuracy	fout	55.0	61.0	67.0	kHz	Measured pin: OUT
	fout temperature stability	dfout/dTa	—	±0.1	—	%/°C	Ta = -40 to 125°C *1
	fout voltage stability	fout-line	-1.5	0.5	1.5	%	VCC = 12 V to 18 V
	CT peak voltage	Vct-H	—	3.6	4.0	V	*1
	Ramp valley voltage	Vct-L	—	0.65	—	V	*1
	RT voltage	Vrt	1.18	1.22	1.26	V	
Soft start	Sink current	Iss	17.0	28.0	39.0	μA	SS = 2 V
Current limit	Threshold voltage	VCL	-15	0	15	mV	
	Delay to output	td-CL	—	200	300	ns	CLIMIT = 1 to -0.3 V
VAMP	Feedback voltage	Vfb	2.44	2.48	2.52	V	FB-EO Short
	Input bias current	Ifb	-0.3	-0.15	0	μA	Measured pin: FB
	Open loop gain	Av-v	—	53	—	dB	*1
	High voltage	Veoh	4.75	4.9	5.05	V	FB = 2.3 V, EO: Open
	Low voltage	Veol	—	0.1	0.3	V	FB = 2.7 V, EO: Open
	Source current	Isrc-eo	-180	-120	-80	μA	FB = 1.0 V, EO = 2.5 V *1
	Sink current	Isrc-eo	—	350	—	μA	FB = 4.0 V, EO = 2.5 V *1
	Transconductance	Gm-v	120	180	240	μA/V	FB = 2.5 V, EO = 2.5 V
CAMP	Input offset voltage	Vio-ca	-10	—	0	mV	*1
	Open loop gain	Av-ca	—	55	—	dB	*1
	High voltage	Vcaoh	4	4.5	5	V	
	Low voltage	Vcaol	—	0.1	0.3	V	
	Source current	Isrc-ca	-150	-105	-67	μA	CAO = 2.5 V
	Sink current	Isrc-ca	67	105	150	μA	CAO = 2.5 V
	Transconductance	Gm-c	420	660	890	μA/V	*1

Note: 1. Design spec.

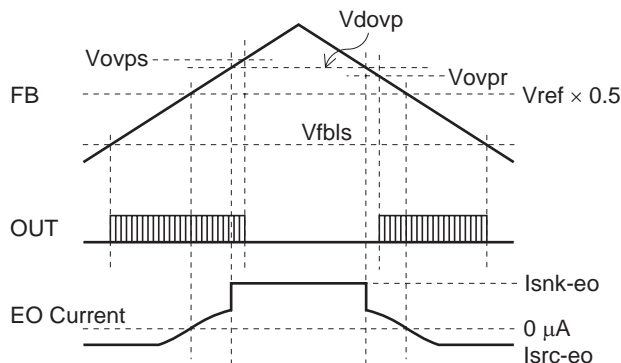
Electrical Characteristics (cont.)

(Ta = 25°C, VCC = 12 V, RT = 27 kΩ, CT = 1000 pF)

	Item	Symbol	Min	Typ	Max	Unit	Test Conditions
IAC/ Multiplier	IAC pin voltage	Viac	0.4	1.4	2.0	V	IAC = 100 μA
	Imo current 1	Imo1	-57	-47	-37	μA	EO = 2.5 V, IAC = 150 μA PFC-ON = 1.2 V
	Imo current 2	Imo2	-158	-125	-91.5	μA	EO = Vcaoh, IAC = 150 μA PFC-ON = 1.2 V
	Imo current 3	Imo3	-35.5	-30	-24.5	μA	EO = 2.5 V, IAC = 375 μA PFC-ON = 2.5 V
	Imo current 4	Imo4	-98.5	-80	-61.5	μA	EO = Vcaoh, IAC = 375 μA PFC-ON = 2.5 V
OUT	Minimum duty cycle	Dmin-out	—	—	0	%	CAO = 4.0 V
	Maximum duty cycle	Dmax-out	90	95	98	%	CAO = 0 V
	Rise time	tr-out	—	30	100	ns	CL = 1000 pF
	Fall time	tf-out	—	30	100	ns	CL = 1000 pF
	Low voltage	Vol1-out	—	0.08	0.2	V	Iout = 20 mA
		Vol2-out	—	0.5	2.0	V	Iout = 200 mA (Pulse test)
		Vol3-out	—	0.07	0.7	V	Iout = 10 mA, VCC = 5 V
High voltage	Voh1-out	11.5	11.9	—	V	Iout = -20 mA	
	Voh2-out	10.0	11.0	—	V	Iout = -200 mA (Pulse test)	
Shut down	Shut down voltage	Vshut	3.30	4.00	4.70	V	Input: DELAY
	Reset voltage	Vres	—	—	4.0	V	Input: Vcc
	Shut down current	Ishut	45	95	190	μA	VCC = 9 V
Supervisor	PFC enable voltage	Von-pfc	0.73	0.81	0.89	V	Input pin: PFC-ON
	PFC disable voltage	Voff-pfc	0.71	0.79	0.86	V	Input pin: PFC-ON
	PFC disable delay threshold voltage	Vd-pfc	1.10	1.20	1.30	V	Input pin: DELAY
	Input current	Ipfc-on	-1.0	-0.2	1	μA	PFC-ON = 2 V
	B+ OVP set voltage	dVovps	0.125	0.188	0.250	V	Input pin: FB *2
	B+ OVP reset voltage	dVovpr	0.010	0.050	0.100	V	Input pin: FB *2
	Dynamic OVP set/reset voltage	dVdovp	0.045	0.065	0.085	V	Input pin: FB *2
	FB low set voltage	Vfbls	0.47	0.52	0.57	V	Input pin: FB
	DELAY source current	Isrc-delay	-50.5	-45.5	-40.5	μA	DELAY = 1 V RT = 27 kΩ
	DELAY sink current	Isnk-delay	—	815	—	μA	DELAY = 1 V RT = 27 kΩ *1

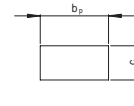
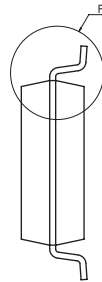
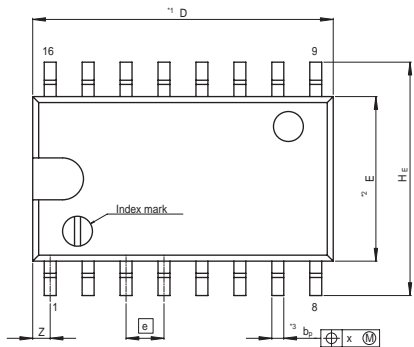
Notes: 1. Design spec.

- 2. $dVovps = Vovps - Vref \times 0.5$
 $dVovpr = Vovpr - Vref \times 0.5$
 $dVdovp = Vdovp - Vref \times 0.5$



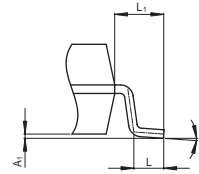
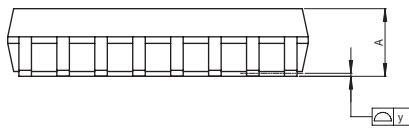
Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP16-5.5x10.06-1.27	PRSP0016DH-B	FP-16DAV	0.24g



Terminal cross section
(Ni/Pd/Au plating)

NOTE)
1. DIMENSIONS**1 (Nom)*AND**2
DO NOT INCLUDE MOLD FLASH.
2. DIMENSION**3*DOES NOT
INCLUDE TRIM OFFSET.



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	10.06	10.5
E	—	5.50	—
A ₂	—	—	—
A ₁	0.00	0.10	0.20
A	—	—	2.20
b _p	0.34	0.40	0.46
b ₁	—	—	—
c	0.15	0.20	0.25
c ₁	—	—	—
θ	0°	—	8°
H _E	7.50	7.80	8.00
Ⓜ	—	1.27	—
x	—	—	0.12
y	—	—	0.15
Z	—	—	0.80
L	0.50	0.70	0.90
L ₁	—	1.15	—

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