5V 120mA Automotive LDO Regulator with Watchdog

Description

The EM6156 offers a high level of integration by combining voltage regulation, voltage monitoring and software monitoring using a watchdog.

A comparator monitors the voltage applied at the VIN input comparing it with an internal voltage reference VREF. The power-on reset function is initialized after VIN reaches VREF and takes the reset output inactive after a delay TPOR. The reset output goes active low when the VIN voltage is less than VREF. The RESET output is guaranteed to be in a correct state for a regulated output voltage as low as 1.2V. The watchdog function monitors software cycle time and execution. If software clears the watchdog too slowly (incorrect execution) it will cause the system to be reset.

In EM6156, the voltage regulator has a low dropout voltage and a low quiescent current. The quiescent current increases only slightly in dropout prolonging battery life. Built-in protection includes a positive transient absorber for up to 45 V (load dump) and the ability to survive an unregulated input voltage of -42 V (reverse battery). The input may be connected to ground or to a reverse voltage without reverse current flowing from the output to the input.

Typical Operating Configuration

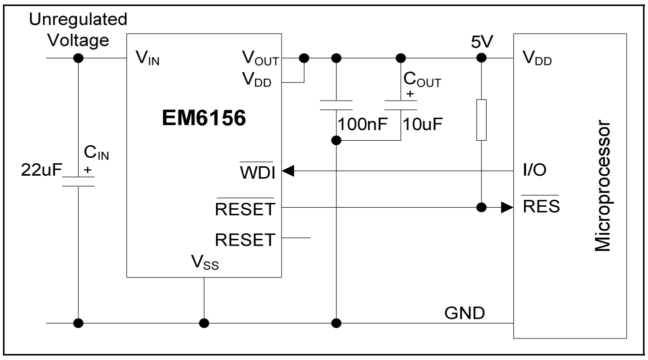


Fig. 1

Features

- -40°C to +125°C temperature range
- Highly accurate 5 V, 120 mA guaranteed output (actual maximum current depends on power dissipation)
- Output voltage tolerance <+/- 3%
- Low dropout voltage, typically 250 mV at 100 mA
- Unregulated DC input can withstand -42 V reverse battery and +45 V power transients
- Fully operational for unregulated DC input voltage up to 40 V and regulated output voltage down to 3.5 V
- No reverse output current
- Very low temperature coefficient for the regulated output
- Current limiting
- Four threshold voltages (2.9V, 3.0V, 4.4V, 4.6V)
- Several timeout reset periods (1.6ms, 25ms, **200ms**, 1600ms)
- Several watchdog timeout periods (6.2ms, 102ms, **1,6s**, 25,6s)
- Push pull or Open-drain active-low RESET output
- Reset output guaranteed for regulated output voltage down to 1.2 V
- Qualified according to AEC-Q100
- Green SO8 Exposed Pad Power Package (RoHS compliant)

Applications

- Automotive systems
- Industrial
- Home security systems

Block Diagram

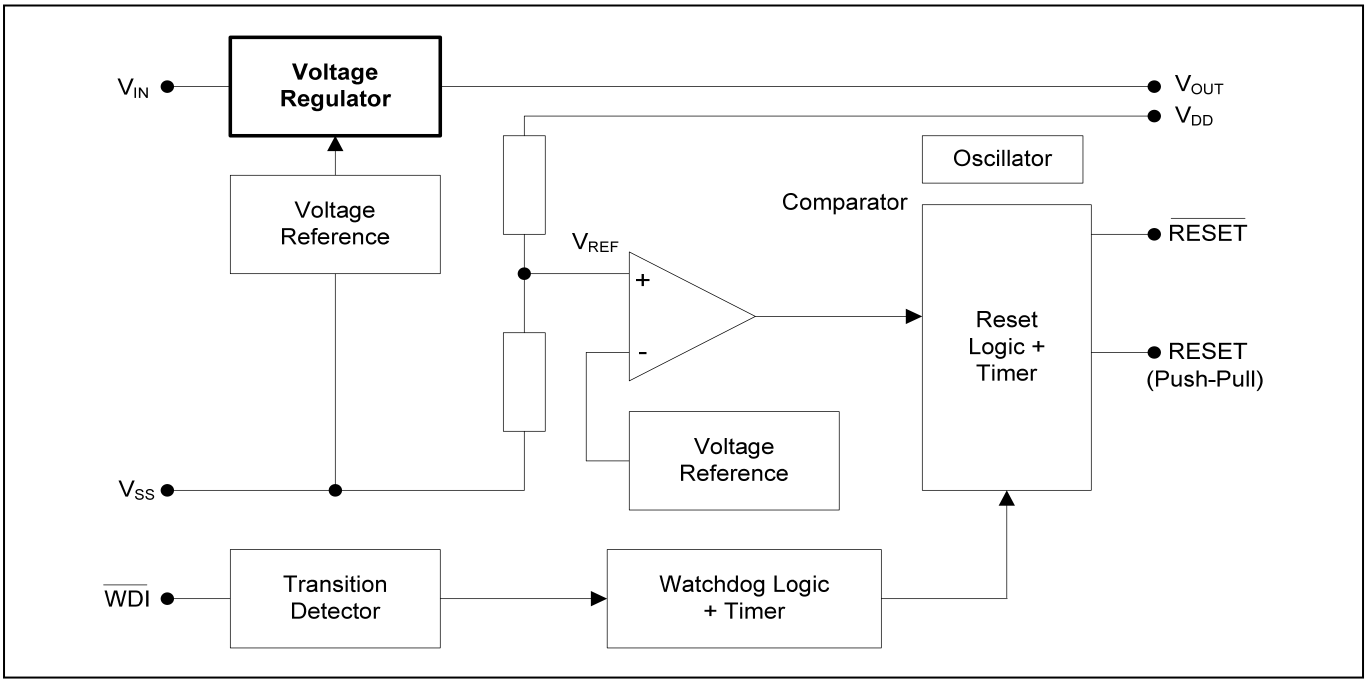
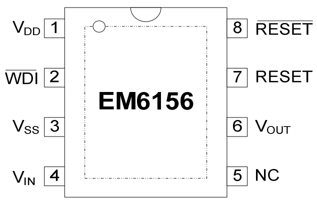


Fig. 2

Pin Assignment



Description

SO8 Exposed Pad	Name	Function
1	V_{DD}	Watchdog power supply
2	$\overline{WDI}$	Watchdog timer clear input signal
3	V_{SS}	Ground terminal
4	V_{IN}	Voltage regulator input
5	NC	Not connected
6	V_{OUT}	Voltage regulator output
7	RESET	RESET Output (Push-pull)
8	$\overline{RESET}$	$\overline{RESET}$ Output
	Exposed pad	Can be connected to V_{SS} or left floating

Table 1

Ordering Information

EM6156 L X ES8B - 4 4 +

RoHS Compliance:
+ = lead-free/green mold compliant

Reset Threshold Voltage:
1.3 = 2.93V **3.1** = 3.08V
4.4 = 4.40V **4.6** = 4.63V

Package & Bonding:
ES8A = Exposed Pad Power Package SO8 Stick 97pcs
ES8B = Exposed Pad Power Package SO8 Tape&Reel 2500pcs

Delays t_{POR} & t_{WD} :

t_{WD} [ms] \ t_{POR} [ms]	1.6	25	200	1600
6.2	**A**	**B**	**C**	**D**
102	**E**	**F**	**G**	**H**
1600	**J**	**K**	**L**	**M**
25600	**N**	**P**	**Q**	**R**

Reset Output Type:
X = Active-low /RESET push-pull
Y = Active-low /RESET open-drain
Z = Active-high RESET push-pull

Standard Versions

Part Number	Threshold Reset	Timeout Reset	Watchdog Timeout	Reset Output	Package	Delivery Form	Package Marking
EM6156LXES8B-4.4+	4.4V	200ms	1.6s	Active Low Push Pull	**ExPadSO8**	Tape & Reel, 2500 pcs	TBD

Note: the "+" symbol at the end of the part number means that this product is RoHS compliant (green).

Sample stock is generally held on **standard versions** only. Please contact factory for other versions not shown here and for availability of non standard versions.

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Continuous voltage at V_{IN} to V_{SS}	V_{IN}	-0.3V to +40V
Transients on V_{IN} for t < 100ms and duty cycle 1%	V_{TRANS}	Up to +45V
Max. voltage at any signal pin	V_{MAX}	V_{OUTPUT} + 0.3V
Min. voltage at any signal pin	V_{MIN}	V_{SS} – 0.3V
Reverse supply voltage on V_{IN}	V_{REV}	-42V
Storage temperature	T_{STO}	-65 to °150°C
ESD According to MIL-STD-883 method 3015.7	V_{Smax}	2000V

Table 2

Stresses above these listed maximum ratings may cause permanent damages to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Decoupling Methods

The input capacitor is necessary to compensate the line influences. A resistor of approx. 1Ω connected in series with the input capacitor may be used to damp the oscillation of the input capacitor and input inductance. The ESR value of the capacitor plays a major role regarding the efficiency of the decoupling. It is recommended also to connect a ceramic capacitor (100nF) directly at the IC's pins. In general the user must assure that pulses on the input line have slew rates lower than 1V/µs. On the output side, the capacitor is necessary for the stability of the regulation circuit. The stability is guaranteed for values of 10 µF or greater. It is especially important to choose a capacitor with a low ESR value. Tantalum capacitors are recommended.

See the notes related to Table 2. Special care must be taken in disturbed environments (automotive, proximity of motors and relays, etc).

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min	Max	Unit
Operating junction temperature	T_j	-40	+150	°C
V_{IN} voltage (Note 1)	V_{INPUT}	4.0	40	V
V_{OUT} voltage (Note 1,2)	V_{OUTPUT}	3.5	5.5	V
$\overline{RESET}$ guaranteed (Note 3)	V_{OUTPUT}	1.2		V
V_{OUT} output current (Note 4)	I_{OUTPUT}	120		mA
Comparator input voltage	V_{IN}	0	V_{OUT}	V
Package thermal resistance from junction to ambient: Exp. Pad SO8 150 MILS (Note 5)	$R_{th(j-a)}$	30	90	°C/W

Table 3

Note 1: Full operation guaranteed. To achieve the load regulation specified in Table 3, a 10 µF capacitor or greater is required on the V_{IN}, see Fig. 1b. The 10 µF must have an effective resistance ≤ 4 Ω and a resonant frequency above 500 kHz.

Note 2: A 10µF load capacitor and a 100 nF decoupling capacitor are required o the regulator output for stability. The 10 µF must have an effective series resistance of < 4 Ω and a resonant frequency above 500 kHz.

Note 3: For open drain output type, $\overline{RESET}$ must be pulled up externally to V_{OUT} even if it is unused.

Note 4: The output current will not apply to the full range of input voltage. Power dissipation that would require the EM6156 to work above the maximum junction temperature (+150 °C) must be avoided.

Note 5: The thermal resistance specified assumes the package is soldered to a PCB. A typical value of 51 °C/W has been obtained with a dual layer board, with the slug soldered to the heat-sink area of the PCB.

Electrical Characteristics

V_{IN} = 13.5V, C_{OUT} = 10µF + 100nF, C_{IN} = 2 µF, V_{DD} connected to V_{OUT}; T_A = -40 to +125 °C (Note 1), unless otherwise specified.

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Low drop Output Regulator							
Supply current (Note 6)	I_{SS}	I_L = 1 mA				412	µA
Supply current	I_{SS}	I_L = 100 mA			9	15	mA
Output voltage	V_{OUTPUT}	5 mA ≤ I_L ≤ 100 mA		4.9	5	5.10	V
Line regulation (Note 7)	V_{LINE}	6 V ≤ V_{IN} ≤ 100 mA, I_L = 5 mA			15	30	mV
Load regulation (Note 7)	V_L	5 mA ≤ I_L ≤ 100 mA, V_{IN} = 6V				40	mV
Dropout voltage (Note 8)	$V_{DROPOUT}$	I_L = 100 mA			250	500	mV
Current limit	I_{Lmax}	Output tied to V_{SS}, V_{IN} = 6V		120	160		mA
Reset							
Threshold hysteresis	V_{HYS}	T_A = +25°C		-	2.1%•V_{TH}	-	V
Reset timeout period	t_{POR}	V_{DD} from 0V to $V_{TH(typ)}$+15% T_A = +25°C (Note 2 & Note 4)	EM6156 C-G-L-Q	160	200	240	ms
			EM6156 A-E-J-N	0.7	1.56	3.8	
			EM6156 B-F-K-P	20	25	30	
			EM6156 D-H-M-R	1280	1600	1920	
Propagation delay time V_{DD} to $\overline{RESET}$ (RESET) delay	t_P	VDD drops from $V_{TH(typ)}$ +0.2V to $V_{TH(typ)}$-0.2V (Note 2). T_A = +25°C		2	70	255	µs
Open-drain $\overline{RESET}$ output voltage	V_{OL}	V_{DD} > 1V	I_{OL} = 100µA	-	-	0.3	V
		V_{DD} > 2.5V	I_{OL} = 1.5mA	-	-	0.3	
		V_{DD} > 5V	I_{OL} = 3mA	-	-	0.35	
Push-pull RESET / $\overline{RESET}$ output voltage	V_{OL}	V_{DD} > 2.5V	I_{OL} = 1.5mA	-	-	0.3	V
		V_{DD} > 5V	I_{OL} = 3mA	-	-	0.35	
		V_{DD} > 1V	I_{OL} = 100µA	-	-	0.3	
	V_{OH}	V_{DD} > 1.1V	I_{OL} = -30µA	0.8	-	-	V
		V_{DD} > 2.5V	I_{OL} = -1.5mA	2	-	-	
		V_{DD} > 5V	I_{OL} = -3mA	4	-	-	
Output leakage current	I_{LEAK}	Only for EM6156_Y (open-drain)		-	-	0.5	µA
Threshold voltage (Note 3)	V_{TH}	EM6156-2.9	+25°C	2.886	2.93	2.974	V
			-40°C to +85°C	2.784		3.091	
			-40°C to +125°C	2.731		3.103	
		EM6156-3.1	+25°C	3.034	3.08	3.126	
			-40°C to +85°C	2.926		3.249	
			-40°C to +125°C	2.871		3.262	
		EM6156-4.4	+25°C	4.334	4.40	4.466	
			-40°C to +85°C	4.180		4.642	
			-40°C to +125°C	4.101		4.660	
		EM6156-4.6	+25°C	4.561	4.63	4.699	
			-40°C to +85°C	4.399		4.885	
			-40°C to +125°C	4.315		4.903	
Watchdog Input (WDI)							
WDI Input low	V_{WDI} low	T_A = +25°C		-	-	0.3•V_{DD}	V
WDI Input high	V_{WDI} high			0.7•V_{DD}	-	-	V
Pulse width at WDI	t_{WP}			1	-	-	µs
Watchdog timeout period	t_{WD}	(Note 5)	EM6156 J-K-L-M	1280	1600	1920	ms
			EM6156 A-B-C-D	5	6.25	7.5	
			EM6156 E-F-G-H	80	100	120	
			EM6156 N-P-Q-R	20480	25600	30720	
High-level input current	I_{IH}	WDI connected to V_{DD}, T_A = +25°C		-	18	-	µA
Low-level input current	I_{IL}	WDI connected to V_{SS}, T_A = +25°C		-	8.3	-	µA

Table 4

Note 1: Production tested at +25°C only. Over temperature limits are guaranteed by design, not production tested.

Note 2: WDI and $\overline{RESET}$ open.

Note 3: Threshold voltage is specified for V_{DD} falling.

Note 4: Standard version for t_{POR} is 200ms (typ). Other option (1.6ms, 25ms, 1600ms) are available by mask option

Note 5: Standard version for t_{WD} is 1600ms (typ). Other option (6.2ms, 102ms, 25.6s) are available by mask option

Note 6: If INPUT is connected to V_{SS}, no reverse current will flow from the OUTPUT to the INPUT.

Note 7: Regulation is measured at constant junction temperature using pulse testing with a low duty cycle.

Note 8: The dropout voltage is defined as the INPUT to OUTPUT differential, measured with the input voltage equal to 5.0 V.

Timing Waveforms

Watchdog Timeout Period

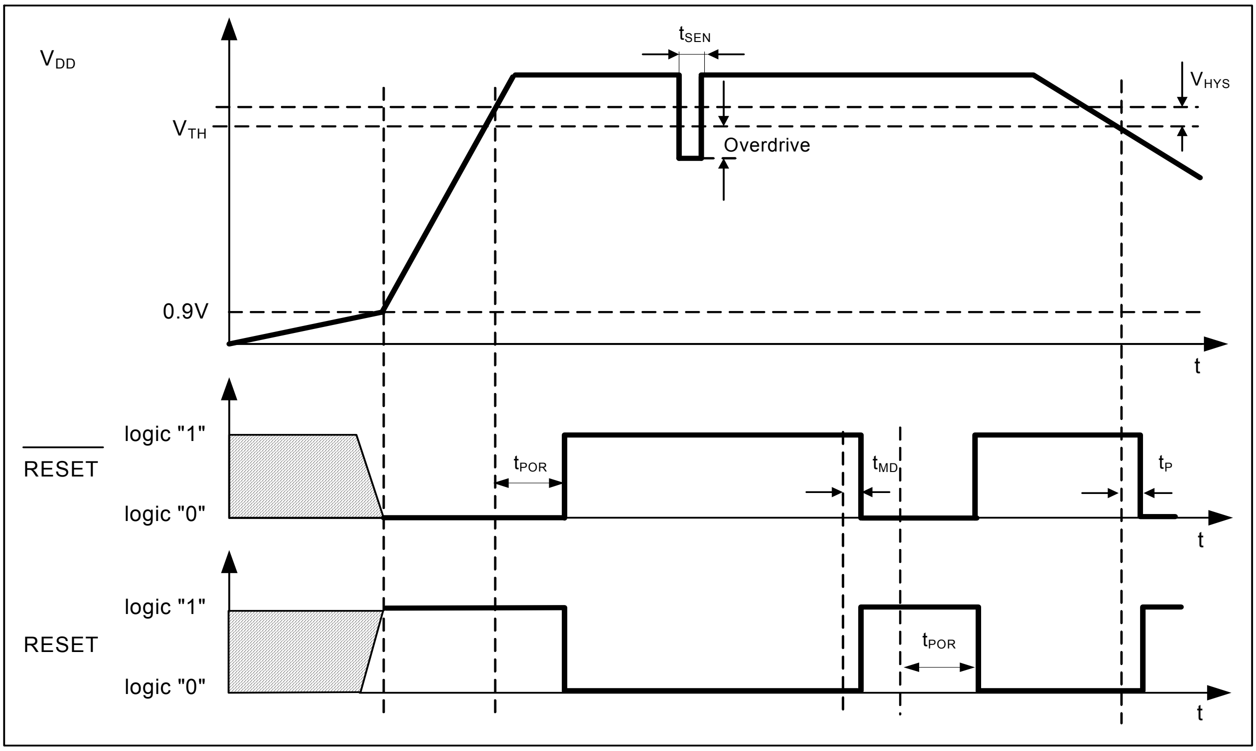


Fig. 3

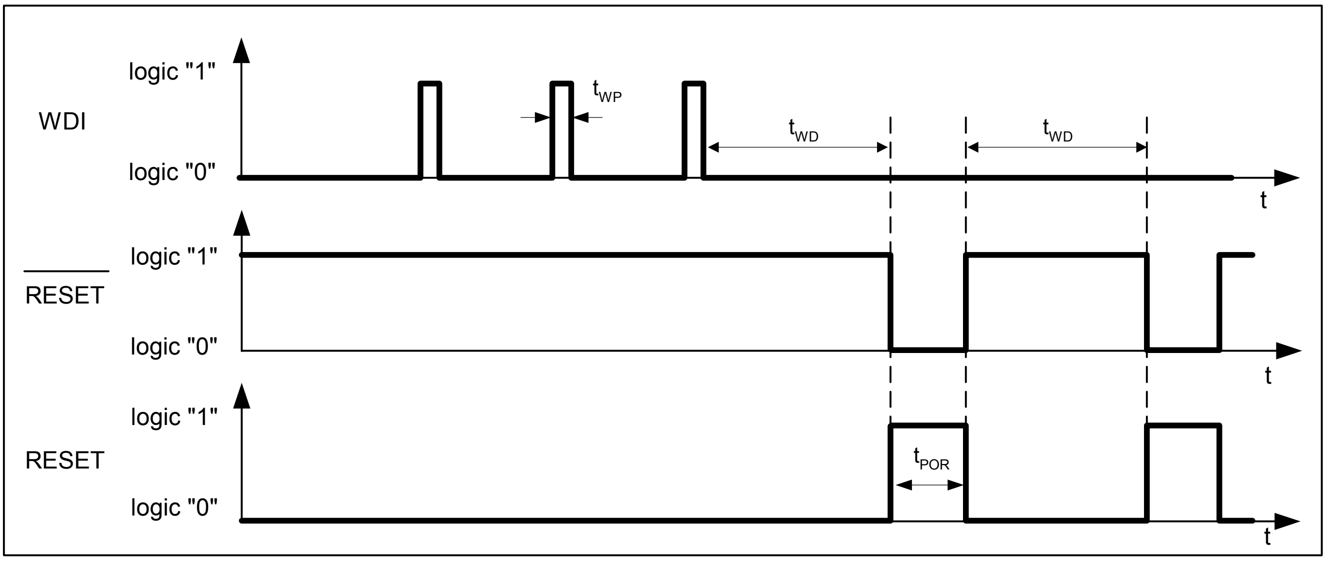


Fig. 4

Note 9: t_{SEN} = Maximum Transient Duration. Please refer to figure on the next page.
Note 10: Overdrive = V_{TH} -V_{DD}. Please refer to figure on the next page.

Typical Operating Characteristics

(Typical values are at T_A=+25°C unless otherwise noted. WDI, $\overline{\text{RESET}}$ and RESET open.)

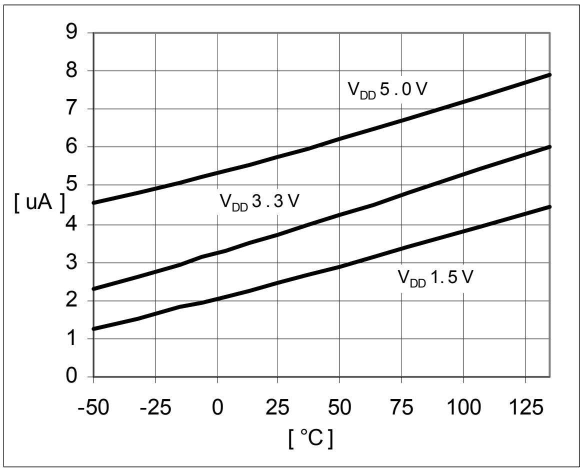


Fig. 5

I_{DD} vs. Temperature

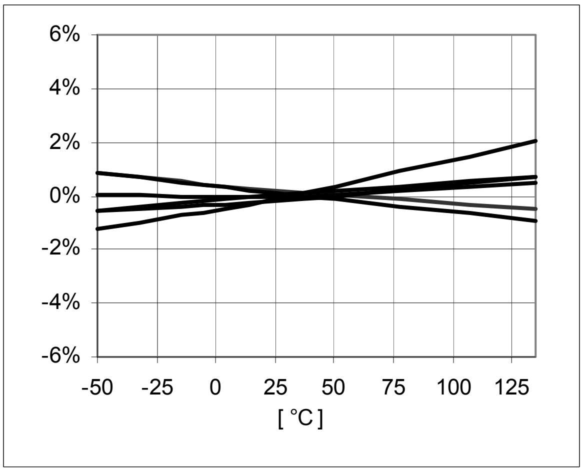


Fig. 6

Threshold Voltage Variation vs. Temperature (normalized)

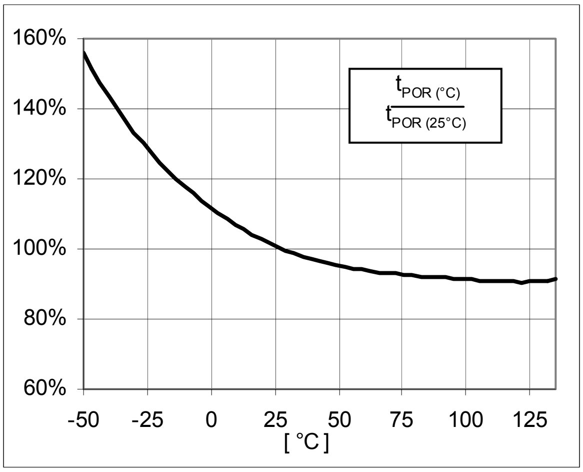


Fig. 7

Reset Timeout Period t_{POR} vs. Temperature (normalized with respect to $t_{POR\ 25°C}$)

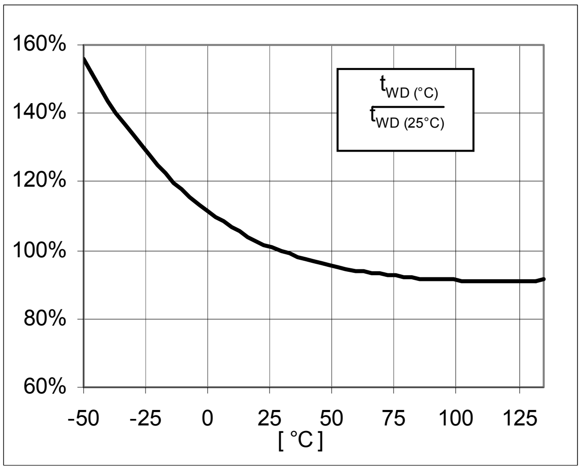


Fig. 8

Watchdog Timeout Period t_{WD} vs. Temperature (normalized with respect to $t_{WD\ 25°C}$)

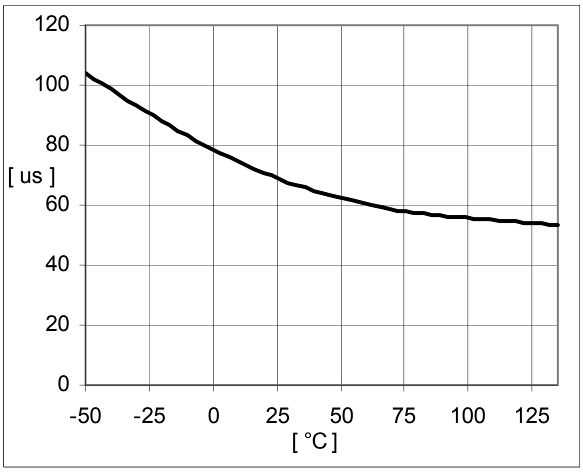


Fig. 9

Propagation Time t_{PHL} vs. Temperature

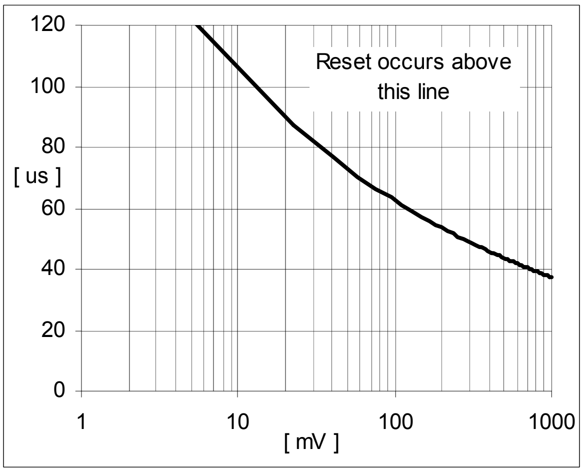


Fig. 10

Maximum Transient Duration t_{SEN} vs. Overdrive V_{TH}-V_D

Typical Operating Characteristics

(Typical values are at TA = +25°C unless otherwise noted. WDI, $\overline{\text{RESET}}$ and RESET open)

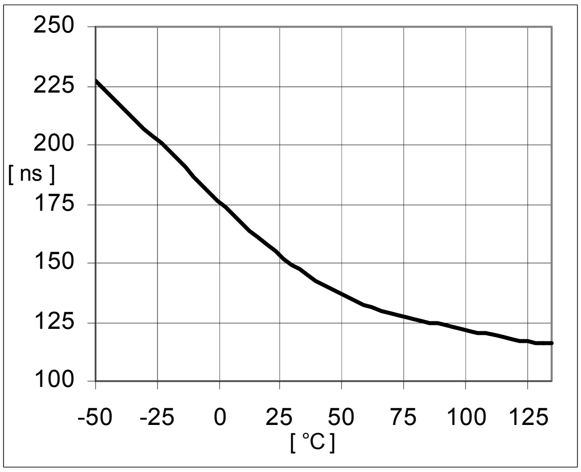


Fig. 11

Watchdog Input Pulse Width t_{WP} vs. Temperature

Functional Description

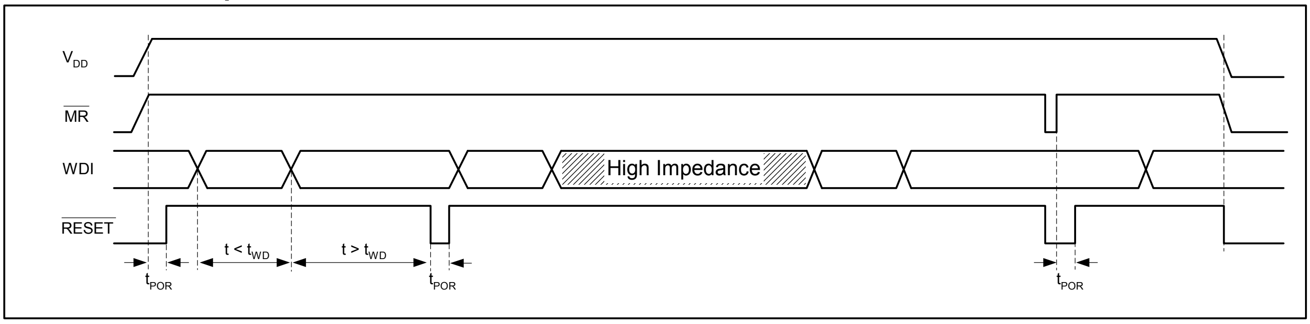


Fig. 12

V_{OUT} Monitoring

A microprocessor (µP) reset input starts the microcontroller in a known state. The EM6156 microcontroller supervisory circuits assert a reset to prevent code-execution errors during power-up, power down, and brownout conditions. $\overline{\text{RESET}}$ is guaranteed to be a logic low for VDD down to 0.9V. Once VDD exceeds the reset threshold, an internal timer keeps $\overline{\text{RESET}}$ low for the specified reset timeout period (tPOR); after this interval, $\overline{\text{RESET}}$ returns high.

If a brownout condition occurs (VDD dips below the reset threshold), $\overline{\text{RESET}}$ goes low. Each time $\overline{\text{RESET}}$ is asserted it stays low for the reset timeout period. Any time VDD goes below the reset threshold the internal timer restarts. $\overline{\text{RESET}}$ is the inverse of RESET.

Voltage Regulator

The EM6156 has a 5 V, 150 mA, low dropout voltage regulator. The low supply current makes the EM6156 particularly suitable for automotive systems which remain continuously powered. The input voltage range is 2.3 V to 40 V for operation and the input protection includes both reverse battery (42 V below ground) and load dump (positive transients up to 45 V). There is no reverse current flow from the VOUT to the VIN when the VIN equals VSS. This feature is important for systems which need to implement (with capacitance) a minimum power supply hold-up time in the event of power failure. To achieve good load regulation a 22 µF capacitor (or greater) is needed on the VIN (see Fig. 17). Tantalum or aluminium electrolytic are adequate for the 22 µF capacitor; film types will work but are relatively expensive. Many aluminium electrolytic have electrolytes that freeze at about –30°C, so tantalums are recommended for operation below –25°C. The important parameters of the 22 µF capacitor are an effective series resistance of lower than 4Ω and a resonant frequency above 500 kHz.

A output 10 µF capacitor (or greater) and a 100 nF capacitor are required on the output to prevent oscillations due to instability. The specification of this 10 µF capacitor is as per the 22 µF capacitor on the input (see previous paragraph).

The EM6156 will remain stable and in regulation with no external load and the dropout voltage is typically constant as the input voltage fall below its minimum level (see Table 2). These features are especially important in CMOS RAM keep-alive applications.

Power Dissipation

Care must be taken not to exceed the maximum junction temperature (+125°C). The power dissipation within the EM6156 is given by the formula:

$$P_{TOTAL} = (V_{INPUT} - V_{OUTPUT}) \times I_{OUTPUT} + (V_{INPUT}) \times I_{SS}$$

The maximum continuous power dissipation at a given temperature can be calculated using the formula:

$$P_{MAX} = (150°C - T_A) / R_{th(j-a)}$$

where $R_{th(j-a)}$ is the thermal resistance from the junction to the ambient and is specified in Table 2. Note that $R_{th(j-a)}$ given in Table 2 assumes that the package is soldered to a PCB. The above formula for maximum power dissipation assumes a constant load (i.e. >100 s). The transient thermal resistance for a single pulse is much lower than the continuous value.

Watchdog Description

If the watchdog timer has not been cleared within t_{WD} (1.6s typ.), reset asserts. The internal 1.6s timer is cleared by either a reset pulse or by toggling WDI. While reset is asserted, the timer remains cleared and does not count. As soon as reset is released, the timer starts counting. If the microcontroller I/O connected to WDI is put in a high impedance condition, the circuit will detect this condition as a microcontroller in sleep mode and prevent its watchdog from timing out. To monitor a high impedance or a three state condition on WDI, the watchdog input is internally driven low during the first 15/16 of the watchdog timeout period and high for the last 1/16 of the watchdog timeout period.

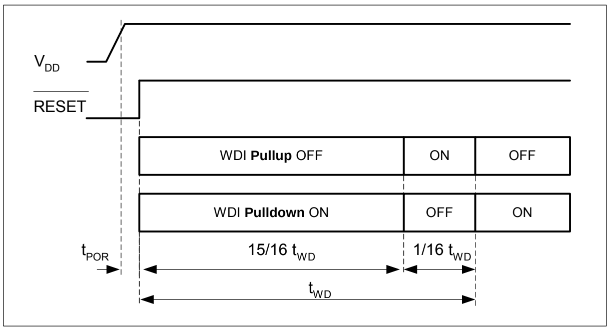


Fig. 13

WDI Input Timing Diagram

When WDI is left unconnected, this internal driver clears the 1.6s timer every 1.5s. When WDI is three-stated or unconnected, the maximum allowable leakage current is 0.5μA.

To minimized the overall system power consumption and therefore for a minimum watchdog input current leave WDI low for the majority of the watchdog timeout period, pulsing it low-high-low once within the first 15/16 of the watchdog timeout period to reset the watchdog timer. If WDI is externally driven high for the majority of the timeout period, up to 35μA can flow into WDI. Meanwhile when the microcontroller is not in sleep mode, the output of the microcontroller which drives WDI has to be strong enough to fight the 35μA.

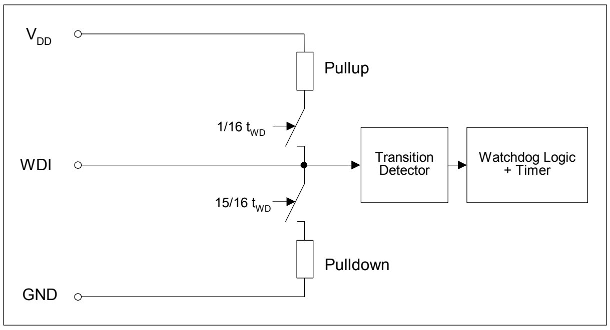


Fig. 14

WDI Input Stage Block Schematic

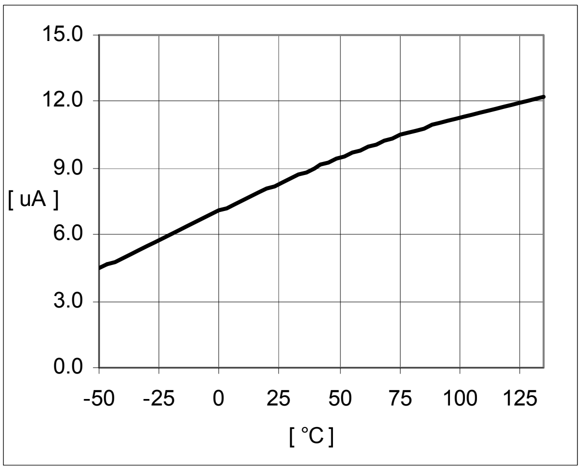


Fig. 15

WDI Input Current Low-level I_{IL} vs. Temperature (V_{DD}=5.5V)

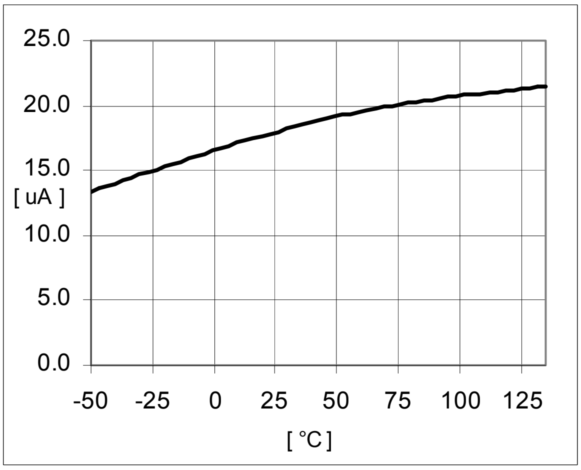


Fig. 16

WDI Input Current High-Level I_{IH} vs. Temperature (V_{DD}=5.5V)

Typical Application

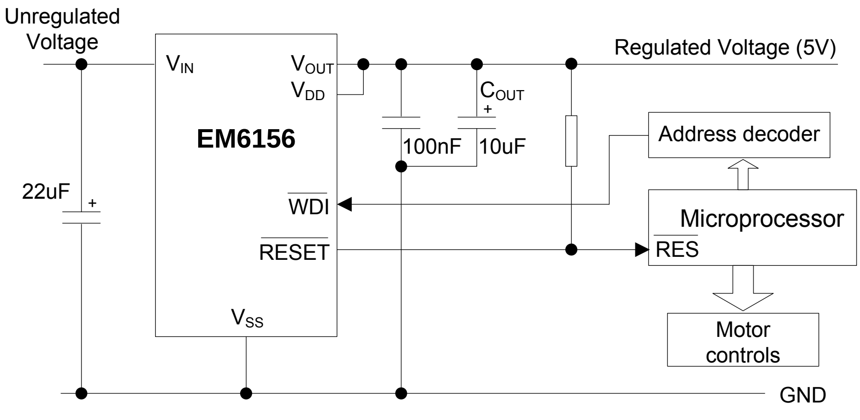
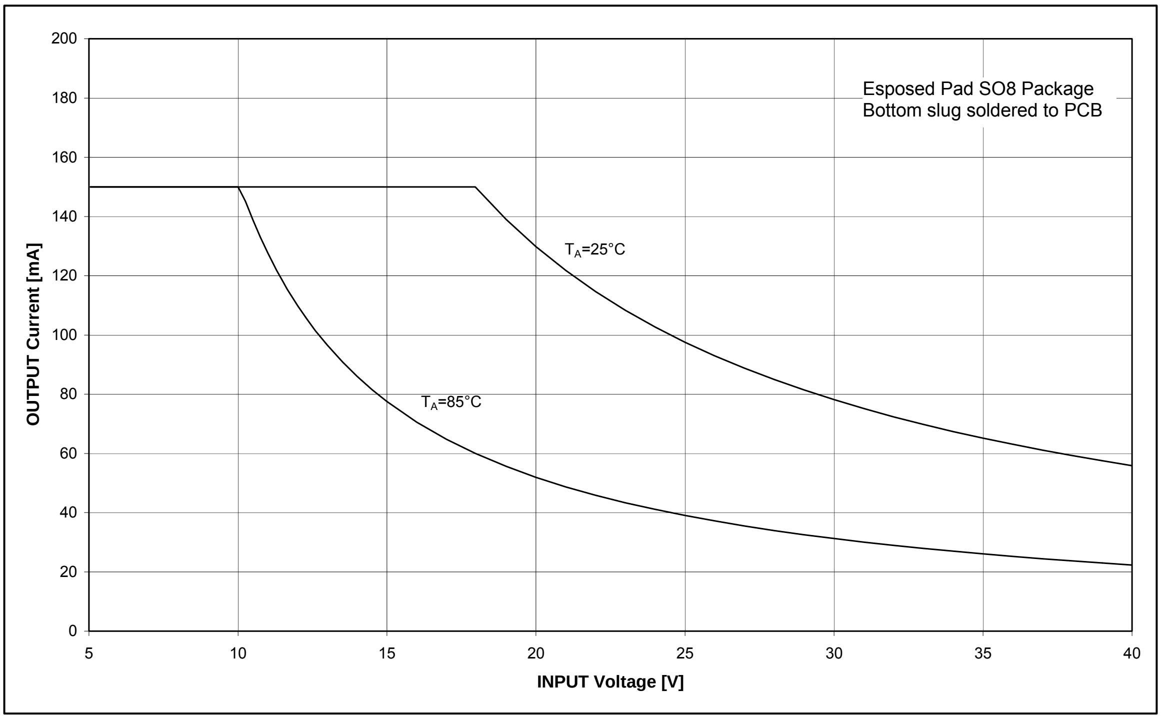


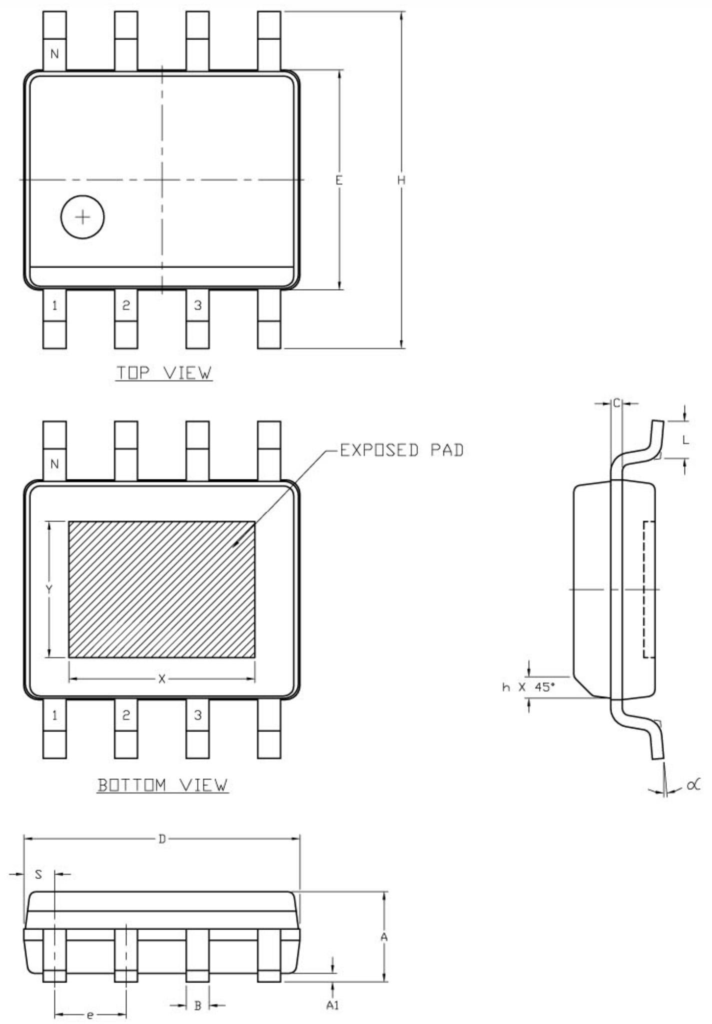
Fig. 17

The important parameters of the 10µF capacitor are an effective series resistance lower than 4Ω and a resonant frequency above 500 kHz.

Typical maximum output current versus V_{IN} (to be confirmed after qualification)



Package Information



NOTES:

1. DIMENSION "D" DOES NOT NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006"(0.15mm) PER SIDE.
2. DIMENSION "E" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSION SHALL NOT EXCEED .010"(0.25mm) PER SIDE.
3. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
4. "N" IS THE NUMBER OF TERMINAL POSITIONS.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. THE LEAD WIDTH "B", AS MEASURED .014"(0.36mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024"(0.61mm).
7. DIMENSIONS X & Y DEFINES EXPOSED METAL AREA (DEPENDENT ON PADDLE DIMENSIONS)
8. REFERENCE DRAWING JEDEC MS012, VARIATION AA.

SYMBOL	DIMENSION IN INCH		DIMENSION IN MM	
	MIN.	MAX.	MIN.	MAX.
A	.053	.069	1.35	1.75
A1	.000	.005	0.00	0.13
B	.013	.020	0.33	0.51
C	.008	.010	0.19	0.25
D	.189	.1968	4.80	5.00
E	.150	.157	3.80	4.00
e	.050 BSC		1.27 BSC	
H	.228	.244	5.80	6.20
h	.010	.020	0.25	0.50
L	.016	.050	0.40	1.27
S	.0155	.0255	0.394	0.648
X	SEE NOTES 7		SEE NOTES 7	
Y	SEE NOTES 7		SEE NOTES 7	
α	0°	8°	0°	8°