ZL2106

Data Sheet February 19, 2009 FN6852.0

6A Digital-DC Synchronous Step-Down DC-DC Converter

Description

The ZL2106 is an innovative power conversion and management IC that combines an integrated synchronous step-down DC-DC converter with key power management functions in a small package, resulting in a flexible and integrated solution. Zilker Labs Digital-DC™ technology enables unparalleled power management integration while delivering industry-leading performance in a tiny footprint.

The ZL2106 can provide an output voltage from 0.54 V to 5.5 V (with margin) from an input voltage between 4.5 V and 14 V. Internal low $R_{DS(ON)}$ synchronous power MOSFETs enable the ZL2106 to deliver continuous loads up to 6 A with high efficiency. An internal Schottky bootstrap diode reduces discrete component count. The ZL2106 also supports phase spreading to reduce system input capacitance.

Power management features such as digital soft-start delay and ramp, sequencing, tracking, and margining can be configured by simple pin-strapping or through an on-chip serial port. The ZL2106 uses the PMBus™ protocol for communication with a host controller and the Digital-DC bus for interoperability between other Zilker Labs devices.

Features

Power Conversion

- Efficient synchronous buck controller
- Integrated MOSFET switches
- 6 A continuous output current
- 4.5 V to 14 V input range
- 0.54 V to 5.5 V output range (with margin)
- ±1% output voltage accuracy
- 200 kHz to 1 MHz switching frequency
- Phase spreading and Fault spreading
- *Snapshot*™ parametric capture
- Small footprint QFN package (6 x 6 mm)

Power Management

- Digital soft start/stop
- Precision delay and ramp-up
- Power good/enable
- Voltage tracking, sequencing, and margining
- Voltage / current / temperature monitoring
- Output voltage and current protection
- I^2C/SMBus interface, PMBus compatible
- Internal non-volatile memory (NVM)

Applications

- Telecom, Networking, Storage equipment
- High-density servers
- Test & Measurement equipment
- Industrial control equipment
- 5V & 12V distributed power systems

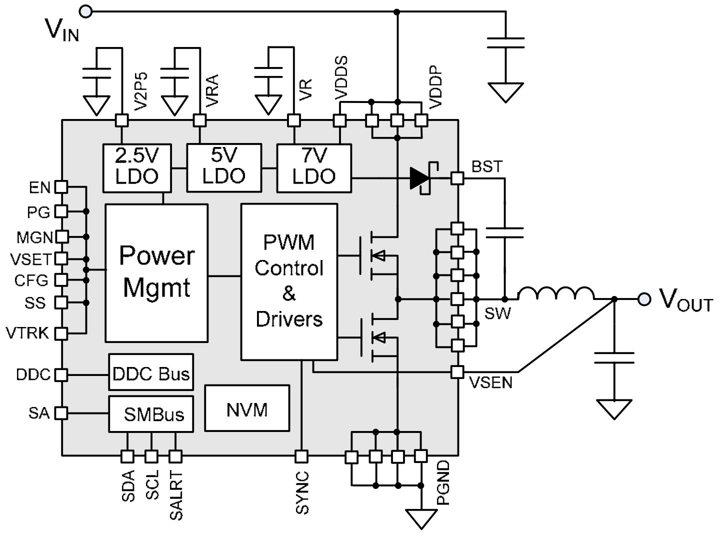

Figure 1. Block Diagram

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1. Electrical Characteristics

Table 1. Absolute Maximum Ratings

Voltage measured with respect to SGND. Operating beyond these limits may cause permanent damage to the device. Functional operation beyond the Recommended Operating Conditions is not implied.

Parameter	Pin	Comments	Value	Unit
DC Supply Voltage	VDDP, VDDS		-0.3 to 17	V
High Side Supply Voltage	BST		-0.3 to 30	V
High Side Boost Voltage	BST - SW		-0.3 to 8	V
Internal MOSFET Reference	VR		-0.3 to 8.5	V
Internal Analog Reference	VRA		-0.3 to 6.5	V
Internal 2.5 V Reference	V2P5		-0.3 to 3	V
Logic I/O Voltage	EN, CFG, DDC, FC, MGN, PG, SDA, SCL, SA, SALRT, SS, SYNC, VTRK, VSET, VSEN		-0.3 to 6.5	V
Ground Differential	DGND - SGND PGND - SGND		±0.3	V
MOSFET Drive Reference Current	VR	Internal bias usage	20	mA
Analog Reference Current	VRA	Internal bias usage	100	mA
2.5 V Reference Current	V2P5	Internal bias usage	60	mA
Switch node current	SW	Peak (sink or source)	10	A
Junction Temperature	–		-55 to 150	°C
Storage Temperature	–		-55 to 150	°C
Lead Temperature	All	Soldering, 10 s	300	°C

Table 2. Recommended Operating Conditions and Thermal Information

Parameter	Symbol	Min	Typ	Max	Unit
Input Supply Voltage Range, VDDP, VDDS (See Figure 13)	VDDS tied to VR, VRA	4.5	–	5.5	V
	VDDS tied to VR, VRA floating	5.5	–	7.5	V
	VR, VRA floating	7.5	–	14	V
Output Voltage Range[1]	V_{OUT}	0.54	–	5.5	V
Operating Junction Temperature Range	T_J	-40	–	125	°C
Junction to Ambient Thermal Impedance[2]	θ_{JA}	–	35	–	°C/W
Junction to Case Thermal Impedance[3]	θ_{JC}	–	5	–	°C/W

Notes:

1. Includes margin limits.
2. θ_{JA} is measured in free air with the device mounted on a multi-layer FR4 test board and the exposed metal pad soldered to a low impedance ground plane using multiple vias.
3. For θ_{JC}, the “case” temperature is measured at the center of the exposed metal pad.

Table 3. Electrical Specifications

$V_{DDP} = V_{DDS} = 12$ V, $T_A = -40$ °C to 85 °C unless otherwise noted.[1] Typical values are at $T_A = 25$ °C.

Parameter	Conditions	Min	Typ	Max	Unit
Input and Supply Characteristics					
I_{DD} supply current	f_{SW} = 200 kHz, no load	–	11	20	mA
	f_{SW} = 1 MHz, no load	–	15	30	mA
I_{DDS} shutdown current	EN = 0 V, No I^2C/SMBus activity	–	0.6	1	mA
VR reference output voltage	$V_{DD} > 8$ V, $I_{VR} < 10$ mA	6.5	7.0	7.5	V
VRA reference output voltage	$V_{DD} > 5.5$ V, $I_{VRA} < 50$ mA	4.5	5.1	5.5	V
V2P5 reference output voltage	$I_{V2P5} < 50$ mA	2.25	2.5	2.75	V
Output Characteristics					
Output current	I_{RMS}, Continuous	–	–	6	A
Output voltage adjustment range [2]	$V_{IN} > V_{OUT}$	0.6	–	5.0	V
Output voltage setpoint resolution	Set using resistors	–	10	–	mV
	Set using I^2C/SMBus	–	±0.025	–	% FS [3]
VSEN output voltage accuracy	Includes line, load, temp	-1	–	1	%
VSEN input bias current	VSEN = 5.5 V	–	110	200	µA
Soft start delay duration range [4]	Set using SS pin or resistor	2	–	20	ms
	Set using I^2C/SMBus	0.002	–	500	s
Soft start delay duration accuracy	Turn-on delay (precise mode) [4,5]	–	±0.25	–	ms
	Turn-on delay (normal mode) [6]	–	-0.25/+4	–	ms
	Turn-off delay [6]	–	-0.25/+4	–	ms
Soft start ramp duration range	Set using SS pin or resistor	2	–	20	ms
	Set using I^2C/SMBus	0	–	200	ms
Soft start ramp duration accuracy		–	100	–	µs
Logic Input/Output Characteristics					
Logic input bias current	EN,PG,SCL,SDA,SALRT pins	-10	–	10	µA
MGN input bias current		- 1	–	1	mA
Logic input low, V_{IL}		–	–	0.8	V
Logic input OPEN (N/C)	Multi-mode logic pins	–	1.4	–	V
Logic input high, V_{IH}		2.0	–	–	V
Logic output low, V_{OL}	$I_{OL} \leq 4$ mA	–	–	0.4	V
Logic output high, V_{OH}	$I_{OH} \geq -2$ mA	2.25	–	–	V
Oscillator and Switching Characteristics					
Switch node current, I_{SW}	Peak (source or sink) [7]			9	A
Switching frequency range		200	–	1000	kHz
Switching frequency set-point accuracy	Predefined settings (Table 13)	-5	–	5	%
PWM duty cycle (max)	Factory default [8]	–	–	95 [9]	%
SYNC pulse width (min)		150	–	–	ns
Input clock frequency drift tolerance	External clock source	-13	–	13	%
$R_{DS(ON)}$ of High Side N-channel FETs	$I_{SW} = 6$ A, $V_{GS} = 6.5$ V	–	60	85	mΩ
$R_{DS(ON)}$ of Low Side N-channel FETs	$I_{SW} = 6$ A, $V_{GS} = 12$ V	–	43	65	mΩ

Notes:

1. Refer to Safe Operating Area in Figure 5 and thermal design guidelines in AN10.
2. Does not include margin limits.

Table 3. Electrical Characteristics (continued)

$V_{DDP} = V_{DDS} = 12$ V, $T_A = -40$ °C to 85 °C unless otherwise noted.[1] Typical values are at $T_A = 25$ °C.

Parameter	Conditions	Min	Typ	Max	Unit
Tracking					
VTRK input bias current	VTRK = 5.5 V	–	110	200	µA
VTRK tracking ramp accuracy	100% Tracking, V_{OUT} - VTRK	-100	–	100	mV
VTRK regulation accuracy	100% Tracking, V_{OUT} - VTRK	-1	–	1	%
Fault Protection Characteristics					
UVLO threshold range	Configurable via I^2C/SMBus	2.85	–	16	V
UVLO set-point accuracy		-150	–	150	mV
UVLO hysteresis	Factory default	–	3	–	%
	Configurable via I^2C/SMBus	0	–	100	%
UVLO delay		–	–	2.5	µs
Power good V_{OUT} low threshold	Factory default	–	90	–	% V_{OUT}
Power good V_{OUT} high threshold	Factory default	–	115	–	% V_{OUT}
Power good V_{OUT} hysteresis	Factory default	–	5	–	%
Power good delay	Using pin-strap or resistor	2	–	20	ms
	Configurable via I^2C/SMBus	0	–	500	s
VSEN undervoltage threshold	Factory default	–	85	–	% V_{OUT}
	Configurable via I^2C/SMBus	0	–	110	% V_{OUT}
VSEN overvoltage threshold	Factory default	–	115	–	% V_{OUT}
	Configurable via I^2C/SMBus	0	–	115	% V_{OUT}
VSEN undervoltage hysteresis		–	5	–	% V_{OUT}
VSEN undervoltage/ overvoltage fault response time	Factory default	–	16	–	µs
	Configurable via I^2C/SMBus	5	–	60	µs
Peak current limit threshold	Factory default	–	–	9.0	A
	Configurable via I^2C/SMBus	0.2	–	9.0	A
Current limit set-point accuracy		–	±10	–	% FS [3]
Current limit protection delay	Factory default	–	5	–	t_{SW} [10]
	Configurable via I^2C/SMBus	1	–	32	t_{SW} [10]
Thermal protection threshold (junction temperature)	Factory default	–	125	–	°C
	Configurable via I^2C/SMBus	-40	–	125	°C
Thermal protection hysteresis		–	15	–	°C

Notes:

3. Percentage of Full Scale (FS) with temperature compensation applied.
4. The device requires a delay period following an enable signal and prior to ramping its output. Precise timing mode limits this delay period to approx 2 ms, where in normal mode it may vary up to 4 ms.
5. Precise ramp timing mode is only valid when using EN pin to enable the device rather than PMBus enable. Precise ramp timing mode is automatically disabled for a self-enabled device (EN pin tied high).
6. The devices may require up to a 4 ms delay following the assertion of the enable signal (normal mode) or following the de-assertion of the enable signal. Precise mode requires Re-Enable delay = $T_{OFF}+T_{FALL}+10$ µs.
7. Switch node current should not exceed I_{RMS} of 6 A.
8. Factory default is the initial value in firmware. The value can be changed via PMBus commands.
9. Maximum duty cycle is limited by the equation MAX_DUTY(%) = $[1 - (150\times10^{-9} \times f_{SW})] \times 100$ and not to exceed 95%.
10. $t_{SW} = 1/f_{SW}$, where f_{SW} is the switching frequency.

2. Typical Performance Curves

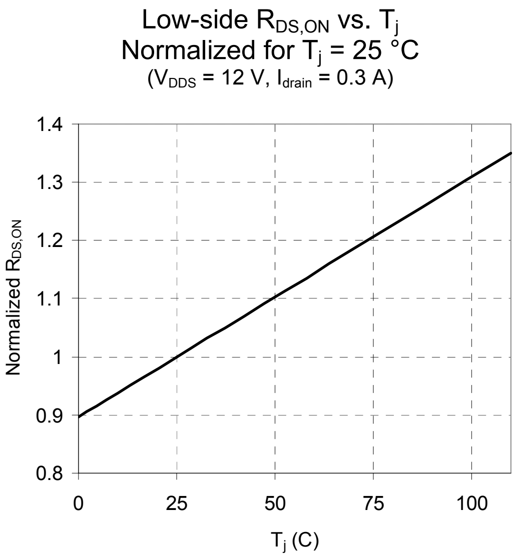

Low-side $R_{DS,ON}$ vs. T_j
Normalized for T_j = 25 °C
(V_{DDS} = 12 V, I_{drain} = 0.3 A)

Figure 2

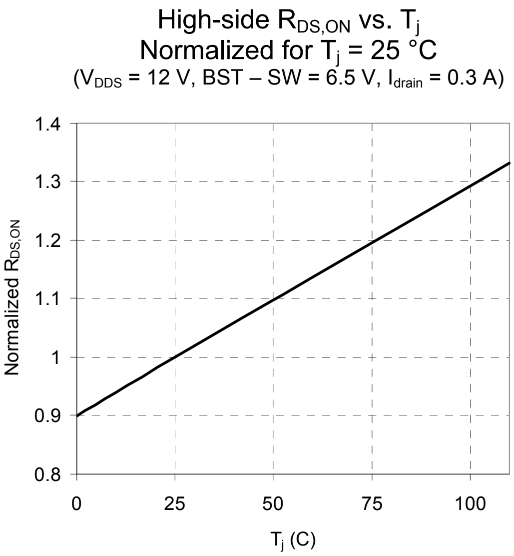

High-side $R_{DS,ON}$ vs. T_j
Normalized for T_j = 25 °C
(V_{DDS} = 12 V, BST – SW = 6.5 V, I_{drain} = 0.3 A)

Figure 3

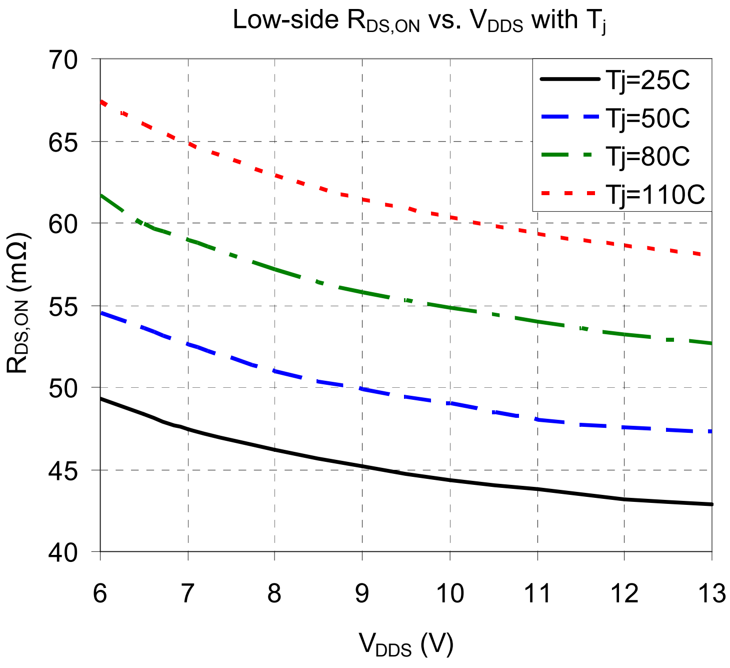

Low-side $R_{DS,ON}$ vs. V_{DDS} with T_j

Figure 4

For some applications, ZL2106 operating conditions (input voltage, output voltage, switching frequency, temperature) may require de-rating to remain within the Safe Operating Area (SOA).
Note: $V_{IN} = V_{DDP} = V_{DDS}$, $T_j \leq 125$ ºC

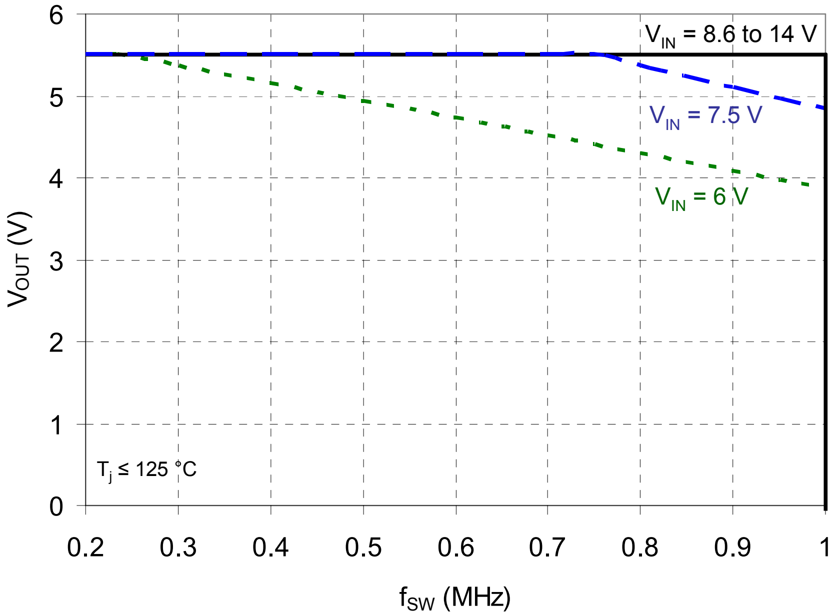


Figure 5. Safe Operating Area

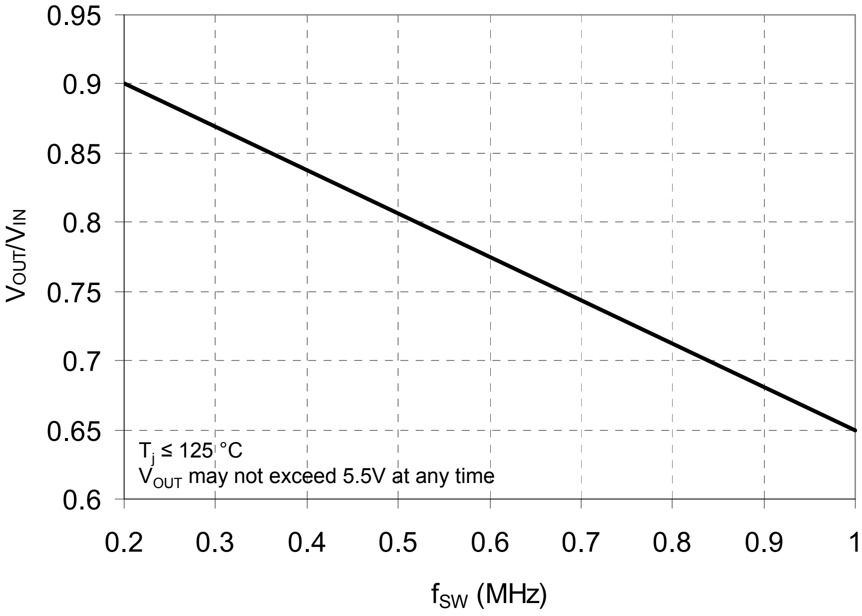


Figure 6. Maximum Conversion Ratio

3. Pin Descriptions

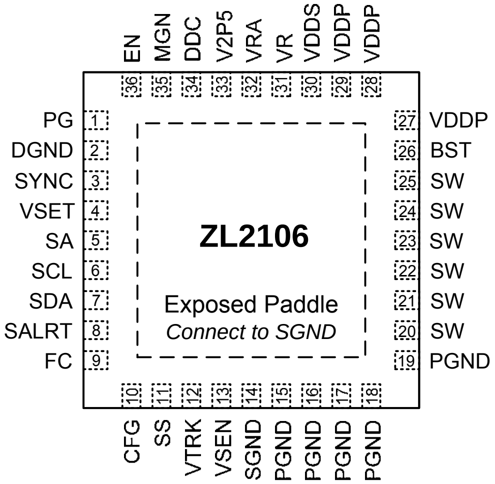


Figure 7. ZL2106 Pin Configurations (top view)

Table 4. Pin Descriptions

Pin	Label	Type[1]	Description
1	PG	O	Power good. This pin transitions high 100 ms after output voltage stabilizes within regulation band. Selectable open drain or push-pull output. Factory default is open drain.
2	DGND	PWR	Digital ground. Common return for digital signals. Connect to low impedance ground plane.
3	SYNC	I/O, M[2]	Clock synchronization pin. Used to set switching frequency of internal clock or for synchronization to external frequency reference.
4	VSET	I, M	Output voltage select pin. Used to set V_{OUT} set-point and V_{OUT} max.
5	SA	I, M	Serial address select pin. Used to assign unique SMBus address to each IC.
6	SCL	I/O	Serial clock. Connect to external host interface.
7	SDA	I/O	Serial data. Connect to external host interface.
8	SALRT	O	Serial alert. Connect to external host interface if desired.
9	FC	I, M	Loop compensation select pin. Used to set loop compensation.
10	CFG	I, M	Configuration pin. Used to control the SYNC pin, sequencing and enable tracking.
11	SS	I, M	Soft Start pin. Used to set the ramp delay and ramp time, sets UVLO and configure tracking.
12	VTRK	I	Track sense pin. Used to track an external voltage source.
13	VSEN	I	Output voltage positive feedback sensing pin.
14	SGND	PWR	Common return for analog signals. Connect to low impedance ground plane.
15-19	PGND	PWR	Power ground. Common return for internal switching MOSFETs. Connect to low impedance ground plane.
20-25	SW	I/O	Switching node (level-shift common).
26	BST	PWR	Bootstrap voltage for level-shift driver (referenced to SW).

Notes:

1. I = Input, O = Output, PWR = Power or Ground, M = Multi-mode pins.
2. The SYNC pin can be used as a logic pin, a clock input or a clock output.

Table 4. Pin Descriptions (continued)

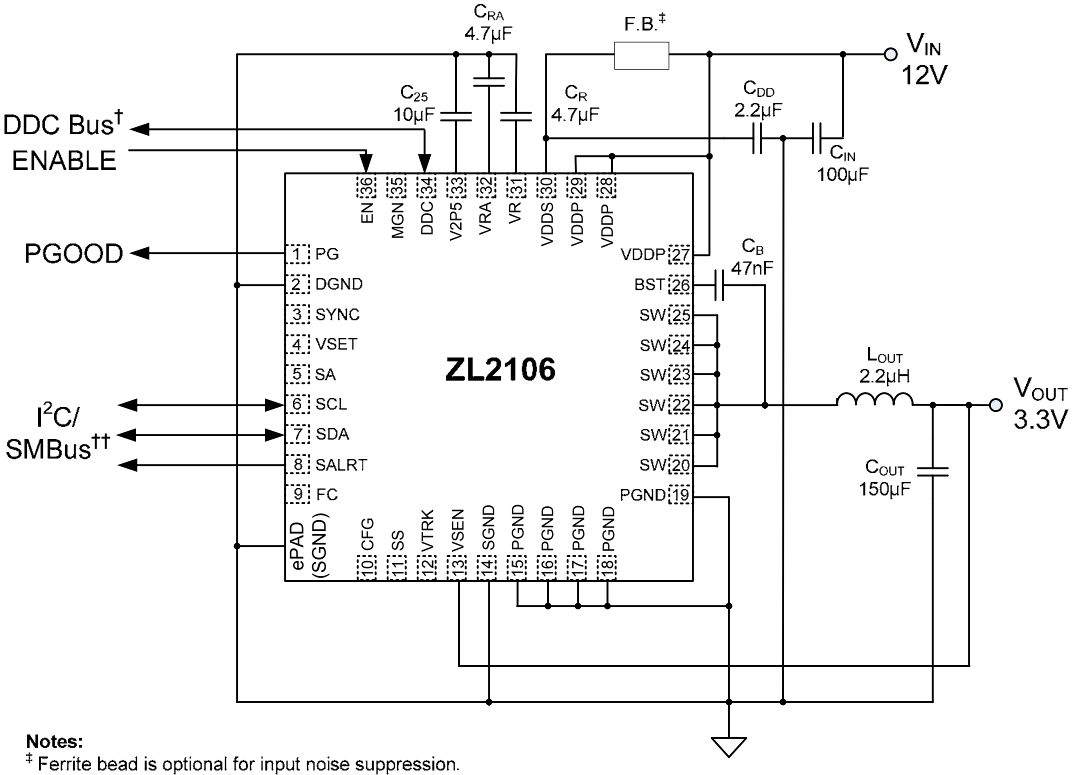
Pin	Label	Type[1]	Description
27-29	VDDP	PWR	Bias supply voltage for internal switching MOSFETs (return is PGND).
30	VDDS	PWR	IC supply voltage (return is SGND).
31	VR	PWR	Regulated bias from internal 7 V low-dropout regulator (return is PGND). Decouple with a 4.7 µF capacitor to PGND.
32	VRA	PWR	Regulated bias from internal 5 V low-dropout regulator for internal analog circuitry (return is SGND). Decouple with a 4.7 µF capacitor to SGND.
33	V2P5	PWR	Regulated bias from internal 2.5 V low-dropout regulator for internal digital circuitry (return is DGND). Decouple with a 10µF capacitor.
34	DDC	I/O	Digital-DC Bus (open drain). Interoperability between Zilker Labs devices.
35	MGN	I	Margin pin. Used to enable margining of the output voltage.
36	EN	I	Enable pin. Used to enable the device (active high).
ePad	SGND	PWR	Exposed thermal pad. Common return for analog signals. Connect to low impedance ground plane.

Notes:

1. I = Input, O = Output, PWR = Power or Ground, M = Multi-mode pins. Please refer to Section 5.4 “Multi-mode Pins,” on page 13.

4. Typical Application Circuit

The following application circuit represents a typical implementation of the ZL2106. For PMBus operation, it is recommended to tie the enable pin (EN) to SGND.



Notes:

[‡] Ferrite bead is optional for input noise suppression.

[†] The DDC bus pull-up resistance will vary based on the capacitive loading of the bus, including the number of devices connected. The 10 kΩ default value, assuming a maximum of 100 pF per device, provides the necessary 1 µs pull-up rise time. Please refer to the Digital-DC Bus section for more details.

[††] The I^{2}C/SMBus pull-up resistance will vary based on the capacitive loading of the bus, including the number of devices connected. Please refer to the I^{2}C/SMBus specifications for more details.

Figure 8. 12 V to 3.3 V / 6 A Application Circuit
(5 ms SS delay, 5 ms SS ramp)

5. ZL2106 Overview

5.1 Digital-DC Architecture

The ZL2106 is an innovative mixed-signal power conversion and power management IC based on Zilker Labs patented Digital-DC technology that provides an integrated, high performance step-down converter for point of load applications. The ZL2106 integrates all necessary PWM control circuitry as well as low $R_{DS(ON)}$ synchronous power MOSFETs to provide an extremely small solution for supplying load currents up to 6 A.

Its unique PWM loop utilizes an ideal mix of analog and digital blocks to enable precise control of the entire power conversion process with no software required, resulting in a very flexible device that is also very easy to use. An extensive set of power management functions are fully integrated and can be configured using simple pin connections. The user configuration can be saved in an internal non-volatile memory (NVM). Additionally, all functions can be configured and monitored via the SMBus hardware interface using standard PMBus commands, allowing ultimate flexibility.

Once enabled, the ZL2106 is immediately ready to regulate power and perform power management tasks with no programming required. Advanced configuration options and real-time configuration changes are available via the I^2C/SMBus interface if desired and continuous monitoring of multiple operating parameters is possible with minimal interaction from a host controller. Integrated sub-regulation circuitry enables single supply operation from any external supply between 4.5 V and 14 V with no secondary bias supplies needed. The ZL2106 can also be configured to operate from a 3.3 V or 5 V standby supply when the main power rail is not present, allowing the user to configure and/or read diagnostic information from the device when the main power has been interrupted or is disabled.

The ZL2106 can be configured by simply connecting its pins according to the tables provided in the following sections. Additionally, a comprehensive set of application notes are available to help simplify the design process. An evaluation board is also available to help the user become familiar with the device. This board can be evaluated as a standalone platform using pin configuration settings. A Windows™-based GUI is also provided to enable full configuration and monitoring capability via the I^2C/SMBus interface using an available computer and the included USB cable.

Application notes and reference designs are available to assist the user in designing to specific application demands. Please register for My ZL on www.zilkerlabs.com to access the most up-to-date documentation or call your local Zilker Labs sales representative to order an evaluation kit.

5.2 Power Conversion Overview

The ZL2106 operates as a voltage-mode, synchronous buck converter with a selectable constant frequency pulse width modulator (PWM) control scheme. The ZL2106 integrates dual low $R_{DS(ON)}$ synchronous MOSFETs to minimize the circuit footprint.

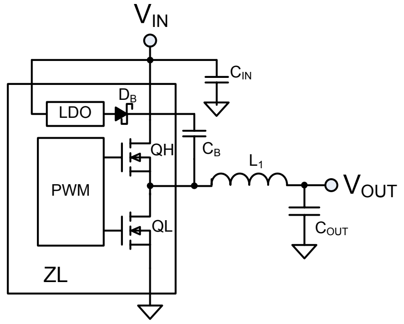


Figure 9. Synchronous Buck Converter

Figure 9 illustrates the basic synchronous buck converter topology showing the primary power train components. This converter is also called a step-down converter, as the output voltage must always be lower than the input voltage.

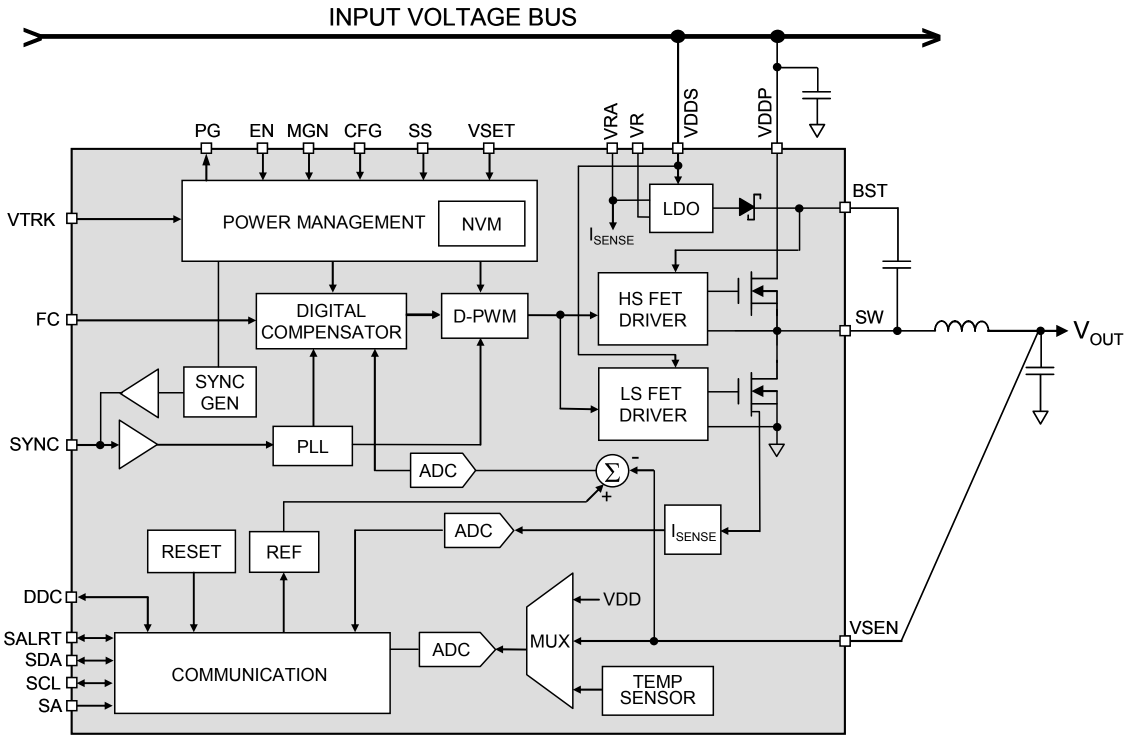


Figure 10. ZL2106 Block Diagram

The ZL2106 integrates two N-channel power MOSFETs; QH is the top control MOSFET and QL is the bottom synchronous MOSFET. The amount of time that QH is on as a fraction of the total switching period is known as the duty cycle *D*, which is described by the following equation:

$$D \approx \frac{V_{OUT}}{V_{IN}}$$

During time D, QH is on and $V_{IN} - V_{OUT}$ is applied across the inductor. The output current ramps up as shown in Figure 11.

When QH turns off (time 1-D), the current flowing in the inductor must continue to flow from the ground up through QL, during which the current ramps down. Since the output capacitor C_{OUT} exhibits low impedance at the switching frequency, the AC component of the inductor current is filtered from the output voltage so the load sees nearly a DC voltage.

The maximum conversion ratio is shown in Figure 6. Typically, buck converters specify a maximum duty cycle that effectively limits the maximum output voltage that can be realized for a given input voltage and switching frequency. This duty cycle limit ensures that the low-side MOSFET is allowed to turn on for a minimum amount of time during each switching cycle, which enables the bootstrap capacitor to be charged up and provide adequate gate drive voltage for the high-side MOSFET.

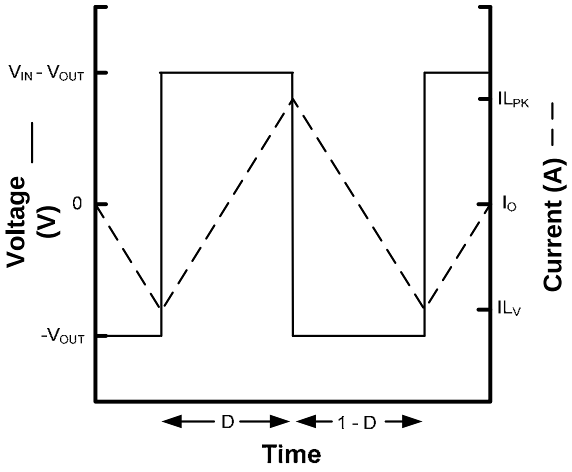


Figure 11. Inductor Waveform

In general, the size of components L_1 and C_{OUT} as well as the overall efficiency of the circuit are inversely proportional to the switching frequency, f_{SW}. Therefore, the highest efficiency circuit may be realized by switching the MOSFETs at the lowest possible frequency; however, this will result in the largest component size. Conversely, the smallest possible footprint may be realized by switching at the fastest possible frequency but this gives a somewhat lower efficiency. Each user should determine the optimal combination of size and efficiency when determining the switching frequency for each application.

The block diagram for the ZL2106 is illustrated in Figure 10. In this circuit, the target output voltage is regulated by connecting the VSEN pin directly to the output regulation point. The VSEN signal is then compared to an internal reference voltage that had been set to the desired output voltage level by the user. The error signal derived from this comparison is converted to a digital value with an analog to digital (A/D) converter. The digital signal is also applied to an adjustable digital compensation filter and the compensated signal is used to derive the appropriate PWM duty cycle for driving the internal MOSFETs in a way that produces the desired output.

5.3 Power Management Overview

The ZL2106 incorporates a wide range of configurable power management features that are simple to implement without additional components. Also, the ZL2106 includes circuit protection features that continuously safeguard the device and load from damage due to unexpected system faults. The ZL2106 can continuously monitor input voltage, output voltage/current and internal temperature. A Power Good output signal is also included to enable power-on reset functionality for an external processor.

All power management functions can be configured using either pin configuration techniques (see Figure 12) or via the I^2C/SMBus interface. Monitoring parameters can also be pre-configured to provide alerts for specific conditions. See Application Note AN33 for more details on SMBus monitoring.

5.4 Multi-mode Pins

In order to simplify circuit design, the ZL2106 incorporates patented multi-mode pins that allow the user to easily configure many aspects of the device without programming. Most power management features can be configured using these pins. The multi-mode pins can respond to four different connections as shown in Table 5. These pins are sampled when power is applied or by issuing a PMBus Restore command (See Application Note AN33).

Pin-strap Settings: This is the simplest method, as no additional components are required. Using this method, each pin can take on one of three possible states: LOW, OPEN, or HIGH. These pins can be connected to the V2P5 pin for logic HIGH settings as this pin provides a regulated voltage higher than 2 V. Using a single pin one of three settings can be selected.

Table 5. Multi-mode Pin Configuration

Pin Tied To	Value
LOW (Logic LOW)	< 0.8 VDC
OPEN (N/C)	No connection
HIGH (Logic HIGH)	> 2.0 VDC
Resistor to SGND	Set by resistor value

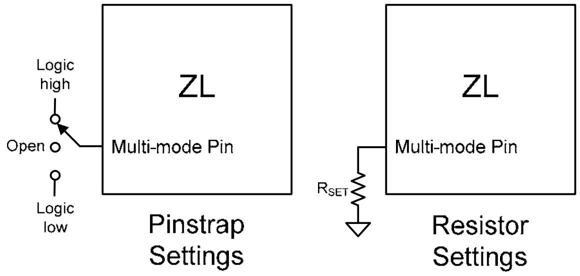


Figure 12. Pin-strap and Resistor Setting Examples

Resistor Settings: This method allows a greater range of adjustability when connecting a finite value resistor (in a specified range) between the multi-mode pin and SGND.

Standard 1% resistor values are used, and only every fourth E96 resistor value is used so the device can reliably recognize the value of resistance connected to the pin while eliminating the error associated with the resistor accuracy. Up to 31 unique selections are available using a single resistor.

I^2C/SMBus Method: ZL2106 functions can be configured via the I^2C/SMBus interface using standard PMBus commands. Additionally, any value that has been configured using the pin-strap or resistor setting methods can also be re-configured and/or verified via the I^2C/SMBus. See Application Note AN33 for more details.

The SMBus device address and VOUT_MAX are the only parameters that must be set by external pins. All other device parameters can be set via the I^2C/SMBus. The device address is set using the SA pin. VOUT_MAX is determined as 10% greater than the voltage set by the VSET pin.

Resistor pin-straps are recommended to be used for all available device parameters to allow a safe initial power-up before configuration is stored via the I^2C/SMBus. For example, this can be accomplished by pin-strapping the undervoltage lockout threshold (using SS pin) to a value greater than the expected input voltage, thus preventing the device from enabling prior to loading a configuration file.

6. Power Conversion Functional Description

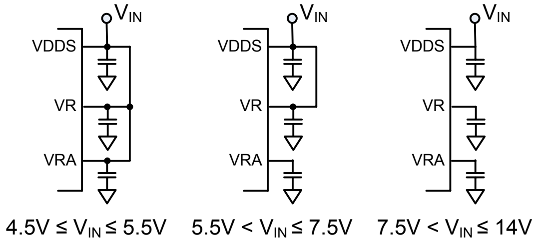
6.1 Internal Bias Regulators and Input Supply Connections

The ZL2106 employs three internal low dropout (LDO) regulators to supply bias voltages for internal circuitry, allowing it to operate from a single input supply. The internal bias regulators are as follows:

VR: The VR LDO provides a regulated 7 V bias supply for the high-side MOSFET driver circuit. It is powered from the VDDS pin and supplies bias current internally. A 4.7 µF filter capacitor is required at the VR pin. The VDDS pin directly supplies the low-side MOSFET driver circuit.

VRA: The VRA LDO provides a regulated 5 V bias supply for the current sense circuit and other analog circuitry. It is powered from the VDDS pin and supplies bias current internally. A 4.7 µF filter capacitor is required at the VRA pin.

V2P5: The V2P5 LDO provides a regulated 2.5 V bias supply for the main controller circuitry. It is powered from the VRA LDO and supplies bias current internally. A 10 µF filter capacitor is required at the V2P5 pin.



$4.5V \le V_{IN} \le 5.5V$ $5.5V < V_{IN} \le 7.5V$ $7.5V < V_{IN} \le 14V$

Figure 13. Input Supply Connections

When the input supply (VDDS) is higher than 7.5 V, the VR and VRA pins should not be connected to any other pins. These pins should only have a filter capacitor attached. Due to the dropout voltage associated with the VR and VRA bias regulators, the VDDS pin must be connected to these pins for designs operating from a supply below 7.5 V. Figure 13 illustrates the required connections for all cases.

Note: The internal bias regulators, VR and VRA, are not designed to be outputs for powering other circuitry. Do not attach external loads to any of these pins. Only the multi-mode pins may be connected to the V2P5 pin for logic HIGH settings.

6.2 High-side Driver Boost Circuit

The gate drive voltage for the high-side MOSFET driver is generated by a floating bootstrap capacitor, C_B (see Figure 9). When the lower MOSFET (QL) is turned on, the SW node is pulled to ground and the capacitor is charged from the internal VR bias regulator through diode D_B. When QL turns off and the upper MOSFET (QH) turns on, the SW node is pulled up to VDDP and the voltage on the bootstrap capacitor is boosted approximately 6.5 V above VDDP to provide the necessary voltage to power the high-side driver. An internal Schottky diode is used with C_B to help maximize the high-side drive supply voltage.

6.3 Output Voltage Selection

The output voltage may be set to any voltage between 0.6 V and 5.0 V provided that the input voltage is higher than the desired output voltage by an amount sufficient to prevent the device from exceeding its maximum duty cycle specification. Using the pin-strap method, V_{OUT} can be set to one of three standard voltages as shown in Table 6.

Table 6. Pin-strap Output Voltage Settings

VSET	V_{OUT}
LOW	1.2 V
OPEN	1.5 V
HIGH	3.3 V

Table 7. ZL2106 Start-up Sequence

Step #	Step Name	Description	Time Duration
1	Power Applied	Input voltage is applied to the ZL2106's VDD pins (VDDP and VDDS).	Depends on input supply ramp time
2	Internal Memory Check	The device will check for values stored in its internal memory. This step is also performed after a Restore command.	Approx 5-10 ms (device will ignore an enable signal or PMBus traffic during this period)
3	Multi-mode Pin Check	The device loads values configured by the multi-mode pins.	
4	Device Ready	The device is ready to accept an enable signal.	—
5	Pre-ramp Delay	The device requires approximately 2 ms following an enable signal and prior to ramping its output. Additional pre-ramp delay may be configured using the SS pin.	Approximately 2 ms

The resistor setting method can be used to set the output voltage to levels not available in Table 6. To set V_{OUT} using resistors, use Table 8 to select the resistor that corresponds to the desired voltage.

Table 8. Resistors for Setting Output Voltage

R_{SET}	V_{OUT}	R_{SET}	V_{OUT}
10 kΩ	0.6 V	46.4 kΩ	2.0 V
11 kΩ	0.7 V	51.1 kΩ	2.1 V
12.1 kΩ	0.75 V	56.2 kΩ	2.2 V
13.3 kΩ	0.8 V	61.9 kΩ	2.3 V
14.7 kΩ	0.9 V	68.1 kΩ	2.4 V
16.2 kΩ	1.0 V	75 kΩ	2.5 V
17.8 kΩ	1.1 V	82.5 kΩ	2.6 V
19.6 kΩ	1.2 V	90.9 kΩ	2.7 V
21.5 kΩ	1.25 V	100 kΩ	2.8 V
23.7 kΩ	1.3 V	110 kΩ	2.9 V
26.1 kΩ	1.4 V	121 kΩ	3.0 V
28.7 kΩ	1.5 V	133 kΩ	3.1 V
31.6 kΩ	1.6 V	147 kΩ	3.2 V
34.8 kΩ	1.7 V	162 kΩ	3.3 V
38.3 kΩ	1.8 V	178 kΩ	5.0 V
42.2 kΩ	1.9 V		

The output voltage may also be set to any value between 0.6 V and 5.0 V using the I^2C interface. See Application Note AN33 for details.

6.4 Start-up Procedure

The ZL2106 follows a specific internal start-up procedure after power is applied to the VDD pins (VDDP and VDDS). Table 7 describes the start-up sequence.

If the device is to be synchronized to an external clock source, the clock frequency must be stable prior to asserting the EN pin. The device requires approximately 5-10 ms to check for specific values stored in its internal memory. If the user has stored values in memory, those values will be loaded. The device will then check the status of all multi-mode pins and load the values associated with the pin settings.

Once this process is completed, the device is ready to accept commands via the I^2C/SMBus interface and the device is ready to be enabled. Once enabled, the device requires approximately 2 ms before its output voltage may be allowed to start its ramp-up process. If a soft-start delay period less than 2 ms has been configured (using PMBus commands), the device will default to a 2 ms delay period. If a delay period greater than 2 ms is configured, the device will wait for the configured delay period prior to starting to ramp its output.

After the delay period has expired, the output will begin to ramp towards its target voltage according to the pre-configured soft-start ramp time that has been set using the SS pin. It should be noted that if the EN pin is tied to VDDP or VDDS, the device will still require approximately 5-10 ms before the output can begin its ramp-up as described in Table 7.

6.5 Soft Start Delay and Ramp Times

It may be necessary to set a delay from when an enable signal is received until the output voltage starts to ramp to its target value. In addition, the designer may wish to set the time required for V_{OUT} to ramp to its target value after the delay period has expired. These features may be used as part of an overall inrush current management strategy or to control how fast a load IC is turned on. The ZL2106 gives the system designer several options for precisely and independently controlling both the delay and ramp time periods.

The soft-start delay period begins when the EN pin is asserted and ends when the delay time expires. The soft-start delay period is set using the SS pin. Precise ramp delay timing mode reduces the delay time variations and is available when the appropriate bit in the MISC_CONFIG register had been set. Please refer to Application Note AN33 for details.

The soft-start ramp timer enables a precisely controlled ramp to the nominal V_{OUT} value that begins once the delay period has expired. The ramp-up is guaranteed monotonic and its slope may be precisely set using the SS pin. Using the pin-strap method, the soft start delay and ramp times can be set to one of three standard values according to Table 9.

Table 9. Soft Start Delay and Ramp Settings

SS Pin Setting	Delay and Ramp Time	UVLO
LOW	2 ms	4.5 V
OPEN	5 ms	
HIGH	10 ms	

If the desired soft start delay and ramp times are not one of the values listed in Table 9, the times can be set to a custom value by connecting a resistor from the SS pin to SGND using the appropriate resistor value from Table 10. The value of this resistor is measured upon start-up or Restore and will not change if the resistor is varied after power has been applied to the ZL2106 (see Figure 14).

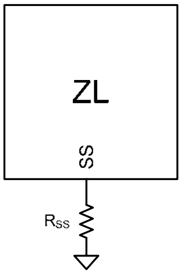


Figure 14. SS Pin Resistor Connections

Table 10. Delay and Ramp Configuration

R_{SS}	Delay Time	Ramp Time	UVLO
10 kΩ	2ms	2ms	4.5 V
11 kΩ		5ms	
12.1 kΩ		10ms	
13.3 kΩ	5ms	2ms	
14.7 kΩ		5ms	
16.2 kΩ		10ms	
17.8 kΩ		20ms	
19.6 kΩ	10ms	2ms	
21.5 kΩ		5ms	
23.7 kΩ		10ms	
26.1 kΩ		20ms	
28.7 kΩ	20ms	2ms	
31.6 kΩ		5ms	
34.8 kΩ		10ms	
38.3 kΩ		20ms	
42.2 kΩ	2ms	2ms	10.8 V
46.4 kΩ		5ms	
51.1 kΩ		10ms	
56.2 kΩ		20ms	
61.9 kΩ	5ms	2ms	
68.1 kΩ		5ms	
75 kΩ		10ms	
82.5 kΩ		20ms	
90.9 kΩ	10ms	2ms	
100 kΩ		5ms	
110 kΩ		10ms	
121 kΩ		20ms	
133 kΩ	20ms	2ms	
147 kΩ		5ms	
162 kΩ		10ms	
178 kΩ		20ms	

The soft start delay and ramp times can also be set to custom values via the I^2C/SMBus interface. When the SS delay time is set to 0 ms, the device will begin its ramp-up after the internal circuitry has initialized (approx. 2 ms). When the soft-start ramp period is set to 0 ms, the output will ramp up as quickly as the output load capacitance and loop settings will allow. It is generally recommended to set the soft-start ramp to a value greater than 500 μs to prevent inadvertent fault conditions due to excessive inrush current.

6.6 Power Good (PG)

The ZL2106 provides a Power Good (PG) signal that indicates the output voltage is within a specified tolerance of its target level and no fault condition exists. By default, the PG pin will assert if the output is within +15%/-10% of the target voltage. These limits may be changed via the I^2C/SMBus interface. See Application Note AN33 for details.

A PG delay period is the time from when all conditions for asserting PG are met and when the PG pin is actually asserted. This feature is commonly used instead of an external reset controller to signal the power supply is at its target voltage prior to enabling any powered circuitry. By default, the ZL2106 PG delay is set to 1 ms and may be changed using the I^2C/SMBus interface as described in AN33.

6.7 Switching Frequency and PLL

The ZL2106 incorporates an internal phase-locked loop (PLL) to clock the internal circuitry. The PLL can be driven by an external clock source connected to the SYNC pin. When using the internal oscillator, the SYNC pin can be configured as a clock source for other Zilker Labs devices.

The SYNC pin is a unique pin that can perform multiple functions depending on how it is configured. The CFG pin is used to select the operating mode of the SYNC pin as shown in Table 11. Figure 15 illustrates the typical connections for each mode.

Table 11. SYNC Pin Function Selection

CFG Pin	SYNC Pin Function
LOW	SYNC is configured as an input
OPEN	Auto detect mode
HIGH	SYNC is configured as an output f_{SW} = 400 kHz

Configuration A: SYNC OUTPUT

When the SYNC pin is configured as an output (CFG pin is tied HIGH), the device will run from its internal oscillator and will drive the resulting internal oscillator signal (preset to 400 kHz) onto the SYNC pin so other devices can be synchronized to it. The SYNC pin will not be checked for an incoming clock signal while in this mode.

Configuration B: SYNC INPUT

When the SYNC pin is configured as an input (CFG pin is tied LOW), the device will automatically check for an external clock signal on the SYNC pin each time

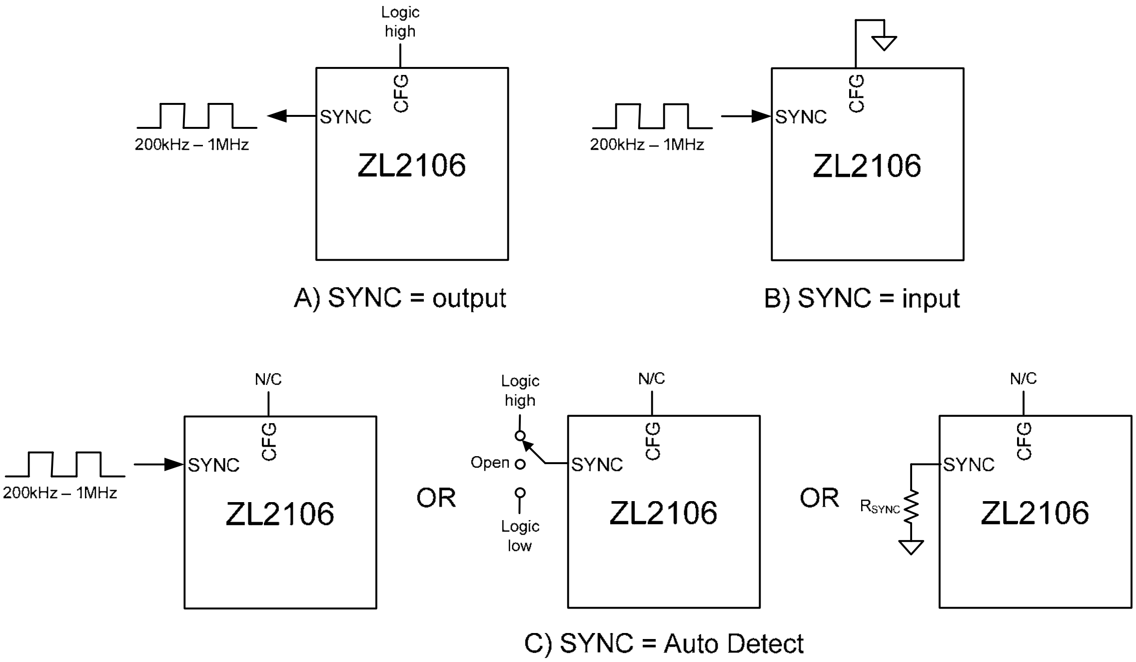


Figure 15. SYNC Pin Configurations

the EN pin is asserted. The internal oscillator will then synchronize with the rising edge of the external clock. The incoming clock signal must be in the range of 200 kHz to 1 MHz with a minimum duty cycle and must be stable when the EN pin is asserted. The external clock signal must also exhibit the necessary performance requirements (see Table 3).

In the event of a loss of the external clock signal, the output voltage may show transient over/undershoot. If this happens, the ZL2106 will automatically switch to its internal oscillator and switch at a frequency close to the previous incoming frequency.

Configuration C: SYNC AUTO DETECT

When the SYNC pin is configured in auto detect mode (CFG pin is left OPEN), the device will automatically check for a clock signal on the SYNC pin after enable is asserted. If a valid clock signal is present, the ZL2106's oscillator will then synchronize with the rising edge of the external clock (refer to SYNC INPUT description).

If no incoming clock signal is present, the ZL2106 will configure the switching frequency according to the state of the SYNC pin as listed in Table 12. In this mode, the ZL2106 will only read the SYNC pin connection during the start-up sequence. Changes to the SYNC pin connection will not affect f_{SW} until the power (VDDS) is cycled off and on again.

Table 12. Switching Frequency Selection

SYNC Pin	Frequency
LOW	200 kHz
OPEN	400 kHz
HIGH	1 MHz
Resistor	See Table 13

If the user wishes to run the ZL2106 at a frequency not listed in Table 12, the switching frequency can be set using an external resistor, R_{SYNC}, connected between SYNC and SGND using Table 13.

Table 13. R_{SYNC} Resistor Values

R_{SYNC}	F_{SW}	R_{SYNC}	F_{SW}
10 kΩ	200 kHz	23.7 kΩ	471 kHz
11 kΩ	222 kHz	26.1 kΩ	533 kHz
12.1 kΩ	242 kHz	28.7 kΩ	571 kHz
13.3 kΩ	267 kHz	31.6 kΩ	615 kHz
14.7 kΩ	296 kHz	34.8 kΩ	727 kHz
16.2 kΩ	320 kHz	38.3 kΩ	800 kHz
17.8 kΩ	364 kHz	46.4 kΩ	889 kHz
19.6 kΩ	400 kHz	51.1 kΩ	1000 kHz
21.5 kΩ	421 kHz		

The switching frequency can also be set to any value between 200 kHz and 1 MHz using the I^2C/SMBus interface. The available frequencies are defined by $f_{SW} = 8$ MHz/N, where whole number N is $8 \leq N \leq 40$. See Application Note AN33 for details.

If a value other than $f_{SW} = 8$ MHz/N is entered using a PMBus command, the internal circuitry will select the valid switching frequency value that is closest to the entered value. For example, if 810 kHz is entered, the device will select 800 kHz (N=10).

Note: The switching frequency read back using the appropriate PMBus command will differ slightly from the selected value in Table 13. The difference is due to hardware quantization.

When multiple Zilker Labs devices are used together, connecting the SYNC pins together will force all devices to synchronize with each other. The CFG pin of one device must set its SYNC pin as an output and the remaining devices must have their SYNC pins set as an input or as auto detect.

Note: Precise ramp timing mode must be disabled to use SYNC clock auto detect.

6.8 Component Selection

The ZL2106 is a synchronous buck converter with integrated MOSFETs that uses an external inductor and capacitors to perform the power conversion process. The proper selection of the external components is critical for optimized performance.

To select the appropriate external components for the desired performance goals, the power supply requirements listed in Table 14 must be defined.

Table 14. Power Supply Requirements

Parameter	Range	Example Value
Input voltage (V_{IN})	4.5 – 14.0 V	12 V
Output voltage (V_{OUT})	0.6 – 5.0 V	3.3 V
Output current (I_{OUT})	0 to 6 A	4 A
Output voltage ripple (V_{orip})	< 3% of V_{OUT}	±1% of V_{OUT}
Output load step (I_{ostep})	< I_o	±25% of I_o
Output load step rate	—	2.5 A/µs
Output deviation due to load step	—	±3% of V_{OUT}
Maximum PCB temp.	120 °C	85 °C
Desired efficiency	—	85%
Other considerations	—	Optimize for small size

6.8.1 Design Goal Trade-offs

The design of the buck power stage requires several compromises among size, efficiency and cost. The inductor core loss increases with frequency, so there is a trade-off between a small output filter made possible by a higher switching frequency and getting better power supply efficiency. Size can be decreased by increasing the switching frequency at the expense of efficiency. Cost can be minimized by using through-hole inductors and capacitors; however these components are physically large.

To start the design, select a frequency based on Table 15. This frequency is a starting point and may be adjusted as the design progresses.

Table 15. Circuit Design Considerations

Frequency Range	Efficiency	Circuit Size
200 – 400 kHz	Highest	Larger
400 – 800 kHz	Moderate	Smaller
800 kHz – 1 MHz	Lower	Smallest

6.8.2 Inductor Selection

The output inductor selection process must include several trade-offs. A high inductance value will result in a low ripple current (I_{opp}), which will reduce output capacitance and produce a low output ripple voltage, but may also compromise output transient load performance. Therefore, a balance must be struck between output ripple and optimal load transient performance. A good starting point is to select the output inductor ripple equal to the expected load transient step magnitude (I_{ostep}):

$$I_{opp} = I_{ostep}$$

Now the output inductance can be calculated using the following equation, where V_{INM} is the maximum input voltage:

$$L_{OUT} = \frac{V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{INM}}\right)}{fsw \times I_{opp}}$$

The average inductor current is equal to the maximum output current. The peak inductor current (I_{Lpk}) is calculated using the following equation where I_{OUT} is the maximum output current:

$$I_{Lpk} = I_{OUT} + \frac{I_{opp}}{2}$$

Select an inductor rated for the average DC current with a peak current rating above the peak current computed above.

In over-current or short-circuit conditions, the inductor may have currents greater than 2X the normal maximum rated output current. It is desirable to use an inductor that still provides some inductance to protect the load and the internal MOSFETs from damaging currents in this situation.

Once an inductor is selected, the DCR and core losses in the inductor are calculated. Use the DCR specified in the inductor manufacturer's datasheet.

$$P_{LDCR} = DCR \times I_{Lrms}{}^{2}$$

I_{Lrms} is given by

$$I_{Lrms} = \sqrt{I_{OUT}{}^{2} + \frac{(I_{opp})^{2}}{12}}$$

where I_{OUT} is the maximum output current. Next, calculate the core loss of the selected inductor. Since this calculation is specific to each inductor and manufacturer, refer to the chosen inductor datasheet. Add the core loss and the DCR loss and compare the total loss to the maximum power dissipation recommendation in the inductor datasheet.

6.8.3 Output Capacitor Selection

Several trade-offs must also be considered when selecting an output capacitor. Low ESR values are needed to have a small output deviation during transient load steps (V_{osag}) and low output voltage ripple (V_{orip}). However, capacitors with low ESR, such as semi-stable (X5R and X7R) dielectric ceramic capacitors, also have relatively low capacitance values. Many designs can use a combination of high capacitance devices and low ESR devices in parallel.

For high ripple currents, a low capacitance value can cause a significant amount of output voltage ripple. Likewise, in high transient load steps, a relatively large amount of capacitance is needed to minimize the output voltage deviation while the inductor current ramps up or down to the new steady state output current value.

As a starting point, apportion one-half of the output ripple voltage to the capacitor ESR and the other half to capacitance, as shown in the following equations:

$$C_{OUT} = \frac{I_{opp}}{8 \times f_{sw} \times \frac{V_{orip}}{2}}$$

$$ESR = \frac{V_{orip}}{2 \times I_{opp}}$$

Use these values to make an initial capacitor selection, using a single capacitor or several capacitors in parallel.

After a capacitor has been selected, the resulting output voltage ripple can be calculated using the following equation:

$$V_{orip} = I_{opp} \times ESR + \frac{I_{opp}}{8 \times f_{sw} \times C_{OUT}}$$

Because each part of this equation was made to be less than or equal to half of the allowed output ripple voltage, the V_{orip} should be less than the desired maximum output ripple.

6.8.4 Input Capacitor

It is highly recommended that dedicated input capacitors be used in any point-of-load design, even when the supply is powered from a heavily filtered 5 or 12 V “bulk” supply from an off-line power supply. This is because of the high RMS ripple current that is drawn by the buck converter topology. This ripple (I_{CINrms}) can be determined from the following equation:

$$I_{CINrms} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

Without capacitive filtering near the power supply circuit, this current would flow through the supply bus and return planes, coupling noise into other system circuitry. The input capacitors should be rated at 1.2X the ripple current calculated above to avoid overheating of the capacitors due to the high ripple current, which can cause premature failure. Ceramic capacitors with X7R or X5R dielectric with low ESR and 1.1X the maximum expected input voltage are recommended.

6.8.5 Bootstrap Capacitor Selection

The high-side driver boost circuit utilizes an internal Schottky diode (D_B) and an external bootstrap capacitor (C_B) to supply sufficient gate drive for the high-side MOSFET driver. C_B should be a 47 nF ceramic type rated for at least 10 V.

6.8.6 C_{V2P5} Selection

This capacitor is used to both stabilize and provide noise filtering for the 2.5 V internal power supply. It should be between 4.7 and 10 µF, should use a semi-stable X5R or X7R dielectric ceramic with a low ESR (less than 10 mΩ) and should have a rating of 4 V or more.

6.8.7 C_{VR} Selection

This capacitor is used to both stabilize and provide noise filtering for the 7 V reference supply. It should be between 4.7 and 10 µF, should use a semi-stable X5R or X7R dielectric ceramic capacitor with a low ESR (less than 10 mΩ) and should have a rating of 10 V or more. Because the current for the bootstrap supply is drawn from this capacitor, C_{VR} should be sized at least 10X the value of C_B so that a discharged C_B does not cause the voltage on it to droop excessively during a C_B recharge pulse.

6.8.8 C_{VRA} Selection

This capacitor is used to both stabilize and provide noise filtering for the analog 5 V reference supply. It should be between 2.2 and 10 µF, should use a semi-stable X5R or X7R dielectric ceramic capacitor with a low ESR (less than 10 mΩ) and should have a rating of 6.3 V or more.

6.8.9 Thermal Considerations

In typical applications, the ZL2106's high efficiency will limit the internal power dissipation inside the package. However, in applications that require a high ambient operating temperature the user must perform some thermal analysis to ensure that the ZL2106's maximum junction temperature is not exceeded.

The ZL2106 has a maximum junction temperature limit of 125 °C, and the internal over temperature limiting circuitry will force the device to shut down if its junction temperature exceeds this threshold. In order to calculate the maximum junction temperature, the user must first calculate the power dissipated inside the IC (P_Q) as follows:

$$P_Q = \left(I_{LOAD}{}^2\right)\left[\left(R_{DS(ON)QH}\right)(D) + \left(R_{DS(ON)QL}\right)(1-D)\right]$$

The maximum operating junction temperature can then be calculated using the following equation:

$$T_{j\max} = T_{PCB} + \left(P_Q \times \theta_{JC}\right)$$

Where T_{PCB} is the expected maximum printed circuit board temperature and θ_{JC} is the junction-to-case thermal resistance for the ZL2106 package.

6.9 Current Sensing and Current Limit Threshold Selection

The ZL2106 incorporates a patented "lossless" current sensing method across the internal low-side MOSFET that is independent of $R_{DS(ON)}$ variations, including temperature. The default value for the gain, which does not represent a $R_{DS(ON)}$ value, and the offset of the internal current sensing circuit can be modified by the IOUT_CAL_GAIN and IOUT_CAL_OFFSET commands.

The design should include a current limiting mechanism to protect the power supply from damage and prevent excessive current from being drawn from the input supply in the event that the output is shorted to ground or an overload condition is imposed on the output. Current limiting is accomplished by sensing the current through the circuit during a portion of the duty cycle. The current limit threshold is set to 9 A by default. The current limit threshold can set to a custom value via the I^2C/SMBus interface. Please refer to Application Note AN33 for further details.

Additionally, the ZL2106 gives the power supply designer several choices for the fault response during over or under current conditions. The user can select the number of violations allowed before declaring a fault, a blanking time and the action taken when a fault is detected. The blanking time represents the time when no current measurement is taken. This is to avoid taking a reading just after a current load step (less accurate due to potential ringing). Please refer to Application note AN33 for further details.

Table 16. Resistor Settings for Loop Compensation

f_n Range	f_{zesr} Range	R_{FC}
$f_{sw}/60 < f_n < f_{sw}/30$	$f_{zesr} > f_{sw}/10$	10 kΩ
	$f_{sw}/10 > f_{zesr} > f_{sw}/30$	11 kΩ
	$f_{sw}/30 > f_{zesr} > f_{sw}/60$	12.1 kΩ
$f_{sw}/120 < f_n < f_{sw}/60$	$f_{zesr} > f_{sw}/10$	13.3 kΩ
	$f_{sw}/10 > f_{zesr} > f_{sw}/30$	14.7 kΩ
	$f_{sw}/30 > f_{zesr} > f_{sw}/60$	16.2 kΩ
$f_{sw}/240 < f_n < f_{sw}/120$	$f_{zesr} > f_{sw}/10$	17.8 kΩ
	$f_{sw}/10 > f_{zesr} > f_{sw}/30$	19.6 kΩ
	$f_{sw}/30 > f_{zesr} > f_{sw}/60$	21.5 kΩ

6.10 Loop Compensation

The ZL2106 operates as a voltage-mode synchronous buck controller with a fixed frequency PWM scheme. Although the ZL2106 uses a digital control loop, it operates much like a traditional analog PWM controller. Figure 16 is a simplified block diagram of the ZL2106 control loop, which differs from an analog control loop only by the constants in the PWM and compensation blocks. As in the analog controller case, the compensation block compares the output voltage to the desired voltage reference and compensation zeroes are added to keep the loop stable. The resulting integrated error signal is used to drive the PWM logic, converting the error signal to a duty cycle to drive the internal MOSFETs.

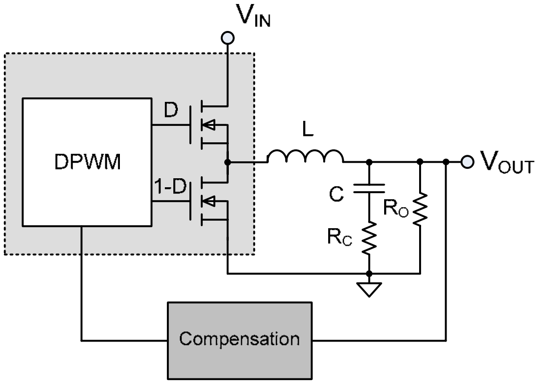


Figure 16. Control Loop Block Diagram

In the ZL2106, the compensation zeros are set by configuring the FC pin or via the I^{2}C/SMBus interface once the user has calculated the required settings. This method eliminates the inaccuracies due to the component tolerances associated with using external resistors and capacitors required with traditional analog controllers. Utilizing the loop compensation settings shown in Table 16 will yield a conservative crossover frequency at a fixed fraction of the switching frequency ($f_{SW}/20$) and 60° of phase margin.

Step 1: Using the following equation, calculate the resonant frequency of the LC filter, f_n.

$$f_n = \frac{1}{2\pi\sqrt{L \times C}}$$

Step 2: Calculate the ESR zero frequency (f_{zesr}).

$$f_{zesr} = \frac{1}{2\pi CRc}$$

Step 3: Based on Table 16, determine the appropriate resistor, R_{FC}.

The loop compensation coefficients can also be set via the I^{2}C/SMBus interface. Please refer to Application Note AN33 for further details. Also refer to Application Note AN35 for further technical details on setting loop compensation.

6.11 Driver Dead-time Control

The ZL2106 utilizes a predetermined fixed dead-time applied between the gate drive signals for the top and bottom MOSFETs.

In a synchronous buck converter, the MOSFET drive circuitry must be operated such that the top and bottom MOSFETs are never in the conducting state at the same time. This is because potentially damaging currents flow in the circuit if both MOSFETs are on simultaneously for periods of time exceeding a few nanoseconds. Conversely, long periods of time in which both MOSFETs are off reduces overall circuit efficiency by allowing current to flow in their parasitic body diodes.

Therefore, it is advantageous to minimize the dead-time to provide peak optimal efficiency without compromising system reliability. The ZL2106 has optimized the dead-time for the integrated MOSFETs to maximizing efficiency.

7. Power Management Functional Description

7.1 Input Undervoltage Lockout

The input undervoltage lockout (UVLO) prevents the ZL2106 from operating when the input falls below a preset threshold, indicating the input supply is out of its specified range. The UVLO threshold (V_{UVLO}) can be set to either 4.5 V or 10.8 V using the SS pin according to Table 10.

The UVLO voltage can also be set to any value between 2.85 V and 16 V via the I^2C/SMBus interface.

Once an input undervoltage fault condition occurs, the device can respond in a number of ways as follows:

1. Continue operating without interruption.
2. Continue operating for a given delay period, followed by shutdown if the fault still exists. The device will remain in shutdown until instructed to restart.
3. Initiate an immediate shutdown until the fault has been cleared. The user can select a specific number of retry attempts.

The default response from a UVLO fault is an immediate shutdown of the device. Please refer to Application Note AN33 for details on how to configure the UVLO threshold or to select specific UVLO fault response options via the I^2C/SMBus interface.

7.2 Output Overvoltage Protection

The ZL2106 offers an internal output overvoltage protection circuit that can be used to protect sensitive load circuitry from being subjected to a voltage higher than its prescribed limits. A hardware comparator is used to compare the actual output voltage (seen at the VSEN pin) to a threshold set to 15% higher than the target output voltage (the default setting). If the VSEN voltage exceeds this threshold, the PG pin will de-assert and the device can then respond in a number of ways as follows:

1. Initiate an immediate shutdown until the fault has been cleared. The user can select a specific number of retry attempts.
2. Turn off the high-side MOSFET and turn on the low-side MOSFET. The low-side MOSFET remains on until the device attempts a restart.

The default response from an overvoltage fault is to immediately shut down. For continuous overvoltage protection when operating from an external clock, the only allowed response is an immediate shutdown. Please refer to Application Note AN33 for details on how to select specific overvoltage fault response options via I^2C/SMBus.

7.3 Output Pre-Bias Protection

An output pre-bias condition exists when an externally applied voltage is present on a power supply's output before the power supply's control IC is enabled. Certain applications require that the converter not be allowed to sink current during start up if a pre-bias condition exists at the output. The ZL2106 provides pre-bias protection by sampling the output voltage prior to initiating an output ramp.

If a pre-bias voltage lower than the target voltage exists after the pre-configured delay period has expired, the target voltage is set to match the existing pre-bias voltage and both drivers are enabled. The output voltage is then ramped to the final regulation value at the ramp rate set by the SS pin.

The actual time the output will take to ramp from the pre-bias voltage to the target voltage will vary depending on the pre-bias voltage but the total time elapsed from when the delay period expires and when the output reaches its target value will match the pre-configured ramp time (see Figure 17).

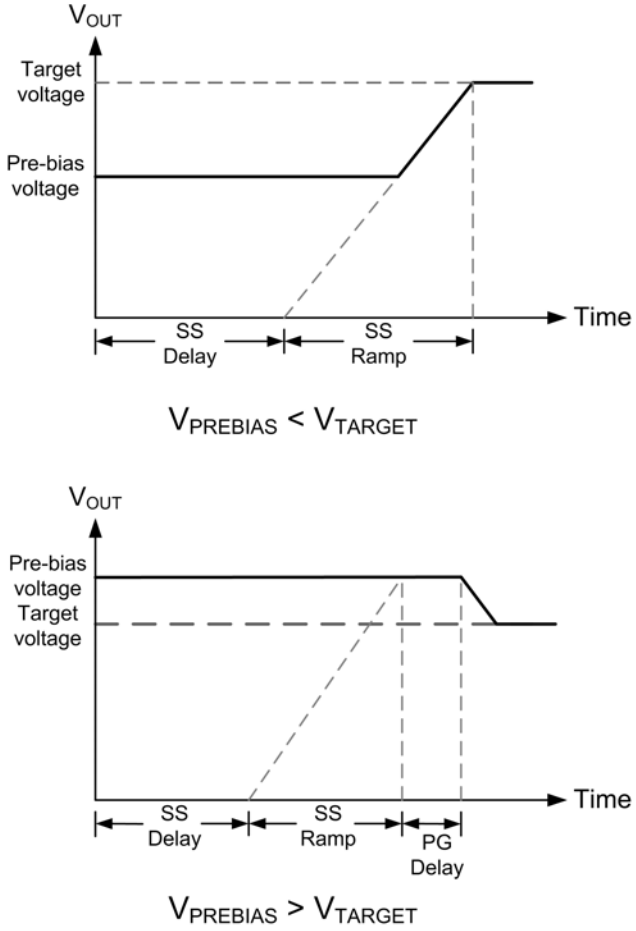


Figure 17. Output Responses to Pre-bias Voltages

If a pre-bias voltage higher than the target voltage exists after the pre-configured delay period has expired, the target voltage is set to match the existing pre-bias voltage and both drivers are enabled with a PWM duty cycle that would ideally create the pre-bias voltage.

Once the pre-configured soft-start ramp period has expired, the PG pin will be asserted (assuming the pre-bias voltage is not higher than the overvoltage limit). The PWM will then adjust its duty cycle to match the original target voltage and the output will ramp down to the pre-configured output voltage.

If a pre-bias voltage higher than the overvoltage limit exists, the device will not initiate a turn-on sequence and will declare an overvoltage fault condition to exist. In this case, the device will respond based on the output overvoltage fault response method that has been selected. See Section 7.2 "Output Overvoltage Protection," for response options due to an overvoltage condition.

7.4 Output Overcurrent Protection

The ZL2106 can protect the power supply from damage if the output is shorted to ground or if an overload condition is imposed on the output. Once the current limit threshold has been selected (see Section 6.9 "Current Limit Threshold Selection"), the user may determine the desired course of action in response to the fault condition. The following overcurrent protection response options are available:

1. Initiate a shutdown and attempt to restart an infinite number of times with a preset delay period between attempts.
2. Initiate a shutdown and attempt to restart a preset number of times with a preset delay period between attempts.
3. Continue operating for a given delay period, followed by shutdown if the fault still exists.
4. Continue operating through the fault (this could result in permanent damage to the power supply).
5. Initiate an immediate shutdown.

The default response from an overcurrent fault is an immediate shutdown of the device. Please refer to Application Note AN33 for details on how to select specific overcurrent fault response options via I^{2}C/SMBus.

7.5 Thermal Overload Protection

The ZL2106 includes an on-chip thermal sensor that continuously measures the internal temperature of the die and will shutdown the device when the temperature exceeds the preset limit. The factory default temperature limit is set to 125 °C, but the user may set the limit to a different value if desired. See Application Note AN33 for details. Note that setting a higher thermal limit via the I^{2}C/SMBus interface may result in permanent damage to the device. Once the device has been disabled due to an internal temperature fault, the user may select one of several fault response options as follows:

1. Initiate a shutdown and attempt to restart an infinite number of times with a preset delay period between attempts.
2. Initiate a shutdown and attempt to restart a preset number of times with a preset delay period between attempts.

3. Continue operating for a given delay period, followed by shutdown if the fault still exists.
4. Continue operating through the fault (this could result in permanent damage to the power supply).
5. Initiate an immediate shutdown.

If the user has configured the device to restart, the device will wait the preset delay period (if configured to do so) and will then check the device temperature. If the temperature has dropped below a threshold that is approx 15 °C lower than the selected temperature fault limit, the device will attempt to re-start. If the temperature still exceeds the fault limit the device will wait the preset delay period and retry again.

The default response from a temperature fault is an immediate shutdown of the device. Please refer to Application Note AN33 for details on how to select specific temperature fault response options via I^2C/SMBus.

7.6 Voltage Tracking

Numerous high performance systems place stringent demands on the order in which the power supply voltages are turned on. This is particularly true when powering FPGAs, ASICs, and other advanced processor devices that require multiple supply voltages to power a single die. In most cases, the I/O interface operates at a higher voltage than the core and therefore the core supply voltage must not exceed the I/O supply voltage according to the manufacturers' specifications.

Voltage tracking protects these sensitive ICs by limiting the differential voltage between multiple power supplies during the power-up and power down sequence. The ZL2106 integrates a lossless tracking scheme that allows its output to track a voltage that is applied to the VTRK pin with no additional components required. The VTRK pin is an analog input that, when tracking mode is enabled, configures the voltage applied to the VTRK pin to act as a reference for the device’s output regulation.

The ZL2106 offers two modes of tracking. Figure 18 illustrates the output voltage waveform for the two tracking modes.

1. *Coincident*. This mode configures the ZL2106 to ramp its output voltage at the same rate as the voltage applied to the VTRK pin.
2. *Ratiometric*. This mode configures the ZL2106 to ramp its output voltage at a rate that is a percentage of the voltage applied to the VTRK pin. The default setting is 50%, but an external resistor may be used to configure a different tracking ratio.

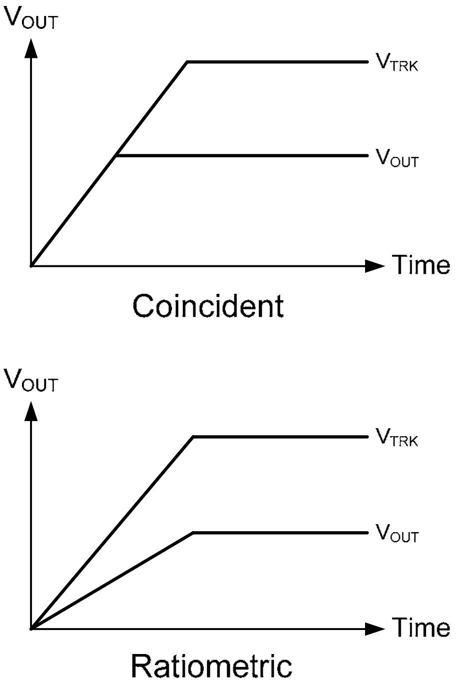


Figure 18. Tracking Modes

The master device in a tracking group is defined as the device that has the highest target output voltage within the group. This master device will control the ramp rate of all tracking devices and is not configured for tracking mode. A delay of at least 10 ms must be configured into the master device using the SS pin, and the user may also configure a specific ramp rate using the SS pin. Tracking mode is enabled through the CFG pin, as shown in Table 20, and configured through the SS pin, as show in Table 17.

Any device that is configured for tracking mode will ignore its soft-start delay and ramp time settings (SS pin) and its output will take on the turn-on/turn-off characteristics of the reference voltage present at the VTRK pin. All of the ENABLE pins in the tracking group must be connected together and driven by a single logic source.

Tracking mode can also be configured via the I^2C/SMBus interface by using the TRACK_CONFIG

PMBus command. Please refer to Application Note AN33 for more information on configuring tracking mode using PMBus.

7.7 Voltage Margining

The ZL2106 offers a simple means to vary its output higher or lower than its nominal voltage setting in order to determine whether the load device is capable of operating over its specified supply voltage range. The MGN command is set by driving the MGN pin or through the I^2C/SMBus interface. The MGN pin is a tri-level input that is continuously monitored and can be driven directly by a processor I/O pin or other logic-level output.

The ZL2106's output will be forced higher than its nominal set point when the MGN command is set HIGH, and the output will be forced lower than its nominal set point when the MGN command is set LOW. Default margin limits of V_{NOM} ±5% are pre-loaded in the factory, but the margin limits can be modified through the I^2C/SMBus interface to as high as V_{NOM} + 10% or as low as 0V, where V_{NOM} is the nominal output voltage set point determined by the VSET pin. A safety feature prevents the user from configuring the output voltage to exceed V_{NOM} + 10% under any conditions.

The margin limits and the MGN command can both be set individually through the I^2C/SMBus interface. Additionally, the transition rate between the nominal output voltage and either margin limit can be configured through the I^2C/SMBus interface. Please refer to Application Note AN33 for detailed instructions on modifying the margining configurations.

Table 17. Tracking Mode Configuration

R_{SS}	UVLO	Tracking Ratio	Upper Track Limit	Ramp-up/down Behavior
19.6 kΩ	4.5V	100%	Limited by target voltage	Output not allowed to decrease before PG
21.5 kΩ				Output will always follow VTRK
23.7 kΩ			Limited by VTRK pin voltage	Output not allowed to decrease before PG
26.1 kΩ				Output will always follow VTRK
28.7 kΩ		50%	Limited by target voltage	Output not allowed to decrease before PG
31.6 kΩ				Output will always follow VTRK
34.8 kΩ			Limited by VTRK pin voltage	Output not allowed to decrease before PG
38.3 kΩ				Output will always follow VTRK
42.2 kΩ	10.8V	100%	Limited by target voltage	Output not allowed to decrease before PG
46.4 kΩ				Output will always follow VTRK
51.1 kΩ			Limited by VTRK pin voltage	Output not allowed to decrease before PG
56.2 kΩ				Output will always follow VTRK
61.9 kΩ		50%	Limited by target voltage	Output not allowed to decrease before PG
68.1 kΩ				Output will always follow VTRK
75 kΩ			Limited by VTRK pin voltage	Output not allowed to decrease before PG
82.5 kΩ				Output will always follow VTRK

7.8 I^2C/SMBus Communications

The ZL2106 provides an I^2C/SMBus digital interface that enables the user to configure all aspects of the device operation as well as monitor the input and output parameters. The ZL2106 can be used with any standard 2-wire I^2C host device.

In addition, the device is compatible with SMBus version 2.0 and includes an SALRT line to help mitigate bandwidth limitations related to continuous fault monitoring. Pull-up resistors are required on the I^2C/SMBus as specified in the SMBus 2.0 specification. The ZL2106 accepts most standard PMBus commands. When controlling the device with PMBus commands, it is recommended that the enable pin is tied to SGND.

7.9 I^2C/SMBus Device Address Selection

When communicating with multiple devices using the I^2C/SMBus interface, each device must have its own unique address so the host can distinguish between the devices. The device address can be set according to the pin-strap options listed in Table 18. Address values are right-justified.

Table 18. SMBus Device Address Selection

SA Pin Setting	SMBus Address
LOW	0x20
OPEN	0x21
HIGH	0x22

If additional device addresses are required, a resistor can be connected to the SA pin according to Table 19 to provide up to 30 unique device addresses.

Table 19. SMBus Address Values

R_{SA}	SMBus Address	R_{SA}	SMBus Address
10 kΩ	0x20	42.2 kΩ	0x2F
11 kΩ	0x21	46.4 kΩ	0x30
12.1 kΩ	0x22	51.1 kΩ	0x31
13.3 kΩ	0x23	56.2 kΩ	0x32
14.7 kΩ	0x24	61.9 kΩ	0x33
16.2 kΩ	0x25	68.1 kΩ	0x34
17.8 kΩ	0x26	75 kΩ	0x35
19.6 kΩ	0x27	82.5 kΩ	0x36
21.5 kΩ	0x28	90.9 kΩ	0x37
23.7 kΩ	0x29	100 kΩ	0x38
26.1 kΩ	0x2A	110 kΩ	0x39
28.7 kΩ	0x2B	121 kΩ	0x3A
34.8 kΩ	0x2C	133 kΩ	0x3B
31.6 kΩ	0x2D	147 kΩ	0x3C
38.3 kΩ	0x2E	162 kΩ	0x3D

7.10 Digital-DC Bus

The Digital-DC Communications (DDC) bus is used to communicate between Zilker Labs Digital-DC devices. This dedicated bus provides the communication channel between devices for features such as sequencing and fault spreading. The DDC pin on all Digital-DC devices in an application should be connected together. A pull-up resistor is required on the DDC bus in order to guarantee the rise time as follows:

Rise time = $R_{PU} * C_{LOAD} \approx 1\mu s$,

Where R_{PU} is the DDC bus pull-up resistance and C_{LOAD} is the bus loading. The pull-up resistor may be tied to VRA or to an external 3.3 V or 5 V supply as long as this voltage is present prior to or during device power-up. As rules of thumb, each device connected to the DDC bus presents approx 10 pF of capacitive loading, and each inch of FR4 PCB trace introduces approx 2 pF. The ideal design will use a central pull-up resistor that is well-matched to the total load capacitance. In power module applications, the user should consider whether to place the pull-up resistor on the module or on the PCB of the end application.

The minimum pull-up resistance should be limited to a value that enables any device to assert the bus to a voltage that will ensure a logic 0 (typically 0.8 V at the device monitoring point) given the pull-up voltage (5 V if tied to VRA) and the pull-down current capability of the ZL2106 (nominally 4 mA).

7.11 Phase Spreading

When multiple point of load converters share a common DC input supply, it is desirable to adjust the clock phase offset of each device such that not all devices start to switch simultaneously. Setting each converter to start its switching cycle at a different point in time can dramatically reduce input capacitance requirements and efficiency losses. Since the peak current drawn from the input supply is effectively spread out over a period of time, the peak current drawn at any given moment is reduced and the power losses proportional to the I_{RMS}^2 are reduced dramatically.

In order to enable phase spreading, all converters must be synchronized to the same switching clock. The CFG pin is used to set the configuration of the SYNC pin for each device as described in Section 6.7 “Switching Frequency and PLL”.

Selecting the phase offset for the device is accomplished by selecting a device address according to the following equation:

Phase offset = device address x 45°

For example:

- A device address of 0x00 or 0x20 would configure no phase offset
- A device address of 0x01 or 0x21 would configure 45° of phase offset
- A device address of 0x02 or 0x22 would configure 90° of phase offset

The phase offset of each device may also be set to any value between 0° and 360° in 22.5° increments via the I^{2}C/SMBus interface. Refer to Application Note AN33 for further details.

7.12 Output Sequencing

A group of Zilker Labs devices may be configured to power up in a predetermined sequence. This feature is especially useful when powering advanced processors, FPGAs, and ASICs that require one supply to reach its operating voltage prior to another supply reaching its operating voltage in order to avoid latch-up from occurring. Multi-device sequencing can be achieved by configuring each device through the I^{2}C/SMBus interface or by using Zilker Labs patented autonomous sequencing mode.

Autonomous sequencing mode configures sequencing by using events transmitted between devices over the DDC bus.

Table 20. CFG Pin Configurations for Sequencing and Tracking

R_{CFG}	SYNC Pin Configuration	Sequencing Configuration
Low	Input	Sequencing and Tracking are disabled.
Open	Auto detect	
High	Output	
10 kΩ	Input	Sequencing and Tracking are disabled.
11 kΩ	Auto detect	
12.1 kΩ	Output	
14.7 kΩ	Input	Device is FIRST in nested sequence. Tracking disabled.
16.2 kΩ	Auto detect	
17.8 kΩ	Output	
21.5 kΩ	Input	Device is LAST in nested sequence. Tracking disabled.
23.7 kΩ	Auto detect	
26.1 kΩ	Output	
31.6 kΩ	Input	Device is MIDDLE in nested sequence. Tracking disabled.
34.8 kΩ	Auto detect	
38.3 kΩ	Output	
46.4 kΩ	Input	Sequence disabled. Tracking enabled as defined in Table 17.
51.1 kΩ	Auto detect	
56.2 kΩ	Output	

The sequencing order is determined using each device’s SMBus address. Using autonomous sequencing mode (configured using the CFG pin), the devices must be assigned sequential SMBus addresses with no missing addresses in the chain. This mode will also constrain each device to have a phase offset according to its SMBus address as described in section 7.11 “Phase Spreading”.

The sequencing group will turn on in order starting with the device with the lowest SMBus address and will continue through to turn on each device in the address chain until all devices connected have been turned on. When turning off, the device with the highest SMBus address will turn off first followed in reverse order by the other devices in the group.

Sequencing is configured by connecting a resistor from the CFG pin to ground as described in Table 20. The CFG pin is also used to set the configuration of the SYNC pin as well as to determine the sequencing method and order. Please refer to section 6.7 “Switching Frequency and PLL” for more details on the operating parameters of the SYNC pin.

Multiple device sequencing may also be achieved by issuing PMBus commands to assign the preceding device in the sequencing chain as well as the device that will follow in the sequencing chain. This method places fewer restrictions on the SMBus address (no need of sequential address) and also allows the user to assign any phase offset to any device irrespective of its SMBus device address.

The Enable pins of all devices in a sequencing group must be tied together and driven high to initiate a sequenced turn-on of the group. Enable must be driven low to initiate a sequenced turnoff of the group. Please refer to Application Note AN33 for details on sequencing via the I^{2}C/SMBus interface.

7.13 Fault Spreading

Digital-DC devices can be configured to broadcast a fault event over the DDC bus to the other devices in the group. When a non-destructive fault occurs and the device is configured to shut down on a fault, the device will shut down and broadcast the fault event over the DDC bus. The other devices on the DDC bus will shut down together if configured to do so, and will attempt to re-start in their prescribed order if configured to do so.

7.14 Monitoring via I^{2}C/SMBus

A system controller can monitor a wide variety of different ZL2106 system parameters through the I^{2}C/SMBus interface. The device can monitor for fault conditions by monitoring the SALRT pin, which will be pulled low when any number of pre-configured fault conditions occur.

The device can also be monitored continuously for any number of power conversion parameters including input voltage, output voltage, output current, internal junction temperature, switching frequency and duty cycle.

The PMBus host should respond to SALRT as follows:

1. ZL device pulls SALRT low.
2. PMBus host detects that SALRT is now low, performs transmission with Alert Response Address to find which ZL device is pulling SALRT low.
3. PMBus host talks to the ZL device that has pulled SALRT low. The actions that the host performs are up to the system designer.

If multiple devices are faulting, SALRT will still be low after doing the above steps and will require transmission with the Alert Response Address repeatedly until all faults are cleared. Please refer to Application Note AN33 for details on how to monitor specific parameters via the I^{2}C/SMBus interface.

7.15 *Snapshot*™ Parametric Capture

The ZL2106 offers a special feature that enables the user to capture parametric data during normal operation or following a fault. The Snapshot functionality is enabled by setting bit 1 of MISC_CONFIG to 1.

The Snapshot feature enables the user to read the parameters listed in Table 21 via a block read transfer through the SMBus. This can be done during normal operation, although it should be noted that reading the 22 bytes will occupy the SMBus for some time.

Table 21. Snapshot Parameters

Byte	Description	Format
31:22	Reserved	Linear
21:20	Vin	Linear
19:18	Vout	Vout Linear
17:16	Iout,ave	Linear
15:14	Iout,peak	Linear
13:12	Duty cycle	Linear
11:10	Internal temp	Linear
9:8	External temp	Linear
7:6	fsw	Linear
5	Vout status	Byte
4	Iout status	Byte
3	Input status	Byte
2	Temp status	Byte
1	CML status	Byte
0	Mfr specific status	Byte

The SNAPSHOT_CONTROL command enables the user to store the snapshot parameters to Flash memory in response to a pending fault as well as to read the stored data from Flash memory after a fault has occurred. Table 22 describes the usage of this command. Automatic writes to Flash memory following a fault are triggered when any fault threshold level is exceeded, provided that the specific fault's response is to shut down (writing to Flash memory is not allowed if the device is configured to re-try following the specific fault condition).

It should also be noted that the device's V_{DD} voltage must be maintained during the time when the device is writing the data to Flash memory; a process that requires between 700-1400 µs depending on whether the data is set up for a block write. Undesirable results may be observed if the device's V_{DD} supply drops below 3.0 V during this process.

Table 22. SNAPSHOT_CONTROL Command

Data Value	Description
1	Copies current SNAPSHOT values from Flash memory to RAM for immediate access using SNAPSHOT command.
2	Writes current SNAPSHOT values to Flash memory. Only available when device is disabled.

In the event that the device experiences a fault and power is lost, the user can extract the last SNAPSHOT parameters stored during the fault by writing a 1 to SNAPSHOT_CONTROL (transfers data from Flash memory to RAM) and then issuing a SNAPSHOT command (reads data from RAM via SMBus).

7.16 Non-Volatile Memory and Device Security Features

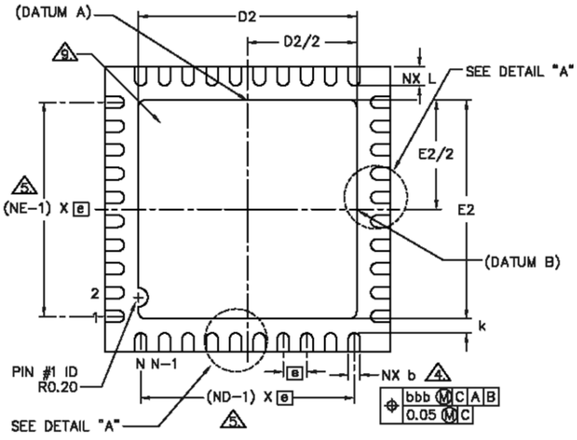
The ZL2106 has internal non-volatile memory where user configurations are stored. Integrated security measures ensure that the user can only restore the device to a level that has been made available to them. Refer to Section 6.4 "Start-up Procedure," for details on how the device loads stored values from internal memory during start-up.

During the initialization process, the ZL2106 checks for stored values contained in its internal memory. The ZL2106 offers two internal memory storage units that are accessible by the user as follows:

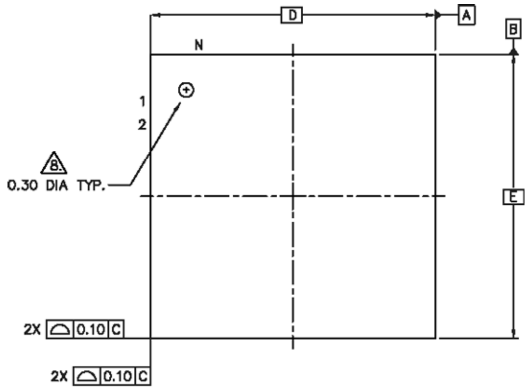
1. *Default Store*: A power supply module manufacturer may want to protect the module from damage by preventing the user from being able to modify certain values that are related to the physical construction of the module. In this case, the module manufacturer would use the Default Store and would allow the user to restore the device to its default setting but would restrict the user from restoring the device to the factory settings.
2. *User Store*: The manufacturer of a piece of equipment may want to provide the ability to modify certain power supply settings while still protecting the equipment from modifying values that can lead to a system level fault. The equipment manufacturer would use the User Store to achieve this goal.

Please refer to Application Note AN33 for details on how to set specific security measures via the I^2C/SMBus interface.

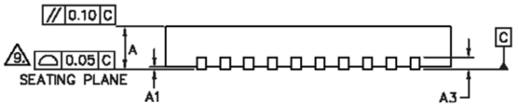
8. Package Dimensions



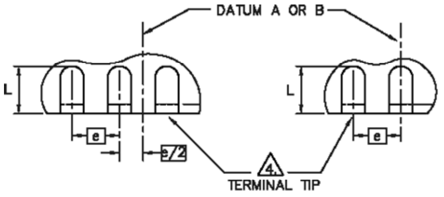
BOTTOM VIEW



TOP VIEW



SIDE VIEW



EVEN TERMINAL/SIDE

ODD TERMINAL/SIDE

DETAIL 'A"

Notes:

1. Dimensions and tolerances conform to ASME Y14.5M – 1994.
2. All dimensions are in millimeters, θ is in degrees.
3. N is the total number of terminals.
4. Dimension b applies to metalized terminal and is measured between 0.15 and 0.33 mm from terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.
5. ND and NE refer to the number of terminals on each D and E side respectively.
6. Max package warpage is 0.05 mm.
7. Maximum allowable burrs is 0.076 mm in all directions.
8. Pin #1 ID on top will be laser marked.
9. Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.
10. This drawing conforms to JEDEC registered outline MO- 220.

SYMBOL	DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.80	0.85	0.90	
A1	0.00	0.02	0.05	
A3	0.20 REF			
θ	0	-	12	2
k	0.20 MIN			
D	6.0 BSC			
E	6.0 BSC			
e	0.50 BSC			
N	36			3
ND	9			5
NE	9			5
L	0.55	0.60	0.65	
b	0.18	0.25	0.30	4
D2	4.00	4.10	4.20	
E2	4.00	4.10	4.20	

9. Ordering Information

Z L 2 1 0 6 A L B N T

Product Designator

Shipping Option
T = Tape & Reel 100 pcs
T1 = Tape & Reel 1000 pcs
Contact factory for other options

Lead Finish
N = Lead-free NiPdAu

Firmware Revision
Alpha character

Ambient Temperature Range
L = -40 to +85°C

Package Designator
A = QFN package

10. Tools and Related Documentation

The following application support documents and tools are available to help simplify your design.

Item	**Description**
ZL2106EVK1	Evaluation Kit – ZL2106EV1, USB Adapter Board, GUI Software
AN10	Application Note: Thermal and Layout Guidelines
AN33	Application Note: PMBus Command Set
AN35	Application Note: Compensation Using CompZL

11. Revision History

Rev. #	Description	Date
1.0	Initial Release	August 2008
1.1	Added Notes 1, 5, 8 and 9 to Table 3 Corrected T_j = 25 °C in Figure 2 and Figure 3 Added $T_j \leq$ 125 °C in Figure 5 and Figure 6 Added last paragraph to Section 5.4 Changed PG delay to 1 ms in Section 6.6 Added note for SYNC clock auto detect in Section 6.7 Updated first paragraph of Section 6.9 Changed default fault response to immediate shutdown in Sections 7.1 , 7.2 , 7.4 , and 7.5 . Updated Ordering Information	November 2008
FN6852.0	Assigned file number FN6852 to datasheet as this will be the first release with an Intersil file number. Replaced header and footer with Intersil header and footer. Updated disclaimer information to read "Intersil and it's subsidiaries including Zilker Labs, Inc." No changes to datasheet content	February 2009

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