PAS109BC QQVGA COLOR CMOS IMAGE SENSOR
PAS109BB QQVGA MONO CMOS IMAGE SENSOR

General Description

The PAS109B is a color and monochrome digital CMOS image sensor with resolution of 164(H) x 124(V). The PAS109B outputs 8, 4 , 2 or 1-bit digital raw data or 8-bit formatted data per pixel.

The PAS109B performs automatic gain control, automatic exposure control and automatic de-flicker. The PAS109B can also be programmed via I^2C^{TM} serial control bus. By programming the internal register settings, it performs on-chip frame rate adjustment, exposure control, offset correction DAC, programmable gain control as well as output formatting. By proprietary technology, FPN, smear and blooming are drastically reduced.

The PAS109 is available in color or monochrome in 32-pin LCC or 32-pin chip-with-lens package.

Features

- **164x124 pixels, 1/11" Lens**
- **Automatic/Manual exposure-gain control**
- **On chip 10-bit ADC**
- **On chip PGA**
- **On chip 9-bit DAC**
- **User selectable output data formats:**
  - **8-bit formatted data**
  - **8/4/2/1-bit raw data**
- **Output tri-state through /CSB pin or register**
- **AE report**
- **Horizontal mirror output**
- **Flash light application allowable**
- **Automatic de-flicker**
- **External oscillator**
- **I^2C Interface**
- **Wide operating supply range: 2.4 – 3.6V**
- **Low power dissipation: 16mW @ 60fps**
- **Low power down dissipation: 200µW**

Key Specification

Power Supply	**Wide operating supply range 2.4V ~ 3.6V**
Array Elements	**164 x 124**
Optical Format	**1/11 "**
Pixel Size	**7.25µm x 7.25µm**
System Clock	**Up to 48MHz**
Max. Pixel Rate	**1.5MHz**
FPN	**< 0.2% of saturation**
Sensitivity	**2.0V/Lux-sec**
PGA Gain	**16X (24dB)**
Frame Rate	**60fps**
Scan Mode	**Progressive**
S/N ratio	**>40dB**
Package	**32-pin LCC or 32-pin LCC chip with lens**

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1. Pin Assignment

Pin#	Name	Type	Description
Power Supply			
28	VDDD	P	Digital VDD
27	GNDD	P	Digital Ground
3	VDDA	P	Analog VDD
2	GNDA	P	Analog Ground
19	VDDQ	P	Digital VDD
18	GNDQ	P	Digital Ground
1	GNDE	P	Ground
Data Interface			
17	D0	O	Pixel data output, LSB
16	D1	O	Pixel data output
15	D2	O	Pixel data output
12	D3	O	Pixel data output
11	D4	O	Pixel data output
10	D5	O	Pixel data output
9	D6	O	Pixel data output
8	D7	O	Pixel data output, MSB
22	PXCK	O	Pixel clock output
23	HSYNC	O	Horizontal Synchronization clock
24	VSYNC	O	Vertical Synchronization clock
Analog pin			
6	VRT	I/O	ADC reference voltage, top level
4	VCM	I/O	Common mode voltage reference
5	VRB	I/O	ADC reference voltage, bottom level
7	VDDY1	BYPASS	Reference voltage
I^2C			
25	SCL	I	I2C interface clock
26	SDA	I/O	I2C interface bi-direction data
Misc. Pins			
30	CSB	I	Chip select bar, active low
20	SYSCLK	I	System clock input pin
14	VLRST	BIAS	Fixed bias input voltage
13	NC	-	Not connected
21	NC	-	Not connected
29	NC	-	Not connected
31	NC	-	Not connected
32	NC	-	Not connected

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2. Block Diagram

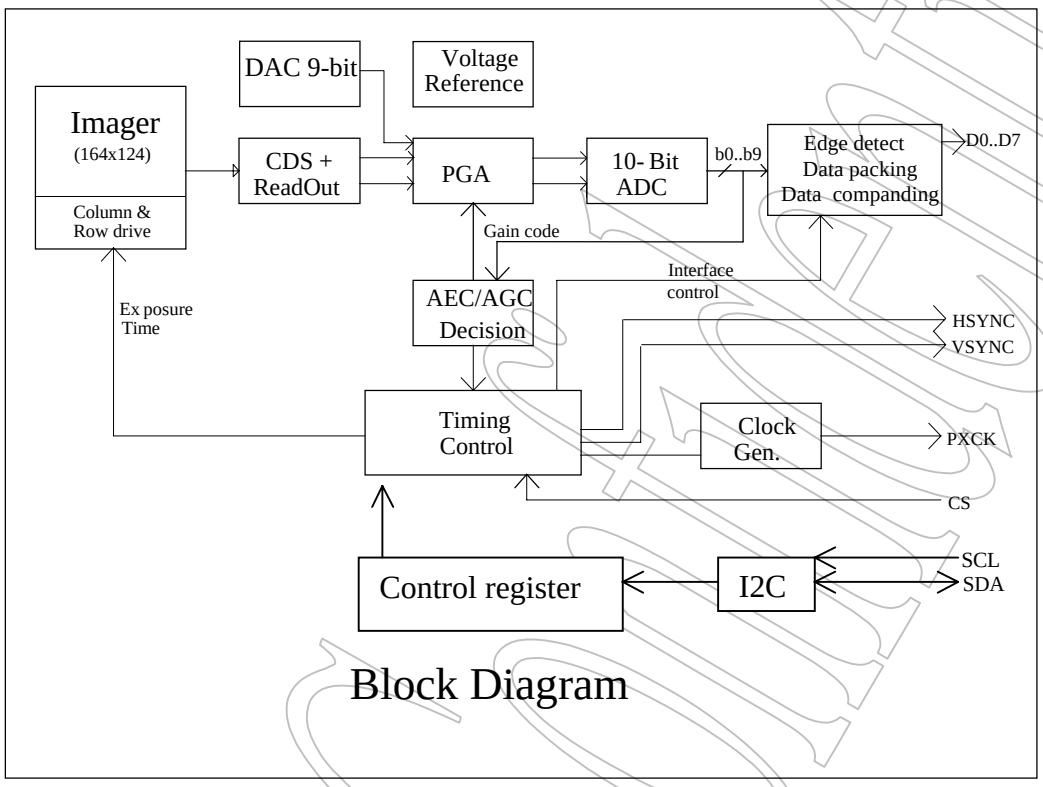


Fig 2.1 – Block diagram of PAS109

As the block diagram of PAS109 is shown in Figure 1. By pulling the CSB pin to low, the 164x124 sensor starts to produce a signal according to the amount of the light integrated in pixels. An entire raw data is then fed to a CDS readout array to reduce FPN noise and reset noise. A differential signal is then read out serially and fed to a programmable gain amplifier (PGA) followed by a 10-bit A/D converter.

Voltage reference block generates all necessary voltage and current for sensor array and analog circuit.

3. Pixel Array And Pixel Color Pattern

3.1. Pixel array and pixel color pattern

The output image format of PAS109B is QQVGA (164x124 pixel array). To provide the co-processor with the extra information it needs for interpolation at the edges of the pixel array, an border of 2 pixels on all 4 sides of the array are available. Fig 3.1. illustrates the pixel array and pixel color pattern.

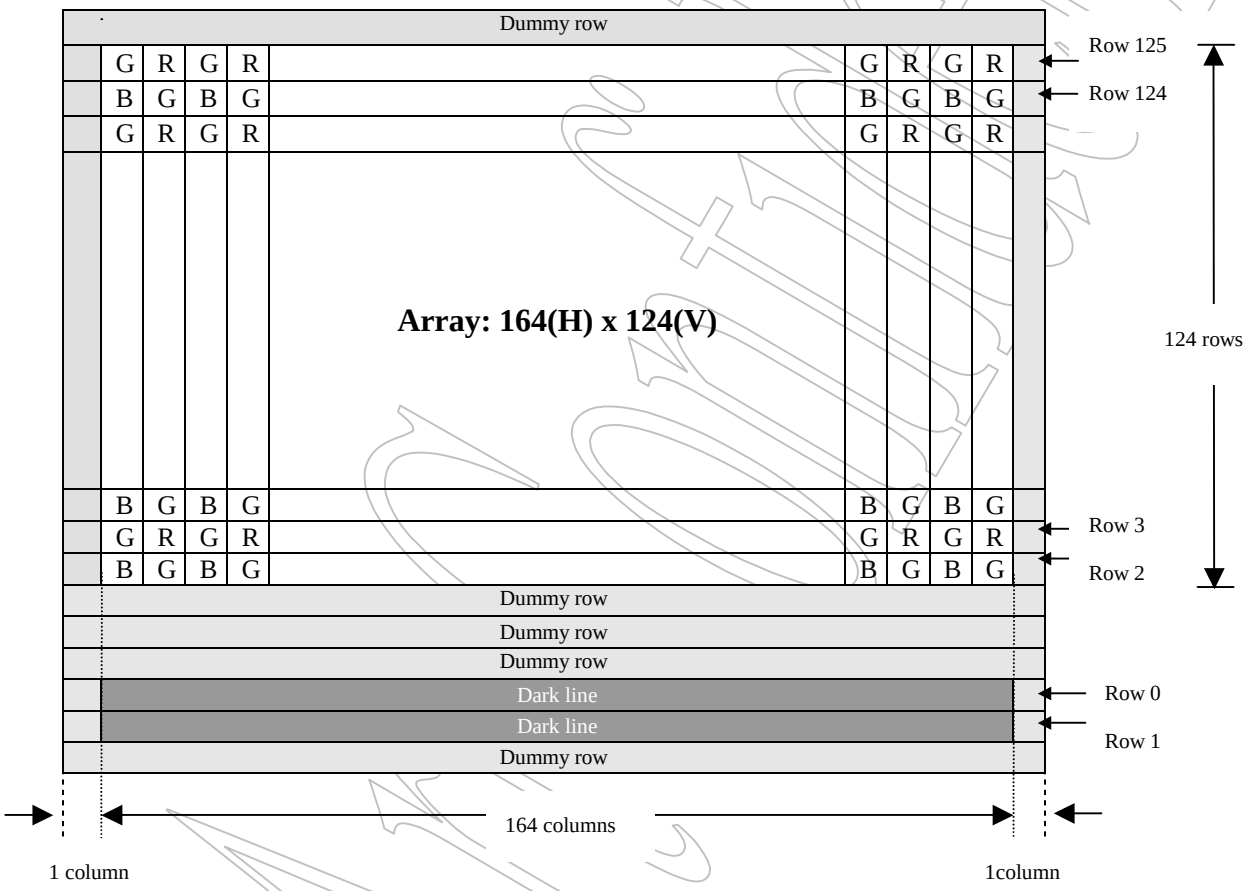


Fig 3.1. Pixel array and pixel color pattern

Note:

1. Pixel color pattern does not apply to monochrome sensor.
2. Pixel read-out proceeds from left to right, and from bottom row to top row.
3. Pixel array not drawn to scale.

4 Output timing:

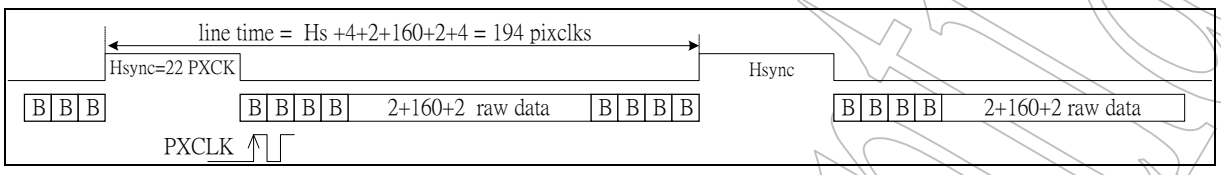


Fig. 4.1 Inter-line timing

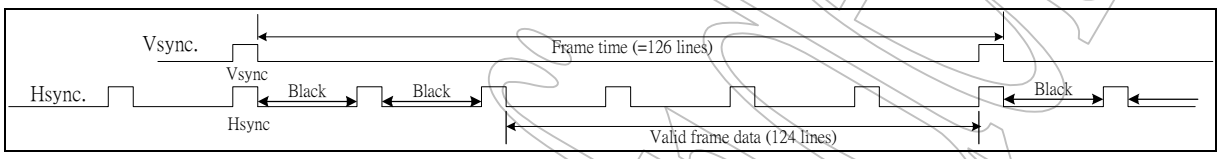


Fig. 4.2 Inter-frame timing (frame time=126 lines)

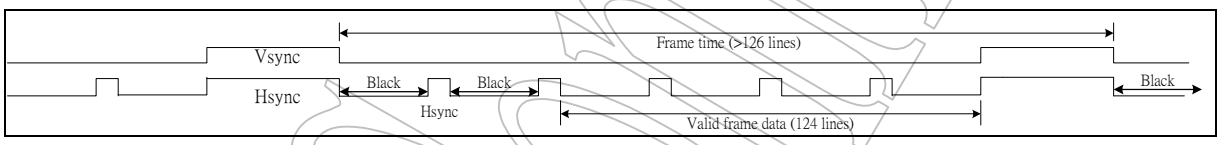


Fig. 4.3 Inter-frame timing(frame time>126 lines)

5. I²C Bus

PAS109B supports I2C-bus transfer protocol and is acting as slave device. The 7 bits unique slave address is 1000000 and supports receiving / transmitting speed up to 400kHz.

5.1 I²C bus overview

- Only two wires SDA (serial data) and SCL (serial clock) carry information between the devices connected to the I2C bus. Normally both SDA and SCL lines are open collector structure and pull high by external pull-up resistors.
- Only the master can initiates a transfer (start), generates clock signals, and terminates a transfer (stop).
- Start and stop condition: A high to low transition of the SDA line while SCL is high defines a start condition. A low to high transition of the SDA line while SCL is high defines a stop condition. Please refer to Fig 5.1.
- Valid data: The data on the SDA line must be stable during the high period of the SCL clock. Within each byte, MSB is always transferred first. Read/write control bit is the LSB of the first byte. Please refer to Fig 5.2.
- Both the master and slave can transmit and receive data from the bus.
- Acknowledge: The receiving device should pull down the SDA line during high period of the SCL clock line when a complete byte was transferred by transmitter. In the case of a master received data from a slave, the master does not generate an acknowledgment on the last byte to indicate the end of a master read cycle.

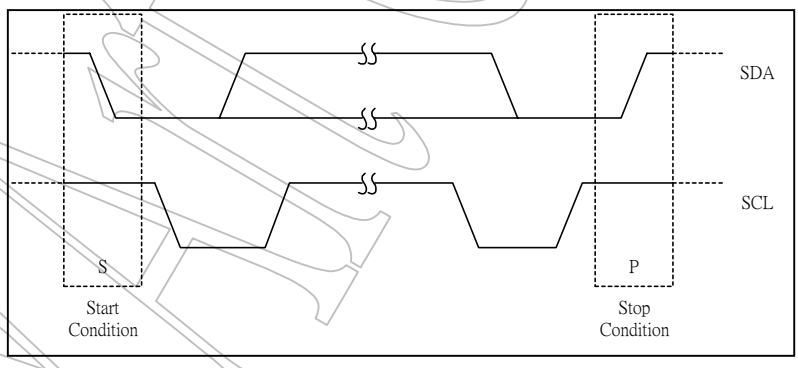


Fig 5.1 Start and Stop Conditions

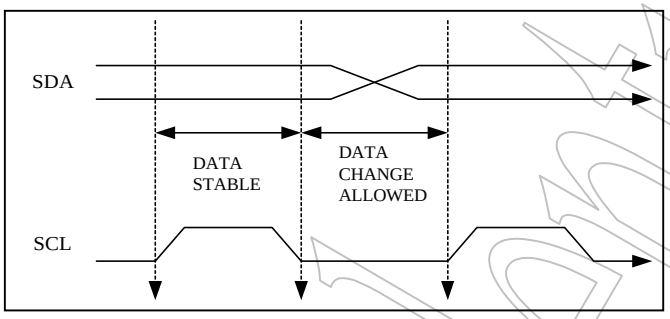
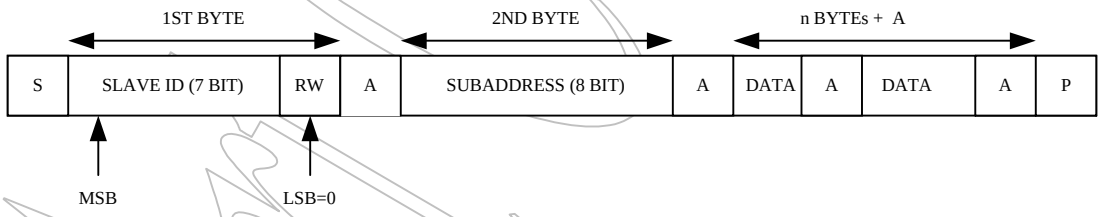


Fig 5.2 Valid Data

5.2 Data Transfer Format

5.2.1 Master transmits data to slave (write cycle)

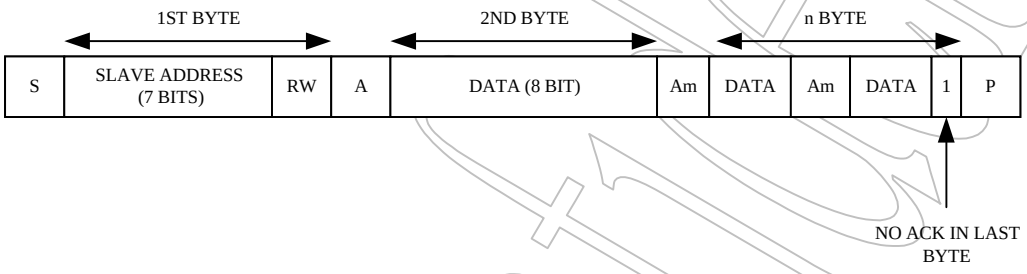
- S : Start
- A : Acknowledge by slave
- P : Stop
- RW : The LSB of 1ST byte to decide whether current cycle is read or write cycle.
  RW=1 read cycle, RW=0 write cycle.
- SUBADDRESS : The address values of PAS109B internal control registers
  (Please refer to PAS109B register description)



During write cycle, the master generates start condition and then places the 1st byte data that are combined slave address (7 bits) with a read/write control bit to SDA line. After slave(PAS109B) issues acknowledgment, the master places 2nd byte (sub-address) data on SDA line. Again follow the PAS109B acknowledgment, the master places the 8 bits data on SDA line and transmit to PAS109B control register (address was assigned by 2nd byte). After PAS109B issue acknowledgment, the master can generate a stop condition to end of this write cycle. In the condition of multi-byte write, the PAS109B sub-address is automatically increment after each DATA byte transferred. The data and A cycles is repeat until last byte write. Every control registers value inside PAS109B can be programming via this way. (Please refer to Fig 5.3.)

5.2.2 Slave transmits data to master (read cycle)

- The sub-address was taken from previous write cycle
- The sub-address is automatically increment after each byte read
- Am : Acknowledge by master
- Note there is no acknowledgment from master after last byte read



During read cycle, the master generates start condition and then place the 1st byte data that are combined slave address (7 bits) with a read/write control bit to SDA line. After issue acknowledgment, 8 bits DATA was also placed on SDA line by PAS109B. The 8 bit data was read from PAS109B internal control register that address was assigned by previous write cycle. Follow the master acknowledgment, the PAS109B place the next 8 bits data (address is increment automatically) on SDA line and then transmit to master serially. The DATA and Am cycles is repeat until the last byte read. After last byte read, Am is no longer generated by master but instead by keep SDA line high. The slave (PAS109B) must releases SDA line to master to generate STOP condition. (Please refer to Fig 5.3.)

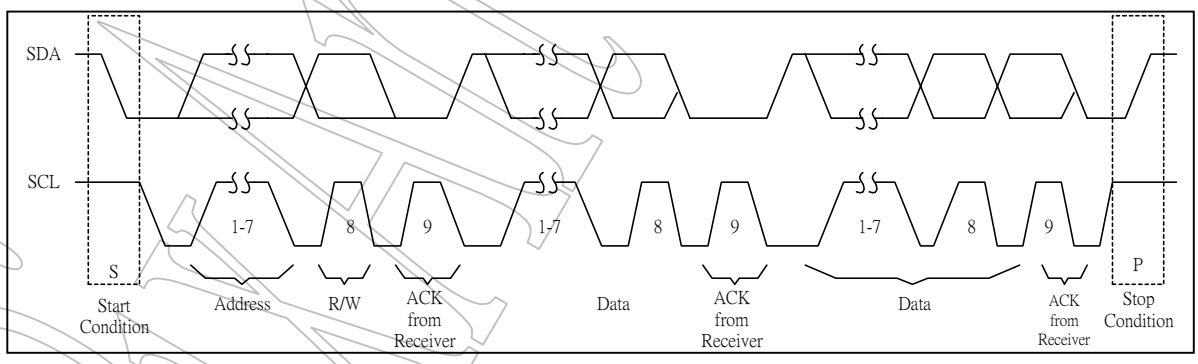


Fig 5.3 Data Transfer Format

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5.3 I²C Bus Timing

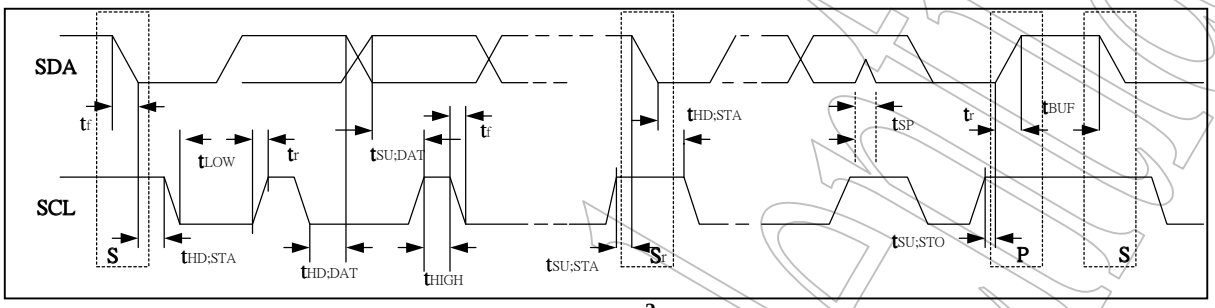

Fig 5.4 I²C Bus Timing

5.4 I²C Bus Timing Specification

PARAMETER	SYMBOL	STANDARD-MODE		UNIT
		MIN.	MAX.	
SCL clock frequency	f_{scl}	10	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{HD;STA}$	4.0	-	us
Low period of the SCL clock	t_{LOW}	4.7	-	us
HIGH period of the SCL clock	t_{HIGH}	0.75	-	us
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	-	us
Data hold time. For I2C-bus device	$t_{HD;DAT}$	0	3.45	us
Data set-up time	$t_{SU;DAT}$	250	-	ns
Rise time of both SDA and SCL signals	t_r	30	N.D.	ns(note1)
Fall time of both SDA and SCL signals	t_f	30	N.D.	ns(note1)
Set-up time for STOP condition	$t_{SU;STO}$	4.0	-	us
Bus free time between a STOP and START	t_{BUF}	4.7	-	us
Capacitive load for each bus line	C_b	1	15	pF
Noise margin at LOW level for each connected device (including hysteresis)	V_{nL}	0.1 V_{DD}	-	V
Noise margin at HIGH level for each connected device (including hysteresis)	V_{nH}	0.2 V_{DD}	-	V

Note: It depends on the "high" period time of SCL.

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6. Specifications

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
Vdd	DC supply voltage	-0.5	3.8	V
Vin	DC input voltage	0.5	Vdd+0.5	V
Vout	DC output voltage	-0.5	Vdd+0.5	V
Topt1	Operating temperature (chip functional)	-10	70	℃
Topt2	Operating temperature (guaranteed performance)	0	40	℃

DC Electrical Characteristics (VDD=3.0V±20%, Ta=10°C~40°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
Type :PWR					
VDD	Analog and digital operating voltage	2.4	3.0	3.6	V
IDD	Operating Current		8		mA
Istby	Standby current		100		uA
Type :IN & I/O Reset and SYSCLK					
VIH	Input voltage HIGH	2.0		VDD	V
VIL	Input voltage LOW	0		0.8	V
Cin	Input capacitor			10	pF
Ilkg	Input leakage current		TBD		uA
Type : OUT & I/O for PXD0:7, PXCK, H/VSYNC & SDA, load 10pf, 1.2kΩ, 3.0volts					
VOH	Output voltage HIGH	Vdd-0.2			V
VOL	Output voltage LOW			0.2	V

AC Operating Condition

Symbol	Parameter	Min.	Typ.	Max.	Unit
SYSCLK	Master clock frequency	4.5		48	MHz
PXCK	Pixel clock output frequency			1.5	MHz

Sensor Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Photo response non-uniformity	PRNU		1.18		%	
Saturation output voltage	Vsat.		1.35		V	
Dark output voltage	Vdark		35		mV/sec	
Dark signal non-uniformity	DSNU		2.52		%	
Sensitivity (Red channel)	R		2.0		V/Lux-sec	
Sensitivity (Green channel)	G		2.0		V/Lux-sec	
Sensitivity (Blue channel)	B		1.35		V/Lux-sec	

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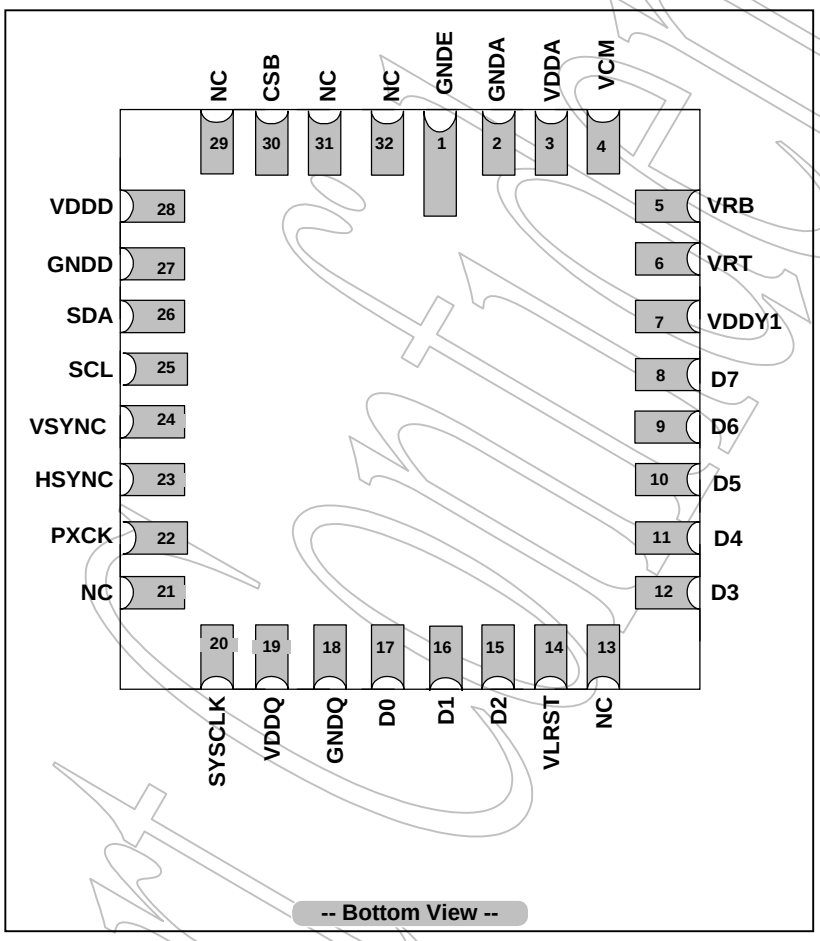
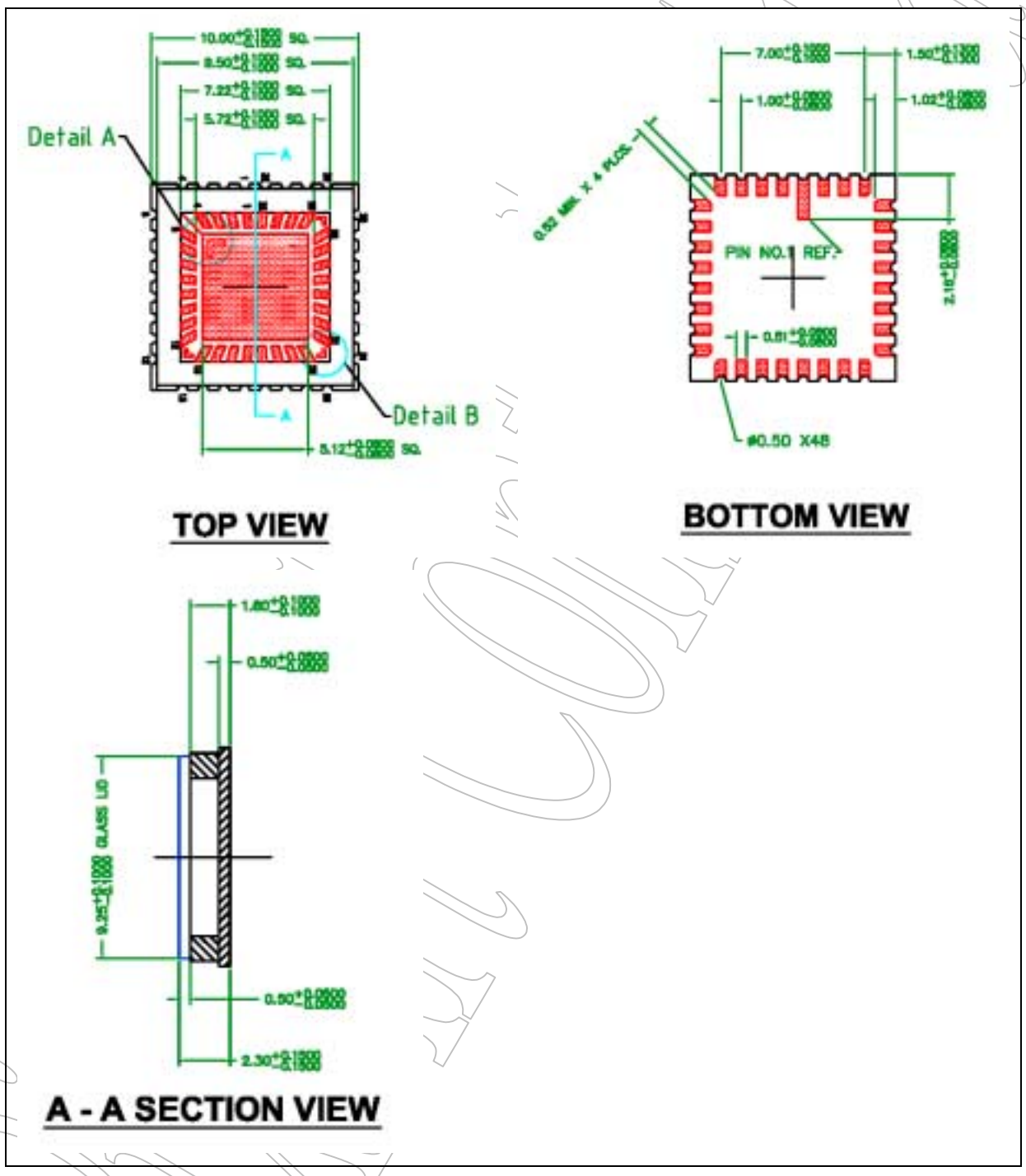
7. Package Information

7.1. 32-pin LCC

7.1.1. Pin Connection Diagram

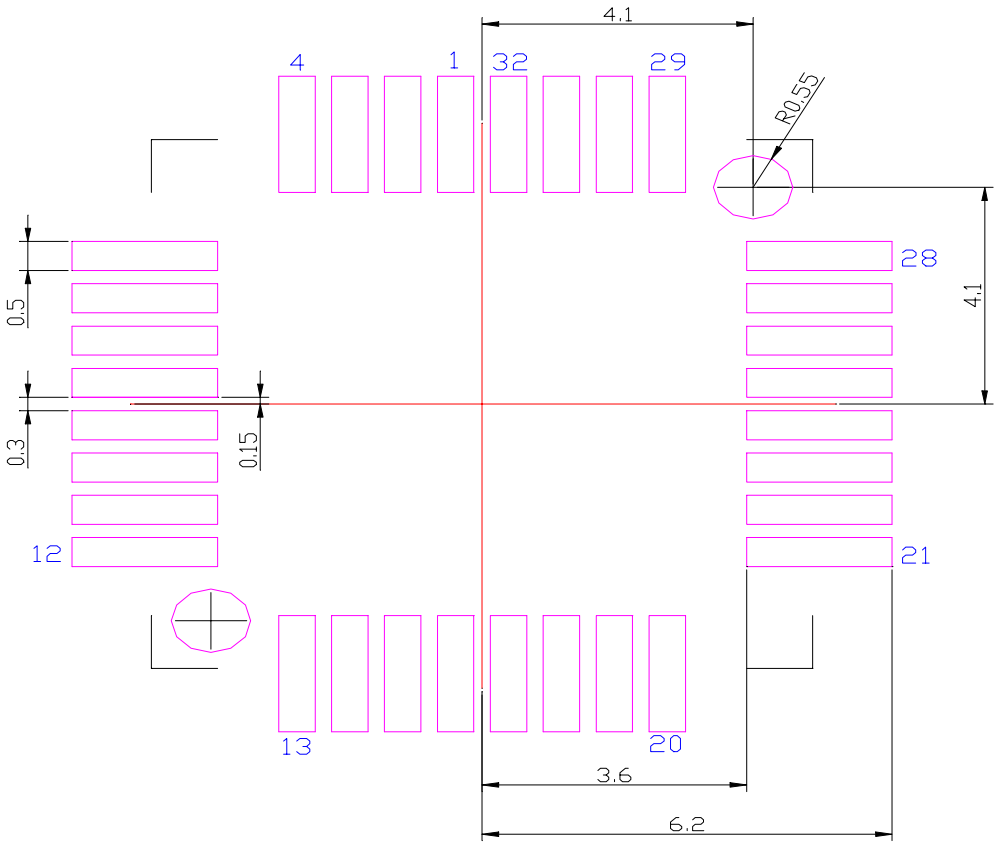


7.1.2. Package Outline



7.2. 32-pin LCC chip with lens package

7.2.1. Pin Connection Diagram



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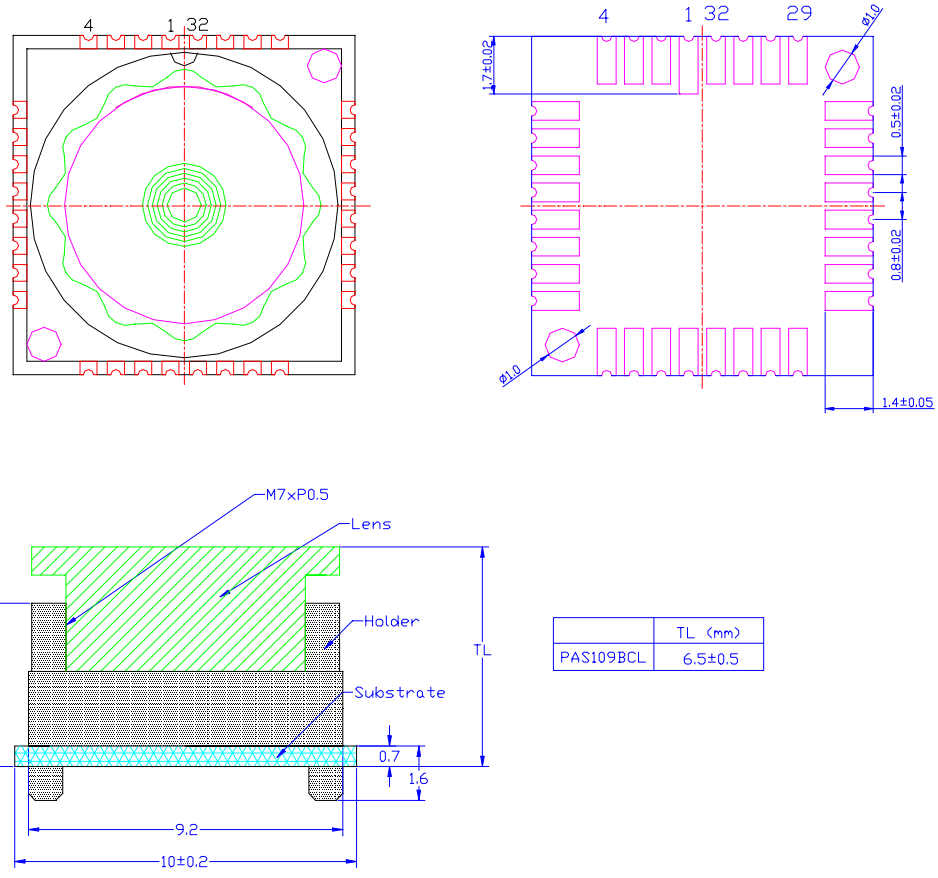
7.2.2. Lens Specification & Package Outline

Lens specification:

EFL	1.7mm
BFL	1.65mm
F no.	2.2
Diagonal Field of View	52°
Distortion	-3%
IR filter cutoff	648nm±10nm

Note: Customized lens is available upon request.

Package Outline:



	TL (mm)
PAS109BCL	6.5±0.5

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8. Ordering Information

Part Number	Color/Monochrome	Package
PAS109BCB-32	Color	32-pin LCC (plastic)
PAS109BBB-32	Monochrome	32-pin LCC (plastic)
PAS109BCL-32	Color	32-pin LCC chip with lens
PAS109BBL-32	Monochrome	32-pin LCC chip with lens

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