Features

- Operating Range from 5V to 27V
- Baud Rate up to 20 Kbaud
- Improved Slew Rate Control According to LIN Specification 2.0, 2.1 and SAEJ2602-2
- Fully Compatible with 3.3V and 5V Devices
- Dominant Time-out Function at Transmit Data (TXD)
- Normal and Sleep Mode
- Wake-up Capability via LIN Bus (90 µs Dominant)
- External Wake-up via WAKE Pin (35 µs Low Level)
- Control of External Voltage Regulator via INH Pin
- Very Low Standby Current During Sleep Mode (10 µA)
- Wake-up Source Recognition
- Bus Pin Short-circuit Protected versus GND and Battery
- LIN Input Current Typically 5 µA if V_{BAT} Is Disconnected
- Overtemperature Protection
- High EMC Level
- Interference and Damage Protection According to ISO/CD 7637
- ESD HBM 8 kV at LIN Bus Pin, Supply Pin VS and WAKE Pin According to STM5.1

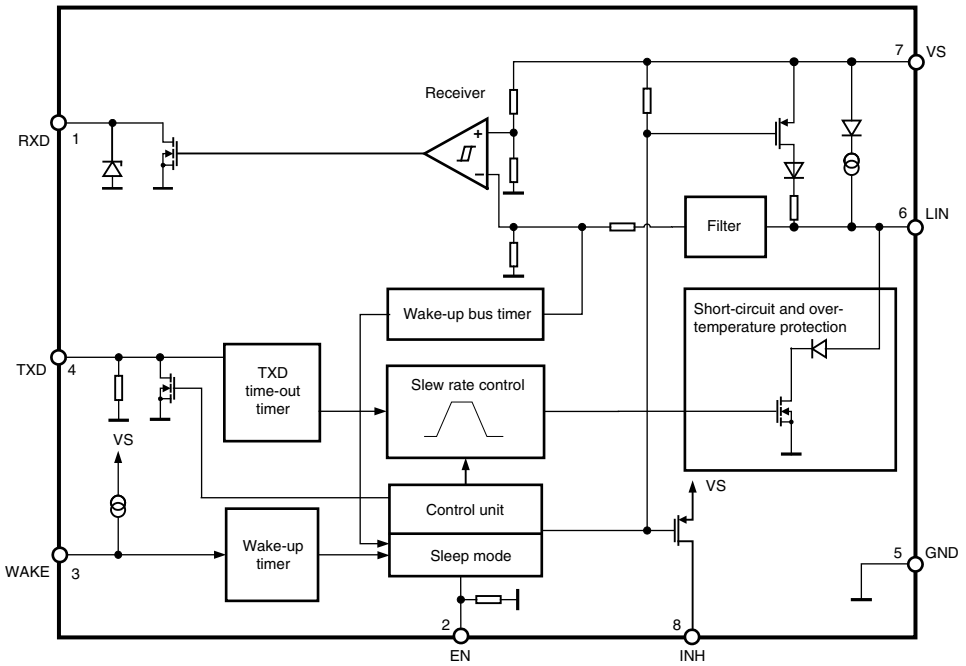
LIN Transceiver

ATA6662

1. Description

The ATA6662 is a fully integrated LIN transceiver complying with the LIN specification 2.0, 2.1 and SAEJ2602-2. It interfaces the LIN protocol handler and the physical layer. The device is designed to handle the low-speed data communication in vehicles, for example, in convenience electronics. Improved slope control at the LIN bus ensures secure data communication up to 20 Kbaud with an RC oscillator for protocol handling. Sleep Mode guarantees minimal current consumption. The ATA6662 has advanced EMI and ESD performance.

Figure 1-1. Block Diagram



4916M–AUTO–09/09

2. Pin Configuration

Figure 2-1. Pinning SO8

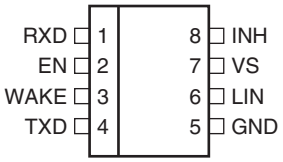


Table 2-1. Pin Description

Pin	Symbol	Function
1	RXD	Receive data output (open drain)
2	EN	Enables Normal Mode; when the input is open or low, the device is in Sleep Mode
3	WAKE	High voltage input for local wake-up request
4	TXD	Transmit data input; active low output (strong pull-down) after a local wake-up request
5	GND	Ground, heat sink
6	LIN	LIN bus line input/output
7	VS	Battery supply
8	INH	Battery-related inhibit output for controlling an external voltage regulator; active high after a wake-up request

3. Functional Description

3.1 Physical Layer Compatibility

Since the LIN physical layer is independent from higher LIN layers (e.g., the LIN protocol layer), all nodes with a LIN physical layer according to revision 2.x can be mixed with LIN physical layer nodes, which, according to older versions (i.e., LIN 1.0, LIN 1.1, LIN 1.2, LIN 1.3), are without any restrictions.

3.2 Supply Pin (V_S)

Undervoltage detection is implemented to disable transmission if V_S falls to a value below 5V in order to avoid false bus messages. After switching on V_S, the IC switches to Fail-safe Mode and INHIBIT is switched on. The supply current in Sleep Mode is typically 10 µA.

3.3 Ground Pin (GND)

The ATA6662 is neutral on the LIN pin in the case of a GND disconnection. It is able to handle a ground shift up to 11.5% of V_S.

3.4 Bus Pin (LIN)

A low-side driver with internal current limitation and thermal shutdown and an internal pull-up resistor are implemented as specified for LIN 2.x. The voltage range is from –27V to +40V. This pin exhibits no reverse current from the LIN bus to V_S, even in the case of a GND shift or V_{Batt} disconnection. The LIN receiver thresholds are compatible to the LIN protocol specification.The fall time (from recessive to dominant) and the rise time (from dominant to recessive) are slope controlled. The output has a self-adapting short circuit limitation; that is, during current limitation, as the chip temperature increases, the current is reduced.

3.5 Input Pin (TXD)

This pin is the microcontroller interface to control the state of the LIN output. TXD is low to bring LIN low. If TXD is high, the LIN output transistor is turned off. Then, the bus is in Recessive Mode via the internal pull-up resistor. The TXD pin is compatible to both a 3.3V or 5V supply.

3.6 TXD Dominant Time-out Function

The TXD input has an internal pull-down resistor. An internal timer prevents the bus line from being driven permanently in dominant state. If TXD is forced low longer than t_{dom} > 6 ms, the pin LIN will be switched off (Recessive Mode). To reset this mode, switch TXD to high (> 10 µs) before switching LIN to dominant again.

3.7 Output Pin (RXD)

This pin reports to the microcontroller the state of the LIN bus. LIN high (recessive) is reported by a high level at RXD, LIN low (dominant) is reported by a low voltage at RXD. The output is an open drain, therefore, it is compatible to a 3.3V or 5V power supply. The AC characteristics are defined with a pull-up resistor of 5 kΩto 5V and a load capacitor of 20 pF. The output is short-current protected. In Unpowered Mode (V_S = 0V), RXD is switched off. For ESD protection a Zener diode is integrated, with V_Z = 6.1V.

3.8 Enable Input Pin (EN)

This pin controls the Operation Mode of the interface. If EN = 1, the interface is in Normal Mode, with the transmission path from TXD to LIN and from LIN to RXD both active. At a falling edge on EN, while TXD is already set to high, the device is switched to Sleep Mode and no transmission is possible. In Sleep Mode, the LIN bus pin is connected to V_S with a weak pull-up current source. The device can transmit only after being woken up (see Section 3.9, "Inhibit Output Pin (INH)").

During Sleep Mode the device is still supplied from the battery voltage. The supply current is typically 10 µA. The pin EN provides a pull-down resistor in order to force the transceiver into Sleep Mode in case the pin is disconnected.

3.9 Inhibit Output Pin (INH)

This pin is used to control an external switchable voltage regulator having a wake-up input. The inhibit pin provides an internal switch towards pin V_S. If the device is in Normal Mode, the inhibit high-side switch is turned on and the external voltage regulator is activated. When the device is in Sleep Mode, the inhibit switch is turned off and disables the voltage regulator.

A wake-up event on the LIN bus or at pin WAKE will switch the INH pin to the V_S level. After a system power-up (V_S rises from zero), the pin INH switches automatically to the V_S level.

3.10 Wake-up Input Pin (WAKE)

This pin is a high-voltage input used to wake the device up from Sleep Mode. It is usually connected to an external switch in the application to generate a local wake-up. If you do not need a local wake-up in your application, connect pin WAKE directly to pin VS. A pull-up current source with typically –10 µA is implemented. The voltage threshold for a wake-up signal is 3V below the VS voltage with an output current of typically –3 µA.

Wake-up events from Sleep Mode:

- LIN bus
- EN pin
- WAKE pin

Figure 3-1 on page 6, Figure 3-2 on page 7 and Figure 3-3 on page 7 show details of wake-up operations.

3.11 Operation Modes

1. Normal Mode
   This is the normal transmitting and Receiving Mode. All features are available.
2. Sleep Mode
   In this mode the transmission path is disabled and the device is in low power mode. Supply current from V_{Batt} is typically 10 µA. A wake-up signal from the LIN bus or via pin WAKE will be detected and will switch the device to Fail-safe Mode. If EN then switches to high, Normal Mode is activated. Input debounce timers at pin WAKE (t_{WAKE}), LIN (t_{BUS}) and EN (t_{sleep},t_{nom}) prevent unwanted wake-up events due to automotive transients or EMI. In Sleep Mode the INH pin is left floating. The internal termination between pin LIN and pin V_S is disabled. Only a weak pull-up current (typical 10 µA) between pin LIN and pin V_S is present. The Sleep Mode can be activated independently from the actual level on pin LIN or WAKE.
3. Fail-safe Mode
   At system power-up or after a wake-up event, the device automatically switches to Fail-safe Mode. It switches the INH pin to a high state, to the V_S level. LIN communication is switched off. The microcontroller of the application will then confirm the Normal Mode by setting the EN pin to high.
4. Unpowered Mode
   If you connect battery voltage to the application circuit, the voltage at the VS pin increases according to the block capacitor. After VS is higher than the VS undervoltage threshold VS_{th}, the IC mode changes from Unpowered Mode to Fail-safe Mode.

3.12 Remote Wake-up via Dominant Bus State

A voltage less than the LIN pre-wake detection V_{LINL} at pin LIN activates the internal LIN receiver and switches on the internal slave termination between the LIN pin and the VS pin.

A falling edge at pin LIN, followed by a dominant bus level V_{BUSdom} maintained for a certain time period (t_{BUS}) and a rising edge at pin LIN results in a remote wake-up request. The device switches to Fail-safe Mode. Pin INH is activated (switches to V_S) and the internal termination resistor is switched on. The remote wake-up request is indicated by a low level at pin RXD to interrupt the microcontroller (see Figure 3-2 on page 7).

3.13 Local Wake-up via Pin WAKE

A falling edge at pin WAKE, followed by a low level maintained for a certain time period (t_{WAKE}), results in a local wake-up request. The wake-up time (t_{WAKE}) ensures that no transient, according to ISO7637, creates a wake-up. The device switches to Fail-safe Mode. Pin INH is activated (switches to V_S) and the internal termination resistor is switched on. The local wake-up request is indicated by a low level at pin RXD to interrupt the microcontroller and a strong pull-down at pin TXD (see Figure 3-3 on page 7). The voltage threshold for a wake-up signal is 3V below the VS voltage with an output current of typical –3 µA. Even in the case of a continuous low at pin WAKE it is possible to switch the IC into Sleep Mode via a low at pin EN. The IC will stay in Sleep Mode for an unlimited time. To generate a new wake up at pin WAKE it needs first a high signal > 6 µs before a negative edge starts the wake-up filtering time again.

3.14 Wake-up Source Recognition

The device can distinguish between a local wake-up request (pin WAKE) and a remote wake-up request (LIN bus). The wake-up source can be read on pin TXD in Fail-safe Mode. If an external pull-up resistor (typically 5 kΩ) has been added on pin TXD to the power supply of the microcontroller, a high level indicates a remote wake-up request (weak pull-down at pin TXD) and a low level indicates a local wake-up request (strong pull-down at pin TXD).

The wake-up request flag (signalled on pin RXD) as well as the wake-up source flag (signalled on pin TXD) are reset immediately if the microcontroller sets pin EN to high (see Figure 3-2 on page 7 and Figure 3-3 on page 7).

Figure 3-1. Mode of Operation

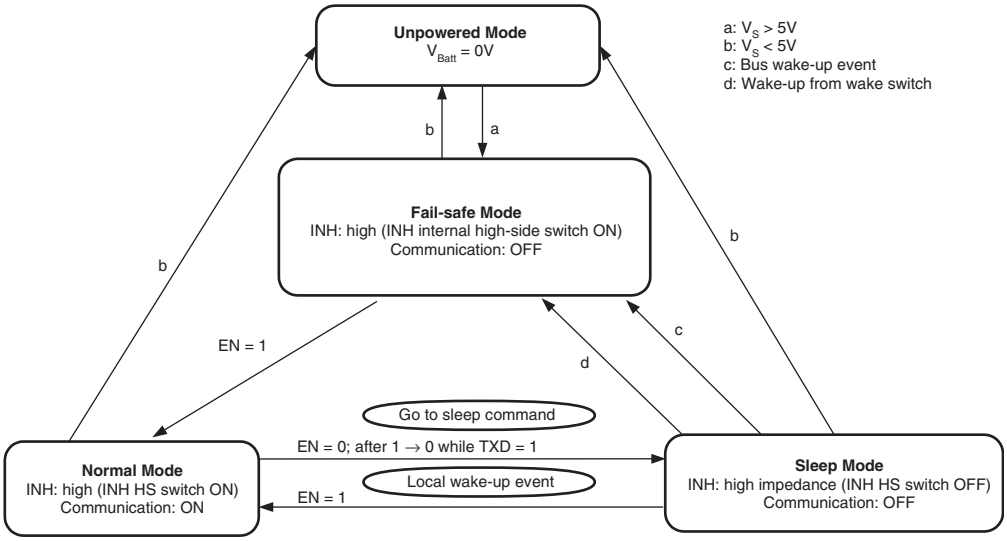


Table 3-1. Table of Modes

Mode of Operation	Transceiver	INH	RXD	LIN
Fail-safe	Off	On	High, except after wake up	Recessive
Normal	On	On	LIN depending	TXD depending
Sleep	Off	Off	High ohmic	Recessive

3.15 Fail-safe Features

- The reverse current is < 2 µA at pin LIN during loss of V_{BAT}; this is optimal behavior for bus systems where some slave nodes are supplied from battery or ignition.
- Pin EN provides a pull-down resistor to force the transceiver into Sleep Mode if EN is disconnected.
- Pin RXD is set floating if V_{BAT} is disconnected.
- Pin TXD provides a pull-down resistor to provide a static low if TXD is disconnected.
- The LIN output driver has a current limitation, and if the junction temperature T_j exceeds the thermal shut-down temperature T_{off}, the output driver switches off.
- The implemented hysteresis, T_{hys}, enables the LIN output again after the temperature has been decreased.

Figure 3-2. LIN Wake-up Waveform Diagram

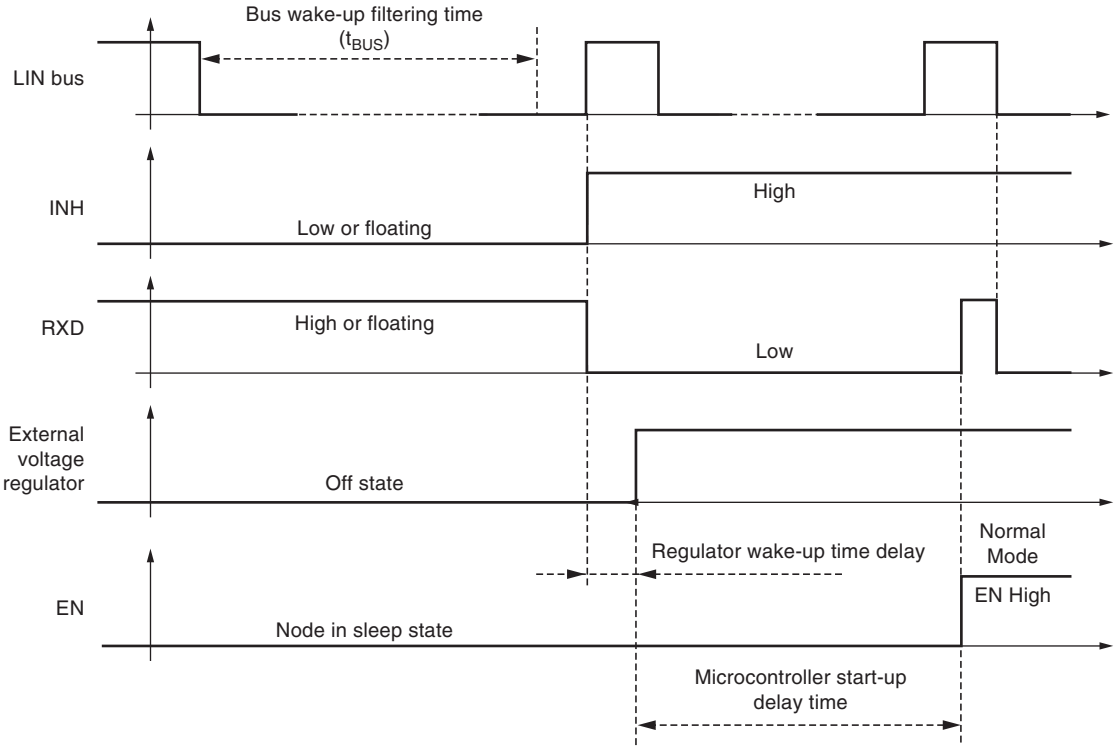
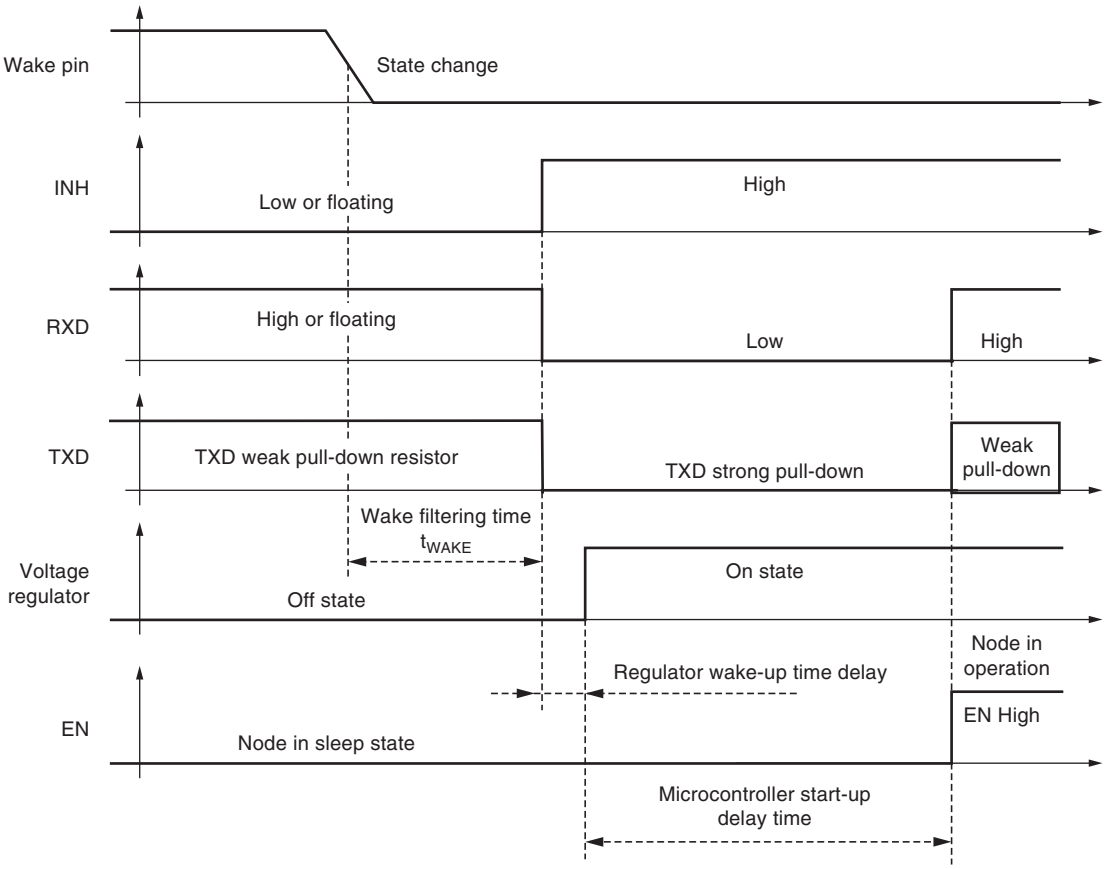


Figure 3-3. Wake-up from Wake-up Switch



4. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Typ.	Max.	Unit
V_S - Continuous supply voltage		–0.3		+40	V
Wake DC and transient voltage (with 33-kΩ serial resistor) - Transient voltage due to ISO7637 (coupling 1 nF)		–1 –150		+40 +100	V V
Logic pins (RXD, TXD, EN)		–0.3		+5.5	V
LIN - DC voltage - Transient voltage due to ISO7637 (coupling 1 nF)		 –27 –150		 +40 +100	 V V
INH - DC voltage		–0.3		V_S + 0.3	V
ESD according to IBEE LIN EMC Test specification 1.0 following IEC 61000-4-2 - Pin VS, LIN to GND - Pin WAKE (33 kΩ serial resistor)		 ±6 ±5			 KV KV
ESD HBM following STM5.1 with 1.5 kΩ/100 pF - Pin VS, LIN, WAKE to GND - Pin INH to GND		 ±8 ±6			 KV KV
HBM ESD ANSI/ESD-STM5.1 JESD22-A114 AEC-Q100 (002)		±3			KV
CDM ESD STM 5.3.1		±750			V
Machine Model ESD AEC-Q100-RevF(003)		±100			V
Junction temperature	T_j	–40		+150	°C
Storage temperature	T_{stg}	–55		+150	°C

5. Thermal Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance junction ambient	R_{thJA}			145	K/W
Special heat sink at GND (pin 5) on PCB (fused lead frame to pin 5)	R_{thJA}		80		K/W
Thermal shutdown	T_{off}	150	165	180	°C
Thermal shutdown hysteresis	T_{hys}	5	10	20	°C

6. Electrical Characteristics

5V < V_S < 27V, T_j = –40°C to +150°C

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	**V_S Pin**								
1.1	DC voltage range nominal		7	V_S	5	13.5	27	V	A
1.2	Supply current in Sleep Mode	Sleep Mode $V_{lin} > V_S - 0.5V$ V_S < 14V	7	$I_{VSsleep}$		10	20	µA	A
1.3	Supply current in Normal Mode	Bus recessive V_S < 14V	7	I_{VSrec}		0.9	1.3	mA	A
1.4		Bus dominant V_S < 14V Total bus load > 500Ω	7	I_{VSdom}		1.2	2	mA	A
1.5	Supply current in Fail-safe Mode	Bus recessive V_S < 14V	7	I_{VSfail}	0.5		1.1	mA	A
1.6	V_S undervoltage threshold on			V_{Sth}	4		4.95	V	A
1.7	V_S undervoltage threshold off			V_{Sth}	4.05		5	V	A
1.8	V_S undervoltage threshold hysteresis		7	V_{Sth_hys}	50		500	mV	A
2	**RXD Output Pin (Open Drain)**								
2.1	Low-level output sink current	Normal Mode V_{LIN} = 0V, V_{RXD} = 0.4V	1	I_{RXDL}	1.3	2.5	8	mA	A
2.2	RXD saturation voltage	5-kΩ pull-up resistor to 5V	1	$Vsat_{RXD}$			0.4	V	A
2.3	High-level leakage current	Normal Mode $V_{LIN} = V_{BAT}$, V_{RXD} = 5V	1	I_{RXDH}	–3		+3	µA	A
2.4	ESD zener diode	I_{RXD} = 100 µA	1	VZ_{RXD}	5.8		8.6	V	A
3	**TXD Input Pin**								
3.1	Low-level voltage input		4	V_{TXDL}	–0.3		+0.8	V	A
3.2	High-level voltage input		4	V_{TXDH}	2		5.5	V	A
3.3	Pull-down resistor	V_{TXD} = 5V	4	R_{TXD}	125	250	600	kΩ	A
3.4	Low-level leakage current	V_{TXD} = 0V	4	I_{TXD_leak}	–3		+3	µA	A
3.5	Low-level output sink current	Fail-safe Mode, local wake up V_{TXD} = 0.4V $V_{LIN} = V_{BAT}$	4	I_{TXD}	1.3	2.5	8	mA	A
4	**EN Input Pin**								
4.1	Low-level voltage input		2	V_{ENL}	–0.3		+0.8	V	A
4.2	High-level voltage input		2	V_{ENH}	2		5.5	V	A
4.3	Pull-down resistor	V_{EN} = 5V	2	R_{EN}	125	250	600	kΩ	A
4.4	Low-level input current	V_{EN} = 0V	2	I_{EN}	–3		+3	µA	A
5	**INH Output Pin**								
5.1	High-level voltage	Normal Mode I_{INH} = –2 mA	8	V_{INHH}	V_S – 3		V_S	V	A
5.2	Leakage current	Sleep Mode V_{INH} = 0V/27V, V_S = 27V	8	I_{INHL}	–3		+3	µA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

6. Electrical Characteristics (Continued)

5V < V_S < 27V, T_j = –40°C to +150°C

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
6	**WAKE Pin**								
6.1	High-level input voltage		3	V_{WAKEH}	V_S – 1V		V_S + 0.3V	V	A
6.2	Low-level input voltage	I_{WAKE} = Typically –3 µA	3	V_{WAKEL}	–1V		V_S – 3.3V	V	A
6.3	Wake pull-up current	V_S < 27V	3	I_{WAKE}	–30	–10		µA	A
6.4	High-level leakage current	V_S = 27V, V_{WAKE} = 27V	3	I_{WAKE}	–5		+5	µA	A
7	**LIN Bus Driver**								
7.1	Driver recessive output voltage	R_{LOAD} = 500Ω / 1 kΩ	6	V_{BUSrec}	0.9 × V_S		V_S	V	A
7.2	Driver dominant voltage $V_{BUSdom\_DRV\_LoSUP}$	V_{VS} = 7V, R_{load} = 500Ω	6	$V_{\_LoSUP}$			1.2	V	A
7.3	Driver dominant voltage $V_{BUSdom\_DRV\_HiSUP}$	V_{VS} = 18V, R_{load} = 500Ω	6	$V_{\_HiSUP}$			2	V	A
7.4	Driver dominant voltage $V_{BUSdom\_DRV\_LoSUP}$	V_{VS} = 7V, R_{load} = 1000Ω	6	$V_{\_LoSUP\_1k}$	0.6			V	A
7.5	Driver dominant voltage $V_{BUSdom\_DRV\_HiSUP}$	V_{VS} = 18V, R_{load} = 1000Ω	6	$V_{\_HiSUP\_1k\_}$	0.8			V	A
7.6	Pull-up resistor to V_S	The serial diode is mandatory	6	R_{LIN}	20	30	60	kΩ	A
7.7	Voltage drop at the serial diodes	In pull-up path with R_{slave} $I_{SerDiode}$ = 10 mA	6	$V_{SerDiode}$	0.4		1.0	V	D
7.8	LIN current limitation V_{BUS} = V_{BAT_max}		6	I_{BUS_LIM}	40	120	200	mA	A
7.9	Input leakage current at the receiver, including pull-up resistor as specified	Input leakage current Driver off V_{BUS} = 0V, V_S = 12V	6	$I_{BUS\_PAS\_dom}$	–1			mA	A
7.10	Leakage current LIN recessive	Driver off 8V < V_{BAT} < 18V 8V < V_{BUS} < 18V $V_{BUS} \geq V_{BAT}$	6	$I_{BUS\_PAS\_rec}$		10	20	µA	A
7.11	Leakage current at ground loss; Control unit disconnected from ground; Loss of local ground must not affected communication in the residual network	GND_{Device} = V_S V_{BAT} =12V 0V < V_{BUS} < 18V	6	$I_{BUS\_NO\_gnd}$	–10	+0.5	+10	µA	A
7.12	Leakage current at loss of battery; Node has to substain the current that can flow under this condition; Bus must remain operational under this condition	V_{BAT} disconnected V_{SUP_Device} = GND 0V < V_{BUS} < 18V	6	$I_{BUS\_NO\_bat}$		0.1	2	µA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

6. Electrical Characteristics (Continued)

5V < V_S < 27V, T_j = –40°C to +150°C

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
8	**LIN Bus Receiver**								
8.1	Center of receiver threshold	V_{BUS_CNT} = (V_{th_dom} + V_{th_rec}) / 2	6	V_{BUS_CNT}	0.475 × V_S	0.5 × V_S	0.525 × V_S	V	A
8.2	Receiver dominant state	V_{EN} = 5V	6	V_{BUSdom}	–27		0.4 × V_S	V	A
8.3	Receiver recessive state	V_{EN} = 5V	6	V_{BUSrec}	0.6 × V_S		40	V	A
8.4	Receiver input hysteresis	V_{HYS} = V_{th_rec} – V_{th_dom}	6	V_{BUShys}	0.028 × V_S	0.1 × V_S	0.175 × V_S	V	A
8.5	Pre-wake detection LIN High-level input voltage		6	V_{LINH}	V_S – 2V		V_S + 0.3V	V	A
8.6	Pre-wake detection LIN Low-level input voltage	Switches the LIN receiver on	6	V_{LINL}	–27V		V_S – 3.3V	V	A
9	**Internal Timers**								
9.1	Dominant time for wake-up via LIN bus	V_{LIN} = 0V	6	t_{BUS}	30	90	150	µs	A
9.2	Time of low pulse for wake-up via pin WAKE	V_{WAKE} = 0V	3	t_{WAKE}	7	35	50	µs	A
9.3	Time delay for mode change from Fail-safe Mode to Normal Mode via pin EN	V_{EN} = 5V	2	t_{norm}	2	7	15	µs	A
9.4	Time delay for mode change from Normal Mode into Sleep Mode via pin EN	V_{EN} = 0V	2	t_{sleep}	2	7	12	µs	A
9.5	TXD dominant time out time	V_{TXD} = 0V	4	t_{dom}	6	9	20	ms	A
9.6	Power-up delay between V_S = 5V until INH switches to high	V_{VS} = 5V		t_{VS}			200	µs	A
10	**LIN Bus Driver AC Parameter with Different Bus Loads** Load 1 (small): 1 nF, 1 kΩ; Load 2 (large): 10 nF, 500Ω; R_{RXD} = 5 kΩ; C_{RXD} = 20 pF; Load 3 (medium): 6.8 nF, 660Ω characterized on samples; 10.1 and 10.2 specifies the timing parameters for proper operation at 20 Kbit/s, 10.3 and 10.4 at 10.4 Kbit/s.								
10.1	Duty cycle 1	$TH_{Rec(max)}$ = 0.744 × V_S $TH_{Dom(max)}$ = 0.581 × V_S V_S = 7.0V to 18V t_{Bit} = 50 µs D1 = $t_{bus\_rec(min)}$ / (2 × t_{Bit})	6	D1	0.396				A
10.2	Duty cycle 2	$TH_{Rec(min)}$ = 0.422 × V_S $TH_{Dom(min)}$ = 0.284 × V_S V_S = 7.0V to 18V t_{Bit} = 50 µs D2 = $t_{bus\_rec(max)}$ / (2 × t_{Bit})	6	D2			0.581		A
10.3	Duty cycle 3	$TH_{Rec(max)}$ = 0.778 × V_S $TH_{Dom(max)}$ = 0.616 × V_S V_S = 7.0V to 18V t_{Bit} = 96 µs D3 = $t_{bus\_rec(min)}$ / (2 × t_{Bit})	6	D3	0.417				A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

6. Electrical Characteristics (Continued)

5V < V_S < 27V, T_j = –40°C to +150°C

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
10.4	Duty cycle 4	$TH_{Rec(min)} = 0.389 \times V_S$ $TH_{Dom(min)} = 0.251 \times V_S$ V_S = 7.0V to 18V t_{Bit} = 96 µs D4 = $t_{bus\_rec(max)}$ / (2 × t_{Bit})	6	D4			0.590		A
11	**Receiver Electrical AC Parameters of the LIN Physical Layer** LIN receiver, RXD load conditions: C_{RXD} = 20 pF, $R_{pull-up}$ = 5 kΩ								
11.1	Propagation delay of receiver (see Figure 6-1 on page 13)	$t_{rec\_pd} = max(t_{rx\_pdr}, t_{rx\_pdf})$ V_S = 7.0V to 18V	1	t_{rx_pd}			6	µs	A
11.2	Symmetry of receiver propagation delay rising edge minus falling edge	$t_{rx\_sym} = t_{rx\_pdr} – t_{rx\_pdf}$ V_S = 7.0V to 18V	1	t_{rx_sym}	–2		+2	µs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Figure 6-1. Definition of Bus Timing Parameter

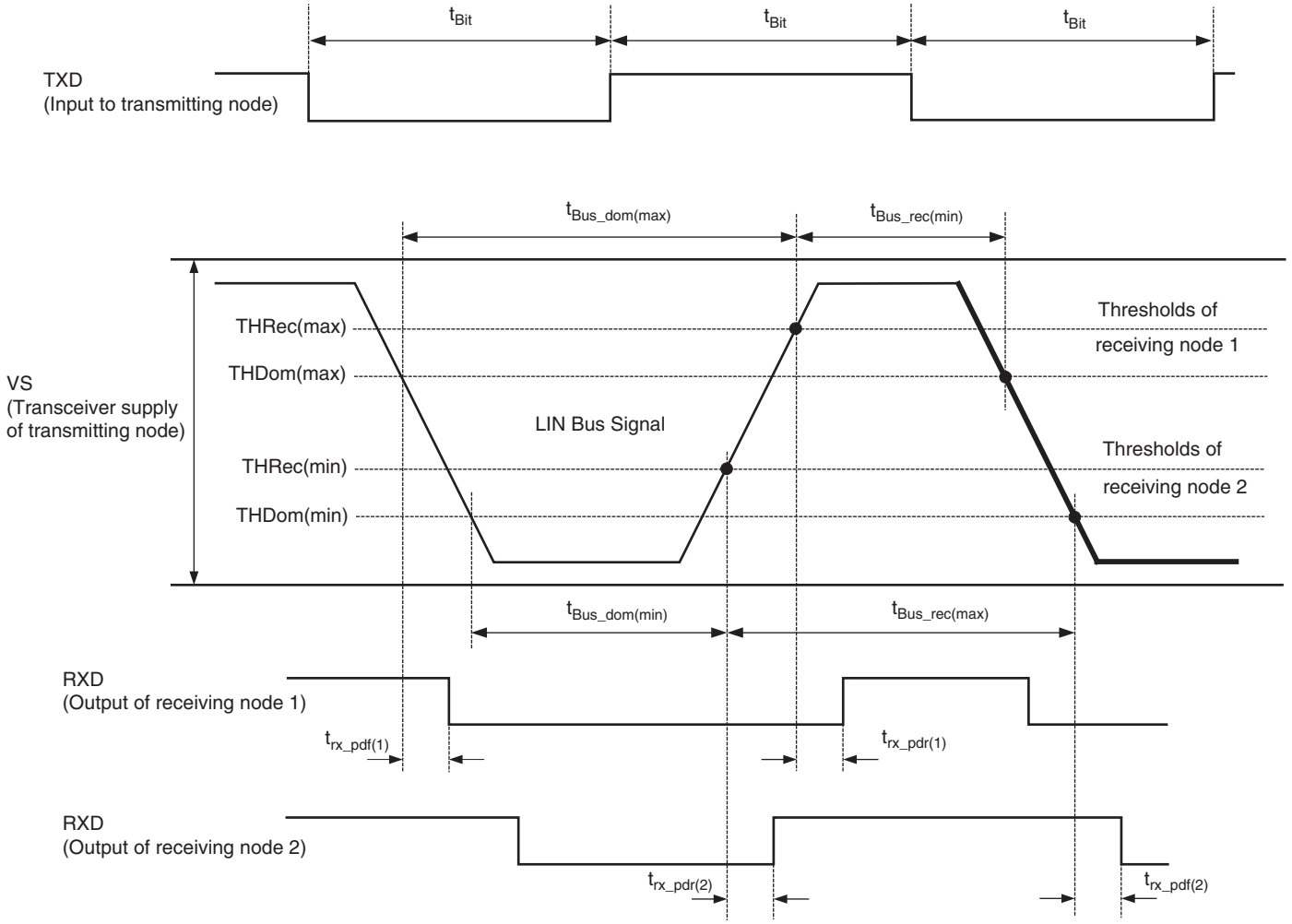
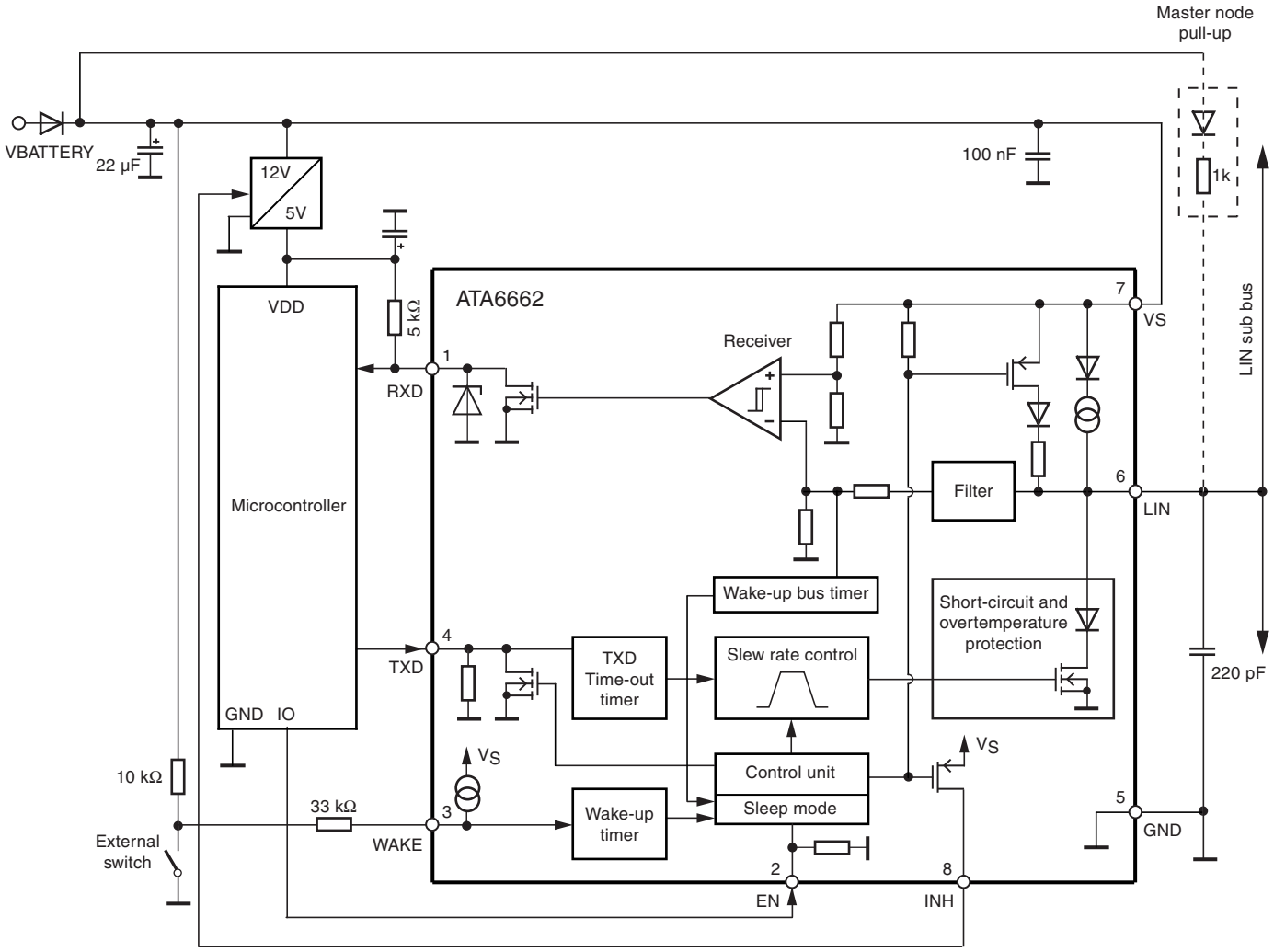


Figure 6-2. Application Circuit



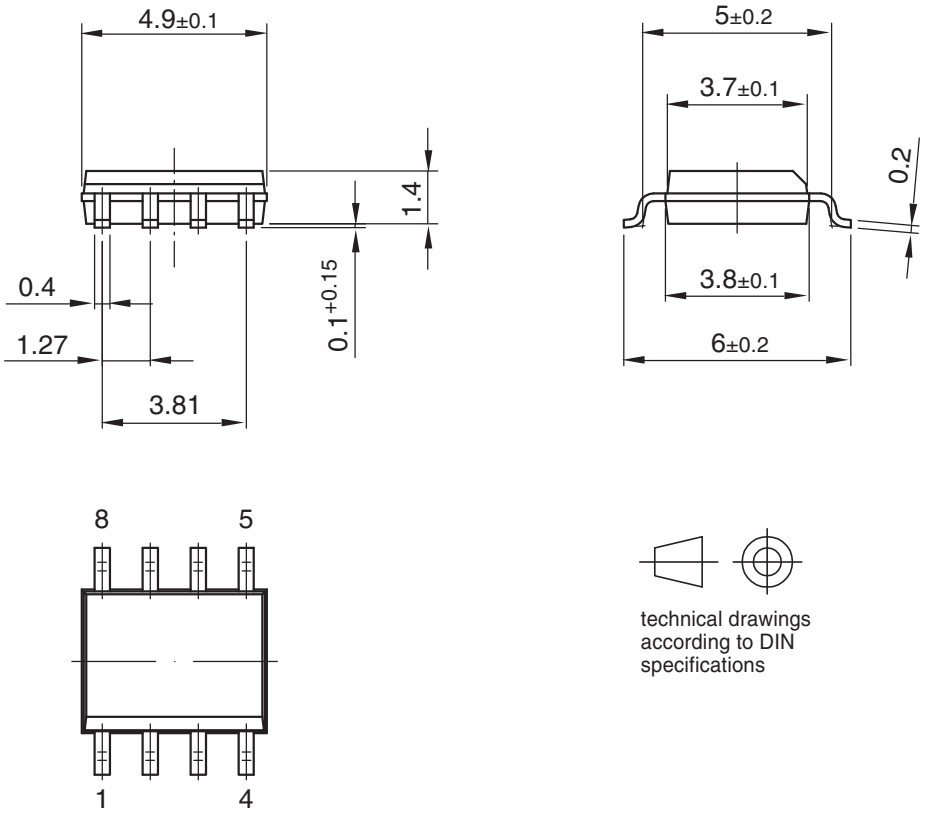
7. Ordering Information

Extended Type Number	Package	Remarks
ATA6662-TAQY	SO8	LIN transceiver, Pb-free, 4k, taped and reeled

8. Package Information

Package: SO 8

Dimensions in mm



Drawing-No.: 6.541-5031.01-4

Issue: 1; 15.08.06

9. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4916M-AUTO-09/09	• Figure 1-1 “Block Diagram” on page 1 changed • Section 4 “Absolute Maximum Ratings” on page 8 changed • Figure 6-2 “Application Circuit” on page 14 changed
4916L-AUTO-02/09	• Section 6 “Electrical Characterisitcs” numbers 3.2 and 4.2 on page 9 changed
4916K-AUTO-12/08	• Figure 2-1 “Pinning SO8” on page 2 changed • Section 3.2 “Supply Pin (V_S)” on page 3 changed • Section 3.8 “Enable Input Pin (EN)” on page 4 changed • Section 3.11 “Operation Modes” on page 5 changed • Section 3.12 “Remote Wake-up via Dominant Bus State” on page 5 changed • Section 3.14 “Wake-up Source Recognition” on page 6 changed • Figure 3.2 “LIN Wake-up Waveform Diagram” on page 7 changed • Figure 3.3 “Wake-up from Wake-up Switch” on page 7 changed • Section 4 “Absolute Maximum Ratings” on page 8 changed • Section 5 “Thermal Resistance” on page 8 changed • Section 6 “Electrical Characteristics” on pages 9 to 12 changed • Figure 6-2 “Application Circuit” on page 13 changed
4916J-AUTO-02/08	• “Pre-normal Mode” in “Fail-safe Mode” changed • Section 3.9 “Inhibit Output Pin (INH) on page 4 changed • Section 4 “Absolute Maximum Ratings” on page 8 changed • Section 6 “Electrical Characteristics” number 5.1 on page 9 changed
4916I-AUTO-12/07	• Section 3.1 “Physical Layer Compatibility” on page 3 added • Section 6 “Electrical Characteristics” numbers 1.5, 1.6 and 1.7 on page 9 changed
4916H-AUTO-10/07	• Section 7 “Ordering Information” on page 14 changed
4916G-AUTO-07/07	• Put datasheet in a new template • Capital T for time generally changed in a lower case t

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4916F-AUTO-05/07	• Figure 1-1 “Block Diagram” on page 1 changed • Figure 6-2 “Application Circuit” on page 13 changed • Features on page 1 changed • Section 6 “Electrical Characteristics” numbers 10.1 to 10.4 and 11.1, 11.2 changed
4916E-AUTO-02/07	• Section 4 “Absolute Maximum Ratings” on page 8 changed • Section 2 “Electrical Characteristics” on pages 9 to 11 changed
4916D-AUTO-02/07	• Features on page 1 changed • Section 1 “Description” on page 1 changed • Table 2-1 “Pin Description” on page 2 changed • Section 3.2 “Ground Pin (GND) on page 3 changed • Section 3.7 “Enable Input Pin (EN)” on page 4 changed • Section 3.11 “Remote Wake-up via Dominant Bus State” on page 5 changed • Figure 3-1 “Mode of Operation” on page 6 changed • Section 3-14 “Fail-safe Features” on page 6 changed • Section 4 “Absolute Maximum Ratings” on page 8 changed • Section 6 “Electrical Characteristics” on pages 9 to 11 changed

Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Unit 1-5 & 16, 19/F
BEA Tower, Millennium City 5
418 Kwun Tong Road
Kwun Tong, Kowloon
Hong Kong
Tel: (852) 2245-6100
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054
Saint-Quentin-en-Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com

Technical Support
auto_control@atmel.com

Sales Contact
www.atmel.com/contacts

Literature Requests
www.atmel.com/literature