

PSRAM

2-Mbit (256K x 8)

Pseudo Static RAM

Features

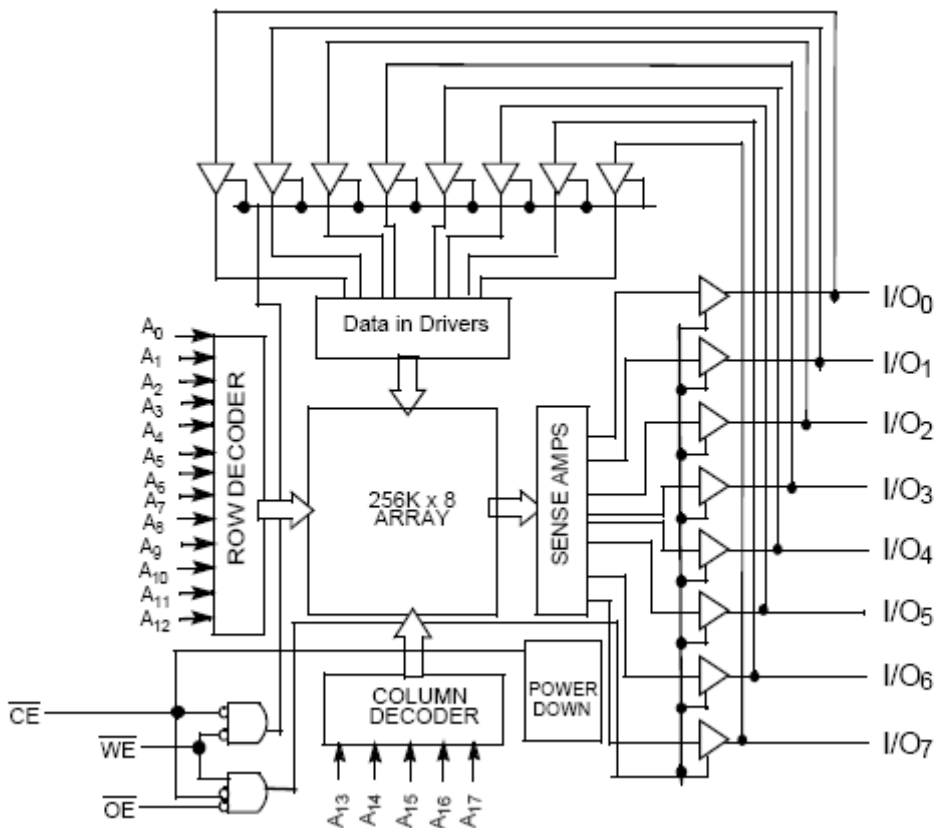
- Advanced low-power architecture
- High speed: 55 ns, 70 ns
- Wide voltage range: 2.7V to 3.6V
- Typical active current: 1 mA @ f = 1 MHz
- Low standby power
- Automatic power-down when deselected

Functional Description

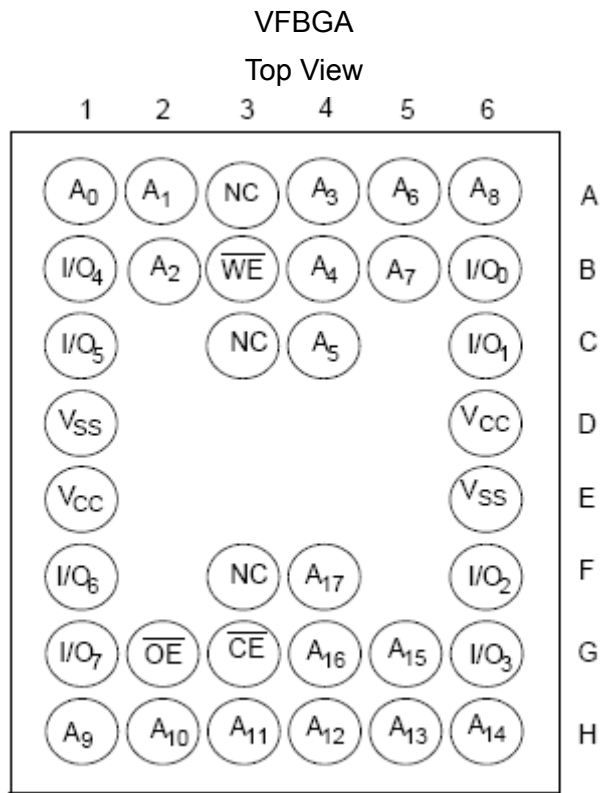
The M24L28256SA is a high-performance CMOS pseudo static RAM (PSRAM) organized as 256K words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ( $\overline{CE}$ ) and active LOW Output Enable ( $\overline{OE}$ ). This device has an automatic power-down feature that reduces power consumption dramatically when deselected. Writing to

the device is accomplished by asserting Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. Data on the eight I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is then written into the location specified on the address pins (A<sub>0</sub> through A<sub>17</sub>). Reading from the device is accomplished by asserting the Chip Enable One ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) inputs LOW while forcing Write Enable ( $\overline{WE}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins. The eight input/output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), or during write operation ( $\overline{CE}$  LOW and  $\overline{WE}$  LOW). See the Truth Table for a complete description of read and write modes.

Logic Block Diagram



Pin Configuration[2, 3]



Product Portfolio

Product	V <sub>CC</sub> Range (V)			Speed(ns)	Power Dissipation					
					Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (μA)	
	f = 1MHz		f = f <sub>MAX</sub>							
	Min.	Typ.	Max.		Typ.[3]	Max.	Typ.[3]	Max.	Typ. [3]	Max.
M24L28256SA	2.7	3.0	3.6	55	1	5	14	22	9	40
				70			8	15		

Notes:

- 2.NC "no connect"—not connected internally to the die.
- 3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC (typ)</sub> and T<sub>A</sub> = 25°C.

## Maximum Ratings

(Above which the useful life may be impaired. For user guide-lines, not tested.)  
 Storage Temperature .....-65°C to +150°C  
 Ambient Temperature with Power Applied .....-55°C to +125°C  
 Supply Voltage to Ground Potential .....-0.4V to 4.6V  
 DC Voltage Applied to Outputs in High-Z State[4, 5, 6] .....-0.4V to 3.7V  
 DC Input Voltage[4, 5, 6].....-0.4V to 3.7V  
 Output Current into Outputs (LOW) .....20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)  
 Latch-up Current .....> 200 mA

## Operating Range

Range	Ambient Temperature (T <sub>A</sub> )	V <sub>CC</sub>
Extended	-25°C to +85°C	2.7V to 3.6V
Industrial	-40°C to +85°C	2.7V to 3.6V

## Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions	-55			-70			Unit
			Min.	Typ. [3]	Max.	Min.	Typ. [3]	Max.	
V <sub>CC</sub>	Supply Voltage		2.7	3.0	3.6	2.7	3.0	3.6	V
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -0.1 mA	V <sub>CC</sub> -0.4			V <sub>CC</sub> -0.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 0.1 mA			0.4			0.4	V
V <sub>IH</sub>	Input HIGH Voltage		0.8* V <sub>CC</sub>		V <sub>CC</sub> +0.4	0.8* V <sub>CC</sub>		V <sub>CC</sub> +0.4	V
V <sub>IL</sub>	Input LOW Voltage		-0.4		0.4	-0.4		0.4	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-1		+1	-1		+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output Disable	-1		+1	-1		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		14	22		8	15	mA
		f = 1 MHz		1	5		1	5	
I <sub>SB1</sub>	Automatic $\overline{CE}$ Power-Down Current —CMOS Inputs	$\overline{CE} \geq V_{CC}-0.2V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≤ 0.2V, f = f <sub>MAX</sub> (Address and Data Only), f = 0		40	250		40	250	μA
I <sub>SB2</sub>	Automatic $\overline{CE}$ Power-Down Current —CMOS Inputs	$\overline{CE} \geq V_{CC}-0.2V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≤ 0.2V, f = 0, V <sub>CC</sub> = 3.6V		9	40		9	40	μA

## Capacitance[7]

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	TA = 25°C, f = 1 MHz	8	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = V <sub>CC(typ)</sub>	8	pF

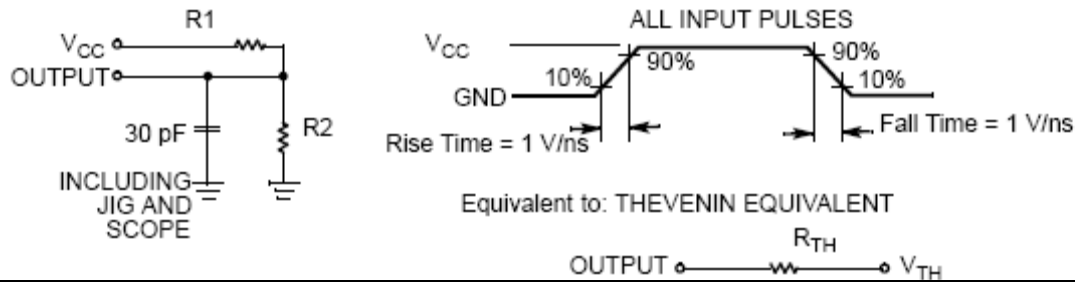
## Thermal Resistance[7]

Parameter	Description	Test Conditions	BGA	Unit
θ <sub>JA</sub>	Thermal Resistance(Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/ JESD51.	55	°C/W
θ <sub>JC</sub>	Thermal Resistance (Junction to Case)		17	°C/W

### Notes:

- V<sub>IH(MAX)</sub> = V<sub>CC</sub> + 0.5V for pulse durations less than 20 ns.
- V<sub>IL(MIN)</sub> = -0.5V for pulse durations less than 20 ns.
- Overshoot and undershoot specifications are characterized and are not 100% tested.
- Tested initially and after design or process changes that may affect these parameters.

## AC Test Loads and Waveforms



Parameters	3.0V (V <sub>CC</sub> )	Unit
R1	22000	Ω
R2	22000	Ω
R <sub>TH</sub>	11000	Ω
V <sub>TH</sub>	1.50	V

## Switching Characteristics Over the Operating Range [8]

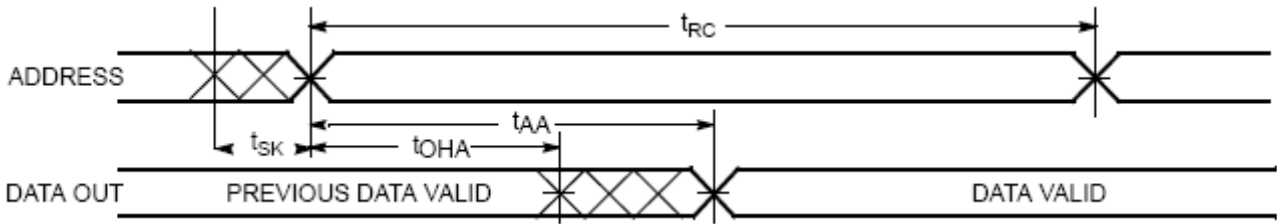
Parameter	Description	-55		-70		Unit
		Min.	Max.	Min.	Max.	
<b>Read Cycle</b>						
t <sub>RC</sub>	Read Cycle Time	55[12]		70		ns
t <sub>AA</sub>	Address to Data Valid		55		70	ns
t <sub>OHA</sub>	Data Hold from Address Change	5		10		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW		55		70	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		25		35	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z[9, 10]	5		5		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z[9, 10]		25		25	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW	2		5		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH		25		25	ns
t <sub>SK</sub> [12]	Address Skew		0		10	ns
<b>Write Cycle [11]</b>						
t <sub>WC</sub>	Write Cycle Time	55		70		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW	45		55		ns
t <sub>AW</sub>	Address Set-Up to Write End	45		55		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	40		55		ns
t <sub>SD</sub>	Data Set-Up to Write End	25		25		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High-Z[9, 10]		25		25	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low-Z[9, 10]	5		5		ns

### Notes:

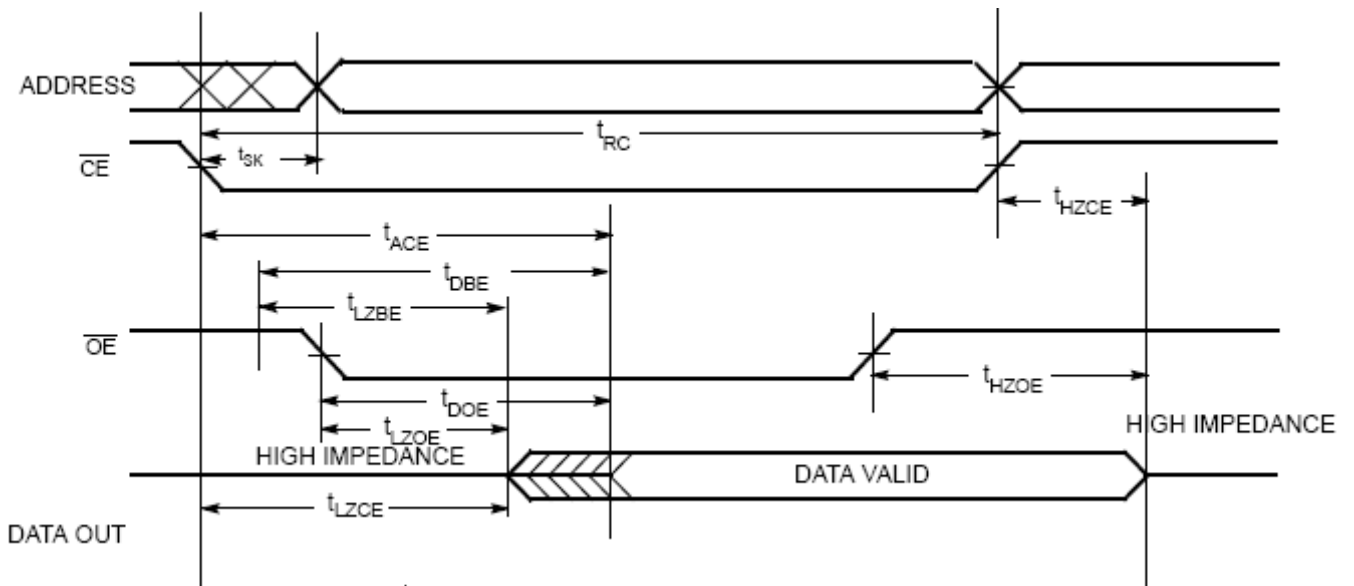
- Test conditions assume signal transition time of 1V/ns or higher, timing reference levels of V<sub>CC(typ)</sub>/2, input pulse levels of 0V to V<sub>CC(typ)</sub>, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance
- t<sub>HZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> transitions are measured when the outputs enter a high-impedance state.
- High-Z and Low-Z parameters are characterized and are not 100% tested.
- The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates write.
- To achieve 55-ns performance, the read access should be  $\overline{CE}$  controlled. In this case t<sub>ACE</sub> is the critical parameter and t<sub>SK</sub> is satisfied when the addresses are stable prior to chip enable going active. For the 70-ns cycle, the addresses must be stable within 10 ns after the start of the read cycle.

Switching Waveforms

Read Cycle 1 (Address Transition Controlled)[12, 13, 14]



Read Cycle 2 ( $\overline{OE}$  Controlled)[12, 14]

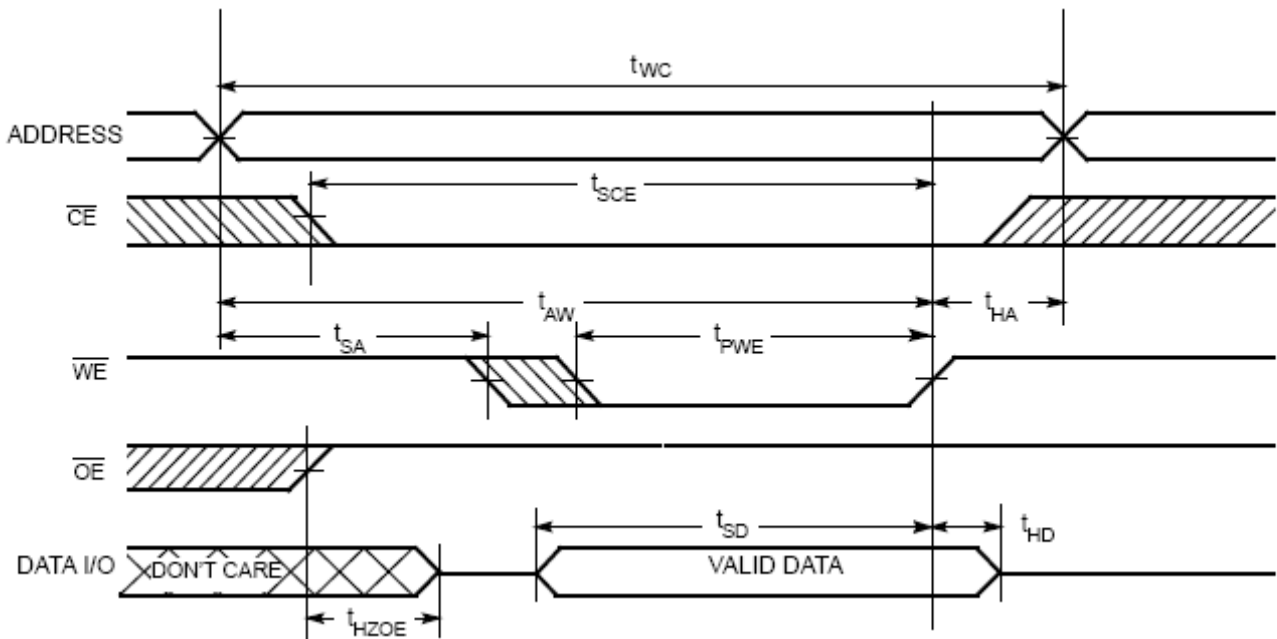


Notes:

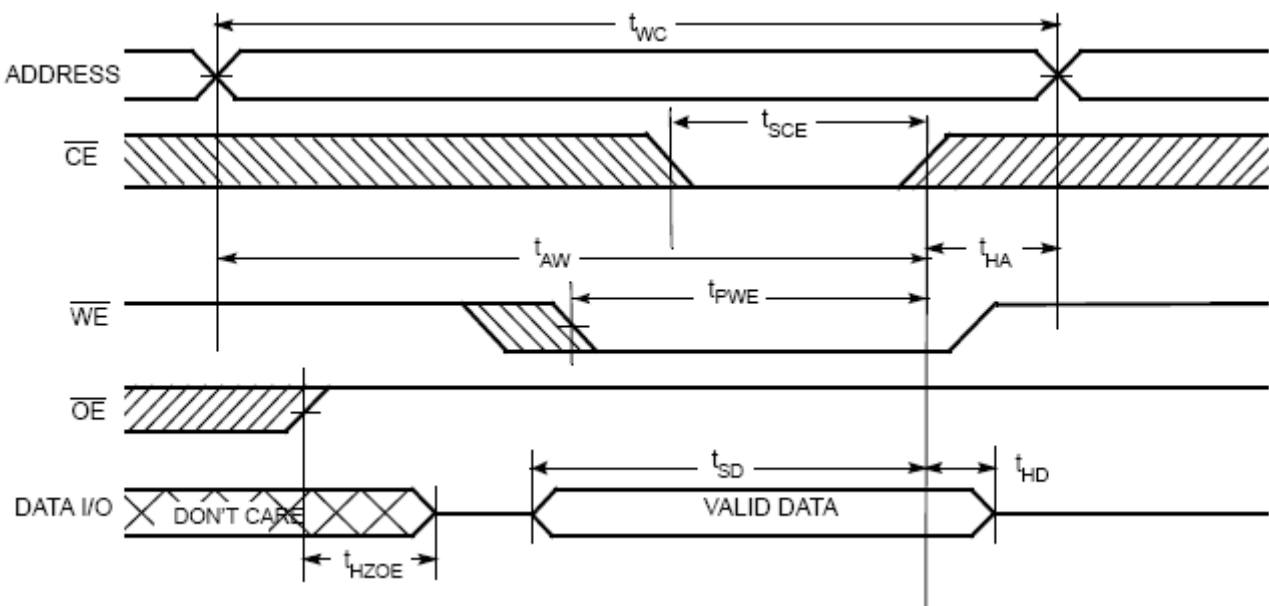
- 13. Device is continuously selected.  $\overline{OE}$  and  $\overline{CE} = V_{IL}$ .
- 14.  $\overline{WE}$  is HIGH for Read Cycle.

Switching Waveforms (continued)

Write Cycle 1 ( $\overline{WE}$  Controlled)[10,11, 15, 16, 17]



Write Cycle 2 ( $\overline{CE}$  Controlled) [9, 10, 15, 16, 17]



Notes:

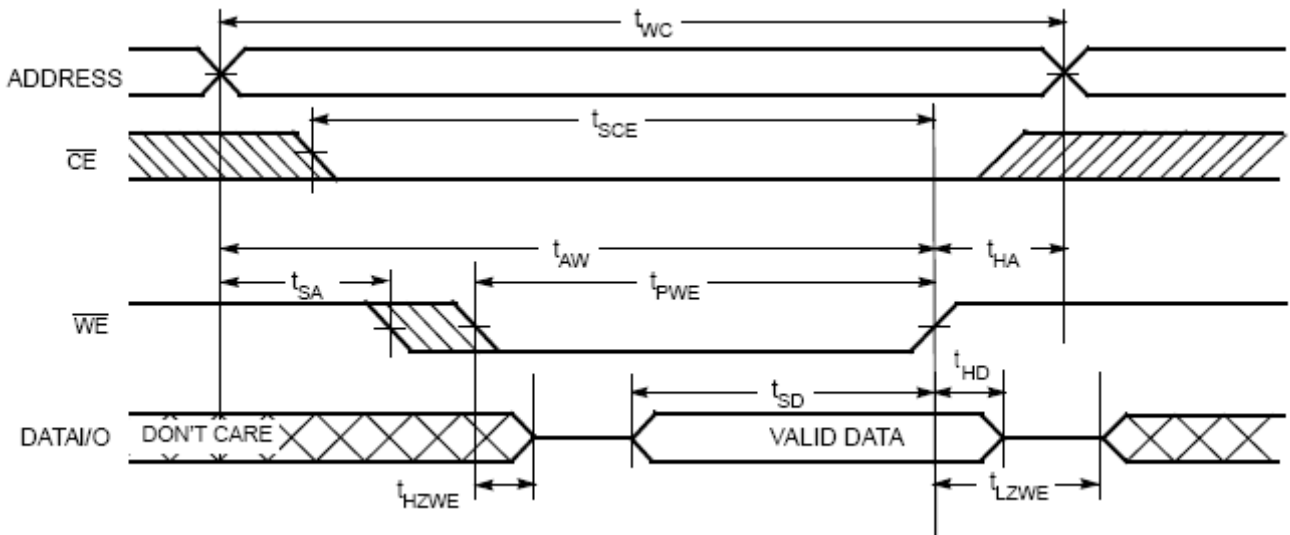
15.Data I/O is high impedance if  $\overline{OE} \geq V_{IH}$ .

16. If Chip Enables go INACTIVE simultaneously with  $\overline{WE} = \text{HIGH}$ , the output remains in a high-impedance state.

17.During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

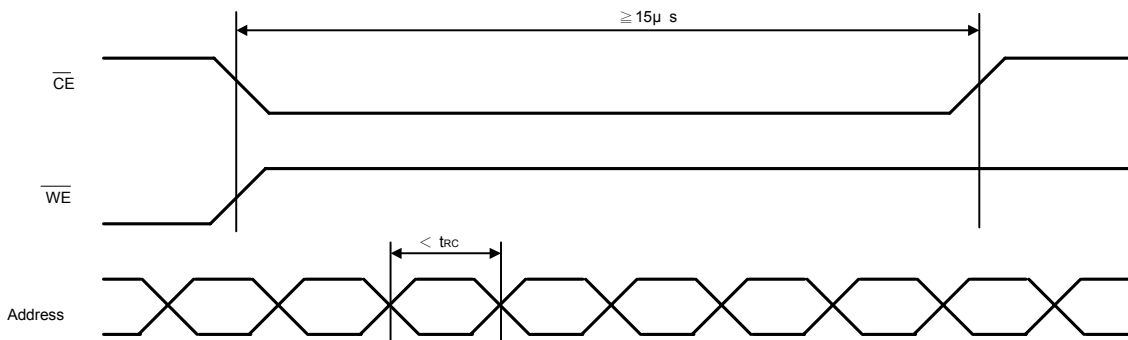
Write Cycle 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)[16, 17]



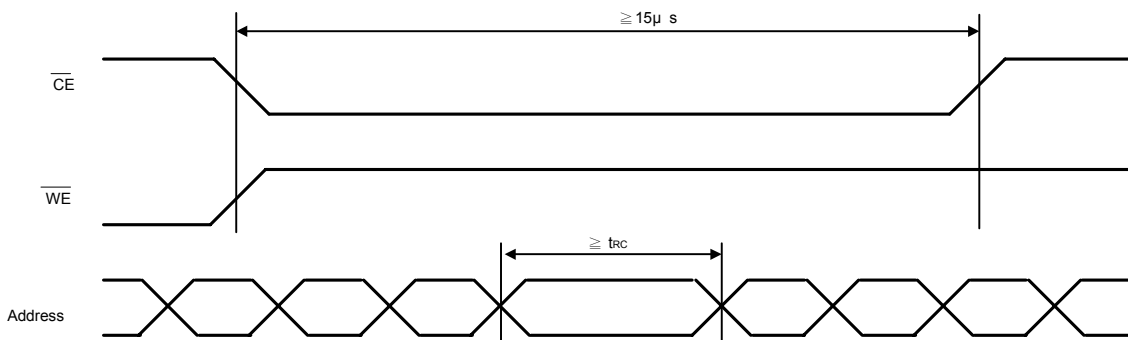
## Avoid Timing

ESMT Pseudo SRAM has a timing which is not supported at read operation, If your system has multiple invalid address signal shorter than  $t_{RC}$  during over  $15\mu s$  at read operation shown as in Abnormal Timing, it requires a normal read timing at least during  $15\mu s$  shown as in Avoidable timing 1 or toggle  $\overline{CE}$  to high ( $\geq t_{RC}$ ) one time at least shown as in Avoidable Timing 2.

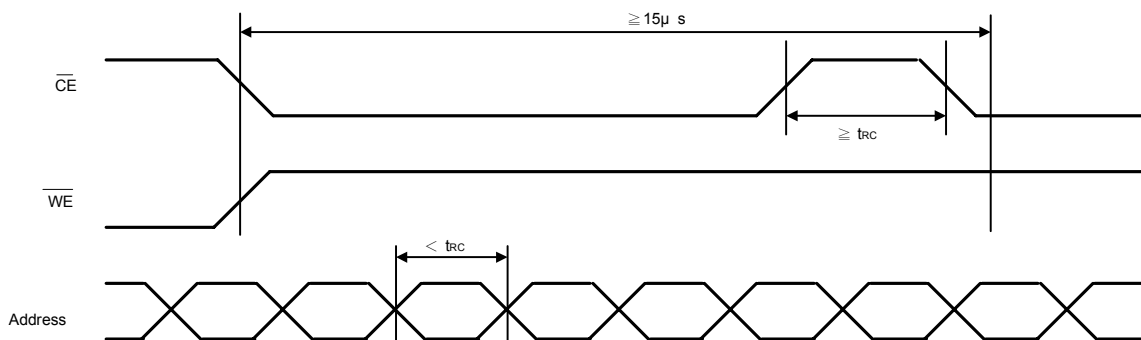
## Abnormal Timing



## Avoidable Timing 1



## Avoidable Timing 2





Truth Table[18]

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O <sub>0</sub> -I/O <sub>7</sub>	Mode	Power
H	X	X	High Z	Power-Down	Standby (I <sub>SB</sub> )
X	X	X	High Z	Power-Down	Standby (I <sub>SB</sub> )
L	L	H	Data Out	Read	Active (I <sub>CC</sub> )
L	X	L	Data In	Write	Active (I <sub>CC</sub> )
L	H	H	High Z	Selected, Outputs Disabled	Active (I <sub>CC</sub> )

## Ordering Information

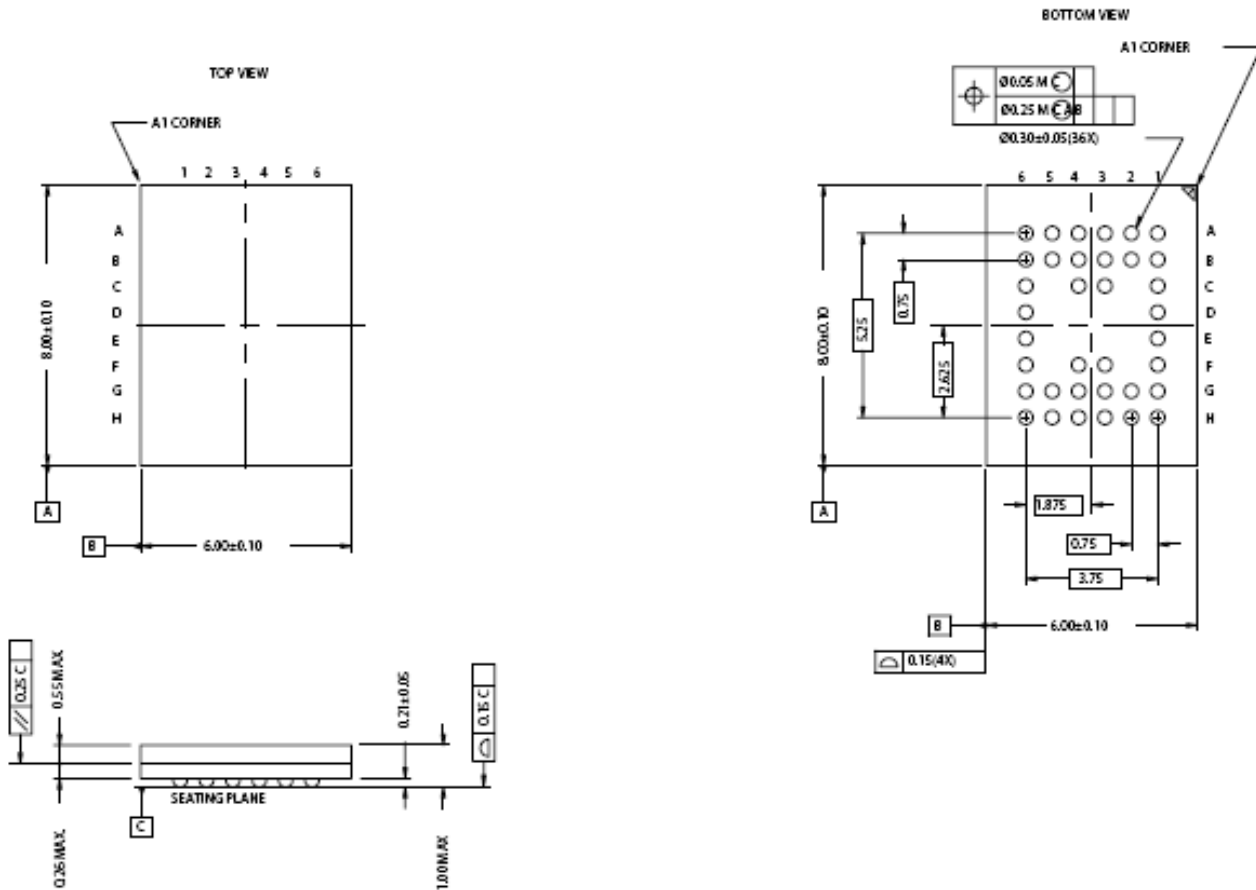
Speed (ns)	Ordering Code	Package Type	Operating Range
55	M24L28256SA-55BEG	36-Lead VFBGA (6 x 8 x 1 mm) (Pb-free)	Extended
70	M24L28256SA-70BEG	36-Lead VFBGA (6 x 8 x 1 mm) (Pb-free)	Extended
55	M24L28256SA-55BIG	36-Lead VFBGA (6 x 8 x 1 mm) (Pb-free)	Industrial
70	M24L28256SA-70BIG	36-Lead VFBGA (6 x 8 x 1 mm) (Pb-free)	Industrial

Note:

18.H = Logic HIGH, L = Logic LOW, X = Don't Care.

## Package Diagrams

### 36-Lead VFBGA (6 x 8 x 1 mm) BV36A



## Revision History

Revision	Date	Description
1.0	2007.07.19	Original
1.1	2008.07.04	<ol style="list-style-type: none"><li>1. Move Revision History to the last</li><li>2. Modify voltage range 2.7V~3.3V to 2.7V~3.6V</li><li>3. Correct type error for Extended Temperature (-40~85°C =&gt; -25~85°C)</li><li>4. Add Industrial grade</li><li>5. Add Avoid timing</li></ol>

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