

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

Designed primarily for CW large-signal output and driver applications with frequencies up to 600 MHz. Devices are unmatched and are suitable for use in industrial, medical and scientific applications.

- Typical CW Performance: $V_{DD} = 50$ Volts, $I_{DQ} = 900$ mA,
 $P_{out} = 300$ Watts, $f = 220$ MHz
 Power Gain — 25.5 dB
 Drain Efficiency — 68%
- Capable of Handling 10:1 VSWR, @ 50 Vdc, 220 MHz, 300 Watts CW Output Power

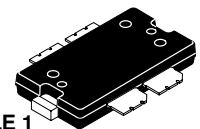
Features

- Integrated ESD Protection
- Excellent Thermal Stability
- Facilitates Manual Gain Control, ALC and Modulation Techniques
- 200°C Capable Plastic Package
- RoHS Compliant
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.

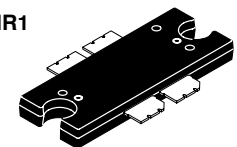
MRF6V2300NR1
MRF6V2300NBR1

10-600 MHz, 300 W, 50 V
LATERAL N-CHANNEL
SINGLE-ENDED
BROADBAND
RF POWER MOSFETs

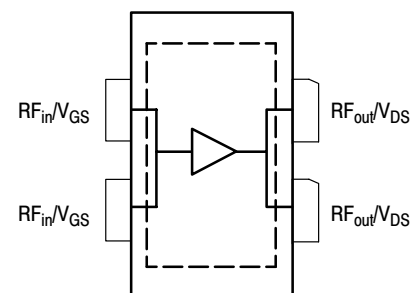
CASE 1486-03, STYLE 1
TO-270 WB-4
PLASTIC
MRF6V2300NR1



CASE 1484-04, STYLE 1
TO-272 WB-4
PLASTIC
MRF6V2300NBR1



PARTS ARE SINGLE-ENDED



(Top View)

Note: Exposed backside of the package is the source terminal for the transistor.

Figure 1. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +110	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +10	Vdc
Storage Temperature Range	T_{stg}	- 65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature	T_J	200	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (1,2)	Unit
Thermal Resistance, Junction to Case Case Temperature 83°C, 300 W CW	$R_{\theta JC}$	0.24	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2 (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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Off Characteristics

Zero Gate Voltage Drain Leakage Current ($V_{DS} = 100\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	2.5	mA
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 50\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	50	μAdc
Drain-Source Breakdown Voltage ($I_D = 150\text{ mA}$, $V_{GS} = 0\text{ Vdc}$)	$V_{(BR)DSS}$	110	—	—	Vdc
Gate-Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	10	μAdc

On Characteristics

Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 800\text{ }\mu\text{Adc}$)	$V_{GS(th)}$	1	1.63	3	Vdc
Gate Quiescent Voltage ($V_{DD} = 50\text{ Vdc}$, $I_D = 900\text{ mAdc}$, Measured in Functional Test)	$V_{GS(Q)}$	1.5	2.6	3.5	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 2\text{ Adc}$)	$V_{DS(on)}$	—	0.28	—	Vdc

Dynamic Characteristics

Reverse Transfer Capacitance ($V_{DS} = 50\text{ Vdc} \pm 30\text{ mV(rms)}$ ac @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{rss}	—	2.88	—	pF
Output Capacitance ($V_{DS} = 50\text{ Vdc} \pm 30\text{ mV(rms)}$ ac @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{oss}	—	120	—	pF
Input Capacitance ($V_{DS} = 50\text{ Vdc}$, $V_{GS} = 0\text{ Vdc} \pm 30\text{ mV(rms)}$ ac @ 1 MHz)	C_{iss}	—	268	—	pF

Functional Tests (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 50\text{ Vdc}$, $I_{DQ} = 900\text{ mA}$, $P_{out} = 300\text{ W}$, $f = 220\text{ MHz}$, CW

Power Gain	G_{ps}	24	25.5	27	dB
Drain Efficiency	η_D	66	68	—	%
Input Return Loss	IRL	—	-16	-9	dB

1. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.



ATTENTION: The MRF6V2300N and MRF6V2300NB are high power devices and special considerations must be followed in board design and mounting. Incorrect mounting can lead to internal temperatures which exceed the maximum allowable operating junction temperature. Refer to Freescale Application Note AN3263 (for bolt down mounting) or AN1907 (for solder reflow mounting) **PRIOR TO STARTING SYSTEM DESIGN** to ensure proper mounting of these devices.

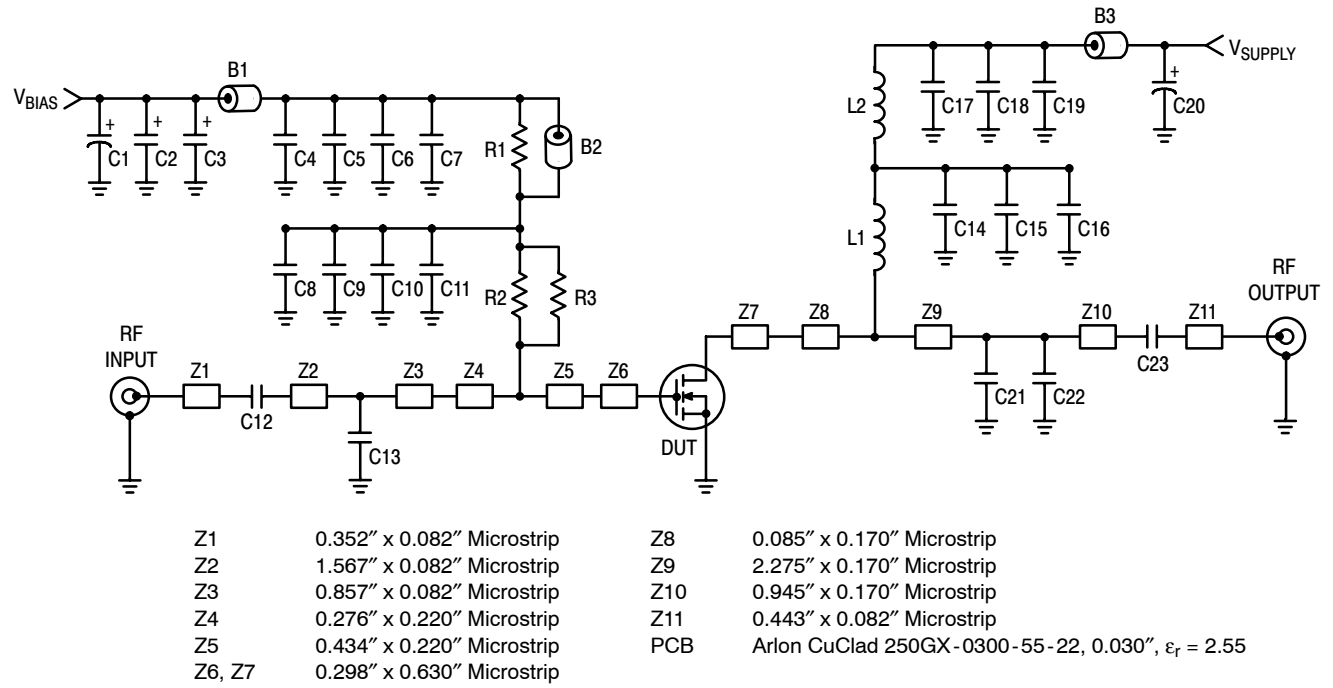
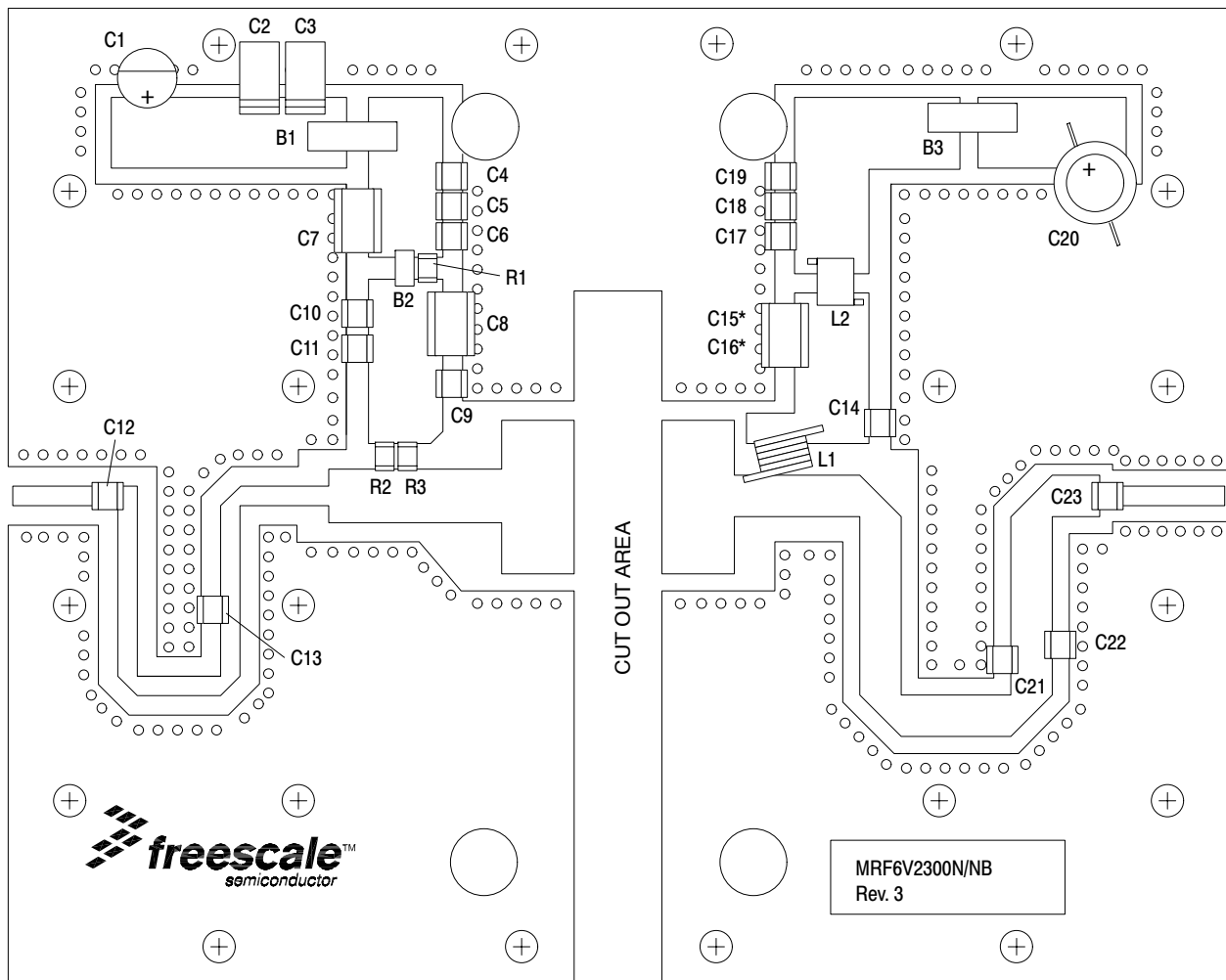


Figure 2. MRF6V2300NR1 (NBR1) Test Circuit Schematic

Table 6. MRF6V2300NR1 (NBR1) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
B1, B2	95 Ω , 100 MHz Long Ferrite Beads, Surface Mount	2743021447	Fair-Rite
B3	47 Ω , 100 MHz Short Ferrite Bead, Surface Mount	2743019447	Fair-Rite
C1	47 μ F, 50 V Electrolytic Capacitor	476KXM063M	Illinois Capacitor
C2	22 μ F, 35 V Tantalum Capacitor	T494X226K035AT	Kemet
C3	10 μ F, 35 V Tantalum Capacitor	T491D106K035AT	Kemet
C4, C19	10 K pF Chip Capacitors	ATC200B103KT50XT	ATC
C5, C18	20 K pF Chip Capacitors	ATC200B203KT50XT	ATC
C6, C11, C17	0.1 μ F, 50 V Chip Capacitors	CDR33BX104AKYS	AVX
C7, C8, C15, C16	2.2 μ F, 50 V Chip Capacitors	C1825C225J5RAC	Kemet
C10	220 nF Chip Capacitor	C1206C224Z5VAC	Kemet
C9, C12, C14, C23	1000 pF Chip Capacitors	ATC100B102JT50XT	ATC
C13	82 pF Chip Capacitor	ATC100B820JT500XT	ATC
C20	470 μ F, 63 V Electrolytic Capacitor	477KXM063M	Illinois Capacitor
C21	24 pF Chip Capacitor	ATC100B240JT500XT	ATC
C22	39 pF Chip Capacitor	ATC100B390JT500XT	ATC
L1	4 Turn #18 AWG, 0.18" ID	None	None
L2	82 nH Inductor	1812SMS-82NJ	Coilcraft
R1	270 Ω , 1/4 W Chip Resistor	CRCW12062700FKTA	Vishay
R2, R3	4.75 Ω , 1/4 W Chip Resistors	CRCW12064R75FKTA	Vishay



* Stacked

Figure 3. MRF6V2300NR1(NBR1) Test Circuit Component Layout

TYPICAL CHARACTERISTICS

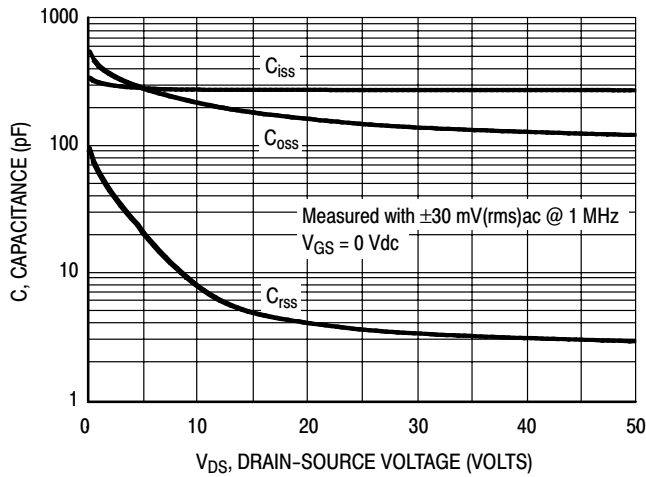


Figure 4. Capacitance versus Drain-Source Voltage

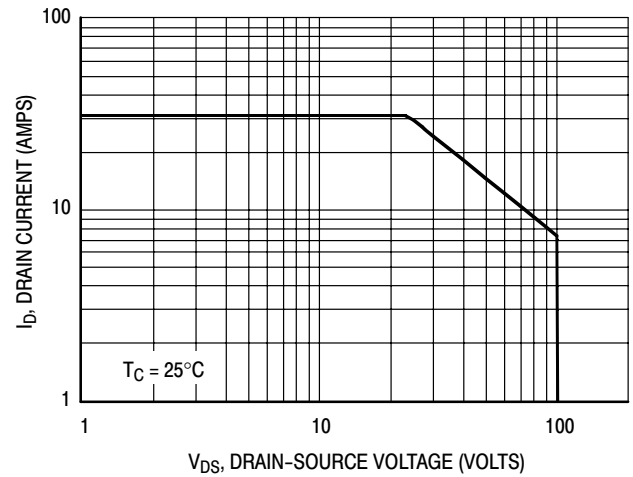


Figure 5. DC Safe Operating Area

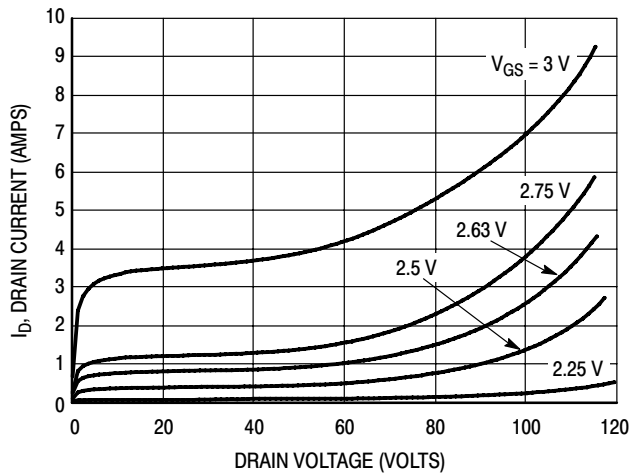


Figure 6. DC Drain Current versus Drain Voltage

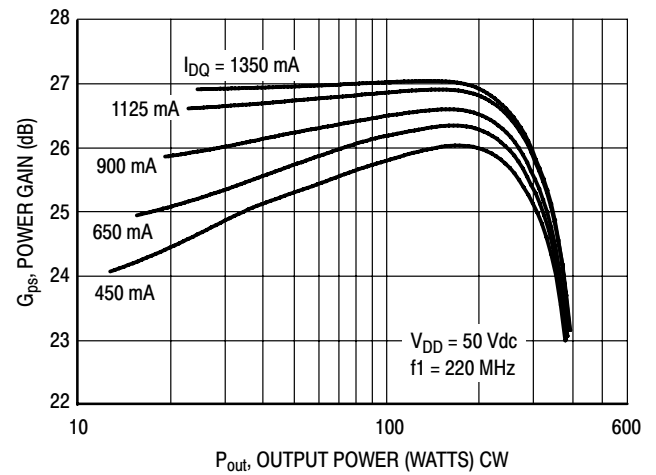


Figure 7. CW Power Gain versus Output Power

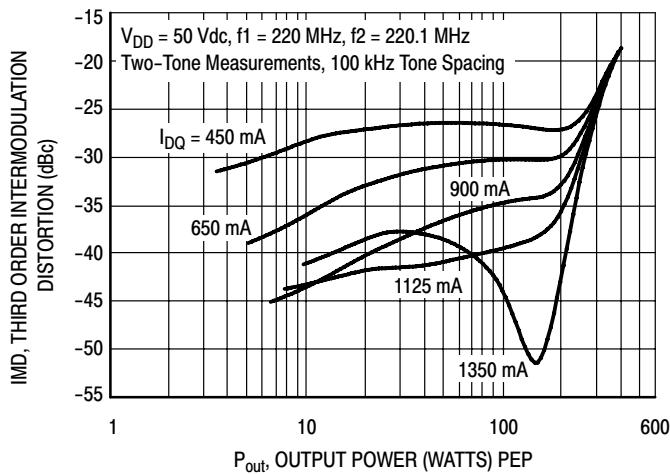


Figure 8. Third Order Intermodulation Distortion versus Output Power

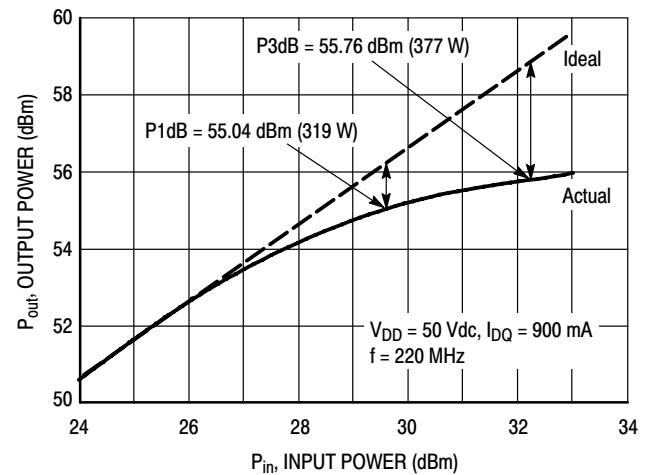


Figure 9. CW Output Power versus Input Power

TYPICAL CHARACTERISTICS

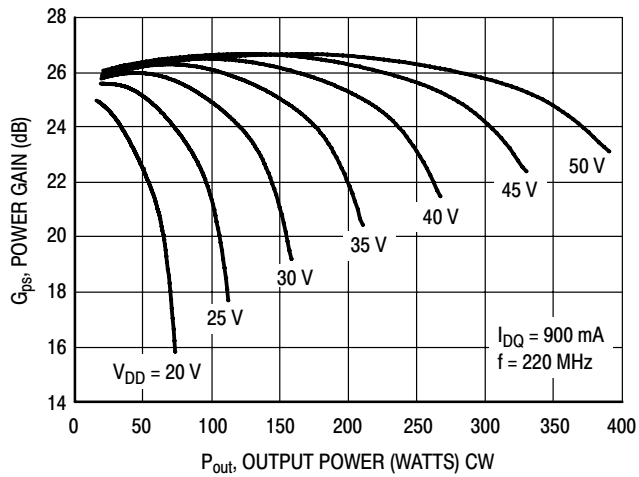


Figure 10. Power Gain versus Output Power

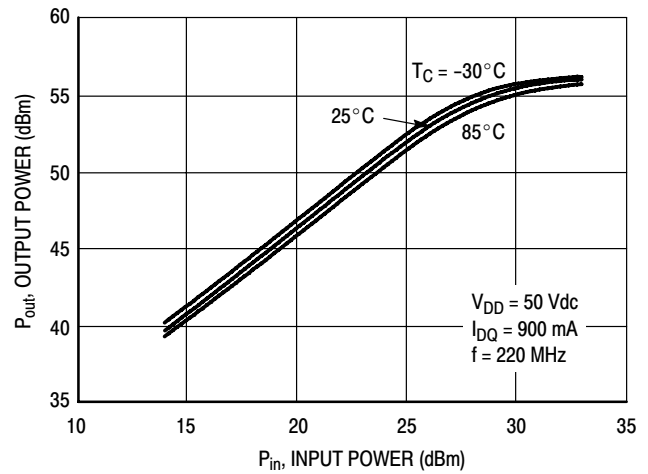


Figure 11. Power Output versus Power Input

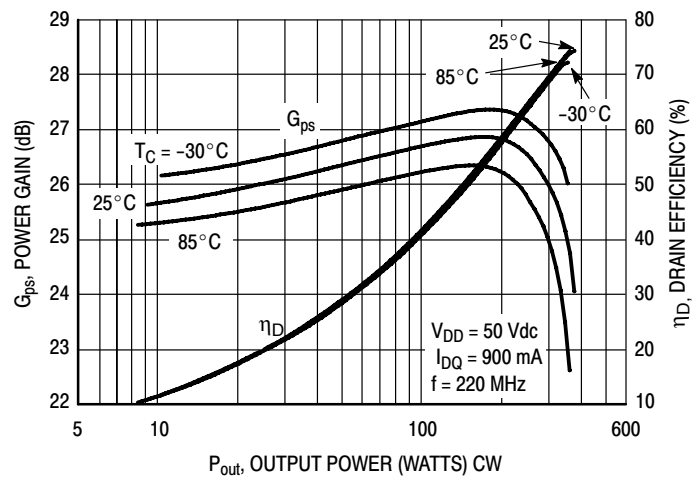


Figure 12. Power Gain and Drain Efficiency versus CW Output Power

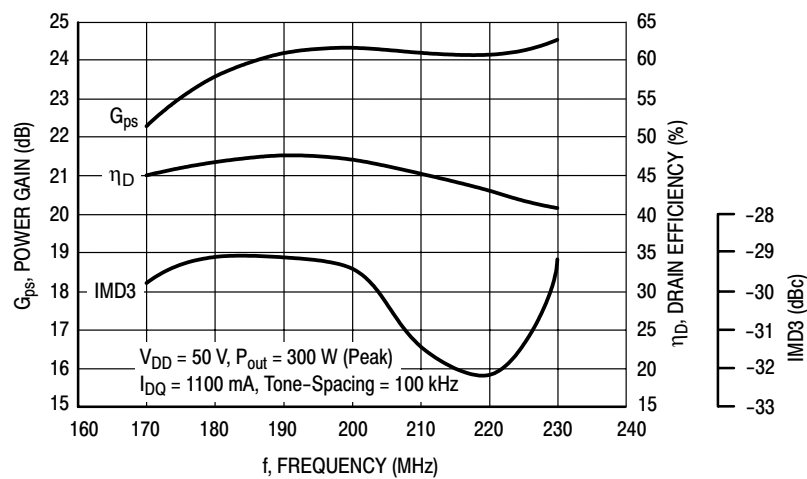
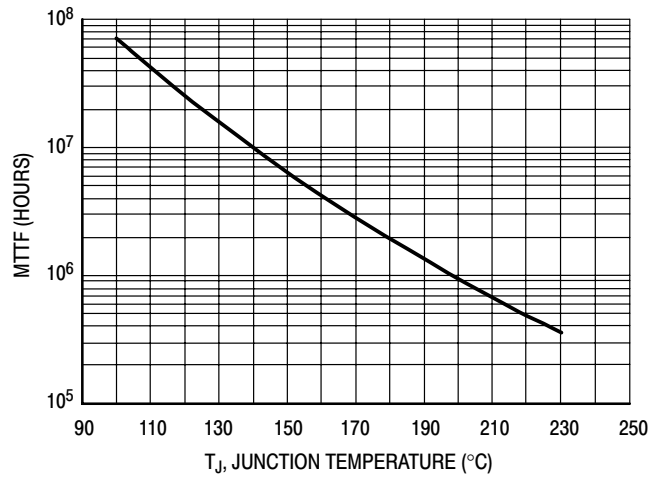


Figure 13. VHF Broadcast Broadband Performance

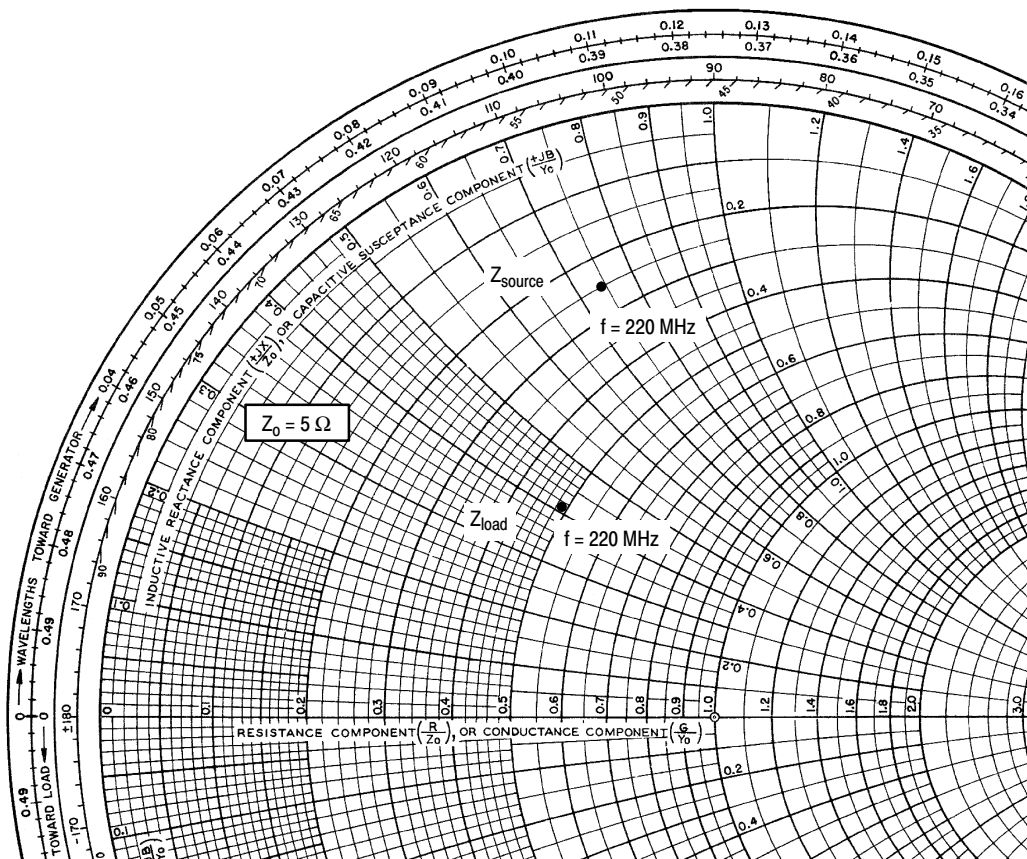
TYPICAL CHARACTERISTICS



This above graph displays calculated MTTF in hours when the device is operated at $V_{DD} = 50$ Vdc, $P_{out} = 300$ W CW, and $\eta_D = 68\%$.

MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

Figure 14. MTTF versus Junction Temperature



$V_{DD} = 50 \text{ Vdc}$, $I_{DQ} = 900 \text{ mA}$, $P_{out} = 300 \text{ W CW}$

f MHz	Z_{source} Ω	Z_{load} Ω
220	$1.23 + j3.69$	$2.43 + j2.04$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

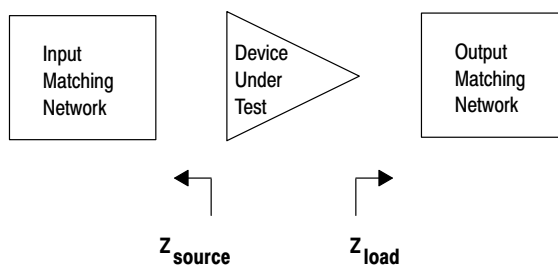
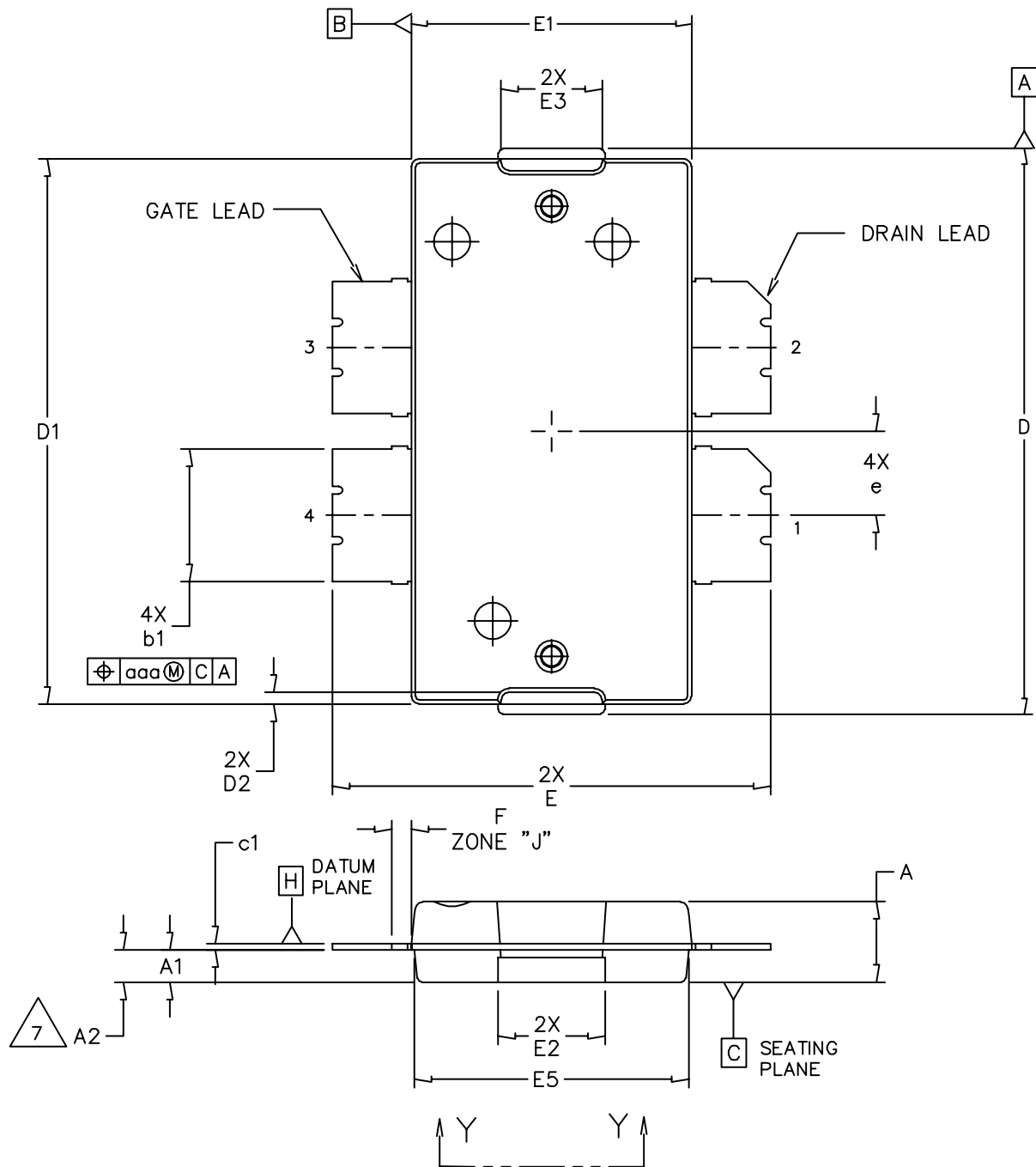


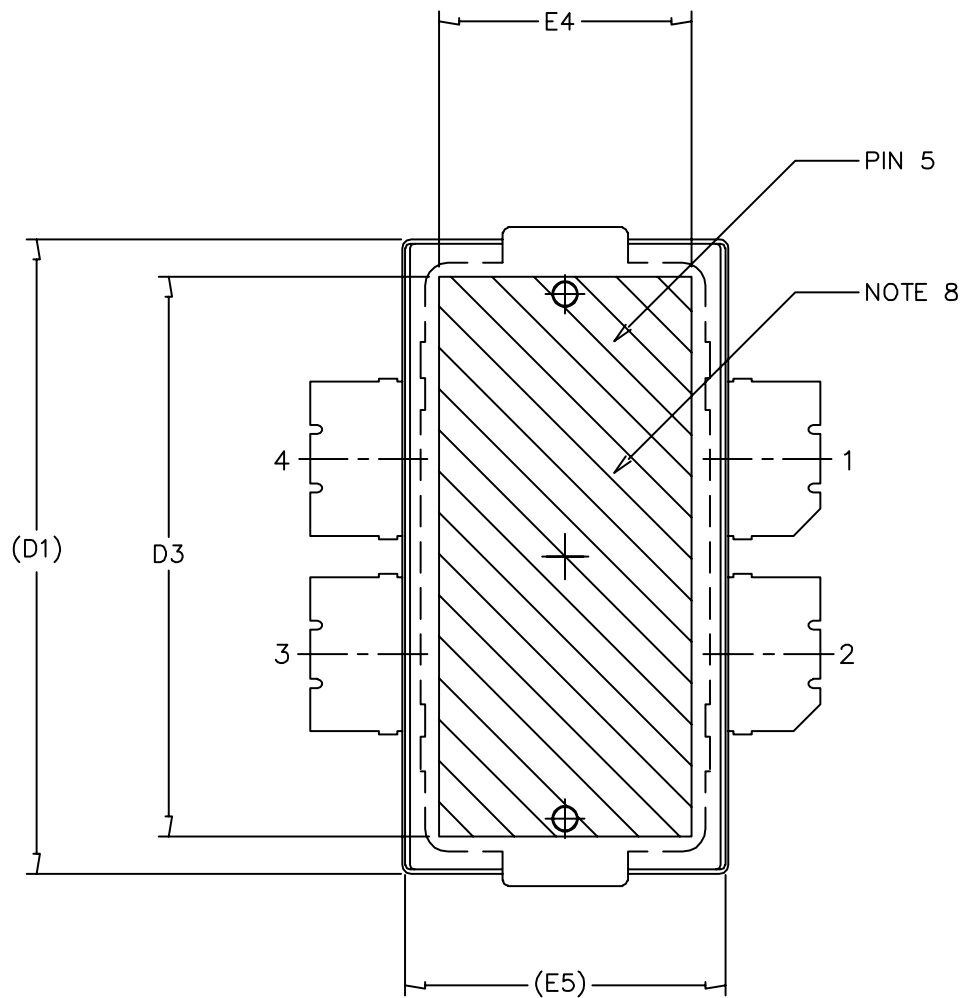
Figure 15. Series Equivalent Source and Load Impedance

PACKAGE DIMENSIONS



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		CASE NUMBER: 1486-03	13 AUG 2007
		STANDARD: NON-JEDEC	

MRF6V2300NR1 MRF6V2300NBR1



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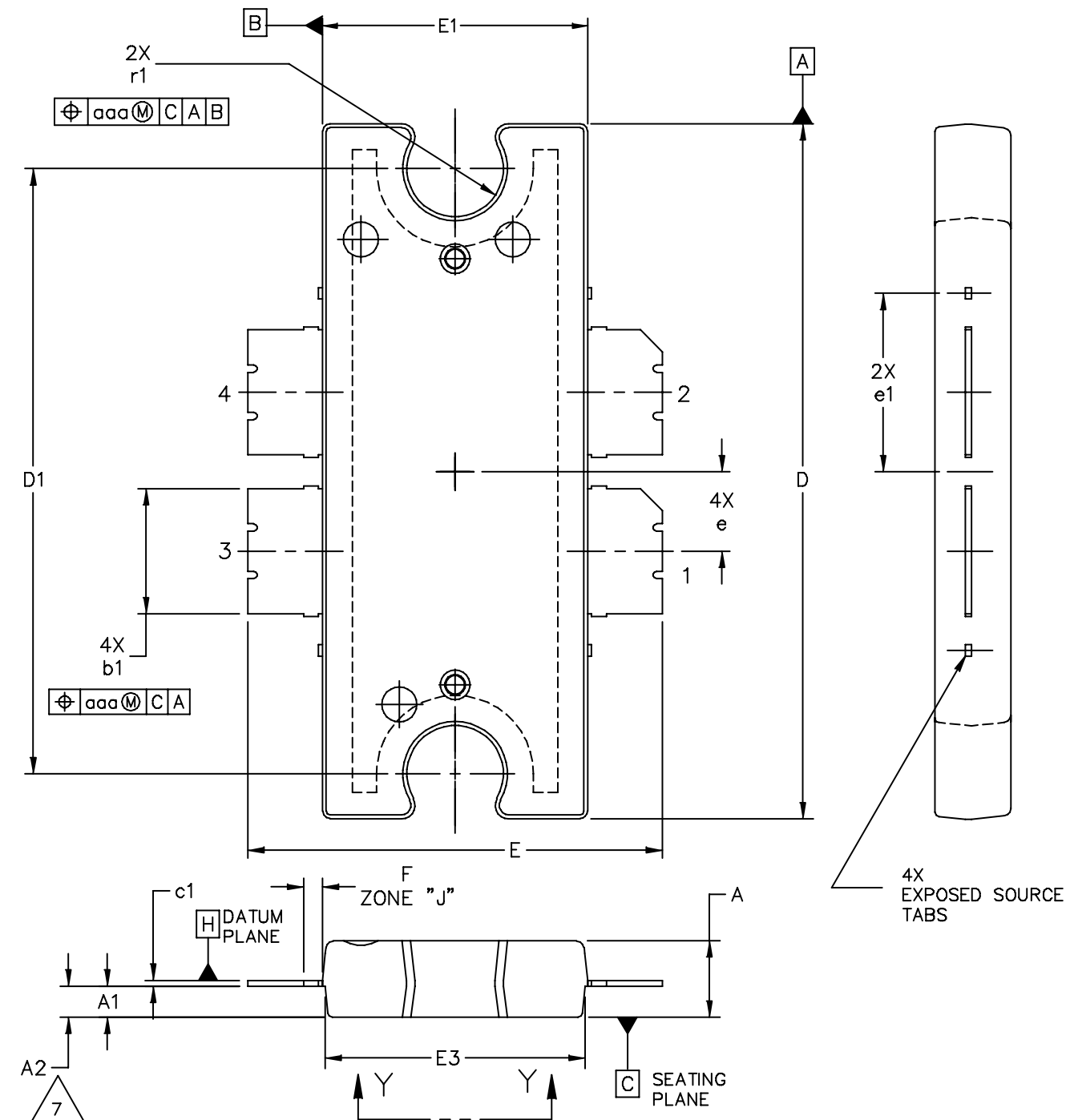
NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

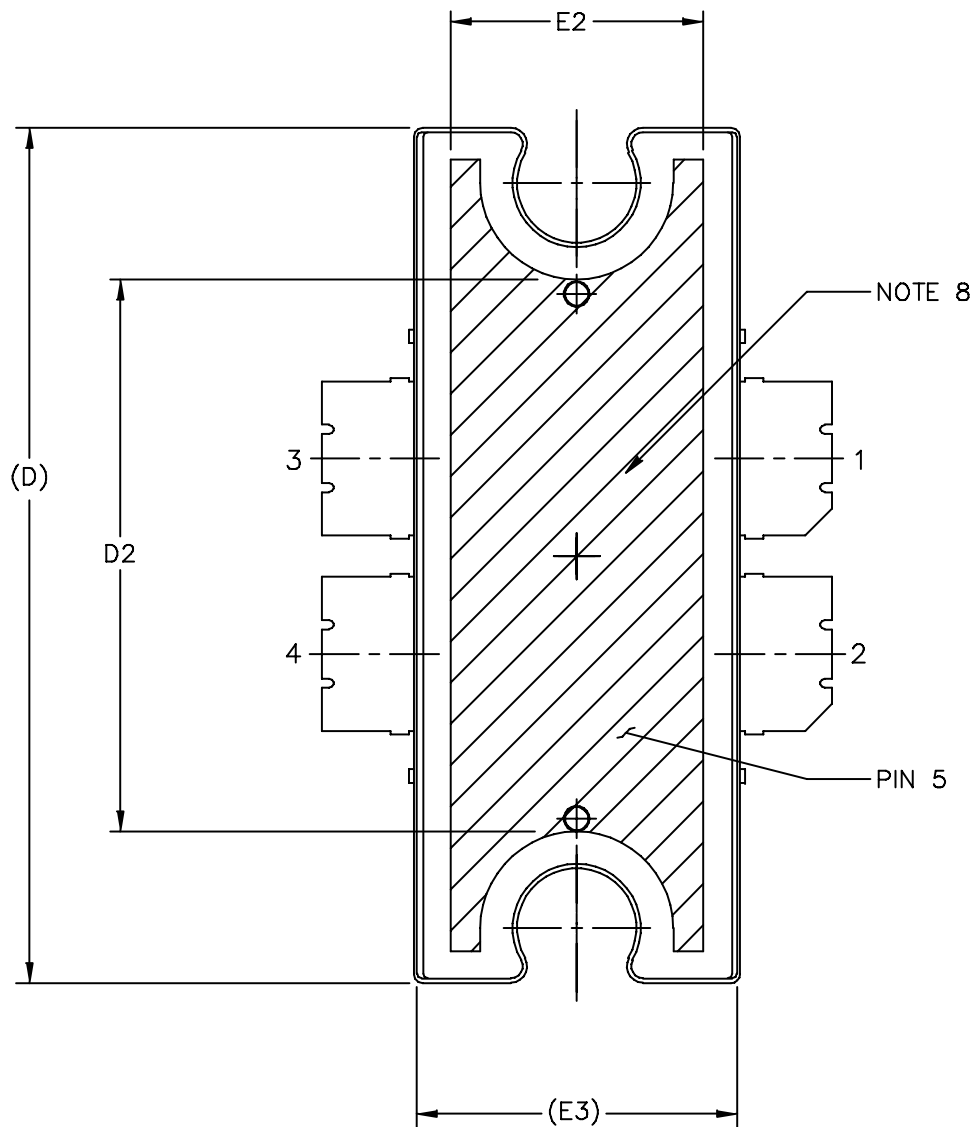
STYLE 1:

PIN 1 - DRAIN PIN 2 - DRAIN
 PIN 3 - GATE PIN 4 - GATE
 PIN 5 - SOURCE

INCH			MILLIMETER		INCH			MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b1	.164	.170	4.17	4.32
A2	.040	.042	1.02	1.07	c1	.007	.011	.18	.28
D	.712	.720	18.08	18.29	e	.106 BSC		2.69 BSC	
D1	.688	.692	17.48	17.58	aaa	.004		.10	
D2	.011	.019	0.28	0.48					
D3	.600	---	15.24	---					
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07					
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35					
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					
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		CASE NUMBER: 1484-04	31 AUG 2007
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		CASE NUMBER: 1484-04	31 AUG 2007
		STANDARD: NON-JEDEC	

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6. DATUM A AND B TO BE DETERMINED AT DATUM PLANE H.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

STYLE 1:
 PIN 1 - DRAIN PIN 2 - DRAIN
 PIN 3 - GATE PIN 4 - GATE
 PIN 5 - SOURCE

INCH			MILLIMETER		INCH			MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	b1	.164	.170	4.17	4.32
A1	.039	.043	0.99	1.09	c1	.007	.011	.18	.28
A2	.040	.042	1.02	1.07	r1	.063	.068	1.60	1.73
D	.928	.932	23.57	23.67	e	.106 BSC		2.69 BSC	
D1	.810 BSC		20.57 BSC		e1	.239 INFO ONLY		6.07 INFO ONLY	
D2	.600	---	15.24	---	aaa	.004		.10	
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07					
E2	.270	---	6.86	---					
E3	.346	.350	8.79	8.89					
F	.025 BSC		0.64 BSC						
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					CASE NUMBER: 1484-04			31 AUG 2007	
					STANDARD: NON-JEDEC				

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Feb. 2007	• Initial Release of Data Sheet
1	Feb. 2007	• Added Fig. 1, Pin Connections, p. 1 • Removed footnote references listed for Operating Junction Temperature, Table 1, Maximum Ratings, p. 1 • Added Max value to Power Gain, Table 5, Functional Tests, p. 2
2	May 2007	• Corrected Test Circuit Component part numbers in Table 6, Component Designations and Values for C4, C19, C5, C18, C9, C12, C14, and C23, p. 3
3	Jan. 2008	• Increased operating frequency to 600 MHz, p. 1 • Added Case Operating Temperature limit to the Maximum Ratings table and set limit to 150°C, p. 1 • Corrected C_{iss} test condition to indicate AC stimulus on the V_{GS} connection versus the V_{DS} connection, Dynamic Characteristics table, p. 2 • Updated PCB information to show more specific material details, Fig. 2, Test Circuit Schematic, p. 3 • Replaced Case Outline 1486-03, Issue C, with 1486-03, Issue D, p. 9-11. Added pin numbers 1 through 4 on Sheet 1. • Replaced Case Outline 1484-04, Issue D, with 1484-04, Issue E, p. 12-14. Added pin numbers 1 through 4 on Sheet 1, replacing Gate and Drain notations with Pin 1 and Pin 2 designations.

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Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
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Asia/Pacific:

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