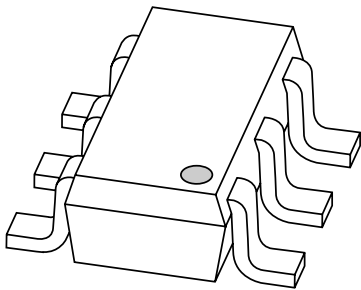


# DATA SHEET



**PBSS4240DPN**  
40 V low  $V_{CEsat}$  NPN/PNP  
transistor

Product data sheet

2003 Feb 20

# 40 V low $V_{CEsat}$ NPN/PNP transistor

# PBSS4240DPN

### FEATURES

- Low collector-emitter saturation voltage  $V_{CEsat}$
- High collector current capability  $I_C$  and  $I_{CM}$
- High collector current gain  $h_{FE}$  at high  $I_C$
- High efficiency leading to reduced heat generation
- Reduced printed-circuit board area requirements.

### APPLICATIONS

- Power management:
  - Complementary MOSFET driver
  - Dual supply line switching.
- Peripheral driver:
  - Half and full bridge motor drivers
  - Multi-phase stepper motor driver.

### DESCRIPTION

NPN/PNP low  $V_{CEsat}$  transistor pair in a SOT457 (SC-74) plastic package.

### MARKING

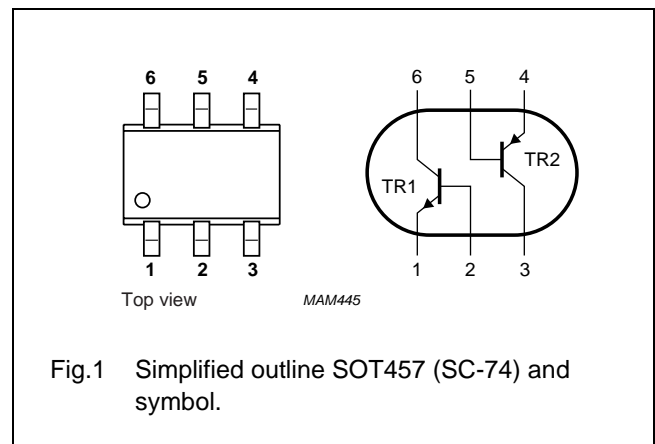
TYPE NUMBER	MARKING CODE
PBSS4240DPN	M3

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.		UNIT
		NPN	PNP	
$V_{CEO}$	emitter-collector voltage	40	-40	V
$I_C$	collector current (DC)	1.35	-1.1	A
$I_{CRP}$	repetitive peak collector current	2	-2	A
$I_{CM}$	peak collector current	3	-3	A
$R_{CEsat}$	equivalent on-resistance	200	260	$m\Omega$

### PINNING

PIN	DESCRIPTION
1, 4	emitter TR1; TR2
2, 5	base TR1; TR2
6, 3	collector TR1; TR2



40 V low  $V_{CEsat}$  NPN/PNP transistor

## PBSS4240DPN

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
<b>Per transistor unless otherwise specified; for the PNP transistor with negative polarity</b>					
$V_{CBO}$	collector-base voltage	open emitter	–	40	V
$V_{CEO}$	collector-emitter voltage	open base	–	40	V
$V_{EBO}$	emitter-base voltage	open collector	–	5	V
$I_C$	collector current (DC) NPN PNP		–	1.35	A
			–	–1.1	A
			–		
$I_{CRP}$	repetitive peak collector current	note 1	–	2	A
$I_{CM}$	peak collector current	single peak	–	3	A
$I_B$	base current (DC)		–	300	mA
$I_{BM}$	peak base current		–	1	A
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ °C}$ ; note 2	–	370	mW
		$T_{amb} \leq 25\text{ °C}$ ; note 3	–	310	mW
		$T_{amb} \leq 25\text{ °C}$ ; note 1	–	1.1	W
$T_{stg}$	storage temperature		–65	+150	°C
$T_j$	junction temperature		–	150	°C
$T_{amb}$	operating ambient temperature		–65	+150	°C
<b>Per device</b>					
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ °C}$ ; note 2	–	600	mW

**Notes**

- Operated under pulsed conditions: duty cycle  $\delta \leq 20\%$ ; pulse width  $t_p \leq 10\text{ ms}$ ; mounting pad for collector standard footprint.
- Device mounted on a printed-circuit board; single-sided copper; tinplated; mounting pad for collector  $1\text{ cm}^2$ .
- Device mounted on a printed-circuit board; single-sided copper; tinplated; standard footprint.

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
<b>Per transistor</b>				
$R_{th\ j-a}$	thermal resistance from junction to ambient	in free air; note 1	340	K/W
		in free air; note 2	110	K/W

**Notes**

- Device mounted on a printed-circuit board, single-sided copper, tinplated, mounting pad for collector  $1\text{ cm}^2$ .
- Operated under pulsed conditions: pulse width  $t_p \leq 10\text{ ms}$ ; duty cycle  $\delta \leq 0.20$ ; mounting pad for collector standard footprint.

40 V low  $V_{CEsat}$  NPN/PNP transistor

## PBSS4240DPN

**CHARACTERISTICS**

$T_{amb} = 25\text{ °C}$  unless otherwise specified.

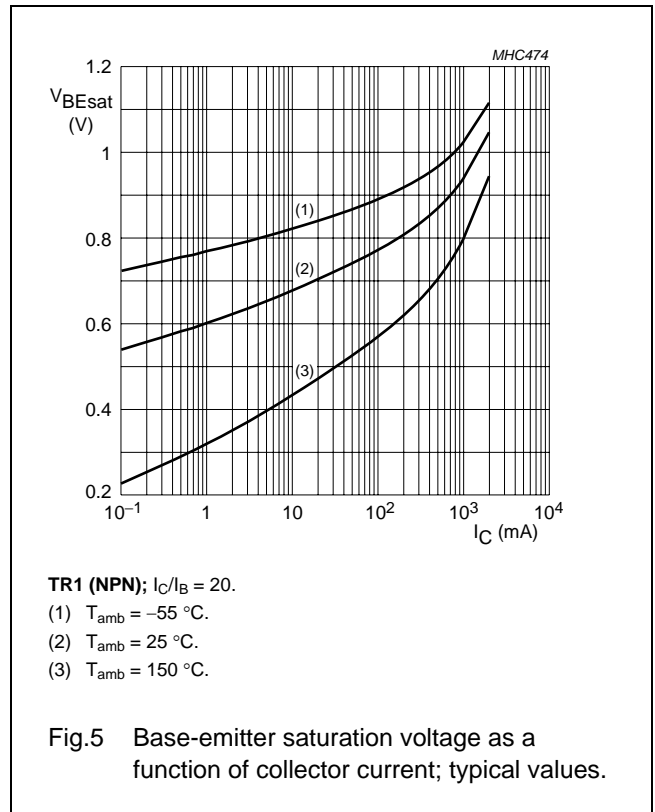
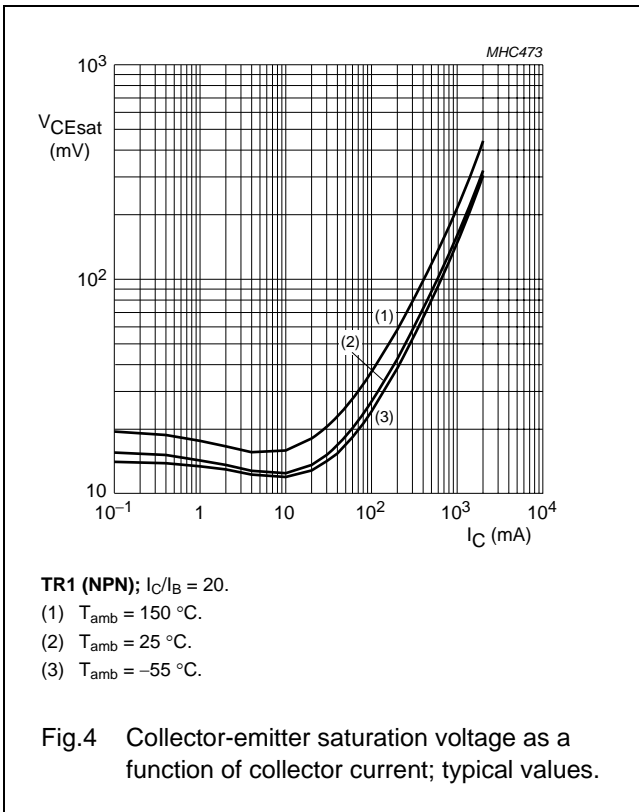
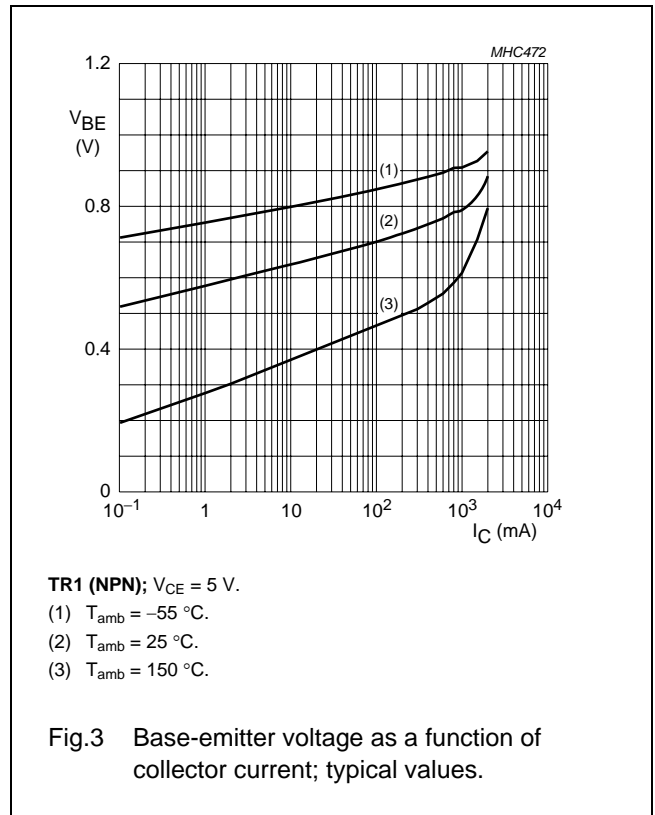
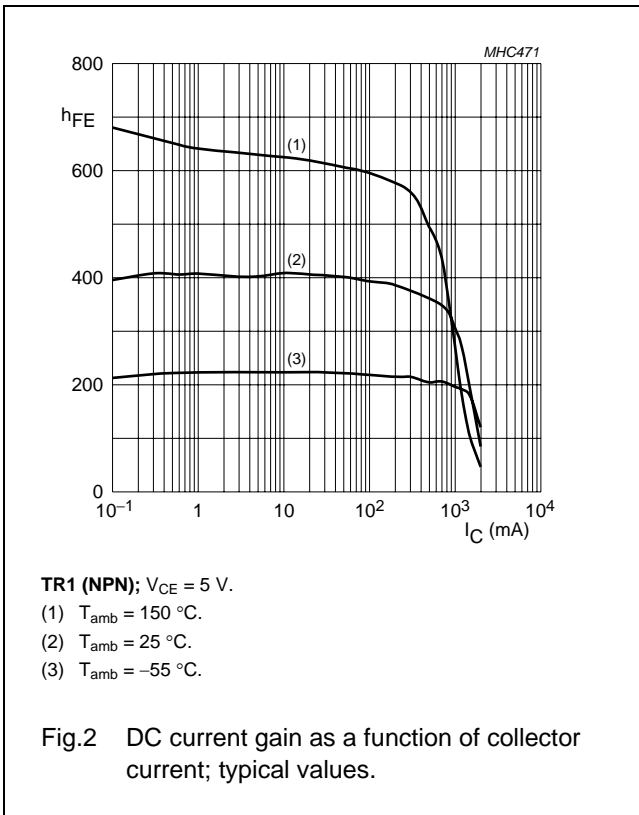
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Per transistor unless otherwise specified; for the PNP transistor with negative polarity</b>						
$I_{CBO}$	collector-base cut-off current	$V_{CB} = 40\text{ V}; I_E = 0$	–	–	100	nA
		$V_{CB} = 40\text{ V}; I_E = 0; T_j = 150\text{ °C}$	–	–	50	$\mu\text{A}$
$I_{CEO}$	collector-emitter cut-off current	$V_{CE} = 30\text{ V}; I_B = 0$	–	–	100	nA
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = 5\text{ V}; I_C = 0$	–	–	100	nA
$h_{FE}$	DC current gain	$V_{CE} = 5\text{ V}; I_C = 1\text{ mA}$	300	–	–	
$f_T$	transition frequency	$I_C = 50\text{ mA}; V_{CE} = 10\text{ V};$ $f = 100\text{ MHz}$	150	–	–	MHz
$C_c$	collector capacitance	$V_{CB} = 10\text{ V}; I_E = I_e = 0;$ $f = 1\text{ MHz}$	–	–	12	pF
<b>TR1 (NPN)</b>						
$h_{FE}$	DC current gain	$V_{CE} = 5\text{ V}; I_C = 500\text{ mA}$	300	–	900	
		$V_{CE} = 5\text{ V}; I_C = 1\text{ A}$	200	–	–	
		$V_{CE} = 5\text{ V}; I_C = 2\text{ A};$ note 1	75	–	–	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = 100\text{ mA}; I_B = 1\text{ mA}$	–	60	75	mV
		$I_C = 500\text{ mA}; I_B = 50\text{ mA}$	–	80	100	mV
		$I_C = 1\text{ A}; I_B = 100\text{ mA}$	–	150	200	mV
		$I_C = 2\text{ A}; I_B = 200\text{ mA};$ note 1	–	300	400	mV
$V_{BEsat}$	base-emitter saturation voltage	$I_C = 1\text{ A}; I_B = 100\text{ mA}$	–	–	1.2	V
$V_{BEon}$	base-emitter turn-on voltage	$V_{CE} = 5\text{ V}; I_C = 1\text{ A}$	–	–	1.1	V
$R_{CEsat}$	equivalent on-resistance	$I_C = 1\text{ A}; I_B = 100\text{ mA}$	–	–	200	$\text{m}\Omega$
<b>TR2 (PNP)</b>						
$h_{FE}$	DC current gain	$V_{CE} = -5\text{ V}; I_C = -100\text{ mA}$	300	–	800	
		$V_{CE} = -5\text{ V}; I_C = -500\text{ mA}$	250	–	–	
		$V_{CE} = -5\text{ V}; I_C = -1\text{ A}$	160	–	–	
		$V_{CE} = -5\text{ V}; I_C = -2\text{ A};$ note 1	50	–	–	
$V_{CEsat}$	saturation voltage	$I_C = -100\text{ mA}; I_B = -1\text{ mA}$	–	-90	-120	mV
		$I_C = -500\text{ mA}; I_B = -50\text{ mA}$	–	-100	-145	mV
		$I_C = -1\text{ A}; I_B = -100\text{ mA}$	–	-180	-260	mV
		$I_C = -2\text{ A}; I_B = -200\text{ mA};$ note 1	–	-400	-530	mV
$V_{BEsat}$	saturation voltage	$I_C = -1\text{ A}; I_B = -50\text{ mA}$	–	–	-1.1	V
$V_{BEon}$	base-emitter turn-on voltage	$V_{CE} = -5\text{ V}; I_C = -1\text{ A}$	–	–	-1	V
$R_{CEsat}$	equivalent on-resistance	$I_C = -1\text{ A}; I_B = -100\text{ mA};$ note 1	–	–	260	$\text{m}\Omega$

**Note**

1. Pulse test:  $t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.02$ .

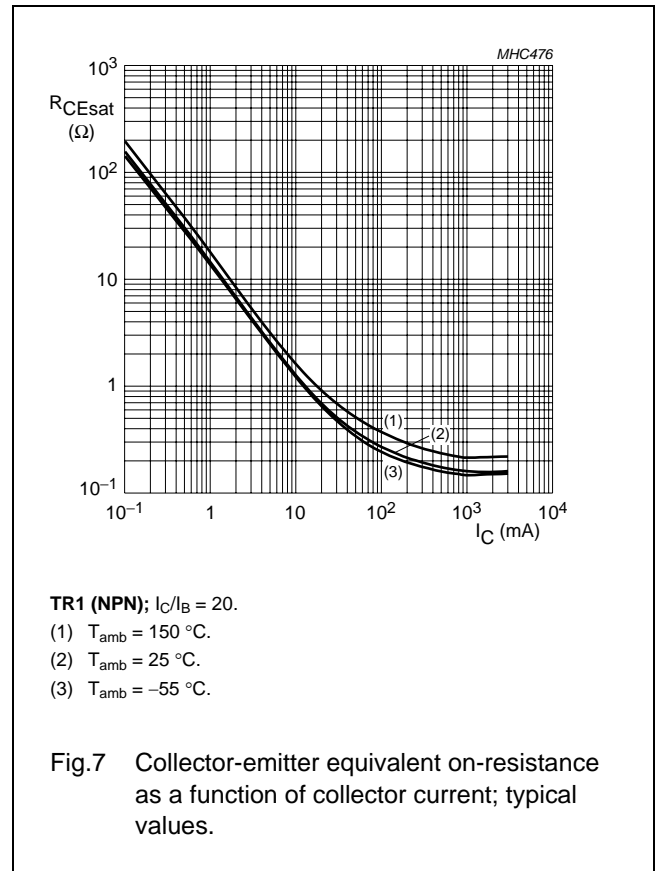
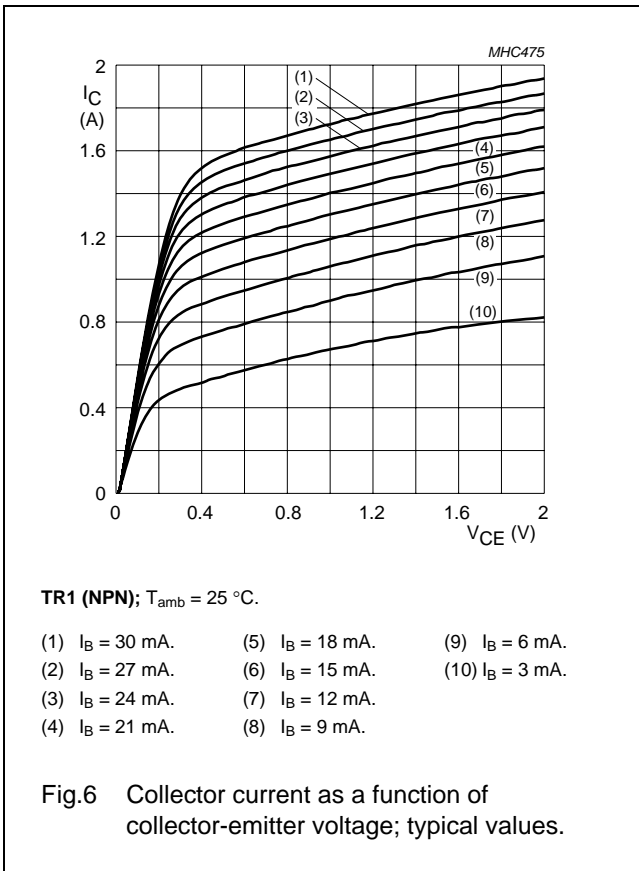
40 V low  $V_{CEsat}$  NPN/PNP transistor

PBSS4240DPN



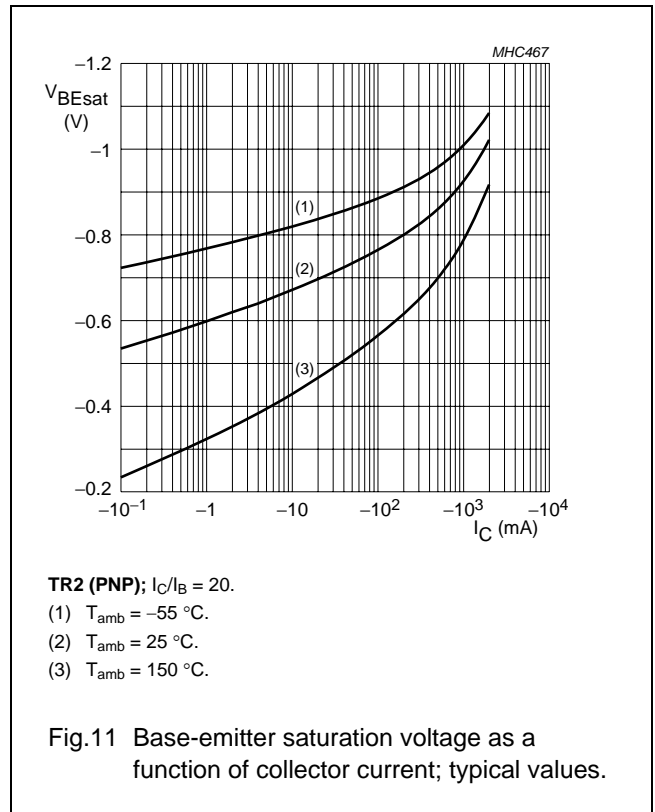
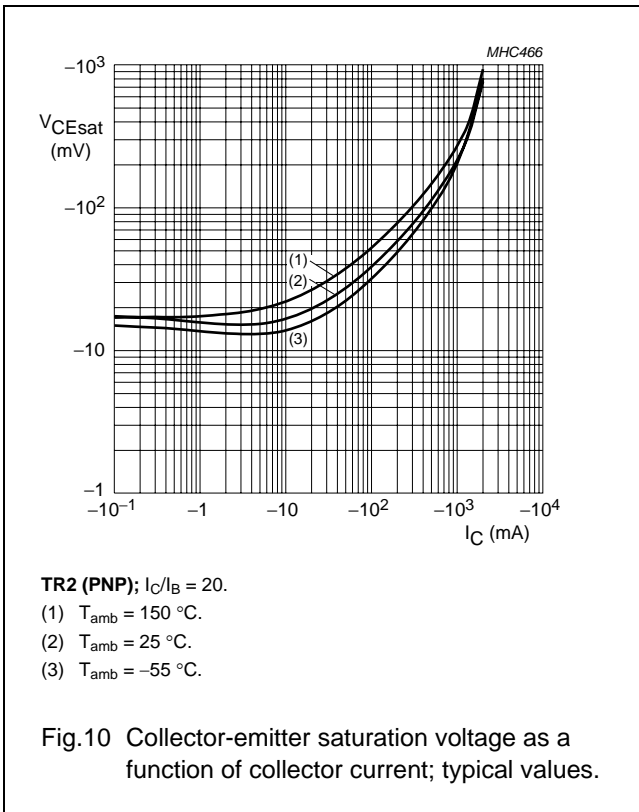
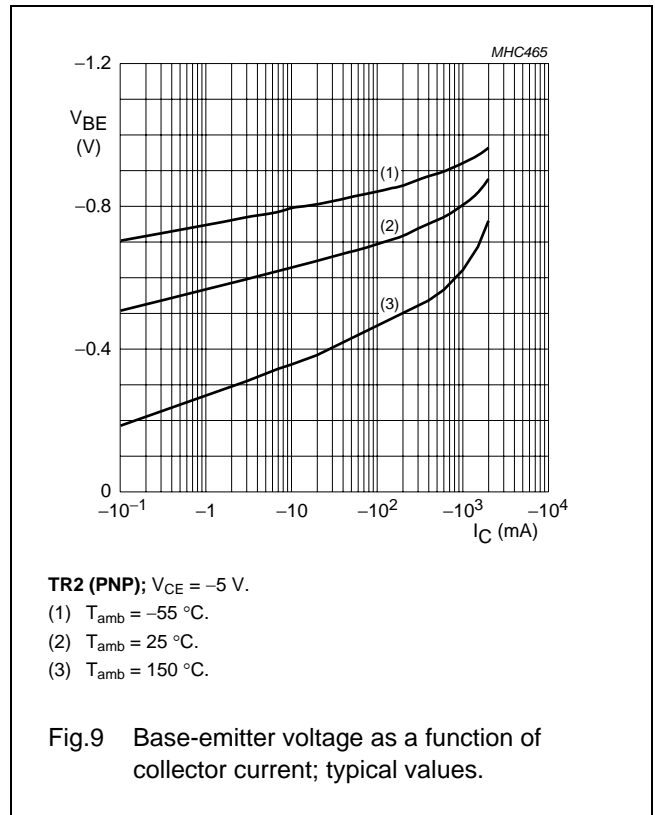
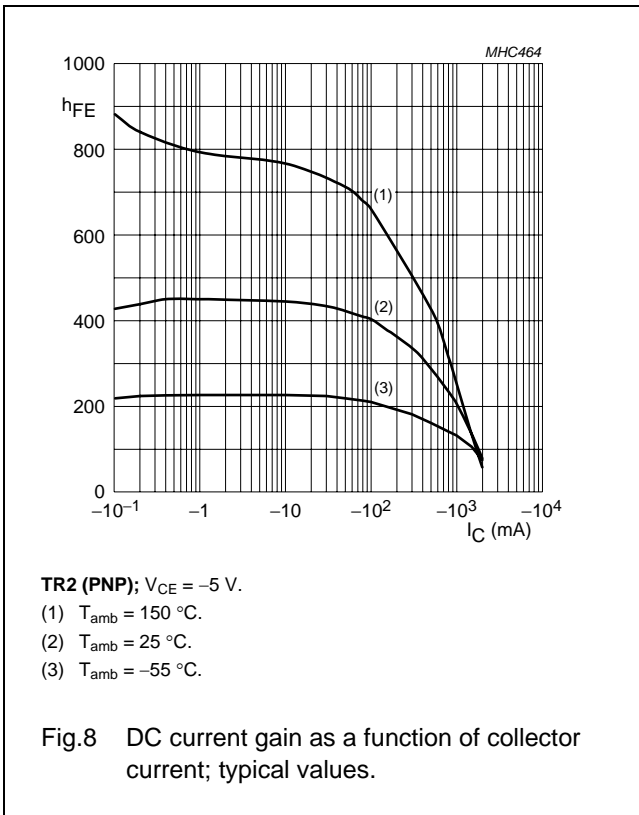
40 V low  $V_{CEsat}$  NPN/PNP transistor

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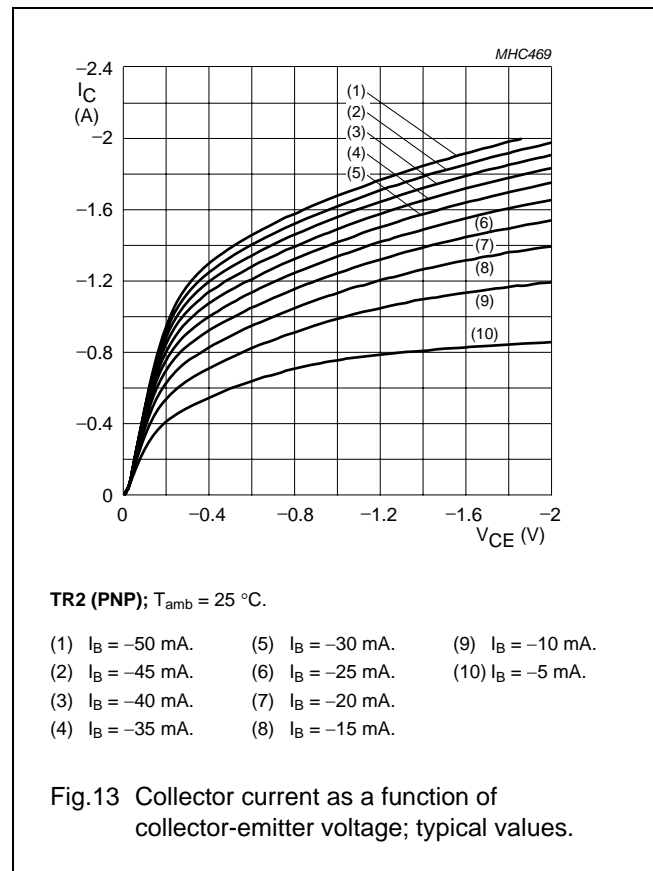
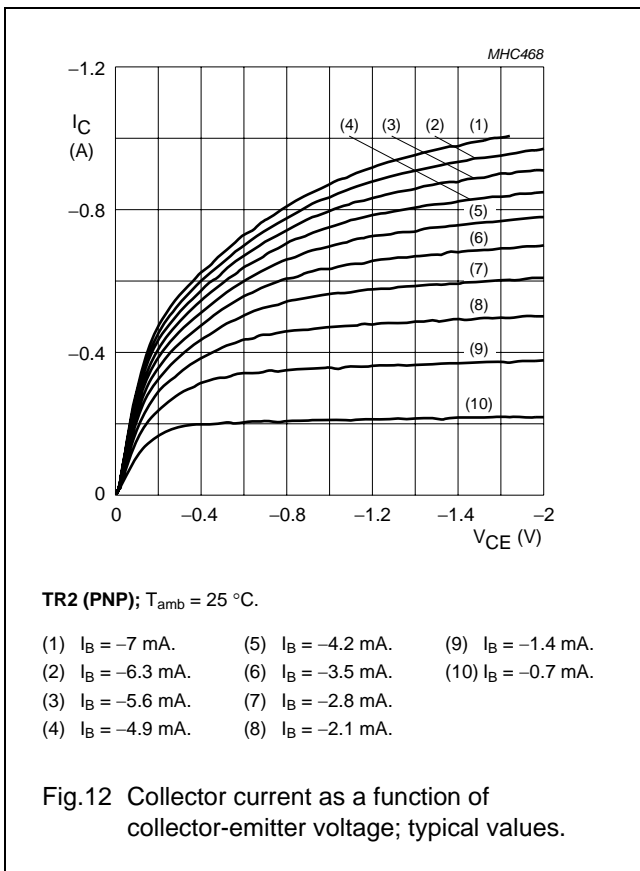
40 V low  $V_{CEsat}$  NPN/PNP transistor

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40 V low  $V_{CEsat}$  NPN/PNP transistor

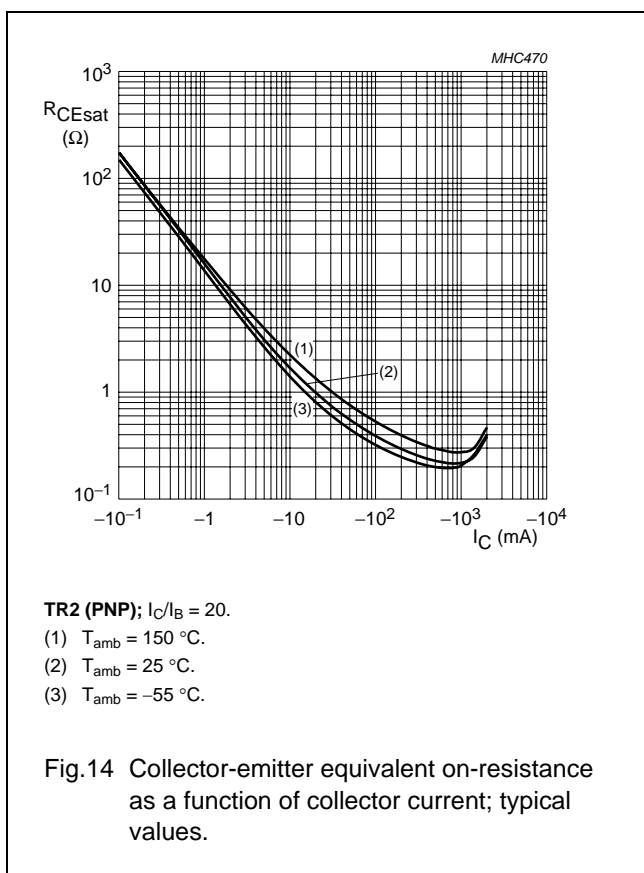
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40 V low  $V_{CEsat}$  NPN/PNP transistor

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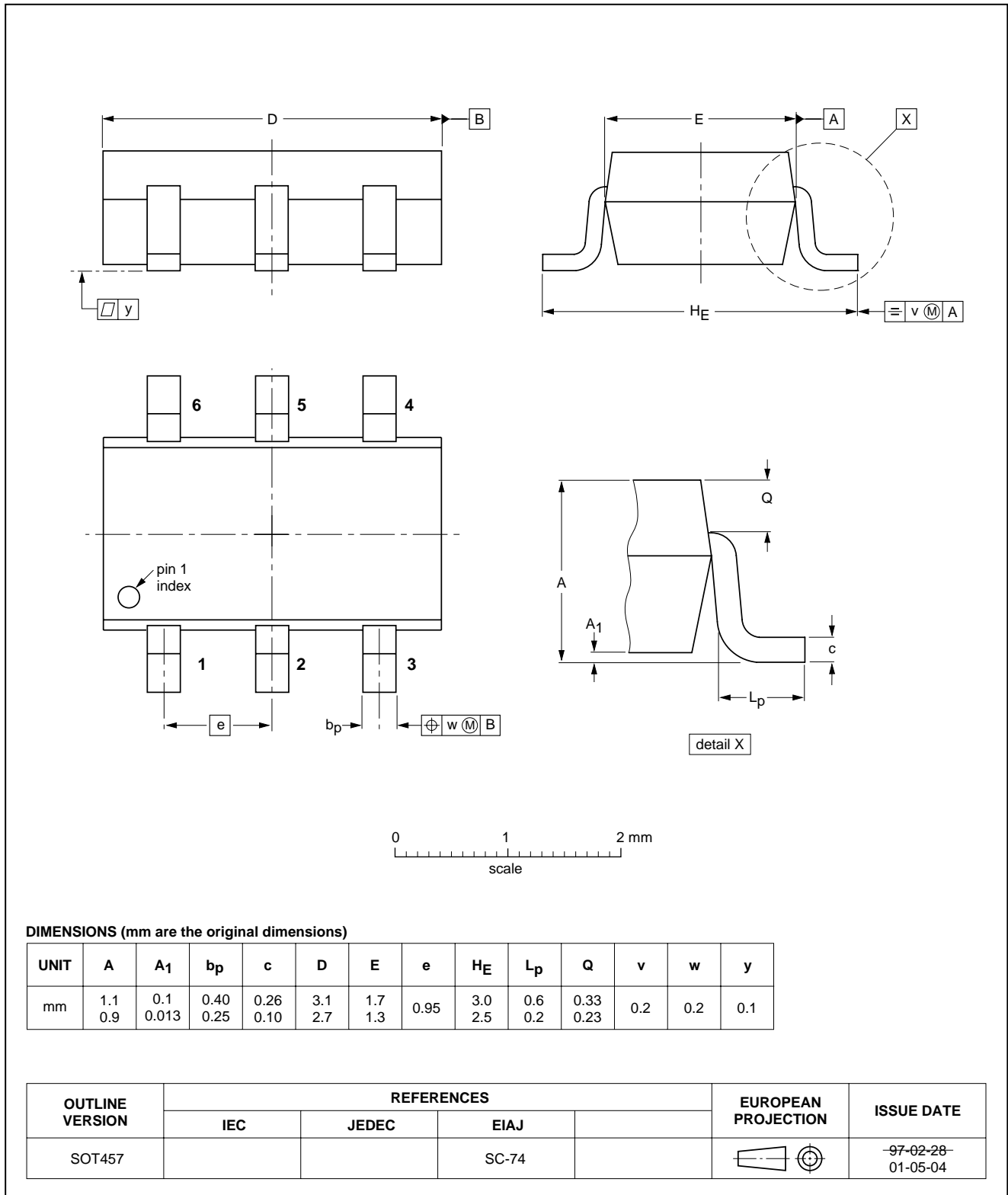
40 V low  $V_{CEsat}$  NPN/PNP transistor

PBSS4240DPN

PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT457



40 V low  $V_{CEsat}$  NPN/PNP transistor

PBSS4240DPN

**DATA SHEET STATUS**

DOCUMENT STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITION
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Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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