

# RJE0605JPD

Silicon P Channel MOS FET Series  
Power Switching

REJ03G1803-0100  
Rev.1.00  
Apr 01, 2010

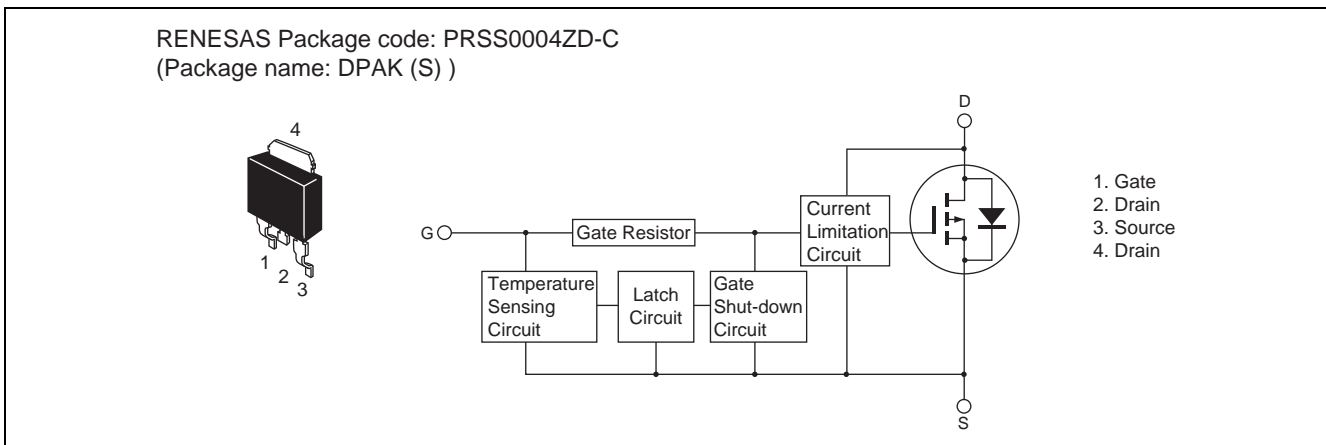
## Description

This FET has the over temperature shut-down capability sensing to the junction temperature. This FET has the built-in over temperature shut-down circuit in the gate area. And this circuit operation to shut-down the gate voltage in case of high junction temperature like applying over power consumption, over current etc..

## Features

- Logic level operation (–6 V Gate drive).
- Built-in the over temperature shut-down circuit.
- High endurance capability against to the short circuit.
- Latch type shut down operation (need 0 voltage recovery).
- Built-in the current limitation circuit.
- Low on-resistance  $R_{DS(on)}$ : 58 mΩ Typ, 75 mΩ Max ( $V_{GS} = -10$  V)

## Outline



## Absolute Maximum Ratings

( $T_a = 25^\circ\text{C}$ )

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	–60	V
Gate to source voltage	$V_{GSS}$	–16	V
Gate to source voltage	$V_{GSS}$	2.5	V
Drain current	$I_D$ <sup>Note 3</sup>	–10	A
Body-drain diode reverse drain current	$I_{DR}$ <sup>Note 2</sup>	–10	A
Avalanche current	$I_{AP}$ <sup>Note 2</sup>	–7	A
Avalanche energy	$E_{AR}$ <sup>Note 2</sup>	210	mJ
Channel dissipation	$P_{ch}$ <sup>Note 1</sup>	30	W
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	–55 +150	$^\circ\text{C}$

- Notes: 1. Value at  $T_c = 25^\circ\text{C}$   
 2.  $T_{ch} = 25^\circ\text{C}$ ,  $R_g \geq 50 \Omega$   
 3. It provides by the current limitation lower bound value.

## Typical Operation Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input voltage	V <sub>IH</sub>	-3.5	—	—	V	
	V <sub>IL</sub>	—	—	-1.2	V	
Input current (Gate non shut down)	I <sub>IH1</sub>	—	—	-100	μA	V <sub>i</sub> = -8 V, V <sub>DS</sub> = 0
	I <sub>IH2</sub>	—	—	-50	μA	V <sub>i</sub> = -3.5 V, V <sub>DS</sub> = 0
	I <sub>IL</sub>	—	—	-1	μA	V <sub>i</sub> = -1.2 V, V <sub>DS</sub> = 0
Input current (Gate shut down)	I <sub>IH(sd)1</sub>	—	-0.8	—	mA	V <sub>i</sub> = -8 V, V <sub>DS</sub> = 0
	I <sub>IH(sd)2</sub>	—	-0.35	—	mA	V <sub>i</sub> = -3.5 V, V <sub>DS</sub> = 0
Shut down temperature	T <sub>sd</sub>	—	175	—	°C	Channel temperature (dv/dt V <sub>GS</sub> ≥ 500 V/ms)
Gate operation voltage	V <sub>op</sub>	-3.5	—	-12	V	
Drain current (Current limitation value)	I <sub>D limit</sub>	-10	—	—	A	V <sub>GS</sub> = -12 V, V <sub>DS</sub> = -10 V <sup>Note 4</sup>

Notes; 4. Pulse test

## Electrical Characteristics

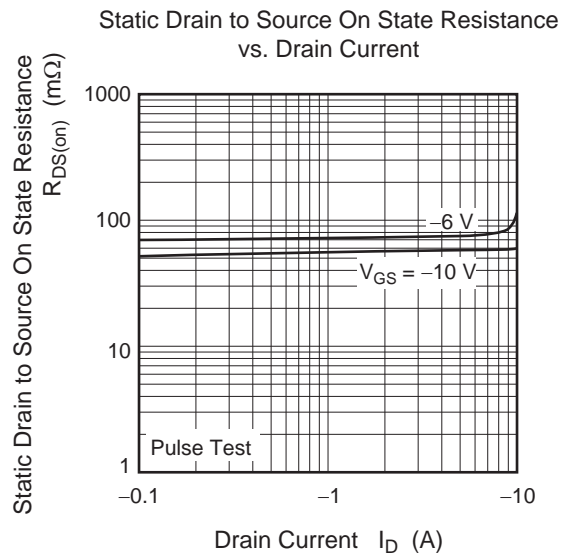
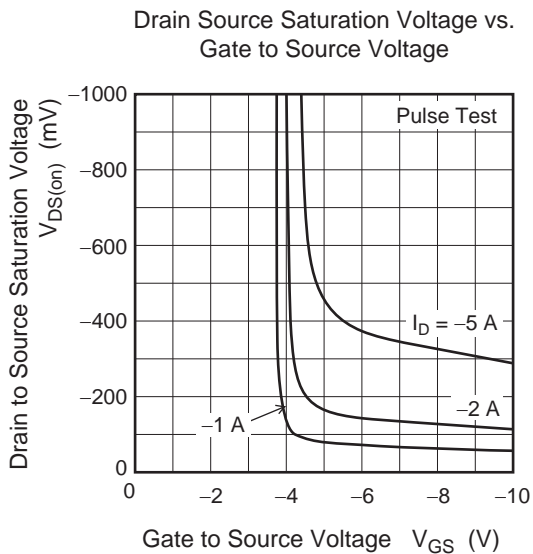
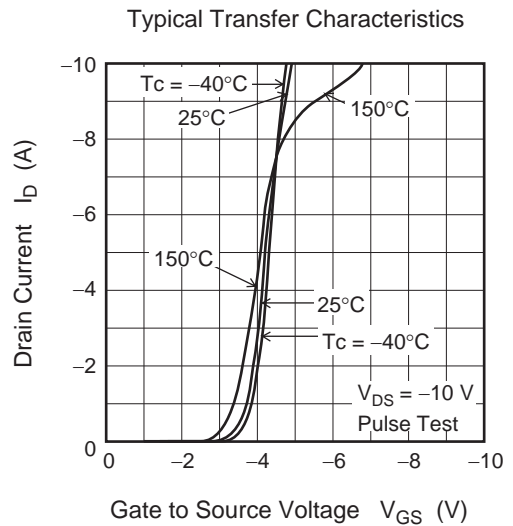
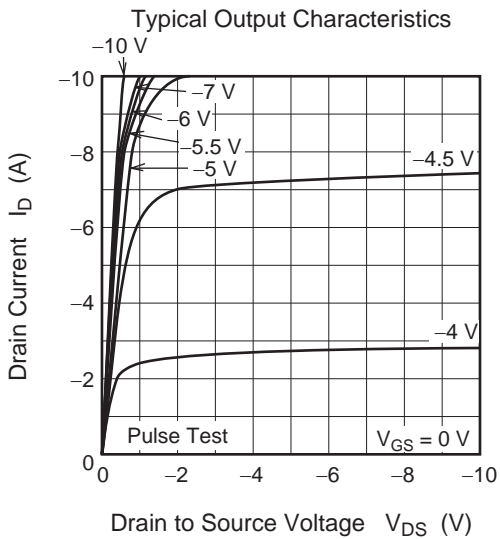
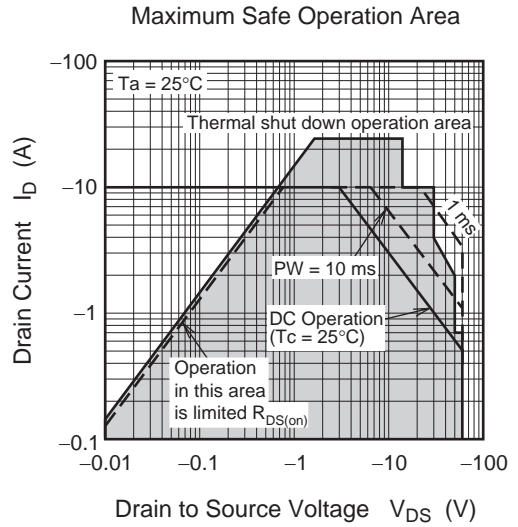
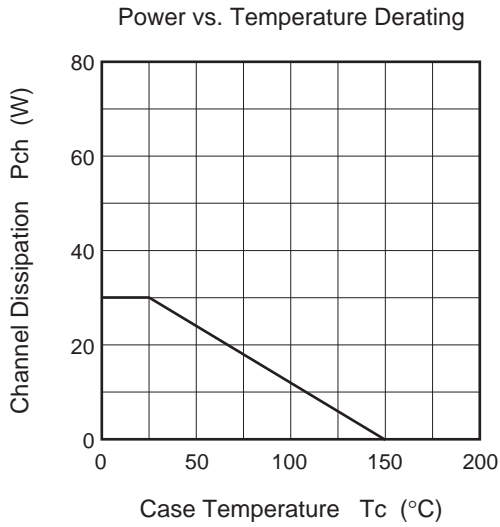
(Ta = 25°C)

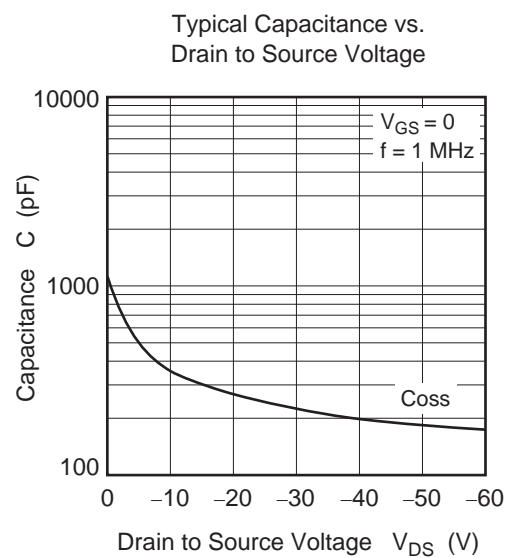
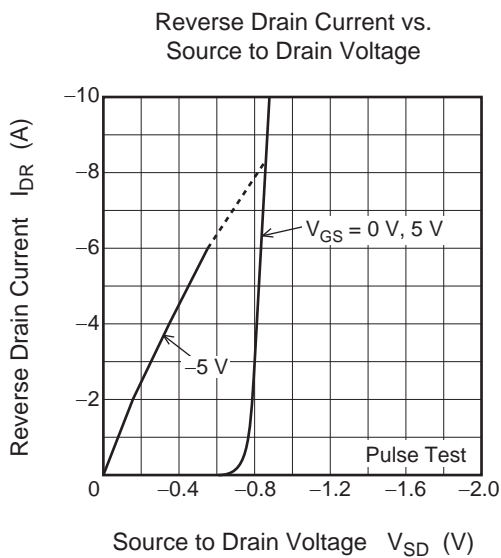
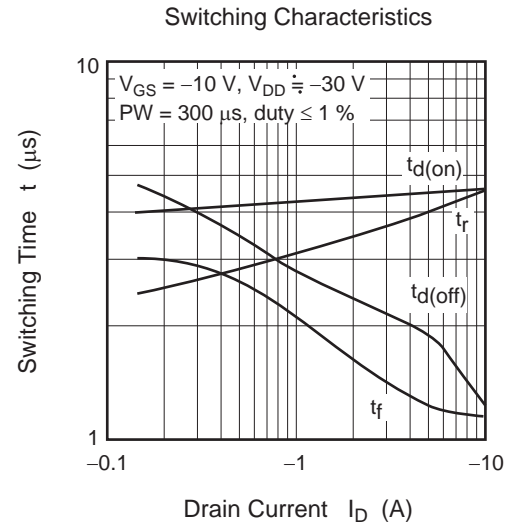
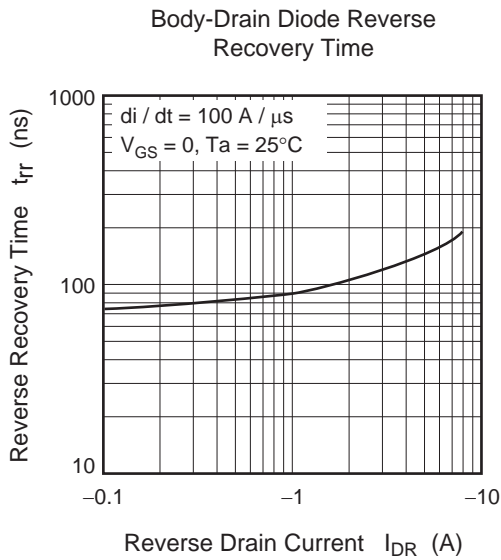
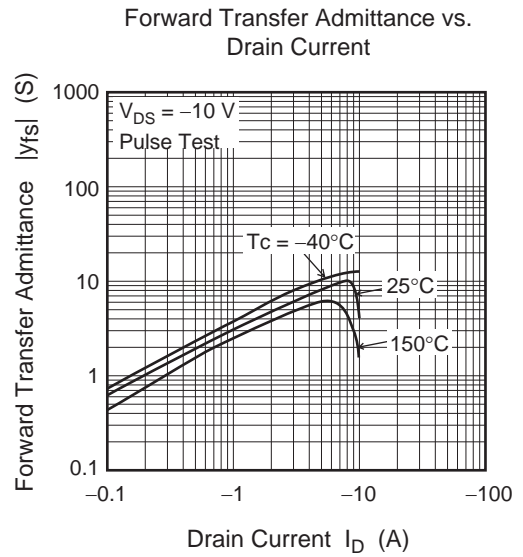
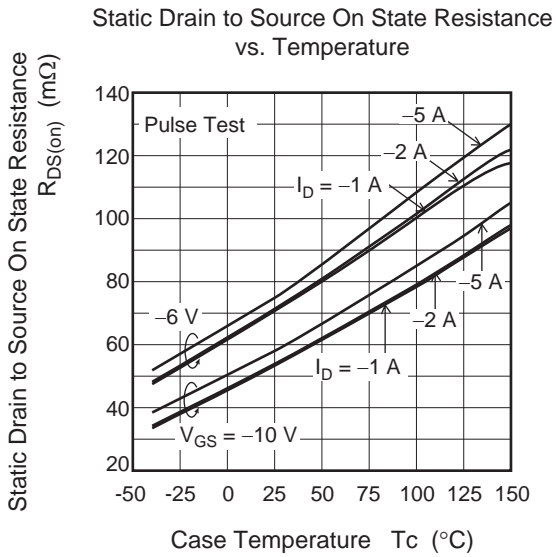
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain current	I <sub>D1</sub>	—	—	-4	A	V <sub>GS</sub> = -3.5 V, V <sub>DS</sub> = -10 V
	I <sub>D2</sub>	—	—	-10	mA	V <sub>GS</sub> = -1.2 V, V <sub>DS</sub> = -10 V
	I <sub>D3</sub>	-10	—	—	A	V <sub>GS</sub> = -12 V, V <sub>DS</sub> = -10 V <sup>Note 5</sup>
Drain to source breakdown voltage	V <sub>(BR)DSS</sub>	-60	—	—	V	I <sub>D</sub> = -10 mA, V <sub>GS</sub> = 0
Gate to source breakdown voltage	V <sub>(BR)GSS</sub>	-16	—	—	V	I <sub>G</sub> = -800 μA, V <sub>DS</sub> = 0
	V <sub>(BR)GSS</sub>	2.5	—	—	V	I <sub>G</sub> = 100 μA, V <sub>DS</sub> = 0
Gate to source leak current	I <sub>GSS1</sub>	—	—	-100	μA	V <sub>GS</sub> = -8 V, V <sub>DS</sub> = 0
	I <sub>GSS2</sub>	—	—	-50	μA	V <sub>GS</sub> = -3.5 V, V <sub>DS</sub> = 0
	I <sub>GSS3</sub>	—	—	-1	μA	V <sub>GS</sub> = -1.2 V, V <sub>DS</sub> = 0
	I <sub>GSS4</sub>	—	—	100	μA	V <sub>GS</sub> = 2.4 V, V <sub>DS</sub> = 0
Input current (shut down)	I <sub>GS(OP)1</sub>	—	-0.8	—	mA	V <sub>GS</sub> = -8 V, V <sub>DS</sub> = 0
	I <sub>GS(OP)2</sub>	—	-0.35	—	mA	V <sub>GS</sub> = -3.5 V, V <sub>DS</sub> = 0
Zero gate voltage drain current	I <sub>DSS</sub>	—	—	-10	μA	V <sub>DS</sub> = -60 V, V <sub>GS</sub> = 0
Gate to source cutoff voltage	V <sub>GS(off)</sub>	-2.2	—	-3.4	V	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1 mA
Forward transfer admittance	y <sub>fs</sub>	4	8	—	S	I <sub>D</sub> = -5 A, V <sub>DS</sub> = -10 V <sup>Note 5</sup>
Static drain to source on state resistance	R <sub>DS(on)</sub>	—	75	110	mΩ	I <sub>D</sub> = -5 A, V <sub>GS</sub> = -6 V <sup>Note 5</sup>
	R <sub>DS(on)</sub>	—	58	75	mΩ	I <sub>D</sub> = -5 A, V <sub>GS</sub> = -10 V <sup>Note 5</sup>
Output capacitance	C <sub>oss</sub>	—	355	—	pF	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = 0, f = 1MHz
Turn-on delay time	t <sub>d(on)</sub>	—	4.5	—	μs	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -5 A, R <sub>L</sub> = 6 Ω
Rise time	t <sub>r</sub>	—	4.0	—	μs	
Turn-off delay time	t <sub>d(off)</sub>	—	1.8	—	μs	
Fall time	t <sub>f</sub>	—	1.3	—	μs	
Body-drain diode forward voltage	V <sub>DF</sub>	—	0.87	—	V	I <sub>F</sub> = -10 A, V <sub>GS</sub> = 0
Body-drain diode reverse recovery time	t <sub>rr</sub>	—	209	—	ns	I <sub>F</sub> = -10 A, V <sub>GS</sub> = 0 di <sub>F</sub> /dt = 50 A/μs
Over load shut down operation time <sup>Note 6</sup>	t <sub>os1</sub>	—	2.3	—	ms	V <sub>GS</sub> = -6 V, V <sub>DD</sub> = -16 V

Notes: 5. Pulse test

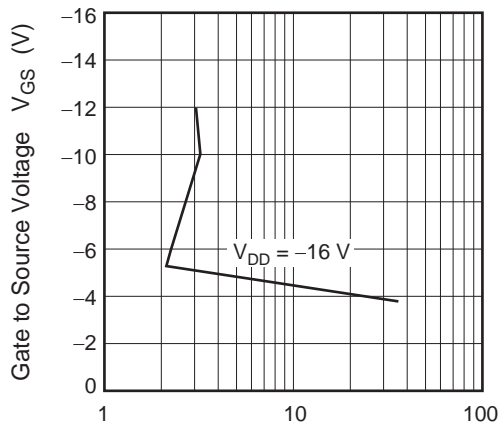
6. Including the junction temperature rise of the over loaded condition.

### Main Characteristics



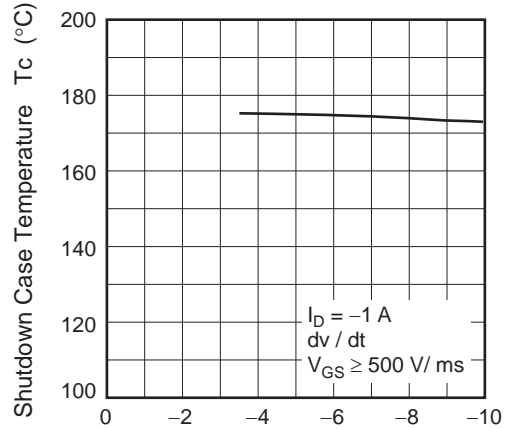


Gate to Source Voltage vs. Shutdown Time of Load-Short Test



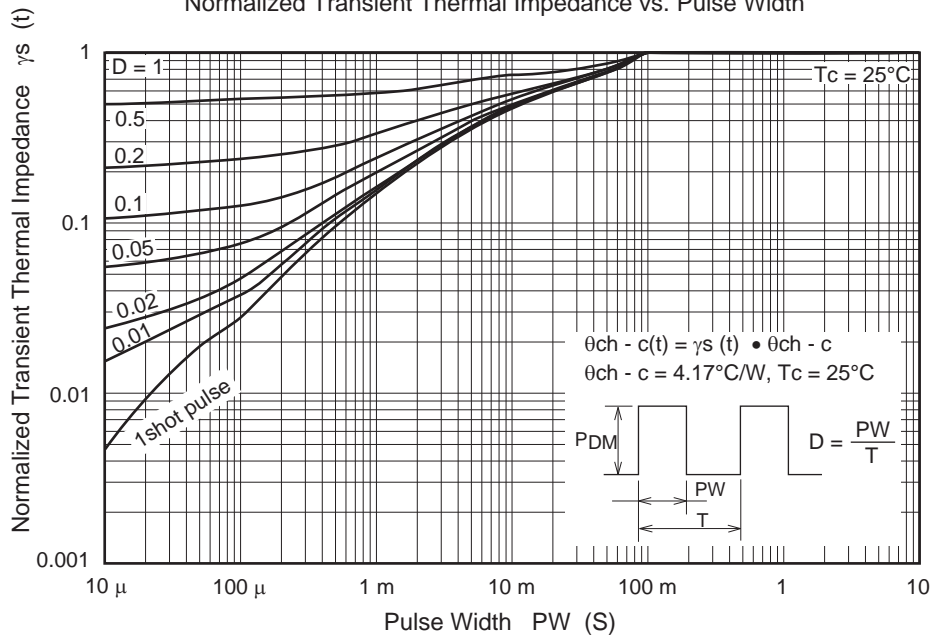
Shutdown Time of Load-Short Test  $P_w$  (ms)

Shutdown Case Temperature vs. Gate to Source Voltage

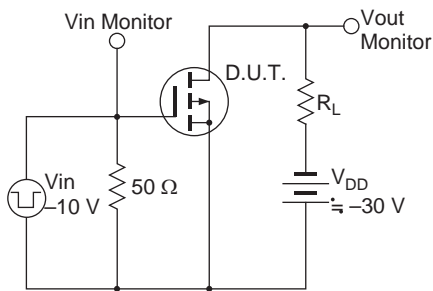


Gate to Source Voltage  $V_{GS}$  (V)

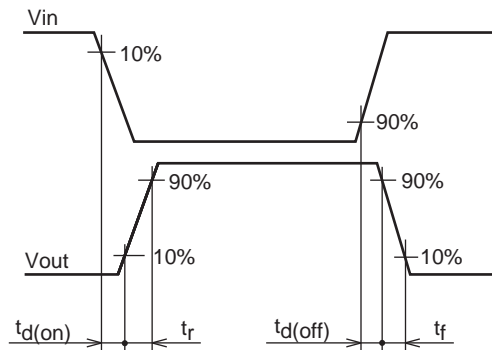
Normalized Transient Thermal Impedance vs. Pulse Width



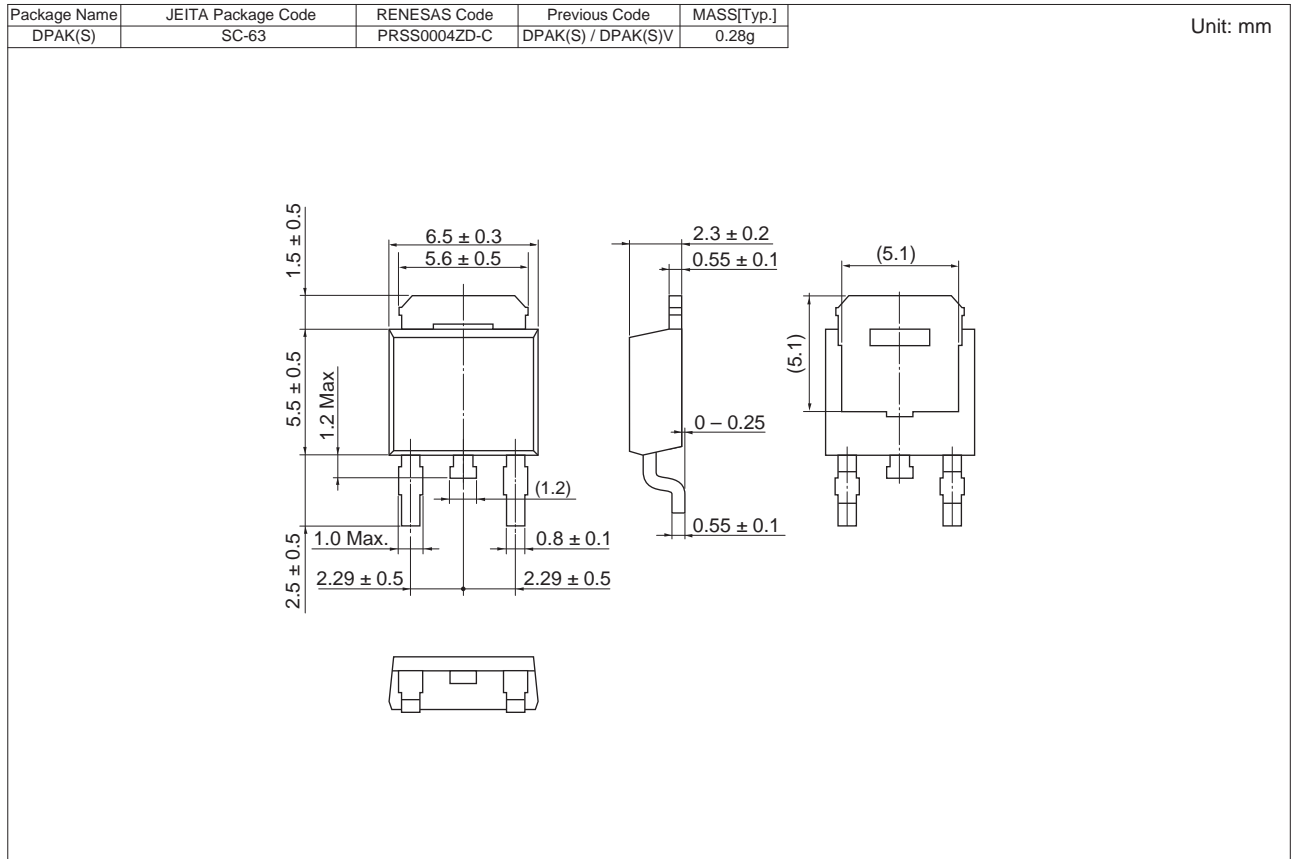
Switching Time Test Circuit



Waveform



### Package Dimensions



### Ordering Information

Part No.	Quantity	Shipping Container
RJE0605JPD-00-J3	3000 pcs	Taping (Sinistrorse)

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