Description

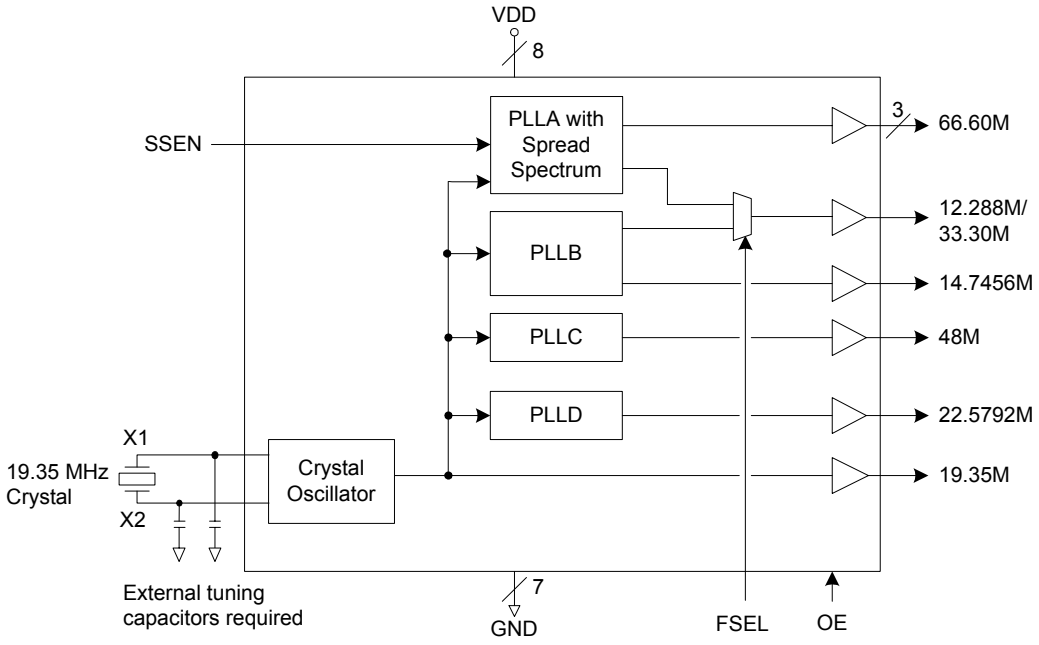
The ICS1493A-19 is a low cost frequency generator used for automotive application. Using patented Phase-Locked-Loop (PLL) techniques, the device uses a 19.35 MHz fundamental crystal source to produce seven clock outputs and one reference clock output. The output clocks are at 12.288 MHz, 14.7456 MHz, 22.5792 MHz, 48 MHz, 66.60 MHz, and 33.30 MHz with a 19.35 MHz reference clock output. The 66.60 MHz and 33.30 MHz clocks have a spread select option. Operating voltage of the ICS1493A-19 is 3.3 V.

ICS makes many frequency generators. Contact us for all of your clocking needs.

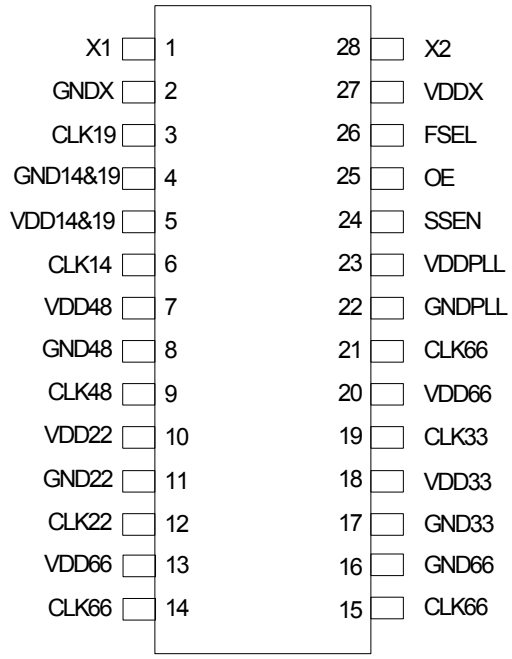
Features

- Packaged in 28-pin TSSOP (4.4mm body)
- Low power CMOS technology
- Input crystal frequency of 19.35 MHz
- 3.3 V operating voltage
- Seven output clocks: 12.288 /33.30 MHz, 14.7456 MHz, 22.5792 MHz, 48 MHz, 66.60 MHz (3 copies)
- One reference clock output at 19.35 MHz
- Spread select option on the 66.60 MHz clock (3 copies) and 33.30 MHz clock outputs
- Output enable pin stops clocks low (tri-state with weak pull-down resistors)
- Zero ppm synthesis error for 48 MHz, 19.35 MHz clocks; 0.5 ppm error for 12.288 MHz, 14.7456 MHz, 22.5792 MHz clocks; 1 ppm error for 66.60 MHz and 33.30 MHz clocks.
- Industrial temperature range (-40°C to +85°C)

Block Diagram



Pin Assignment



28-pin (173 mil) TSSOP

Spread Enable Table 1

SSEN	66.60/33.30 MHz Clock
0	No spread (default)
1	-1.0%

Output Enable Function Table 2

OE	Output Status
0	Stopped low
1	Running (default)

Frequency Select Table 3

FSEL	Clock Selected (MHz)
0	12.288
1	33.30 (default)

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1	Input	Crystal connection. Connect to a 19.35 MHz fundamental crystal.
2	GNDX	Power	Crystal oscillator circuit ground.
3	CLK19	Output	19.35 MHz reference clock output. Internal weak pull-down resistor.
4	GND14&19	Power	Connect to 14.7456 MHz and 19.35 MHz clock output ground.
5	VDD14&19	Power	Output driver power for 14.7456 MHz clock output.
6	CLK14	Output	14.7456 MHz clock output. Internal weak pull-down resistor.
7	VDD48	Power	Output driver power for 48 MHz clock output.
8	GND48	Power	Connect to 48 MHz clock output ground.
9	CLK48	Output	48 MHz clock output. Internal weak pull-down resistor.
10	VDD22	Power	Output driver power for 22.5792 MHz clock output.
11	GND22	Power	Connect to 22.5792 MHz clock output circuit ground.
12	CLK22	Output	22.5792 MHz clock output. Internal weak pull-down resistor.
13	VDD66	Power	Output driver power for 66.60 MHz clock output.
14	CLK66	Output	66.60 MHz clock output. Internal weak pull-down resistor.
15	CLK66	Output	66.60 MHz clock output. Internal weak pull-down resistor.

Pin Number	Pin Name	Pin Type	Pin Description
16	GND66	Power	Connect to 66.60 MHz clock output circuit ground.
17	GND33	Power	Connect to 33.30 MHz clock output circuit ground.
18	VDD33	Power	Output driver power for 33.30 MHz clock output.
19	CLK33 /12.288	Output	33.30 /12.288 MHz clock output. Internal weak pull-down resistor.
20	VDD66	Power	Output driver power for 66.60 MHz clock output.
21	CLK66	Output	66.60 MHz clock output. Internal weak pull-down resistor.
22	GNDPLL	Power	Connect to PLL circuit ground.
23	VDDPLL	Power	VDD for PLL circuits Connect to 3.3 V.
24	SSEN	Input	Spread enable pin for 66.60 MHz clock. See table 1 above. Internal pull-down resistor.
25	OE	Input	Enables output when =1 and disables (pulled low) when =0. See table above 2. Internal pull-up resistor.
26	FSEL	Input	Frequency select pin, internal pull-up. See Table 3.
27	VDDX	Power	VDD for crystal oscillator circuit. Connect to 3.3.V.
28	X2	Input	Crystal connection. Connect to a 19.35 MHz fundamental crystal.

External Components

Decoupling Capacitor

As with any high-performance mixed-signal IC, the ICS1493A-19 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01µF must be connected between each VDD and the PCB ground plane.

Series Termination Resistor

Clock output traces should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

Crystal Load Capacitors

The device crystal connections should include pads for capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance.

The value (in pF) of these crystal caps should equal (C_L - 6 pF)*2. In this equation, C_L= crystal load capacitance in pF. Example: For a crystal with a 16 pF load capacitance, each crystal capacitor would be 20 pF [(16-6) x 2 = 20 pF].

PCB Layout Recommendations

Observe the following guidelines for optimum device performance and lowest output phase noise:

1) The 0.01µF decoupling capacitors should be mounted on the component side of the board as close to the VDD pins as possible. No vias should be used between the decoupling capacitors and VDD pins. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via.

2) The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces. Instead, they should be separated and away from other traces.

3) Place the 33Ω series termination resistor (if needed) close to the clock output to minimize EMI.

4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the ICS1493A-19. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS1493A-19. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	-0.5 V to 7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	-40 to +85° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-40		+85	° C
Power Supply Voltage (measured in respect to GND)	+3.0	+3.3	+3.6	V

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±10%**, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0	3.3	3.6	V
Supply Current	IDD	No load		80		mA
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Output High Voltage	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Short Circuit Current	I_{OS}	Clock outputs,15 and 21		±80		mA
Short Circuit Current	I_{OS}	Clock outputs 3, 6, 9, 12, 14, and 19		±70		mA
Input Capacitance	C_{IN}	Input		5		pF
Nominal Output Impedance	Z_{OUT}			20		Ω
Internal Pull-up Resistor	R_{PU}	FSEL, OE pins		200		kΩ

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Internal Pull-down Resistor	R_{Pd}	All clock outputs except SSEN pin		200		kΩ
		SSEN pin		100		kΩ

AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±10%**, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	f_{IN}			19.35		MHz
Output Rise Time	t_{OR}	20% to 80%, C_L=12 pF		1.1	1.5	ns
Output Fall Time	t_{OF}	80% to 20%, C_L=12 pF		1.1	1.5	ns
Output Clock Duty Cycle		at VDD/2, C_L=12 pF	45	50	55	%
		at VDD/2, Pin 3, C_L=12 pF	40	50	60	%
Output-to-Output Skew		Pins 14, 15, and 21 only			175	ps
Output Enable Time		OE going high to output valid			1	ms
Output Disable Time		OE going low to output Invalid			1	ms
Power-up Time		Power on to output valid			20	ms
Spread Modulation		Spread rate		32		kHz
Jitter, Cycle-to-cycle		All clocks except reference clock 19.35 MHz		300		ps
Jitter, Cycle-to-cycle		Reference clock 19.35 MHz		500		ps
Jitter, Peak-to-peak		Peak-to-peak, all clocks except reference clock 19.35 MHz		±150		ps
Jitter, Peak-to-peak		Peak-to-peak, reference clock 19.35 MHz		±250		ps
Output Frequency Synthesis Error		All clocks			10	ppm
Transition Time	t_{TR}	Measured from a change of FSEL until clock stable within ±1%		1		ms

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		83		°C/W
	θ_{JA}	1 m/s air flow		75		°C/W
	θ_{JA}	3 m/s air flow		61		°C/W
Thermal Resistance Junction to Case	θ_{JC}			60		°C/W

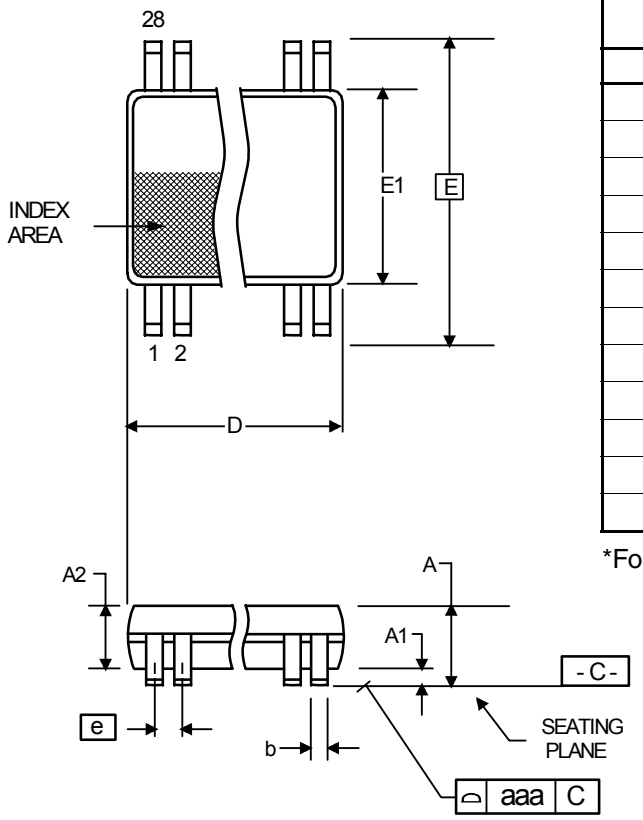
Marking Diagram

Notes:

1. ###### is the lot number.
2. YYWW is the last two digits of the year and week that the part was assembled.
3. “LF” denotes Pb (lead) free package.
4. Bottom marking: (origin)
   Origin = country of origin if not USA.

Package Outline and Package Dimensions (28-pin TSSOP, 4.4mm body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches*	
Symbol	Min	Max	Min	Max
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	9.60	9.80	0.378	0.386
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	0.018	0.030
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004

*For reference only. Controlling dimensions in mm.

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
ICS1493AGI-19LF	see page 7	Tubes	28-pin TSSOP	-40° to +85° C
ICS1493AGI-19LFT		Tape and Reel	28-pin TSSOP	-40° to +85° C

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.