

Comlinear[®] CLC1003

Low Distortion, Low Offset, RRIO Amplifier

FEATURES

- 1mV max input offset voltage
- 0.00005% THD at 1kHz
- 5.3nV/√Hz input voltage noise >10kHz
- -90dB/-85dB HD2/HD3 at 100kHz, $R_L=100\Omega$
- <-100dB HD2 and HD3 at 10kHz, $R_L=1k\Omega$
- Rail-to-Rail input and output
- 55MHz unity gain bandwidth
- 12V/μs slew rate
- +80mA, -55mA output current
- -40°C to +125°C operating temperature range
- Fully specified at 3V and ±5V supplies
- CLC1003: Pb-free SOT23-5, SOIC-8
- Future option CLC2003: Dual
- Future option CLC4003: Quad

APPLICATIONS

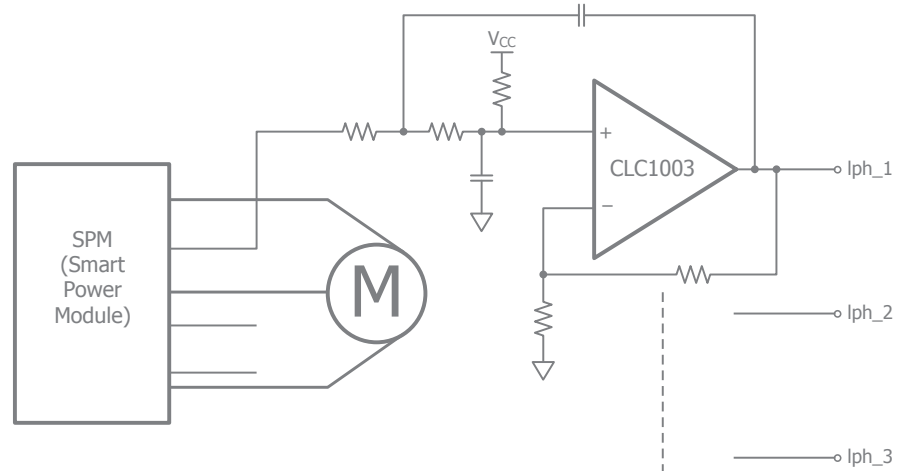
- Active filters
- Sensor interface
- High-speed transducer amp
- Medical instrumentation
- Probe equipment
- Test equipment
- Smoke detectors
- Hand-held analytic instruments

General Description

The COMLINEAR CLC1003 is a single channel, high-performance, voltage feedback amplifier with near precision performance, low input voltage noise, and ultra low distortion. The CLC1003 family of amplifiers offers 1mV maximum input offset voltage, 3.5nV/√Hz broadband input voltage noise, and 0.00005% THD at 1kHz. These amplifiers also provide 55MHz gain bandwidth product and 12V/μs slew rate making them well suited for applications requiring precision DC performance and high AC performance. These COMLINEAR high-performance amplifiers also offer a rail-to-rail input and output, simplifying single supply designs and offering larger dynamic range possibilities. The inputs extend beyond the rails by 500mV.

The COMLINEAR CLC1003 family of amplifiers are designed to operate from 2.5V to 12V supplies and operate over the extended temperature range of -40°C to +125°.

Typical Application - Current Sensing in 3-Phase Motor



Ordering Information

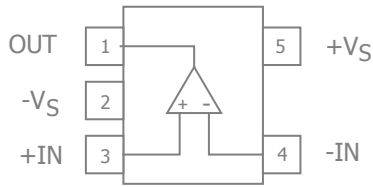
| Part Number | Package | Pb-Free | RoHS Compliant | Operating Temperature Range | Packaging Method |
|---------------|---------|---------|----------------|-----------------------------|------------------|
| CLC1003IST5X | SOT23-5 | Yes | Yes | -40°C to +85°C | Reel |
| CLC1003ISO8X* | SOIC-8 | Yes | Yes | -40°C to +85°C | Reel |
| CLC1003ISO8* | SOIC-8 | Yes | Yes | -40°C to +85°C | Rail |
| CLC1003AST5X | SOT23-5 | Yes | Yes | -40°C to +125°C | Reel |
| CLC1003ASO8X* | SOIC-8 | Yes | Yes | -40°C to +125°C | Reel |
| CLC1003ASO8* | SOIC-8 | Yes | Yes | -40°C to +125°C | Rail |

*Preliminary Product Information

Moisture sensitivity level for all parts is MSL-1.



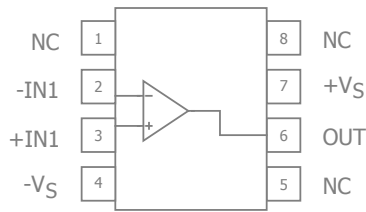
CLC1003 SOT Pin Configuration



CLC1003 SOT23-5 Pin Assignments

| Pin No. | Pin Name | Description |
|---------|----------|-----------------|
| 1 | OUT | Output |
| 2 | -VS | Negative supply |
| 3 | +IN | Positive input |
| 4 | -IN | Negative input |
| 5 | +VS | Positive supply |

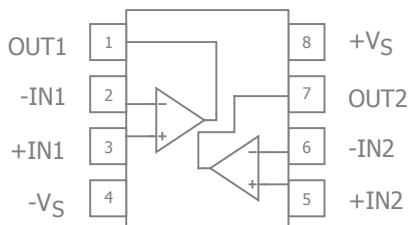
CLC1003 SOIC Pin Configuration



CLC1003 SOIC Pin Assignments

| Pin No. | Pin Name | Description |
|---------|----------|-----------------|
| 1 | NC | No connect |
| 2 | -IN1 | Negative input |
| 3 | +IN1 | Positive input |
| 4 | -VS | Negative supply |
| 5 | NC | No connect |
| 6 | OUT | Output |
| 7 | +VS | Positive supply |
| 8 | NC | No connect |

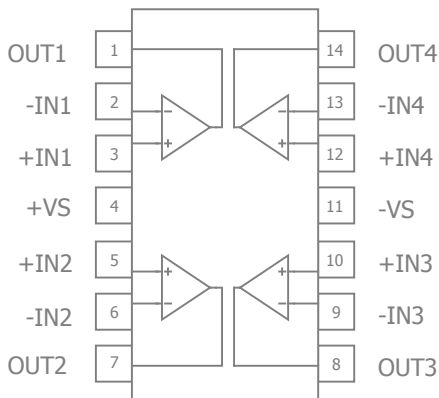
CLC2003 Pin Configuration



CLC2003 (Future Option) Pin Configuration

| Pin No. | Pin Name | Description |
|---------|----------|---------------------------|
| 1 | OUT1 | Output, channel 1 |
| 2 | -IN1 | Negative input, channel 1 |
| 3 | +IN1 | Positive input, channel 1 |
| 4 | -VS | Negative supply |
| 5 | +IN2 | Positive input, channel 2 |
| 6 | -IN2 | Negative input, channel 2 |
| 7 | OUT2 | Output, channel 2 |
| 8 | +VS | Positive supply |

CLC4003 Pin Configuration



CLC4003 (Future Option) Pin Configuration

| Pin No. | Pin Name | Description |
|---------|----------|---------------------------|
| 1 | OUT1 | Output, channel 1 |
| 2 | -IN1 | Negative input, channel 1 |
| 3 | +IN1 | Positive input, channel 1 |
| 4 | +VS | Positive supply |
| 5 | +IN2 | Positive input, channel 2 |
| 6 | -IN2 | Negative input, channel 2 |
| 7 | OUT2 | Output, channel 2 |
| 8 | OUT3 | Output, channel 3 |
| 9 | -IN3 | Negative input, channel 3 |
| 10 | +IN3 | Positive input, channel 3 |
| 11 | -VS | Negative supply |
| 12 | +IN4 | Positive input, channel 4 |
| 13 | -IN4 | Negative input, channel 4 |
| 14 | OUT4 | Output, channel 4 |



Absolute Maximum Ratings

The safety of the device is not guaranteed when it is operated above the "Absolute Maximum Ratings". The device should not be operated at these "absolute" limits. Adhere to the "Recommended Operating Conditions" for proper device function. The information contained in the Electrical Characteristics tables and Typical Performance plots reflect the operating conditions noted on the tables and plots.

| Parameter | Min | Max | Unit |
|---------------------|---------------|---------------|------|
| Supply Voltage | 0 | 14 | V |
| Input Voltage Range | $-V_S - 0.5V$ | $+V_S + 0.5V$ | V |

Reliability Information

| Parameter | Min | Typ | Max | Unit |
|-----------------------------------|-----|-----|-----|------|
| Junction Temperature | | | 150 | °C |
| Storage Temperature Range | -65 | | 150 | °C |
| Lead Temperature (Soldering, 10s) | | | 260 | °C |
| Package Thermal Resistance | | | | |
| 5-Lead SOT23 | | 221 | | °C/W |
| 8-Lead SOIC | | 100 | | °C/W |
| 14-Lead SOIC | | 88 | | °C/W |

Notes:

Package thermal resistance (θ_{JA}), JEDEC standard, multi-layer test boards, still air.

Recommended Operating Conditions

| Parameter | Min | Typ | Max | Unit |
|--|-----|-----|------|------|
| Operating Temperature Range (CLC1003I) | -40 | | +85 | °C |
| Operating Temperature Range (CLC1003A) | -40 | | +125 | °C |
| Supply Voltage Range | 2.5 | | 12 | V |



Electrical Characteristics at +3V

$T_A = 25^\circ\text{C}$, $V_S = +3\text{V}$, $R_f = 1\text{k}\Omega$, $R_L = 1\text{k}\Omega$ to $V_S/2$, $G = 2$; unless otherwise noted.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---------------------------|------------------------------|---|-----|---------------|-----|------------------------------|
| Frequency Domain Response | | | | | | |
| GBWP | -3dB Gain Bandwidth Product | $G = 10$, $V_{OUT} = 0.05V_{pp}$ | | 31 | | MHz |
| UGBW | Unity Gain Bandwidth | $V_{OUT} = 0.05V_{pp}$, $R_f = 0$ | | 50 | | MHz |
| BW _{SS} | -3dB Bandwidth | $V_{OUT} = 0.05V_{pp}$ | | 24 | | MHz |
| BW _{LS} | Large Signal Bandwidth | $V_{OUT} = 2V_{pp}$ | | 3.3 | | MHz |
| Time Domain Response | | | | | | |
| t_R , t_F | Rise and Fall Time | $V_{OUT} = 2\text{V}$ step; (10% to 90%) | | 150 | | ns |
| t_S | Settling Time to 0.1% | $V_{OUT} = 2\text{V}$ step | | 78 | | ns |
| OS | Overshoot | $V_{OUT} = 2\text{V}$ step | | 0.3 | | % |
| SR | Slew Rate | 2V step | | 11 | | V/ μs |
| Distortion/Noise Response | | | | | | |
| HD2 | 2nd Harmonic Distortion | $2V_{pp}$, 10kHz, $R_L = 1\text{k}\Omega$ | | -98 | | dBc |
| | | $2V_{pp}$, 100kHz, $R_L = 100\Omega$ | | -85 | | dBc |
| HD3 | 3rd Harmonic Distortion | $2V_{pp}$, 10kHz, $R_L = 1\text{k}\Omega$ | | -95 | | dBc |
| | | $2V_{pp}$, 100kHz, $R_L = 100\Omega$ | | -81 | | dBc |
| THD | Total Harmonic Distortion | $1V_{pp}$, 1kHz, $G=1$, $R_L = 2\text{k}\Omega$ | | 0.0005 | | % |
| e_n | Input Voltage Noise | > 10kHz | | 5.5 | | nV/ $\sqrt{\text{Hz}}$ |
| | | > 100kHz | | 3.9 | | nV/ $\sqrt{\text{Hz}}$ |
| DC Performance | | | | | | |
| V_{IO} | Input Offset Voltage | | | 0.088 | | mV |
| dV_{IO} | Average Drift | | | 1.3 | | $\mu\text{V}/^\circ\text{C}$ |
| I_b | Input Bias Current | | | -0.340 | | μA |
| dI_b | Average Drift | | | 0.8 | | nA/ $^\circ\text{C}$ |
| I_{os} | Input Offset Current | | | 0.2 | | nA |
| PSRR | Power Supply Rejection Ratio | DC | | 100 | | dB |
| A_{OL} | Open-Loop Gain | $V_{OUT} = V_S / 2$ | | 104 | | dB |
| I_S | Supply Current | per channel | | 1.85 | | mA |
| Input Characteristics | | | | | | |
| R_{IN} | Input Resistance | Non-inverting, $G = 1$ | | 30 | | M Ω |
| C_{IN} | Input Capacitance | | | 1.1 | | pF |
| CMIR | Common Mode Input Range | | | -0.5 to 3.5 | | V |
| CMRR | Common Mode Rejection Ratio | DC, $V_{cm} = 0.5\text{V}$ to 2.5V | | 94 | | dB |
| Output Characteristics | | | | | | |
| V_{OUT} | Output Voltage Swing | $R_L = 150\Omega$ | | 0.085 to 2.80 | | V |
| | | $R_L = 1\text{k}\Omega$ | | 0.04 to 2.91 | | V |
| I_{OUT} | Output Current | | | +75, -40 | | mA |
| I_{SC} | Short-Circuit Output Current | $V_{OUT} = V_S / 2$ | | +95, -50 | | mA |

Notes:

- 100% tested at 25°C



Electrical Characteristics at $\pm 5V$

$T_A = 25^\circ C$, $V_S = \pm 5V$, $R_f = 1k\Omega$, $R_L = 1k\Omega$ to GND, $G = 2$; unless otherwise noted.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---------------------------|---|--|------|-----------------|------|---------------------|
| Frequency Domain Response | | | | | | |
| GBWP | -3dB Gain Bandwidth Product | $G = 10$, $V_{OUT} = 0.05V_{pp}$ | | 35 | | MHz |
| UGBW | Unity Gain Bandwidth | $V_{OUT} = 0.05V_{pp}$, $R_f = 0$ | | 55 | | MHz |
| BW _{SS} | -3dB Bandwidth | $V_{OUT} = 0.05V_{pp}$ | | 25 | | MHz |
| BW _{LS} | Large Signal Bandwidth | $V_{OUT} = 2V_{pp}$ | | 3.6 | | MHz |
| Time Domain Response | | | | | | |
| t_R , t_F | Rise and Fall Time | $V_{OUT} = 2V$ step; (10% to 90%) | | 125 | | ns |
| t_S | Settling Time to 0.1% | $V_{OUT} = 2V$ step | | 80 | | ns |
| OS | Overshoot | $V_{OUT} = 2V$ step | | 0.3 | | % |
| SR | Slew Rate | 4V step | | 12 | | V/ μ s |
| Distortion/Noise Response | | | | | | |
| HD2 | 2nd Harmonic Distortion | $2V_{pp}$, 10kHz, $R_L = 1k\Omega$ | | -125 | | dBc |
| | | $2V_{pp}$, 100kHz, $R_L = 100\Omega$ | | -90 | | dBc |
| HD3 | 3rd Harmonic Distortion | $2V_{pp}$, 10kHz, $R_L = 1k\Omega$ | | -127 | | dBc |
| | | $2V_{pp}$, 100kHz, $R_L = 100\Omega$ | | -85 | | dBc |
| THD | Total Harmonic Distortion | $1V_{pp}$, 1kHz, $G=1$, $R_L = 2k\Omega$ | | 0.00005 | | % |
| e_n | Input Voltage Noise | > 10kHz | | 5.3 | | nV/ \sqrt{Hz} |
| | | > 100kHz | | 3.5 | | nV/ \sqrt{Hz} |
| DC Performance | | | | | | |
| V_{IO} | Input Offset Voltage ⁽¹⁾ | | -1 | 0.050 | 1 | mV |
| dV_{IO} | Average Drift | | | 1.3 | | μ V/ $^\circ C$ |
| I_b | Input Bias Current ⁽¹⁾ | | -2.6 | -0.30 | 2.6 | μ A |
| dI_b | Average Drift | | | 0.85 | | nA/ $^\circ C$ |
| I_{os} | Input Offset Current ⁽¹⁾ | | | 0.2 | 0.7 | μ A |
| PSRR | Power Supply Rejection Ratio ⁽¹⁾ | DC | 82 | 100 | | dB |
| A_{OL} | Open-Loop Gain ⁽¹⁾ | $V_{OUT} = V_S / 2$ | 95 | 115 | | dB |
| I_S | Supply Current ⁽¹⁾ | per channel | | 2.2 | 2.75 | mA |
| Input Characteristics | | | | | | |
| R_{IN} | Input Resistance | Non-inverting, $G = 1$ | | 30 | | M Ω |
| C_{IN} | Input Capacitance | | | 1 | | pF |
| CMIR | Common Mode Input Range | | | ± 5.5 | | V |
| CMRR | Common Mode Rejection Ratio ⁽¹⁾ | DC, $V_{cm} = -3V$ to 3V | 70 | 95 | | dB |
| Output Characteristics | | | | | | |
| V_{OUT} | Output Voltage Swing | $R_L = 150\Omega$ | | -4.826 to 4.534 | | V |
| | | $R_L = 1k\Omega$ ⁽¹⁾ | -4.7 | -4.93 to 4.85 | 4.7 | V |
| I_{OUT} | Output Current | | | +80, -55 | | mA |
| I_{SC} | Short-Circuit Output Current | $V_{OUT} = V_S / 2$ | | +115, -90 | | mA |

Notes:

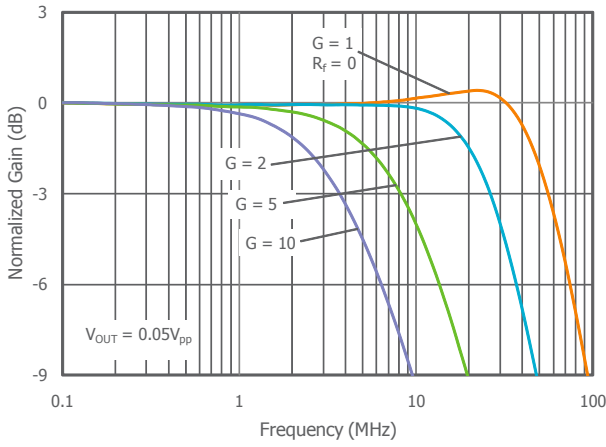
- 100% tested at 25°C



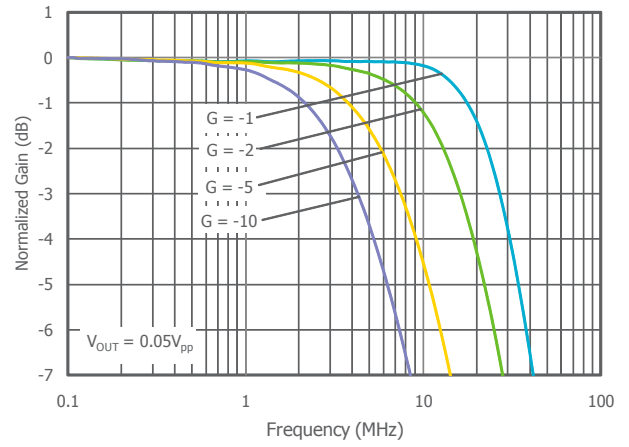
Typical Performance Characteristics

$T_A = 25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_f = 1\text{k}\Omega$, $R_L = 1\text{k}\Omega$ to GND, $G = 2$; unless otherwise noted.

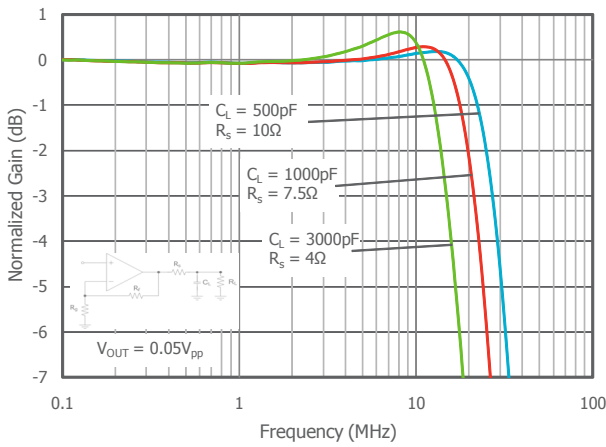
Non-Inverting Frequency Response



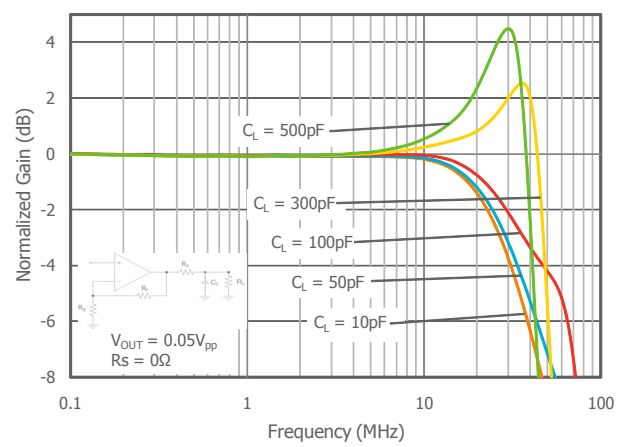
Inverting Frequency Response



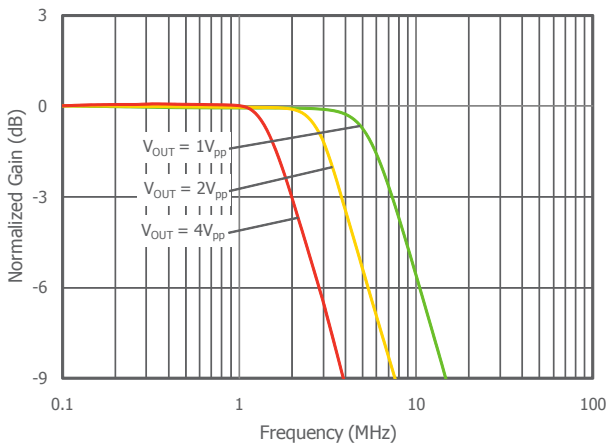
Frequency Response vs. C_L



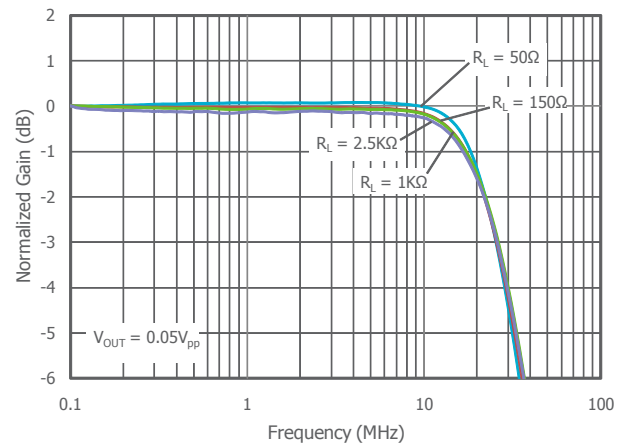
Frequency Response vs. C_L without R_S



Frequency Response vs. V_{OUT}



Frequency Response vs. R_L

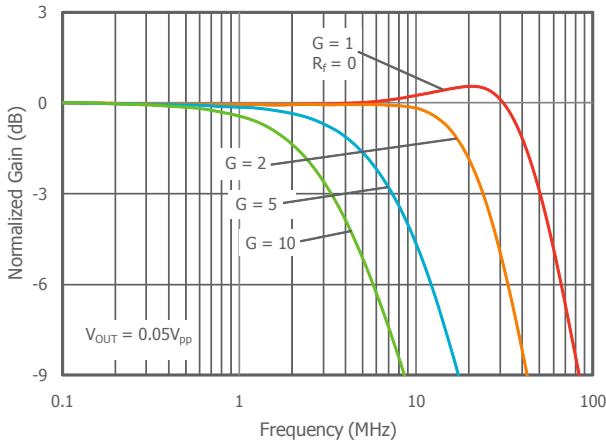




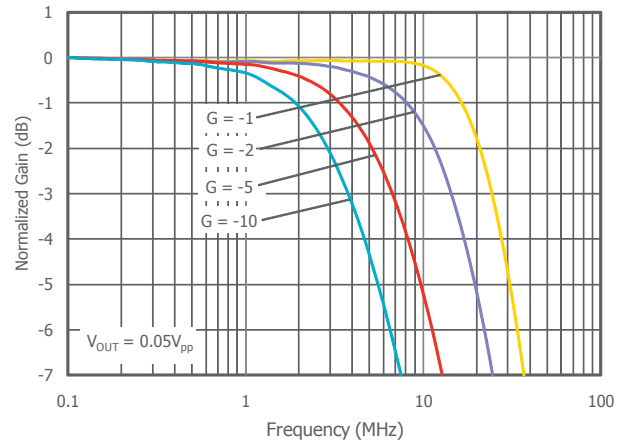
Typical Performance Characteristics

$T_A = 25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_f = 1\text{k}\Omega$, $R_L = 1\text{k}\Omega$ to GND, $G = 2$; unless otherwise noted.

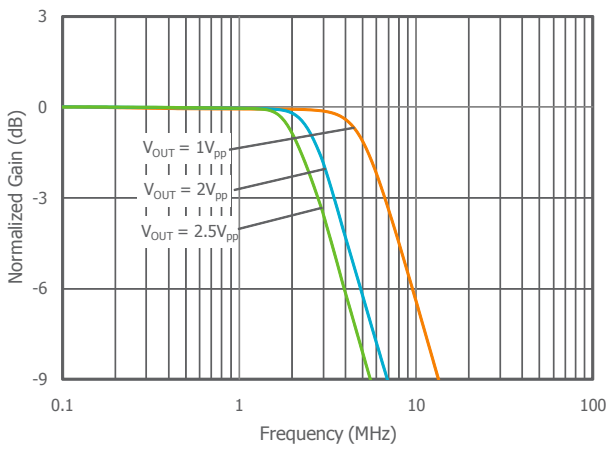
Non-Inverting Frequency Response at $V_S = 3\text{V}$



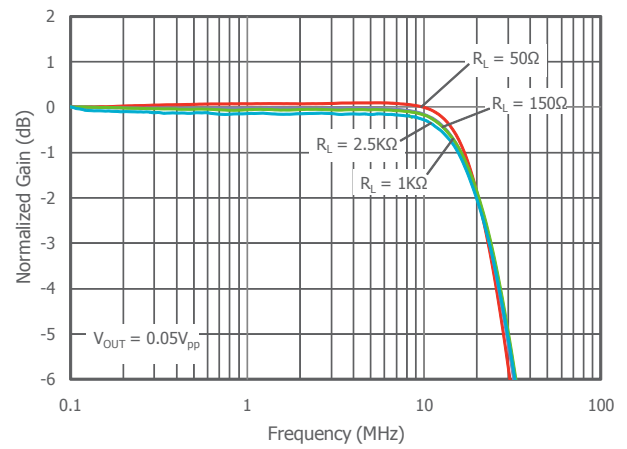
Inverting Frequency Response at $V_S = 3\text{V}$



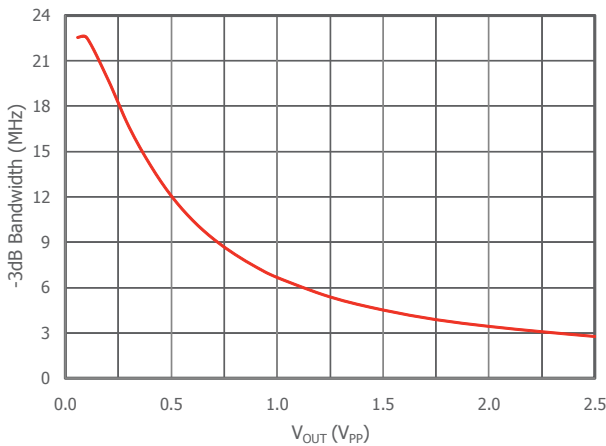
Frequency Response vs. V_{OUT} at $V_S = 3\text{V}$



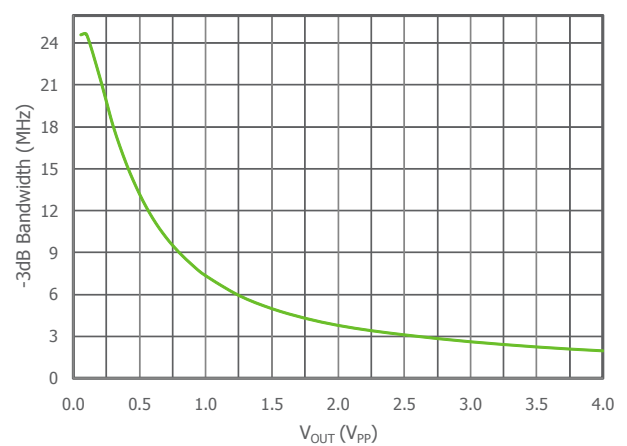
Frequency Response vs. R_L at $V_S = 3\text{V}$



-3dB Bandwidth vs. Output Voltage at $V_S = 3\text{V}$



-3dB Bandwidth vs. Output Voltage

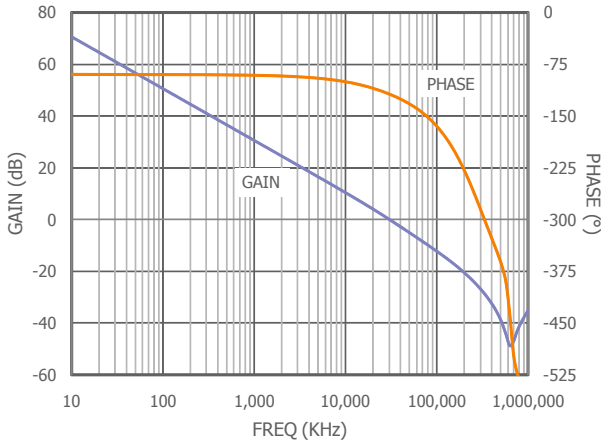




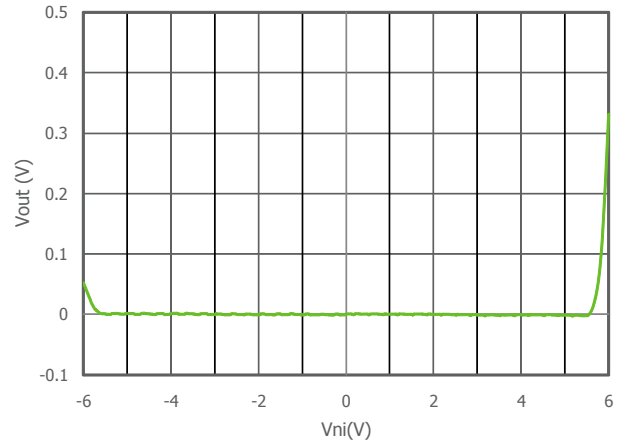
Typical Performance Characteristics - Continued

$T_A = 25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_f = 1\text{k}\Omega$, $R_L = 1\text{k}\Omega$ to GND, $G = 2$; unless otherwise noted.

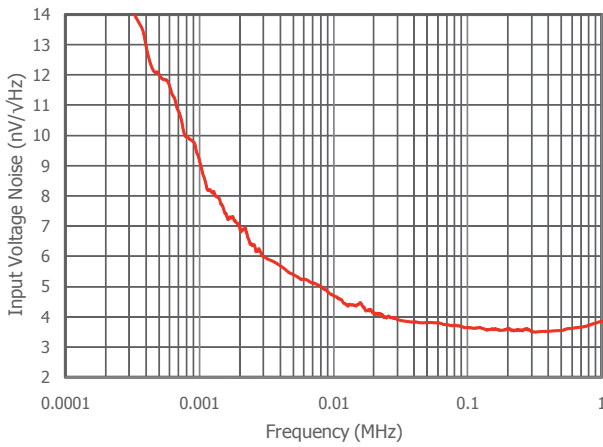
Open Loop Gain and Phase vs. Frequency



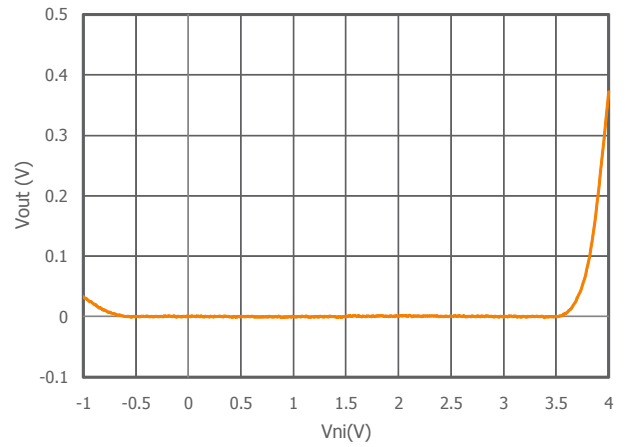
CMIR



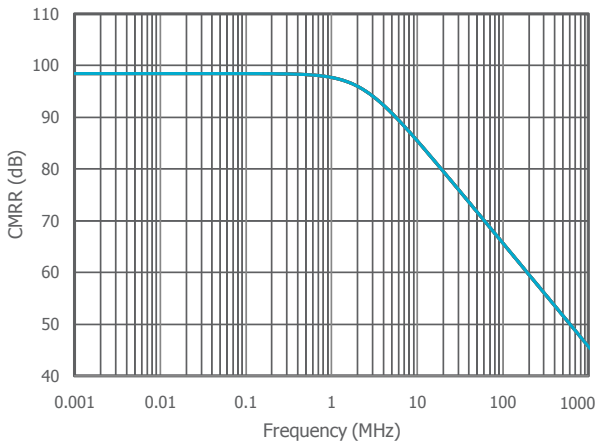
Input Voltage Noise



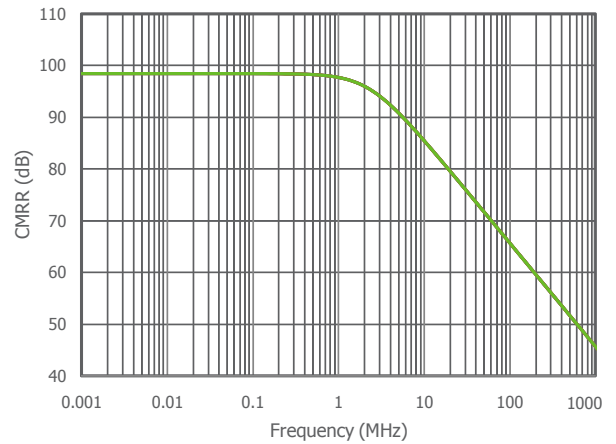
CMIR at $V_S = 3\text{V}$



CMRR vs. Frequency



PSRR vs. Frequency

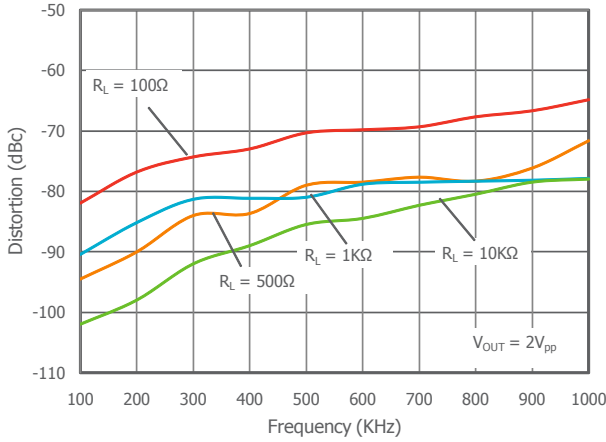




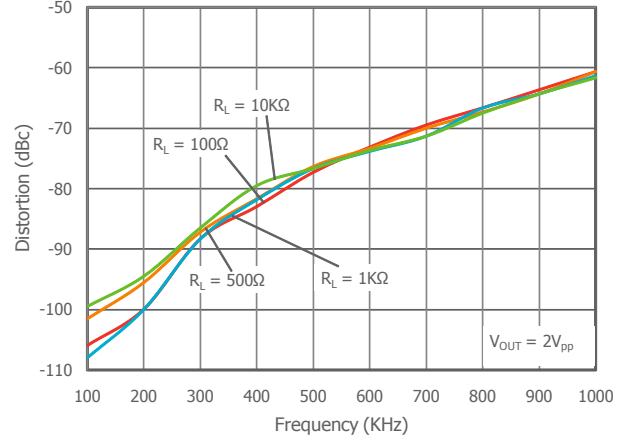
Typical Performance Characteristics - Continued

$T_A = 25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_f = 1\text{k}\Omega$, $R_L = 1\text{k}\Omega$ to GND, $G = 2$; unless otherwise noted.

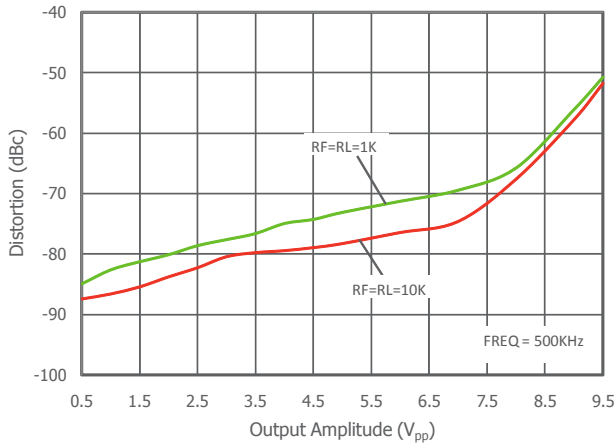
2nd Harmonic Distortion vs. R_L



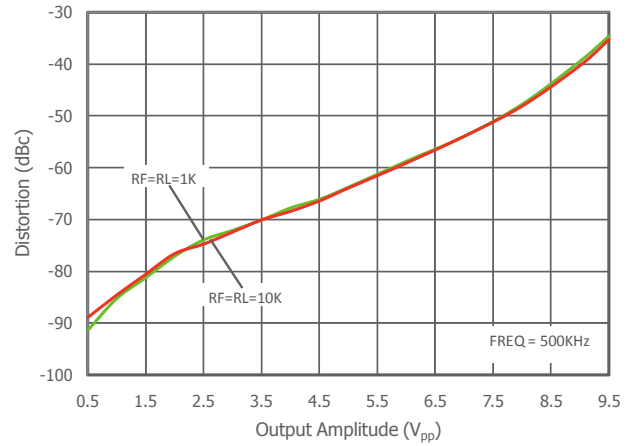
3rd Harmonic Distortion vs. R_L



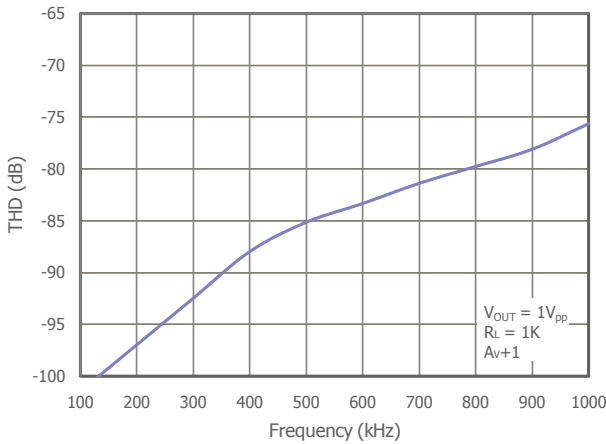
2nd Harmonic Distortion vs. V_{OUT}



3rd Harmonic Distortion vs. V_{OUT}



THD vs. Frequency

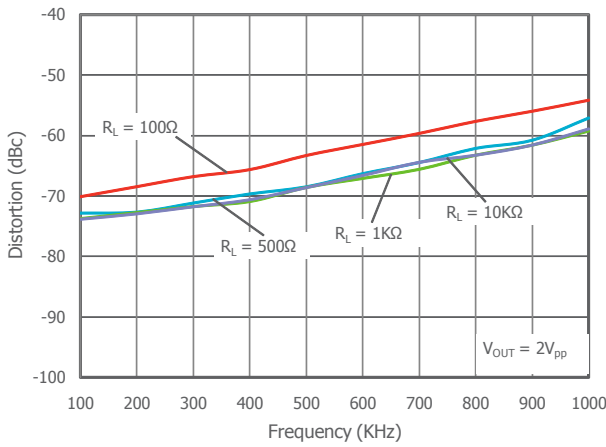




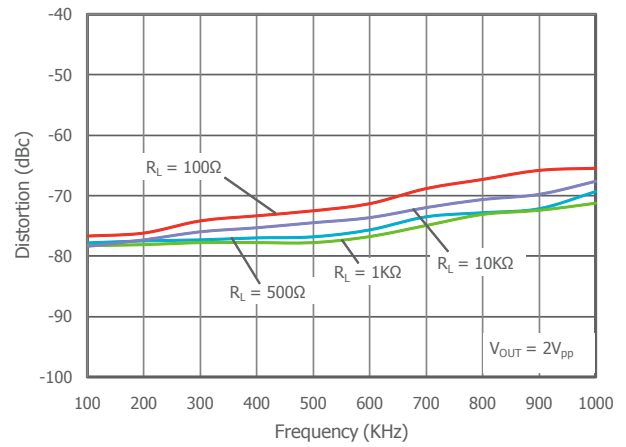
Typical Performance Characteristics - Continued

$T_A = 25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_f = 1\text{k}\Omega$, $R_L = 1\text{k}\Omega$ to GND, $G = 2$; unless otherwise noted.

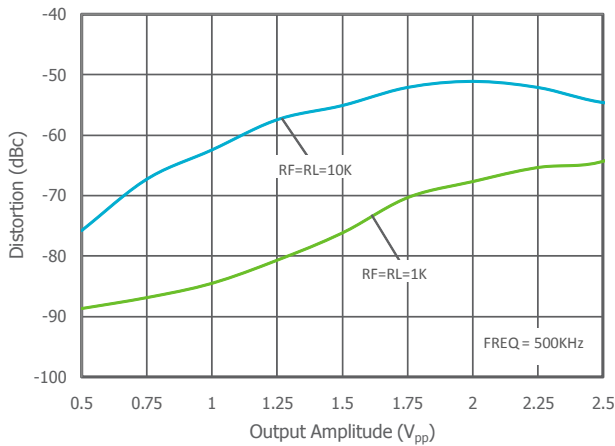
2nd Harmonic Distortion vs. R_L at $V_S = 3\text{V}$



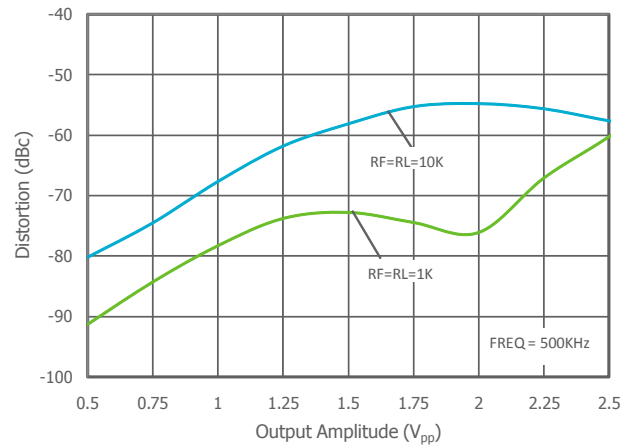
3rd Harmonic Distortion vs. R_L at $V_S = 3\text{V}$



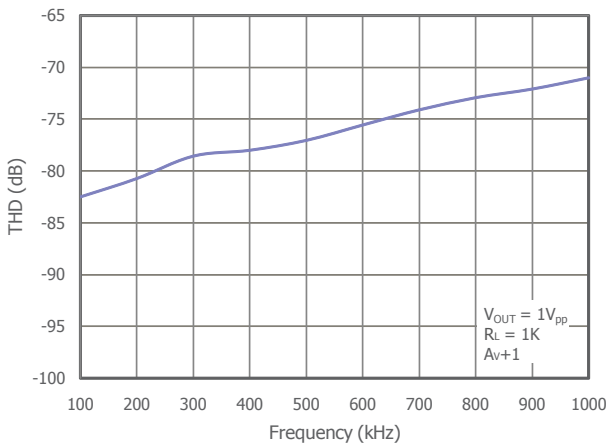
2nd Harmonic Distortion vs. V_{OUT} at $V_S = 3\text{V}$



3rd Harmonic Distortion vs. V_{OUT} at $V_S = 3\text{V}$



THD vs. Frequency at $V_S = 3\text{V}$

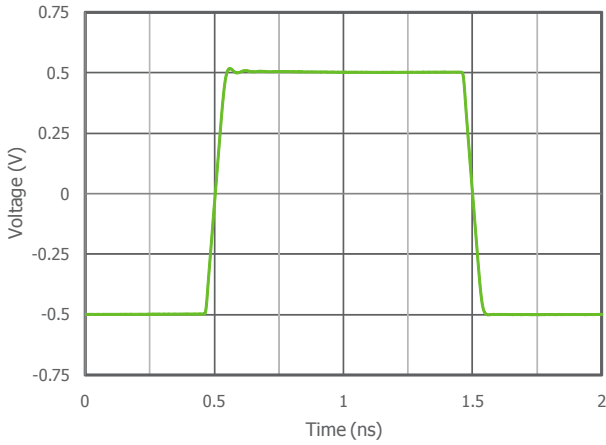




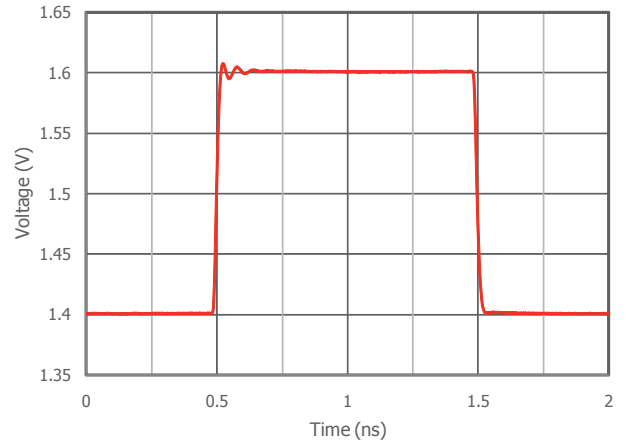
Typical Performance Characteristics - Continued

$T_A = 25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_f = 1\text{k}\Omega$, $R_L = 1\text{k}\Omega$ to GND, $G = 2$; unless otherwise noted.

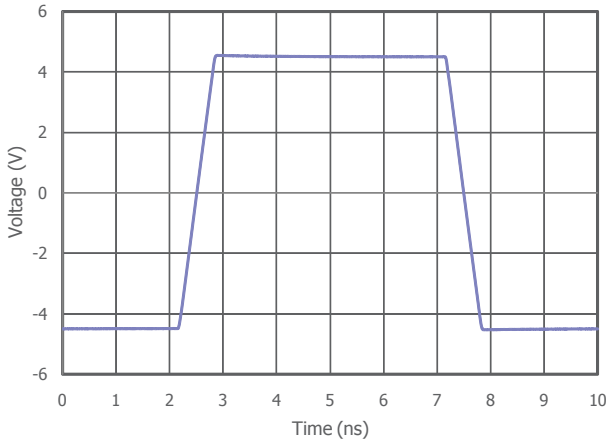
Small Signal Pulse Response



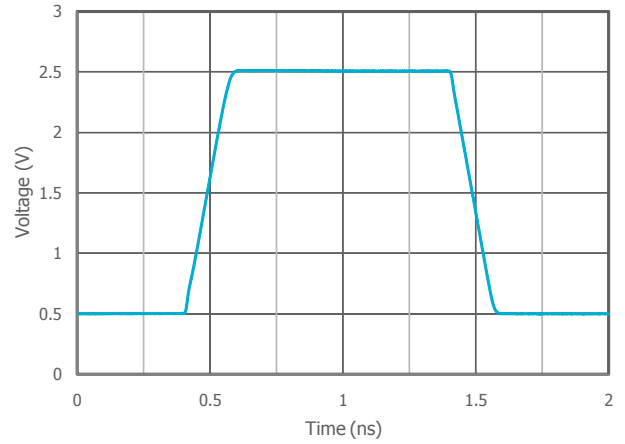
Small Signal Pulse Response at $V_S = 3\text{V}$



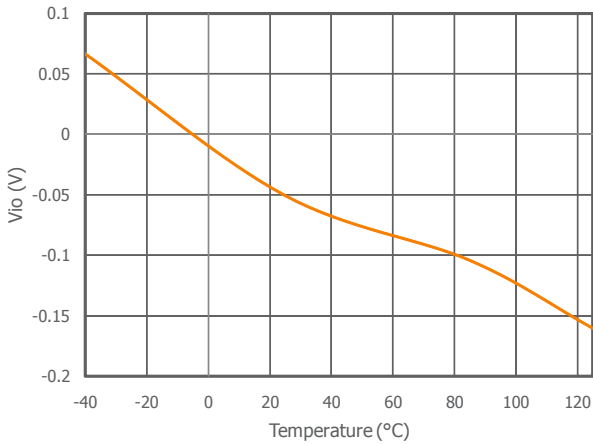
Large Signal Pulse Response



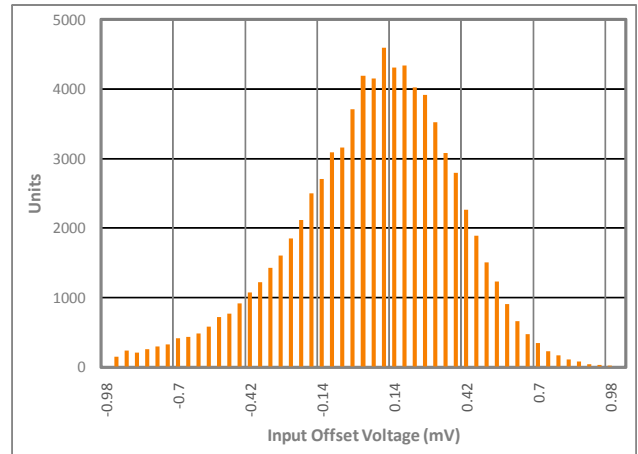
Large Signal Pulse Response at $V_S = 3\text{V}$



Input Offset Voltage vs. Temperature



Input Offset Voltage Distribution





Application Information

Basic Operation

Figures 1 and 2 illustrate typical circuit configurations for non-inverting, inverting, and unity gain topologies for dual supply applications. They show the recommended bypass capacitor values and overall closed loop gain equations.

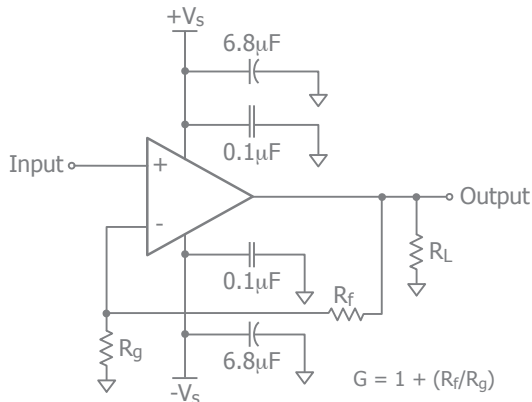


Figure 1. Typical Non-Inverting Gain Circuit

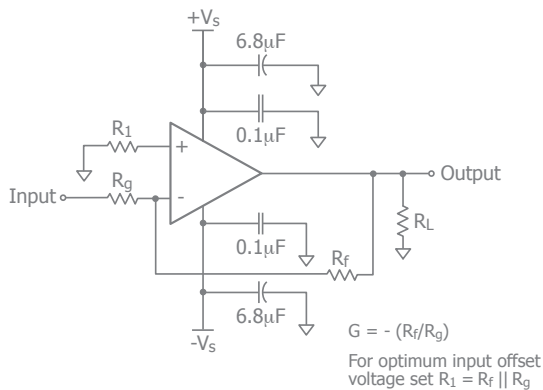


Figure 2. Typical Inverting Gain Circuit

Power Dissipation

Power dissipation should not be a factor when operating under the stated 300 ohm load condition. However, applications with low impedance, DC coupled loads should be analyzed to ensure that maximum allowed junction temperature is not exceeded. Guidelines listed below can be used to verify that the particular application will not cause the device to operate beyond its intended operating range.

Maximum power levels are set by the absolute maximum junction rating of 150°C. To calculate the junction tem-

perature, the package thermal resistance value Θ_{JA} (Θ_{JA}) is used along with the total die power dissipation.

$$T_{\text{Junction}} = T_{\text{Ambient}} + (\Theta_{JA} \times P_D)$$

Where T_{Ambient} is the temperature of the working environment.

In order to determine P_D , the power dissipated in the load needs to be subtracted from the total power delivered by the supplies.

$$P_D = P_{\text{supply}} - P_{\text{load}}$$

Supply power is calculated by the standard power equation.

$$P_{\text{supply}} = V_{\text{supply}} \times I_{\text{RMS supply}}$$

$$V_{\text{supply}} = V_{S+} - V_{S-}$$

Power delivered to a purely resistive load is:

$$P_{\text{load}} = ((V_{\text{LOAD}})_{\text{RMS}}^2) / R_{\text{load eff}}$$

The effective load resistor ($R_{\text{load eff}}$) will need to include the effect of the feedback network. For instance,

$R_{\text{load eff}}$ in figure 3 would be calculated as:

$$R_L \parallel (R_f + R_g)$$

These measurements are basic and are relatively easy to perform with standard lab equipment. For design purposes however, prior knowledge of actual signal levels and load impedance is needed to determine the dissipated power. Here, P_D can be found from

$$P_D = P_{\text{Quiescent}} + P_{\text{Dynamic}} - P_{\text{Load}}$$

Quiescent power can be derived from the specified I_S values along with known supply voltage, V_{Supply} . Load power can be calculated as above with the desired signal amplitudes using:

$$(V_{\text{LOAD}})_{\text{RMS}} = V_{\text{PEAK}} / \sqrt{2}$$

$$(I_{\text{LOAD}})_{\text{RMS}} = (V_{\text{LOAD}})_{\text{RMS}} / R_{\text{load eff}}$$

The dynamic power is focused primarily within the output stage driving the load. This value can be calculated as:

$$P_{\text{DYNAMIC}} = (V_{S+} - V_{\text{LOAD}})_{\text{RMS}} \times (I_{\text{LOAD}})_{\text{RMS}}$$

Assuming the load is referenced in the middle of the power rails or $V_{\text{supply}}/2$.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the packages available.

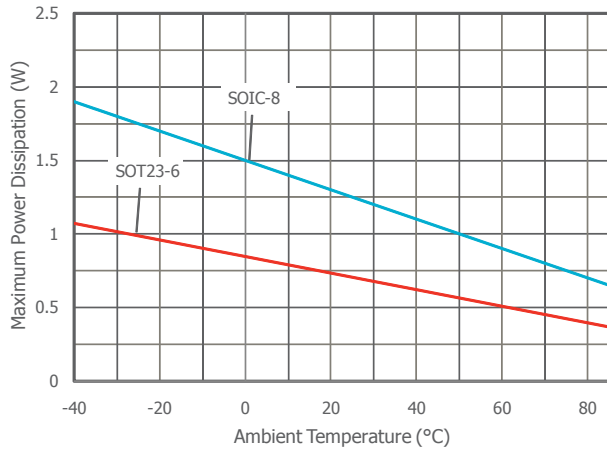


Figure 3. Maximum Power Derating

Driving Capacitive Loads

Increased phase delay at the output due to capacitive loading can cause ringing, peaking in the frequency response, and possible unstable behavior. Use a series resistance, R_S , between the amplifier and the load to help improve stability and settling performance. Refer to Figure 4.

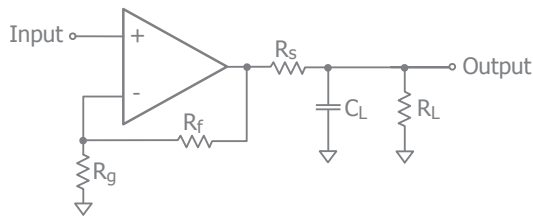


Figure 4. Addition of R_S for Driving Capacitive Loads

The CLC1003 family of amplifiers is capable of driving up to 300pF directly, with no series resistance. Directly driving 500pF causes over 4dB of frequency peaking, as shown in the plot on page 6. Table 1 provides the recommended R_S for various capacitive loads. The recommended R_S values result in ≤ 1 dB peaking in the frequency response. The Frequency Response vs. C_L plots, on page 6, illustrates the response of the CLCx003.

| C_L (pF) | R_S (Ω) | -3dB BW (MHz) |
|------------|--------------------|---------------|
| 500 | 10 | 27 |
| 1000 | 7.5 | 20 |
| 3000 | 4 | 15 |

Table 1: Recommended R_S vs. C_L

For a given load capacitance, adjust R_S to optimize the tradeoff between settling time and bandwidth. In general, reducing R_S will increase bandwidth at the expense of additional overshoot and ringing.

Overdrive Recovery

An overdrive condition is defined as the point when either one of the inputs or the output exceed their specified voltage range. Overdrive recovery is the time needed for the amplifier to return to its normal or linear operating point. The recovery time varies, based on whether the input or output is overdriven and by how much the range is exceeded. The CLCx003 will typically recover in less than 20ns from an overdrive condition. Figure 5 shows the CLC1003 in an overdriven condition.

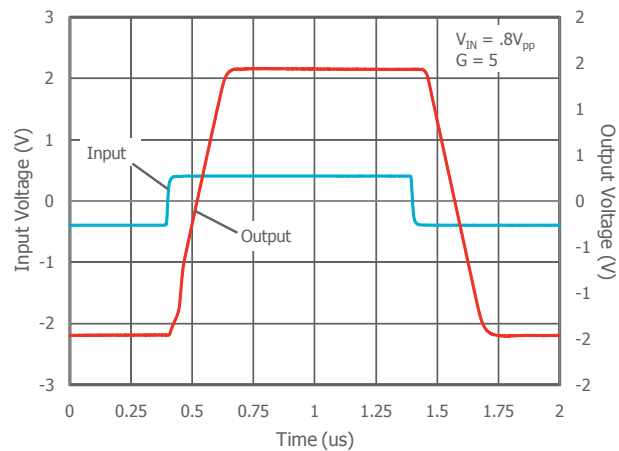


Figure 5. Overdrive Recovery

Considerations for Offset and Noise Performance

Offset Analysis

There are three sources of offset contribution to consider; input bias current, input bias current mismatch, and input offset voltage. The input bias currents are assumed to be equal with and additional offset current in one of the inputs to account for mismatch. The bias currents will not affect the offset as long as the parallel combination of R_f and R_g matches R_t . Refer to Figure 6.

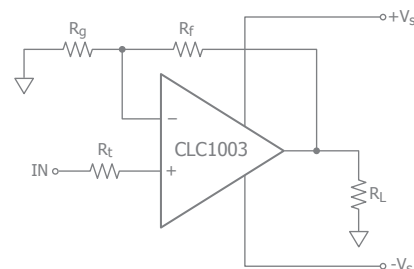


Figure 6: Circuit for Evaluating Offset



The first place to start is to determine the source resistance. If it is very small an additional resistance may need to be added to keep the values of R_f and R_g to practical levels. For this analysis we assume that R_t is the total resistance present on the non-inverting input. This gives us one equation that we must solve:

$$R_t = R_g || R_f$$

This equation can be rearranged to solve for R_g :

$$R_g = (R_t * R_f) / (R_f - R_t)$$

The other consideration is desired gain (G) which is:

$$G = (1 + R_f/R_g)$$

By plugging in the value for R_g we get

$$R_f = G * R_t$$

And R_g can be written in terms of R_t and G as follows:

$$R_g = (G * R_t) / (G - 1)$$

The complete input offset equation is now only dependent on the voltage offset and input offset terms given by:

$$VI_{OS} = \sqrt{(V_{IO})^2 + (I_{OS} * RT)^2}$$

And the output offset is:

$$VO_{OS} = G * \sqrt{(V_{IO})^2 + (I_{OS} * RT)^2}$$

Noise analysis

The complete equivalent noise circuit is shown in Figure 7.

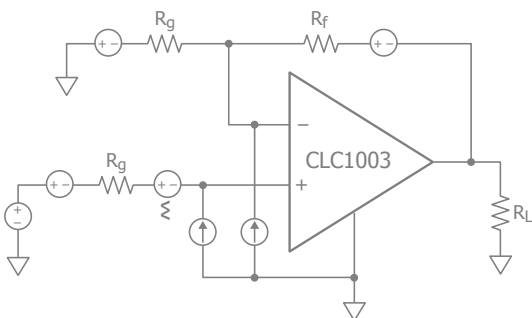


Figure 7: Complete Equivalent Noise Circuit

The complete noise equation is given by:

$$v_o^2 = v_{orext}^2 + \left(e_n \left(1 + \frac{R_f}{R_g} \right) \right)^2 + \left(i_{bp} * RT \left(1 + \frac{R_f}{R_g} \right) \right)^2 + \left(i_{bn} * R_f \right)^2$$

Where V_{orext} is the noise due to the external resistors and is given by:

$$v_o^2 = \left(e_n \left(1 + \frac{R_f}{R_g} \right) \right)^2 + \left(e_G * \frac{R_f}{R_g} \right)^2 + e_F^2$$

The complete equation can be simplified to:

$$v_o^2 = 3 * (4kT * G * RT) + (e_n G)^2 + 2 * (i_n * RT)^2$$

It's easy to see that the effect of amplifier voltage noise is proportionate to gain and will tend to dominate at large gains. The other terms will have their greatest impact at large R_t values at lower gains.

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. CADEKA has evaluation boards to use as a guide for high frequency layout and as aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8 μ F and 0.1 μ F ceramic capacitors for power supply decoupling
- Place the 6.8 μ F capacitor within 0.75 inches of the power pin
- Place the 0.1 μ F capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts below for more information.

Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of these devices:

| Evaluation Board | Products |
|------------------|--------------------|
| CEB002 | CLC1003 in SOT23-5 |
| CEB003 | CLC1003 in SOIC-8 |



Evaluation Board Schematics

Evaluation board schematics and layouts are shown in Figures 8-13. These evaluation boards are built for dual-supply operation. Follow these steps to use the board in a single-supply application:

1. Short -Vs to ground.
2. Use C3 and C4, if the -Vs pin of the amplifier is not directly connected to the ground plane.

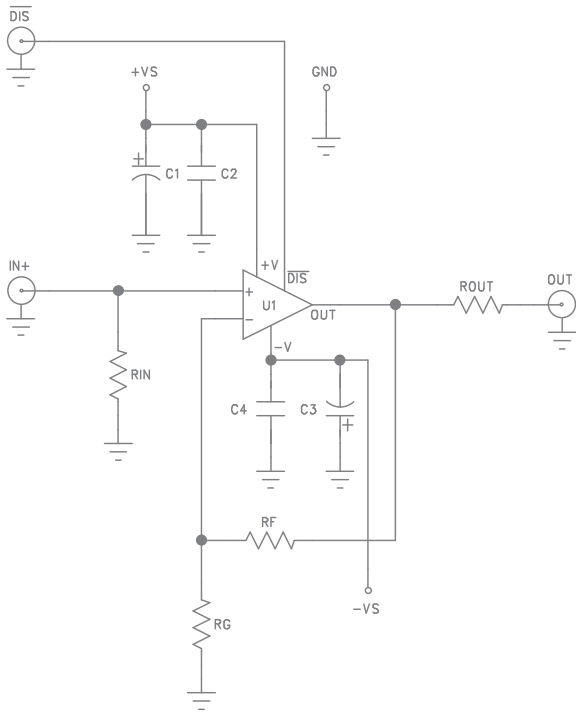


Figure 8. CEB002 Schematic

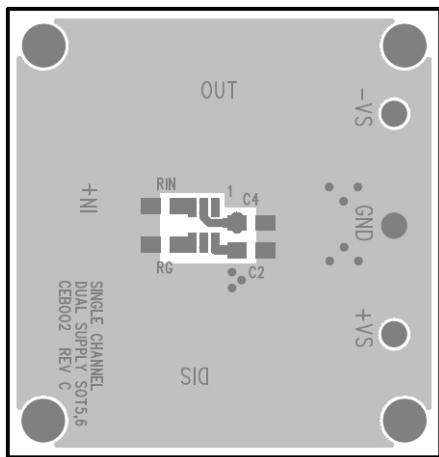


Figure 9. CEB002 Top View

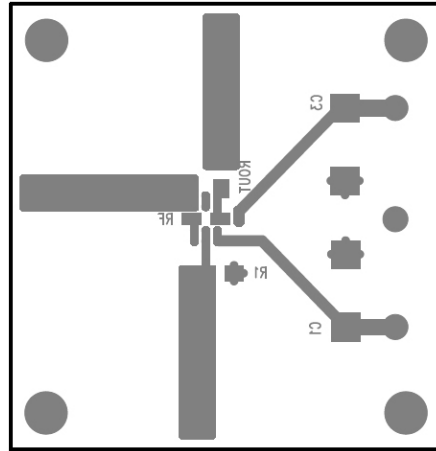


Figure 10. CEB002 Bottom View

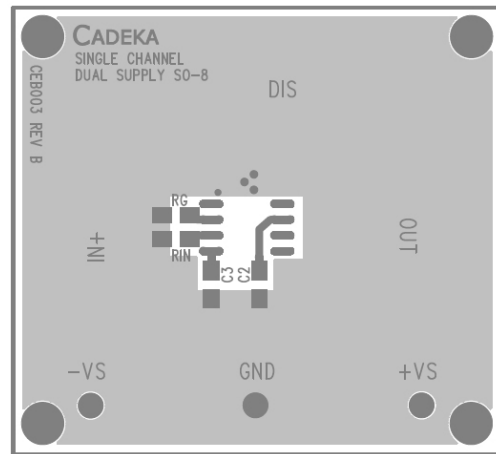


Figure 11. CEB003 Top View

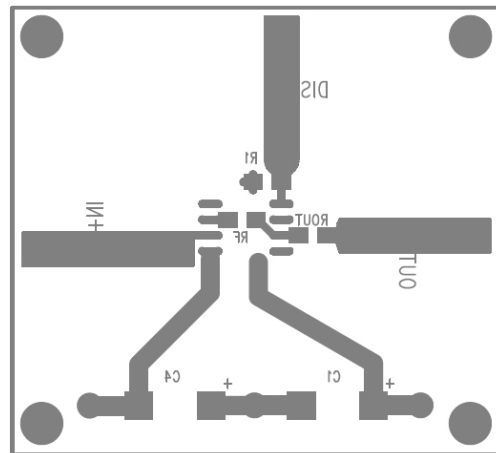
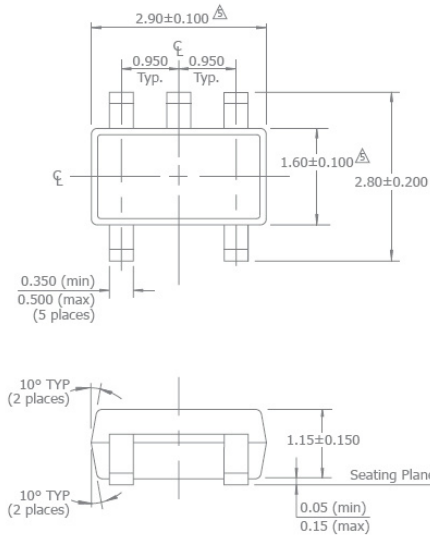


Figure 12. CEB003 Bottom View



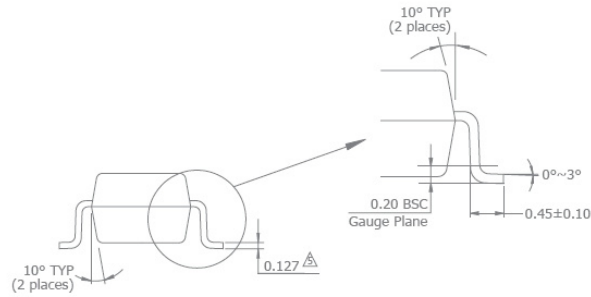
Mechanical Dimensions

SOT23-5 Package

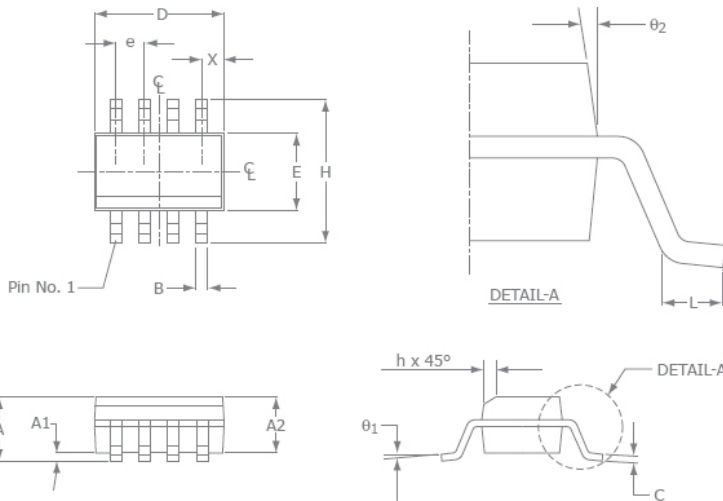


NOTES:

1. Dimensions and tolerances are as per ANSI Y14.5M-1982.
2. Package surface to be matte finish VDI 11~13.
3. Die is facing up for mold. Die is facing down for trim/form, ie. reverse trim/form.
4. The footlength measuring is based on the gauge plane method.
- △ Dimension are exclusive of mold flash and gate burr.
- △ Dimension are exclusive of solder plating.



SOIC-8



| SOIC-8 | | |
|----------------|----------|------|
| SYMBOL | MIN | MAX |
| A1 | 0.10 | 0.25 |
| B | 0.36 | 0.48 |
| C | 0.19 | 0.25 |
| D | 4.80 | 4.98 |
| E | 3.81 | 3.99 |
| e | 1.27 BSC | |
| H | 5.80 | 6.20 |
| h | 0.25 | 0.5 |
| L | 0.41 | 1.27 |
| A | 1.37 | 1.73 |
| θ ₁ | 0° | 8° |
| X | 0.55 ref | |
| θ ₂ | 7° BSC | |

NOTE:

1. All dimensions are in millimeters.
2. Lead coplanarity should be 0 to 0.1mm (0.004") max.
3. Package surface finishing: VDI 24~27
4. All dimension excluding mold flashes.
5. The lead width, B to be determined at 0.1905mm from the lead tip.

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