CS1600

Low-cost PFC Controller for Electronic Ballasts

Features

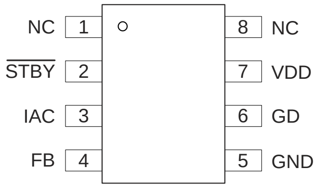
- ☐ Lowest PFC System Cost for Electronic Ballasts
- ☐ Variable Frequency Discontinuous Conduction Mode
- ☐ Improved Efficiency Due to Variable Switching Frequency
- ☐ EMI Signature Reduction from Digital Noise Shaping
- ☐ Integrated Feedback Compensation
- ☐ Overvoltage Protection with Hysteresis
- ☐ Overpower Protection with Shutdown
- ☐ UVLO with Wide Hysteresis
- ☐ Thermal Shutdown with Hysteresis

Description

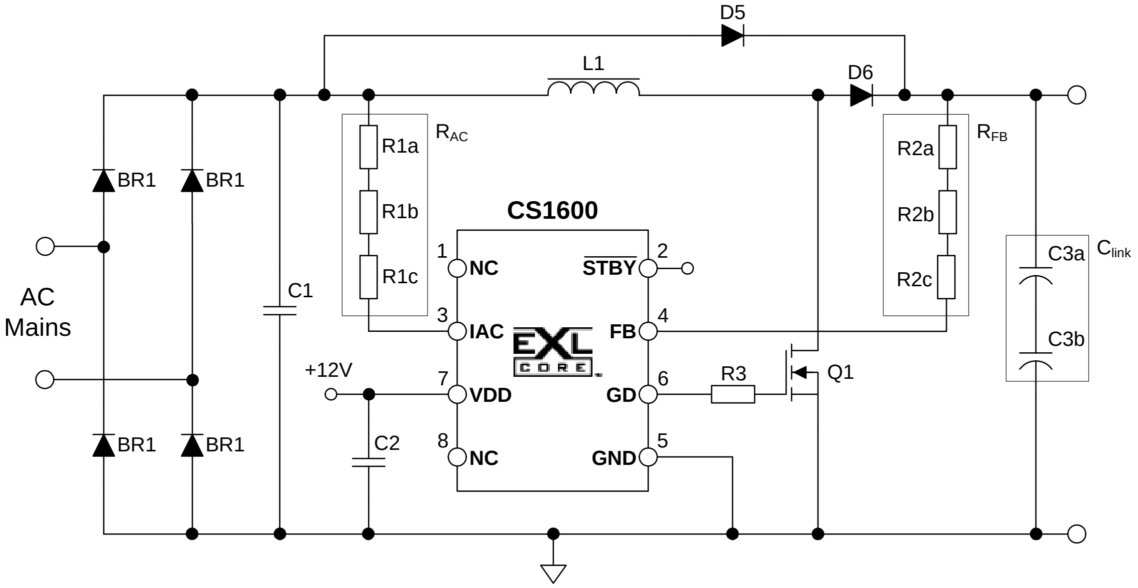
CS1600 is a high-performance Variable Frequency Discontinuous Conduction Mode (VF - DCM), active Power Factor Correction (PFC) controller, optimized to deliver the lowest PFC system cost for electronic ballast applications.

A variable ON time / variable frequency algorithm is used to achieve near unity power factor. This algorithm spreads the EMI frequency spectrum, which reduces the conducted EMI filtering requirements. The feedback loop is closed through an integrated compensation network within the IC, eliminating the need for additional external components. Protection features such as overvoltage, overcurrent, overpower, open- and short-circuit protection, overtemperature, and brownout help protect the device during abnormal transient conditions.

Pin Assignments



8-lead SOIC



Cirrus Logic, Inc.
http://www.cirrus.com

1. PIN DESCRIPTIONS

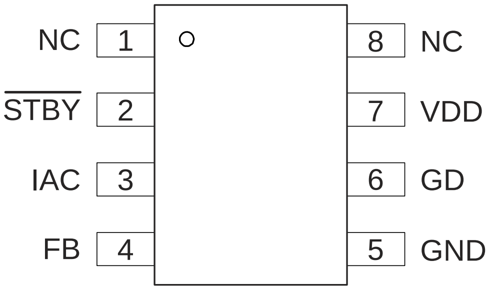


Table 1. Pin Descriptions

Pin Name	Pin #	I/O	Description
NC	1, 8	-	**No Connect** — Connect these pins to V_{DD} to prevent any leakage path that could arise from leaving them unterminated.
$\overline{\text{STBY}}$	2	IN	**Standby** — This is an active-low pin. Shorting this pin to GND disables PFC switching. The input has a pull-up resistor and should be driven with an open-collector device. Leave this pin unterminated when not in use.
IAC	3	IN	**Rectified Line Voltage Sense** — The IAC pin is used to sense the rectified line voltage. This signal, in conjunction with the signal on the FB pin, is used in the Power Factor Correction (PFC) algorithm A filter capacitor of up to 2.2 nF may be added between this pin and VDD to provide noise immunity.
FB	4	IN	**Feedback Voltage Sense** — The FB pin is used to sense the output voltage of the PFC stage. This signal, in conjunction with the signal on the IAC pin, is used in the Power Factor Correction (PFC) algorithm. A filter capacitor of up to 2.2 nF may be added between this pin and VDD to provide noise immunity.
GND	5	–	**Ground** — GND is a common reference for all the functional blocks in this device.
GD	6	OUT	**Gate Drive** — GD is the output of the device with a source capability of 0.5 A and a current sink capacity of 1 A.
VDD	7	IN	**IC Supply Voltage** — V_{DD} is the input used to provide bias to the device. This pin has an internal shunt to ground. An external bias needs to be applied for steady-state operation. A low-ESR ceramic decoupling capacitor at this pin is recommended for reliable operation of this device.

2. CHARACTERISTICS AND SPECIFICATIONS

2.1 Absolute Maximum Ratings

Pin	Symbol	Parameter	Value	Unit
7	V_{DD}	IC Supply Voltage[1]	V_z	V
2,3,4	V_{IN}	Input Voltage	-0.5 to V_{DD}	V
3,4	I_{IN}	Input Current	50	mA
6	V_{GD}	Gate Drive Voltage	-0.3 to V_{DD}	V
6	I_{GD}	Gate Drive Current	-1.0 / +0.5	A
1,2,3,4,5,6,8	ESD	Human Body Model	2000	V
1,2,3,4,5,6,8	ESD	Machine Model	200	V
1,2,3,4,5,6,8	ESD	Charged Device Model	500	V
-	P_D	Total Power Dissipation at 50° C[2]	600	mW
-	T_J	Junction Temperature Operating Range	-40 to +125	ºC
-	T_{Stg}	Storage Temperature Range	-65 to +150	ºC

Notes:
1. The CS1600 has an internal shunt regulator that controls the nominal operating voltage on the VDD pin.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation at the rate of 50 mW / ºC for variation over temperature.

2.2 Electrical Characteristics

Recommended operating conditions (unless otherwise specified): $T_A = T_J$ = -40º to +125º C, V_{DD} = 10 to 15 V, GND = 0 V. *Typical* values are at T_A = 25º C.

Parameter	Condition	Symbol	Min	Typ	Max	Unit
V_{DD} Supply Voltage						
V_{DD} Turn-on Threshold Voltage	V_{DD} increasing	$V_{th(St)}$	8.4	8.8	9.3	V
V_{DD} Turn-off Threshold Voltage	V_{DD} decreasing	$V_{th(Stp)}$	7.1	7.4	7.9	V
UVLO Hysteresis		V_{Hys}	-	1.3	-	V
Zener Voltage	I_{DD} = 20 mA	V_Z	17.0	17.9	18.5	V
Supply Current Section						
Start-up Supply Current	$V_{DD} < V_{th(St)}$	I_{ST}	-	68	80	µA
Standby Supply Current	$\overline{STBY}$ < 0.8V	I_{SB}	-	80	112	µA
Operating Supply Current	C_L = 1nF, f_{sw} = 70 kHz	I_{DD}	-	1.7	1.9	mA
PFC Gate Drive Section						
Maximum Operating Frequency[3,4]	Normal mode, V_{DD} = 13 V	$f_{SW(max)}$	62	66	70	kHz
Minimum Operating Frequency[3,4]	Normal mode, V_{DD} = 13 V	$f_{SW(min)}$	20	22	23	kHz
Minimum Duty Cycle	V_{DD} = 13 V, $\overline{STBY}$ < 0.8 V	t_{DC_min}	-	-	0	%
Maximum Duty Cycle[3,4]	V_{DD} = 13 V	D_{max}	64	66	68	%
Minimum On Time	V_{DD} = 13 V	t_{on_min}	0.45	0.5	0.55	µs
Output Source Resistance	I_{GD} = 100 mA, V_{DD} = 13 V	R_{OH}	-	9	-	Ω
Output Sink Resistance	I_{GD} = -200 mA, V_{DD} = 13 V	R_{OL}	-	6	-	Ω
Rise Time	C_L = 1 nF, V_{DD} = 13 V	t_r	-	32	45	ns

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Fall Time	C_L = 1 nF, V_{DD} = 13 V	t_f	-	15	25	ns
Output Voltage Low	IGD = -200 mA,VDD = 13 V	V_{OL}	-	0.9	1.3	v
Output Voltage High	IGD = 100 mA,VDD = 13 V	V_{OH}	11.3	11.8	-	v
Feedback and Protection						
Reference Current		I_{ref}	127	130	133	µA
Overvoltage Protection Threshold		I_{OVP}/I_{ref}	105	107	110	%
Overvoltage Protection Current Hysteresis		$I_{OVP(Hy)}$	-	4	-	%
Undervoltage Protection Threshold		I_{UVP}/I_{ref}	83	85	87	%
Undervoltage Protection Current Hysteresis		$I_{UVP(Hy)}$	-	10	-	%
Overpower Protection Threshold [3,4]	% of full load as defined by Eq. 3		123	125	127	%
Overpower Protection Recovery [3,4]			35	49	60	%
Input Brownout Protection Threshold[7]	V_{out} = 460V, GDRV turns off	$V_{BP(th)}$	82	86	90	Vrms
Input Brownout Recovery Threshold[7]	V_{out} = 460V, GDRV turns on	V_{BR}	94	97	100	Vrms
Thermal Protection						
Thermal Shutdown Threshold [3]		T_{SD}	130	143	155	ºC
Thermal Shutdown Hysteresis		$T_{SD(Hy)}$	-	9	-	ºC
STBY Input						
Logic Threshold [5] Low High			- V_{DD} – 0.8	- -	0.8 -	V

2.3 Thermal Characteristics

Symbol	Parameter	Value	Unit
$R\theta_{JA}$	Thermal Resistance (Junction to Ambient)[6].	159	ºC / W
$R\theta_{JC}$	Thermal Resistance (Junction to Case)[6].	39	ºC / W

[3] Specifications guaranteed by design & characterization.

[4] Specifications measured as an instantaneous quantity NOT as a time-averaged quantity.

[5] $\overline{\text{STBY}}$ is designed to be driven by an open-collector device. The input is internally pulled up with a 600 kΩ resistor.

[6] The package thermal impedance is calculated in accordance with JESD 51.

[7] For an output voltage, V_{out}, other than 460V, the threshold scales by a factor of $V_{out}/460$

3. TYPICAL ELECTRICAL PERFORMANCE

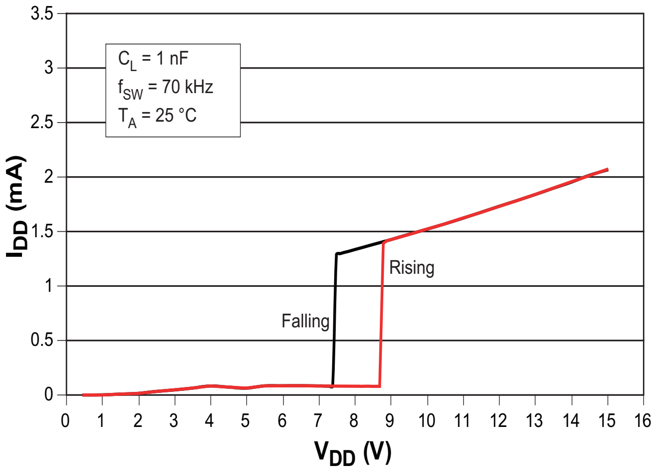


Figure 1. UVLO Characteristics

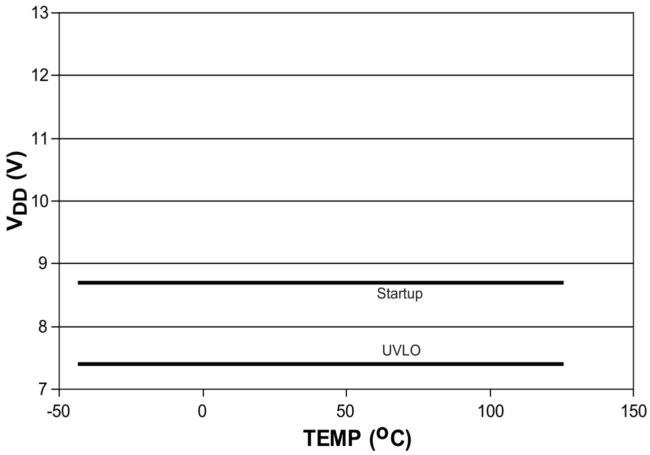
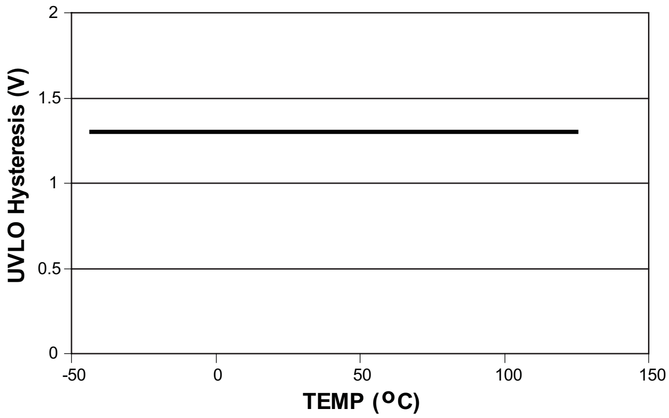


Figure 2. Start-up & UVLO vs. Temperature



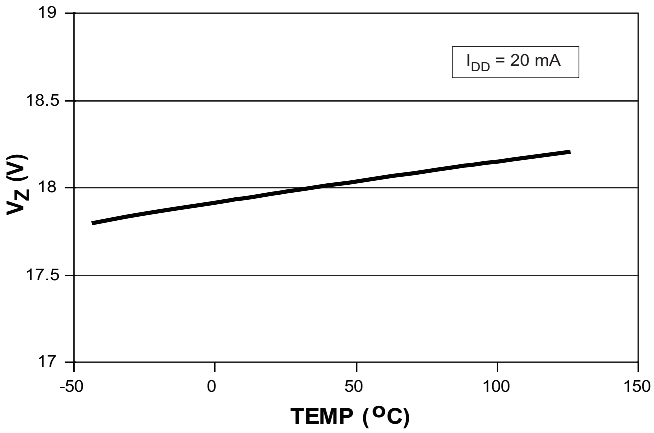


Figure 3. UVLO Hysteresis vs. Temperature

Figure 4. VDD Zener Voltage vs. Temperature

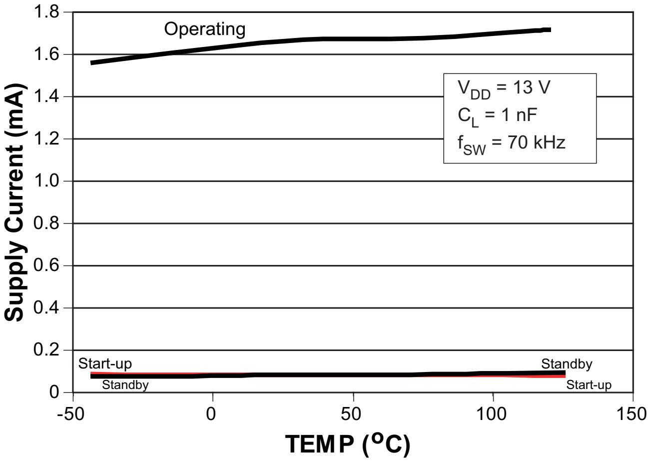


Figure 5. Supply Current (I_{SB}, I_{ST}, I_{DD}) vs. Temperature

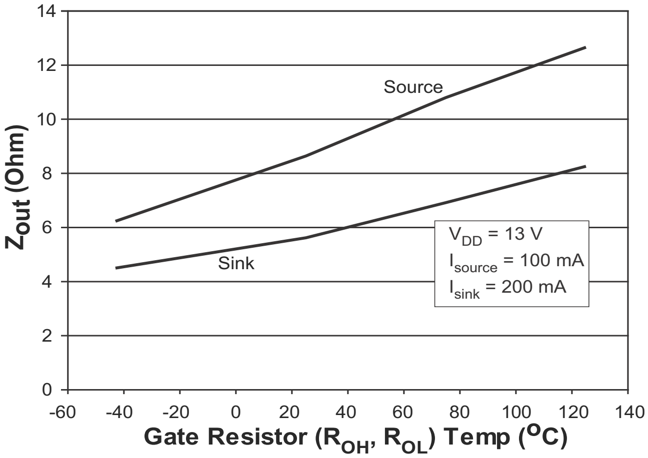


Figure 6. Gate Resistance (R_{OH}, R_{OL}) vs. Temperature

4. INTRODUCTION

CS1600 is a digitally controlled Power Factor Correction (PFC) controller that operates in the Variable Frequency Discontinuous Conduction Mode (VF - DCM). The CS1600 uses a proprietary digital algorithm to optimize control of the power switch to deliver highly efficient performance for electronic ballast applications. With this control scheme, the total number of external components needed is minimized in comparison to conventional control techniques, thus reducing the overall system cost.

Digital control is achieved by constantly monitoring two voltages – the PFC output voltage (V_{link}) at pin FB and the rectified AC line voltage (V_{rect}) at pin IAC. This is done by measuring the currents that flow into the respective pins. These currents are then fed to the inputs of two analog-to-digital converters (ADCs) and are compared against an internal target current, I_{ref}.

The digital outputs of the two ADCs are then processed in a control algorithm which determines the behavior of the CS1600 during start-up, normal operation, and under fault conditions such as brownout, overvoltage, overcurrent, overpower, and over-temperature. Details of operation during these conditions are discussed in later sections of this document.

Some of the key features of the CS1600 are as follows:

- **Discontinuous Conduction Mode with Continuously Variable Switching Frequency**

  The PFC switching frequency is varied every switching cycle. This allows for a spread spectrum which minimizes the conducted EMI peaks at any given frequency, thereby minimizing the size and cost of the EMI filter required at the front-end.

  During start-up, the control algorithm limits the maximum ON time and adjusts the frequency to avoid inductor saturation and provides a near-trapezoidal envelope for the input current during every half cycle. During normal operation, as the line voltage changes over half of a line cycle, the frequency varies approximately 2:1 as shown in Figure 7 below.

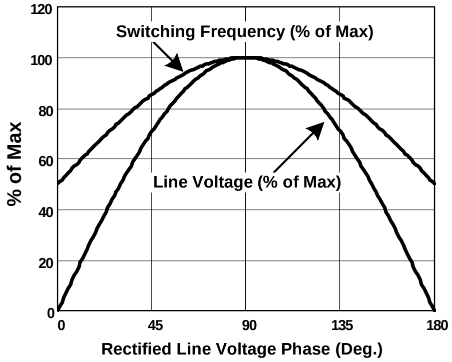


Figure 7. Switching Frequency vs. Phase Angle

  Maximum power transfer occurs at the peak of the AC line voltage, at which time, the frequency reaches its maximum value. Switching losses are minimized during periods of low power transfer by switching at lower frequencies near the zero-crossing of the AC line.

  This switching frequency profile helps reduce total BOM cost through savings in the size of the boost inductor and the EMI filter components, while at the same time, improving overall system efficiency.

- **Integrated Feedback Control**

  No external feedback compensation components are required for the CS1600. The internal digital control engine self-compensates the feedback error signal using an adaptive control algorithm.

- **Protection Features**

  The CS1600 provides various protection features such as undervoltage, overcurrent, overpower, open and short circuit protection and brownout. It also provides the user with the option of using the $\overline{\text{STBY}}$ pin to disable switching of the device.

4.1 PFC Implementation

The PFC switching frequency profile over the line period has been discussed in detail in Section 4. In addition, the digital control algorithm tracks changes the AC input and operates in different frequency bands at different line voltages as illustrated in Figure 8 and Figure 9 below.

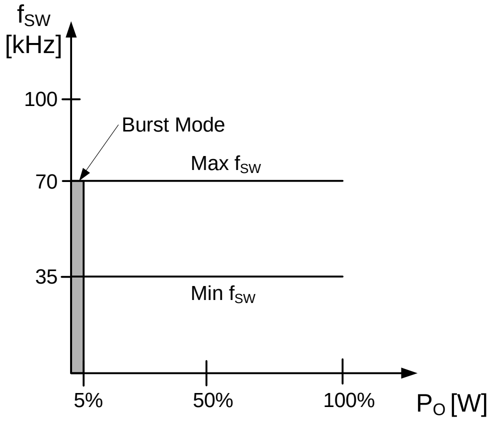


Figure 8. Switching Frequency vs. Output Power V_{in} < 165 VAC

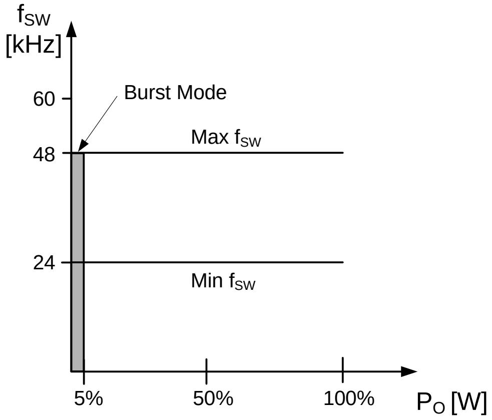


Figure 9. Switching Frequency vs. Output Power V_{in} > 165 VAC

The CS1600 primarily operates in the DCM mode with a properly sized inductor. However, it will move into a quasi-CRM mode near the peaks of the input line, in order to enable maximum power delivery, as illustrated in Figure 10 below.

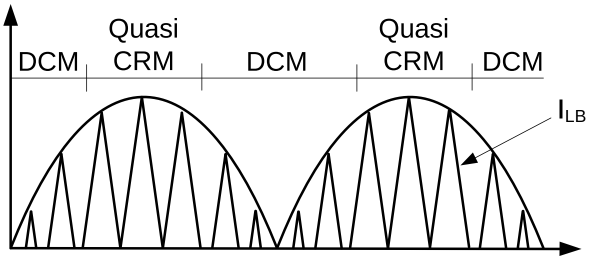


Figure 10. DCM and quasi-CRM Operation with CS1600

4.1.1 *Start-up Mode vs. Normal Mode*

CS1600 operates in two discrete states:

Start-up mode:

When the output voltage of the PFC stage, V_{link}, is <90% of its nominal value, the device operates in the start-up mode. It continues operating in this mode till the nominal V_{link} voltage is reached. The start-up algorithm provides an ON time which is varied in proportion to the sensed rectified voltage, while changing the switching frequency to provide maximum power.

During this start-up phase of operation, the switching frequency could be significantly lower than the normal operating frequency, and the input current waveform is forced into following a trapezoidal envelope in phase with the line voltage, to maximize energy transfer. The ON time and the switching frequency of the IC ensure that peak currents are kept controlled to prevent saturation of the boost inductor during this period.

Normal mode:

Once V_{link} reaches its nominal value, the chip operates in the normal mode. Here, the frequency follows the profile shown in Figure 7, and the ON time is varied to achieve PFC. Any drop in V_{link} to below its undervoltage threshold, as defined in Section 2.2. Electrical Characteristics re-triggers the start-up mode of operation. A simplified illustration of operation in these two modes is shown below in Figure 11.

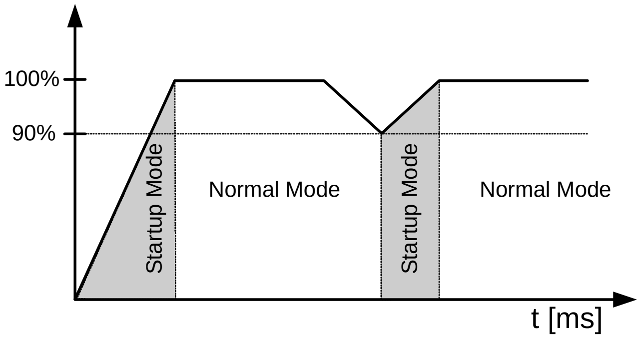


Figure 11. Start-up and Normal Modes

4.1.2 Burst Mode

In addition to the start-up mode and normal mode of operation, the controller enters the burst mode of operation when the estimated output power (P_O) is < 5% of its nominal value. During this stage, the PFC driver is disabled intermittently over a full line cycle period, as shown in Figure 12. The period of time for which the PFC drive is disabled depends on the level of loading present..

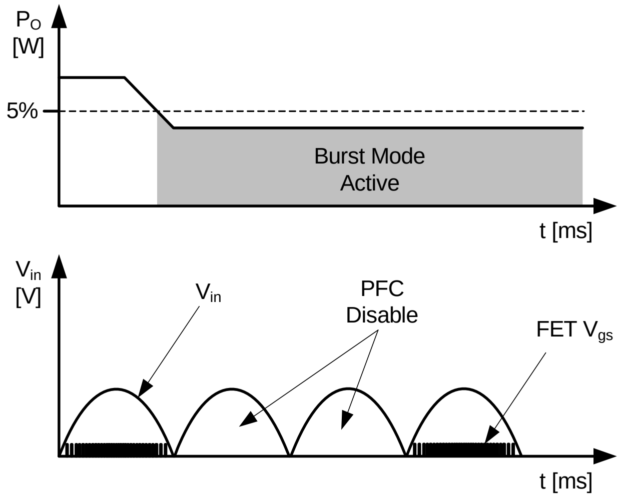


Figure 12. Burst Mode of Operation

4.2 Input Feedforward and Output Regulation

The CS1600 continuously monitors the rectified AC line and the PFC output voltage through sense resistors tied to the IAC and the FB pins to monitor the voltages, scaled as currents. The rectified AC line sense resistor R_{AC} needs to be the same size of the resistor R_{FB} used for current feedback from the PFC output voltage. These currents are effectively compared against an internal reference current to provide adaptive PFC control. The resistor values are calculated as follows:

$$R_{FB} = \frac{V_{link} - V_{DD}}{I_{ref}} \qquad \text{[Eq.1]}$$

$$R_{AC} = R_{FB} \qquad \text{[Eq.2]}$$

where

R_{FB} = Feedback resistor used to sense the PFC output voltage

R_{AC} = Feedforward resistor used to sense the rectified line voltage

V_{link}= PFC Output Voltage

V_{DD} = IC Supply Voltage

I_{ref} = Target Reference current used for feedback

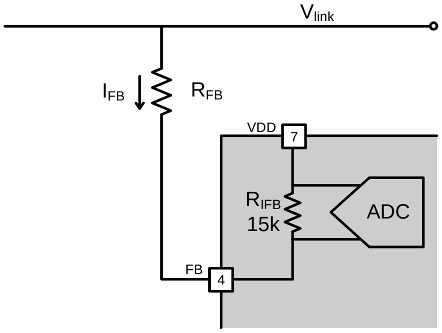


Figure 13. Output Feedback

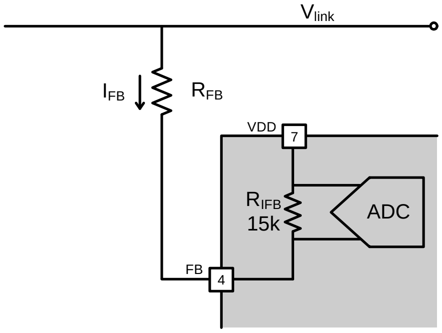


Figure 14. Input Feedforward

4.3 Protection Features

4.3.1 Overvoltage Protection

If the PFC output voltage, V_{link}, exceeds the overvoltage threshold, as scaled by the current monitored by the sense resistors, the CS1600 provides protection by disabling the gate drive. A nominal hysteresis is provided to allow the system to recover from the fault condition, before switching is resumed.

4.3.2 Overcurrent Protection

The CS1600's digital controller algorithm limits the ON time of the Power MOSFET by the following equation:

$$T_{on} \le \frac{0.001126}{V_{rect}}$$

Where T_{on} is the max time that the power MOSFET is turned on and V_{rect} is the rectified line voltage. In the event of a sudden line surge or sporadic, high dv/dt line voltages, this equation may not limit the ON time appropriately. For this type of line disturbance, additional protection mechanisms, such as fusible resistors, fast-blow fuses, or other current-limiting devices, are recommended.

4.3.3 *Overpower Protection*

The nominal output power is estimated internally by the CS1600 from the following equation

$$P_o = \alpha \times \eta \times (V_{in(min)})^2 \times \frac{V_{link} - (V_{in(min)} \times \sqrt{2})}{2 \times f_{max} \times L_B \times V_{link}} \qquad \text{[Eq.3]}$$

where

P_o = rated output power of the system

η = efficiency of the boost converter = estimated as 100% by the internal PFC algorithm

$V_{in(min)}$ = minimum RMS line voltage for operation

V_{link} = PFC output voltage

f_{max} = maximum switching frequency

L_B = boost inductor used in the application

$$\alpha = \left(\frac{V_{link}}{400V} \times \frac{90V}{V_{in(min)}}\right)^2 \times \frac{V_{link} - \left(\frac{V_{link}}{400V} \times 90V \times \sqrt{2}\right)}{V_{link} - V_{in(min)} \times \sqrt{2}}$$

Operation estimated to be at power levels higher than that calculated by Eq. 3 above is tracked by the IC as an overpower condition. During this phase, the PFC output voltage, V_{link}, is reduced and will continue to decrease as the power draw increases. When V_{link} reaches its undervoltage threshold, it goes into the start-up mode as explained in section 4.1.1.

At this point, the overpower protection timer is activated. If this condition continues to exist for 112 ms, the gate drive is disabled for a period of about 3 seconds. This “hiccup” mode of operation continues until the fault is removed.

If a value of the boost inductor other than that obtained from Eq. 3 above is used, the total output power capability as well as the thresholds for the different operating conditions will scale accordingly.

4.3.4 *Open/short circuit protection*

The CS1600 protects the system in case the feedforward resistor tied to the IAC pin or the feedback resistor tied to the FB pin is open or shorted to ground.

A fault seen on the resistor going into the FB pin would imply no current being fed into the pin, which would trigger the V_{link} undervoltage algorithm as described in Section 4.3.1.

A fault detected on the IAC pin would trigger the brownout condition discussed in Section 4.3.5 below.

4.3.5 *Brownout Protection*

Brownout occurs when the current representing the rectified input voltage, nominally 100% of the reference current used for the output voltage, drops to 49% of its nominal value. Detection of brownout for a period of 56 ms disables the gate drive. The device continues to monitor the input voltage while in this condition. The CS1600 exits the brownout mode when the input current scales up to, and stays above 56.4% of its nominal value for a period of 56 ms.

To minimize false detects, the brownout detection circuit increases the brownout detection time by a factor of 1.6 mS/V for every volt differential between the minimum operating voltage and the brownout threshold, following half of a line cycle of exceeding the brownout threshold. The following diagram illustrates the brownout sequence whereby the CS1600 enters standby, and upon recovery from brownout, enters normal operation..

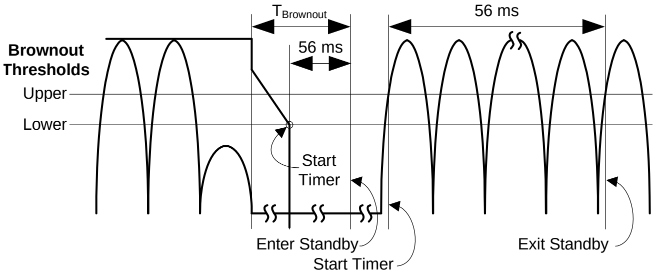


Figure 15. Brownout

4.3.6 *Over-temperature Protection*

Over-temperature protection is activated and PFC switching is disabled when the die temperature of the device exceeds 125°C. There is a hysteresis of about 30°C before resumption of normal operation.

4.4 Standby ($\overline{\text{STBY}}$) Function

The standby ($\overline{\text{STBY}}$) pin may be used as a means to force the CS1600 into a non-operating, low-power state. The $\overline{\text{STBY}}$ input should be driven by an open-collector/open-drain device. Internal to the pin, there is a pull-up resistor connected to the VDD pin as shown in Figure 16. A filter capacitance of about 1000 pF is recommended while this pin is being used.

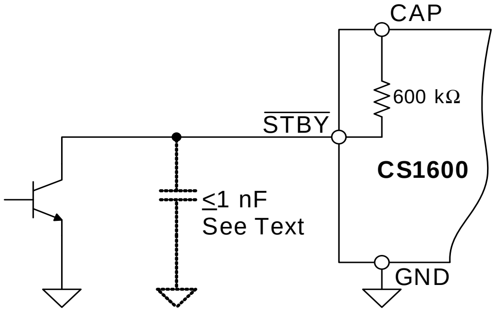


Figure 16. $\overline{\text{STBY}}$ Pin Connection

5. FLUORESCENT BALLAST APPLICATION EXAMPLE

The following section gives an example for a front-end PFC stage design for an electronic ballast application. The equations that follow may be used as guidelines for any other requirements using the CS1600.

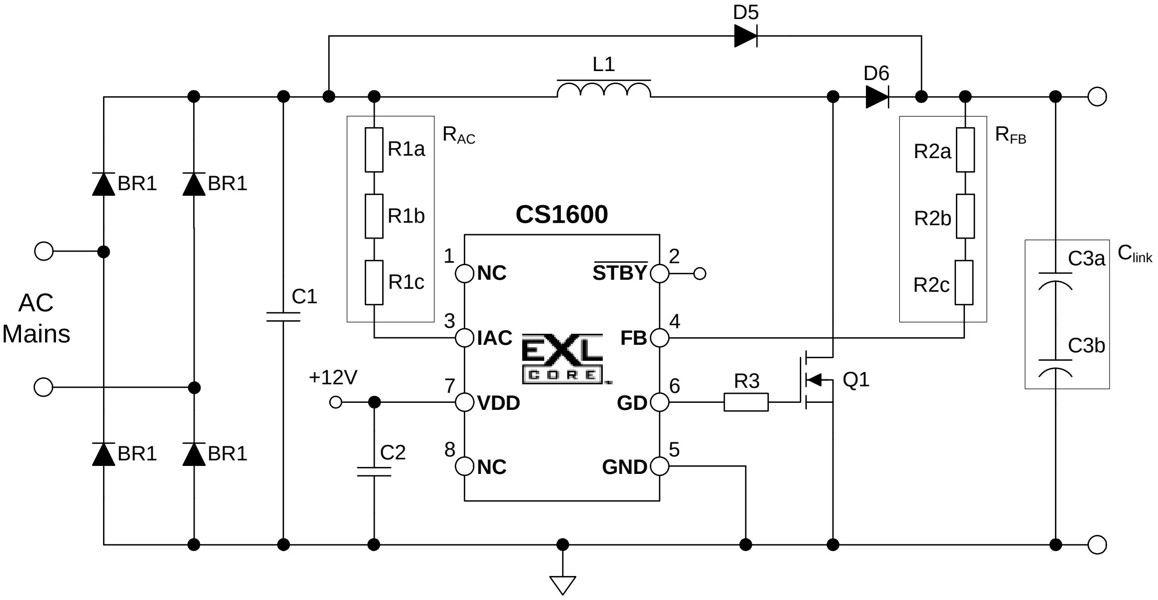


Figure 17. CS1600 Basic Application Circuit

5.1 Component Selection Guidelines

The following design example is for a wide-input-voltage fluorescent ballast application using 2 T5 lamps in series for a total nominal power of 108W.The target specifications for the PFC portion of the design, assuming a 94% efficient second stage, are as follows:

$V_{in(min)}$	108 VAC
$V_{in(max)}$	305 VAC
V_{link}	460 V
P_o	115 W
η	95%

5.1.1 I_{AC} and I_{FB} Sense Resistors

The rectified line voltage, V_{AC}, and the output voltage of the PFC boost converter, V_{link}, are scaled as currents by using sense resistors, whose values are estimated based on the equations below:

$$R_{FB} = \frac{V_{link} - V_{dd}}{I_{ref}} \qquad \text{[Eq.4]}$$

$$R_{FB} = \frac{460 - 12}{130 \times 10^{-6}}$$

$$R_{FB} = 3.45\text{M}\Omega$$

$$R_{AC} = R_{FB} \qquad \text{[Eq.5]}$$

$$R_{AC} = 3.45\text{M}\Omega$$

where

R_{FB} = Feedback resistor used to reflect the PFC output voltage

R_{AC} = Feedforward resistor used to reflect the rectified line voltage

V_{link}= PFC Output Voltage

V_{DD} = IC Supply Voltage

I_{ref} = Target reference current used for feedback

1% or lower tolerance resistors are recommended to maximize the tightly toleranced system behavior provided by the unique digital controller in the CS1600. Resistors may be separated into two or more series elements if voltage breakdown and/or regulatory compliance is of concern.

5.1.2 PFC Input Filter Capacitor

For a typical 115 W PFC output stage required to power up a 108 W fluorescent ballast, an input filter capacitance of 0.33 µF is recommended. Capacitor tolerances and the value of the EMI filter capacitor need to be considered when selecting the value of the capacitor to be used in this application.

5.1.3 PFC Boost Inductor

Equation 3 can be rewritten to calculate the PFC boost Inductor, L_B, as follows:

$$\alpha = \left(\frac{V_{link}}{400V} \times \frac{90V}{V_{in(min)}}\right)^2 \times \frac{V_{link} - \left(\frac{V_{link}}{400V} \times 90V \times \sqrt{2}\right)}{V_{link} - V_{in(min)} \times \sqrt{2}} \qquad \text{[Eq.6]}$$

$$\alpha = \left(\frac{V_{link}}{400V} \times \frac{90V}{V_{in(min)}}\right)^2 \times \frac{V_{link} - \left(\frac{V_{link}}{400V} \times 90V \times \sqrt{2}\right)}{V_{link} - V_{in(min)} \times \sqrt{2}} = 0.937$$

$$L_B = \alpha \times \eta \times (V_{in(min)})^2 \times \frac{V_{link} - (V_{in(min)} \times \sqrt{2})}{2 \times f_{max} \times P_O \times V_{link}} \qquad \text{[Eq.6]}$$

$$L_B = 0.937 \times 0.95 \times 108^2 \times \frac{(460 - 108 \times \sqrt{2})}{2 \times 70 \times 10^3 \times 115 \times 460} = 431 \mu H$$

The RMS current rating for the inductor is estimated using an scaling factor used to account for variations in the input current shape across the AC line cycle, over and above the nominally calculated value. The nominal value before using the scaling factor is as follows:

$$I_{LB(rms)} = \frac{P_O}{V_{in(min)} \times \sqrt{2} \times \eta} \times \beta \qquad \text{[Eq.7]}$$

$$I_{LB(rms)} = \frac{115}{108 \times \sqrt{2} \times 0.95} \times 1.35$$

$$I_{LB(rms)} = 1.07 A$$

where

β = inductor scaling factor

The peak inductor current, $I_{LB(pk)}$, may be estimated using the following equation:

$$I_{LB(pk)} = \frac{4 \times P_O}{\eta \times V_{in(min)} \times \sqrt{2}} \qquad \text{[Eq.8]}$$

$$I_{LB(pk)} = \frac{4 \times 115}{0.95 \times 108 \times \sqrt{2}}$$

$$I_{LB(pk)} = 3.17 \ A$$

Inductor tolerances should be considered when estimating the peak currents present in the application.

The internal control algorithm of the controller dictates that the peak inductor current seen in the application could be as high as a pre-defined threshold of 0.001984 times the inverse of the inductor, which in this example amounts to 4.72 A. Care needs to be taken to ensure that the saturation current rating of the PFC boost inductor factors in this threshold used for the protection schemes.

For a 40 V ripple and minimum line frequency of 45 Hz, the

5.1.4 PFC MOSFET

The peak voltage stress on the PFC MOSFET is a diode drop above the output voltage. Accounting for leakage spikes, for the 460 V output application, a 600 V FET is recommended.

The FET should be able to handle the same peak current as that seen through the inductor. This would amount to 3.96 A.

The scaling factor to determine the RMS current through the MOSFET for a 108 V input is about 1.15, and the minimum RMS current rating, $I_{FET(rms)}$, required for the FET is calculated as follows:

$$I_{FET(rms)} = \frac{P_O}{V_{in(min)} \times \sqrt{2} \times \eta} \times \gamma \qquad \text{[Eq.9]}$$

$$I_{LB(rms)} = \frac{115}{108 \times \sqrt{2} \times 0.95} \times 1.15$$

$$I_{LB(rms)} = 0.91 A$$

where

γ = FET scaling factor

5.1.5 PFC Diode

The PFC diode peak current is equal to the inductor peak current:

$$I_{D(pk)} = I_{LB(pk)} \qquad \text{[Eq.10]}$$

$$I_{D(pk)} = 3.17 \ A$$

The PFC diode average current is calculated as follows:

$$I_{D(avg)} = \frac{P_O}{V_{link}} \qquad \text{[Eq.11]}$$

$$I_{D(avg)} = \frac{115}{460}$$

$$I_{D(avg)} = 0.25 A$$

5.1.6 PFC Output Capacitor

The output capacitor needs to be designed to meet the voltage ripple and hold-up time requirements. In the case of a cost-sensitive ballast application, the hold-up requirement is not a key requirement.

To address the output ripple requirements, the following equation may be used as a guide:

$$C_{out} = \frac{P_O}{2\pi \times f_{line(min)} \times V_{link} \times \Delta V_{link(rip)}} \qquad \text{[Eq.12]}$$

where

C_{out} = Output Capacitance value

P_o = Output Power

$f_{line(min)}$ = Minimum Line Frequency

V_{link} = PFC Output Voltage

ΔV_{link} = Peak-Peak Voltage Ripple on the PFC Output

output capacitance needed is calculated as:

$$C_{out} = \frac{115}{2\pi \times 45 \times 460 \times 40} = 22.1\mu F$$

The voltage rating on the capacitor needs to account for the operation of the device before it hits the overvoltage protection threshold. This is typically 105% of nominal value, which is 483 V. With the ripple voltage factored in, 22 µF of capacitance rated at 500 V would suffice for this application.

5.2 Bill of Materials (for Application Example shown in Figure 17)

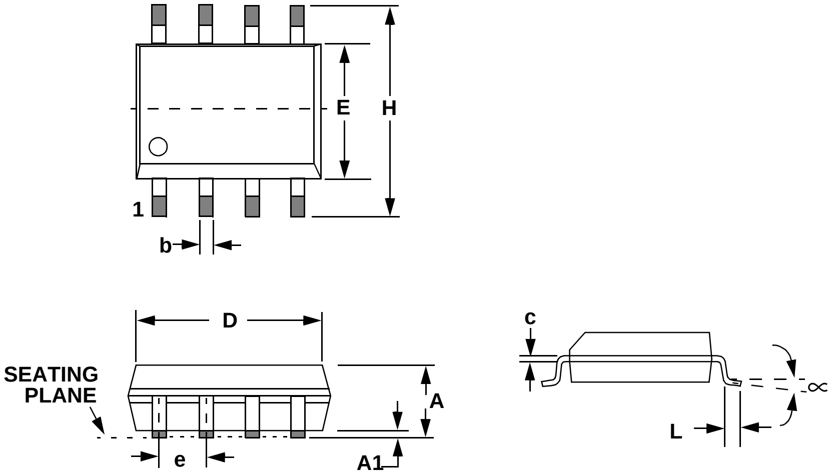
Designator	Value	Description/Part Number
R1a	1.5 MΩ	
R1b	1.5 MΩ	
R1c	1.5 MΩ	
R2a	1.5 MΩ	
R2b	1.5 MΩ	
R2c	1.5 MΩ	
R3	24.9Ω	
C1	0.47µF	
C2	4.7µF	
C3a	23.5µF	2 47µF, 250V caps in series
C3b		
BR1	4A, 600V	Bridge diode - GBU4J-BP
D5	1 A, 600	1N4005
D6	3A, 600V	MURS360
L1	360µH (max)	TBD (Premier Magnetics)
Q1	9A, 600V	FCP9N60N
CS1600	-	CS1600-FSZ

5.3 Summary of Equations

Eq. #	Equation
1, 4	$R_{FB} = \frac{V_{link} - V_{DD}}{I_{ref}}$
2, 5	$R_{AC} = R_{FB}$
3, 6	$P_O = \alpha \times \eta \times (V_{in(min)})^2 \times \frac{V_{link} - (V_{in(min)} \times \sqrt{2})}{2 \times f_{max} \times L_B \times V_{link}}$
7	$I_{LB(rms)} = \frac{P_O}{V_{in(min)} \times \sqrt{2} \times \eta} \times \beta$
8	$I_{LB(pk)} = \frac{4 \times P_O}{\eta \times V_{in(min)} \times \sqrt{2}}$
9	$I_{FET(rms)} = \frac{P_O}{V_{in(min)} \times \sqrt{2} \times \eta} \times \gamma$
10	$I_{D(pk)} = I_{LB(pk)}$
11	$I_{D(avg)} = \frac{P_O}{V_{link}}$
12	$C_{out} = \frac{P_O}{2\pi \times f_{line(min)} \times V_{link} \times \Delta V_{link(rip)}}$

6. PACKAGE DRAWING

8L SOIC (150 MIL BODY) PACKAGE DRAWING



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.19	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.80	4.00
e	0.040	0.060	1.02	1.52
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
∝	0°	8°	0°	8°

JEDEC # : MS-012

7. ORDERING INFORMATION

Part #	Temperature Range	Package Description
CS1600-FSZ	-40 °C to +125 °C	8-lead SOIC, Lead (Pb) Free

8. ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

Model Number	Peak Reflow Temp	MSL Rating[a]	Max Floor Life[b]
CS1600-FSZ	260 °C	2	365 Days

[a] MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

[b] Stored at 30 °C, 60% relative humidity.

9. REVISION HISTORY

Revision	Date	Changes
A1	OCT 2009	Initial Advance Information release.
A2	MAR 2010	Revised feature list, product description and parametric table to reflect the C0 version of silicon.
A3	MAR 2010	Revised to reflect the update in switching frequency and variation of frequency over line.
A4	APR 2010	Revised parametric table and equations to reflect the C1 version of silicon.
A5	MAY 2010	Updated with additional test bench data for EP level.
A6	JUN 2010	Added $R\theta_{JA}$ and $R\theta_{JC}$ in electrical specifications section.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to http://www.cirrus.com

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