Flash-ROM Module 8MByte (4Mx16bit), 68-pin JLCC type, 3.3V Design **Part No. HMF4M16J4V**

GENERAL DESCRIPTION

The HMF4M16J4V is a high-speed flash read only memory (FROM) module containing 2,097,152 words organized in an x16bit configuration. The module consists of four 2M x 8bit FROM mounted on a 68-pin, JLCC connector FR4-printed circuit board.

Commands are written to the command register using standard microprocessor write timings.

Register contents serve as input to an internal state-machine, which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0V flash or EPROM devices.

Output enable (/OE) and write enable (/WE) can set the memory input and output. The host system can detect a program or erase operation is complete by observing the Ready Pin, or reading the DQ7(Data # Polling) and DQ6(Toggle) status bits.

When FROM module is disable condition the module is becoming power standby mode, system designer can get low -power design. All module components may be powered from a single + 3V DC power supply and all inputs and outputs are LVTTL-compatible.

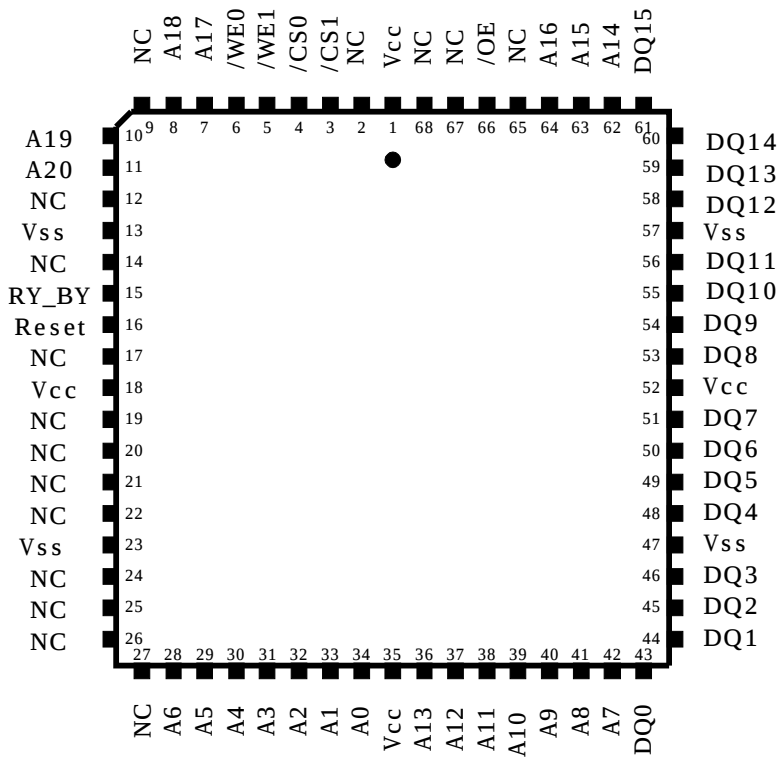
FEATURES

- Part identification
  - HMF4M16J4V
    (Bottom boot block configuration)
- Access time: 70, 80, 90, 120ns
- High-density 8MByte design
- High-reliability, low-power design
- Single + 3V to 3.6V power supply
- 68-Pin JLCC Designed
- Minimum 1,000,000 write cycle guarantee per sector
- 20-year data retention at 125 ^{O}C
- Flexible sector architecture
- Embedded algorithms
- Erase suspend / Erase resume

OPTIONS MARKING

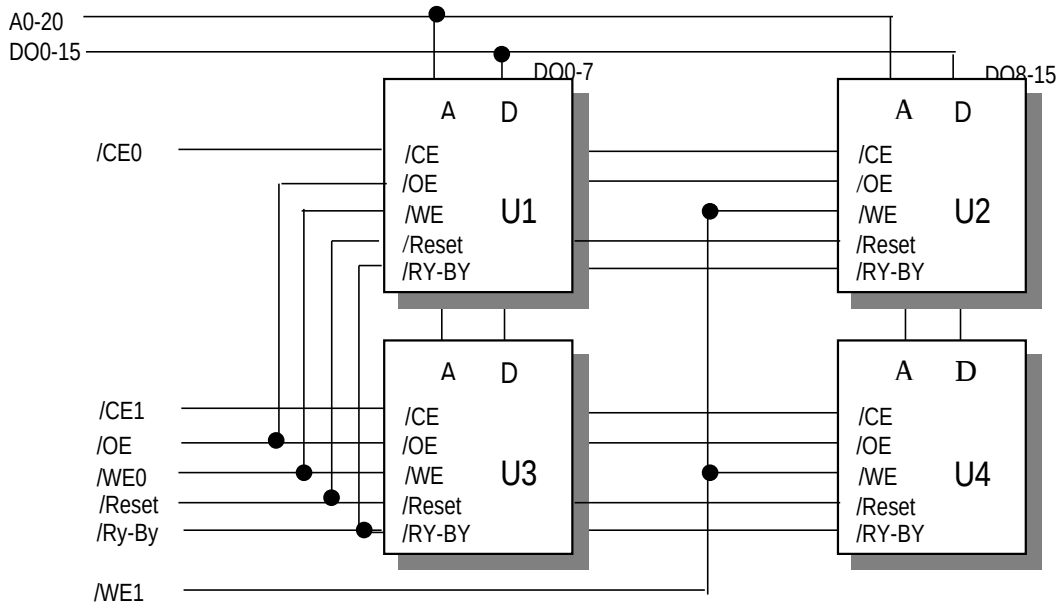
- Timing
  - 70ns access - 70
  - 80ns access - 80
  - 90ns access - 90
  - 120ns access -120
- Packages
  - 68-pin JLCC J

PIN ASSIGNMENT



68-Pin JLCC TOP View

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	/CS	/OE	/WE	RESET	DQ
STANDBY	Vcc±0.3V	X	X	Vcc±0.3V	HIGH-Z
RESET	X	X	X	L	HIGH-Z
SECTOR PROTECT	L	H	L	V_{ID}	D_{IN}, D_{OUT}
SECTOR UNPROTECT	L	H	L	V_{ID}	D_{IN}, D_{OUT}
READ	L	L	H	H	D_{OUT}
WRITE	L	H	L	H	D_{OUT}

Note : X means don't care, WE0* Low byte (D0~7) Write enable, WE1* High byte(D8~15) Write enable.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
Voltage on Any Pin Relative to Vss	-0.5V to Vcc +0.5V
Voltage on Vcc Supply Relative to Vss	-0.5V to +4.0V
Output Short Circuit Current	1,600mA
Storage Temperature	-65^{O}C to +150^{O}C
Operating Temperature	-0^{O}C to +70^{O}C

w Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RANGE
Vcc for regulated Supply Voltage	+3.0V to 3.6V
Vcc for full voltage	+2.7V to 3.6V

DC AND OPERATING CHARACTERISTICS

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	MAX	UNITS
Input Load Current	V_{IN}= V_{SS} to V_{CC} , V_{CC}= V_{CC} max	I_{L1}		±8.0	μA
Output Leakage Current	V_{OUT}= V_{SS} to V_{CC}, V_{CC}= V_{CC} max	I_{L0}		±8.0	μA
Output High Voltage	I_{OH} = -2.0mA, Vcc = Vcc min	V_{OH}	0.85Vcc		V
Output Low Voltage	I_{OL} = 4.0mA, Vcc = Vcc min	V_{OL}		0.45	V
Vcc Active Read Current	/CE = V_{IL}, ,/OE=V_{IH}, f=5MHz	I_{CC1}		128	mA
Vcc Active Write Current	/CE = V_{IL}, /OE=V_{IH}	I_{CC2}		240	mA
Vcc Standby Current	/CE, RESET=V_{CC}±0.3V	I_{CC3}		40	μA
Vcc Reset Current	/RESET=Vss±0.3V,	I_{CC4}		40	μA
Low Vcc Lock-Out Voltage		V_{LKO}	2.3	2.5	V

ERASE AND PROGRAMMING PERFORMANCE

PARAMETER	LIMITS			UNIT	COMMENTS
	MIN.	TYP.	MAX.		
Sector Erase Time	-	0.7	15	Sec	Excludes 00H programming prior to erasure
Byte Programming Time	-	9	300	μS	Excludes system-level overhead
Chip Programming Time	-	18	54	sec	Excludes system-level overhead

TSOP PIN CAPACITANCE

PARAMETER SYMBOL	PARAMETER DESCRIPTION		TEST SETUP	TYP.	MAX	UNIT
C_{IN}	Input Capacitance	Address	V_{IN} = 0	48	60	pF
		Data		24	30	
C_{OUT}	Output Capacitance		V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	/CE	V_{IN} = 0	7.5	9	pF
		/WE		30	36	
		/OE		60	72	

Notes: Test conditions T_A = 25° C, f=1.0 MHz.

AC CHARACTERISTICS

u Read Only Operations Characteristics

PARAMETER SYMBOLS		DESCRIPTION	TEST SETUP		-80 (NOTE1)	-90 (NOTE1)	UNIT
JEDEC	STANDARD						
t_{AVAV}	t_{RC}	Read Cycle Time		Min	80	90	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	/CE = V_{IL} /OE = V_{IL}	Max	80	90	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	/OE = V_{IL}	Max	80	90	ns
t_{GLQV}	t_{OE}	Chip Enable to Output Delay		Max	80	90	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High-Z		Max	25	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High-Z		Max	25	30	ns
t_{AXQX}	t_{QH}	Output Hold Time From Addresses, /CE or /OE, Whichever Occurs First		Min	0	0	ns

TEST CONDITIONS

Notes : Test Conditions : Output Load : 1TTL gate and 100 pF

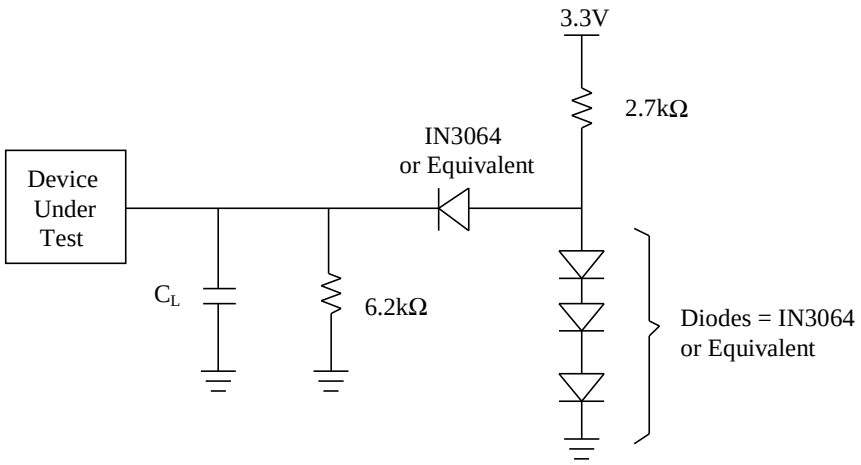
Input rise and fall times : 5 ns

Input pulse levels: 0V to 3.0V

Timing measurement reference level

Input : 1.5 V

Output : 1.5V



Note : C_L = 100pF including jig capacitance

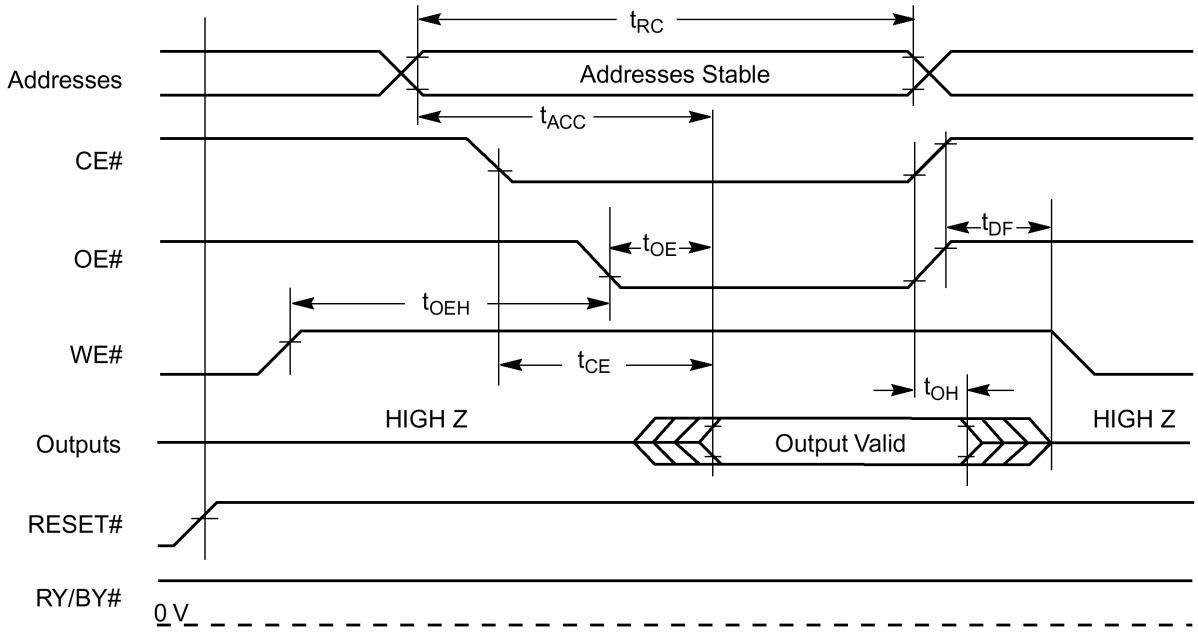
u Erase/Program Operations

PARAMETER SYMBOLS		DESCRIPTION		-80	-90	UNIT
JEDEC	STANDARD					
t_{AVAV}	t_{WC}	Write Cycle Time	Min	80	90	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	45	45	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	35	45	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0	0	ns
	t_{OES}	Output Enable Setup Time	Min	0	0	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write	Min	0	0	ns
t_{ELWL}	t_{CS}	/CE Setup Time	Min	0	0	ns
t_{WHEH}	t_{CH}	/CE Hold Time	Min	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	35	35	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min	30	30	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation	Typ	9	9	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation	Typ	0.7	0.7	sec
			Max	50	50	sec
	t_{VCS}	Vcc Setup Time	Min	50	50	µs
	t_{RB}	Recovery time from RY/BY	Min	0	0	µs
	t_{BUSY}	Program/Erase Valid to RY/BY Delay	Min	90	90	µs

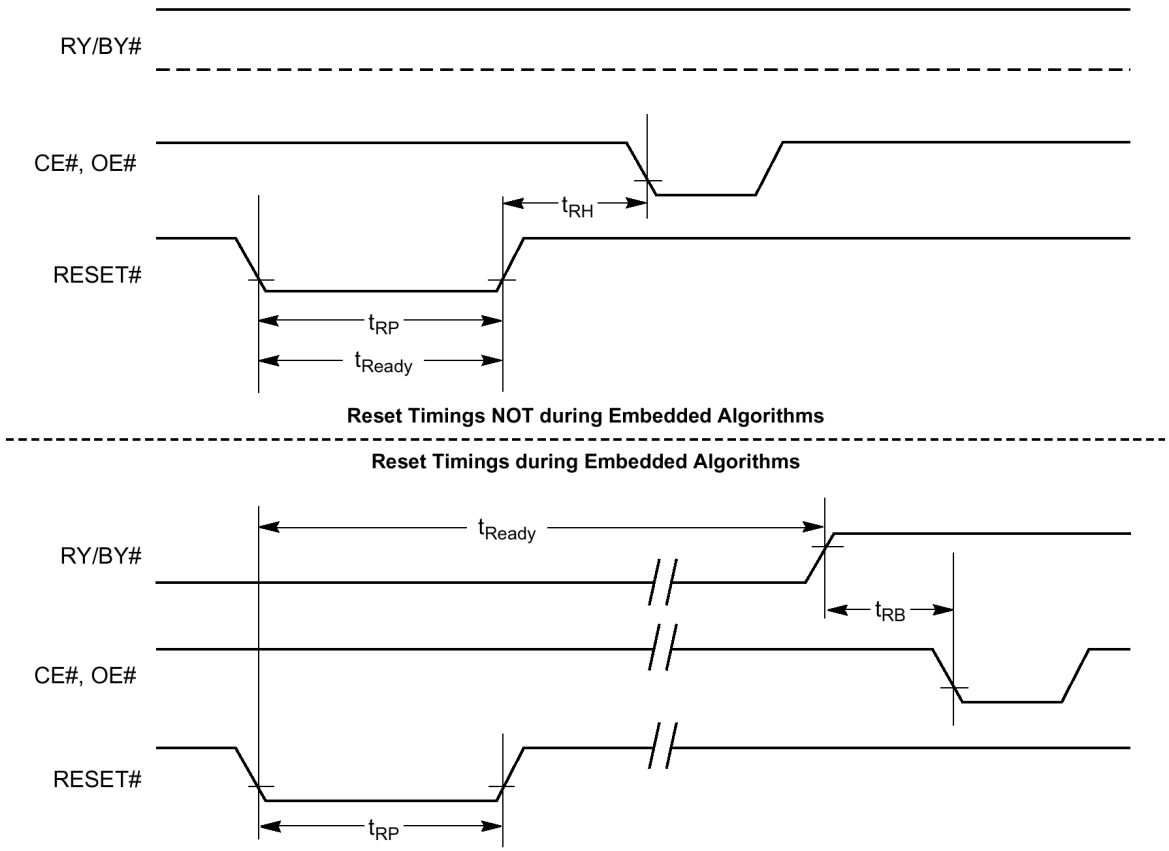
u Alternate /CE Controlled Erase/Program Operations

PARAMETER SYMBOLS		DESCRIPTION		-80	-90	UNIT
JEDEC	STANDARD					
t_{AVAV}	t_{WC}	Write Cycle Time	Min	80	90	ns
t_{AVEL}	t_{AS}	Address Setup Time	Min	0	0	ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	45	45	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	35	45	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0	0	ns
	t_{OES}	Output Enable Setup Time	Min	0	0	ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write /OE High to /WE Low	Min	0	0	ns
t_{WLEL}	t_{WS}	/WE Setup Time	Min	0	0	ns
t_{EHWH}	t_{WH}	/WE Hold Time	Min	0	0	ns
t_{ELEH}	t_{CP}	/CE Pulse Width	Min	35	35	ns
t_{EHEL}	t_{CPH}	/CE Pulse Width High	Min	30	30	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation	Typ	9	9	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation	Typ	0.7	0.7	sec

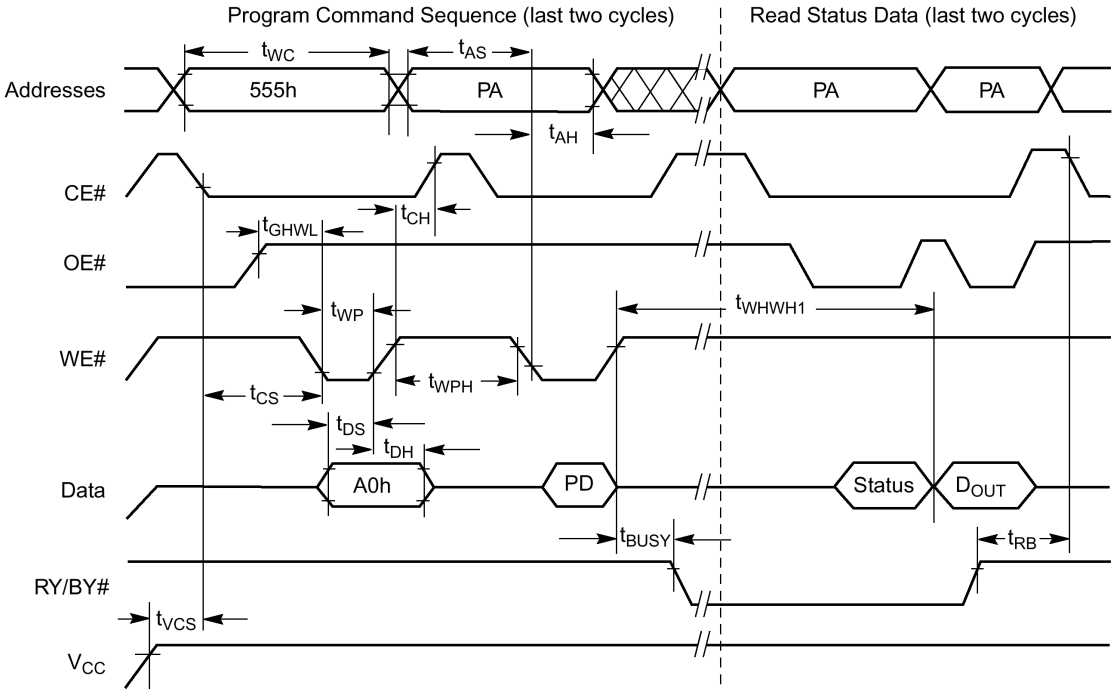
u READ OPERATIONS TIMING



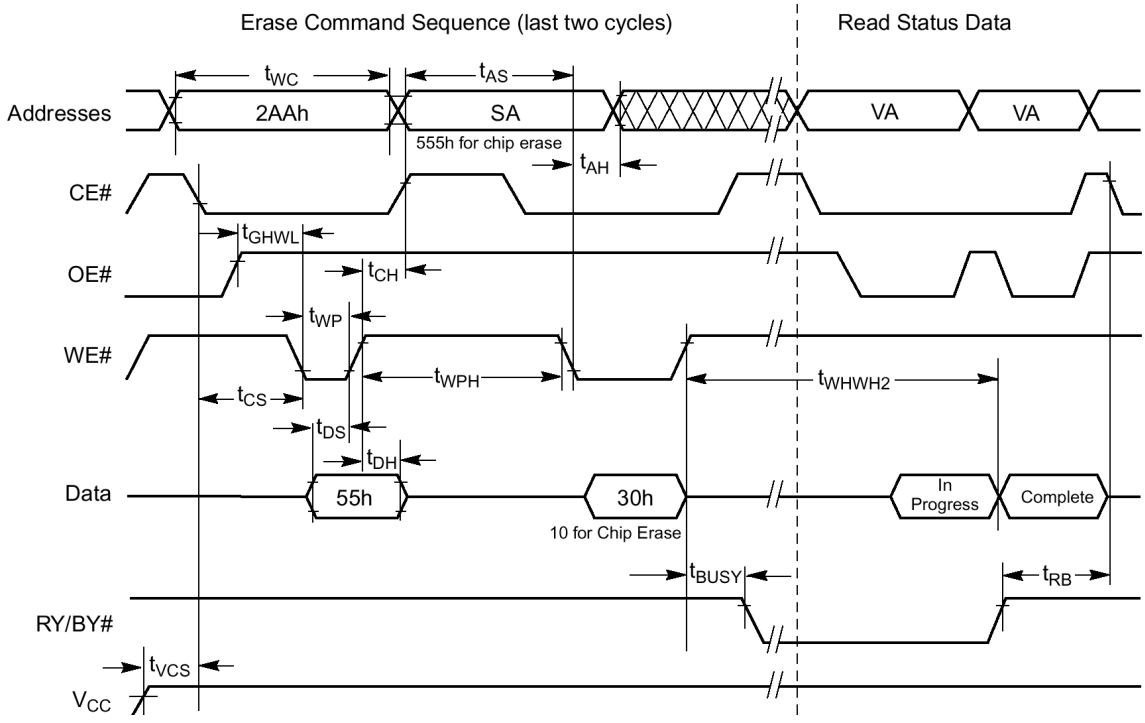
u RESET TIMING



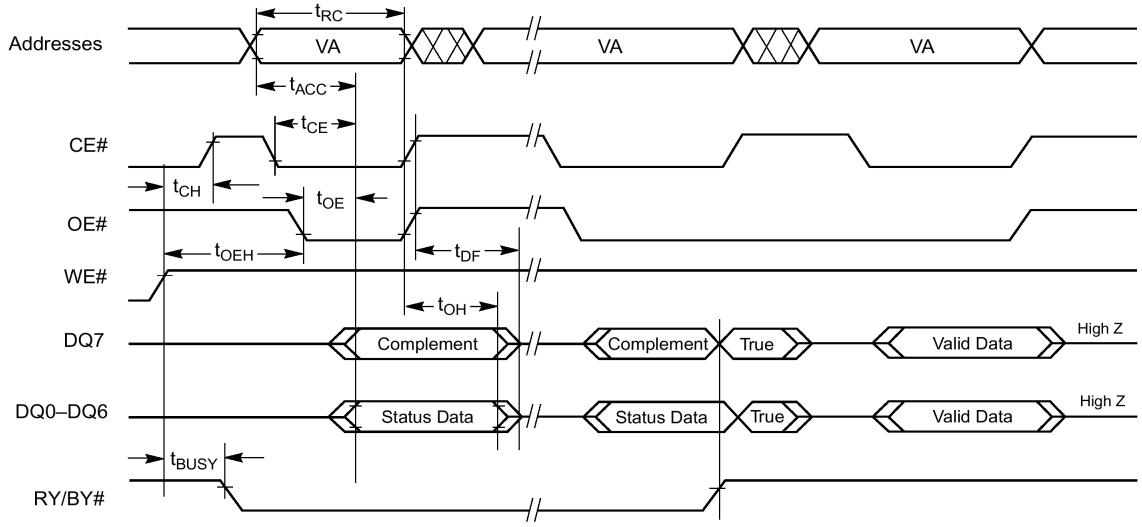
u PROGRAM OPERATIONS TIMING



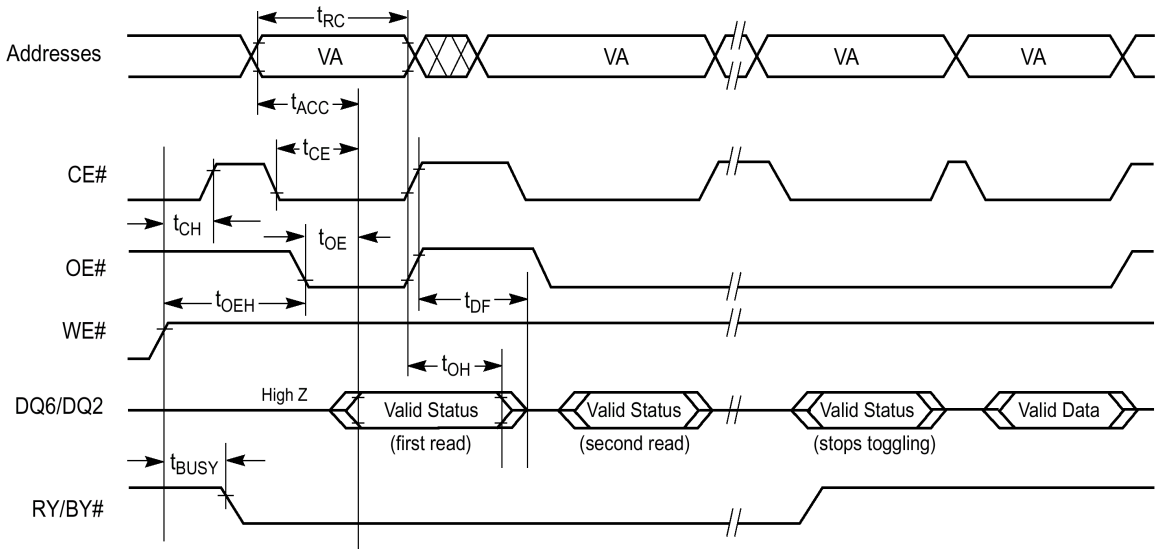
u CHIP/SECTOR ERASE OPERATION TIMINGS



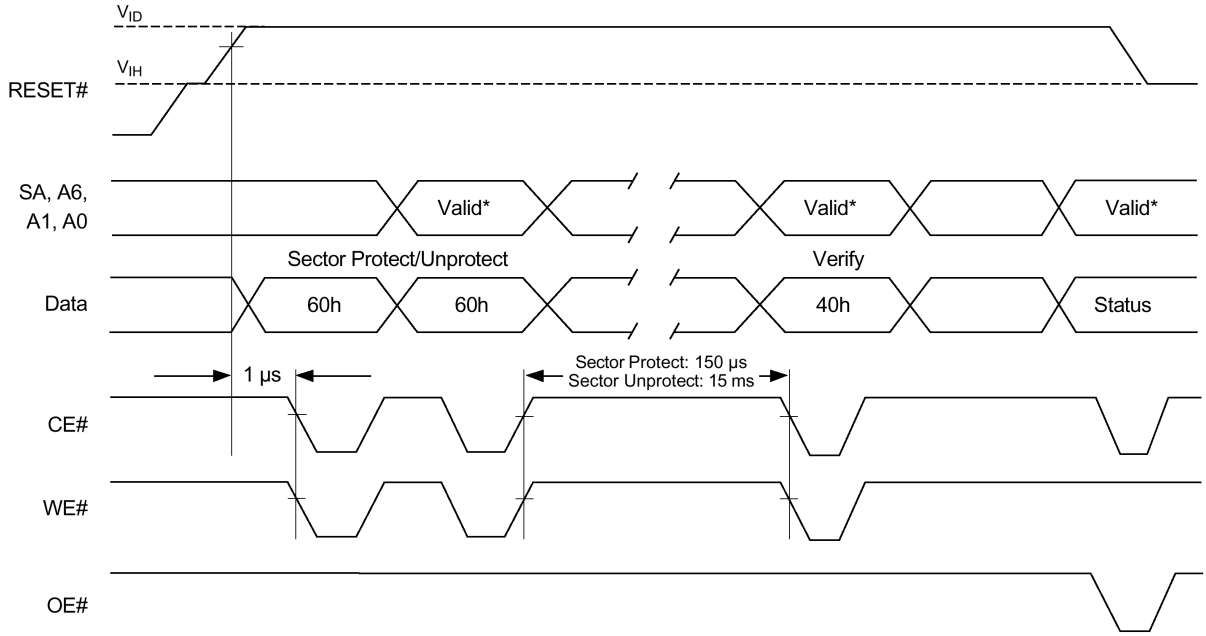
u DATA# POLLING TIMES(DURING EMBEDDED ALGORITHMS)



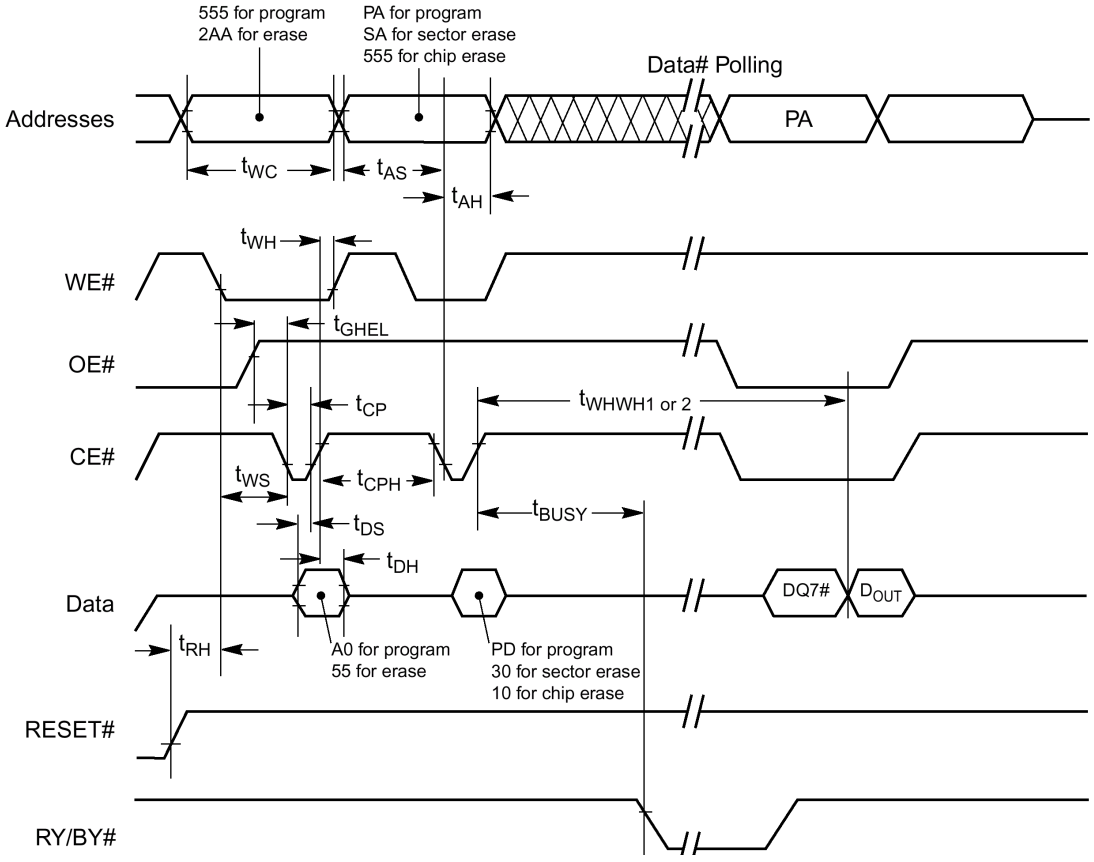
u TOGGLE# BIT TIMINGS (DURING EMBEDDED ALGORITHMS)



u SECTOR PROTECT UNPROTECT TIMEING DIAGRAM



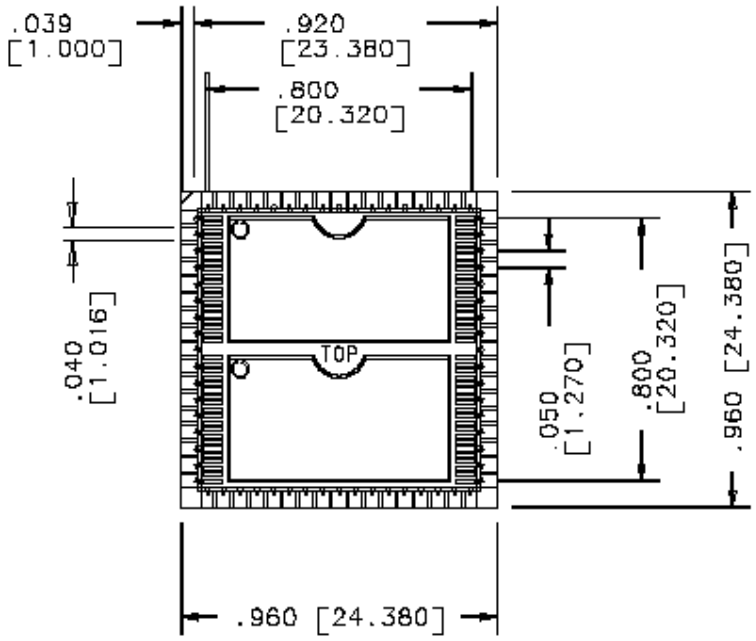
u ALTERNATE CE# CONTROLLED WRITE OPERATING TIMINGS

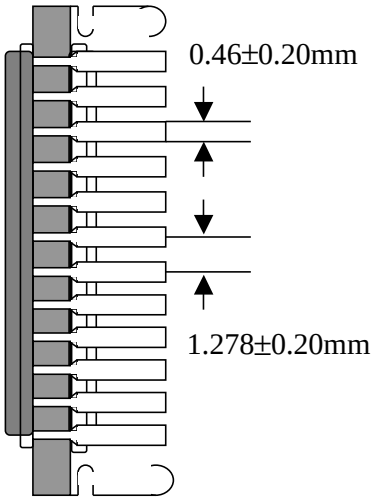


PACKAGE DIMENSIONS

UNIT: inch(mm)

(TOP Dimension**)**





ORDERING INFORMATION

Part Number	Density	Org.	Package	Component Number	Vcc	SPEED
HMF4M16J4V-70	8MByte	x 16	68Pin -JLCC	4EA	3.3V	70ns
HMF4M16J4V -80	8MByte	x 16	68Pin -JLCC	4EA	3.3V	80ns
HMF4M16J4V -90	8MByte	x 16	68Pin -JLCC	4EA	3.3V	90ns
HMF4M16J4V -120	8MByte	x 16	68Pin -JLCC	4EA	3.3V	120ns