Three-cell Lithium-Ion Battery Protection IC

FEATURES

- Ultra-low quiescent current of 13μA (V_{cell} = 3.5V).
- Ultra-low power-down current of 1.3μA (V_{cell} = 2.3V).
- Wide supply voltage range: 2V to 18V.
- Precision over-charge protection voltage:
  - 4.35V±30mV for the SS6803A
  - 4.30V±30mV for the SS6803B
  - 4.25V±30mV for the SS6803C
  - 4.20V±30mV for the SS6803D
- Externally set over-charge, over-discharge and over-current delay time.
- Built-in cell-balancing bleeding network under over-charge condition.
- Three detection levels for over-current protection.

APPLICATIONS

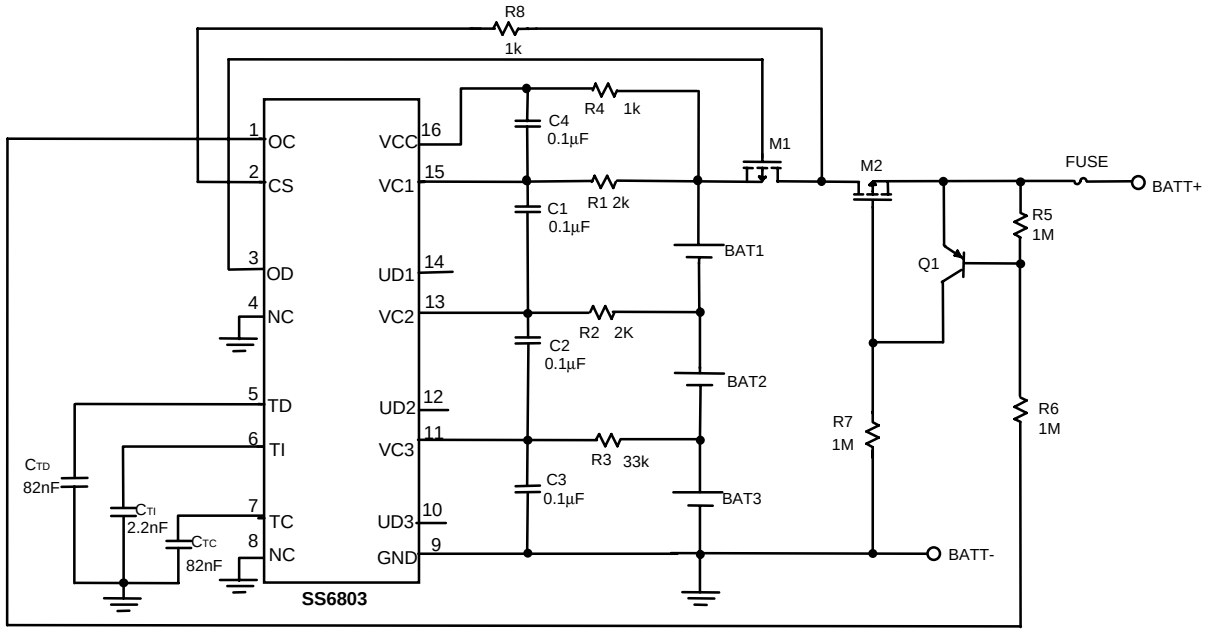
Protection IC for three-cell lithium-ion battery pack.

DESCRIPTION

The SS6803 is designed to protect a lithium-ion battery from damage or degraded lifetime due to over-charging, over-discharging and over-current for three-cell lithium-ion battery powered systems such as notebook PCs.
It provides the cell-balancing "bleeding" function to automatically discharge the over-charged cell until the over-charge condition is eliminated.

Safe charging with full utilization is ensured by the accurate ±30mV over-charge detection. Four different specification values for over-charge protection voltage are provided for various protection requirements. The very low standby current represents little drain from the cell while in storage.

TYPICAL APPLICATION CIRCUIT



Protection Circuit for a Three-cell Lithium-Ion Battery Pack

ORDERING INFORMATION

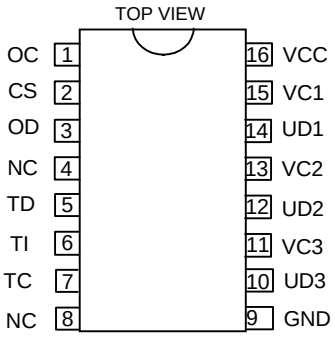
SS6803XCXXX

- Packing type
  - TR: Tape and reel
  - TB: Tube
- Package type
  - S: SO-16
- Over-charge Protection Voltage
  - A: 4.35V
  - B: 4.30V
  - C: 4.25V
  - D: 4.20V

Example: SS6803ACSTR

→ 4.35v version, in SO-16, packed on tape and reel

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

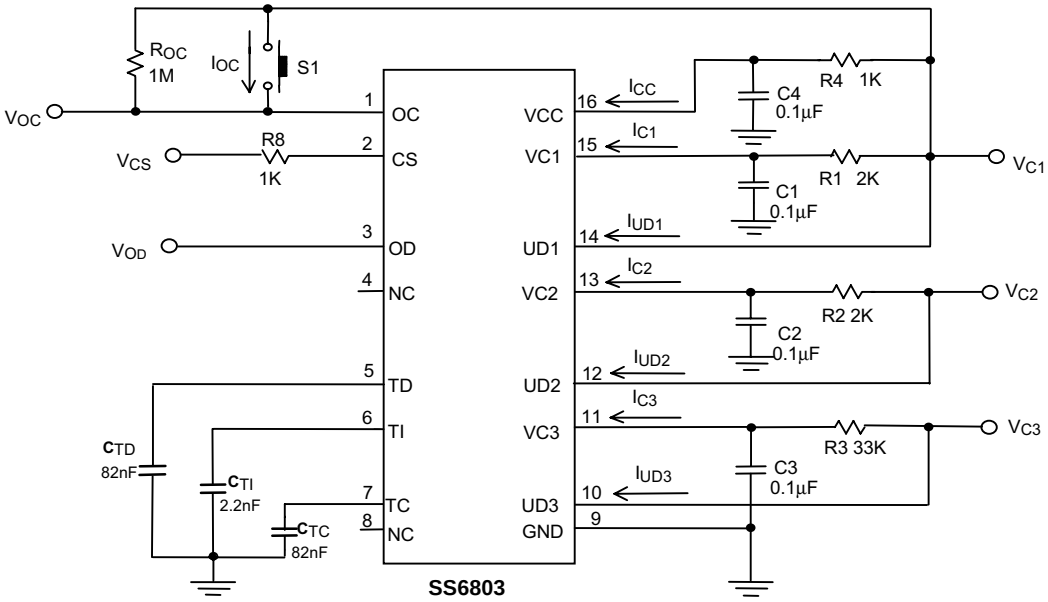
Supply Voltage 18V

DC Voltage Applied on other Pins 18V

Operating Temperature Range..... -20°C~70°C

Storage Temperature Range ..... - 65°C ~125°C

TEST CIRCUIT



ELECTRICAL CHARACTERISTISTICS (T_A = 25°C unless otherwise specified.)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
VCC Pin Input Current in Normal Mode	V_{CELL}=3.5V	I_{CC}		13	20	µA
VC1 Pin Input Current in Normal Mode	V_{CELL}=3.5V	I_{C1}		0.4	1.0	µA
VC2 Pin Input Current in Normal Mode	V_{CELL}=3.5V	I_{C2}		0.4	1.0	µA
VC3 Pin Input Current in Normal Mode	V_{CELL}=3.5V	I_{C3}		0.2	0.5	µA
Vcc Pin Input Current in Power-Down Mode	V_{CELL}=2.3V	$I_{CC(PD)}$		1.3	2	µA
VC1,VC2,VC3 Input Current in Power-Down Mode	V_{CELL}=2.3V	$I_{C(PD)}$		0.01	0.15	µA
Overcharge Protection Voltage	SS6803A	V_{OCP}	4.32	4.35	4.38	V
	SS6803B		4.27	4.30	4.33	
	SS6803C		4.22	4.25	4.28	
	SS6803D		4.17	4.20	4.23	
Overcharge Hysteresis Voltage		V_{HYS}	150	200	250	mV
Overdischarge Protection Voltage		V_{ODP}	2.27	2.40	2.53	V
Overdischarge Release Voltage		V_{ODR}	2.85	3.00	3.15	V
Overcurrent Protection Voltage	V_{CELL}=3.5V	V_{OIP}	135	150	165	mV
Overcharge Delay Time	V_{CELL1}=V_{OCP}-30mV →V_{OCP}+30mV V_{CELL2}= V_{CELL3}=3.5V , C_{TC}=1nF	T_{OC}	10	21	32	ms
Overdischarge Delay Time	V_{CELL1}= 2.5V→ 2.3V V_{CELL2}= V_{CELL3}=3.5V, C_{TD}=1nF	T_{OD}	10	21	32	ms

ELECTRICAL CHARACTERISTICS (continued)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Overcurrent Delay Time (1)	V_{CELL}= 3.5V 0.15V<V_{CC} - V_{CS} <0.3V, C_{TI}=2.2nF	T_{OI1}	7	15	23	ms
Overcurrent Delay Time (2)	V_{CELL}=3.5V, 0.3V<V_{CC}-V_{CS}<1.0V	T_{OI2}	2	4	6	ms
Overcurrent Delay Time (3)	V_{CELL}=3.5V V_{CC}– V_{CS}>1.0V	T_{OI3}	150	300	450	µs
OC Pin Sink Current	V_{CELL1}=4.4V, V_{CELL2}= V_{CELL3}=3.5V, OC Pin Short to V_{CC}	I_{OC}	2.0	2.8	3.6	mA
OD Pin Output “H” Voltage		V_{DH}	V_{CC}-0.15V		V_{CC}-0.03V	V
OD Pin Output “L” Voltage		V_{DL}		0.01	0.15	V
Charge Detection Threshold Voltage	V_{CELL}=2.3V	V_{CH}		V_{CC} +0.4	V_{CC} +0.55	V
UD1 Pin Cell-Balancing Bleeding Current	V_{CELL1}=4.4V, V_{CELL2}= V_{CELL3}=3.5V	I_{UD1}	5.9	8.4	10.9	mA
UD2 Pin Cell-Balancing Bleeding Current	V_{CELL2}=4.4V, V_{CELL1}= V_{CELL3}=3.5V	I_{UD2}	6.1	8.7	11.3	mA
UD3 Pin Cell-Balancing Bleeding Current	V_{CELL3}=4.4V, V_{CELL1}= V_{CELL2}=3.5V	I_{UD3}	6.4	9.2	12.0	mA

Note: V_{CELL} means the battery cell voltage. Therefore,
$V_{CELL1} = V_{C1} – V_{C2}$
$V_{CELL2} = V_{C2} – V_{C3}$
$V_{CELL3} = V_{C3}$

TYPICAL PERFORMANCE CHARACTERISTICS

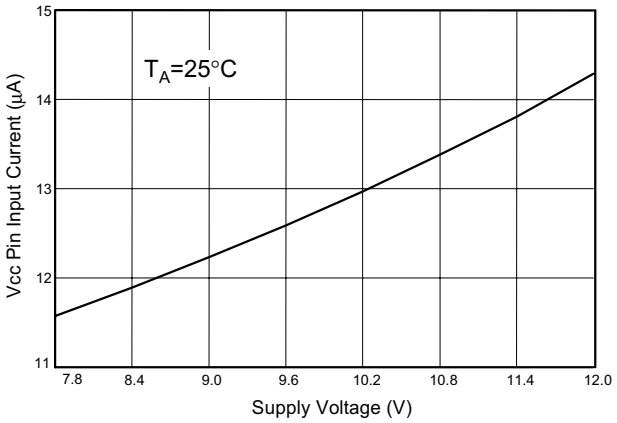


Fig. 1 Vcc Pin Input Current vs. Supply Voltage

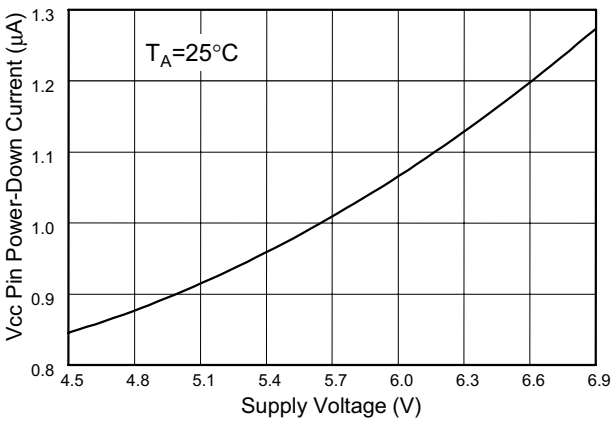


Fig. 2 Vcc Pin Power-Down Current vs. Supply Voltage

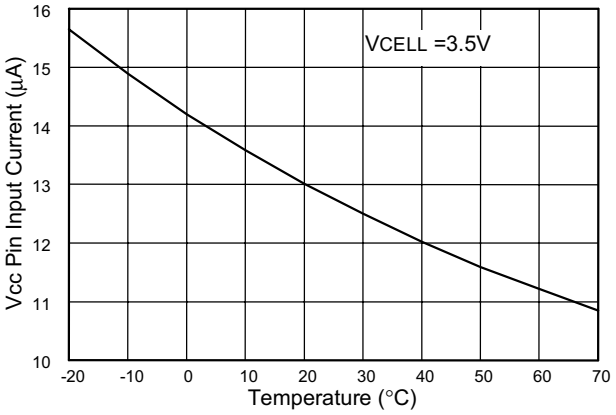


Fig. 3 Vcc Pin Input Current vs. Temperature

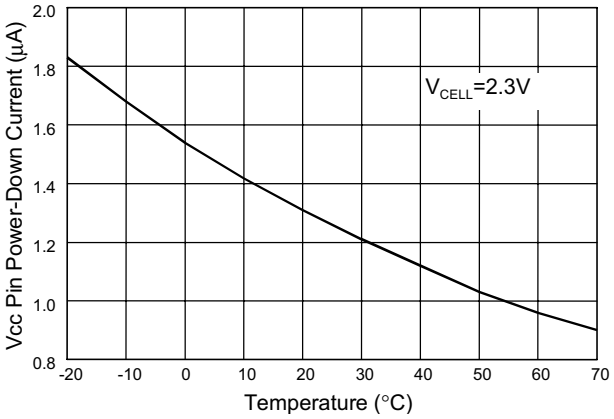


Fig. 4 Vcc Pin Power-Down Current vs. Temperature

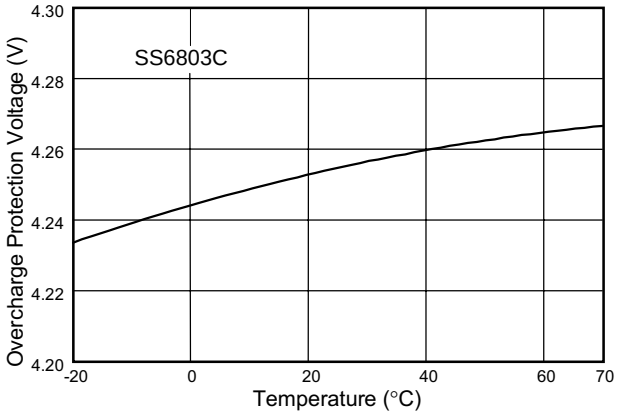


Fig. 5 Overcharge Protection Voltage vs. Temperature

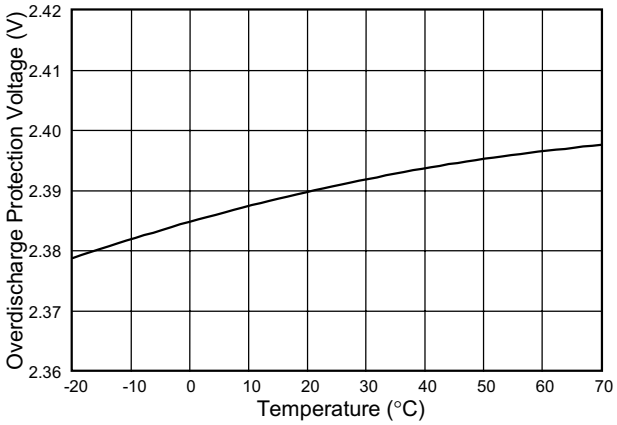


Fig. 6 Overdischarge Protection Voltage vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

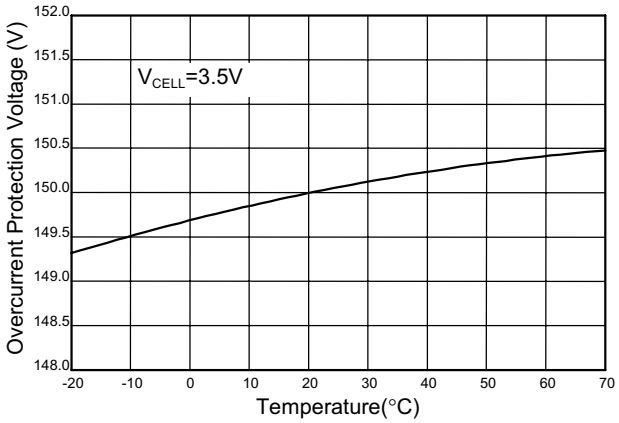


Fig. 7 Overcurrent Protection Voltage vs. Temperature

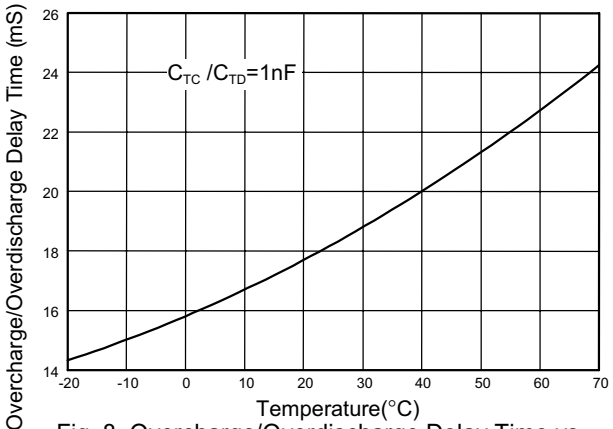


Fig. 8 Overcharge/Overdischarge Delay Time vs. Temperature

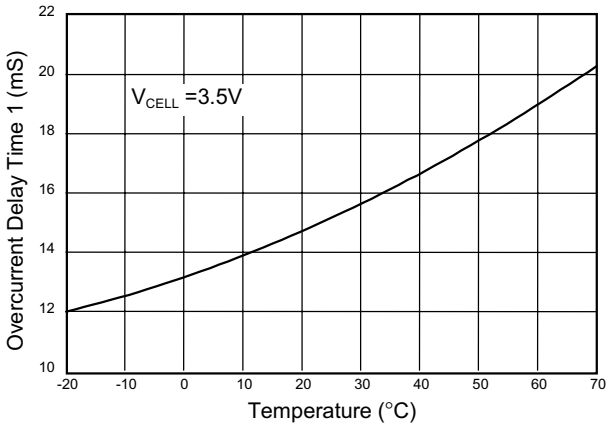


Fig. 9 Overcurrent Delay Time 1 vs. Temperature

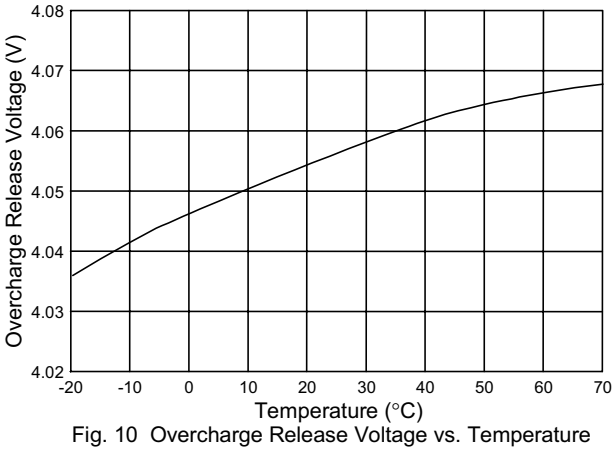


Fig. 10 Overcharge Release Voltage vs. Temperature

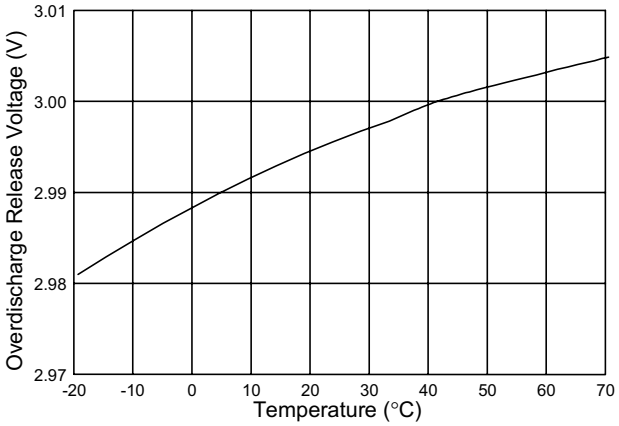
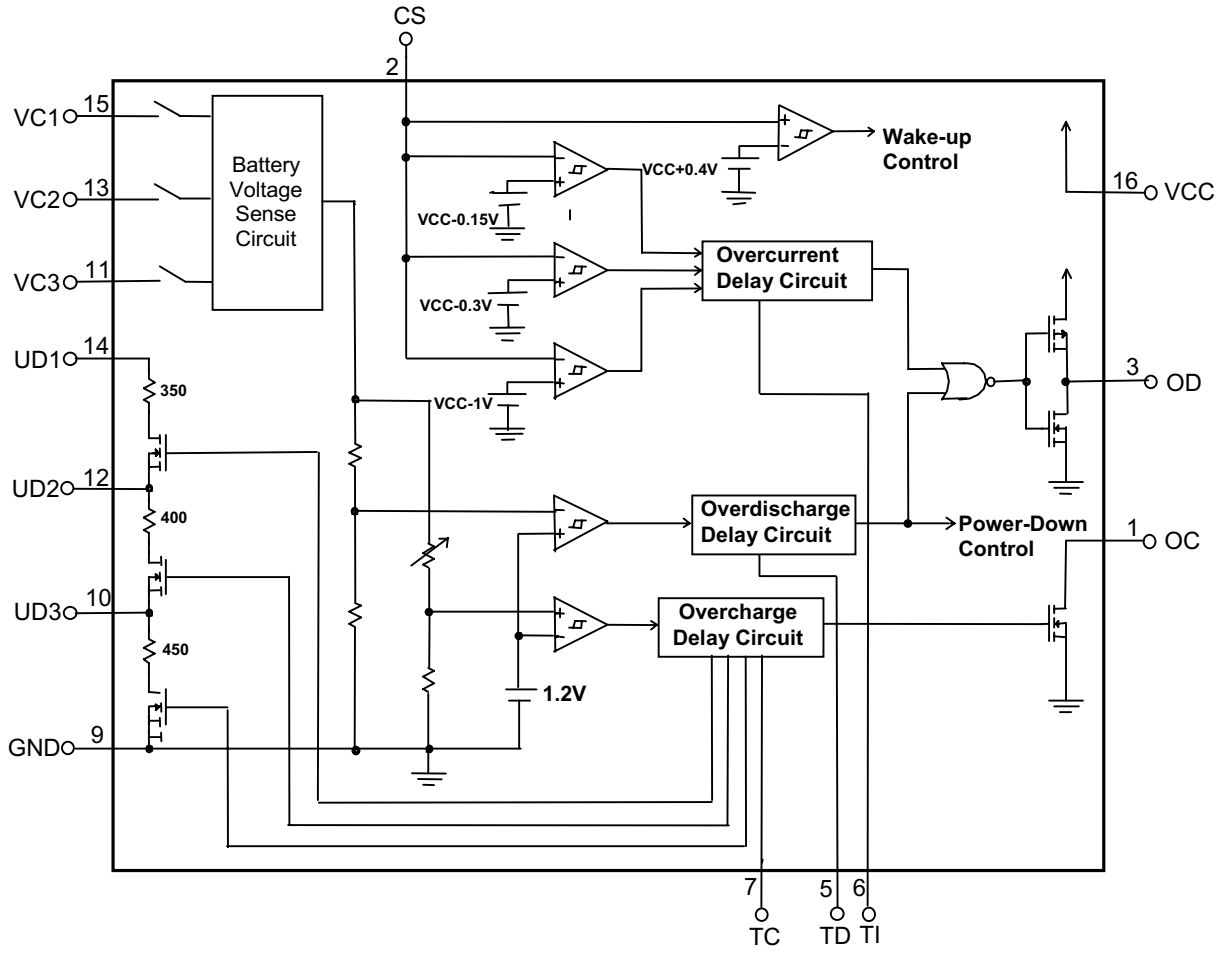


Fig. 11 Overdischarge Release Voltage vs. Temperature

BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN 1: OC- NMOS open drain output for control of the charge control MOSFET M2. When overcharge occurs, this pin sinks current to switch the external PNP Q1 on, and charging is inhibited by turning off the charge control MOSFET M2.

PIN 2: CS- Input pin for current sensing. Using the drain-source voltage of the discharge control MOSFET M1 (voltage between VCC and CS), it senses discharge current during normal mode and detects whether charging current is present during power-down mode.

PIN 3: OD - Output pin for control of discharge control MOSFET M1. When overdischarge occurs, this pin goes high to turn off the discharge control MOSFET M1 and discharging is inhibited.

PIN 4: NC - No connection

PIN 5: TD- Overdischarge delay time setting pin.

PIN 6: TI - Overcurrent delay time setting pin.

PIN 7: TC - Overcharge delay time setting pin.

PIN 8: NC - No connection.

PIN 9: GND - Ground pin. This pin is to be connected to the negative terminal of the battery cell BAT3.

PIN10: UD3 - This pin is to be connected to the positive terminal of the battery cell BAT3 for cell-balancing bleeding function under overcharge condition.

PIN11: VC3- Input pin for battery BAT3 voltage sensing. This pin is to be connected to the positive terminal of the battery cell BAT3.

PIN12: UD2 - This pin is to be connected to the positive terminal of the battery cell BAT2 for cell-balancing bleeding function under overcharge condition.

PIN13: VC2- Input pin for battery BAT2 voltage sensing. This pin is to be connected to the positive terminal of the battery cell BAT2.

PIN14: UD1- This pin is to be connected to the positive terminal of the battery BAT1 for cell-balancing bleeding function under overcharge condition.

PIN15: VC1- Input pin for battery BAT1 voltage sensing. This pin is to be connected to the positive terminal of the battery cell BAT1.

PIN16: VCC - Power supply pin. This pin is to be connected to the positive terminal of the battery cell BAT1.

APPLICATION INFORMATION

Operation

Initialization

On initial power-up, such as connecting the battery pack for the first time to the SS-6803 , the SS6803 enters the power-down mode . A charger must be applied to the SS6803 circuit to enable the pack.

Overcharge Protection

When the voltage of either of the battery cells exceeds the overcharge protection voltage (V_{OCP}) beyond the overcharge delay time (T_{OC}) period, charging is inhibited by the turning-off of the charge control MOSFET M2. The overcharge

delay time is set by the external capacitor C_{TC} Inhibition of charging is immediately released when the voltage of the overcharged cell becomes lower than overcharge release voltage (V_{OCR} or V_{OCP}-V_{HYS}) through discharging.

Overdischarge Protection

When the voltage of either of the battery cells falls below the overdischarge protection voltage (V_{ODP}) beyond the overdischarge delay time (T_{OD}) period, discharging is inhibited by the turning-off of the discharge control MOSFET M1. The overdischarge delay time is set by the external capacitor C_{TD}. Inhibition of discharging is immediately released when the voltage of the overdischarge cell becomes higher than the overdischarge release voltage (V_{ODR}) through charging.

Overcurrent Protection

In normal mode, the SS6803 continuously monitors the discharge current by sensing the voltage of CS pin. If the voltage V_{CC}-V_{CS} exceeds the overcurrent protection voltage (V_{OIP}) beyond the overcurrent delay time (T_{OI}) period, the overcurrent protection circuit operates and discharging is inhibited by the turning-off of the discharge control MOSFET M1. Discharging must be inhibited for at least 256mS after overcurrent takes place to avoid damage to external control MOSFETs due to rapidly switching transient between BATT+ and BATT- terminals. The overcurrent condition returns to normal mode when the load is released and the impedance between the BATT+ and BATT- terminals is 20MΩ or higher.

The SS6803 is provided with the three overcurrent detection levels (0.15V, 0.3V and 1.0V) and the three overcurrent delay time (T_{OI1}, T_{OI2} and T_{OI3}) corresponding to each overcurrent detection level. T_{OI1} is set by the external capacitor C_{TI}. T_{OI2} and T_{OI3} default to 4ms and 300µs respectively, and can not be adjusted due to protection of external MOSFETs

Cell-Balancing Bleeding after Overcharge

When either of the battery cells is overcharged, the SS6803 provides the cell-balancing bleeding function to discharge the overcharged cell at about 9mA until the voltage of the overcharged cell decreases to overcharge release voltage (V_{OCR} or V_{OCP}-V_{HYS}). This function is accomplished by connecting UD1, UD2, UD3 pins to the positive terminals of battery cells BAT1, BAT2, BAT3 respectively. The bleeding current can be decreased by inserting resistors along UD1 pin to BAT1 positive terminal path and UD3 pin to BAT3 positive terminal path.

Power-Down after Overdischarge

When overdischarge occurs, the SS-6803 will go into power-down mode, turning off all the timing generation and detection circuitry to reduce the quiescent current to about 1.3µA (V_{CC}=6.9V). In the unusual case where one battery cell is overdischarged while another one under overcharge condition, the SS6803 will turn off all the detection circuitry except the overcharge detection circuit for the cell under overcharge condition.

Charge Detection after Overdischarge

When overdischarge occurs, the discharge control MOSFET M1 turns off and discharging is inhibited. However, charging is still permitted through the parasitic diode of M1. Once the charger is connected to the battery pack, the SS6803 immediately turns on all the timing generation and detection circuitry and goes into normal mode. Charging is determined to be in progress if the CS

pin voltage is higher than VCC + 0.4V (charge detection threshold voltage V_{CH}).

Design Guide

Setting the Overcharge and Over-discharge Delay Time

The overcharge delay time is set by the external capacitor C_{TC} and the overdischarge delay time is set by the external capacitor C_{TD}. The relationship between capacitance of the external capacitors and delay time is tabulated as below.

C_{TC} ,C_{TD}(F)	1n	5n	10n	22n	33n
T_{OC} ,T_{OD}(S)	21m	52m	132m	253m	347m

C_{TC} ,C_{TD}(F)	47n	68n	82n	100n
T_{OC} ,T_{OD}(S)	617m	748m	1004m	1630m

The delay time can also be approximately calculated by the following equations (if C_{TC} , C_{TD} ≤ 82nF) :

$T_{OC}(mS) = 11.8 \times C_{TC}(nF)$

$T_{OD}(mS) = 11.8 \times C_{TD}(nF)$

Setting the Overcurrent Delay Time 1

The overcurrent delay time 1 (T_{OI1}) at 0.15V < V_{CC}-V_{CS} < 0.3V is set by the external capacitor C_{TI}, while the overcurrent delay time 2 and 3 (T_{OI2} and T_{OI3}) is fixed by IC internal circuit.The relationship between capacitance of the external capacitor and delay time is tabulated as below.

C_{TI}(F)	1n	2.2n	3.3n	5n	6.8n	10n
T_{OI}(ms)	4.8	15.0	18.8	23.6	31.0	61.8

Selection of External Control MOSFETs

Because the overcurrent protection voltage is preset, the threshold current for overcurrent detection is determined by the turn-on resistance of the discharge control MOSFET M1. The turn-on resistance of the external control MOSFETs can be determined by the equation: $R_{ON}=V_{OIP}/I_T$ (I_T is the overcurrent threshold current). For example, if the overcurrent threshold current I_T is designed to be 5A, the turn-on resistance of the external control MOSFETs must be 30mΩ. Users should be aware that turn-on resistance of the MOSFET changes with temperature variation due to heat dissipation. It changes with the voltage between gate and source as well. (Turn-on resistance of a MOSFET increases as the voltage between gate and source decreases). Once the turn-on resistance of the external MOSFET changes, the overcurrent threshold current will change accordingly.

Suppressing the Ripple and Disturbance from Charger

To suppress the ripple and disturbance from charger, connecting R1 to R4 and C1 to C4 is recommended.

Controlling the Charge Control MOSFET

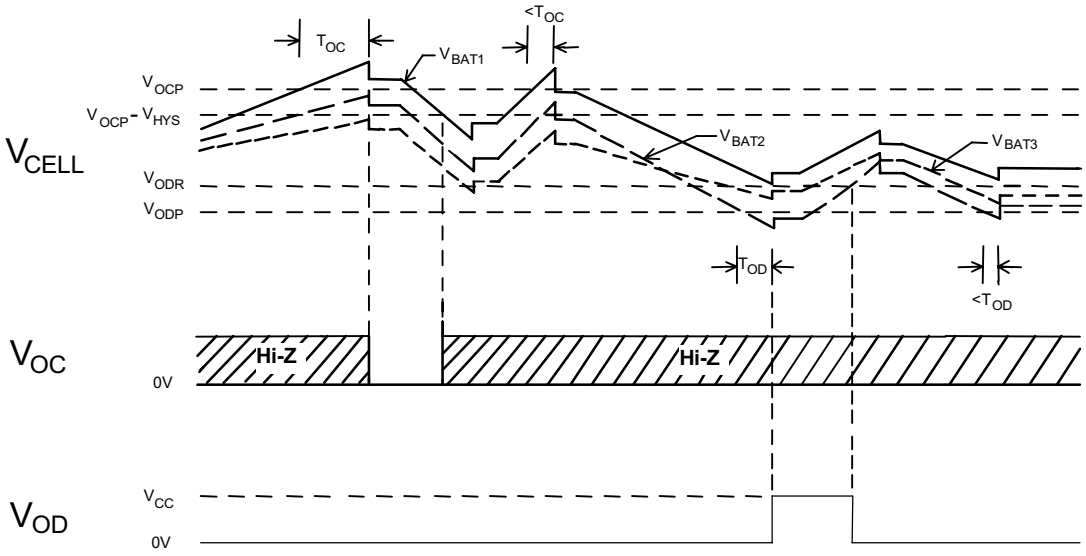
R5, R6, R7 and NPN transistor Q1 are used to switch the charge control MOSFET M2. If overcharge does not occur, no current flows into OC pin and Q1 is turned off, then M2 is turned on. When overcharge occurs, current flows into OC pin and Q1 is turned on, which turns off M2 in turn.

Protection at CS Pin

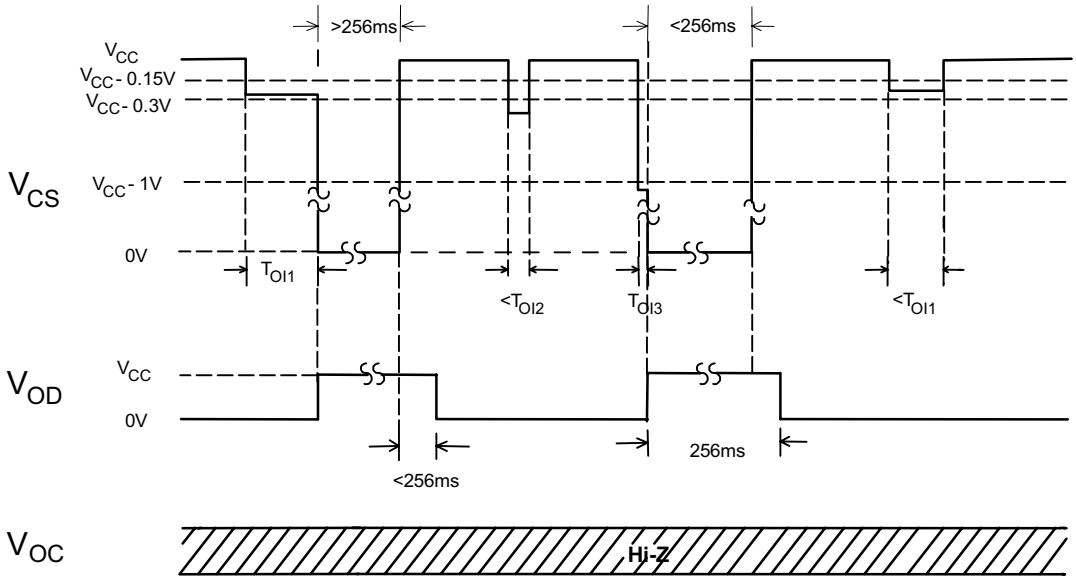
R8 is used for protection of IC when charger is connected in reverse. The charge detection function after overdischarge is possibly disabled by larger value of R8. Resistance of 1KΩ is recommended.

TIMING DIAGRAM

Overcharge and Overdischarge Protection (V_{CS}=V_{CC})

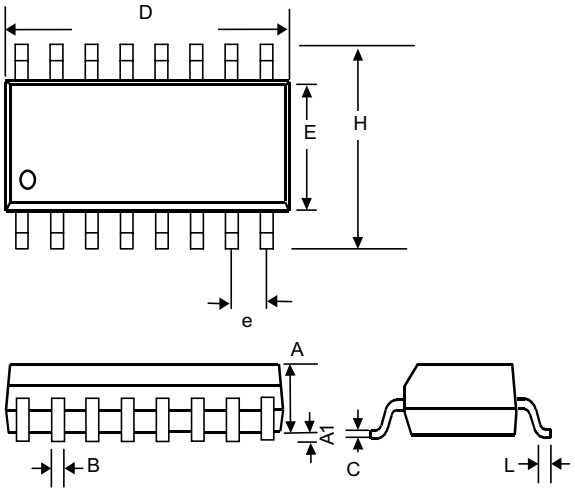


Overcurrent Protection (V_{CELL}=3.5V)



PHYSICAL DIMENSIONS

16 LEAD PLASTIC SO (150 mil) (unit: mm)



SYMBOL	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	9.80	10.00
E	3.80	4.00
e	1.27 (TYP)	
H	5.80	6.20
L	0.40	1.27